| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| COST ($ in Millions) | All Prior Years | FY 2012 | FY 2013# | FY 2014 Base | FY 2014 OCO ## | FY 2014 Total | FY 2015 | FY 2016 | FY 2017 | FY 2018 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | - | 216.102 | 222.416 | 243.469 | - | 243.469 | 254.104 | 253.843 | 245.305 | 244.425 | Continuing | Continuing |
| ELT-01: *ELECTRONICS TECHNOLOGY* | - | 216.102 | 222.416 | 243.469 | - | 243.469 | 254.104 | 253.843 | 245.305 | 244.425 | Continuing | Continuing |

# FY 2013 Program is from the FY 2013 President's Budget, submitted February 2012

## The FY 2014 OCO Request will be submitted at a later date

**A. Mission Description and Budget Item Justification**

This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices.

This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| B. Program Change Summary ($ in Millions) | FY 2012 | FY 2013 | FY 2014 Base | FY 2014 OCO | FY 2014 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 215.178 | 222.416 | 222.218 | - | 222.218 |
| Current President's Budget | 216.102 | 222.416 | 243.469 | - | 243.469 |
| Total Adjustments | 0.924 | 0.000 | 21.251 | - | 21.251 |
| • Congressional General Reductions | 0.000 | 0.000 | | | |
| • Congressional Directed Reductions | 0.000 | 0.000 | | | |
| • Congressional Rescissions | 0.000 | 0.000 | | | |
| • Congressional Adds | 0.000 | 0.000 | | | |
| • Congressional Directed Transfers | 0.000 | 0.000 | | | |
| • Reprogrammings | 6.788 | 0.000 | | | |
| • SBIR/STTR Transfer | -5.864 | 0.000 | | | |
| • TotalOtherAdjustments | - | - | 21.251 | - | 21.251 |

**Change Summary Explanation**

FY 2012: Increase reflects internal below threshold reprogrammings offset by reductions for the SBIR/STTR transfer.

FY 2014: Increase reflects expansion of efforts to build true systems on a chip that will dramatically reduce the size, weight and volume for a wide array of DoD systems.

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| ***Title:*** Terahertz Electronics | 15.667 | 17.250 | 15.020 |

***Description:*** Terahertz Electronics is developing the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits for electronics operating in the THz regime and multiple new applications in imaging, radar, communications, and spectroscopy. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules.

***FY 2012 Accomplishments:***

- Continued the development of device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz.
- Developed key device, integration, and metrology technologies to enable the manufacture of microsystems, such as heterodyne detectors, between 0.67 and 1.03 THz for advanced communications and radar applications at sub-millimeter wave frequencies.

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrated useful output power of a high power amplifier at 0.85 THz and measured integrated circuits with performance above 0.8 THz.<br>***FY 2013 Plans:***<br>- Achieve key device and integration technologies to realize compact, high performance electronic circuits operating beyond 1.03 THz.<br>- Complete the development of device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz.<br>- Complete device, integration, and metrology technologies to enable the manufacture of microsystems, such as heterodyne detectors, between 0.67 and 1.03 THz for advanced communications and radar applications at sub-millimeter wave frequencies.<br>- Initiate multiple circuit implementations for applications between 0.67 THz and 1.03 THz, including passive structures required for signal handling at sub-mm-wave frequencies.<br>- Develop measurement techniques for verifying circuit capability above 0.85 THz and calibrate these methods in a laboratory environment.<br>- Demonstrate receiver/exciter technology for sensor applications requiring coherent processing.<br>***FY 2014 Plans:***<br>- Complete circuit demonstrations between 0.67 THz and 1.03 THz, including high power amplifiers and integrated circuits.<br>- Complete measurements of receiver/exciter technologies above 0.67 THz.<br>- Demonstrate heterodyne detection and sensor capability at THz frequencies. | | | |
| ***Title:*** Adaptive Radio Frequency Technology (ART)<br>***Description:*** There is a critical ongoing military need for flexible, affordable, hand-held cognitive military electromagnetic interfaces. The Adaptive Radio Frequency Technology (ART) program will provide the warfighter with a new, fully adaptive radio platform capable of sensing the electromagnetic and waveform environment in which it operates, making decisions on how to best communicate in that environment, and rapidly adapting its hardware to meet ever-changing requirements, while simultaneously significantly reducing the size, weight and power (SWaP) of such radio nodes. ART will also equip each warfighter, as well as small-scale unmanned platforms, with compact and efficient signal identification capabilities for next-generation cognitive communications, sensing and electronic warfare applications. ART technology will also enable rapid radio platform deployment for new waveforms and changing operational requirements. The project will remove the separate design tasks needed for each unique RF system, which will dramatically reduce the procurement and sustainment cost of military systems. ART aggregates the Feedback Linearized Microwave Amplifiers program, the Analog Spectral Processing program, and Chip Scale Spectrum Analyzers (CSSA) program, and initiates new thrusts in Cognitive Low-energy Signal Analysis and Sensing Integrated Circuits (CLASIC), Radio-Frequency Field-Programmable Gate Arrays (RF-FPGA), and Dynamic Live Active Nulling (DyLAN). | 26.622 | 27.702 | 26.949 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| ***FY 2012 Accomplishments:***<br>- Completed development of feedback-linearized InP Heterojunction Bipolar Transition (HBT) monolithic low-noise amplifiers with improved third-order-intercept point and noise figure for potential transition to signal intelligence and electronic warfare platform applications.<br>- Completed development of feedback-linearized amplifier approaches to analog/RF applications such as high-speed/high dynamic range sample-and-holds and active impedance matching of electrically small antennas, and developed an integrated field-effect-transistor switch process in support of these applications.<br>- Completed development of InP high electron mobility transistor material structure with 0.5-m gate lengths and achieved > 10 V FET breakdown voltage.<br>- Continued development of novel signal recognition sensor algorithms and integrated circuits that can achieve >400 times reduction in signal recognition energy as compared to state-of-the-art sensor systems. Demonstrated concepts for signal recognition at the simulation level and initiated plans for realization of these techniques in hardware.<br>- Initiated development of reconfigurable RF circuit (RF-FPGA) technologies capable of adapting in the field to at least five wireless RF standards. Development is proceeding along three thrusts: adaptive component technologies, reconfigurable systems, and computer-aided design.<br>- Demonstrated MEMS-based resonators with world-record frequency quality-factor product for RF channelization. | | | |
| ***FY 2013 Plans:***<br>- Initiate development of RF signal cancellation concepts which will actively eliminate unwanted signals within a receiver without the need for large and typically static passive filtering.<br>- Demonstrate Highly linear Time Delay Unit (TDU) Monolithic Microwave Integrated Circuit (MMIC) for beam-steering applications in wideband phased arrays.<br>- Demonstrate MEMS-based channelized RF receiver topology for use in high-speed spectrum sensing applications<br>- Continue development of novel signal recognition sensor integrated circuits. Demonstrate initial hardware implementations of developed signal recognition concepts/techniques.<br>- Continue development of reconfigurable RF circuit (RF-FPGA) technologies. | | | |
| ***FY 2014 Plans:***<br>- Continue development of integrated cancellation circuits for the purpose of RF filter replacement in low-SWaP military radios and signal intelligence platforms.<br>- Demonstrate reconfigurable RF circuit (RF-FPGA) technologies at the component and system levels along with the necessary computer-aided design approaches.<br>- Demonstrate the applicability of one piece of RF hardware for 5 different application spaces, as a prototype of how research can lead the way to life cycle cost reduction. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate concepts for signal recognition at the hardware level and initiate plans for transitioning these approaches to relevant DoD systems. | | | |
| ***Title:*** Nitride Electronic NeXt-Generation Technology (NEXT) | 11.200 | 10.360 | 11.870 |
| ***Description:*** The objective of the Nitride Electronic NeXt-Generation Technology (NEXT) program is to develop a revolutionary nitride transistor technology that simultaneously provides extremely high-speed and high-voltage swing [Johnson Figure of Merit (JFoM) larger than 5 Terahertz (THz)-V] in a process consistent with large scale integration in enhancement/depletion (E/D) mode logic circuits of 1000 or more transistors. In addition, this fabrication process will be manufacturable, high-yield, high-uniformity, and highly reliable. The accomplishment of this goal will be validated through the demonstration of specific Program Process Control Monitor (PCM) Test Circuits such as 5, 51, and 501-stage of ring oscillators in each program phase. | | | |
| ***FY 2012 Accomplishments:***<br>- Improved scaling efforts for self-aligned structures with short gate length, novel barrier layers and reduced parasitic elements to achieve additional cutoff frequency performance gains.<br>- Completed transistor performance trade-space analysis to achieve ultra-fast power switching capability.<br>- Continued development of an optimized enhancement mode power switch process to complement the high frequency field effect transistors (FET) process.<br>- Established an integrated process for power switching and Microwave Monolithic Integrated Circuit (MMIC) capability using advanced wide band gap devices.<br>- Increased passive element performance of MMIC process utilizing both enhancement and depletion mode devices.<br>- Initiated development of complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes. | | | |
| ***FY 2013 Plans:***<br>- Continue development of complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes.<br>- Complete scaling efforts for self-aligned structures with short gate length, novel barrier layers and reduced parasitic elements to achieve additional cutoff frequency performance gains.<br>- Increase the Technology Readiness Level (TRL) of the integrated process for power switching and Microwave Monolithic Integrated Circuit (MMIC) capability using advanced wide band gap devices.<br>- Continue to increase passive element performance of MMIC process utilizing both enhancement and depletion mode devices. | | | |
| ***FY 2014 Plans:***<br>- Demonstrate monolithic integration of mixed signal and power amplifier circuits. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Complete final demonstrations of complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes.<br>- Complete final E/D mode transistor scaling for fully self-aligned nitride transistors with full process compatibility. | | | |
| ***Title:*** Diverse & Accessible Heterogeneous Integration (DAHI) | 15.500 | 28.100 | 33.584 |
| ***Description:*** Prior DARPA efforts have demonstrated the ability to monolithically integrate inherently different semiconductor types to achieve near-ideal "mix-and-match" capability for DoD circuit designers. Specifically, the Compound Semiconductor Materials On Silicon (COSMOS) program, in which transistors of Indium Phosphide (InP) could be freely mixed with silicon complementary metal-oxide semiconductor (CMOS) circuits to obtain the benefits of both technologies (very high speed and very high circuit complexity/density, respectively). The Diverse & Accessible Heterogeneous Integration (DAHI) effort will take this capability to the next level, ultimately offering the seamless co-integration of a variety of semiconductor devices (for example, Gallium Nitride, Indium Phosphide, Gallium Arsenide, Antimonide Based Compound Semiconductors), microelectromechanical (MEMS) sensors and actuators, photonic devices (e.g., lasers, photo-detectors) and thermal management structures. This capability will revolutionize our ability to build true "systems on a chip" (SoCs) and allow dramatic size, weight and volume reductions for a wide array of system applications.<br><br>In the Applied Research part of this program, high performance RF/optoelectronic/mixed-signal SoCs for specific DoD transition applications will be developed as a demonstration of the DAHI technology. In addition, in order to provide maximum benefit to the DoD, as these processes are developed, they will be transferred to a manufacturing flow and made available (with appropriate computer aided design support) to a wide variety of DoD laboratory, FFRDC, academic and industrial designers. Manufacturing yield and reliability of the DAHI technologies will be characterized and enhanced. This program has basic research efforts funded in PE 0601101E, Project ES-01, and advanced technology development efforts funded in PE 0603739E, Project MT-15.<br><br>***FY 2012 Accomplishments:***<br>- Completed design of advanced heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converters with in situ silicon enabled calibration and linearization.<br>- Completed design and initiated fabrication of higher complexity new generation of heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converters with in situ silicon enabled calibration and linearization.<br>- Continued multi-user compound-semiconductor on silicon foundry process, which will ultimately be accessible to the wider defense and commercial integrated circuit design community. Completed fabrication of first multi-project wafer run, and initiated fabrication for second multi-project wafer run.<br>- Initiated design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, including ultra-low noise lasers, optoelectronic RF signal sources, and imaging array chips.<br><br>***FY 2013 Plans:*** | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Complete fabrication and testing of advanced heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converters with in situ silicon enabled calibration and linearization.<br>- Complete fabrication and testing of higher complexity new generation of heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converters with in situ silicon enabled calibration and linearization.<br>- Continue multi-user compound-semiconductor on silicon foundry process, which will ultimately be accessible to the wider defense and commercial integrated circuit design community. Complete fabrication of second multi-project wafer run, and initiate and complete fabrication of third and fourth multi-project wafer runs.<br>- Initiate new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.<br>- Initiate manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.<br>- Continue design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, optoelectronic RF signal sources, and laser radar and imaging array chips.<br>***FY 2014 Plans:***<br>- Continue new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.<br>- Continue manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.<br>- Continue design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, optoelectronic RF signal sources, and laser radar systems. | | | |
| ***Title:*** Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) | 12.116 | 18.201 | 23.396 |
| ***Description:*** The Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) program is developing technology for self-contained chip-scale inertial navigation and precision guidance. This technology promises to effectively mitigate dependence on Global Positioning System (GPS) or any other external signals, and enable uncompromised navigation and guidance capabilities. The program will enable positioning, navigation and timing functions without the need for external information updates by employing on-chip calibration, thereby overcoming vulnerabilities which arise in environments where external updates are not available such as caves, tunnels, or dense urban locations. The technologies developed will enable small, low-power, micro-gyroscopes capable of operating in both moderate and challenging dynamic environments; chip-scale primary atomic clock standards; and on-chip calibration systems for error correction. Advanced micro-fabrication techniques allow a single package containing all the necessary devices (clocks, accelerometers, gyroscopes, and calibration mechanisms) to be incorporated into | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|

a volume the size of a sugar cube. The small size, weight and power of these technologies and their integration into a single package responds to the needs of guided munitions, unmanned aerial vehicles (UAVs) and individual soldiers.

The successful realization of a Micro PN&T device is dependent on developing fundamentally new batch microfabrication processes, gaining an understanding of the sources and effects of error at the micro-scale, and exploring new combinatorial physics. Innovative 3-D microfabrication techniques will allow co-fabrication of different materials and devices on a single chip. Clocks, gyroscopes, accelerometers, calibration stages, and 3D structures could be integrated into a small, low power architecture. This co-location of different inertial and timing devices opens the possibility for utilization of combinatorial physics in a single micro-system, enabling fast start-up time, increased bandwidth and long-term stability, thus effectively providing very accurate navigation devices. Advanced research for the program is budgeted in PE 0603739E, Project MT-12.

***FY 2012 Accomplishments:***

- Demonstrated co-fabrication of clocks and inertial sensors into an all silica package smaller than ten cubic millimeters, leveraging the high-quality factor mechanical properties of this material.
- Demonstrated silicon dioxide micro-Hemispherical Resonating Gyro with a frequency mismatch of 6 Hertz.
- Demonstrated a compact Nuclear Magnetic Resonance (NMR) gyroscope with scale factor instability below 8.7 ppm Root Mean Square (RMS), better than the program goal of 50 ppm. Demonstrated rotation rates up to 2500 degrees per second, greater than program goal of 500 degrees per second.

***FY 2013 Plans:***

- Develop monolithic microfabrication process to co-integrate clock, accelerometers and gyroscopes into small form factor.
- Demonstrate the technique for error correction of an inertial sensor on an integrated calibration stage.
- Explore and develop predictive models of error sources for gyroscope and accelerometers.
- Identify physical and algorithmic self-calibration techniques to compensate for stability and drift of inertial sensors.
- Develop turn-key software and provide extended testing results from an NMR gyroscope.
- Demonstrate new algorithmic approaches to improve performance by using complimentary acceleration and rotation measurement techniques.

***FY 2014 Plans:***

- Demonstrate a physical structure and architecture of an inertial sensor capable of near navigation-grade performance.
- Demonstrate architecture for co-integrated clock, accelerometers, and gyroscope on a small single platform with a volume of less than ten cubic millimeters.
- Use predictive error models for on-chip calibration of gyroscopes and accelerometers.
- Explore new physics for chip-scale combinatorial atomic navigator and determine fundamental limits of the microtechnology.

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Develop architectures and algorithms to enable reduced startup time for atomic inertial devices. | | | |
| ***Title:*** Advanced X-Ray Integrated Sources (AXIS) | 4.500 | 9.500 | 9.450 |
| ***Description:*** The objective of the Advanced X-Ray Integrated Sources (AXIS) program is to develop tunable, mono-energetic, spatially coherent X-ray sources with greatly reduced size, weight and power while dramatically increasing their electrical efficiency through application of micro-scale engineering technologies such as MEMS and NEMS. Such X-ray sources will enable new versatile imaging modalities based on phase contrast techniques which are 1000X more sensitive than the conventional absorption contrast imaging. Such imaging modalities should enable reverse engineering of integrated circuits to validate trustworthiness as well as battlefield imaging of soft tissues and blood vessel injuries from blunt trauma without the injection of a contrast enhancing agent. The radiation dose required for imaging will also be reduced.<br><br>The Applied Research component of this effort will focus on applying basic research discoveries to the development of a compact, pulsed X-ray source. Such sources are a necessary component to enable future technologies with high-speed motion imaging capabilities and the reverse engineering of integrated circuits. This program also includes related basic research efforts funded under PE 0601101E, Project ES-01.<br><br>***FY 2012 Accomplishments:***<br>- Developed advanced designs for compact and energy-efficient X-ray sources that are spectrally tunable and have narrow energy width.<br>- Developed a coded array of micro-focused X-ray sources for phase contrast imaging.<br>- Designed and evaluated the performance potential of a short-lifetime photoconductor switched tip-on-post (Spindt) field emitter.<br>- Developed concepts and demonstrated components of a miniaturized wafer-scale electron accelerator and electron storage ring.<br>- Investigated the feasibility of an advanced hard X-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and high-gain material.<br>- Demonstrated the feasibility of 50X higher spatial resolution using phase contrast computed tomography (CT) of soft tissues; and achieved 10X increase of the contrast resolution in tissue discrimination.<br><br>***FY 2013 Plans:***<br>- Fabricate and demonstrate a short-lifetime photoconductor switched tip-on-post (Spindt) field emitter with short pulse duration, high pulse repetition rate, and low emittance.<br>- Begin fabrication of an advanced hard X-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and gain. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Coordinate the development of devices capable of producing synchrotron-quality X-rays by integrating the most successful components (cathodes, accelerators, undulators & lasers) in the program.<br>***FY 2014 Plans:***<br>- Demonstrate an advanced hard X-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and gain.<br>- Demonstrate a flat panel x-ray panel based on coded array of micro-focused X-ray sources for phase contrast imaging.<br>- Successfully demonstrate a compact, low-power device capable of generating phase contrast images. | | | |
| ***Title:*** Microscale Plasma Devices (MPD)<br>***Description:*** The goal of the Microscale Plasma Devices (MPD) program is to design, develop, and characterize MPD technologies, circuits, and substrates. The MPD program will focus on development of fast, small, reliable, carrier dense, microplasma switches capable of operating in extreme conditions such as high-radiation and high-temperature environments. Specific focus will be given to methods that produce efficient, high-pressure (up to or even beyond atmospheric pressure) generation of ions, radio frequency energy, and light sources. Applications for such devices are far reaching, including the construction of complete high-frequency plasma-based logic circuits, and integrated circuits with superior resistance to radiation and extreme temperature environments. It is envisaged that both two and multi-terminal devices consisting of various architectures will be developed and optimized under the scope of this program. MPDs will be developed in various circuits and substrates to demonstrate the efficacy of different unique approaches.<br><br>The MPD applied research program is focused on transferring the fundamental scientific advances funded by PE 0601101E, Project ES-01 to produce complex circuit designs that may be integrated with commercial electronic devices. It is expected that the MPD program will result in the design and modeling tools, as well as the fabrication capabilities necessary to commercially manufacture high-performance microscale-plasma-device-based electronic systems for advanced DoD applications.<br><br>***FY 2012 Accomplishments:***<br>- Completed initial circuit demonstrations necessary for DoD-relevant high-performance microplasma electronics.<br>- Began microplasma modeling and simulation efforts for development of the modeling and simulation design tools (MSDT).<br>- Completed first prototypes of microplasma electronics required for a complete radiation-hardened RF system.<br>- Demonstrated initial development of a microcavity-plasma-based material capable of passively protecting against high power electromagnetic (microwave) pulses while embedded into complex substrates.<br>- Initiated development of fundamental nonlinear signal processing architectures and circuit concepts for use in demonstration of microscale plasma device (MPD) technology.<br>***FY 2013 Plans:*** | 6.390 | 7.816 | 8.500 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Verify microplasma modeling simulation results against microscale plasma device measurement results to begin optimization of the microplasma modeling and simulation design tool (MSDT) for commercial development of microplasma-based electronics.<br>- Determine feasibility of light absorption and switching utilizing microscale plasmas.<br>- Begin development of a full microplasma-electronics-based radiation-hardened RF system.<br>- Investigate the use of microscale plasma devices for protection of sensing and imaging systems in extreme environments.<br>- Initial field testing of the passive microcavity metamaterial for high power microwave protection.<br>***FY 2014 Plans:***<br>- Complete integration of the simulation efforts into the modeling and simulation design tool (MSDT) for commercial development of microplasma based electronics.<br>- Complete fabrication and begin testing of full microplasma-based radiation-hardened RF system including tunable antenna.<br>- Optimize plasma microcavity material for DoD systems of interest, demonstrating protection from high power electromagnetic radiation.<br>- Demonstrate and test nonlinear signal processing circuit concepts and architectures based on microscale plasma device (MPD) technologies. | | | |
| ***Title:*** IntraChip Enhanced Cooling (ICECool)<br>***Description:*** The IntraChip Enhanced Cooling program is exploring disruptive technologies that will remove thermal barriers to the operation of military electronic systems, while significantly reducing size, weight, and power consumption. These thermal barriers will be removed by integrating thermal management into the chip, substrate, or package technology. Successful completion of this program will close the gap between chip-level heat generation density and system-level heat removal density in RF arrays and embedded computers.<br><br>Specific areas of focus in this program include overcoming limiting evaporative and diffusive thermal transport mechanisms at the micro/nano scale to provide an order-of-magnitude increase in on-chip heat flux and heat removal density , determining the feasibility of exploiting these mechanisms for intrachip thermal management, characterizing the performance limits and physics-of-failure of high heat density, intrachip cooling technologies, and integrating chip-level thermal management techniques into prototype high power electronics in the form factor of RF arrays and embedded computing systems.<br>***FY 2013 Plans:***<br>- Determine feasibility of implementing advanced thermal management techniques into compact defense electronic systems.<br>- Determine limits of advanced thermal technologies through fundamental studies on intra and interchip cooling.<br>- Initiate efforts to apply intra and interchip cooling as part of the thermal management approach of defense electronic systems.<br>***FY 2014 Plans:*** | 0.000 | 11.000 | 21.500 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate proof of concept of fundamental building blocks of intrachip thermal management including microfabrication in relevant electronic substrates and preliminary thermofluid results.<br>- Prepare and refine initial thermal models of intrachip cooling to explain and predict experimental results.<br>- Demonstrate benefits to system-level performance and size, weight, power, and cost (SWaPC) through the use of intrachip thermal management technologies. | | | |
| ***Title:*** In vivo Nanoplatforms (IVN)<br><br>***Description:*** The In vivo Nanoplatforms (IVN) program seeks to develop the nanoscale systems necessary for in vivo sensing and physiologic monitoring and delivery vehicles for targeted biological therapeutics. The nanoscale components to be developed will enable continuous in vivo monitoring of both small (e.g. glucose, lactate, and urea) and large molecules (e.g. biological threat agents). A reprogrammable therapeutic platform will enable tailored therapeutic delivery to specific areas of the body (e.g. cells, tissue, compartments) in response to traditional, emergent, and engineered threats. The key challenges to developing these systems include safety, toxicity, biocompatibility, sensitivity, response, and targeted delivery. The IVN program will have diagnostic and therapeutic goals that enable a versatile, rapidly adaptable system to provide operational support to the warfighter in any location.<br><br>***FY 2013 Plans:***<br>- Achieve a safe in vivo nanoplatform sensor to detect one military-relevant analyte (e.g. glucose) in living cells for one month.<br>- Achieve a safe in vivo nanoplatform therapeutic to reduce a military-relevant pathogen or disease cofactor in living cells by 50%.<br>- Facilitate development of a regulatory approval pathway for diagnostic and therapeutic nanoplatforms.<br><br>***FY 2014 Plans:***<br>- Achieve a safe in vivo nanoplatform sensor to detect two military-relevant analytes (e.g. glucose, pathogen) in a small animal for six months.<br>- Achieve a safe in vivo nanoplatform therapeutic to reduce a military-relevant pathogen or disease cofactor in a small animal by 70%.<br>- Begin to obtain regulatory approval of identified safe and effective diagnostic and therapeutic nanoplatforms. | 0.000 | 5.000 | 18.500 |
| ***Title:*** Pixel Network (PIXNET) for Dynamic Visualization<br><br>***Description:*** The Pixel Network for dynamic visualization (PIXNET) program addresses the squad level capability gap for target detection, recognition and identification in all weather and day/night missions. The vision of the program is to offer the warfighter a small and versatile infrared (IR) camera that would be affordable to individual soldiers and provide multiple IR band imagery with fusion capability to take full advantage of different wavelength band phenomenology in a compact single unit. In the future, the availability of the PIXNET camera would enable a peer-to-peer networked system for image sharing within a squad, thereby providing a better common operating picture of the battlefield and significantly enhancing the warfighter's situational | 0.000 | 15.000 | 22.700 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|

understanding. The program aims to develop a low size, weight and power (SWaP), low cost, soldier portable multiband infrared camera that will render real-time single and multiple imagery using thermal and reflective bands. The camera will also provide fused reflective and thermal band imagery on demand. The use of fused imagery in the PIXNET design will allow the soldier to detect camouflaged targets and distinguish targets from decoys. The PIXNET camera will eliminate limitations posed by current capability to detect, recognize and identify targets in low light and no light nighttime operations.

The PIXNET program will focus on a significant reduction in SWaP and cost of infrared sensor components to enable portability and ability to deploy widely to all participants in the theater. Low-cost manufacturing of wafer scale IR sensors and coolers will provide a price point that will allow these components to be deployed to each warfighter. The emphasis on a small form-factor will naturally enable new opportunities such as surveillance with small UAVs, rifle sights with multiple bands, vehicle mounted, helmet mounted and handheld surveillance systems. The phenomenology of different infrared wavelengths will be exploited for a target of interest and only chunks of relevant data will be fused by a smart phone android processing platform, thus reducing the data burden and ease of display. The combination of a smart phone and PIXNET camera at the soldier level will enable more effective tactics, techniques and procedures (TTP) over the current capability. The PIXNET program takes advantage of the computing capability of smart phones to process and fuse multicolor images and send them as videos or still images to the warfighter's helmet mounted display via a wireless or wired connection. The smart phone and PIXNET camera integration allows for a strategy to produce low cost imaging system with single band and combined band imagery. PIXNET capability could be further exploited in the future to enable a fully networked system such as the Network Warrior integrated multiple Soldier systems capability with full spectrum image and video sharing.

***FY 2013 Plans:***

- Develop and review IR camera design and overall architecture that will demonstrate digital image data transmission and signal processing via wireless connectivity using an android based platform.
- Identify parameters required for multi-color helmet mounted technology for very low SWaP multi-color IR camera.
- Initiate novel optics materials and constructs for multi-band IR.
- Identify wireless interface protocols for rifles/weapons and helmet displays that are compliant with dismount requirements.
- Determine optimum algorithm for image fusion and image data transmission.

***FY 2014 Plans:***

- Refine algorithms to fuse data from thermal and reflective bands with good image registration.
- Establish interim small form-factor camera integration and demonstrate connectivity to heads up display and Android based platform.

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate multicolor image acquisition by interim PIXNET camera, data transmission to android platform, image fusion by android platform, and viewing of fused imagery on heads-up display. | | | |
| ***Title:*** Microscale Power Conversion (MPC) | 0.000 | 10.000 | 11.500 |
| ***Description:*** The Microscale Power Conversion (MPC) program will address the fundamental limitations of power conversion by enabling a new technology and approach that exploits advances in basic power devices that can operate at very high frequencies with low losses. A key benefit of these new devices is that they can be integrated into very compact circuits and assemblies that will provide dramatic advances to the power bus of a platform. Specifically, this program will develop the technology to enable DC to DC power conversion for military applications at the scale of an integrated circuit so it can be embedded within the electronics subsystem and a new distributed power architecture can be realized. The focus of this program is on attaining 100 Megahertz (MHz) internal operation frequencies of power circuits since the size of the passive elements (inductors and capacitors) in a power converter scales inversely as the fourth power of the internal operating frequency. In FY 2012, MPC is funded in PE 0602715E, Project MBT-03. | | | |
| ***FY 2013 Plans:***<br>- Continue development of very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers.<br>- Initiate final co-designs of advanced X-band power amplifier technologies to include drain and gate bias modulation, dynamic output impedance matching, and closed-loop control to enable fast-switching power modulation.<br>- Design and prototype second generation amplifier architectures for highly efficient handling of large peak-to-average ratio RF waveforms for military systems.<br>- Demonstrate second generation converter efficiency and losses, including co-designed power amplifiers of many classes and approaches in a laboratory environment.<br>- Fabricate low-loss packages and monolithically integrated switches for amplifier-modulator circuits of final selection. | | | |
| ***FY 2014 Plans:***<br>- Complete very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers.<br>- Demonstrate final co-designs of advanced X-band power amplifier technologies to include drain and gate bias modulation, dynamic output impedance matching, and closed-loop control to enable fast-switching power modulation.<br>- Miniaturize most promising amplifier concepts for transmit module integration feasibility.<br>- Demonstrate second generation converter efficiency and losses, including co-designed power amplifiers of many classes and approaches in a laboratory environment. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate transmission of relevant military waveforms for electronic warfare applications. | | | |
| ***Title:*** Arrays at Commercial Timescales (ACT)<br><br>***Description:*** Phased arrays are critical system components for high performance military electronics with widespread applications in communications, electronic warfare and radar. The DoD relies heavily on phased arrays to maintain technological superiority in nearly every theater of conflict. The DoD cannot update these high cost specialized arrays at the pace necessary to effectively counter adversarial threats under development using commercial-of-the-shelf components that can undergo technology refresh far more frequently. The Arrays at Commercial Timescales (ACT) program will develop adaptive and standardized digital-at-every-element arrays. The hand designed, static RF beamformers will be replaced with cost effective digital array systems capable of a yearly technology refresh. By doing so, phased arrays will become ubiquitous throughout the DoD, proliferating onto many platforms for which phased arrays had been previously prohibitively expensive to develop or maintain. The basic research component of this program is budgeted under PE 0601101E, Project ES-01.<br><br>***FY 2014 Plans:***<br>- Initiate development of common digital hardware components for phased array elements that can be seamlessly integrated into a wide range of platforms.<br>- Initiate the development of digital array systems with performance capabilities that evolve with Moore's law at commercial time scales.<br>- Initiate the development of electromagnetic (EM) interface elements capable of reconfiguring for various array use cases and operational specifications.<br>- Develop array components that can demonstrate interoperability over a wired or wireless network such that the realized performance is an integrated sum of each individual array's performance.<br>- Demonstrate reconfigurability of EM interface components for various array performance specifications and demonstrate compatibility with common digital back-end. | 0.000 | 0.000 | 18.000 |
| ***Title:*** Efficient Computing and Sensing through Optics (ECSO)<br><br>***Description:*** The Efficient Computing and Sensing through Optics program will develop a system of efficient, high-speed optical sources, waveguides, detectors and non-linear elements for parallelized computation in the optical domain. The program will deliver a device capable of low-power optical transforms and convolutions yielding efficient computation orders of magnitude faster than the state of the art. Applications include real-time network security and object identification.<br><br>***FY 2014 Plans:***<br>- Identify architectures scalable to future telecom line rates.<br>- Demonstrate real-time correlation for 8 bits at 40 Gbps. | 0.000 | 0.000 | 11.000 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate in-line discrete Fourier Transform at 40 Gbps. | | | |
| ***Title:*** Micro-coolers for Focal Plane Arrays (MC-FPA)<br><br>***Description:*** The Micro-coolers for FPAs program will develop low Size, Weight, Power, and cost (SWaP-C) cryogenic coolers for application in high performance IR cameras. The sensitivity of an IR focal-plane array (FPA) is improved by cooling its detectors to cryogenic temperatures. The disadvantages of state-of-the art Sterling cryo-coolers used for high performance IR FPAs are large size, high power and high cost. On the other hand, thermoelectric (TE) coolers used in low performance IR cameras are relatively small, high power and it is difficult to achieve temperatures below 200 K.<br><br>To reduce IR camera SWaP-C, innovations in cooler technology are needed. This program will exploit the Joule-Thompson (J-T) cooling principle, in a silicon-based MEMS technology, for making IR FPA coolers with very low SWaP-C. MEMS microfluidics, piezoelectric MEMS, and complementary metal-oxide semiconductor (CMOS) electronics will be used to demonstrate an integrated cold head and compressor, all in a semiconductor chip. Since a J-T cooler works by cooling from gas expansion, the coefficient of performance is expected to be much higher than state-of-the-art TE coolers and significantly smaller than Sterling coolers. The chip-scale J-T cooler will be designed for pressure ratios of 4 or 5 to 1 with high compressor frequency in small volume. The goal of the MC-FPA Program will be to demonstrate cooling down to 150K. The microcoolers chip-scale size will cost less and will be significantly smaller. Once the proof-of-principle is demonstrated, subsequent program effort would focus on transitioning to chip-scale manufacture on 8-12 inch wafers, resulting in cooler costs decreasing to as low as $50. An extended wavelength-range short-wave IR detector will be integrated with a micro-cooler for demonstration of the MC-FPA. The basic research component of this program is budgeted under PE 0601101E, Project ES-01.<br><br>***FY 2014 Plans:***<br>- Develop 640X480 extended shortwave infrared (1-2.4 micrometer cutoff) FPA.<br>- Design a readout integrated circuit for the IR FPA chip.<br>- Demonstrate camera electronics for the FPA with provision for chip-scale micro-cooler. | 0.000 | 0.000 | 5.000 |
| ***Title:*** Quantum Information Science (QIS)<br><br>***Description:*** The Quantum Information Science (QIS) program will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. The QIS program is a broad effort addressing the fundamental material science and physics associated with solid-state qubits. The primary technical challenges include loss of information due to quantum decoherence and the practical limitations associated with solid-state devices (operation at cryogenic temperatures, susceptibility to electronic and magnetic noise, limited coupling distance for qubit interactions, etc.). Theoretical efforts in QIS are investigating novel techniques for preserving coherence, distributing quantum entanglement, and | 4.700 | 2.350 | 0.000 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| efficiently modeling qubit operation. Complementary experiments are seeking to demonstrate qubits with better coherence properties than existing devices and to implement entangling operations between two or more solid-state qubits. Future technologies utilizing quantum information science could enable ultra-secure communications; faster algorithms for optimization and simulation in logistics, war gaming, and pharmaceutical development; and new methods for image and signal processing in measurement and signature intelligence activities (MASINT).<br><br>***FY 2012 Accomplishments:***<br>- Explored novel materials, noise characteristics and decoherence mitigation strategies for qubits.<br>- Performed detailed theoretical modeling of single and double semiconductor qubits.<br>- Demonstrated entangling operation with two semiconductor qubits and high-fidelity (>99%) readout of qubit states.<br>***FY 2013 Plans:***<br>- Improve speed and accuracy of numerical modeling of semiconductor qubit operation.<br>- Perform advanced state tomography on qubits.<br>- Demonstrate interconversion of quantum information between different qubits technologies.<br>- Demonstrate transport of quantum information over microscopic scales. | | | |
| ***Title:*** Vanishing Programmable Resources (VAPR) | 0.000 | 0.000 | 6.500 |
| ***Description:*** The Vanishing Programmable Resources (VAPR) program will create electronic systems capable of physically disappearing (either in whole or in part) in a controlled, triggerable manner. VAPR will enable a host of previously unrealizable technologies that can be programmed to disappear, are biocompatible, and/or are physically reconfigurable. Applications include sensors for conventional indoor/outdoor environments (buildings, transportation and material), environmental monitoring over large areas, and simplified diagnosis, treatment, and health monitoring in the field. The program will develop and establish an initial set of materials and components along with integration and manufacturing capabilities to undergird a fundamentally new class of electronics defined by their performance and transience. These transient electronics will perform in a manner comparable to Commercial Off-The-Shelf (COTS) systems, but with limited device persistence that can be programmed, adjusted in real-time, triggered, and/or sensitive to the environment. VAPR will provide an initial capability to make transient electronics a deployable technology for the DoD and Nation. Basic research for the VAPR program is being performed in PE 0601101E, TRS-01.<br><br>To manufacture transient systems at scale will require significant research and development into: higher levels of circuit integration and complexity to realize advanced circuit functionalities; integrated system designs to achieve required function (in modes that offer programmed or triggered transience); integration of novel materials into circuit fabrication processes; and development of new packaging strategies. The efficacy of the technological capability developed through VAPR will be demonstrated through a final test vehicle of a transient sensor system. The goal is to develop a suite of design principles, develop | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| strategies and pathways, process flows, tools and basic components that are readily generalizable and can be leveraged towards the development of many other transient electronics devices<br><br>***FY 2014 Plans:***<br>- Begin development of foundry fabrication of transient electronics with key functions (RF, memory, digital logic, power supply, etc.).<br>- Begin development of increased circuit integration and complexity to implement advanced functionalities.<br>- Begin development of transient sensors and power supply strategies.<br>- Begin development of transient device fabrication approaches.<br>- Begin demonstration of transience modes in test vehicles. | | | |
| ***Title:*** Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) | 29.555 | 12.000 | 0.000 |
| ***Description:*** The vision of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program is the development of biological-scale neuromorphic electronic systems for autonomous, unmanned, robotic systems where humans are currently the only viable option. Successful development of this technology could revolutionize warfare by providing intelligent terrestrial, underwater, and airborne systems that remove humans from dangerous environments and remove the limitations associated with today's remote-controlled robotic systems. Applications for neuromorphic electronics include not only robotic systems, but also natural human-machine interfaces and diverse sensory and information integration applications in the defense and civilian sectors. If successful, the program will also reinvigorate the maturing microelectronics industry by enabling a plethora of computer and consumer electronics applications.<br><br>***FY 2012 Accomplishments:***<br>- Designed and simulated in software a complete neural system of ~10 billion synapses and ~1 million neurons performing cognitive tasks in a virtual environment comparable to those routinely tested in mice.<br>- Designed and validated a hardware neural system of ~10 billion synapses and ~1 million neurons.<br>- Demonstrated a chip fabrication process and development plan supporting ~10 billion synapses per square centimeter and ~1 million neurons per square centimeter.<br>- Downselected among fabrication processes for complimentary metal-oxide semiconductor (CMOS) and novel synaptic memory to optimize for density and power performance.<br>- Refined design tools and techniques by codifying design rules and component properties and matching them to fabrication and simulation capabilities.<br>- Demonstrated a virtual environment supporting visual perception, decision and planning, and navigation environments fully integrated with software or hardware neural systems enabling the testing, training, and evaluation of these neural systems. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Introduced modalities of competition within the virtual environment to further tailor the evolution of the neural systems.<br>***FY 2013 Plans:***<br>- Demonstrate fabricated neuromorphic chips of 1 million neurons performing behavioral tests in the virtual environment.<br>- Demonstrate functionality of chip performing perception challenge task and benchmark against state-of-the-art algorithms and methods.<br>- Determine scalability of hardware systems and future densities and power consumption for next-generation systems. | | | |
| ***Title:*** Self-HEALing mixed-signal Integrated Circuits (HEALICs) | 10.851 | 2.670 | 0.000 |
| ***Description:*** The goal of the Self-HEALing mixed-signal Integrated Circuits (HEALICs) program is to develop technologies to autonomously maximize the number of fully operational mixed-signal systems-on-a-chip (SoC) per wafer that meet all performance goals in the presence of extreme process technology variations, environmental conditions, and aging. Virtually all DoD systems employ mixed-signal circuits for functions such as communications, radar, navigation, sensing, high-speed image and video processing. A self-healing integrated circuit is defined as a design that is able to sense undesired circuit/system behaviors and correct them automatically. As semiconductor process technologies are being scaled to even smaller transistor dimensions, there is a dramatic increase in intra-wafer and inter-die process variations, which have a direct impact on realized circuit performance, as well as significantly increased sensitivity to temperature and ageing effects.<br><br>This applied research program aims to develop techniques to regain lost performance and stabilize operation of mixed-signal SoCs over system lifetimes. Consequently, the long-term reliability of DoD electronic systems is expected to be significantly enhanced.<br><br>***FY 2012 Accomplishments:***<br>- Demonstrated effectiveness of self-healing for several mixed-signal cores, including analog-to-digital converters (ADCs), and microwave/mm-wave power amplifiers, receiver chains and phase-locked loop frequency synthesizers. In each case, performance was significantly enhanced relative to baseline designs without integrated self-healing.<br>- Measured 100% performance yield (relative to 0% for a baseline non-healed design) for a 60 Gigahertz (GHz) fully integrated self-healing 16-QAM transceiver.<br>- Designed integrated radar front-end chip exhibiting a 32 decibel (dB) Channel Pair Cancellation Ratio (CPCR) due to self-healing of channel-channel gain and phase errors. This represents a 35 dB improvement over a typical baseline chip without self-healing.<br>- Demonstrated through simulation increased performance yields of mixed-signal SoCs to greater than ninety-five percent with minimal power and die area overhead for a wideband electronic receiver chain, 3 Gigasamples per second analog-to-digital converter and a 4 Gbps radio-on-a-chip. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Continued the development of a self-healing intellectual property core library for DoD user access and demonstrated self-healing integrated circuit designs leveraging cores from multiple performer teams.<br>- Designed self-healing circuits capable of mitigating the effects of negative-bias temperature instability (NBTI) and hot-carrier injection (HCI) which contribute to long-term circuit aging in deep-submicron CMOS transistors.<br>***FY 2013 Plans:***<br>- Continue to integrate previously demonstrated mixed-signal cores into a full self-healing microsystems/SoCs and show self-healing techniques capable of achieving >95% performance yield with <5% power consumption overhead through measurement of a sufficient number of sample die.<br>- Continue to develop global self-healing control at the microsystem/SoC level.<br>- Demonstrate self-healing design strategies to compensate for chip ageing.<br>- Make self-healing IP core library widely available for DoD user access. | | | |
| ***Title:*** Efficient Linearized All-Silicon Transmitter ICs (ELASTx) | 6.306 | 7.750 | 0.000 |
| ***Description:*** The goal of the Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program is the development of revolutionary high-power/high-efficiency/high-linearity single-chip millimeter (mm)-wave transmitter integrated circuits (ICs) in leading-edge silicon technologies for future miniaturized communications and sensor systems on mobile platforms. The high levels of integration possible in silicon technologies enable on-chip linearization, complex waveform synthesis, and digital calibration and correction. Military applications include ultra-miniaturized transceivers for satellite communications-on-the-move, collision avoidance radars for micro-/nano-air vehicles, and ultra-miniature seekers for small munitions. The technology developed under this program could also be leveraged to improve the performance of high-power amplifiers based-on other nonsilicon technologies through heterogeneous integration strategies. Significant technical obstacles to be overcome include the development of highly efficient circuits for increasing achievable output power of silicon devices (e.g., device stacking, power combining) at mm-waves; scaling high-efficiency amplifier classes to the mm-wave regime; integrated linearization architectures for complex modulated waveforms; and robust RF/mixed-signal isolation strategies.<br>***FY 2012 Accomplishments:***<br>- Demonstrated watt-level regime, high power added efficiency (PAE) silicon-based power amplifier (PA) circuits at Q-band frequencies.<br>- Demonstrated linearized transmitter circuits based on high PAE PAs at Q-band frequencies with complex modulated waveforms.<br>- Continued the development of watt-level, high PAE silicon-based PA circuits at W-band frequencies.<br>- Continued the development of linearized transmitter circuits based on high PAE PAs at W-band frequencies.<br>***FY 2013 Plans:***<br>- Demonstrate watt-level, high PAE silicon-based PA circuits at W-band frequencies. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrate linearized transmitter circuits based on high-PAE PAs at W-band frequencies with complex modulated waveforms.<br>- Initiate development of watt-level, high PAE silicon-based PA circuits at D-band frequencies.<br>- Initiate development of linearized transmitter circuits based on high PAE PAs at D-band frequencies with complex modulated waveforms. | | | |
| ***Title:*** Photonically Optimized Embedded Microprocessor (POEM)<br><br>***Description:*** Based upon current scaling trends, microprocessor performance is projected to fall far short of future military needs. Microprocessor performance is saturating and leading to reduced computational efficiency because of the limitations of electrical communications. The Photonically Optimized Embedded Microprocessor (POEM) program will demonstrate chip-scale, silicon-photonic technologies that can be integrated within embedded microprocessors for seamless, energy-efficient, high-capacity communications within and between the microprocessor and dynamic random access memory (DRAM). This technology will propel microprocessors onto a higher performance trajectory by overcoming the "memory wall", and thus satisfy projected microprocessor performance needs.<br><br>***FY 2012 Accomplishments:***<br>- Designed and fabricated electrical and optical components capable of a wavelength-division-multiplexed, complementary metal-oxide semiconductor (CMOS)-compatible, optical link with 80 gigabit/second capacity and a link energy efficiency of 1.5 picojoules per bit of data.<br>- Developed DRAM-compatible modulator, multiplexer, coupler, waveguide, and photodetector devices and associated drivers for low-power, high capacity photonic links.<br>- Designed on-chip photonic network to rapidly re-organize data, improving the execution time and total energy consumption of a matrix transpose operation.<br><br>***FY 2013 Plans:***<br>- Demonstrate a DRAM-compatible photonic link which enables photonic communication between CMOS and DRAM chips with 80 gigabits/second capacity and a link energy efficiency of 6.7 picojoules per bit of data.<br>- Continue to develop and improve CMOS-compatible modulator, multiplexer, coupler, and photodetector devices and associated drivers for low-power, high capacity photonic links for insertion in final demonstration.<br>- Develop an on-chip, uncooled laser operating at 3% wall plug efficiency.<br>- Identify applications where a cluster of photonically optimized microprocessors is useful and design the cluster architecture and photonic network. | 26.000 | 23.417 | 0.000 |
| ***Title:*** Analog-to-Information (A-to-I) Look-Through<br><br>***Description:*** The Analog-to-Information (A-to-I) Look-Through program will fundamentally improve the operational bandwidth, linearity, and efficiency of electronic systems where the objective is to receive and transmit information using electromagnetic | 10.500 | 3.800 | 0.000 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| (radio) waves under extreme size/weight/power and environmental conditions required for DoD applications. The A-to-I Look-Through program will develop ultra-wideband digital radio frequency (RF) receivers based on Analog-to-Information Converter (AIC) technology. Compared to conventional RF receivers, AIC-based designs will increase receiver dynamic range and frequency band of regard while reducing data glut, power consumption and size. Likewise, limitations of current-art power amplifier technology in simultaneously achieving high operational bandwidth, linearity, efficiency and power has resulted in well documented instances of electronic fratricide. This program will overcome these limitations by converting digital signals directly to high power RF analog signals, thus eliminating the traditional high power amplifiers that are limited by the above-mentioned tradeoffs. Transition is anticipated into airborne SIGINT and electronic warfare systems, as well as ground-based special operations forces systems.<br><br>***FY 2012 Accomplishments:***<br>- Finalized implementation and testing of A-to-I receiver data processing algorithms with focus on improving algorithm robustness against operationally-realistic conditions.<br>- Initiated technology transition plans to transition A-to-I receivers to one or more operationally-focused end user organizations.<br>- Developed and demonstrated through analysis, simulation and measurement, suitable Look-Through transmitter architectures.<br>- Designed, fabricated and characterized in laboratory environment Look-Through transmitter cells and signal combining structures.<br>- Demonstrated in a laboratory environment, using only two cells, the concept of current-summed travelling wave combining in a transmission line, achieving 6 dB of forward gain and 58 dB of reverse wave suppression. This is the first-ever demonstration of this kind and a key "proof-of-concept" for this program.<br>***FY 2013 Plans:***<br>- Finalize technology transition plans and transition A-to-I receivers to one or more operationally-focused end user organizations.<br>- Complete design, tape out and characterization in laboratory environment of Look-Through transmitters with high linearity, high power, wide bandwidth and high efficiency.<br>- Demonstrate capability of transmitter cells and associated distributed architectures to be re-programmed to perform distributed receiver-mode functions in order to mitigate electronic fratricide.<br>- Demonstrate the transmitter performance in realistic environments for a DoD system of interest. | | | |
| ***Title:*** Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) | 8.000 | 7.500 | 0.000 |
| ***Description:*** The Advanced Wide Field of View (FOV) Architectures for Image Reconstruction & Exploitation (AWARE) program addresses the passive imaging needs for multi-band, wide field of view (FOV) and high-resolution imaging for ground and near ground platforms. The AWARE program aims to solve the technological barriers that will enable FOV, high resolution and multi-band camera architectures by focusing on four major tasks: high space-bandwidth product (SBP) camera architecture; small pitch pixel focal plane array architecture; broadband focal plane array architecture; and multi-band focal plane array architecture. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| The AWARE program demonstrates technologies such as detectors, focal plane arrays, read-out integrated circuitry, and computational imaging that enable wide FOV and high space bandwidth, novel optical designs, high resolution and multiple wavelength band imagers. These technologies will be integrated into subsystem demonstrations under the related project in PE 0603739E, MT-15. This program also includes technologies previously addressed in the Wide Field of View (formerly MultiScale Optical Sensor Array Imaging (MOSAIC)) program.<br><br>***FY 2012 Accomplishments:***<br>- Constructed and demonstrated a compact multiscale 1.3 Gigapixel snapshot imaging system. The camera has a 120 by 60 degree FOV and 38 microradian instantaneous field of view (IFOV).<br>- Completed design of 10 Gigapixel camera with 100 by 60 degree FOV and an IFOV of 20 microradians.<br>***FY 2013 Plans:***<br>- Assemble and demonstrate 10 Gigapixel camera for diversity of operating modes, such as region of interest, feature detection and full frame capture. | | | |
| ***Title:*** Leading Edge Access Program (LEAP)<br><br>***Description:*** Most Integrated Circuit (IC) foundries offering leading edge technology are located outside of the United States. The detrimental effects of this trend are twofold: a lack of access to advanced onshore technology accelerates the migration of highly trained circuit designers from the United States; and DoD is faced with fewer trusted domestic foundries despite becoming increasingly reliant on leading edge semiconductor processes for its most critical systems.<br><br>Research at advanced semiconductor technology nodes is essential for driving future technology developments in both commercial and DoD application spaces. Thus, the objective of the Leading Edge Access Program (LEAP) is to provide university, industry and Government researchers access to state-of-the-art, onshore complementary metal-oxide semiconductor (CMOS) technology to develop advanced IC concepts relevant to DoD problems. Specifically, LEAP will offer onshore foundry access to CMOS technology nodes of 45 nm and below to increase the number of U.S. designers possessing expertise in leading edge CMOS nodes.<br><br>***FY 2012 Accomplishments:***<br>- Developed foundry offerings at 45nm and 32nm CMOS nodes and a special 22 nanometer multiproduct wafer.<br>***FY 2013 Plans:***<br>- Develop new foundry offerings at 32nm and 22nm CMOS technologies.<br>- Develop new foundry offerings for 9HP 90 nm Silicon-Germanium (SiGE) BiCMOS technologies. | 2.000 | 3.000 | 0.000 |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Investigate support for access to silicon photonics MPW efforts.<br>- Initiate discussions and develop plans for 14nm CMOS and 3-D access. | | | |
| ***Title:*** High Frequency Integrated Vacuum Electronic (HiFIVE) | 4.540 | 0.000 | 0.000 |
| ***Description:*** The objective of the High Frequency Integrated Vacuum Electronics (HiFIVE) program was to develop and demonstrate new high-performance and low-cost technologies for implementing high-power millimeter-wave sources and components. This program developed new semiconductor and micro-fabrication technologies to produce vacuum electronic high-power amplifiers for use in high-bandwidth, high-power transmitters. Innovations in design and fabrication were pursued to enable precision etching, deposition, and pattern transfer techniques to produce resonant cavities, electrodes, and magnetics, and electron emitting cathodes for compact high-performance millimeter wave devices. These new technologies eliminated the limitations associated with the conventional methods for assembly of high-power sources in this frequency range. Advanced research for this program was budgeted in PE 0603739E, Project MT-15.<br><br>***FY 2012 Accomplishments:***<br>- Continued efforts to perform laboratory measurements of performance and validate RF power levels, including advanced driver amplifiers.<br>- Continued fabrication and initial testing of a high-power amplifier prototype device incorporating HiFIVE micro-fabrication technologies into a compact module form factor. | | | |
| ***Title:*** Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) | 7.466 | 0.000 | 0.000 |
| ***Description:*** The objective of the Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) program was to develop chip-scale dense waveguide modular technology to achieve true embedded phase array control for beams equivalent to 10W average power, less than 0.1 degree instantaneous field of view (IFOV), greater than 45 degree total field of view (TFOV), and frame rates of greater than 100 hertz (Hz) in packages that are "chip-scale." Such performance represents a three order of magnitude increase in speed, while also achieving a greater than two orders of magnitude reduction in size. Additionally, the integrated phase control provided the unprecedented ability to rapidly change the number of simultaneous beams, beam profile, and power-per-beam, thus opening a whole new direction in operational capability. Key technical challenges included the ability to achieve the needed facet density (facet pitch should be on the order of a wavelength or two), control the relative phase across all facets equivalent to 9-bits, and efficiently couple and distribute coherent light to facets from a master laser oscillator with an integrated waveguide structure.<br><br>***FY 2012 Accomplishments:***<br>- Demonstrated 8x8 integrated photonic chip scale array beam forming with path towards a 32x32 array.<br>- Demonstrated better than 10°x10° beam steering with <20 decibel sidelobes. | | | |

| Exhibit R-2, RDT&E Budget Item Justification: PB 2014 Defense Advanced Research Projects Agency | DATE: April 2013 |
|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 2: *Applied Research* | R-1 ITEM NOMENCLATURE<br>PE 0602716E: *ELECTRONICS TECHNOLOGY* |

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2012 | FY 2013 | FY 2014 |
|---|---|---|---|
| - Demonstrated a 32x32 integrated photonic chip optical phased array with dynamic beam forming and a path towards a 64x64 array.<br>- Demonstrated sidelobe suppression <20 decibels. | | | |
| ***Title:*** Compact Mid-Ultraviolet Technology<br><br>***Description:*** The goal of the Compact Mid-Ultraviolet Technology (CMUVT) program was to develop compact high-brightness Middle Ultraviolet source and detector technologies based on wide band gap diode structures. This program addressed a critical technology shortfall preventing mid-UV capability in portable chem-bio defense systems for aerosol detection (enhanced capability for small particulates), chem-bio identification (Raman scattering and spectroscopy), and chemical decontamination/ water purification applications. The technologies also addressed solar-blind detectors for missile plume identification.<br><br>***FY 2012 Accomplishments:***<br>- Increased the diameter of high-quality aluminum nitride substrates and ternary templates up to 30mm diameter to enable development of optimized devices.<br>- Demonstrated high wall plug efficiency middle-UV (250-270nm) Light-emitting Diodes (LED) with brightness over 100mW, an improvement of >100x over state-of-the-art at the start of the program.<br>- Demonstrated aluminum gallium nitride semiconductor lasers operating at wavelengths as short as 237nm, a reduction of over 100nm compared to state-of-the-art at the start of the program.<br>- Demonstrated insertion of high-power, high-efficiency UV LEDs into Army Tactical Biological Detector (TAC-BIO) aerosol detection system. TAC-BIO using CMUVT LEDs demonstrated 10x enhancement in signal response per Watt of output power compared to TAC-BIO using commercial off-the-shelf UV LEDs. | 14.189 | 0.000 | 0.000 |
| **Accomplishments/Planned Programs Subtotals** | 216.102 | 222.416 | 243.469 |

**D. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**E. Acquisition Strategy**

N/A

**F. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.