| Exhibit R-2, RDT&E Budget Item Justification: PB 2021 Defense Advanced Research Projects Agency | Date: February 2020 |
|---|---|
| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research* | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* |

| COST ($ in Millions) | Prior Years | FY 2019 | FY 2020 | FY 2021 Base | FY 2021 OCO | FY 2021 Total | FY 2022 | FY 2023 | FY 2024 | FY 2025 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | - | 331.905 | 317.192 | 322.693 | - | 322.693 | 357.162 | 370.355 | 414.550 | 416.015 | - | - |
| ELT-01: *ELECTRONIC TECHNOLOGY* | - | 99.777 | 120.882 | 122.986 | - | 122.986 | 153.262 | 166.145 | 210.340 | 211.805 | - | - |
| ELT-02: *BEYOND SCALING TECHNOLOGY* | - | 232.128 | 196.310 | 199.707 | - | 199.707 | 203.900 | 204.210 | 204.210 | 204.210 | - | - |

**A. Mission Description and Budget Item Justification**

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project will therefore pursue electronics performance advancements that do not rely on Moore's Law but instead exploit new concepts in circuit specialization, by the optimization of materials, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies, this envisioned electronics specialization will require incorporation of security safeguards. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials, and new techniques for securing DoD and commercial data and hardware.

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| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research* | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* |

| B. Program Change Summary ($ in Millions) | FY 2019 | FY 2020 | FY 2021 Base | FY 2021 OCO | FY 2021 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 348.847 | 332.192 | 340.000 | - | 340.000 |
| Current President's Budget | 331.905 | 317.192 | 322.693 | - | 322.693 |
| Total Adjustments | -16.942 | -15.000 | -17.307 | - | -17.307 |
| • Congressional General Reductions | 0.000 | -15.000 | | | |
| • Congressional Directed Reductions | 0.000 | 0.000 | | | |
| • Congressional Rescissions | 0.000 | 0.000 | | | |
| • Congressional Adds | 0.000 | 0.000 | | | |
| • Congressional Directed Transfers | 0.000 | 0.000 | | | |
| • Reprogrammings | 0.551 | 0.000 | | | |
| • SBIR/STTR Transfer | -17.493 | 0.000 | | | |
| • TotalOtherAdjustments | - | - | -17.307 | - | -17.307 |

| Congressional Add Details ($ in Millions, and Includes General Reductions) | FY 2019 | FY 2020 |
|---|---|---|
| **Project:** ELT-02: *BEYOND SCALING TECHNOLOGY* | | |
| Congressional Add: *DARPA Electronics Resurgence Initiative* | 30.000 | - |
| Congressional Add Subtotals for Project: ELT-02 | 30.000 | - |
| Congressional Add Totals for all Projects | 30.000 | - |

**Change Summary Explanation**

FY 2019: Decrease reflects the SBIR/STTR transfer offset by reprogrammings.
FY 2020: Decrease reflects congressional reduction.
FY 2021: Decrease reflects completion of several Electronic Technology programs in FY 2020.

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | | Date: February 2020 |
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| Appropriation/Budget Activity<br>0400 / 2 | R-1 Program Element (Number/Name)<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | Project (Number/Name)<br>ELT-01 / *ELECTRONIC TECHNOLOGY* | |

| COST ($ in Millions) | Prior Years | FY 2019 | FY 2020 | FY 2021 Base | FY 2021 OCO | FY 2021 Total | FY 2022 | FY 2023 | FY 2024 | FY 2025 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ELT-01: *ELECTRONIC TECHNOLOGY* | - | 99.777 | 120.882 | 122.986 | - | 122.986 | 153.262 | 166.145 | 210.340 | 211.805 | - | - |

**A. Mission Description and Budget Item Justification**

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| ***Title:*** Modular Optical Aperture Building Blocks (MOABB) | 17.000 | 19.000 | 14.141 |
| ***Description:*** The Modular Optical Aperture Building Blocks (MOABB) program aims to greatly improve the cost, size, weight, and performance of free-space optical systems. These systems enable applications such as Light Detection And Ranging (LIDAR), laser communications, laser illumination, navigation, and 3D imaging. Specifically, MOABB will construct millimeter-scale optical building blocks that can be coherently arrayed to form larger, higher power devices. These building blocks would replace the traditional large and expensive precision lenses and mirrors, which require slow mechanical steering, that form conventional optical systems. MOABB will develop scalable optical phased arrays that can steer light waves without the use of mechanical components. These advances would allow for a 100-fold reduction in size and weight and a 1,000-fold increase in the steering rate of optical systems. | | | |
| ***FY 2020 Plans:***<br>- Synthesize multiple light beams from a single optical phased array aperture of one square centimeter area.<br>- Demonstrate integration of laser sources and optical phased arrays on photonic chips.<br>- Create and characterize a prototype LIDAR module using optical phased arrays. | | | |
| ***FY 2021 Plans:***<br>- Improve optical phased array LIDAR range.<br>- Demonstrate optical phased array LIDAR on un-manned ground and air vehicles. | | | |
| ***FY 2020 to FY 2021 Increase/Decrease Statement:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| The FY 2021 decrease reflects final demonstrations. | | | |
| ***Title:*** Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) | 11.540 | 10.000 | 9.000 |
| ***Description:*** The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program will develop novel magnetic sensors capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. In recent years, the value of magnetic imaging, for example for cardiac and other biological signals, has shown tremendous potential for advanced research and clinical diagnosis. Practical application, however, has been limited. Interference from natural and manmade ambient magnetic fields has required that the measurements be performed in specialized, magnetically-shielded research facilities. The AMBIIENT program will exploit novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself must be able to detect the gradient of a local magnetic field while subtracting the much larger ambient signal. This would enable low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors promise to enable diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and ultralow frequency communications.<br><br>***FY 2020 Plans:***<br>- Complete sensor package architecture meeting AMBIIENT size weight and power, accuracy, and sensitivity goals.<br>- Fabricate and test architectures for direct gradient sensing of magnetic fields.<br><br>***FY 2021 Plans:***<br>- Design sensor package architecture meeting AMBIIENT size weight and power, accuracy, and sensitivity goals.<br>- Integrate control electronics for direct gradient sensing of magnetic fields.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects the program going from initial to final design of the sensor package architecture. | | | |
| ***Title:*** Dynamic Range-enhanced Electronics and Materials (DREaM) | 13.000 | 17.000 | 15.000 |
| ***Description:*** The Dynamic Range-enhanced Electronics and Materials (DREaM) program aims to develop intrinsically linear (ideal) radio frequency (RF) transistors with improved power efficiency and extremely high dynamic range. Linearity, power efficiency, and dynamic range are fundamental characteristics that allow RF systems to reliably transmit clear signals. Improving these characteristics is essential to operating in a crowded RF environment and to enabling next-generation communication, sensing, and electronic warfare systems. Traditional RF transistor designs typically require a trade-off between linearity and broadcast power, and poor linearity results in undesired interference. DREAM will overcome this tradeoff by employing new transistor materials, architectures, and designs. The resulting DREAM-enabled technologies will allow future RF electronics to increase their operating range without polluting the already-congested RF spectrum and while consuming less system power.<br><br>***FY 2020 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Manufacture and characterize transistor unit cells with both a three times improvement over the state of the art in output power density and ten times higher linearity.<br>- Optimize fabrication processes and explore novel transistor topology to enable higher breakdown voltage, for design of transistors with four times higher power density than the state of the art.<br>- Exploit new channel materials and perform device modeling to enable scaling to 30 times higher linearity than state of the art at 30 gigahertz operational frequency.<br>***FY 2021 Plans:***<br>- Design, simulate and optimize transistor unit cells with both a five times improvement over the state of the art in output power density and ten times higher linearity.<br>- Optimize novel transistor topology and fabrication processes to enable higher breakdown voltage, for design of transistors with five times higher power density than the state of the art, and identify thermal solution for high power operation.<br>- Exploit new channel materials, device topology and modeling to enable scaling to 100 times better linearity than state of the art at 30 gigahertz operational frequency.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects the program transitioning from developing advanced transistor architectures to manufacturing transistor unit cells. | | | |
| ***Title:*** SHort Range Independent Microrobotic Platforms (SHRIMP) | 4.500 | 9.000 | 8.000 |
| ***Description:*** The SHort Range Independent Microrobotic Platforms (SHRIMP) program is developing and demonstrating multi-functional millimeter-to-centimeter scale robotic platforms with a focus on untethered mobility, maneuverability, and dexterity. To achieve this goal, SHRIMP conducted foundational research in the area of micro-actuator materials and energy efficient power systems for extremely size, weight, and power constrained microrobotic systems. The program's platform development activities will leverage recent advances in low power, application specific integrated circuit electronics and low power sensors from the internet of things community to increase the functionality of microrobotic platforms while increasing platform mobility, maneuverability, and dexterity. The microrobotic platform capabilities enabled by SHRIMP will provide the DoD with significantly more access and capability to operate in small spaces that are practically inaccessible to today's state-of-the-art robotic platforms. Such capability will have impact in search and rescue, disaster relief, infrastructure inspection, and equipment maintenance, among other operations. Foundational research efforts are funded in PE 0601101E, Project ES-01.<br>***FY 2020 Plans:***<br>- Demonstrate tethered microrobotic platforms meeting program metrics on length, weight, and duration of operation.<br>- Initiate development of untethered microrobotic platforms with an emphasis on size, weight, and performance.<br>***FY 2021 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Demonstrate untethered microrobotic platforms meeting improved program metrics on length, weight, and duration of operation.<br>- Refine and optimize untethered microrobotic platforms for competition in Olympic-style events.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects the program shifting from demonstrating tethered to refining and optimizing untethered microrobotic platforms. | | | |
| ***Title:*** Focal Arrays for Curved Infrared Imagers (FOCII)*<br>***Description:*** *Formerly Intelligent Spectroscopic & Temporal Fusion (INSPECT)<br><br>The Focal Arrays for Curved Infrared Imagers (FOCII) program will add curved focal plane arrays to broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. The resulting desired capability is analogous to human vision that enables wide fields of view in a compact optical system package. Currently fielded imaging systems are flat broadband infrared sensors that rely on large and complex optics to correct aberrations and improve illumination and resolution. FOCII will (1) leverage curving strategies for state of the art focal plane arrays combined with advances in designing and manufacturing stress relief features to demonstrate hardware that simultaneously provides maximum resolution and illumination, and (2) develop novel designs for IR imagers that enable minimal size, weight and cost for size-constrained applications. This will enable new applications in passive seeker technology for missiles, overhead persistent infrared imaging, 360 degree situational awareness, infrared search and track, and long range targeting.<br>***FY 2020 Plans:***<br>- Develop mechanical stress models for use with existing broadband imaging hardware.<br>- Fabricate initial curved focal plane array prototypes that meet program goals for radius of curvature and size of pixels.<br>***FY 2021 Plans:***<br>- Measure baseline spectral uniformity of curved large area focal arrays.<br>- Measure mechanical stress of curved large area focal arrays to validate mechanical stress models.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects the program shifting from fabricating initial curved focal plan array prototypes to measuring mechanical stress of curved large area focal arrays. | - | 13.000 | 17.000 |
| ***Title:*** Wideband Adaptive RF Protection (WARP)*<br>***Description:*** *Formerly Instinctual RF | - | 11.200 | 16.845 |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| The Wideband Adaptive RF Protection (WARP) program will develop radio frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference, through tunable filtering, limiting, and/or signal cancellation. Today's advanced wideband DoD systems, such as multi-function phased arrays, are open to all frequencies by design with little or no RF filtering. This is due to a lack of tunable and reconfigurable filters that are small enough to integrate into the arrays, limiting the use of wideband multi-function arrays in contested environments. The ability to create tunable and reconfigurable bandpass and bandstop filters in the range of 2-18 GHz will be important for implementing transmit/ receive modules in next generation multi-function arrays. Another important area of interference mitigation is self-interference. Specifically, in electronic warfare, it would be advantageous to be able to receive and perform signal intelligence functions while simultaneously transmitting a high-power jamming self-protect signal. WARP will develop the signal cancellation technology that will listen to the transmitted jamming signal and subtract it from the input of the receiver so faint signals near the noise floor can still be detected. Program research will provide feedback mechanisms that intelligently correct these problems. Whether for self-induced interference or external interference jamming, WARP will develop intelligent filtering and self-interference cancellation technologies to protect wideband DoD receivers.<br><br>***FY 2020 Plans:***<br>- Begin investigating new materials, devices and/or circuit architectures that will enable frequency tuning of band pass and band stop filters in chip-scale size for use in next generation wideband receivers for DoD systems.<br>- Begin investigating new materials, devices and/or circuit architectures that will enable cancellation of signal leakage between two adjacent antennas for simultaneous transmit and receive electronic warfare applications on small platforms.<br><br>***FY 2021 Plans:***<br>- Demonstrate new materials, devices and/or circuit architectures that will enable frequency tuning of band pass and band stop filters in chip-scale size for use in next generation wideband receivers for DOD systems.<br>- Demonstrate new materials, devices and/or circuit architectures that will enable cancellation of signal leakage between two adjacent antennas for simultaneous transmit and receive electronic warfare applications on small platforms.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects the program shifting from investigating to demonstrating RF front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference, through tunable filtering, limiting, and/or signal cancellation. | | | |
| ***Title:*** Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) | - | 12.000 | 20.000 |
| ***Description:*** The Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) program, building upon technologies developed in the AMBIIENT program, budgeted within this PE and Project, will develop full tensor magnetic /electric field sensors and demonstrate them in DoD relevant applications and concept of operations. Magnetometers and electrometers are widely | | | |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| used within the DoD and industry. The medical community utilizes sensitive magnetometers for magnetoencephalography and magnetocardiography. In addition to being diagnostically relevant, such sensitive magnetometers could enable future human-machine/brain-machine interfaces. The DoD and industry also uses magnetometers for magnetic anomaly detection, which may allow for the discovery of mineral/oil deposits, discovery of old wellheads, or the detection of improvised explosive devices. In addition, magnetometers offer the possibility of magnetic navigation, which may operate in GPS-denied environments. High sensitivity electrometers are used by industry to locate live current and static electricity sources. Recent developments have resulted in the potential to develop highly sensitive vector electrometers and magnetometers, which would enable the consequent development of sensitive full tensor gradient sensors. Such tensors offer more degrees of freedom than their scalar or vector counterparts and potentially provide additional information about the source.<br><br>***FY 2020 Plans:***<br>- Design prototype tensor gradient magnetometer and/or tensor gradient electrometer.<br>***FY 2021 Plans:***<br>- Build preliminary magnetic or electric field tensor gradiometer.<br>- Develop tensor-based algorithms for DoD relevant applications.<br>- Initiate research into building a magnetic or electric field tensor sensor.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects a shift from design to building preliminary magnetic/electric field sensors. | | | |
| ***Title:*** High Operating Temperature Sensors for Hypersonics and Turbine Engines (HOTSHOT) | - | - | 11.000 |
| ***Description:*** The High Operating Temperature Sensors for Hypersonics and Turbine Engines (HOTSHOT) program seeks to enable electronics and sensing in harsh temperature environments for next generation vehicles. Currently, sensing systems are not robust to the temperature extremes expected over a mission lifetime. This technology gap hampers the ability to capture flight test data from air vehicles (boost glide, air-breathing, etc.) during development. HOTSHOT will develop the material, device, and sensor technologies required to create high-temperature capable sensing systems. These new material choices allow transduction, signal conditioning, digitization, and processing at elevated temperatures, thus reducing the need for temperature shielding of these components. Reduced shielding drops the on-vehicle size, weight, and power requirements for many components. HOTSHOT will enable faster and more predictable design of new air vehicles, which will lead to more efficient system performance.<br><br>***FY 2021 Plans:***<br>- Demonstrate initial results of transduction and signal conditioning at elevated temperatures.<br>- Release of initial design parameters for selected electronics process. | | | |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Develop base electronics that can perform logic functions.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects program initiation. | | | |
| ***Title:*** Data Privacy for Virtual Environments (DPRIVE)<br><br>***Description:*** The Data Privacy in Virtual Environments (DPRIVE) program will enable data privacy at the user and application level, through the development of new hardware accelerators, to achieve acceptable computational times. The program plans to provide strong privacy protections at the tactical edge with no more than one order of magnitude penalty in computation time and enable very strong privacy at the enterprise level with no more than three orders of magnitude penalty over unencrypted processing. The DoD is increasingly reliant on cloud computing services and storage. Cloud-enabled virtualized storage and the accompanying virtualized computing play a key role in data processing for planning and operations. Networks are also becoming more virtualized spaces, such as in 5G systems. The growing virtualization storage, computing, and networking puts data privacy of all users at risk. DPRIVE will build hardware to accelerate the computation of homomorphic encryption, which enables mathematical operations to execute on encrypted data such that the data is never unencrypted. The program will enable the development and deployment of these hardware accelerators to edge computing devices where power and time are a premium as well as enterprise computing facilities where the amount and sensitivity of the data requires increased protection.<br><br>***FY 2021 Plans:***<br>- Develop algorithms and simulate performance for both edge and enterprise mission sets.<br>- Create a hardware design model.<br>- Prove the ability to compute deep neural networks on encrypted data.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects program initiation. | - | - | 12.000 |
| ***Title:*** High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC)<br><br>***Description:*** The High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) program seeks to develop compact radio frequency signal amplifiers for air, ground, and ship-based communications and sensing systems. HAVOC amplifiers would enable these systems to access the high-frequency millimeter-wave portion of the electromagnetic (EM) spectrum, facilitating increased range and other performance improvements. Today, the effectiveness of combat operations across all domains increasingly depends on DoD's ability to control and exploit the EM spectrum and to deny its use to adversaries. However, the proliferation of inexpensive commercial RF sources has made the EM spectrum crowded and contested, challenging our spectrum dominance. Operating at higher frequencies, such as the millimeter-wave, helps DoD to overcome these issues and offers numerous tactical advantages such as high data-rate communications and high resolution and | 6.000 | 6.000 | - |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| sensitivity for radar and sensors. Technology transfer efforts will follow a spiral development process to mitigate risk and provide the opportunity to incorporate new technological developments as they occur. Basic research for this program is funded within PE 0601101E, Project ES-01.<br><br>***FY 2020 Plans:***<br>- Fabricate single-beam vacuum amplifiers and test at high average-power output.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects program completion. | | | |
| ***Title:*** Precise Robust Inertial Guidance for Munitions (PRIGM)<br><br>***Description:*** The Precise Robust Inertial Guidance for Munitions (PRIGM) program is developing inertial sensor technologies for positioning, navigation, and timing (PNT) in GPS-denied environments. When GPS is not available, these inertial sensors can provide autonomous PNT information. The program will exploit recent advances in integrating photonic (light-manipulating) components into electronics and in employing Microelectromechanical Systems (MEMS) as high-performance inertial sensors for use in extreme environments. Whereas conventional MEMS inertial sensors can suffer from inaccuracies due to factors such as temperature sensitivity, new photonics-based PNT techniques have demonstrated the ability to mitigate these inaccuracies. PRIGM will focus on two areas. By 2022, it aims to develop and transition a Navigation-Grade Inertial Measurement Unit (NGIMU), a state-of-the-art MEMS device, to DoD platforms. By 2030, it aims to develop advanced inertial MEMS sensors that can provide gun-hard, high-bandwidth, high dynamic range navigation for GPS-free munitions. These advances should enable navigation applications, such as smart munitions, that require low-cost, size, weight, and power inertial sensors with high bandwidth, precision, and shock tolerance. PRIGM will advance state-of-the-art MEMS gyros from TRL-3 devices to a TRL-6 transition platform, eventually enabling the Service Labs to perform TRL-7 field demonstrations. Basic research for this program was funded within PE 0601101E, Project ES-01 and advanced technology development for the program is budgeted in PE 0603739E, Project MT-15.<br><br>***FY 2020 Plans:***<br>- Demonstrate inertial sensor survival and operation through representative launch environments in the laboratory.<br>- Demonstrate two-chip, low power, near tactical grade Inertial Measurement Unit (IMU).<br>- Demonstrate single-chip, low power, tactical grade IMU capable of gun-hard operation.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects program completion. | 9.069 | 5.000 | - |
| ***Title:*** Wafer-scale Infrared Detectors (WIRED) | 12.000 | 5.682 | - |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| ***Description:*** The WIRED program addresses the need for low-cost, high-performance imaging sensors in the short-wave and mid-wave infrared (SWIR/MWIR) bands. These sensors will provide increased standoff distances for small unmanned aerial vehicles, low-cost missiles, handheld weapon sights and surveillance systems, helmet-mounted systems, and ground-vehicle-mounted threat warning systems. WIRED proposes to manufacture these sensors at the wafer scale, which reduces costs by processing dozens to hundreds of camera imaging arrays at a time. Wafer-scale manufacturing has already driven a revolution in optical imaging in both the visible and the long-wave infrared (LWIR) spectrum, with high-resolution digital cameras and LWIR sensors having become commonplace or widely-available. However, no similar technologies exist for the SWIR/MWIR bands. WIRED could therefore drive a similar revolution in SWIR/MWIR. The program aims to significantly reduce the weight and volume of MWIR detectors, which today require heavy cryogenic cooling systems, and increase the resolution of SWIR detectors by dramatically reducing their pixel size relative to the state-of-the-art.<br><br>***FY 2020 Plans:***<br>- Demonstrate improved performance of the MWIR imager compatible with requirements for relevant DoD applications.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects program completion. | | | |
| ***Title:*** Atomic Clock with Enhanced Stability (ACES) | 16.000 | 6.000 | - |
| ***Description:*** The Atomic Clock with Enhanced Stability (ACES) program is developing extremely stable chip-scale atomic clocks for unmanned aerial vehicles and other low size, weight, and power (SWaP) platforms with extended mission durations. Atomic clocks provide the high-performance backbone of timing and synchronization for DoD navigation; communications; electronic warfare; and intelligence, surveillance, and reconnaissance systems. However, atomic clocks are limited, particularly by temperature sensitivity, aging over long timescales, and a loss of accuracy when power cycled. By employing alternative approaches to confining and measuring atomic particles, ACES could yield a 100x - 1,000x improvement in key performance parameters related to each of these limitations. ACES will also focus on developing the component technologies necessary for low-cost manufacturing and for deployment in harsh DoD-relevant environments. Among its many benefits, program success could help reduce the risk posed by a growing national dependence on GPS, allowing systems to maintain their timing accuracy in the event of temporary GPS unavailability.<br><br>***FY 2020 Plans:***<br>- Fabricate a fully integrated prototype including electronics and physics package meeting SWaP objectives such that prototypes can be delivered and tested.<br>- Deliver prototype to government facility for testing and verification of GPS-independent timing accuracy.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:*** | | | |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| The FY 2021 decrease reflects program completion. | | | |
| ***Title:*** Limits of Thermal Sensors (LOTS)<br><br>***Description:*** The Limits of Thermal Sensors (LOTS) program aims to demonstrate long-wave infrared (LWIR) detector technologies with both high performance and low-size, weight, power, and cost (SWaP-C). The resulting technologies would enable improvements in imaging systems such as night-vision goggles, infrared-guided missiles, and missile threat warning systems. Currently, LWIR-enabled systems must choose between large and expensive cryogenically-cooled detectors, which offer high sensitivity and low response times, and uncooled detectors called microbolometers, which offer significant SWaP-C reductions at lower performance. LOTS seeks to develop microbolometers that can compete with larger cameras in terms of higher sensitivity required to detect signals over long ranges and lower response time required to avoid image blur. These technologies will allow DoD to deploy smaller, lighter, and cheaper sensors on critical, high-value assets while maintaining or improving their ability to engage fast-moving or distant targets.<br><br>***FY 2020 Plans:***<br>- Demonstrate microbolometer arrays on improved read-out integrated circuits and develop design variants appropriate for different platforms and use cases.<br>- Build final cameras for demonstration in relevant environments.<br>- Demonstrate the utility of high performance microbolometers for low-cost infrared search and track applications, including evaluating the impact of jitter.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects program completion. | 7.668 | 7.000 | - |
| ***Title:*** Direct On-Chip Digital Optical Synthesis (DODOS)<br><br>***Description:*** The Direct On-chip Digital Optical Synthesis (DODOS) program aimed to integrate diverse electronic and photonic components to create a compact, robust, and highly-accurate optical frequency synthesizer for various mission-critical DoD applications. DODOS leveraged recent developments in the field of integrated photonics to enable the development of a ubiquitous, low-cost optical frequency synthesizers. The program lead to disruptive DoD capabilities, including high-bandwidth optical communications, higher performance Light Detection And Ranging (LiDAR), portable high-accuracy atomic clocks, and high-resolution detection of chemical/biological threats at a distance. Basic research for this program was funded within PE 0601101E, Project ES-01. | 3.000 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 99.777 | 120.882 | 122.986 |

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**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

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| Appropriation/Budget Activity<br>0400 / 2 | R-1 Program Element (Number/Name)<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | Project (Number/Name)<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* | |

| COST ($ in Millions) | Prior Years | FY 2019 | FY 2020 | FY 2021 Base | FY 2021 OCO | FY 2021 Total | FY 2022 | FY 2023 | FY 2024 | FY 2025 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ELT-02: *BEYOND SCALING TECHNOLOGY* | - | 232.128 | 196.310 | 199.707 | - | 199.707 | 203.900 | 204.210 | 204.210 | 204.210 | - | - |

**A. Mission Description and Budget Item Justification**

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project will therefore pursue electronics performance advancements that do not rely on Moore's Law but instead exploit new concepts in circuit specialization, by the optimization of materials, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies, this envisioned electronics specialization will require incorporation of security safeguards. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials, and new techniques for securing DoD and commercial data and hardware.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| ***Title:*** Beyond Scaling - Materials | 44.349 | 44.000 | 37.000 |
| ***Description:*** The Beyond Scaling - Materials program is demonstrating the integration of novel materials into next-generation logic and memory components. Historically, the DoD had taken the lead in shaping the electronics field through research in semiconductor materials, circuits, and processors. However, as DoD focuses on military-specific components and commercial investments eschew the semiconductor space, U.S. fundamental electronics research is stagnant just as an inflection point in Moore's Law (silicon scaling) is about to occur. This program is pursuing potential enhancements in electronics that do not rely on Moore's Law, including research not only into new materials but also into the implications of those materials at the device, algorithm, and packaging levels. Research areas include heterogeneous integration of multiple materials, "sticky logic" devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. Further research will support innovation in the technology cycle by working with entrepreneurs focused on DoD-relevant businesses. The program is demonstrating the manufacturability of functioning switches, memory, and novel computational units in a large-scale system. Previous DARPA work on unconventional computing, integration, and reprogrammable memory give confidence in this approach. Basic research for this program is funded within PE 0601101E, Project ES-02.<br><br>***FY 2020 Plans:***<br>- Demonstrate fabrication of fully integrated monolithic 3D circuits at a commercial fabrication facility.<br>- Release distribution quality design tools to enable external design of monolithic 3D circuits. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Demonstrate large-scale fully functional chips using alternative materials fabricated in a 90 nm foundry with capabilities that are competitive with advanced technology nodes.<br>- Demonstrate superconductor multi-chip module carrier production on 300 mm wafers by a commercial foundry.<br>- Simulate critical high-speed circuit blocks for supporting mixed-mode integrated circuitry to be fabricated at a commercial foundry.<br>- Design and simulate highly scaled transistors with new materials and device topology for high speed mixed-mode electronics based on advanced silicon complementary metal oxide semiconductor fabrication processes.<br>- Develop and demonstrate innovative component technologies for next-generation photonic interconnect, targeting concepts for 100x improvement to link energy and bandwidth over current state-of-the-art performance.<br>- Leverage access to Federally Funded Research and Development Centers (FFRDC)-based entrepreneurial research hubs to refine and develop select academic discoveries for delivery into DoD systems.<br>***FY 2021 Plans:***<br>- Demonstrate operational digital signal processing circuits using novel superconductor electronics.<br>- Test critical mixed-mode demonstration circuit blocks fabricated at a commercial foundry.<br>- Integrate innovative component technologies and characterize link performance towards next-generation photonic interconnect capabilities.<br>- Release final design tools to be utilized for design of 3D monolithic circuits.<br>- Expand access to the Federally Funded Research and Development Centers (FFRDC) infrastructure to include additional academic researchers, leading to new technology prototypes with a validated path to deployment by U.S. suppliers.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects the program transitioning towards demonstrating the ability to take alternative materials through a full commercial process flow. | | | |
| ***Title:*** Beyond Scaling - Architectures | 43.000 | 35.000 | 36.707 |
| ***Description:*** The Beyond Scaling - Architectures program is demonstrating a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program is exploring technologies and techniques such as new domain-specific circuit architectures; co-design of electronics hardware and software; intelligent edge sensors; hardware security architectures; and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Further research will enable significant productivity improvements in programming productivity for massively parallel heterogeneous processing systems (e.g. data centers). Basic research for this program is funded within PE 0601101E, Project ES-02.<br>***FY 2020 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Demonstrate initial reconfigurable architecture simulation and emulation environment that will drive hardware design decisions and definitions.<br>- Emulate a specialized processor design and demonstrate an emulation of the processor executing two simultaneous applications.<br>- Define diverse data flow management approaches, and develop architecture simulations to drive architecture decisions and definitions.<br>- Develop initial architecture field programmable gate array based emulation environment and software development environments.<br>- Design and demonstrate a prototype system or the detection of hardware Trojans in commercial-off-the-shelf hardware commonly found in DoD systems.<br>- Develop a compilation architecture, domain-specific framework, and system modeling approach compatible with high productivity/high performance compilation for extreme parallelism and heterogeneity.<br>***FY 2021 Plans:***<br>- Produce, test and demonstrate a specialized processor design executing two simultaneous applications.<br>- Advance the software tools, development technologies, and design methodologies for system-on-chips (SoCs) with heterogeneous components that can be easily reprogrammed for specialized applications.<br>- Complete full architecture designs.<br>- Demonstrate FPGA-based full architecture emulation environments and fully functional software development environments.<br>- Prototype a compiler that demonstrates the feasibility of achieving high levels of productivity, efficiency, portability, and execution speed on a DoD-relevant workload.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects minor program repricing. | | | |
| ***Title:*** Beyond Scaling - Design | 33.000 | 22.000 | 25.000 |
| ***Description:*** The Beyond Scaling - Design program is developing and demonstrating the tools required for rapidly designing and deploying specialized circuits. As Moore's Law slows and the nation loses the benefit of free, exponential improvements in electronics cost, speed, and power derived from silicon scaling, the DoD will need to maximize the benefits of available silicon technologies by using design tools that enable circuit specialization. Research efforts are exploring technologies and techniques such as intelligent design tools, automated physical layout generation, and open-source circuit designs. The goal of this program is to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a secure pathway for the rapid upgrade of electronics. Advances under this program will demonstrate a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon scaling. Rapid design and deployment techniques | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| developed will also consider the need to incorporate security into DoD hardware. Basic research for this program is funded within PE 0601101E, Project ES-02.<br><br>***FY 2020 Plans:***<br>- Deliver software for physical layout of integrated circuits, packages and boards that is 100% automated and achieves 50% power, performance and area compared to traditional best in class techniques.<br>- Demonstrate fabrication of circuits generated from high-level schematics using a fully automated intelligent design flow.<br>- Publically release open source Intellectual Property (IP) modules developed in the program and demonstrate portability between multiple technology nodes.<br>- Publically release a hardware verification platform with functionality evaluated through simulation and emulation of a comprehensive set of digital and mixed signal circuits.<br><br>***FY 2021 Plans:***<br>- Optimize algorithms and the physical design platform to demonstrate path to improvement of power, performance, and area for performance equivalent to traditional best in class techniques.<br>- Extend physical design platform applicability to support large circuits at leading-edge complementary metal oxide-semiconductor technology nodes.<br>- Develop initial SoC design leveraging open source IP building blocks verified with open source simulation technology.<br><br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects the transition from initial design and development to the delivery of functional tools, software, intellectual property, and fabricated hardware. | | | |
| ***Title:*** Common Heterogeneous integration & IP reuse Strategies (CHIPS)<br><br>***Description:*** The Common Heterogeneous integration & IP reuse Strategies (CHIPS) program is developing the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS is pursuing standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets could be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers.<br><br>***FY 2020 Plans:***<br>- Complete module fabrication and testing to demonstrate functionality of the CHIPS interface and chiplets in representative applications. | 15.500 | 17.800 | 7.000 |

| Exhibit R-2A, RDT&E Project Justification: PB 2021 Defense Advanced Research Projects Agency | | Date: February 2020 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Initiate design of upgraded modules to determine performance and program benefits of new processes enabled by the program.<br>- Complete study of the system level impact of IP re-use for the optimal use of digital functional blocks.<br>***FY 2021 Plans:***<br>- Complete design of upgraded modules to determine performance and benefits of new processes enabled by the program.<br>- Demonstrate functionality of the CHIPS interface and chiplets in representative defense applications.<br>- Continue work with transition partners to evaluate the system level impact of CHIPS in DoD applications.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects a shift from module design to module fabrication. | | | |
| ***Title:*** Hierarchical Identify Verify Exploit (HIVE)<br>***Description:*** The Hierarchical Identify Verify Exploit (HIVE) program is pursuing new hardware architectures and algorithms for improving the efficiency of graph and sparse data analytics. When developing operationally significant intelligence, human analysts today are forced to reduce the scope of the problems that they can address and the tempo of their analyses due to the limitations of currently deployed hardware. Because of these limitations the amount of information gathered is quickly outstripping the human ability to review, process, fuse, and interpret. To resolve this challenge, HIVE is leveraging improvements in computational efficiency to augment the analyst's ability to integrate large streams of data. The program is investigating advances in chip architecture and data analytics algorithms that can allow machines to infer meaning out of data based on the information needs of the warfighter. This program will enable the warfighter to understand far more of the battlespace in real time.<br>***FY 2020 Plans:***<br>- Complete development of the Field Programmable Gateway Array (FPGA) emulator and porting of government workflows.<br>- Finalize the chip architecture and deliver design for fabrication.<br>- Complete application programming interface for runtime environment.<br>***FY 2021 Plans:***<br>- Fabricate functional HIVE architecture prototype.<br>- Deliver graph analytic tool set and software stack for use with HIVE chip.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease is the result of development work on architectural design concluding and focusing on delivering final design for fabrication. | 17.600 | 16.510 | 12.000 |
| ***Title:*** Digital RF Battlespace Emulator (DRBE)<br>***Description:*** The Digital RF Battlespace Emulator (DRBE) program is developing a large-scale, interactive, emulated radiofrequency (RF) environment, providing the DoD with much needed capability to cost-effectively evaluate adaptive, intelligent, | 8.000 | 15.000 | 24.000 |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| and spatially distributed next-generation RF systems. Current U.S. test infrastructure is no longer able to successfully exercise RF systems in relevant environments, which should account for hundreds of DoD systems coordinating against hundreds of adversary systems. Due to the critical dependency of nearly all platforms and missions on the RF spectrum and the increasingly advanced RF capabilities of peer adversaries, current infrastructure limitations represent a critical capability gap. Existing test approaches are either: 1) small-scale laboratory tests under well controlled but unrealistic conditions or 2) massive training exercises, which occur at most annually due to the required cost and manpower and do not fully collect necessary data. To overcome these limitations, DRBE is leveraging advances in massively multi-core computing hardware and high-bandwidth digital cross connects to emulate realistic RF environments that account for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. The electronics architecture which supports these goals is beyond anything that exists today, based on the power and latency requirements that this emulation environment demands. DRBE is pursuing three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment will allow plug-and-play connections for hundreds of RF systems in a 100 km battlespace test. Multi-system exercises will then be quickly executed through many different combat scenarios and variations. DRBE is serving to develop concept of operations (CONOPS), inform battle plans, and fine-tune the performance of both individual and large groups of RF systems.<br><br>***FY 2020 Plans:***<br>- Complete first-generation DRBE system design to the level of a Concept Design Review (CoDR).<br>- Complete DRBE real-time High-Performance Computer (HPC) design to the level of a CoDR.<br>- Emulate first-generation DRBE system performance using non-real-time software.<br>***FY 2021 Plans:***<br>- Complete DRBE system design to the level of a Preliminary Design Review (PDR).<br>- Complete DRBE real-time HPC design to the level of a PDR.<br>- Design first-spin computational accelerator chips to the level of tape-out.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects the program shifting from beginning fabrication to completing design of the DRBE system. | | | |
| ***Title:*** Automatic Implementation of Secure Silicon (AISS)*<br>***Description:*** *Previously part of Beyond Scaling - Design<br><br>The Automatic Implementation of Secure Silicon (AISS) program will enable a design tool and Intellectual Property (IP) ecosystem where security is pervasive and can be naturally incorporated into chip design with minimal effort and expense. The program will enable rapid evaluation of architectural alternatives in platform integration where security is considered with conventional design | - | 12.000 | 20.000 |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| economics, together being power, area, speed, and security. The program will advance multi-level provenance and integrity validation techniques for design through advances in current methods or invention of novel technical approaches and demonstrate new capabilities in the context of reduced instruction set computing (RISC) architectures or computer processors. AISS aims to automate inclusion of scalable defense mechanisms into chip designs to enable optimization of the security versus economics trade space. It will protect advanced chips from known attack strategies by incorporating security into a highly automated system aimed at reducing design time while maximizing exploration of architectural alternatives. As a result, the DoD applications will benefit from more secure chips becoming pervasive whether designed specifically for the defense systems or commercially procured.<br><br>***FY 2020 Plans:***<br>- Demonstrate three proof-of-concept (PoC) systems implemented at low, medium and high security levels.<br>- Demonstrate high level synthesis generating register-transfer level design code instrumented with security features, encapsulated in an extensible markup language and accompanied by a corresponding high speed simulation model.<br>***FY 2021 Plans:***<br>- Demonstrate rapid power and security estimation models executed on the auto-integrated PoC systems and accurately grade their relative attack resistivity.<br>- Demonstrate that the three selected PoC designs can be semi-automatically built out of AISS IP and the design finalized.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects a shift from demonstrating the three selected PoC designs can be semi-automatically built out of AISS IP to the final design. | | | |
| ***Title:*** Guaranteed Architectures for Physical Security (GAPS)*<br>***Description:*** *Previously a part of Beyond Scaling - Architectures<br><br>The goal of the Guaranteed Architectures for Physical Security (GAPS) program is to develop hardware security and software architectures with provable security interfaces. These interfaces will physically isolate high risk transactions during both system design and system build and track that such protections are enforced at run-time. GAPS will reduce the inherent complexity through the development of hardware and software that will be open, extendible, and compatible with size, weight, and power constrained environments to enable security across DoD and commercial systems. The program will substantially lower the barrier to safely enabling high-risk transactions, thus allowing for: a) fast computer-to-computer transactions; b) physical spatial isolation reducing the need for unreliable software partitioning solutions; and c) more complex missions without putting sensitive data at risk. | - | 7.000 | 12.000 |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| ***FY 2020 Plans:***<br>- Initiate research to develop a range of capabilities, including verifiable bus standards and board support packages (BSPs), around required components and develop topologies that require minimal feedback while maintaining high reliable throughput.<br>- Research and develop high-level languages capable of expressing unidirectional data-flow assertions and transactions.<br>- Develop novel modelling and compilation techniques to produce physical layouts and multiple binaries.<br>- Identify and create security frameworks for emerging needs for DoD systems and provide interface control documents.<br>***FY 2021 Plans:***<br>- Continue research and development of verifiable bus standards and BSPs while increasing the number of protocol layers.<br>- Extend research and development of high level languages and novel modeling techniques while reducing transaction overhead on embedded devices.<br>- Demonstrate GAPS techniques on DoD platforms.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects a shift from research and development to demonstration of techniques on DoD platforms. | | | |
| ***Title:*** Lasers for Universal Microscale Optical Systems (LUMOS)* | - | 8.000 | 21.000 |
| ***Description:*** *Previously a part of Beyond Scaling - Design<br><br>The Lasers for Universal Microscale Optical Systems (LUMOS) program will integrate high performance light sources into integrated silicon photonics to enable compact, rugged, high-performance systems for positioning, navigation, communications, 3D imaging, and quantum technologies. Silicon photonics today enables microscale integration of complex optical systems, but the platform's lack of optical gain precludes the creation of lasers and amplifiers through foundry processes. LUMOS will deliver the missing capability to provide compact optical sources at wavelengths from the visible to the infrared, and will create a universal manufacturing platform that builds upon the current photonics ecosystem. To drive innovation and maintain DoD access to leading-edge deployable photonic solutions, LUMOS will establish a technology pathway connecting government, academic, commercial, and defense users of integrated photonics, and will provide multi-project wafer runs through an open-access foundry.<br>***FY 2020 Plans:***<br>- Complete a process development evaluation of heterogeneous integration approaches including a discussion of potential risks and component specifications.<br>- Begin development of heterogeneous integration of optical gain on a capable photonics platform.<br>***FY 2021 Plans:*** | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| - Develop heterogeneous integration technology for optical gain and nonlinear photonics components in a complementary metal-oxide semiconductor compatible photonics process.<br>- Create initial process design rules and design methodologies to enable early foundry users to fabricate integrated photonics circuits leveraging novel gain mediums and nonlinear photonic components.<br>- Investigate new materials and components for high-performance lasers at unique wavelengths on emerging platforms.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 increase reflects program going from initial design to fabrication of integrated photonic circuits. | | | |
| ***Title:*** System Security Integrated Through Hardware and firmware (SSITH)<br>***Description:*** The System Security Integrated Through Hardware and firmware (SSITH) program seeks to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. Current responses to cybersecurity attacks typically consist of developing and deploying software patches to address specific vulnerabilities in a software firewall without addressing potential vulnerabilities in the underlying hardware architecture. To address this challenge, SSITH is driving new research in electronics hardware security and exploiting current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas has been enabled by the extremely capable semiconductor technology driven by Moore's Law. The program is also investigating flexible hardware architectures that adapt to and limit the impact of new cybersecurity attacks. Finally, SSITH is mitigating the potential negative impact of new security protection architectures on system performance and power usage. Once developed, SSITH capabilities will be applicable to both commercial and military electronic systems.<br>***FY 2020 Plans:***<br>- Implement new hardware architectures on field programmable gate array (FPGA) platforms that demonstrate scalable, flexible, and robust protection against external attacks on complex, high-performance, out-of-order processing hardware.<br>- Develop distribution-ready design tools to implement SSITH hardware protection methods in new hardware.<br>- Formalize security metrics and establish a clear distribution mechanism for those metrics.<br>***FY 2021 Plans:***<br>- Utilize hardware demonstrations to evaluate the tradeoffs between security, power, and performance of hardware.<br>***FY 2020 to FY 2021 Increase/Decrease Statement:***<br>The FY 2021 decrease reflects the program transitioning from implementing hardware design to testing hardware. | 21.279 | 19.000 | 5.000 |
| ***Title:*** Circuit Realization At Faster Timescales (CRAFT)<br>***Description:*** The Circuit Realization At Faster Timescales (CRAFT) program developed novel integrated circuit (IC) design flows to reduce the design and verification time required for high-performance military electronics by a factor of ten. CRAFT | 9.400 | - | - |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2019 | FY 2020 | FY 2021 |
|---|---|---|---|
| reduced barriers to the design and fabrication of custom ICs in leading-edge complementary metal oxide semiconductor (CMOS) technology. The program investigated and leveraged novel design flows that utilize recent advances in electronic design automation and software design methodologies. CRAFT also explored increased design reuse and flexibility, which will allow DoD to migrate chip fabrication between different foundries or to more advanced technology nodes. | | | |
| ***Title:*** Near Zero Energy RF and Sensor Operations (N-ZERO)<br>***Description:*** The Near Zero Power RF and Sensor Operations (N-ZERO) program developed and demonstrated the technologies required to extend the lifetimes of remotely-deployed sensors from months to years. N-ZERO sought to develop electronics with passive or extremely low-power devices that continuously monitor the environment and wake up active electronics upon detection of a specific trigger. In doing so, N-ZERO enabled wireless sensors with drastically increased mission life to meet DoD's unfulfilled need for a persistent, event-driven sensing capability. | 10.000 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 202.128 | 196.310 | 199.707 |

| | FY 2019 | FY 2020 |
|---|---|---|
| ***Congressional Add:*** DARPA Electronics Resurgence Initiative | 30.000 | - |
| ***FY 2019 Accomplishments:*** - Enhanced ongoing efforts to demonstrate electronics that can enforce security and privacy protections for electronics components critical to DoD overmatch capabilities.<br>- Confirmed via emulation and physical demonstration, that DARPA-developed hardware security technologies can improve the protection of hardware architectures and national critical infrastructure.<br>- Completed abstractions for the physical design of cryptographic hardware intellectual property for use in critical DoD applications.<br>- Incorporated techniques for the physical isolation of sensitive data processing transactions into an application associated with an ongoing DoD program. | | |
| **Congressional Adds Subtotals** | 30.000 | - |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A