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Exhibit R-2, RDT&E Budget Item Justification: PB 2022 Defense Advanced Research Projects Agency **Date:** May 2021

Appropriation/Budget Activity 0400: <i>Research, Development, Test & Evaluation, Defense-Wide I BA 2: Applied Research</i>	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>
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COST (\$ in Millions)	Prior Years	FY 2020	FY 2021	FY 2022 Base	FY 2022 OCO	FY 2022 Total	FY 2023	FY 2024	FY 2025	FY 2026	Cost To Complete	Total Cost
Total Program Element	-	309.811	322.693	357.384	-	357.384	-	-	-	-	-	-
ELT-01: <i>ELECTRONIC TECHNOLOGY</i>	-	116.520	122.986	160.891	-	160.891	-	-	-	-	-	-
ELT-02: <i>BEYOND SCALING TECHNOLOGY</i>	-	193.291	199.707	196.493	-	196.493	-	-	-	-	-	-

A. Mission Description and Budget Item Justification

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter. This Program Element also supports innovation and robust transition planning in the technology cycle by working with entrepreneurs to increase the likelihood that DARPA funded technologies take root in the U.S. and provide new capabilities for national defense.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project will therefore pursue electronics performance advancements that do not rely on Moore's Law but instead exploit new concepts in circuit specialization, by the optimization of materials, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies, this envisioned electronics specialization will require incorporation of security safeguards. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials, and new techniques for securing DoD and commercial data and hardware.

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B. Program Change Summary (\$ in Millions)	FY 2020	FY 2021	FY 2022 Base	FY 2022 OCO	FY 2022 Total
Previous President's Budget	317.192	322.693	357.162	-	357.162
Current President's Budget	309.811	322.693	357.384	-	357.384
Total Adjustments	-7.381	0.000	0.222	-	0.222
• Congressional General Reductions	0.000	0.000			
• Congressional Directed Reductions	0.000	0.000			
• Congressional Rescissions	0.000	0.000			
• Congressional Adds	0.000	0.000			
• Congressional Directed Transfers	0.000	0.000			
• Reprogrammings	2.171	0.000			
• SBIR/STTR Transfer	-9.552	0.000			
• TotalOtherAdjustments	-	-	0.222	-	0.222

Change Summary Explanation

FY 2020: Decrease reflects the SBIR/STTR transfer offset by reprogrammings.

FY 2021: N/A

FY 2022: Increase reflects minor program repricing.

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Appropriation/Budget Activity 0400 / 2					R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>				Project (Number/Name) ELT-01 / <i>ELECTRONIC TECHNOLOGY</i>			
COST (\$ in Millions)	Prior Years	FY 2020	FY 2021	FY 2022 Base	FY 2022 OCO	FY 2022 Total	FY 2023	FY 2024	FY 2025	FY 2026	Cost To Complete	Total Cost
ELT-01: <i>ELECTRONIC TECHNOLOGY</i>	-	116.520	122.986	160.891	-	160.891	-	-	-	-	-	-

A. Mission Description and Budget Item Justification

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

B. Accomplishments/Planned Programs (\$ in Millions)

	FY 2020	FY 2021	FY 2022
<p>Title: Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT)</p> <p>Description: The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program is developing novel magnetic sensors capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. The AMBIIENT program will exploit novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself must be able to detect the gradient of a local magnetic field while subtracting the much larger ambient signal. This would enable low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors promise to enable diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and ultralow frequency communications.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Design sensor package array architecture meeting AMBIIENT size weight and power, and sensitivity goals. - Integrate control electronics for direct gradient sensing of magnetic fields. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Demonstrate AMBIIENT array's medical effectiveness using simulated neural signals. - Test AMBIIENT sensor's sensitivity and dynamic range in government owned and operated facility. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects the shift from final design to testing the AMBIIENT sensor's sensitivity and dynamic range architecture.</p>	10.000	9.000	4.000
<p>Title: Focal Arrays for Curved Infrared Imagers (FOCII)</p>	13.000	19.000	19.750

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B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
<p>Description: The Focal Arrays for Curved Infrared Imagers (FOCII) program is developing curved focal plane arrays for broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. FOCII will leverage curving strategies for state of the art focal plane arrays combined with advances in designing and manufacturing stress relief features to demonstrate hardware that simultaneously provides maximum resolution and illumination. This program will develop novel designs for IR imagers that enable minimal size, weight and cost for size-constrained applications. This will enable new applications in passive seeker technology for missiles, overhead persistent infrared imaging, 360-degree situational awareness, infrared search and track, and long-range targeting.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Measure baseline spectral uniformity of curved large area focal arrays. - Measure mechanical stress of curved large area focal arrays to validate mechanical stress models. - Measure seam width and deviation from sphericity. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Measure operability of large area focal arrays curved to program specified objective radius. - Design and fabricate readout integrated circuits for structured focal arrays. - Measure initial effects of thermal cycling and baking. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects minor program repricing.</p>			
<p>Title: Wideband Adaptive RF Protection (WARP)</p> <p>Description: The Wideband Adaptive RF Protection (WARP) program is developing radio frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference through tunable filtering, limiting, and/or signal cancellation. The ability to create tunable and reconfigurable bandpass and bandstop filters in the range of 2-18 gigahertz will be important for implementing transmit/receive modules in next-generation multi-function arrays. Another important area of interference mitigation is self-interference. WARP will develop the signal cancellation technology that will listen to the transmitted interfering signal and subtract it from the input of the receiver so faint signals near the noise floor can still be detected. Program research will provide feedback mechanisms that intelligently correct these problems. Whether for self-induced interference or external interference jamming, WARP will develop intelligent filtering and self-interference cancellation technologies to protect wideband DoD receivers.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Demonstrate new materials, devices and/or circuit architectures that will enable frequency tuning of band pass and band stop filters in chip-scale size for use in next generation wideband receivers for DoD systems. 	11.200	19.845	19.141

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B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
<p>- Demonstrate new materials, devices and/or circuit architectures that will enable cancellation of signal leakage between two adjacent antennas for simultaneous transmit and receive electronic warfare applications on small platforms.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Demonstrate a 2:1 center frequency tuning range and 3:1 bandwidth tuning range of band pass and band stop filters for use in next generation wideband receivers for DoD systems. - Demonstrate analog signal cancellers covering 0.1-1 gigahertz with 100 megahertz of cancellation bandwidth over a 25 nanosecond leakage path delay spread. - Demonstrate analog signal cancellers covering 1-6 gigahertz with 400 megahertz of cancellation bandwidth over a 5 nanosecond leakage path delay spread. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects minor program repricing.</p>			
<p>Title: Quantum Imaging of Vector Electromagnetic Radiation (QuIVER)</p> <p>Description: The Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) program is developing full tensor magnetic field sensors and will demonstrate them in DoD-relevant applications and concept of operations. In addition to being diagnostically relevant, such sensitive magnetometers could enable future human-machine/brain-machine interfaces. The DoD and industry also use magnetometers for magnetic anomaly detection, which may allow for the discovery of mineral/oil deposits, discovery of old wellheads, or the detection of improvised explosive devices. In addition, magnetometers offer the possibility of magnetic navigation, which may operate in GPS-denied environments. Recent developments have resulted in the potential to develop highly sensitive vector magnetometers, which would enable the consequent development of sensitive full tensor gradient sensors. Such sensors offer more degrees of freedom than their scalar or vector counterparts and potentially provide additional information about the source.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Build preliminary magnetic or electric field tensor gradiometer. - Develop tensor-based algorithms for DoD relevant applications. - Initiate research into building a magnetic or electric field tensor sensor. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Demonstrate sensitivity and functionality of tensor magnetometer. - Design portable tensor magnetometer system for field testing. - Initiate construction of tensor magnetometer system for field testing. <p>FY 2021 to FY 2022 Increase/Decrease Statement:</p>	12.000	20.000	21.000

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B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
The FY 2022 increase reflects a shift from designing to initiating construction of tensor magnetometer system.				
<p>Title: Fast Event-based Neuromorphic Camera and Electronics (FENCE)</p> <p>Description: The Fast Event-based Neuromorphic Camera and Electronics (FENCE) program, building upon technologies developed in the FOCII program (budgeted within this PE and Project) will develop and demonstrate a low latency, low power event-based infrared (IR) camera to enable intelligent sensors for tactical DoD applications. Event-based imagers are an emerging class of sensors with major demonstrated advantages relative to traditional cameras. State of the art visible event-based cameras have been shown to produce over two orders of magnitude less data in optimal conditions relative to traditional framing cameras, because they only transmit data from pixels that have changed. This leads directly to two orders of magnitude lower data latency and a commensurate reduction in power consumption. Despite their inherent advantages, existing event-based cameras are not compatible with DoD applications because DoD applications regularly face conditions that are not naturally sparse, where issues such as clutter and noise would cause a large percentage of the event-based pixels to change simultaneously. When this happens event-based cameras do not perform significantly better than traditional cameras. FENCE will develop an infrared event-based imager consistent with military requirements. FENCE will develop a four megapixel asynchronous read-out integrated circuit (ROIC), co-designed with a 3D integrated processor that will intelligently remove noise and clutter to maintain low power and latency operation even when faced with all of the pixels firing simultaneously. If successful, this new class of sensors enabled by FENCE will be capable of responding to fast moving targets and discriminating dim targets in noisy conditions.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Conduct advanced design review for the ROIC. - Develop preliminary design of the processor layer. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Conduct ROIC preliminary design review. - Simulate timing accuracy and power of the ROIC. - Conduct processor layer preliminary design review. - Perform initial analysis of relevant system parameters including power and latency. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects the shift from concept to design for the ROIC.</p>		-	16.000	24.000
<p>Title: Quantum Apertures (QA)</p> <p>Description: The Quantum Apertures (QA) program, building upon technologies developed in the QuIVER program (budgeted within this PE and Project) will develop novel radio receiver and aperture systems utilizing quantum sensors as the receiving</p>		-	10.000	19.000

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B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
<p>elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly excited "Rydberg" states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical-systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. In this program, the receiver systems enhanced capabilities will also be leveraged to develop novel waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum "Rydberg" receiving elements, lasers to program the sensor and read out radio signals, and processing electronics.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Design quantum aperture sensor for improved sensitivity and frequency range. - Develop government-owned model of quantum aperture receiver for complex signal inputs. - Initiate DoD-relevant application studies that utilize single-element or phased array quantum aperture receiver system. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Demonstrate quantum aperture sensor for sensitivity and frequency tunability. - Complete DoD-relevant application studies that utilize single-element or phased array quantum aperture receiver system. - Complete government-owned model of quantum aperture receiver for complex signal inputs. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects the shift from initial design to demonstrate quantum aperture sensor for sensitivity and frequency tunability.</p>			
<p>Title: Waveform Agile Radio-frequency Directed Energy (WARDEN)</p> <p>Description: The Waveform Agile Radio-frequency Directed Energy (WARDEN) program, building upon technologies developed in the DREaM program (budgeted within this PE and Project) aims to extend the range and lethality of high power microwave (HPM) systems by introducing flexible waveform techniques that use combinations of frequency-, amplitude-, and pulse-width modulations to significantly improve electromagnetic coupling into complex target enclosures and increase the probability of disruption or damage to internal electronic components and circuits. Applications for HPM systems include counter-unmanned aerial systems (C-UAS), vehicle and vessel disruption, electronic strike, and guided missile defense. Current HPM systems use oscillators to produce electromagnetic radiation. These systems are inherently narrowband and lack the frequency agility to support waveforms to maximize electromagnetic coupling and to optimally exploit electronic system vulnerabilities. Lacking the capability to use optimized waveforms, HPM oscillators have been pushed close to the physical limits of peak power generation. To develop a more efficient, lower power, waveform agile approach, the WARDEN program will develop and demonstrate the first</p>	-	6.000	15.000

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B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
broadband HPM amplifier; create new theory and simulation tools to predict electromagnetic coupling into complex enclosures and the effects on electronics; and develop novel agile waveform techniques capable of reducing the susceptibility threshold of targeted electronics systems to HPM attack.				
<p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Perform analysis of existing methods of electromagnetic coupling theory and relevant computational models. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Finalize broadband amplifier design confirmed through 3D simulation. - Develop time-domain electromagnetic coupling theory and demonstrate early concept computational models. - Fabricate broadband amplifier. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 program increase is due to increased amplifier fabrication activities.</p>				
<p>Title: Generating RF with Photonics for low Noise (GRYPHON)</p> <p>Description: The Generating RF with Photonics for low Noise (GRYPHON) program will develop compact sources of microwaves and millimeter waves with extremely low noise. Compact signal sources used today, such as crystal oscillators, are too noisy to support advanced military radar and communications functions. Conversely, best-in-class oscillators which use optical techniques to synthesize extremely pure microwaves are too large and expensive to deploy on the airborne systems, munitions, and other size-constrained platforms where the DoD requires high-performance capabilities. The GRYPHON program will draw on recent advances in miniature optical components in order to replicate best-in-class optical synthesis techniques in microchip form factors.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Develop optical synthesis theoretical models. - Perform initial demonstration of chip-scale component functionality. - Fabricate chip-scale optical components. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects program initiation.</p>		-	-	13.000
<p>Title: COmpact Front-end Filters at the EIEment-level (COFFEE)</p> <p>Description: The COmpact Front-end Filters at the EIEment-level (COFFEE) program will develop and demonstrate compact, high frequency radio frequency (RF) filter technology without compromising low insertion loss and high-power handling. The new filtering technology will enable interference rejection capability, efficient spectral management, and coexistence with commercial 5G applications. It is projected that COFFEE filter technology will enhance the resilience of military microwave and mm-wave</p>		-	-	14.000

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B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>radar and communication systems for DoD spectral dominance into the future. For commercial applications, COFFEE will result in more efficient use of mm-wave frequency allocations for 5G networks.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Design new high frequency resonator technologies significantly smaller than current state of the art electromagnetic resonators. - Demonstrate, through modeling and simulation, the feasibility of high-performance filters using resonators developed in the program. - Initiate fabrication of high frequency resonators. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects program initiation.</p>				
<p>Title: Compact High Intensity Radiating Photonics (CHIRP)</p> <p>Description: The Compact High Intensity Radiating Photonics (CHIRP) program will develop compact, high-power lasers. Current high-power lasers are capable of providing the high optical intensities required to achieve directed energy effects, but the size of these lasers limits their ability to be used on or against highly mobile platforms. CHIRP will decrease the size, weight and power (SWaP) of high-power laser sources by employing emerging integrated photonics and amplification techniques. Additionally, CHIRP will develop high-performance components and package these elements employing innovative thermal management strategies.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Analyze designs for high peak-power laser systems with reduced SWaP. - Initiate development of high efficiency ultra-fast laser components. - Perform initial thermal management analysis for compact, high peak-power laser systems. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects program initiation.</p>		-	-	12.000
<p>Title: Modular Optical Aperture Building Blocks (MOABB)</p> <p>Description: The Modular Optical Aperture Building Blocks (MOABB) program aims to greatly improve the cost, size, weight, and performance of free-space optical systems. These systems enable applications such as Light Detection And Ranging (LIDAR), laser communications, laser illumination, navigation, and 3D imaging. Specifically, MOABB will construct millimeter-scale optical building blocks that can be coherently arrayed to form larger, higher power devices. These building blocks would replace the traditional large and expensive precision lenses and mirrors, which require slow mechanical steering, that form conventional optical systems. MOABB will develop scalable optical phased arrays that can steer light waves without the use of mechanical</p>		19.000	13.141	-

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B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>components. These advances would allow for a 100-fold reduction in size and weight and a 1,000-fold increase in the steering rate of optical systems.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Improve optical phased array LIDAR range. - Demonstrate optical phased array LIDAR on unmanned ground and air vehicles. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects program completion.</p>				
<p>Title: Dynamic Range-enhanced Electronics and Materials (DREaM)</p> <p>Description: The Dynamic Range-enhanced Electronics and Materials (DREaM) program aims to develop intrinsically linear (ideal) radio frequency (RF) transistors with improved power efficiency and extremely high dynamic range. Linearity, power efficiency, and dynamic range are fundamental characteristics that allow RF systems to reliably transmit clear signals. Improving these characteristics is essential to operating in a crowded RF environment and to enabling next-generation communication, sensing, and electronic warfare systems. Traditional RF transistor designs typically require a trade-off between linearity and broadcast power, and poor linearity results in undesired interference. DREAM will overcome this tradeoff by employing new transistor materials, architectures, and designs. The resulting DREAM-enabled technologies will allow future RF electronics to increase their operating range without polluting the already-congested RF spectrum and while consuming less system power.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Optimize novel transistor topology and fabrication processes to enable an output power density five times higher than the state-of-the-art at 94 gigahertz, and identify thermal solutions for high power operation. - Explore new channel materials, device topology and modeling to enable scaling to achieve linearity-to-DC-power ratios ten times better than state-of-the-art at 94 gigahertz. - Design, simulate, fabricate and characterize wideband high power and low noise amplifier integrated circuits to deliver 10 Watts of output power with a factor of four times improvement in the DC-to-millimeter wave power-added efficiency, or a factor of ten better low noise linear amplification over the state-of-the-art between 20 to 40 gigahertz. - Optimize novel transistor topologies and fabrication processes to demonstrate a factor of five improvement in output power density over the state-of-the-art at 94 gigahertz with good DC-to-millimeter wave conversion efficiency. - Explore and demonstrate new channel materials, device topologies, and modeling techniques to enable scaling to linearity-to-DC-power ratio by a factor of ten over than the state-of-the-art at 94 gigahertz. <p>FY 2021 to FY 2022 Increase/Decrease Statement:</p>		17.000	10.000	-

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B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
The FY 2022 decrease reflects program completion.			
<p>Title: SHort Range Independent Microrobotic Platforms (SHRIMP)</p> <p>Description: The SHort Range Independent Microrobotic Platforms (SHRIMP) program developed multi-functional millimeter-to-centimeter scale robotic platforms with a focus on untethered mobility, maneuverability, and dexterity. To achieve this goal, SHRIMP conducted foundational research in the area of micro-actuator materials and energy efficient power systems for extremely size, weight, and power constrained microrobotic systems. The program's platform development activities leveraged recent advances in low power, application specific integrated circuit electronics and low power sensors from the internet of things community to increase the functionality of microrobotic platforms while increasing platform mobility, maneuverability, and dexterity. The future microrobotic platform capabilities enabled by SHRIMP will provide the DoD with capability to operate in small spaces that are practically inaccessible to today's state-of-the-art robotic platforms. Foundational research efforts are funded in PE 0601101E, Project ES-01.</p>	9.000	-	-
<p>Title: High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC)</p> <p>Description: The High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) program developed compact radio frequency signal amplifiers for air, ground, and ship-based communications and sensing systems. HAVOC amplifiers enabled these systems to access the high-frequency millimeter-wave portion of the electromagnetic spectrum, facilitating increased range and other performance improvements. Operating at higher frequencies, such as the millimeter-wave, offers numerous tactical advantages such as high data-rate communications and high resolution and sensitivity for radar and sensors.</p>	6.000	-	-
<p>Title: Precise Robust Inertial Guidance for Munitions (PRIGM)</p> <p>Description: The Precise Robust Inertial Guidance for Munitions (PRIGM) program developed inertial sensor technologies for positioning, navigation, and timing (PNT) in GPS-denied environments. These inertial sensors can provide autonomous PNT information when GPS is unavailable. PRIGM developed and plans to transition a Navigation-Grade Inertial Measurement Unit (NGIMU), a state-of-the-art Microelectromechanical Systems (MEMS) device, to DoD platforms in 2022. These advances should enable navigation applications, such as smart munitions, that require low-cost, size, weight, and power inertial sensors with high bandwidth, precision, and shock tolerance. PRIGM advanced state-of-the-art MEMS gyros from Technology Readiness Level (TRL) 3 devices to a TRL 6 transition platform. Advanced technology development for the program is budgeted in PE 0603739E, Project MT-15.</p>	3.000	-	-
<p>Title: Wafer-scale Infrared Detectors (WIRED)</p>	3.320	-	-

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B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
<p>Description: The Wafer-scale Infrared Detectors (WIRED) program addressed the need for low-cost, high-performance imaging sensors in the short-wave and mid-wave infrared (SWIR/MWIR) bands. These sensors provided increased standoff distances for small unmanned aerial vehicles, low-cost missiles, handheld weapon sights and surveillance systems, helmet-mounted systems, and ground-vehicle-mounted threat warning systems. WIRED manufactured these sensors at the wafer scale, which reduces costs by processing dozens to hundreds of camera imaging arrays at a time. The program significantly reduced the weight and volume of MWIR detectors, which today require heavy cryogenic cooling systems, and increased the resolution of SWIR detectors by dramatically reducing their pixel size relative to the state-of-the-art.</p>			
<p>Title: Atomic Clock with Enhanced Stability (ACES)</p> <p>Description: The Atomic Clock with Enhanced Stability (ACES) program developed extremely stable chip-scale atomic clocks for unmanned aerial vehicles and other low size, weight, and power (SWaP) platforms with extended mission durations. ACES developed the component technologies necessary for low-cost manufacturing and for deployment in harsh DoD-relevant environments. Among its many benefits, the program helped reduce the risk posed by a growing national dependence on GPS, allowing systems to maintain their timing accuracy in the event of temporary GPS unavailability.</p>	6.000	-	-
<p>Title: Limits of Thermal Sensors (LOTS)</p> <p>Description: The Limits of Thermal Sensors (LOTS) program demonstrated long-wave infrared (LWIR) detector technologies with both high performance and low size, weight, power, and cost (SWaP-C). The resulting technologies will enable improvements in imaging systems such as night-vision goggles, infrared-guided missiles, and missile threat warning systems. LOTS developed microbolometers that can compete with larger cameras in terms of higher sensitivity required to detect signals over long ranges and lower response time required to avoid image blur. These technologies will allow DoD to deploy smaller, lighter, and cheaper sensors on critical, high-value assets while maintaining or improving their ability to engage fast-moving or distant targets.</p>	7.000	-	-
Accomplishments/Planned Programs Subtotals	116.520	122.986	160.891

C. Other Program Funding Summary (\$ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency **Date:** May 2021

Appropriation/Budget Activity 0400 / 2					R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>				Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>			
COST (\$ in Millions)	Prior Years	FY 2020	FY 2021	FY 2022 Base	FY 2022 OCO	FY 2022 Total	FY 2023	FY 2024	FY 2025	FY 2026	Cost To Complete	Total Cost
ELT-02: <i>BEYOND SCALING TECHNOLOGY</i>	-	193.291	199.707	196.493	-	196.493	-	-	-	-	-	-

A. Mission Description and Budget Item Justification

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project pursues electronics performance advancements that do not rely on Moore's Law but instead exploit new concepts in circuit specialization, by the optimization of materials, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies, this envisioned electronics specialization will require incorporation of security safeguards. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

B. Accomplishments/Planned Programs (\$ in Millions)

	FY 2020	FY 2021	FY 2022
<p>Title: Beyond Scaling - Materials</p> <p>Description: The Beyond Scaling - Materials program is demonstrating the integration of novel materials into next-generation logic and memory components. This program is pursuing potential enhancements in electronics that do not rely on Moore's Law, i.e. silicon scaling, including research into new materials and the implications of those materials at the device, algorithm, and packaging levels. Research areas include heterogeneous integration of multiple materials, "sticky logic" and novel transistor devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. Further research supports innovation in the technology cycle by working with entrepreneurs focused on DoD-relevant businesses. Basic research for this program is funded within PE 0601101E, Project ES-02.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Test critical mixed-mode demonstration circuit blocks fabricated at a commercial foundry. - Improve switching speed of transistors with enhanced fabrication processes in a commercial foundry. - Release final design tools to be utilized for design of 3D monolithic circuits. - Expand access to the Federally Funded Research and Development Centers (FFRDC) infrastructure to include additional academic researchers, leading to new technology prototypes with a validated path to deployment by U.S. suppliers. - Analyze relevant magnetic materials and perform initial spin wave device design. <p>FY 2022 Plans:</p>	42.981	32.000	16.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<ul style="list-style-type: none"> - Demonstrate the manufacturability of a large-scale fully integrated 3D monolithic system-on-chip, and share design with DoD and commercial end users. - Demonstrate broadband low noise mixed-mode integrated circuits with enhanced transistors in a commercial foundry. - Integrate advanced transistor processing technology and models in a commercial foundry. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects the shift towards demonstrating the ability to take alternative materials through a full commercial process flow.</p>				
<p>Title: Beyond Scaling - Architectures</p> <p>Description: The Beyond Scaling - Architectures program is demonstrating a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program is exploring technologies and techniques such as new domain-specific circuit architectures, co-design of electronics hardware and software, intelligent edge sensors, hardware security architectures, and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Further research will enable significant improvements in programming productivity for massively parallel heterogeneous processing systems (e.g., data centers). Basic research for this program is funded within PE 0601101E, Project ES-02.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Produce, test and demonstrate a specialized processor design executing two simultaneous applications. - Advance the software tools, development technologies, and design methodologies for a system-on-chip with heterogeneous components that can be easily reprogrammed for specialized applications. - Demonstrate field-programmable gate array-based full architecture emulation environments and fully functional software development environments. - Prototype a compiler that demonstrates the feasibility of achieving high levels of productivity, efficiency, portability, and execution speed on a DoD-relevant workload. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Prototype reconfigurable software defined hardware and associated software. - Demonstrate a system-on-chip executing five simultaneous applications utilizing multiple heterogeneous processing elements. - Demonstrate a prototype test bench that can detect anomalous system behavior due to hardware Trojans in complex systems. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects a shift from software enhancement to testing and demonstration.</p>		35.000	31.707	26.000
<p>Title: Beyond Scaling - Design</p>		22.000	25.000	15.493

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2		R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>		Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>Description: The Beyond Scaling - Design program is developing and demonstrating the tools required for rapidly designing and deploying specialized circuits. Research efforts are exploring technologies and techniques for rapid, specialized design such as intelligent design tools, automated physical layout generation, and open-source circuit design. The goal of this program is to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a secure pathway for the rapid upgrade of electronics. Advances under this program demonstrate a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon scaling. Rapid design and deployment techniques developed also consider the need to incorporate security into DoD hardware. Basic research for this program is funded within PE 0601101E, Project ES-02.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Optimize algorithms and the physical design platform to demonstrate a path to improvement of power, performance, and area for performance equivalent to traditional best in-class techniques. - Extend physical design platform applicability to support large circuits at leading-edge complementary metal oxide semiconductor (CMOS) technology nodes. - Develop initial system-on-chip design leveraging open source Intellectual Property (IP) building blocks verified for correctness with open source simulation technologies. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Optimize algorithms and the physical design platform to demonstrate path to improvement of power, performance, and area for performance beyond existing state-of-the-art techniques. - Further develop open source tools to enhance interoperability and integration between tools and move toward a unified chip development infrastructure. - Fabricate and test initial system-on-chip design using open source IP building blocks verified for correctness with open source simulation technologies. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects the transition from development to the delivery of functional tools, software, intellectual property, and fabricated hardware.</p>				
<p>Title: Digital RF Battlespace Emulator (DRBE)</p> <p>Description: The Digital RF Battlespace Emulator (DRBE) program is developing a large-scale, interactive, emulated radio frequency (RF) environment, providing the DoD with the capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. DRBE is leveraging advances in massively multi-core computing hardware and high-bandwidth digital cross-connects to emulate realistic RF environments accounting for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. An electronics architecture supporting the power</p>		15.000	24.000	23.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>and latency requirements demanded by these emulation environments does not currently exist. DRBE is pursuing three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment will allow plug-and-play connections for hundreds of RF systems in a battlespace test. Multi-system exercises will then be quickly executed through many different combat scenarios and variations. DRBE is serving to develop concept of operations (CONOPS), inform battle plans, and fine-tune the performance of both individual and large groups of RF systems.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Complete DRBE real-time High Performance Computer (HPC) design to the level of a Concept Design Review (CoDR). - Complete DRBE system design to the level of a Preliminary Design Review (PDR). <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Complete DRBE real-time HPC design to the level of a PDR. - Complete DRBE system design to the level of a Critical Design Review. - Design first-spin computational accelerator chips to the level of tape-out. - Fabricate and test first-spin computational accelerator chips. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects minor program repricing.</p>				
<p>Title: Automatic Implementation of Secure Silicon (AISS)</p> <p>Description: The Automatic Implementation of Secure Silicon (AISS) program is enabling a design tool and Intellectual Property (IP) ecosystem where security is pervasive and can be naturally incorporated into chip design with minimal effort and expense. The program will enable rapid evaluation of architectural alternatives in platform integration where security is considered with conventional design economics, together being power, area, speed, and security. The program will advance multi-level provenance and integrity validation techniques for design through advances in current methods or invention of novel technical approaches, and will demonstrate new capabilities in the context of reduced instruction set computing (RISC) architectures or computer processors. AISS aims to automate inclusion of scalable defense mechanisms into chip designs to enable optimization of the security versus economics trade space. It will protect advanced chips from known attack strategies by incorporating security into a highly automated system aimed at reducing design time while maximizing exploration of architectural alternatives. As a result, DoD applications will benefit from more secure chips becoming pervasive whether procured commercially or designed specifically for defense systems.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Demonstrate a static implementation of the on-chip Security Engine capable of protecting common attack surfaces. - Demonstrate three proof-of-concept (PoC) systems on the cloud infrastructure. 		12.000	18.000	19.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>- Demonstrate high-level synthesis generating register-transfer level design code instrumented with security features, encapsulated in an extensible markup language and accompanied by a corresponding high-speed simulation model.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Demonstrate automatic generation of the on-chip Security Engine, adjustable to different cost points and defense intensities. - Demonstrate rapid power and security estimation models executed on the auto-integrated PoC systems and accurately grade their relative attack resistivity. - Finalize design and demonstrate that the three selected PoC designs can be semi-automatically built out of AISS IP. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects a shift from PoC to demonstrating the AISS IP.</p>				
<p>Title: Guaranteed Architectures for Physical Security (GAPS)</p> <p>Description: The Guaranteed Architectures for Physical Security (GAPS) program is developing hardware security and software architectures with provable security interfaces. These interfaces will physically isolate high-risk transactions during both system design and system build, and will track that such protections are enforced at run-time. GAPS will reduce the inherent complexity through the development of hardware and software that is open, extendible, and compatible with size, weight, and power constrained environments to enable security across DoD and commercial systems. The program will substantially lower the barrier to safely enabling high-risk transactions, thus allowing for fast computer-to-computer transactions, physical spatial isolation reducing the need for unreliable software partitioning solutions, and more complex missions without putting sensitive data at risk.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Continue research and development of verifiable bus standards and board support packages (BSPs) while increasing the number of protocol layers. - Extend research and development of high-level languages and novel modeling techniques while reducing transaction overhead on embedded devices. - Demonstrate GAPS techniques on platforms representative of DoD systems. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Implement interconnect architectures and BSPs for a single common embedded bus while increasing the number of protocol layers. - Demonstrate a reduction in transaction overhead on embedded busses when implementing GAPS extensions for multilevel security. - Permit at least one gigabit per second sustained throughput across multiple security level architectures. 		7.000	12.000	8.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
- Integrate GAPS isolation techniques to a research application associated with an ongoing DoD platform.				
FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects a shift from demonstration to implementing the GAPS techniques on DoD platforms.				
Title: Lasers for Universal Microscale Optical Systems (LUMOS)		8.000	21.000	23.000
Description: The Lasers for Universal Microscale Optical Systems (LUMOS) program is integrating high-performance light sources into integrated silicon photonics enabling compact, rugged, high-performance systems for positioning, navigation, communications, 3D imaging, and quantum technologies. Silicon photonics today enables microscale integration of complex optical systems, but the platform's lack of optical gain precludes the creation of lasers and amplifiers through foundry processes. LUMOS will deliver the missing capability to provide compact optical sources at wavelengths from the visible to the infrared, and will create a universal manufacturing platform that builds upon the current photonics ecosystem. To drive innovation and maintain DoD access to leading-edge deployable photonic solutions, LUMOS will establish a technology pathway connecting government, academic, commercial, and defense users of integrated photonics, and will provide multi-project wafer runs through an open-access foundry.				
FY 2021 Plans:				
- Complete a process development evaluation of heterogeneous integration approaches including a discussion of potential risks and component specifications.				
- Investigate new materials and components for high-performance lasers at unique wavelengths on emerging platforms.				
FY 2022 Plans:				
- Develop heterogeneous integration technology for optical gain and nonlinear photonics components in a complementary metal-oxide semiconductor (CMOS) compatible photonics process.				
- Create initial process design rules and design methodologies to enable early foundry users to fabricate integrated photonics circuits leveraging novel gain mediums and nonlinear photonic components.				
- Demonstrate active platform components, including modulators and detectors, with high performance.				
FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects the shift from initial design to demonstrating active platform components.				
Title: System Security Integrated Through Hardware and firmware (SSITH)		17.000	9.000	4.000
Description: The System Security Integrated Through Hardware and firmware (SSITH) program seeks to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. Current responses to cybersecurity attacks typically consist of developing and deploying software patches to address specific vulnerabilities in a software firewall without addressing potential vulnerabilities in the				

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
<p>underlying hardware architecture. To address this challenge, SSITH is driving new research in electronics hardware security and exploiting current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas has been enabled by the extremely capable semiconductor technology driven by Moore's Law. The program is also investigating flexible hardware architectures that adapt to and limit the impact of new cybersecurity attacks. Finally, SSITH is mitigating the potential negative impact of new security protection architectures on system performance and power usage. Once developed, SSITH capabilities will be applicable to both commercial and military electronic systems.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Utilize hardware demonstrations to evaluate the tradeoffs between security, power, and performance of hardware. - Organize a second, open, crowd-sourced red team event to evaluate revised security capabilities. - Begin manufacturing of a high-performance, secure SSITH application-specific integrated circuit. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Deliver a high-performance, secure SSITH application-specific integrated circuit (ASIC) for transition and demonstration purposes. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects the shift from testing hardware to transitioning fully secure SSITH ASIC.</p>				
<p>Title: Hierarchical Identify Verify Exploit (HIVE)</p> <p>Description: The Hierarchical Identify Verify Exploit (HIVE) program is pursuing new hardware architectures and algorithms for improving the efficiency of graph and sparse data analytics. When developing operationally significant intelligence, human analysts today are forced to reduce the scope of the problems they can address and the tempo of their analyses due to the limitations of currently deployed hardware. Because of these limitations, the amount of information gathered is quickly outstripping the human ability to review, process, fuse, and interpret. To resolve this challenge, HIVE is leveraging improvements in computational efficiency to augment the analyst's ability to integrate large streams of data. The program is investigating advances in chip architecture and data analytics algorithms that can allow machines to infer meaning out of data based on the information needs of the warfighter. This program will enable the warfighter to understand far more of the battlespace in real time.</p> <p>FY 2021 Plans:</p> <ul style="list-style-type: none"> - Fabricate functional HIVE architecture prototype. - Deliver graph analytic tool set and software stack for use with HIVE architecture. - Deliver single-node HIVE architecture platform. <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Evaluate transition of HIVE architectures defense applications. 		16.510	10.000	7.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021		
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>		
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021	FY 2022
- Initiate design of HIVE platform for specific high performance computing application.				
FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects a shift to transition activities.				
Title: Data Privacy for Virtual Environments (DPRIVE) Description: The Data Privacy in Virtual Environments (DPRIVE) program will enable data privacy at the user and application level, through the development of new hardware accelerators to achieve acceptable computational times. The program plans to provide strong privacy protections at the tactical edge with no more than one order of magnitude penalty in computation time and enable very strong privacy at the enterprise level with no more than three orders of magnitude penalty over unencrypted processing. DPRIVE will build hardware to accelerate the computation of homomorphic encryption, which enables mathematical operations to execute on encrypted data such that the data is never unencrypted. The program will enable the development and deployment of these hardware accelerators to edge computing devices where power and time are a premium as well as enterprise computing facilities where the amount and sensitivity of the data requires increased protection. The DPRIVE program was originally funded within PE 0602716E, ELT-01. FY 2021 Plans: - Develop algorithms and simulate performance for both edge and enterprise mission sets. - Create a hardware design model. - Prove the ability to compute deep neural networks on encrypted data. FY 2022 Plans: - Design an accelerator that is ready for fabrication. - Emulate integrated accelerator design for relevant workloads. - Verify accelerator design through appropriate testing. FY 2021 to FY 2022 Increase/Decrease Statement: The FY2022 increase reflects the shift from concept development to designing an accelerator for fabrication.		-	10.000	18.000
Title: Ferroelectric Computing (FC) Description: The Ferroelectric Computing (FC) program will develop low energy ferroelectric technology for dense and scalable computing performance. Current state of the art silicon devices are not capable of scaling to the performance and efficiency levels necessary for future data-centric architectures and applications in high performance computing. This program addresses this need by developing ferroelectric transistor technology for next-generation power-efficient and scalable computing that is readily integrated into current complementary metal oxide semiconductor (CMOS) fabrication process flows.		-	-	10.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021	
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>	
B. Accomplishments/Planned Programs (\$ in Millions)		FY 2020	FY 2021
<p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Perform initial designs of novel ferroelectric transistors that are fast, dense, and energy efficient. - Initiate plans to integrate novel ferroelectric transistors into state of the art silicon technology. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects program initiation.</p>			
<p>Title: Low Temperature Logic Technology (LTLT)</p> <p>Description: The Low Temperature Logic Technology (LTLT) program will exploit the unique device and material performance characteristics of state-of-the-art silicon transistors at cryogenic temperatures. Current silicon transistors are performance and power limited when operating at room temperature or higher. This program removes these limitations through modifying the design of existing silicon transistors to optimize their performance at cryogenic temperatures. These devices will be compatible with current complementary metal-oxide-semiconductor (CMOS) fabrication process flows and will offer significant increases in performance and power efficiency over room temperature devices.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Perform initial design of transistor, memory, and interconnect technologies that are optimized for low temperature operation. - Initiate plans to modify the fabrication flow for state of the art silicon technology for transistors with optimized cryogenic performance. <p>FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 increase reflects program initiation.</p>		-	-
<p>Title: Quantum Inspired Classical Computing (QuICC)</p> <p>Description: The Quantum Inspired Classical Computing (QuICC) program will implement quantum-inspired algorithms using classical dynamic systems in novel computing architectures for the efficient solving of complex optimization problems. Currently, too much computational energy is required to solve mission-scale optimization problems leading to sub-optimal solutions and excessive computation times. This program will create frameworks for analyzing the computational advantage provided by quantum-inspired algorithms and perform the hardware and algorithm co-design needed to reduce the required energy to optimally solve mission-scale problems.</p> <p>FY 2022 Plans:</p> <ul style="list-style-type: none"> - Initiate development of quantum inspired algorithms for scalable optimization problems on classical hardware. - Perform initial hardware and algorithm co-design analysis for representative mission-scale optimization problems. <p>FY 2021 to FY 2022 Increase/Decrease Statement:</p>		-	-
		15.000	12.000

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Exhibit R-2A, RDT&E Project Justification: PB 2022 Defense Advanced Research Projects Agency		Date: May 2021
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / <i>ELECTRONICS TECHNOLOGY</i>	Project (Number/Name) ELT-02 / <i>BEYOND SCALING TECHNOLOGY</i>

B. Accomplishments/Planned Programs (\$ in Millions)	FY 2020	FY 2021	FY 2022
The FY 2022 increase reflects program initiation.			
Title: Common Heterogeneous integration and IP reuse Strategies (CHIPS)	17.800	7.000	-
Description: The Common Heterogeneous integration and IP reuse Strategies (CHIPS) program is developing the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS is pursuing standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets can be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers.			
FY 2021 Plans: - Demonstrate IP re-use of commercial off-the-shelf circuit designs for integration into the CHIPS platform. - Demonstrate functionality of the CHIPS interface and chiplets in representative defense applications. - Continue work with transition partners to evaluate the system-level impact of CHIPS in DoD applications.			
FY 2021 to FY 2022 Increase/Decrease Statement: The FY 2022 decrease reflects program completion.			
Accomplishments/Planned Programs Subtotals	193.291	199.707	196.493

C. Other Program Funding Summary (\$ in Millions) N/A
Remarks
D. Acquisition Strategy N/A