Exhibit R-2, RDT&E Budget Item Justification: PB 2023 Defense Advanced Research Projects Agency	**Date:** April 2022
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

COST ($ in Millions)	Prior Years	FY 2021	FY 2022	FY 2023 Base	FY 2023 OCO	FY 2023 Total	FY 2024	FY 2025	FY 2026	FY 2027	Cost To Complete	Total Cost
Total Program Element	-	307.791	393.384	557.745	-	557.745	571.062	565.566	587.146	586.896	-	-
ELT-01: *ELECTRONIC TECHNOLOGY*	-	113.633	160.891	136.744	-	136.744	143.985	142.356	139.622	146.872	-	-
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	194.158	232.493	421.001	-	421.001	427.077	423.210	447.524	440.024	-	-

A. Mission Description and Budget Item Justification

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter. This Program Element also supports innovation and robust transition planning in the technology cycle by working with entrepreneurs to increase the likelihood that DARPA funded technologies take root in the U.S. and provide new capabilities for national defense.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project pursues electronics performance advancements that exploit new concepts in circuit specialization by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies, this envisioned electronics specialization will require incorporation of security safeguards. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

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B. Program Change Summary ($ in Millions)	FY 2021	FY 2022	FY 2023 Base	FY 2023 OCO	FY 2023 Total
Previous President's Budget	322.693	357.384	0.000	-	0.000
Current President's Budget	307.791	393.384	557.745	-	557.745
Total Adjustments	-14.902	36.000	557.745	-	557.745
• Congressional General Reductions	0.000	0.000			
• Congressional Directed Reductions	0.000	0.000			
• Congressional Rescissions	0.000	0.000			
• Congressional Adds	0.000	36.000			
• Congressional Directed Transfers	0.000	0.000			
• Reprogrammings	-4.512	0.000			
• SBIR/STTR Transfer	-10.390	0.000			
• Adjustments to Budget Year	-	-	557.745	-	557.745

Congressional Add Details ($ in Millions, and Includes General Reductions)	FY 2021	FY 2022
Project: ELT-02: *BEYOND SCALING TECHNOLOGY*		
Congressional Add: *ERI 2.0 - Congressional Add*	-	36.000
Congressional Add Subtotals for Project: ELT-02	-	36.000
Congressional Add Totals for all Projects	-	36.000

Change Summary Explanation

FY 2021: Decrease reflects reprogrammings and SBIR/STTR transfer.
FY 2022: Increase reflects a Congressional add for ERI 2.0.
FY 2023: FY 2023 funding increase reflects the fact that the FY 2022 President's Budget request did not include out-year funding.

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency			Date: April 2022
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*	

COST ($ in Millions)	Prior Years	FY 2021	FY 2022	FY 2023 Base	FY 2023 OCO	FY 2023 Total	FY 2024	FY 2025	FY 2026	FY 2027	Cost To Complete	Total Cost
ELT-01: *ELECTRONIC TECHNOLOGY*	-	113.633	160.891	136.744	-	136.744	143.985	142.356	139.622	146.872	-	-

A. Mission Description and Budget Item Justification

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
Title: Focal Arrays for Curved Infrared Imagers (FOCII)	19.000	21.750	12.139

Description: The Focal Arrays for Curved Infrared Imagers (FOCII) program is developing curved focal plane arrays for broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. FOCII will leverage curving strategies for state-of-the-art focal plane arrays combined with advances in designing and manufacturing stress relief features to demonstrate hardware that simultaneously provides maximum resolution and illumination. This program will develop novel designs for IR imagers that enable minimal size, weight and cost for size-constrained applications. This will enable new applications in passive seeker technology for missiles, overhead persistent infrared imaging, 360-degree situational awareness, infrared search and track, and long-range targeting.

FY 2022 Plans:
- Measure operability of large area focal arrays curved to program specified objective radius.
- Design and fabricate readout integrated circuits for structured focal arrays.
- Measure initial effects of thermal cycling and baking.

FY 2023 Plans:
- Demonstrate large area focal array curved to final program specified objective radius.
- Complete preliminary camera design with curved structured focal array.
- Measure curved focal array performance on laboratory scale test equipment.

FY 2022 to FY 2023 Increase/Decrease Statement:

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
The FY 2023 decrease reflects the shift from design and fabrication to demonstration and testing.			
Title: Wideband Adaptive RF Protection (WARP)	19.845	20.141	17.000
Description: The Wideband Adaptive RF Protection (WARP) program is developing radio frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference through tunable filtering, limiting, and/or signal cancellation. The ability to create tunable and reconfigurable band pass and band stop filters in the range of 2 gigahertz (GHz) to 8 GHz will be important for implementing transmit/receive modules in next-generation multi-function arrays. Another important area of interference mitigation is self-interference. WARP is developing the signal cancellation technology that will listen to the transmitted interfering signal and subtract it from the input of the receiver so faint signals near the noise floor can still be detected. Program research will provide feedback mechanisms that intelligently correct these problems. Whether for self-induced interference or external interference jamming, WARP is developing intelligent filtering and self-interference cancellation technologies to protect wideband DoD receivers. ***FY 2022 Plans:*** - Demonstrate a center frequency and bandwidth tuning range of band pass and band stop filters that aligns with the need to protect wideband digital receivers. - Demonstrate analog signal cancellers that mitigate transmitter self-leakage into a wideband receiver and while achieving relevant bandwidth and delay spread. - Evaluate scalability of candidate approaches for wideband adaptive filtering and signal cancellation architectures to achieve desired RF protection. ***FY 2023 Plans:*** - Demonstrate wideband adaptive filters that implement embedded interference sensing and closed-loop adaptive tuning. - Demonstrate analog signal cancellers that implement embedded leakage channel sensing and closed-loop adaptive tuning. - Prepare demonstration of the RF protection technology that is well-aligned to transition partners within the government. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects the transition from initial component demonstration to component scaling.			
Title: Quantum Imaging of Vector Electromagnetic Radiation (QuIVER)	20.000	21.000	15.000
Description: The Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) program is developing full-tensor magnetic field sensors and will demonstrate them in DoD-relevant applications and concept of operations. In addition to being diagnostically relevant, such sensitive magnetometers could enable future human-machine/brain-machine interfaces. The DoD and industry also use magnetometers for magnetic anomaly detection, which may allow for the discovery of mineral/oil deposits, discovery of old wellheads, or the detection of improvised explosive devices. In addition, magnetometers offer the possibility of magnetic			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
navigation, which may operate in GPS-denied environments. Recent advancements have resulted in the potential to develop highly-sensitive vector magnetometers, which would enable the consequent development of sensitive full-tensor gradient sensors. Such tensors offer more degrees of freedom than their scalar or vector counterparts and potentially provide additional information about the source of the magnetic field. ***FY 2022 Plans:*** - Demonstrate sensitivity and functionality of tensor magnetometer. - Design portable tensor magnetometer system for field testing. - Initiate construction of tensor magnetometer system for field testing. ***FY 2023 Plans:*** - Validate sensitivity and functionality of tensor magnetometer. - Complete construction of tensor magnetometer system for field testing. - Field test tensor magnetometer system. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects the completion of system construction and transition to testing.			
Title: Fast Event-based Neuromorphic Camera and Electronics (FENCE) ***Description:*** The Fast Event-based Neuromorphic Camera and Electronics (FENCE) program will develop and demonstrate a low latency, low power event-based infrared (IR) camera to enable intelligent sensors for tactical DoD applications. Event-based imagers are an emerging class of sensors with major demonstrated advantages relative to traditional cameras. State-of-the-art visible event-based cameras have been shown to produce over two orders of magnitude less data in optimal conditions relative to traditional framing cameras because they transmit data only from pixels that have changed. This leads directly to two orders of magnitude lower data latency and a commensurate reduction in power consumption. Despite their inherent advantages, existing event-based cameras are not compatible with DoD applications because DoD applications regularly face conditions that are not naturally sparse, where issues such as clutter and noise would cause a large percentage of the event-based pixels to change simultaneously. When this happens, today's event-based cameras do not perform significantly better than traditional cameras. FENCE will develop an infrared event-based imager consistent with military requirements. FENCE will develop a four-megapixel asynchronous read-out integrated circuit (ROIC), co-designed with a 3D integrated processor that will intelligently remove noise and clutter to maintain low power and latency operation even when faced with all of the pixels firing simultaneously. If successful, this new class of sensors enabled by FENCE will be capable of responding to fast moving targets and discriminating dim targets in noisy conditions. ***FY 2022 Plans:***	16.000	24.000	20.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Conduct ROIC preliminary design review. - Simulate timing accuracy and power of the ROIC. - Conduct processor layer preliminary design review. - Perform initial analysis of relevant system parameters including power and latency. ***FY 2023 Plans:*** - Measure ROIC power and timing fidelity. - Conduct critical design review of processor layer. - Fabricate processor layer in advanced node silicon. - Measure processing layer power consumption. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects the shift from ROIC design and simulations to processing layer design and fabrication.			
Title: Quantum Apertures (QA)	15.000	19.000	16.000
Description: The Quantum Apertures (QA) program will develop novel radio receiver and aperture systems using quantum sensors as the receiving elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly-excited "Rydberg" states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. The receiver system's enhanced capabilities will be leveraged in this program to develop novel waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum receiving elements, lasers to program the sensor and read out radio signals, and processing electronics. ***FY 2022 Plans:*** - Demonstrate quantum aperture sensor sensitivity and frequency tunability. - Complete government-owned model of quantum aperture receiver for complex signal inputs. - Complete DoD-relevant application studies that use a single-element or phased array quantum aperture receiver system. ***FY 2023 Plans:*** - Develop architecture for quantum aperture sensors in multiple-element arrays. - Demonstrate reception of novel waveforms by quantum aperture.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Design system to use a single quantum aperture sensor in a DoD-relevant application. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects the shift from development of multiple models and application studies to development of a specific architectures and system designs.			
Title: Waveform Agile Radio-frequency Directed Energy (WARDEN)	6.000	20.000	23.000
Description: The Waveform Agile Radio-frequency Directed Energy (WARDEN) program aims to extend the range and lethality of high-power microwave (HPM) systems by introducing flexible waveform techniques that use combinations of frequency, amplitude, and pulse-width modulations to significantly improve electromagnetic coupling into complex target enclosures and increase the probability of disruption or damage to internal electronic components and circuits. Applications for HPM systems include counter-unmanned aerial systems (C-UAS), vehicle and vessel disruption, electronic strike, and guided missile defense. Current HPM systems use oscillators to produce electromagnetic radiation. These systems are inherently narrowband and lack the frequency agility to support waveforms to maximize electromagnetic coupling and to optimally exploit electronic system vulnerabilities. Lacking the capability to use optimized waveforms, HPM oscillators have been pushed close to the physical limits of peak power generation. To develop a more efficient, lower power, waveform agile approach, the WARDEN program will develop and demonstrate the first broadband HPM amplifier; create new theory and simulation tools to predict electromagnetic coupling into complex enclosures and the effects on electronics; and develop novel agile waveform techniques capable of reducing the susceptibility threshold of targeted electronics systems to HPM attack. ***FY 2022 Plans:*** - Develop broadband amplifier designs and verify them through 3D simulation. - Develop time-domain electromagnetic coupling theory and demonstrate early concept computational models. - Develop initial electronic effects models and demonstrate agile waveforms optimized for effects on basic electronics. ***FY 2023 Plans:*** - Finalize broadband amplifier designs and initiate fabrication, procurement, and laboratory preparation. - Develop initial hybrid electromagnetic coupling tools that combine deterministic, reduced-model, and statistical approaches. - Develop predictive models and agile waveform techniques to produce disruptive effects on integrated electronics. - Validate electromagnetic coupling tools, predictive models, and agile waveform techniques through comparison with experimental measurements. - Develop high current electron gun and high power, broadband amplifier designs and verify them through 3D simulation. ***FY 2022 to FY 2023 Increase/Decrease Statement:***			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
The FY 2023 increase reflects the transition from initial development to initiation of fabrication.			
Title: Generating RF with Photonics for low Noise (GRYPHON) ***Description:*** The Generating RF with Photonics for low Noise (GRYPHON) program will develop compact sources of microwaves and millimeter waves with extremely low phase noise. Compact signal sources used today, such as crystal oscillators, are too noisy to support advanced military radar and communications functions. Conversely, best-in-class oscillators which use optical techniques to synthesize extremely pure microwaves are too large and expensive to deploy on the airborne systems, munitions, and other size-constrained platforms where the DoD requires high-performance capabilities. The GRYPHON program will draw on recent advances in miniature optical components to replicate best-in-class optical frequency synthesis techniques in microchip form factors. ***FY 2022 Plans:*** - Develop optical synthesis theoretical models. - Design and fabricate chip-scale optical components. - Perform initial demonstration of chip-scale component functionality. ***FY 2023 Plans:*** - Perform benchtop-level integration of components. - Setup characterization equipment and frequency references for phase noise measurements. - Demonstrate microwave generation at a fixed frequency. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects the shift from the initial chip-scale demonstration to integration of components testing and characterization.	-	17.000	21.000
Title: Compact High Intensity Radiating Photonics (CHIRP) ***Description:*** The Compact High Intensity Radiating Photonics (CHIRP) program will develop compact, ultra-fast, high-power lasers. Current high-power lasers are capable of providing the high optical intensities required to achieve directed energy effects, but the size of these lasers limits their ability to be used on or against highly mobile platforms. CHIRP will decrease the size, weight and power (SWaP) of ultra-fast laser sources by employing emerging integrated photonics and amplification techniques. Additionally, CHIRP will develop high-performance components and package these elements employing innovative thermal management strategies. ***FY 2022 Plans:*** - Analyze designs for high peak-power laser systems with reduced SWaP.	-	12.000	12.605

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Initiate development of high efficiency ultra-fast laser components. ***FY 2023 Plans:*** - Begin development of materials for high performance at high optical intensities. - Perform initial thermal management analysis for compact, high peak-power laser systems. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects minor program repricing.			
Title: Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) ***Description:*** The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program is developing novel magnetic sensors capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. The AMBIIENT program will exploit novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself must be able to detect the gradient of a local magnetic field while subtracting the much larger ambient signal. This capability would enable low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors promise to enable diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and ultra-low frequency communications. ***FY 2022 Plans:*** - Demonstrate medical effectiveness of the AMBIIENT array using simulated neural signals. - Test AMBIIENT sensor sensitivity and dynamic range in government owned and operated facility. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects program completion.	4.788	6.000	-
Title: Modular Optical Aperture Building Blocks (MOABB) ***Description:*** The Modular Optical Aperture Building Blocks (MOABB) program greatly improved the cost, size, weight, and performance of free-space optical systems. Specifically, MOABB constructed millimeter-scale optical building blocks that can be coherently arrayed to form larger, higher power devices. MOABB developed scalable optical phased arrays that can steer light waves without the use of mechanical components. These advances allow for a 100-fold reduction in size and weight and a 1,000-fold increase in the steering rate of optical systems.	4.000	-	-
Title: Dynamic Range-enhanced Electronics and Materials (DREaM) ***Description:*** The Dynamic Range-enhanced Electronics and Materials (DREaM) program developed intrinsically linear (ideal) radio frequency (RF) transistors with improved power efficiency and extremely high dynamic range. Linearity, power efficiency, and dynamic range are fundamental characteristics that allow RF systems to reliably transmit clear signals. Improving these	9.000	-	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
characteristics is essential to operating in a crowded electromagnetic spectrum environment and to enabling next-generation communication, sensing, and electronic warfare systems. Traditional RF transistor designs typically require a trade-off between linearity and output power, and poor linearity results in undesired interference. DREAM overcame this tradeoff by employing new transistor materials, architectures, and designs. The resulting DREAM-enabled technologies will allow future RF electronics to increase their operating range while consuming less system power, without adding interference to the already-congested electromagnetic spectrum.			
Accomplishments/Planned Programs Subtotals	113.633	160.891	136.744

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

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COST ($ in Millions)	Prior Years	FY 2021	FY 2022	FY 2023 Base	FY 2023 OCO	FY 2023 Total	FY 2024	FY 2025	FY 2026	FY 2027	Cost To Complete	Total Cost
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	194.158	232.493	421.001	-	421.001	427.077	423.210	447.524	440.024	-	-

A. Mission Description and Budget Item Justification

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project pursues electronics performance advancements that exploit new concepts in circuit specialization and three-dimensional heterogeneous integration (3DHI) by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our -microelectronics infrastructure relies, this envisioned specialization will require incorporation of security safeguards and advancing manufacturing tools and process automation. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and 3DHI by improving producibility. This will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized microelectronics, particularly for operation in extreme environments. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting 3DHI to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
Title: Digital RF Battlespace Emulator (DRBE)	24.000	23.000	22.000

Description: The Digital RF Battlespace Emulator (DRBE) program is developing a large-scale, interactive, emulated radio frequency (RF) environment, providing the DoD with the capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. DRBE is leveraging advances in massively multi-core computing hardware and high-bandwidth digital cross-connects to emulate realistic RF environments accounting for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. An electronics architecture supporting the power and latency requirements demanded by these emulation environments does not currently exist. DRBE is pursuing three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment will allow plug-and-play connections for hundreds of RF systems in a battlespace test. Multi-system exercises will then be quickly executed through many different combat scenarios and variations. DRBE is serving to develop concept of operations (CONOPS), inform battle plans, and fine-tune the performance of both individual and large groups of RF systems.

FY 2022 Plans:
- Complete DRBE real-time High Performance Computer (HPC) design to the level of a Preliminary Design Review.
- Complete DRBE system design to the level of a Critical Design Review.
- Design, fabricate, and test computational accelerator chips.

FY 2023 Plans:

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Complete DRBE real-time HPC design to the level of Critical Design Review. - Validate DRBE system design following the Critical Design Review. - Demonstrate real-time RF emulation on computational accelerator chip. - Establish agreement to transition DRBE to DoD laboratory. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects minor program repricing.			
Title: Low Temperature Logic Technology (LTLT) ***Description:*** The Low Temperature Logic Technology (LTLT) program will exploit the unique device and material performance characteristics of state-of-the-art silicon transistors at cryogenic temperatures. Current silicon transistors are performance and power limited when operating at room temperature or higher. This program removes these limitations through modifying the design of existing silicon transistors to optimize their performance at cryogenic temperatures. These devices will be compatible with current complementary metal-oxide-semiconductor (CMOS) fabrication process flows and will offer significant increases in performance and power efficiency over room temperature devices. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2022 Plans:*** - Perform initial design of transistor, memory, and interconnect technologies that are optimized for low temperature operation. - Initiate plans to modify the fabrication flow for state-of-the-art silicon technology for transistors with optimized cryogenic performance. ***FY 2023 Plans:*** - Complete design of transistor, memory, and interconnect technologies that are optimized for low temperature operation. - Develop high speed, low power switching devices and experimentally demonstrate their performance at low temperature. - Demonstrate a low power and high-performance memory unit at low temperature. - Continue improving low-temperature device characteristics to enhance performance. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects transition from design to component fabrication and testing.	-	15.000	22.000
Title: Automatic Implementation of Secure Silicon (AISS) ***Description:*** The Automatic Implementation of Secure Silicon (AISS) program is enabling a design tool and Intellectual Property (IP) ecosystem where security is pervasive and can be incorporated naturally into chip design with minimal effort and expense. The program will enable rapid evaluation of architectural alternatives in platform integration where security can be optimized relative to the conventional design economic measure of power, area, and speed. The program will advance multi-level	18.000	18.000	21.700

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
provenance and integrity validation techniques for design through improvement of current methods or invention of novel technical approaches, and will demonstrate new capabilities in the context of reduced instruction set computing (RISC) architectures or computer processors. AISS will protect advanced chips from known attack strategies by incorporating security into a highly automated system aimed at reducing design time while maximizing exploration of architectural alternatives. As a result, DoD applications will benefit from more secure chips becoming pervasive whether procured commercially or designed specifically for defense systems. ***FY 2022 Plans:*** - Demonstrate automatic generation of the on-chip Security Engine, adjustable to different cost points and defense intensities. - Demonstrate rapid power and security estimation models executed on the auto-integrated proof-of-concept (PoC) systems and accurately grade their relative attack resistivity. - Finalize design and demonstrate that the two selected PoC designs can be built semi-automatically using AISS IP. ***FY 2023 Plans:*** - Develop additional static components including balanced and noisy cryptography cores, boot and activity odometers. - Add features to support bus monitoring and uploading of security policies. - Develop a threat analysis prototype and a library of heuristics. - Demonstrate optimized generation of two selected PoC designs can be built semi-automatically using AISS IP. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects a shift from modeling and design to prototype development and testing.			
Title: Lasers for Universal Microscale Optical Systems (LUMOS) ***Description:*** The Lasers for Universal Microscale Optical Systems (LUMOS) program is integrating high-performance light sources into silicon integrated photonics enabling compact, rugged, high-performance systems for positioning, navigation, communications, 3D imaging, and quantum technologies. Silicon photonics today enables microscale integration of complex optical systems, but the platform's lack of optical gain precludes the creation of lasers and amplifiers through foundry processes. LUMOS will deliver the missing capability to provide compact optical sources at wavelengths from the visible to the infrared, and will create a universal manufacturing platform that builds upon the current photonics ecosystem. To drive innovation and maintain DoD access to leading-edge deployable photonic solutions, LUMOS will establish a technology pathway connecting government, academic, commercial, and defense users of integrated photonics, and will provide multi-project wafer runs through an open-access foundry. ***FY 2022 Plans:***	21.000	23.000	18.000

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Develop heterogeneous integration technology for optical gain and nonlinear photonics components in a complementary metal-oxide semiconductor (CMOS) compatible photonics process. - Create initial process design rules and design methodologies to enable early foundry users to fabricate integrated photonics circuits leveraging novel gain mediums and nonlinear photonic components. - Demonstrate active platform components, including modulators and detectors, with high performance. ***FY 2023 Plans:*** - Optimize high-performance lasers and optical amplifiers while providing designers access through first active foundry runs. - Begin layout and characterization of advanced lasers, and testing of essential demonstration components. - Scale optical power and component bandwidth for integrated microwave-compatible platform. - Demonstrate narrow linewidth lasers at design wavelengths on integrated visible platform. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects transition from fabrication and initial demonstration to optimization and component characterization.			
Title: COmpact Front-end Filters at the ElEment-level (COFFEE) ***Description:*** The COmpact Front-end Filters at the ElEment-level (COFFEE) program will develop and demonstrate compact, high frequency radio frequency (RF) filter technology without compromising performance, specifically low insertion loss and high power handling. The new filtering technology will enable interference rejection capability, efficient spectral management, and coexistence with commercial 5G applications. It is projected that COFFEE filter technology will enhance the resilience of military microwave and mm-wave radar and communication systems for DoD spectral dominance into the future. For commercial applications, COFFEE will result in more efficient use of mm-wave frequency allocations for 5G networks. The COFFEE program was originally funded within PE 0602716E, ELT-01. ***FY 2022 Plans:*** - Design new high frequency resonator technologies that are significantly smaller than current state-of-the-art electromagnetic resonators. - Demonstrate, through modeling and simulation, the feasibility of high-performance filters using resonators developed in the program. - Initiate fabrication of high frequency resonators. ***FY 2023 Plans:*** - Verify and validate performance of new high frequency resonators in the laboratory. - Demonstrate new high frequency resonators and evaluate performance against program technical metrics.	-	12.000	17.000

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Integrate new high frequency resonators into new high-performance filters. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects the program moving from design to component demonstration and integration.			
Title: ELectronics for G-band ARrays (ELGAR) ***Description:*** The ELectronics for G-band ARrays (ELGAR) program, building upon technologies developed in the LUMOS program (budgeted within this PE and Project) will develop the integration technologies needed to create compact, high-performance G-band array front-end electronics to enable phased array antenna systems for DoD communications and sensing. ELGAR will address the key technical challenges that prevent III-V electronics from realizing high-performance G-band arrays, namely, 1) achieving efficient, compact G-band III-V monolithic microwave/millimeter wave integrated circuit power amplifiers (MMIC PAs) with high output power density, and 2) achieving low loss off-chip interconnects between adjacent G-band array components. In particular, ELGAR will develop III-V compatible, silicon like fabrication and integration approaches to enable compact, high power density, high efficiency G-band MMICs and arrays. The technologies developed will support transitions including enabling emerging satellite communication and sensing missions to provide enhanced situational awareness. ***FY 2022 Plans:*** - Initiate development of III-V semiconductor compatible silicon-like multilayer interconnects and integration processes. - Design and fabricate 1) compact, low loss passive component test structures, 2) compact, multi-finger III-V transistor test structures whose power and efficiency are not degraded by the silicon-like interconnects, and 3) high aspect ratio, solid filled III-V through substrate via (TSV) test structures. ***FY 2023 Plans:*** - Continue to compact and reduce the loss of the III-V semiconductor compatible silicon-like multilayer interconnects, integration processes, and test structures. - Design, fabricate, and characterize compact G-band III-V MMIC PAs that use the silicon-like multilayer interconnects. - Design, fabricate, and characterize low loss, array-level interconnects for integration of G-band PAs with other array components. - Perform design of III-V circuits and transmitters with spectrally pure output. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects the program moving from initial design to fabrication and characterization of components.	-	7.000	16.000
Title: Data Privacy for Virtual Environments (DPRIVE) ***Description:*** The Data Privacy in Virtual Environments (DPRIVE) program will enable homomorphic encryption for data privacy at the user and application level through the development of new hardware accelerators to achieve acceptable computational	10.000	16.000	15.960

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
times. The program plans to provide strong privacy protections at the tactical edge with no more than one order of magnitude penalty in computation time, and to enable very strong privacy at the enterprise level with no more than three orders of magnitude penalty over unencrypted processing. DPRIVE will build hardware to accelerate the computation of homomorphic encryption, which enables mathematical operations to execute on encrypted data such that the data is never unencrypted. The program will enable the development and deployment of these hardware accelerators to edge computing devices where power and time are a premium, as well as to enterprise computing facilities where the amount and sensitivity of the data requires increased protection. ***FY 2022 Plans:*** - Design an accelerator that is ready for fabrication. - Emulate integrated accelerator design for relevant workloads. - Verify accelerator design through appropriate testing. ***FY 2023 Plans:*** - Fabricate DPRIVE accelerator design in advanced node complementary metal oxide semiconductor (CMOS). - Execute and demonstrate mission workloads with full design simulations. - Complete full DPRIVE accelerator software integration. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY2023 decrease reflects minor program repricing.			
Title: Quantum Inspired Classical Computing (QuICC) ***Description:*** The Quantum Inspired Classical Computing (QuICC) program will implement quantum-inspired algorithms using classical dynamic systems in novel computing architectures for the efficient solving of complex optimization problems. Currently, too much computational energy is required to solve mission-scale optimization problems leading to sub-optimal solutions and excessive computation times. This program will create frameworks for analyzing the computational advantage provided by quantum-inspired algorithms and perform the hardware and algorithm co-design needed to reduce the required energy to optimally solve mission-scale problems. ***FY 2022 Plans:*** - Initiate development of quantum-inspired algorithms on classical hardware for scalable optimization problems. - Perform initial hardware and algorithm co-design analysis for representative mission-scale optimization problems. ***FY 2023 Plans:*** - Initiate development of analog subsystems for quantum-inspired solvers. - Perform initial hardware performance model development. - Demonstrate co-design framework for digital resource estimation.	-	10.000	14.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Develop systematic methodologies for predictive benchmarks. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects the move from initial algorithm and hardware design to subsystem development and design.			
Title: Guaranteed Architectures for Physical Security (GAPS) ***Description:*** The Guaranteed Architectures for Physical Security (GAPS) program is developing hardware security and software architectures with provable security interfaces. These interfaces will physically isolate high-risk transactions during both system design and system build, and will ensure that such protections are enforced at run-time. GAPS will reduce the inherent complexity through the development of hardware and software that is open, extendible, and compatible with size, weight, and power constrained environments to enable security across DoD and commercial systems. The program will substantially lower the barrier to safely enabling high-risk transactions, thus allowing for fast computer-to-computer transactions, physical spatial isolation reducing the need for unreliable software partitioning solutions, and more complex missions without putting sensitive data at risk. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2022 Plans:*** - Implement interconnect architectures and board support packages (BSPs) for a single common embedded bus while increasing the number of protocol layers. - Demonstrate a reduction in transaction overhead on embedded busses when implementing GAPS extensions for multilevel security. - Permit at least one gigabit per second sustained throughput across multiple security level architectures. - Integrate GAPS isolation techniques to a research application associated with an ongoing DoD platform. ***FY 2023 Plans:*** - Implement interconnect architectures and BSPs for a single common embedded bus while increasing to three protocol layers or more. - Demonstrate further reduction in transaction overhead on embedded busses when implementing GAPS extensions for multilevel security. - Permit multiple gigabit per second sustained throughput across multiple security level architectures.	12.000	12.000	12.000
Title: Massive Cross Correlation (MAX) ***Description:*** *Previously part of Beyond Scaling - Architectures The Massive Cross Correlation (MAX) program aims to develop a scalable wideband correlator that can simultaneously achieve the state-of-the-art dynamic range of a digital correlator with the power efficiency enabled by analog electronics. Correlators	-	4.000	12.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
are the core signal processing component used in critical DoD applications such as spread spectrum communications, passive coherent location (PCL) and synthetic aperture radar. Current correlator implementations use FPGAs and general-purpose graphics processing units (GPGPUs) requiring thousands of watts of power and racks of supporting computer equipment for today's low frequency, low bandwidth applications, which creates challenges for their use in power-constrained platforms and in applications that require high frequency, high bandwidth solutions. The MAX program will leverage advances in analog signal processing and state-of-the-art fin field-effect transistor (FinFET) semiconductor processes to overcome these challenges. ***FY 2022 Plans:*** - Perform proof-of-concept design of scalable wideband correlator that combines benefits of digital correlator with efficiency of analog electronics. ***FY 2023 Plans:*** - Implement proof-of-concept designs showing program efficiency goals at program dynamic range requirements meeting initial bandwidth metrics. - Fabricate initial designs of scalable, wideband analog correlators. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program moving from initial concept design to design completion and the start of device fabrication.			
Title: Structured Array Hardware for Automatically Realized Applications (SAHARA)* ***Description:*** *Previously part of Beyond Scaling - Design The Structured Array Hardware for Automatically Realized Applications (SAHARA) program is developing technology for the secure development of custom chips for defense systems. Current DoD systems often employ field-programmable gate array (FPGAs), whose flexibility advantages are offset by lower performance. Structured application specific integrated circuits (ASICs) deliver significantly higher performance and lower power consumption, which makes them an efficient and effective alternative to FPGAs for defense electronic systems. Manually converting FPGAs to structured ASICs, however, is a complex, lengthy, and costly process. SAHARA is developing automated technologies to reduce design time, optimize performance, and minimize the power dissipated by the secure, structured ASIC. ***FY 2022 Plans:*** - Perform initial design of secure, structured ASICs. ***FY 2023 Plans:*** - Finalize design of secure, structured ASICs.	-	3.500	7.500

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Analyze transition impact of secure, structured ASICs for DoD applications. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects the shift from initial to final design of secure, structured ASICs.			
Title: Ferroelectric Computing (FC) ***Description:*** The Ferroelectric Computing (FC) program will develop advanced, complementary metal oxide semiconductor (CMOS)-compatible ferroelectric transistor, compute-in-memory element, and memory compute array technologies for critical data-intensive DoD applications such as radar processing, signal intercept and identification, and image processing. Current compute-in-memory devices are not compatible with advanced CMOS and are too large be scaled to the performance and efficiency levels necessary to support these applications. This program will address this shortfall by developing CMOS-compatible ferroelectric transistor technology for next-generation power-efficient, dense, and scalable compute-in-memory accelerators. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2022 Plans:*** - Perform initial designs of novel ferroelectric transistors that are fast, dense, and energy efficient. - Initiate plans to integrate novel ferroelectric transistors into state-of-the-art silicon technology. ***FY 2023 Plans:*** - Demonstrate an initial compact compute-in-memory element using ferroelectric transistors. - Initiate strategy for connecting memory compute elements into memory compute arrays for computing in memory. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects transition from initial designs to proof-of-concept demonstration.	-	3.000	7.341
Title: Technologies for Rapid Assembly of Microsystems (TRAM) ***Description:*** The Technologies for Rapid Assembly of Microsystems (TRAM) program will develop technology to assemble heterogeneous electronics modules with high performance that can be readily inserted into DoD modules, arrays, and systems. Current low-volume assembly of heterogeneous electronics is time-intensive, expensive, and offers varying levels of performance and state-of-the-art packaging capability that is increasingly dominated by foreign industry and driven by commercial needs and volumes. Low-volume, domestic assembly of high-performance electronics is needed to preserve capability and security of DoD systems. In order to enable new electronics capabilities that can be readily transitioned into prototypes and systems, TRAM will develop technologies for desktop assembly and packaging of different electronics technologies to rapidly move them from design to systems. ***FY 2023 Plans:***	-	-	12.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Analyze candidate technologies for heterogeneous desktop assembly. - Establish candidate circuits and modules with two or more electronics technologies. - Create initial process design rules and design methodologies for the heterogenous desktop assembly capability. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.			
Title: Reconfigurable, Actionable, Passive Technologies for Operational Remote Sensing (RAPTORS) ***Description:*** The Reconfigurable, Actionable, Passive Technologies for Operational Remote Sensing (RAPTORS) program will enable a passive, all-optical kill chain capable of finding both stationary and moving targets with a single sensor. Sensor format can be selected based on platform requirements. RAPTORS will achieve this by combining tileable focal plane arrays (FPAs) that have adaptable spatial resolution with agile filters to adapt the spectral content of the infrared radiation impinging upon the detector. Using a custom read-out integrated circuit (ROIC), the FPA will intelligently balance resolution and number of spectral filters to optimize the information content transmitted off of the chip to enable real-time actionable decisions. This system will enable search and track and improved probability of detection and identification for hard targets, e.g., camouflaged, concealed, and deceptive (CCD) targets, at tactical speeds within the constraints of the cryocooler power limit. If successful, this capability has applications across ground-, air- and space-based platforms. ***FY 2023 Plans:*** - Conduct advanced design review for custom ROIC. - Demonstrate single-pixel filters demonstrating speed and transmission. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.	-	-	9.500
Title: Robust Electronics for Radiative Environments (RE2) ***Description:*** The Robust Electronics for Radiative Environments (RE2) program will develop advanced radiation-hardened (rad-hard) and radiation-tolerant electronics, including processors and memory technologies, to meet the demands of emerging missions. Current rad-hard and rad-tolerant electronics are many generations behind state-of-the-art commercial electronics and cannot meet the needs of future systems. In order to address these needs, RE2 will work to deliver high-performance electronics for space and strategic systems while maintaining the security of these electronics throughout the supply chain. ***FY 2023 Plans:*** - Perform trade study on modifying advanced node complementary metal oxide semiconductor (CMOS) fabrication for rad-hard and rad-tolerant processors and memory.	-	-	9.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Initiate design of candidate rad-hard and rad-tolerant processor and memory architectures. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.			
Title: Next Generation Microelectronics - Advanced Manufacturing Tools ***Description:*** Next Generation Microelectronics - Advanced Manufacturing Tools addresses the development of new manufacturing tools for the design, fabrication, packaging, assembly, testing, and digital emulation of the next generation of advanced microsystems. Specifically, these advanced microsystems include three-dimensional heterogeneous integration (3DHI) and designs targeted for use in extreme environments such as high voltage, high current, high temperature, low temperature, and radiation exposure. New tools to improve manufacturing and testing will be designed, built, and characterized. These tools will enable cost-effective on-shoring of automated processes for packaging, assembly, and testing of advanced microsystems. The software and hardware tools addressed in this program will advance integration techniques beyond current commercial capabilities to support national security needs. Design, verification, and security for 3DHI will be supported by coordinated investments that couple manufacturing and electronic design automation. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Establish tools for design, simulation, testing, and cost-optimization of 3DHI components and packages. - Develop specialized tools for design, simulation, and testing of thermally and radiation hardened components and microsystems. - Initiate developing multi-domain models for virtual prototyping of 3DHI components and packages. - Create methodologies for design optimization for multi-chip, multi-technology packaging and assembly techniques consistent with high density interconnects. - Identify advancements required to automate packaging tools and metrology for volume 3DHI manufacturing. - Increase fidelity and accuracy of techniques for digital twin emulation to decrease prototyping cycle-time that includes system analysis. - Determine an equivalent to a front opening unified pod to facilitate automating die and chiplet handling during the assembly and packaging process. - Demonstrate first version of tools for power and thermal management of high-voltage and high-current microsystems. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.	-	-	90.000
Title: Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI)	-	-	60.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
Description: Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI) addresses the unique manufacturing requirements for 3DHI microsystems, including design, fabrication, packaging, assembly, testing, and digital emulation. These new manufacturing methods will feature increasing circuit-scale interconnect densities for integration, and enhancing the security and interoperability of these complex designs. New multi-chip, multi-technology assembly and packaging will advance beyond silicon-centric integration to include integration of radio frequency (RF), photonics, novel memory, and compound semiconductors. In order to enable this diversity of materials and functions, integration technologies will be enabled by improving thermal management, improving inter-chip power delivery, and improving the modeling and simulation of these new systems on chip. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Initiate developing multi-chip, multi-technology assembly and packaging techniques consistent with high density interconnects (less than or equal to one-micron pitch). - Identify techniques to improve co-planarity for die-to-die, wafer-to-wafer, and die-to-wafer high density interconnects. - Launch development of integration techniques consistent with high-volume automation and inspection. - Expand automated integration techniques to enable low-volume manufacturing. - Implement manufacturing, assembly, and packaging techniques for high-density integration of photonics and electronics. - Increase integration density of silicon digital microelectronic components with compound semiconductor RF microelectronic components through maturation of manufacturing, assembly, and packaging techniques. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.			
Title: Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics ***Description:*** Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics addresses the design, fabrication, packaging, assembly, testing, and digital emulation of the next generation of microsystems targeted for use in extreme environments: high voltage, high current, high temperature, low temperature, and radiation exposure. New manufacturing methods along with new testing and evaluation methods will be created, with an emphasis on developing techniques to enable in-situ measurements of these microsystems while operating in the extreme environments. These new manufacturing methods will also focus on a higher degree of automation in the packaging, assembly, and testing processes. This effort will also develop techniques to significantly improve thermal management, inter-chip power delivery, package integrity, and the modeling and simulation of these unique microsystems. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:***	-	-	30.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
- Initiate developing multi-chip, multi-technology assembly and packaging techniques for thermally-hardened and radiation-hardened microsystems. - Define device design and thermal management techniques for very high operating temperatures. - Initiate developing techniques for power management and thermal management of high-voltage and high-current microsystems. - Create extremely low-loss passive materials for efficient power distribution in high-voltage and high-current microsystems. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.			
Title: Next Generation Microelectronics Prototyping Designs ***Description:*** Next Generation Microelectronics Prototyping Designs supports the development of novel three-dimensional heterogeneous integration (3DHI) capable of being prototyped using the National Network for Next-generation Microelectronics Manufacture (N3M2). The N3M2 will include public-private partnerships that provide the ability to manufacture prototypes of next-generation 3DHI microsystems, including fabrication, packaging, assembly, and testing. The design challenges provide the opportunity to explore approaches that will improve and accelerate the adoption of 3DHI standardized chip-to-chip interfaces and package optimization. Leading-edge chip designs will be fabricated, and subsequently integrated into 3DHI designs in multi-project demonstration runs. Research related to this effort is funded within PE 0603739E, Project MT-16. ***FY 2023 Plans:*** - Identify and initiate challenge problems for 3DHI microsystems and establish appropriate metrics. - Determine goals for design challenges for standardized chip-to-chip integration practices. - Establish a fabrication run for leading edge chips to develop components for novel 3DHI prototype designs. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 increase reflects program initiation.	-	-	25.000
Title: Beyond Scaling - Materials ***Description:*** The Beyond Scaling - Materials program is demonstrating the integration of novel materials into next-generation logic and memory components. This program is pursuing potential enhancements in electronics that do not rely on Moore's Law, i.e. silicon transistor scaling, including research into new materials and the implications of those materials at the device, algorithm, and packaging levels. Research areas include heterogeneous integration of multiple materials, "sticky logic" and novel transistor devices that combine elements of computation and memory, and three-dimensional vertical circuit integration to demonstrate dramatic performance improvements using older silicon technologies. Further research supports innovation in the technology cycle by working with entrepreneurs focused on DoD-relevant businesses. Basic research for this program is funded within PE 0601101E, Project ES-02.	26.451	16.000	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
FY 2022 Plans: - Analyze the manufacturability of a large-scale fully integrated 3D monolithic system-on-chip, and share analysis with DoD and commercial end users. - Demonstrate broadband, low noise mixed-mode integrated circuits with enhanced transistors in a commercial foundry. - Integrate advanced transistor processing technology and models in a commercial foundry. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects program completion.			
Title: Beyond Scaling - Architectures ***Description:*** The Beyond Scaling - Architectures program is demonstrating a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program is exploring technologies and techniques such as new domain-specific circuit architectures, co-design of electronics hardware and software, intelligent edge sensors, hardware security architectures, and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Further research will enable significant improvements in programming productivity for massively parallel heterogeneous processing systems (e.g., data centers). Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2022 Plans:*** - Prototype reconfigurable software-defined hardware and associated software. - Demonstrate a system-on-chip executing five simultaneous applications utilizing multiple heterogeneous processing elements. - Demonstrate a prototype test bench that can detect anomalous system behavior due to hardware Trojans in complex systems. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects program completion.	31.707	18.000	-
Title: Beyond Scaling - Design ***Description:*** The Beyond Scaling - Design program is developing and demonstrating the tools required for rapidly designing and deploying specialized circuits. Research efforts are exploring technologies and techniques for rapid, specialized design such as intelligent design tools, automated physical layout generation, and open-source circuit design. The goal of this program is to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a pathway for the rapid upgrade of electronics. Advances under this program demonstrate a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon transistor scaling. Basic research for this program is funded within PE 0601101E, Project ES-02.	25.000	11.993	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
FY 2022 Plans: - Optimize algorithms and the physical design platform to demonstrate path to improvement of power, performance, and area for performance beyond existing state-of-the-art techniques. - Further develop open source tools to enhance interoperability and integration between tools and begin integration into a unified chip development infrastructure. - Fabricate and test initial system-on-chip design using open source Intellectual Property (IP) building blocks verified for correctness with open source simulation technologies. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects program completion.			
Title: System Security Integrated Through Hardware and firmware (SSITH) ***Description:*** The System Security Integrated Through Hardware and firmware (SSITH) program seeks to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. Current responses to cybersecurity attacks typically consist of developing and deploying software patches to address specific vulnerabilities in a software firewall without addressing potential vulnerabilities in the underlying hardware architecture. To address this challenge, SSITH is driving new research in electronics hardware security and exploiting current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas has been enabled by the extremely capable semiconductor technology driven by Moore's Law. The program also is investigating flexible hardware architectures that adapt to and limit the impact of new cybersecurity attacks. Finally, SSITH is mitigating the potential negative impact of new security protection architectures on system performance and power usage. Once developed, SSITH capabilities will be applicable to both commercial and military electronic systems. ***FY 2022 Plans:*** - Deliver a high-performance, secure SSITH application-specific integrated circuit (ASIC) for transition and demonstration purposes. ***FY 2022 to FY 2023 Increase/Decrease Statement:*** The FY 2023 decrease reflects program completion.	9.000	4.000	-
Title: Hierarchical Identify Verify Exploit (HIVE) ***Description:*** The Hierarchical Identify Verify Exploit (HIVE) program pursued new hardware architectures and algorithms for improving the efficiency of graph and sparse data analytics. When developing operationally significant intelligence, human analysts today are forced to reduce the scope of the problems that they can address and the tempo of their analyses due to the limitations of currently deployed hardware. Because of these limitations, the amount of information gathered is quickly outstripping	10.000	-	-

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2021	FY 2022	FY 2023
the human ability to review, process, fuse, and interpret data. To resolve this challenge, HIVE leveraged improvements in computational efficiency to augment the analyst's ability to integrate large streams of data. The program investigated advances in chip architecture and data analytics algorithms that can allow machines to infer meaning out of data based on the information needs of the warfighter. This program enabled the warfighter to understand far more of the battlespace in real time.			
Title: Common Heterogeneous integration and IP reuse Strategies (CHIPS) ***Description:*** The Common Heterogeneous integration and IP reuse Strategies (CHIPS) program developed the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program designed chiplets which can be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers.	7.000	-	-
Accomplishments/Planned Programs Subtotals	194.158	196.493	421.001

	FY 2021	FY 2022
Congressional Add: ERI 2.0 - Congressional Add ***FY 2022 Plans:*** - Identify tools for software/hardware logic co-design to identify three-dimensional heterogeneous integration (3DHI) security vulnerabilities. - Evaluate status of additive manufacturing for 3DHI. - Characterize current state of automation in packaging tools, metrology, and test for 3DHI to identify capabilities required for fully automated 3DHI manufacturing. - Analyze techniques for digital twin emulation of microsystems and associated methods for validation of complete digital models. - Initiate developing multi-domain models for virtual prototyping of three-dimensional heterogeneous integration (3DHI) components and packages. - Initiate developing co-design techniques for optimizing a thermal floorplan and performance in microsystems. - Investigate new dielectric and magnetic materials integrated into high power and high temperature microsystems. - Identify methodologies to develop multi-physics, multi-scale design tools that incorporate on-chip generated electromagnetic interference effects in high-voltage and high-current microsystems.	-	36.000
Congressional Adds Subtotals	-	36.000

Exhibit R-2A, RDT&E Project Justification: PB 2023 Defense Advanced Research Projects Agency		Date: April 2022
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A