Exhibit R-2, RDT&E Budget Item Justification: PB 2024 Defense Advanced Research Projects Agency	Date: March 2023
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

COST ($ in Millions)	Prior Years	FY 2022	FY 2023	FY 2024 Base	FY 2024 OCO	FY 2024 Total	FY 2025	FY 2026	FY 2027	FY 2028	Cost To Complete	Total Cost
Total Program Element	-	378.625	554.155	572.662	-	572.662	595.500	598.021	571.552	585.627	-	-
ELT-01: *ELECTRONIC TECHNOLOGY*	-	133.776	133.154	120.837	-	120.837	145.956	149.372	146.381	146.356	-	-
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	244.849	421.001	451.825	-	451.825	449.544	448.649	425.171	439.271	-	-

A. Mission Description and Budget Item Justification

The efforts described in this Program Element (PE) address the Applied Research associated with the Electronics Technology Program that is directed towards developing electronics that make a wide range of military applications possible. The PE focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter. This PE also supports innovation and robust transition planning in the technology cycle by working with entrepreneurs to increase the likelihood that DARPA funded technologies take root in the U.S. and provide new capabilities for national defense.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project pursues electronics performance advancements that exploit new concepts in circuit specialization and three-dimensional heterogeneous integration (3DHI) by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our microelectronics infrastructure relies, this envisioned specialization will require incorporation of security safeguards and advancing manufacturing tools and process automation. Accordingly, programs within the Beyond Scaling project will reduce barriers to making specialized circuits in today's silicon hardware and 3DHI by improving producibility. This will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized microelectronics, particularly for operation in extreme environments. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting 3DHI to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

Exhibit R-2, RDT&E Budget Item Justification: PB 2024 Defense Advanced Research Projects Agency	Date: March 2023
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

B. Program Change Summary ($ in Millions)	FY 2022	FY 2023	FY 2024 Base	FY 2024 OCO	FY 2024 Total
Previous President's Budget	393.384	557.745	571.062	-	571.062
Current President's Budget	378.625	554.155	572.662	-	572.662
Total Adjustments	-14.759	-3.590	1.600	-	1.600
• Congressional General Reductions	0.000	-3.590			
• Congressional Directed Reductions	0.000	0.000			
• Congressional Rescissions	0.000	0.000			
• Congressional Adds	0.000	0.000			
• Congressional Directed Transfers	0.000	0.000			
• Reprogrammings	-3.025	0.000			
• SBIR/STTR Transfer	-11.734	0.000			
• TotalOtherAdjustments	-	-	1.600	-	1.600

Congressional Add Details ($ in Millions, and Includes General Reductions)	FY 2022	FY 2023
Project: ELT-02: *BEYOND SCALING TECHNOLOGY*		
Congressional Add: *ERI 2.0 - Congressional Add*	36.000	-
Congressional Add Subtotals for Project: ELT-02	36.000	-
Congressional Add Totals for all Projects	36.000	-

Change Summary Explanation

FY 2022: Decrease reflects SBIR/STTR transfer and reprogrammings.
FY 2023: Decrease reflects FFRDC reduction.
FY 2024: Increase reflects minor program repricing.

Exhibit R-2A, RDT&E Project Justification: PB 2024 Defense Advanced Research Projects Agency			Date: March 2023
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / *ELECTRONICS TECHNOLOGY*	Project (Number/Name) ELT-01 / *ELECTRONIC TECHNOLOGY*	

COST ($ in Millions)	Prior Years	FY 2022	FY 2023	FY 2024 Base	FY 2024 OCO	FY 2024 Total	FY 2025	FY 2026	FY 2027	FY 2028	Cost To Complete	Total Cost
ELT-01: *ELECTRONIC TECHNOLOGY*	-	133.776	133.154	120.837	-	120.837	145.956	149.372	146.381	146.356	-	-

A. Mission Description and Budget Item Justification

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
Title: Focal Arrays for Curved Infrared Imagers (FOCII)	16.000	12.139	8.000
Description: The Focal Arrays for Curved Infrared Imagers (FOCII) program is developing curved focal plane arrays for broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. FOCII will leverage curving strategies for state-of-the-art focal plane arrays combined with advances in designing and manufacturing stress relief features to demonstrate hardware that simultaneously provides maximum resolution and illumination. This program will develop novel designs for IR imagers that enable minimal size, weight and cost for size-constrained applications. This will enable new applications in passive seeker technology for missiles, overhead persistent infrared imaging, 360-degree situational awareness, infrared search and track, and long-range targeting. ***FY 2023 Plans:*** - Demonstrate large area focal array curved to final program specified objective radius. - Complete preliminary camera design with curved structured focal array. - Measure curved focal array performance on laboratory-scale test equipment. ***FY 2024 Plans:*** - Measure radiometric performance of large area focal array curved to final program specified objective radius. - Demonstrate thermal cycling of large area focal array curved to final program specified objective radius. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the shift from design and fabrication to demonstration and testing.			
Title: Wideband Adaptive RF Protection (WARP)	18.000	17.000	13.840

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Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
Description: The Wideband Adaptive RF Protection (WARP) program is developing radio frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference through tunable filtering, limiting, and/or signal cancellation. The ability to create tunable and reconfigurable band pass and band stop filters in the range of 2 gigahertz (GHz) to 18 GHz will be important for implementing transmit/receive modules in next-generation multi-function arrays. Another important area of interference mitigation is self-interference. WARP is developing the signal cancellation technology that will listen to the transmitted interfering signal and subtract it from the input of the receiver so faint signals near the noise floor can still be detected. Program research will provide feedback mechanisms that intelligently correct these problems. Whether for self-induced interference or external interference jamming, WARP is developing intelligent filtering and self-interference cancellation technologies to protect wideband DoD receivers. ***FY 2023 Plans:*** - Demonstrate wideband adaptive filters that implement embedded interference sensing and closed-loop adaptive tuning. - Demonstrate analog signal cancellers that implement embedded leakage channel sensing and closed-loop adaptive tuning. - Prepare demonstration of the RF protection technology that is well-aligned to transition partners within the government. ***FY 2024 Plans:*** - Scale adaptive wideband adaptive filter designs to provide full-band coverage. - Scale adaptive analog signal canceller designs to full-band coverage of low-band and high-band. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the transition from initial component demonstration to component scaling.			
Title: Quantum Imaging of Vector Electromagnetic Radiation (QuIVER)	17.000	16.000	9.000
Description: The Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) program is developing full-tensor magnetic field sensors and will demonstrate them in DoD-relevant applications and concept of operations. In addition to being diagnostically relevant, such sensitive magnetometers could enable future human-machine/brain-machine interfaces. The DoD and industry also use magnetometers for magnetic anomaly detection, which may allow for the discovery of mineral/oil deposits, discovery of old wellheads, or the detection of improvised explosive devices. In addition, magnetometers offer the possibility of magnetic navigation, which may operate in GPS-denied environments. Recent advancements have resulted in the potential to develop highly-sensitive vector magnetometers, which would enable the consequent development of sensitive full-tensor gradient sensors. Such tensors offer more degrees of freedom than their scalar or vector counterparts and potentially provide additional information about the source of the magnetic field. ***FY 2023 Plans:*** - Validate sensitivity and functionality of tensor magnetometer.			

Exhibit R-2A, RDT&E Project Justification: PB 2024 Defense Advanced Research Projects Agency		Date: March 2023
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Complete construction of tensor magnetometer system for field testing. - Perform field test of tensor magnetometer system. ***FY 2024 Plans:*** - Design reduced size, weight, and power (SWaP) tensor magnetometer with sensor fusion and automation. - Complete construction of reduced-SWaP tensor magnetometer system for field testing and validate sensitivity and functionality. - Perform field test of reduced-SWaP tensor magnetometer system. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the completion of system construction and transition to testing.			
Title: Fast Event-based Neuromorphic Camera and Electronics (FENCE)	22.000	19.410	16.997
Description: The Fast Event-based Neuromorphic Camera and Electronics (FENCE) program will develop and demonstrate a low latency, low power event-based infrared (IR) camera to enable intelligent sensors for tactical DoD applications. Event-based imagers are an emerging class of sensors with major demonstrated advantages relative to traditional cameras. State-of-the-art visible event-based cameras have been shown to produce over two orders of magnitude less data in optimal conditions relative to traditional framing cameras because they transmit data only from pixels that have changed. This leads directly to two orders of magnitude lower data latency and a commensurate reduction in power consumption. Despite their inherent advantages, existing event-based cameras are not compatible with DoD applications because DoD applications regularly face conditions that are not optimal, where issues such as clutter and noise cause a large percentage of the event-based pixels to change simultaneously. When this happens, today's event-based cameras do not perform significantly better than traditional cameras. FENCE will develop an infrared event-based imager consistent with military requirements. FENCE will develop a four-megapixel asynchronous read-out integrated circuit (ROIC), co-designed with a 3D integrated processor that will intelligently remove noise and clutter to maintain low power and latency operation even when faced with all of the pixels firing simultaneously. If successful, this new class of sensors enabled by FENCE will be capable of responding to fast moving targets and discriminating dim targets in noisy conditions. ***FY 2023 Plans:*** - Measure ROIC power and timing fidelity. - Conduct critical design review of processor layer. - Fabricate processor layer in advanced node silicon. - Measure processing layer power consumption. ***FY 2024 Plans:*** - Integrate components into full focal plane array (FPA). - Measure integrated processor layer power consumption.			

Exhibit R-2A, RDT&E Project Justification: PB 2024 Defense Advanced Research Projects Agency		Date: March 2023
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Perform initial FPA functionality testing. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects moving from design and fabrication to integration and testing.			
Title: Waveform Agile Radio-frequency Directed Energy (WARDEN) ***Description:*** The Waveform Agile Radio-frequency Directed Energy (WARDEN) program aims to extend the range and lethality of high-power microwave (HPM) systems by introducing flexible waveform techniques that use combinations of frequency, amplitude, and pulse-width modulations to significantly improve electromagnetic coupling into complex target enclosures and increase the probability of disruption or damage to internal electronic components and circuits. Applications for HPM systems include counter-unmanned aerial systems (C-UAS), vehicle and vessel disruption, electronic strike, and guided missile defense. Current HPM systems use oscillators to produce electromagnetic radiation. These systems are inherently narrowband and lack the frequency agility to support waveforms to maximize electromagnetic coupling and to optimally exploit electronic system vulnerabilities. Lacking the capability to use optimized waveforms, HPM oscillators have been pushed close to the physical limits of peak power generation. To develop a more efficient, lower power, waveform agile approach, the WARDEN program will develop and demonstrate the first broadband HPM amplifier; create new theory and simulation tools to predict electromagnetic coupling into complex enclosures and the effects on electronics; and develop novel agile waveform techniques capable of reducing the susceptibility threshold of targeted electronics systems to HPM attack. ***FY 2023 Plans:*** - Finalize broadband amplifier designs and initiate fabrication, procurement, and laboratory preparation. - Develop initial hybrid electromagnetic coupling tools that combine deterministic, reduced-model, and statistical approaches. - Develop predictive models and agile waveform techniques to produce disruptive effects on integrated electronics. - Validate initial hybrid electromagnetic coupling tools, predictive models, and agile waveform techniques through comparison with experimental measurements. - Develop high current electron gun and high power, broadband amplifier designs and verify them through 3D simulation. ***FY 2024 Plans:*** - Experimentally demonstrate broadband amplifier power, bandwidth, and pulse duration performance at low repetition rates. - Integrate electromagnetic coupling tools that combine deterministic, reduced-model, and statistical approaches into a hybrid framework. - Validate electromagnetic coupling tools and predictive models through comparison with experimental measurements. - Demonstrate disruptive agile waveform techniques on integrated electronics.	19.000	20.000	20.000
Title: Generating RF with Photonics for low Noise (GRYPHON)	19.776	17.000	14.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
Description: The Generating RF with Photonics for low Noise (GRYPHON) program will develop compact sources of microwaves and millimeter waves with extremely low phase noise. Compact signal sources used today, such as crystal oscillators, are too noisy to support advanced military radar and communications functions. Conversely, best-in-class oscillators which use optical techniques to synthesize extremely pure microwaves are too large and expensive to deploy on the airborne systems, munitions, and other size-constrained platforms where the DoD requires high-performance capabilities. The GRYPHON program will draw on recent advances in miniature optical components to replicate best-in-class optical frequency synthesis techniques in microchip form factors. ***FY 2023 Plans:*** - Perform initial demonstration of chip-scale component functionality. - Perform benchtop-level integration of components. - Setup characterization equipment and frequency references for phase noise measurements. ***FY 2024 Plans:*** - Demonstrate microwave generation at a fixed frequency. - Demonstrate microwave generation with frequency tunability. - Characterize environmental robustness of microwave oscillators. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects shifting from final design and fabrication into testing.			
Title: Quantum Apertures (QA) ***Description:*** The Quantum Apertures (QA) program will develop novel radio receiver and aperture systems using quantum sensors as the receiving elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly-excited "Rydberg" states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. The receiver system's enhanced capabilities will be leveraged in this program to develop novel waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum receiving elements, lasers to program the sensor and read out radio signals, and processing electronics. Beginning in FY 2024, this program is funded in PE 0602716E, Project ELT-02. ***FY 2023 Plans:*** - Improve quantum aperture sensor sensitivity and frequency tunability.	16.000	16.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2024 Defense Advanced Research Projects Agency		Date: March 2023
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Advance government-owned model of quantum aperture receiver for realistic complex signal inputs. - Develop system to utilize single quantum aperture sensor in a DoD-relevant application. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the program moving to PE 0602716E, Project ELT-02.			
Title: Compact High Intensity Radiating Photonics (CHIRP) ***Description:*** The Compact High Intensity Radiating Photonics (CHIRP) program will develop compact, ultra-fast, high-power lasers. Ultra-short-pulse lasers are crucial tools for high-precision sensing and timing, novel manufacturing, and directed energy effects, but the size of these lasers limits their ability to be used on or against highly mobile platforms. CHIRP will decrease the size, weight and power (SWaP) of ultra-fast laser sources by employing emerging integrated photonics and amplification techniques. ***FY 2023 Plans:*** - Analyze designs for high peak-power laser systems with reduced SWaP. - Initiate design of high-efficiency ultra-fast laser components. - Begin development of materials for high performance at high optical intensities. ***FY 2024 Plans:*** - Perform analysis of size, weight, power reduction and expected performance of quantum cascade lasers. - Complete design of fully-integrated sub-picosecond lasers. - Initiate process development for broadband gain integrated photonic platforms. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the program shifting from initial design to development for broadband gain integrated photonic platforms.	-	6.000	13.000
Title: Humboldt ***Description:*** The Humboldt program, building on technology developed in the Waveform Agile Radio-frequency Directed Energy (WARDEN) program also budgeted in this PE/Project, seeks to develop directed energy (DE) devices to produce disruptive effects in electronic systems. The devices have potential for dual-use as sources to characterize the susceptibility of commercial electronics to electromagnetic interference (EMI). ***FY 2023 Plans:*** - Characterize the baseline performance of critical materials.	-	9.605	17.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Develop initial designs of prototype proof-of-concept devices. ***FY 2024 Plans:*** - Experimentally characterize the operation of the proof-of-concept devices. - Demonstrate the effectiveness of the proof-of-concept devices on electronic systems. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the program shifting from initial design to demonstration of the proof-of-concept devices on electronic systems.			
Title: Robust Protection for Electronic Systems (ROPES) ***Description:*** The Robust Protection for Electronic Systems (ROPES) program will develop and mature ultra-wide bandgap (UWBG) materials and devices to achieve robust, high-power operation and fast switching speed required to protect sensitive RF electronics in harsh environments. ROPES will address the key technical challenges that limit the performance of conventional diodes and switches. These challenges include: 1) demonstrating materials and device architectures capable of simultaneous high current operation and low leakage current under high electric field and 2) simultaneously achieving low device resistance and capacitance resulting in fast switching speed. To be successful, ROPES will leverage advances in UWBG materials and innovative device architectures to enable high power, high speed, and low loss switches. ROPES will support multiple DoD platforms and arrays by enabling high-power (kilowatt class), low-loss front end receiver protect circuitry, as well as high voltage (10 kilovolt class), low-loss switches required for future electric ship power systems. Basic research for this program is funded in PE 0601101E, Project ES-01. ***FY 2024 Plans:*** - Develop and optimize fabrication processes of UWBG materials by designing, fabricating, and characterizing test structures that incorporate novel device architectures. - Design, fabricate, and characterize RF switches that include UWBG materials and novel device architectures, demonstrating high power handling switches through kilobits per second band frequencies with fast switching speed and low leakage currents. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects program initiation.	-	-	5.000
Title: Vacuum Electronic Amplifiers for Millimeter-wave Power and Spectrum Superiority (VAMPS) ***Description:*** The Vacuum Electronic Amplifiers for Millimeter-wave Power and Spectrum Superiority (VAMPS) program seeks to develop compact, high power radio-frequency (RF) signal amplifiers to enable electronic warfare systems to provide DoD platforms with protection from current and evolving millimeter-wave missile seeker threats. The explosive growth of commercial applications in the millimeter-wave spectrum has led to the wide availability of inexpensive RF sources and components,	-	-	4.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
expanding the threat space to increasingly higher frequencies. The VAMPS program will develop and demonstrate millimeter-wave vacuum electronic amplifiers integrated with solid-state pre-drivers to achieve breakthrough power and bandwidth to enable DoD electronic attack systems to operate in the high-frequency millimeter-wave portion of the electromagnetic spectrum with increased range and effectiveness. ***FY 2024 Plans:*** - Develop integrated solid-state pre-amplifier/high power vacuum electronic amplifier design. - Develop and verify solid-state pre-amplifier design and layout. - Develop high power vacuum electronic amplifier design and verify performance and stability through 3D simulation. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects program initiation.			
Title: Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) ***Description:*** The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program developed a novel magnetic sensor capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. The AMBIIENT program exploited novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself detected the gradient of a local magnetic field while subtracting the much larger ambient signal. This capability enabled low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors enabled diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and ultra-low frequency communications.	6.000	-	-
Accomplishments/Planned Programs Subtotals	133.776	133.154	120.837

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

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COST ($ in Millions)	Prior Years	FY 2022	FY 2023	FY 2024 Base	FY 2024 OCO	FY 2024 Total	FY 2025	FY 2026	FY 2027	FY 2028	Cost To Complete	Total Cost
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	244.849	421.001	451.825	-	451.825	449.544	448.649	425.171	439.271	-	-

A. Mission Description and Budget Item Justification

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. This project pursues electronics performance advancements that exploit new concepts in circuit specialization and three-dimensional heterogeneous integration (3DHI) by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our microelectronics infrastructure relies, this envisioned specialization will require incorporation of security safeguards and advancing manufacturing tools and process automation. Accordingly, programs within the Beyond Scaling Technology project will reduce barriers to making specialized circuits in today's silicon hardware and 3DHI by improving producibility. This will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized microelectronics, particularly for operation in extreme environments. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting 3DHI to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
Title: Digital RF Battlespace Emulator (DRBE)	20.356	20.000	7.285

Description: The Digital RF Battlespace Emulator (DRBE) program is developing a large-scale, interactive, emulated radio frequency (RF) environment, providing the DoD with the capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. DRBE is leveraging advances in massively multi-core computing hardware and high-bandwidth digital cross-connects to emulate realistic RF environments accounting for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. An electronics architecture supporting the power and latency requirements demanded by these emulation environments does not currently exist. DRBE is pursuing three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment will allow plug-and-play connections for hundreds of RF systems in a battlespace test. Multi-system exercises will then be quickly executed through many different combat scenarios and variations. DRBE is serving to develop concept of operations (CONOPS), inform battle plans, and fine-tune the performance of both individual and large groups of RF systems.

FY 2023 Plans:
- Complete DRBE real-time High Performance Computer (HPC) design to the level of Critical Design Review.
- Validate DRBE system design following the Critical Design Review.
- Demonstrate real-time RF emulation on computational accelerator chip.

FY 2024 Plans:

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Integrate HPC with RF interfaces. - Deliver DRBE components to DoD laboratory for integration. - Validate real-time HPC performance with a representative DRBE workload. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the program moving from design to integration and testing.			
Title: Low Temperature Logic Technology (LTLT) ***Description:*** The Low Temperature Logic Technology (LTLT) program will exploit the unique device and material performance characteristics of state-of-the-art silicon transistors at cryogenic temperatures. Current silicon transistors are performance and power limited when operating at room temperature or higher. This program removes these limitations through modifying the design of existing silicon transistors to optimize their performance at cryogenic temperatures. These devices will be compatible with current complementary metal-oxide-semiconductor (CMOS) fabrication process flows and will offer significant increases in performance and power efficiency over room temperature devices. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Complete design of transistor, memory, and interconnect technologies that are optimized for low temperature operation. - Develop high speed, low power switching devices and experimentally demonstrate their performance at low temperature. - Demonstrate a low power and high-performance memory unit at low temperature. - Continue improving low-temperature device characteristics to enhance performance. ***FY 2024 Plans:*** - Demonstrate the performance/power improvement of the LTLT devices. - Demonstrate the performance/power improvement of a central processing unit with large on-chip static random access memory. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects transition from design to component fabrication and testing.	15.000	22.000	21.000
Title: Automatic Implementation of Secure Silicon (AISS) ***Description:*** The Automatic Implementation of Secure Silicon (AISS) program is enabling a design tool and Intellectual Property (IP) ecosystem where security is pervasive and can be incorporated naturally into chip design with minimal effort and expense. The program will enable rapid evaluation of architectural alternatives in platform integration where security can be optimized relative to the conventional design economic measure of power, area, and speed. The program will advance multi-level provenance and integrity validation techniques for design through improvement of current methods or invention of novel technical approaches, and will demonstrate new capabilities in the context of reduced instruction set computing (RISC) architectures	18.000	21.700	6.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
or computer processors. AISS will protect advanced chips from known attack strategies by incorporating security into a highly automated system aimed at reducing design time while maximizing exploration of architectural alternatives. As a result, DoD applications will benefit from more secure chips becoming pervasive whether procured commercially or designed specifically for defense systems. ***FY 2023 Plans:*** - Develop additional static components including balanced and noisy cryptography cores, boot and activity odometers. - Add features to support bus monitoring. - Develop an enhanced library of heuristics. - Demonstrate generation of two selected proof-of-concept (PoC) designs can be built semi-automatically using AISS IP. ***FY 2024 Plans:*** - Develop design automation and optimization recommendations as a means to override/interact with defaults. - Simplify automation flow in consideration of third-party security techniques and cryptographic IP. - Develop two forms of documentation; one that will serve as a User guide, and one for the purposes of interfacing to AISS. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects a shift from prototype development to final testing.			
Title: Lasers for Universal Microscale Optical Systems (LUMOS)	23.000	18.000	8.000
Description: The Lasers for Universal Microscale Optical Systems (LUMOS) program is integrating high-performance light sources into silicon integrated photonics enabling compact, rugged, high-performance systems for positioning, navigation, communications, 3D imaging, and quantum technologies. Silicon photonics today enables microscale integration of complex optical systems, but the platform's lack of optical gain precludes the creation of lasers and amplifiers through foundry processes. LUMOS will deliver the missing capability to provide compact optical sources at wavelengths from the visible to the infrared, and will create a universal manufacturing platform that builds upon the current photonics ecosystem. To drive innovation and maintain DoD access to leading-edge deployable photonic solutions, LUMOS will establish a technology pathway connecting government, academic, commercial, and defense users of integrated photonics, and will provide multi-project wafer runs through an open-access foundry. ***FY 2023 Plans:*** - Optimize high-performance lasers and optical amplifiers while providing designers access through first active foundry runs. - Begin layout and characterization of advanced lasers and testing of essential demonstration components. - Scale optical power and component bandwidth for integrated microwave-compatible platform.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Demonstrate narrow linewidth lasers at design wavelengths on integrated visible platform. ***FY 2024 Plans:*** - Incorporate device improvements and higher-complexity external designs in a second laser-enabled foundry run. - Construct system demonstrators utilizing high-power and visible-wavelength integrated platforms. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects transition from fabrication and initial demonstration to optimization and component characterization.			
Title: COmpact Front-end Filters at the ElEment-level (COFFEE) ***Description:*** The COmpact Front-end Filters at the ElEment-level (COFFEE) program will develop and demonstrate compact, high frequency radio frequency (RF) filter technology without compromising performance, specifically low insertion loss and high power handling. The new filtering technology will enable interference rejection capability, efficient spectral management, and coexistence with commercial 5G applications. It is projected that COFFEE filter technology will enhance the resilience of military microwave and mm-wave radar and communication systems for DoD spectral dominance into the future. For commercial applications, COFFEE will result in more efficient use of mm-wave frequency allocations for 5G networks. ***FY 2023 Plans:*** - Verify and validate performance of new high frequency resonators in the laboratory. - Demonstrate new high frequency resonators and evaluate performance against program technical metrics. - Integrate new high frequency resonators into new high-performance filters. ***FY 2024 Plans:*** - Integrate the resonators into low insertion loss filters demonstrated at microwave frequencies. - Construct filters with high power handling and, as required, integrable tuning. - Demonstrate repeatable manufacturability with low device-to-device variability. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the shift from design to component demonstration and integration.	15.000	17.000	14.000
Title: ELectronics for G-band ARrays (ELGAR) ***Description:*** The ELectronics for G-band ARrays (ELGAR) program will develop the integration technologies needed to create compact, high-performance G-band (220 GHz) array front-end electronics to enable phased array antenna systems for DoD communications and sensing. ELGAR will address the key technical challenges that prevent III-V electronics from realizing high-performance G-band arrays, namely achieving efficient, compact G-band III-V monolithic microwave/millimeter wave integrated circuit power amplifiers (MMIC PAs) with high output power density, and achieving low loss off-chip interconnects between	10.000	18.000	19.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
adjacent G-band array components. In particular, ELGAR will develop III-V compatible, silicon-like fabrication and integration approaches to enable compact, high power density, high efficiency G-band MMICs and arrays. The technologies developed will support applications including high data rate communications in size, weight, and power-constrained platforms. ***FY 2023 Plans:*** - Continue to compact the size and reduce the power loss of the III-V semiconductor compatible silicon-like multilayer interconnects, integration processes, and test structures. - Design, fabricate, and characterize compact G-band III-V MMIC PAs that use the silicon-like multilayer interconnects. - Design, fabricate, and characterize low loss, array-level interconnects for integration of G-band PAs with other array components. ***FY 2024 Plans:*** - Further improve the efficiency and output power of compact G-band III-V MMIC PAs that use the silicon-like multilayer interconnects. - Further reduce the power loss of array-level interconnects for integration of G-band PAs with other array components. - Design, fabricate and characterize circularly-polarized, medium-power transmit array test articles. - Design, fabricate, and characterize circularly-polarized, low-noise receive array test articles. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from initial design to fabrication and characterization of components.			
Title: Data Privacy for Virtual Environments (DPRIVE)	18.000	15.960	10.000
Description: The Data Privacy in Virtual Environments (DPRIVE) program will enable homomorphic encryption for data privacy at the user and application level through the development of new hardware accelerators to achieve acceptable computational times. The program plans to provide strong privacy protections at the tactical edge with no more than one order of magnitude penalty in computation time, and to enable very strong privacy at the enterprise level with no more than three orders of magnitude penalty over unencrypted processing. DPRIVE will build hardware to accelerate the computation of homomorphic encryption, which enables mathematical operations to execute on encrypted data such that the data is never unencrypted. The program will enable the development and deployment of these hardware accelerators to edge computing devices where power and time are a premium, as well as to enterprise computing facilities where the amount and sensitivity of the data requires increased protection. ***FY 2023 Plans:*** - Refine DPRIVE accelerator design in advanced node complementary metal oxide semiconductor (CMOS). - Execute and demonstrate mission workloads with full design simulations.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Tape-out for DPRIVE accelerator design in advanced node CMOS. ***FY 2024 Plans:*** - Fabricate mother board to accommodate the homomorphic encryption coprocessor and appropriate interfaces to a central processing unit (CPU). - Package and test the DPRIVE coprocessor microcircuit for basic operations. - Execute pre-determined workloads and benchmarks to establish performance, speed, and accuracy of the coprocessor's homomorphic encryption capabilities. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the shift from design to integration and testing.			
Title: Quantum Inspired Classical Computing (QuICC) ***Description:*** The Quantum Inspired Classical Computing (QuICC) program will implement quantum-inspired algorithms using classical dynamic systems in novel computing architectures for the efficient solving of complex optimization problems. Currently, too much computational energy is required to solve mission-scale optimization problems leading to sub-optimal solutions and excessive computation times. This program will create frameworks for analyzing the computational advantage provided by quantum-inspired algorithms and perform the hardware and algorithm co-design needed to reduce the required energy to optimally solve mission-scale problems. ***FY 2023 Plans:*** - Develop quantum-inspired algorithms on classical hardware for scalable optimization problems. - Perform initial hardware and algorithm co-design analysis for representative mission-scale optimization problems. ***FY 2024 Plans:*** - Initiate development of analog subsystems for quantum-inspired solvers. - Perform initial hardware performance model development. - Demonstrate co-design framework for digital resource estimation. - Develop systematic methodologies for predictive benchmarks. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects the shift from algorithm and hardware design to subsystem development and design.	13.000	17.000	15.000
Title: Massive Cross Correlation (MAX) ***Description:*** The Massive Cross Correlation (MAX) program aims to develop a scalable wideband correlator that can simultaneously achieve the state-of-the-art dynamic range of a digital correlator with the power efficiency enabled by analog electronics. Correlators are the core signal processing component used in critical DoD applications such as spread spectrum	6.000	12.000	19.000

B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
communications, passive coherent location, and synthetic aperture radar. Current correlator implementations use field-programmable gate array and general-purpose graphics processing units requiring thousands of watts of power and racks of supporting computer equipment for today's low frequency, low bandwidth applications, which creates challenges for their use in power-constrained platforms and in applications that require high frequency, high bandwidth solutions. The MAX program will leverage advances in analog signal processing and state-of-the-art fin field-effect transistor (FinFET) semiconductor processes to overcome these challenges. ***FY 2023 Plans:*** - Critical design review of analog correlators meeting high efficiency in simulation. - Fabricate initial designs of scalable, wideband analog correlators achieving high efficiency in a laboratory test environment. ***FY 2024 Plans:*** - Independent verification and validation of correlators meeting program metrics with government-furnished waveforms. - Implement proof-of-concept designs showing program efficiency goals at program dynamic range requirements meeting initial bandwidth metrics. - Critical design review of analog correlators meeting intrinsic hardware dynamic range in simulation. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from design completion to the start of device fabrication.			
Title: Reconfigurable, Actionable, Passive Technologies for Operational Remote Sensing (RAPTORS)	-	8.000	10.000
Description: The Reconfigurable, Actionable, Passive Technologies for Operational Remote Sensing (RAPTORS) program will enable a passive, all-optical kill chain capable of finding both stationary and moving targets with a single sensor. Sensor format can be selected based on platform requirements. RAPTORS will achieve this by combining tile able focal plane arrays (FPAs) that have adaptable spatial resolution with agile filters to adapt the spectral content of the infrared radiation impinging upon the detector. Using a custom read-out integrated circuit (ROIC), the FPA will intelligently balance resolution and number of spectral filters to optimize the information content transmitted off of the chip to enable real-time actionable decisions. This system will enable search and track and improved probability of detection and identification for hard targets, e.g., camouflaged, concealed, and deceptive (CCD) targets, at tactical speeds within the constraints of the cryocooler power limit. If successful, this capability has applications across ground, air, and space-based platforms. ***FY 2023 Plans:*** - Conduct initial design review for custom ROIC. - Design single-pixel filters demonstrating speed and information transmission. ***FY 2024 Plans:***			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Conduct advanced design review for custom ROIC. - Conduct final design review and Initiate fabrication of custom ROIC. - Demonstrate single-pixel filters demonstrating speed and information transmission. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from initial design review to final design review and initiation of fabrication of custom ROIC.			
Title: Robust Electronics for Radiative Environments (RE2) ***Description:*** The Robust Electronics for Radiative Environments (RE2) program will develop advanced radiation-hardened (rad-hard) and radiation-tolerant electronics, including processors and memory technologies, to meet the demands of emerging missions. Current rad-hard and rad-tolerant electronics are many generations behind state-of-the-art commercial electronics and cannot meet the needs of future systems. In order to address these needs, RE2 will work to deliver high-performance electronics for space and strategic systems while maintaining the security of these electronics throughout the supply chain. ***FY 2023 Plans:*** - Perform trade study on modifying advanced node complementary metal oxide semiconductor (CMOS) fabrication for rad-hard and rad-tolerant processors and memory. - Initiate design evaluation of candidate rad-hard and rad-tolerant processor and memory architectures. ***FY 2024 Plans:*** - Evaluate results of trade study on modifying advanced node complementary metal oxide semiconductor (CMOS) fabrication for rad-hard and rad-tolerant processors and memory. - Complete design evaluation of candidate rad-hard and rad-tolerant processor and memory architectures. - Perform analysis of impact of technology under development for space and strategic systems. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from initiating to completing design evaluation of candidate rad-hard and rad-tolerant processor and memory architectures.	-	5.000	7.000
Title: Next Generation Microelectronics - Advanced Manufacturing Tools ***Description:*** Next Generation Microelectronics - Advanced Manufacturing Tools addresses the development of new manufacturing tools for the design, fabrication, packaging, assembly, testing, and digital emulation of the next generation of advanced microsystems. Specifically, these advanced microsystems include three-dimensional heterogeneous integration (3DHI) and designs targeted for use in extreme environments such as high voltage, high current, high temperature, low temperature, and radiation exposure. New tools to improve manufacturing and testing will be designed, built, and characterized. These tools will enable cost-effective on-shoring of automated processes for packaging, assembly, and testing of advanced microsystems.	-	50.000	50.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
The software and hardware tools addressed in this program will advance integration techniques beyond current commercial capabilities to support national security needs. Design, verification, and security for 3DHI will be supported by coordinated investments that couple manufacturing and electronic design automation. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Establish tools for design, simulation, testing, and cost-optimization of 3DHI components and packages. - Develop specialized tools for design, simulation, and testing of thermally-hardened and radiation-hardened components and microsystems. - Initiate developing multi-domain models for virtual prototyping of 3DHI components and packages. - Create methodologies for design optimization for multi-chip, multi-technology packaging and assembly techniques consistent with high density interconnects. - Identify advancements required to automate packaging tools and metrology for volume 3DHI manufacturing. - Initiate development of methods to increase fidelity and accuracy of techniques for digital twin emulation to decrease prototyping cycle-time that includes system analysis. - Determine an equivalent to a front opening unified pod to facilitate automating die and chiplet handling during the assembly and packaging process. ***FY 2024 Plans:*** - Develop test and evaluation plans for tools for design, simulation, testing, and cost-optimization of 3DHI components and packages. - Continue development of specialized tools for design, simulation, and testing of thermally-hardened and radiation-hardened components and microsystems. - Continue developing multi-domain models for virtual prototyping of 3DHI components and packages. - Implement methodologies for design optimization for multi-chip, multi-technology packaging and assembly techniques consistent with high density interconnects. - Initiate development of automated packaging tools and metrology for volume 3DHI manufacturing. - Continue development of methods to increase fidelity and accuracy of techniques for digital twin emulation to decrease prototyping cycle-time that includes system analysis. - Demonstrate first version of tools for power and thermal management of high-voltage and high-current microsystems. - Evaluate methods for implementing security features into 3DHI electronics and their associated interconnects.			
Title: Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI)	-	40.000	40.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024

Description: Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI) addresses the unique manufacturing requirements for 3DHI microsystems, including design, fabrication, packaging, assembly, testing, and digital emulation. These new manufacturing methods will feature increasing circuit-scale interconnect densities for integration, and enhancing the security and interoperability of these complex designs. New multi-chip, multi-technology assembly and packaging will advance beyond silicon-centric integration to include integration of radio frequency (RF), photonics, novel memory, and compound semiconductors. In order to enable this diversity of materials and functions, integration technologies will be enabled by improving thermal management, improving inter-chip power delivery, and improving the modeling and simulation of these new systems on chip. Basic research related to this effort is funded within PE 0601101E, Project ES-02.

FY 2023 Plans:
- Initiate developing multi-chip, multi-technology assembly and packaging techniques consistent with high density interconnects (less than or equal to one-micron pitch).
- Identify techniques to improve co-planarity for die-to-die, wafer-to-wafer, and die-to-wafer high density interconnects.
- Launch development of integration techniques consistent with high-volume automation and inspection.
- Expand automated integration techniques to enable low-volume manufacturing.
- Implement manufacturing, assembly, and packaging techniques for high-density integration of photonics and electronics.
- Increase integration density of silicon digital microelectronic components with compound semiconductor RF microelectronic components through maturation of manufacturing, assembly, and packaging techniques.

FY 2024 Plans:
- Continue developing multi-chip, multi-technology assembly and packaging techniques consistent with high density interconnects (less than or equal to one-micron pitch).
- Perform initial characterization of techniques to improve co-planarity for die-to-die, wafer-to-wafer, and die-to-wafer high density interconnects.
- Continue development of integration techniques consistent with high-volume automation and inspection.
- Characterize performance of expanded automated integration techniques to enable low-volume manufacturing.
- Continue to implement manufacturing, assembly, and packaging techniques for high-density integration of photonics and electronics.
- Continue to increase integration density of silicon digital microelectronic components with compound semiconductor RF microelectronic components through maturation of manufacturing, assembly, and packaging techniques.
- Initiate design for demonstrating novel thermal management techniques in 3D assemblies.
- Develop requirements for a distributed heterogenous processing architecture.

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Develop a heterogenous memory compute element with high switching speed.			
Title: Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics	-	43.000	43.000
Description: Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics addresses the design, fabrication, packaging, assembly, testing, and digital emulation of the next generation of microsystems targeted for use in extreme environments: high voltage, high current, high temperature, low temperature, and radiation exposure. New manufacturing methods along with new testing and evaluation methods will be created, with an emphasis on developing techniques to enable in-situ measurements of these microsystems while operating in the extreme environments. These new manufacturing methods will also focus on a higher degree of automation in the packaging, assembly, and testing processes. This effort will also develop techniques to significantly improve thermal management, inter-chip power delivery, package integrity, and the modeling and simulation of these unique microsystems. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Initiate developing multi-chip, multi-technology assembly and packaging techniques for thermally-hardened and radiation-hardened microsystems. - Define device design and thermal management techniques for very high operating temperatures. - Initiate developing techniques for power management and thermal management of high-voltage and high-current microsystems. - Create extremely low-loss passive materials for efficient power distribution in high-voltage and high-current microsystems. ***FY 2024 Plans:*** - Continue developing multi-chip, multi-technology assembly and packaging techniques for thermally-hardened and radiation-hardened microsystems. - Perform initial design of devices and thermal management techniques for very high operating temperatures. - Initiate design of power management and thermal management systems of high-voltage and high-current microsystems. - Characterize extremely low-loss passive materials for efficient power distribution in high-voltage and high-current microsystems. - Perform trade study of testing needs for research and development of radiation-hardened electronics. - Analyze electronics sensor needs of hypersonic and other high operating temperature platforms. - Analyze potential approaches for passive ranging from airborne platforms.			
Title: Next Generation Microelectronics Prototyping - Designs	-	25.000	25.000
Description: Next Generation Microelectronics Prototyping - Designs supports the development of novel three-dimensional heterogeneous integration (3DHI) capable of being prototyped using the National Network for Next-generation Microelectronics Manufacture (N3M2). The N3M2 will include public-private partnerships that provide the ability to manufacture prototypes of next-generation 3DHI microsystems, including fabrication, packaging, assembly, and testing. The design challenges provide the opportunity to explore approaches that will improve and accelerate the adoption of 3DHI standardized chip-to-chip interfaces			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
and package optimization. Leading-edge chip designs will be fabricated, and subsequently integrated into 3DHI designs in multi-project demonstration runs. Research related to this effort is funded within PE 0603739E, Project MT-16. ***FY 2023 Plans:*** - Identify and initiate challenge problems for 3DHI microsystems and establish appropriate metrics. - Determine goals for design challenges for standardized chip-to-chip integration practices. - Establish a fabrication run for leading-edge chips to develop components for novel 3DHI prototype designs. ***FY 2024 Plans:*** - Run two design challenges for 3DHI microsystems standardized chip-to-chip integration practices. - Complete two fabrication runs for leading-edge chips as components for novel 3DHI prototype designs. - Assess and validate assembly design kit based upon novel 3DHI prototype designs from challenge runs. - Update goals for the next set of design challenges for standardized chip-to-chip integration practices based up assessment of assembly design kit and the interface standard.			
Title: H6 ***Description:*** The H6 program, building on technology developed in the Lasers for Universal Microscale Optical Systems (LUMOS) program (budgeted in this PE and Project), is developing the first tactical-grade clock. Tactical-grade clocks are ultra-small, low power, fieldable and can maintain the timing needed for DoD-relevant applications in challenging environments. Precise timing in a tactical package will decouple operations from GPS dependence, overcoming a significant operational vulnerability for the warfighter. Precise tactical-grade clocks from H6 will enable increased signal assurance and pervasive communications security in high-jamming regions. Additionally, H6 will enable real-time, physical monitoring and tracking of warfighters and special forces and will play a critical role in search and rescue through the ability to maintain precise time over a long mission duration without having to re-establish external communications. ***FY 2023 Plans:*** - Demonstrate the principle of operation for the tactical-grade clock. - Develop sensor components for temperature-insensitive operation of the clock. - Measure the clock stability. ***FY 2024 Plans:*** - Initiate construction of tactical-grade clock components. - Demonstrate temperature-insensitive operation in realistic environments. - Develop clock components towards miniaturization of the final system. ***FY 2023 to FY 2024 Increase/Decrease Statement:***	-	12.000	15.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
The FY 2024 increase reflects the shift from initial design to initiating construction of tactical-grade clock components.			
Title: Technologies for Heat Removal in Electronics At the Device Scale (THREADS)*	-	14.000	28.000
Description: *Previously part of Next Generation Microelectronics - Advanced Manufacturing Tools The Technologies for Heat Removal in Electronics At the Device Scale (THREADS) program will develop technologies to overcome transistor thermal limits to realize robust, high power density transistors that operate near their fundamental electronic limit of radio-frequency (RF) output power. DoD's RF transmitters increasingly use high-power gallium nitride (GaN) wide bandgap (WBG) transistors, which provide a 5X improvement in RF power output compared to the legacy gallium arsenide (GaAs) technology. Achieving high RF power output while maintaining a transistor operating temperature below the nominal maximum reliable operation temperature faces two challenges. First, reducing thermal resistance within the device. This will be achieved by leveraging recent advances epitaxial growth processes and phonon bridges to reduce semiconductor material thermal resistance. Second, more efficiently moving heat away from the transistor "hot spots". This will be achieved through novel transistor topologies and by leveraging recent advances in the integration of 2D and 3D cooling structures and high thermal conductivity materials, such as diamond, into the transistor. THREADS will demonstrate high efficiency X-band (8-12 GHz) transistors and power amplifier (PA) test vehicles with an output power density of 81 W/mm (16X higher than production GaN amplifiers). THREADS technology will enable increased range for radar, communications, and electronic warfare systems. ***FY 2023 Plans:*** - Initiate development of preliminary concepts and test structures for the reduction of transistor thermal resistance. - Initiate development of preliminary concepts for robust RF PAs with increased output power density. ***FY 2024 Plans:*** - Finalize preliminary concepts for the reduction of transistor thermal resistance. - Fabricate thermal resistance test structures and measure a 2.5X reduction in thermal resistance. - Finalize preliminary concepts for robust RF PAs with increased output power density. - Fabricate transistors and PAs and measure a 5X increase in output power density. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects a shift from initial development to finalizing preliminary concepts.			
Title: Minitherms3D*	-	9.341	18.000
Description: * Previously part of Next Generation Microelectronics - 3DHI			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
Minitherms3D will develop thermal management solutions for the three-dimensional heterogeneous integration (3DHI) of microelectronics, to accelerate the growth of compact, high high-performance microsystems. 3DHI microsystems are enabling for phased array systems, and for dense computing for on artificial intelligence / machine learning applications. Minitherms3D will reduce the size, weight and power (SWaP) of high high-performance 3DHI microsystems by developing new methods to remove heat from within the 3D stack, transmit it further away to the outer boundaries of the stack, and reject it to outside the ambient environment. ***FY 2023 Plans:*** - Efficiently mitigate localized hot spots within a single tier in a 3D stack. - Begin development of thermal isolation solutions between adjacent functional blocks. ***FY 2024 Plans:*** - Develop in-tier heat removal solutions. - Begin development of efficient thermal link to heat rejection components. - Begin development of low-SWaP thermal rejection components. - Provide a three-tier test vehicle to demonstrate improved thermal management capabilities. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from initial concept to begin developing new methods to remove heat with the 3D stack.			
Title: Space Power Conversion Electronics (SPCE)* ***Description:*** *Previously part of Next Generation Microelectronics - Extreme Environment Electronics The Space Power Conversion Electronics (SPCE) program is developing highly efficient, radiation radiation-tolerant point of load (POL) converters for low-earth-orbit satellites. In today's space power systems, POL converters derate their operating voltage to maintain radiation- tolerance, resulting in decreased efficiency and limiting the satellite's available power, capabilities, and battery lifetime. To address this deficiency, SPCE will develop high-performance, radiation radiation-tolerant high voltage switches by exploiting advanced wide-bandgap semiconductor advance material synthesis, novel device architectures, and 3D heterogeneous integration technology. ***FY 2023 Plans:*** - Perform initial analysis of candidate wide-bandgap material systems for radiation-tolerant high voltage transistors with increased switching performance.	-	12.000	21.200

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Perform initial simulations of expected switching performance of advanced radiation-tolerant high voltage transistors enabled by wide-bandgap materials. ***FY 2024 Plans:*** - Complete analysis of candidate wide-bandgap material systems for radiation-tolerant high voltage transistors with increased switching performance. - Complete initial simulations of expected switching performance of advanced radiation-tolerant high voltage transistors enabled by wide-bandgap materials. - Perform design of high-performance radiation-tolerant high voltage switches enabled by wide-bandgap semiconductor transistors. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects a shift from initial development of tools to demonstration.			
Title: Faithful Integration Reverse-engineering and Emulation (FIRE)* ***Description:*** *Previously part of Next Generation Microelectronics - Advanced Manufacturing Tools The Faithful Integration Reverse-engineering and Emulation (FIRE) program will develop tools to find and patch vulnerabilities within cyber-physical systems. FIRE will develop novel modeling and simulation techniques to help expedite finding and patching vulnerabilities in cyber-physical systems. ***FY 2023 Plans:*** - Begin development on modeling and simulation tools. ***FY 2024 Plans:*** - Creation of a surrogate cyber-physical test vehicle to demonstrate the tools. - Proof of concept demonstration of tools on the surrogate cyber-physical test vehicle. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects a shift from initial development to proof of concept of tools.	-	3.000	14.040
Title: NanoWatt Platforms for Sensing, Analysis, and Computation (NaPSAC)* ***Description:*** *Previously part of Next Generation Microelectronics 3DHI Efficient, high-speed scientific computing architectures are a ubiquitous requirement for applications including modeling of complex physical systems, advanced device designs, and multiscale computations of dynamical phenomena such as climate models or turbulence. Current state-of-the-art computing systems requires prohibitive amounts of energy and time to perform	-	5.500	14.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
such calculations. The NanoWatt Platforms for Sensing, Analysis, and Computation (NaPSAC) program aims to develop a novel computational architecture for massively parallel, ultralow power "in-memory" computation. NaPSAC-based computing architectures can potentially yield transformative impact by enabling beyond-state-of-the-art computational speed and accuracy. Applications of immediate relevance to the DoD include simulations of turbulent flows, multiscale electromagnetic simulations of plasma dynamics, advanced semiconductor device design, and the modeling of high-performance materials. ***FY 2023 Plans:*** - Develop theoretical concepts and initial device designs for novel nanoresonator-based computational architectures for advanced high-speed scientific computing. ***FY 2024 Plans:*** - Develop computational algorithms to enable efficient computations of complex systems including high performance materials and advanced semiconductor devices. - Demonstrate preliminary proof-of-concept prototypes of novel nanoresonator-based computing engines for high speed, energy efficient scientific computations. - Perform concept validation and preliminary benchmarking of computing accuracy, speed and power efficiency of nanoresonator computing modules. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects a shift from initial device design to prototype development.			
Title: Optomechanical Thermal Imaging (OpTIm)* ***Description:*** *Previously part of Next Generation Microelectronics - Microelectronics Prototyping Designs Advanced infrared (IR) detectors and thermal imaging systems underpin a vast DoD application space including biochemical detection; infrared Search-and-Track; and terrestrial and space-based Intelligence, Surveillance, and Reconnaissance. Current IR detectors suffer from numerous limitations including poor sensitivity, poor signal bandwidth, or the need for expensive cryogenic cooling. The Optomechanical Thermal Imaging (OpTIm)* program will develop a new modality of low size, weight, and power, room temperature IR detectors capable of quantum-level sensitivity, thereby enabling transformative enhancements to DoD capabilities including, but not limited to, night vision, surveillance, hyperspectral detection, and remote detection of trace industrial pollutants or other anthropogenic activity. ***FY 2023 Plans:***	-	5.000	12.300

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Develop designs and fabrication processes for a new modality of quantum-level infrared (IR) detectors for applications including chemical or pathogen detection. ***FY 2024 Plans:*** - Investigate technical and fundamental performance limits of this modality of IR detection. - Execute device simulations and demonstrations of single-pixel prototypes of a new modality of infrared detection. - Demonstrate design, simulation, and fabrication of novel detection surface coatings capable of identifying specific chemical or biological signatures in the infrared spectrum. - Develop device designs to extend single-pixel IR detector concepts to larger arrays for applications including IR imaging and surveillance. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects a shift from design to fabrication and demonstration.			
Title: Processor Reconfiguration for Wideband Sensing Systems (PROWESS)	-	8.000	9.500
Description: The Processor Reconfiguration for Wideband Sensing Systems (PROWESS) program, building on technology developed in the Digital RF Battlespace Emulator (DRBE) program (budgeted in this PE and Project), will develop high-throughput streaming-data processors that change their programming at nanosecond timescales to detect novel radiofrequency (RF) signals. Sensing complex and unanticipated signals across wide RF bandwidths is limited by the computing capacity available at the tactical edge. Today's tactical spectrum sensors rely on field-programmable gate arrays (FPGAs) for low-latency, high-throughput signal processing. Since FPGA reconfiguration time (milliseconds) is much slower than RF signal dynamics (nanoseconds), FPGAs cannot optimize their signal processing in real time as new signals are observed. Recent advances in application-specific processing arrays, real-time task scheduling, and high-bandwidth input/output enable the development of new run-time reconfigurable array (RTRA) processors capable of reprogramming themselves as new signals are received. PROWESS will investigate RTRA processors and receiver integration approaches to enhance the performance of tactical RF sensors in congested spectrum. ***FY 2023 Plans:*** - Derive low-level processing benchmarks for high-throughput spectrum sensing applications. - Develop preliminary concept designs for RTRA processor test chips. ***FY 2024 Plans:*** - Develop preliminary concept designs to integrate RTRA processors into complete spectrum sensing systems. - Finalize concept design for RTRA processor test chips.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
- Conduct design review of RTRA processor test chips and their integration into systems. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects the shift from initial concept designs to finalizing concept designs for the test chips and their integration into systems integration.			
Title: Quantum Apertures (QA) ***Description:*** The Quantum Apertures (QA) program will develop novel radio receiver and aperture systems using quantum sensors as the receiving elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly-excited "Rydberg" states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. The receiver system's enhanced capabilities will be leveraged in this program to develop novel waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum receiving elements, lasers to program the sensor and read out radio signals, and processing electronics. Prior to FY 2024, this program was funded in PE 0602716E, Project ELT-01. ***FY 2024 Plans:*** - Design an architecture for quantum aperture sensors in multiple-element arrays. - Demonstrate novel waveforms reception by quantum aperture. - Conduct quantum aperture sensor testing within a DoD-cleared facility. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The program was originally funded in PE 0602716E, ELT-01. The FY 2024 decrease reflects the shift from development of a specific architecture and system design to demonstration and testing.	-	-	12.000
Title: Predictive Antijam Artificial Intelligence Receivers (PAIR) ***Description:*** The Predictive Antijam Artificial Intelligence Receivers (PAIR) program aims to develop a next-generation artificial intelligence (AI)-enabled antijam receiver, to enable reliable communications links in a fully congested spectrum. Today's mission-relevant communication spectrum has become increasingly congested, leading to signal loss, signal distortion and link loss. Today's state-of-the-art receivers utilize analog limiters and filters, power hungry oversampling analog to digital converters, and advanced digital signal processing to attempt to operate through the spectrum clutter, but struggle to maintain dynamic range and signal quality at the receiver. To be successful, the PAIR program will leverage advances in predictive AI-controlled filters and analog to digital converters, as well as neural network digital signal processing producing low latency real-time feedback to	-	-	6.500

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
the receiver components. These innovations will deliver intelligent in-band interference removal, low-power high dynamic range analog to digital signal conversion, and efficient back end neural net signal processing to produce a high data rate communication link with unparalleled hardware dynamic range. The PAIR program will enable new capabilities in tactical and long-range radio frequency (RF) communication systems, addressing future military needs for assured, on-demand, antijam information delivery, in environments where today communication would be impossible. ***FY 2024 Plans:*** - Perform system level study of AI-based receiver requirements necessary to achieve the program goals. Utilize system study to derive requirements for interference suppression, data conversion, signal purification and channel prediction targets. - Develop individual AI-enabled receiver components including analog filters, analog to digital converters, and neural network digital signal processors meeting the derived system study requirements - Demonstrate predictive low latency feedback loops necessary to control analog filters and analog digital converters with neural network signal processing architecture. - Design and simulate first-generation functional test prototype of the antijam RF receiver. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 increase reflects program initiation.			
Title: Analog-to-Decision Classifier (A2DC) ***Description:*** The Analog-to-Decision Classifier (A2DC) program will increase automated classification capabilities at the edge and simultaneously reduce the size, weight, and power (SWaP) needs of edge platforms. Currently, sensor outputs are digitized at the edge, which consumes SWaP and limits capabilities of edge platforms, but are then transmitted for processing at the command center. A2DC aims to skip or delay the digitization step and implement analog inferencing and compression techniques directly on the analog sensor data at the edge. A2DC objectives are to enable 1000-fold reduction on data transmission bandwidth required to communicate results for follow-on processing, and 100-fold reduction on SWaP for classification and processing of sensor data. A2DC will enable edge processing for missions that collect large amounts of sensor data, such as hyper spectral imaging for unmanned aerial systems. ***FY 2024 Plans:*** - Initiate development of analog feature extraction and classification techniques for analog sensor data. - Initiate development of inferencing and compression algorithms. - Perform initial hardware and algorithm co-design analysis for the system design of representative mission-relevant sensor systems. ***FY 2023 to FY 2024 Increase/Decrease Statement:***	-	-	7.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
The FY 2024 increase reflects program initiation.			
Title: Guaranteed Architectures for Physical Security (GAPS) ***Description:*** The Guaranteed Architectures for Physical Security (GAPS) program is developing hardware security and software architectures with provable security interfaces. These interfaces will physically isolate high-risk transactions during both system design and system build, and will ensure that such protections are enforced at run-time. GAPS will reduce the inherent complexity through the development of hardware and software that is open, extendible, and compatible with size, weight, and power constrained environments to enable security across DoD and commercial systems. The program will substantially lower the barrier to safely enabling high-risk transactions, thus allowing for fast computer-to-computer transactions, physical spatial isolation reducing the need for unreliable software partitioning solutions, and more complex missions without putting sensitive data at risk. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2023 Plans:*** - Implement interconnect architectures and board support packages for a single common embedded bus while increasing to three protocol layers or more. - Demonstrate further reduction in transaction overhead on embedded busses when implementing GAPS extensions for multilevel security. - Permit multiple gigabits per second sustained data throughput across multiple security level architectures. ***FY 2023 to FY 2024 Increase/Decrease Statement:*** The FY 2024 decrease reflects program completion.	14.000	12.000	-
Title: Structured Array Hardware for Automatically Realized Applications (SAHARA) ***Description:*** The Structured Array Hardware for Automatically Realized Applications (SAHARA) program is developing technology for the secure development of custom chips for defense systems. Current DoD systems often employ field-programmable gate array (FPGAs), whose flexibility advantages are offset by lower performance. Structured application specific integrated circuits (ASICs) deliver significantly higher performance and lower power consumption, which makes them an efficient and effective alternative to FPGAs for defense electronic systems. Manually converting FPGAs to structured ASICs, however, is a complex, lengthy, and costly process. SAHARA is developing automated technologies to reduce design time, optimize performance, and minimize the power dissipated by the secure, structured ASIC. ***FY 2023 Plans:*** - Finalize design of secure, structured ASICs. - Analyze transition impact of secure, structured ASICs for DoD applications. ***FY 2023 to FY 2024 Increase/Decrease Statement:***	3.500	7.500	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
The FY 2024 decrease reflects program completion.			
Title: Beyond Scaling - Materials ***Description:*** The Beyond Scaling - Materials program demonstrated the integration of novel materials into next-generation logic and memory components. This program pursued potential enhancements in electronics that do not rely on Moore's Law, i.e., silicon transistor scaling, including research into new materials and the implications of those materials at the device, algorithm, and packaging levels. Research areas included heterogeneous integration of multiple materials, "sticky logic", and novel transistor devices that combine elements of computation and memory with three-dimensional vertical circuit integration to demonstrate dramatic performance improvements using older silicon technologies. Basic research for this program was funded within PE 0601101E, Project ES-02.	16.000	-	-
Title: Beyond Scaling - Architectures ***Description:*** The Beyond Scaling - Architectures program demonstrated a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program explored technologies and techniques such as new domain-specific circuit architectures, co-design of electronics hardware and software, intelligent edge sensors, hardware security architectures, and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Basic research for this program was funded within PE 0601101E, Project ES-02.	18.000	-	-
Title: Beyond Scaling - Design ***Description:*** The Beyond Scaling - Design program developed and demonstrated the tools required for rapidly designing and deploying specialized circuits. Research efforts explored technologies and techniques for rapid, specialized design such as intelligent design tools, automated physical layout generation, and open-source circuit design. The goal of this program was to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a pathway for the rapid upgrade of electronics. Advances under this program demonstrated a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon transistor scaling. Basic research for this program was funded within PE 0601101E, Project ES-02.	11.993	-	-
Title: System Security Integrated Through Hardware and firmware (SSITH) ***Description:*** The System Security Integrated Through Hardware and firmware (SSITH) program sought to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. SSITH provided new research in electronics hardware security and exploited current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas was enabled by the extremely capable semiconductor technology driven by Moore's Law. The program also investigated flexible hardware	7.000	-	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2022	FY 2023	FY 2024
architectures that adapted to and limited the impact of new cybersecurity attacks. Finally, SSITH mitigated the potential negative impact of new security protection architectures on system performance and power usage. SSITH capabilities are applicable to both commercial and military electronic systems.			
Accomplishments/Planned Programs Subtotals	208.849	421.001	451.825

	FY 2022	FY 2023
Congressional Add: ERI 2.0 - Congressional Add	36.000	-
FY 2022 Accomplishments: - Identify tools for software/hardware logic co-design to identify three-dimensional heterogeneous integration (3DHI) security vulnerabilities. - Evaluate status of additive manufacturing for 3DHI. - Characterize current state of automation in packaging tools, metrology, and test for 3DHI to identify capabilities required for fully automated 3DHI manufacturing. - Analyze techniques for digital twin emulation of microsystems and associated methods for validation of complete digital models. - Initiate developing multi-domain models for virtual prototyping of three-dimensional heterogeneous integration (3DHI) components and packages. - Initiate developing co-design techniques for optimizing a thermal floorplan and performance in microsystems. - Investigate new dielectric and magnetic materials integrated into high power and high temperature microsystems. - Identify methodologies to develop multi-physics, multi-scale design tools that incorporate on-chip generated electromagnetic interference effects in high-voltage and high-current microsystems.		
Congressional Adds Subtotals	36.000	-

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A