Exhibit R-2, RDT&E Budget Item Justification: PB 2025 Defense Advanced Research Projects Agency	Date: March 2024
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

COST ($ in Millions)	Prior Years	FY 2023	FY 2024	FY 2025 Base	FY 2025 OCO	FY 2025 Total	FY 2026	FY 2027	FY 2028	FY 2029	Cost To Complete	Total Cost
Total Program Element	-	527.882	572.662	573.265	-	573.265	527.916	525.030	558.054	568.074	-	-
ELT-01: *ELECTRONIC TECHNOLOGY*	-	105.209	120.837	88.921	-	88.921	107.331	114.289	120.835	125.136	-	-
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	422.673	451.825	484.344	-	484.344	420.585	410.741	437.219	442.938	-	-

A. Mission Description and Budget Item Justification

The efforts described in this Program Element (PE) address the Applied Research associated with the Electronics Technology Program that is directed towards developing electronics that make a wide range of military applications possible. The PE focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter. This PE also supports innovation and robust transition planning in the technology cycle by working with entrepreneurs to increase the likelihood that DARPA funded technologies take root in the U.S. and provide new capabilities for national defense.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project pursues electronics performance advancements that exploit new concepts in circuit specialization and three-dimensional heterogeneous integration (3DHI) by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our microelectronics infrastructure relies, this envisioned specialization will require incorporation of security safeguards and advancing manufacturing tools and process automation. Accordingly, programs within the Beyond Scaling Technology project will reduce barriers to making specialized circuits in today's silicon hardware and 3DHI by improving producibility. This will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized microelectronics, particularly for operation in extreme environments. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting 3DHI to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

Exhibit R-2, RDT&E Budget Item Justification: PB 2025 Defense Advanced Research Projects Agency	Date: March 2024
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

B. Program Change Summary ($ in Millions)	FY 2023	FY 2024	FY 2025 Base	FY 2025 OCO	FY 2025 Total
Previous President's Budget	554.155	572.662	595.500	-	595.500
Current President's Budget	527.882	572.662	573.265	-	573.265
Total Adjustments	-26.273	0.000	-22.235	-	-22.235
• Congressional General Reductions	0.000	0.000			
• Congressional Directed Reductions	0.000	0.000			
• Congressional Rescissions	0.000	0.000			
• Congressional Adds	0.000	0.000			
• Congressional Directed Transfers	0.000	0.000			
• Reprogrammings	-8.431	0.000			
• SBIR/STTR Transfer	-17.842	0.000			
• TotalOtherAdjustments	-	-	-22.235	-	-22.235

Change Summary Explanation

FY 2023: Decrease reflects SBIR/STTR transfer and reprogrammings.

FY 2024: N/A

FY 2025: Decrease reflects minor program repricing.

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency			Date: March 2024
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / *ELECTRONICS TECHNOLOGY*	Project (Number/Name) ELT-01 / *ELECTRONIC TECHNOLOGY*	

COST ($ in Millions)	Prior Years	FY 2023	FY 2024	FY 2025 Base	FY 2025 OCO	FY 2025 Total	FY 2026	FY 2027	FY 2028	FY 2029	Cost To Complete	Total Cost
ELT-01: *ELECTRONIC TECHNOLOGY*	-	105.209	120.837	88.921	-	88.921	107.331	114.289	120.835	125.136	-	-

A. Mission Description and Budget Item Justification

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Areas of particular emphasis of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards. This project has six major focus areas: Electronics, Photonics, Microelectromechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
Title: Fast Event-based Neuromorphic Camera and Electronics (FENCE)	19.500	16.037	7.000

Description: The Fast Event-based Neuromorphic Camera and Electronics (FENCE) program will develop and demonstrate a low latency, low power event-based infrared (IR) camera to enable intelligent sensors for tactical DoD applications. Event-based imagers are an emerging class of sensors with major demonstrated advantages relative to traditional cameras. State-of-the-art visible event-based cameras have been shown to produce over two orders of magnitude less data in optimal conditions relative to traditional framing cameras because they transmit data only from pixels that have changed. This leads directly to two orders of magnitude lower data latency and a commensurate reduction in power consumption. Despite their inherent advantages, existing event-based cameras are not compatible with DoD applications because DoD applications regularly face conditions that are not optimal, where issues such as clutter and noise cause a large percentage of the event-based pixels to change simultaneously. When this happens, today's event-based cameras do not perform significantly better than traditional cameras. FENCE will develop an infrared event-based imager consistent with military requirements. FENCE will develop a four-megapixel asynchronous read-out integrated circuit (ROIC), co-designed with a 3D integrated processor that will intelligently remove noise and clutter to maintain low power and latency operation even when faced with all of the pixels firing simultaneously. If successful, this new class of sensors enabled by FENCE will be capable of responding to fast moving targets and discriminating dim targets in noisy conditions.

FY 2024 Plans:
- Measure processing layer power consumption.
- Integrate components into full focal plane array (FPA).

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Measure integrated processor layer power consumption. ***FY 2025 Plans:*** - Conduct ROIC control demonstration. - Perform initial FPA functionality testing. - Test fully integrated camera for final program metrics. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects moving from design and fabrication to integration and testing.			
Title: Waveform Agile Radio-frequency Directed Energy (WARDEN)	15.000	20.000	8.000
Description: The Waveform Agile Radio-frequency Directed Energy (WARDEN) program aims to extend the range and lethality of high-power microwave (HPM) systems by introducing flexible waveform techniques that use combinations of frequency, amplitude, and pulse-width modulations to significantly improve electromagnetic coupling into complex target enclosures and increase the probability of disruption or damage to internal electronic components and circuits. Applications for HPM systems include counter-unmanned aerial systems (C-UAS), vehicle and vessel disruption, electronic strike, and guided missile defense. Current HPM systems use oscillators to produce electromagnetic radiation. These systems are inherently narrowband and lack the frequency agility to support waveforms to maximize electromagnetic coupling and to optimally exploit electronic system vulnerabilities. Lacking the capability to use optimized waveforms, HPM oscillators have been pushed close to the physical limits of peak power generation. To develop a more efficient, lower power, waveform agile approach, the WARDEN program will develop and demonstrate the first broadband HPM amplifier; create new theory and simulation tools to predict electromagnetic coupling into complex enclosures and the effects on electronics; and develop novel agile waveform techniques capable of reducing the susceptibility threshold of targeted electronics systems to HPM attack. ***FY 2024 Plans:*** - Experimentally demonstrate broadband amplifier power, bandwidth, and pulse duration performance at low repetition rates. - Integrate electromagnetic coupling tools that combine deterministic, reduced-model, and statistical approaches into a hybrid framework. - Validate electromagnetic coupling tools and predictive models through comparison with experimental measurements. - Demonstrate disruptive agile waveform techniques on integrated electronics. ***FY 2025 Plans:*** - Experimentally demonstrate broadband amplifier power, bandwidth, and pulse duration performance at full repetition rate using WARDEN developed waveforms. - Demonstrate integrated electromagnetic coupling tools that combine deterministic, reduced-model, and statistical approaches using a hybrid framework.			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Validate electromagnetic coupling tools and predictive models through comparison with experimental measurements on relevant targets. - Demonstrate disruptive agile waveform techniques on integrated electronics relevant to the DoD. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the move from development to demonstration and validation.			
Title: Generating RF with Photonics for low Noise (GRYPHON) ***Description:*** The Generating RF with Photonics for low Noise (GRYPHON) program will develop compact sources of microwaves and millimeter waves with extremely low phase noise. Compact signal sources used today, such as crystal oscillators, are too noisy to support advanced military radar and communications functions. Conversely, best-in-class oscillators which use optical techniques to synthesize extremely pure microwaves are too large and expensive to deploy on the airborne systems, munitions, and other size-constrained platforms where the DoD requires high-performance capabilities. The GRYPHON program will draw on recent advances in miniature optical components to replicate best-in-class optical frequency synthesis techniques in microchip form factors. ***FY 2024 Plans:*** - Demonstrate microwave generation with frequency tunability. - Reduce phase noise of components and microwave synthesizers. - Characterize environmental robustness of microwave oscillators. ***FY 2025 Plans:*** - Package microwave synthesizers into compact modules. - Optimize the design of synthesizers with output across multiple frequency bands. - Optimize the design of synthesizers with robustness to environmental stress. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the move from development to design optimization.	16.000	14.000	6.000
Title: Humboldt ***Description:*** The Humboldt program seeks to develop directed energy (DE) devices to produce disruptive effects in electronic systems. The devices have potential for dual-use as sources to characterize the susceptibility of commercial electronics to electromagnetic interference (EMI). ***FY 2024 Plans:*** - Experimentally characterize the operation of the proof-of-concept devices.	9.500	17.000	15.300

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Demonstrate the effectiveness of the proof-of-concept devices on electronic systems. - Validate the effectiveness of the proof-of-concept devices on electronic systems. ***FY 2025 Plans:*** - Develop integrated devices in final form factor. - Experimentally characterize the operation of the fully-integrated devices. - Validate the effectiveness of the fully-integrated devices. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the move from proof-of-concept to the development of fully-integrated devices.			
Title: Ultra-Wide BandGap Semiconductors (UWBGS)*	-	13.000	22.621
Description: *Formerly Robust Protection for Electronic Systems (ROPES) The Ultra-Wide BandGap Semiconductors (UWBGS) program will develop and optimize ultra-wide bandgap (UWBG) materials and fabrication processes required to enable the next revolution in semiconductor electronics. UWBGS will establish the foundation for the creation of producible and reliable, high performance UWBG devices for a variety of DoD (and commercial) applications. These include, but are not limited to: high power radio frequency (RF) switches; high power density RF amplifiers; high RF power protection device; high voltage switches for power electronics; high temperature electronics and deep ultraviolet light-emitting diodes and lasers. The program will address the key technical challenges that are limiting the performance of UWBG device. These challenges include realizing high quality UWBG materials, ability to tailor electrical characteristics of UWBG materials; ability to create homo- and heterostructures with abrupt junctions and low defect density; and the realization of ultra-low resistance electrical contacts. UWBGS will fabricate device test structures to quantify the improvements in these areas. To be successful, the program will leverage recent advances in UWBG materials. ***FY 2024 Plans:*** - Develop UWBG material synthesis approaches to reduce defect density and improve doping and uniformity required for producing UWBG devices; establish a baseline for material quality by designing, fabricating, and characterizing test structures. - Develop materials and fabrication process to create low resistance electrical contacts to UWBG materials; fabricate and characterize test structures to quantify improvement in contact resistance. ***FY 2025 Plans:*** - Optimize UWBG material synthesis approaches to reduce defect density and improve doping and uniformity; quantify improvements in material quality by designing, fabricating, and characterizing test structures. - Optimize fabrication process to create robust, low resistance electrical contacts to UWBG materials; fabricate and characterize test structures to quantify robustness and improvement in contact resistance.			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Evaluate characterization results versus current state-of-the-art to quantify the improvement possible with UWBG devices. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from investigating approaches and processes of interest to materials and device development and optimization.			
Title: Scalable Analog Neural networks (ScAN) ***Description:*** Building upon technologies discovered under the Fast Event-based Neuromorphic Camera and Electronics (FENCE) program, the Scalable Analog Neural networks (ScAN) program will increase neural network (NN) inferencing capabilities at the edge and simultaneously reduce the size, weight, and power (SWaP) needs of edge platforms. Currently, sensor outputs are digitized at the edge, which consumes SWaP and limits capabilities of edge platforms, but are then transmitted for processing at the command center. ScAN aims to skip or delay the digitization step and implement analog inferencing and compression techniques directly on the analog sensor data at the edge. ScAN objectives are to enable 2000-fold reduction in SWaP for processing of sensor data. ScAN will enable intelligence generation at the edge for missions that collect large amounts of sensor data, such as hyper-spectral imaging for unmanned aerial systems. ***FY 2024 Plans:*** - Initiate development of analog feature extraction and classification techniques for analog sensor data. - Initiate development of inferencing and compression algorithms. - Perform initial hardware and algorithm co-design analysis for the system design of representative mission-relevant sensor systems. ***FY 2025 Plans:*** - Demonstrate analog hardware at medium scales. - Extend development of analog feature extraction and classification techniques to larger scales. - Extend development of inferencing and compression algorithms to larger scales. - Extend hardware and algorithm co-design analysis to larger-scale, mission-relevant sensor systems. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from initial design and development to design finalization and initial demonstration.	-	6.800	19.000
Title: Warfighting Performance for Electronic Technology ***Description:*** Studies conducted under this thrust explore electronics and electronic systems have the potential to offer disruptive performance for the warfighter. This includes advancing the underlying electronics and leveraging the gains associated with tightly integrating advanced electronics at the module and system level. The feasibility and impact of these potential improvements is	-	-	7.000

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Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
also evaluated. Topics include: processing architectures for modern digital arrays, advanced software algorithms for electronic systems, and passive target tracking technologies ***FY 2025 Plans:*** - Evaluate high performance computing and processing architectures and needs in modern digital arrays. - Perform analysis of the current state-of-the-art of array algorithms and identify areas for development. - Identify trade space of active and passive tracking techniques for advanced targeting applications. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects thrust initiation.			
Title: Non-Kinetic Delivery for Electronic Technology ***Description:*** Studies conducted under this thrust examine and evaluate new technologies that employ non-physical means to degrade or deny targeted adversary capabilities. Studies are also being conducted to investigate technologies to protect against intentional and unintentional non-kinetic effects on friendly systems. The feasibility and potential impact of these technologies for the warfighter is also evaluated. Topics include: high power radio frequency (RF) and optical sources, ultrawide bandgap materials, RF filters, rectifiers, and diodes, and advanced modeling and simulation capabilities. ***FY 2025 Plans:*** - Perform trade study for suitability of using non-kinetic effects across a suite of relevant DoD missions. - Evaluate candidate RF and optical materials and architectures for high power sources to be used for non-kinetic effects. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects thrust initiation.	-	-	4.000
Title: Focal Arrays for Curved Infrared Imagers (FOCII) ***Description:*** The Focal Arrays for Curved Infrared Imagers (FOCII) program is developing curved focal plane arrays for broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. FOCII will leverage curving strategies for state-of-the-art focal plane arrays combined with advances in designing and manufacturing stress relief features to demonstrate hardware that simultaneously provides maximum resolution and illumination. This program will develop novel designs for IR imagers that enable minimal size, weight and cost for size-constrained applications. This will enable new applications in passive seeker technology for missiles, overhead persistent infrared imaging, 360-degree situational awareness, infrared search and track, and long-range targeting. ***FY 2024 Plans:*** - Measure radiometric performance of large area focal array curved to final program specified objective radius.	10.000	9.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Demonstrate thermal cycling of large area focal array curved to final program specified objective radius. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.			
Title: Wideband Adaptive RF Protection (WARP) ***Description:*** The Wideband Adaptive RF Protection (WARP) program is developing radio-frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference through tunable filtering, limiting, and/or signal cancellation. The ability to create tunable and reconfigurable band pass and band stop filters at microwave frequencies will be important for implementing transmit/receive modules in next-generation multi-function arrays. Another important area of interference mitigation is self-interference. WARP is developing the signal cancellation technology that will listen to the transmitted interfering signal and subtract it from the input of the receiver so faint signals near the noise floor can still be detected. Program research will provide feedback mechanisms that intelligently correct these problems. Whether for self-induced interference or external interference jamming, WARP is developing intelligent filtering and self-interference cancellation technologies to protect wideband DoD receivers. ***FY 2024 Plans:*** - Scale adaptive wideband adaptive filter designs to provide full-band coverage. - Scale adaptive analog signal canceller designs to full-band coverage of low-band and high-band. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.	14.000	14.000	-
Title: Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) ***Description:*** The Quantum Imaging of Vector Electromagnetic Radiation (QuIVER) program is developing full-tensor magnetic field sensors and will demonstrate them in DoD-relevant applications and concept of operations. In addition to being diagnostically relevant, such sensitive magnetometers could enable future human-machine/brain-machine interfaces. The DoD and industry also use magnetometers for magnetic anomaly detection, which may allow for the discovery of mineral/oil deposits, discovery of old wellheads, or the detection of improvised explosive devices. In addition, magnetometers offer the possibility of magnetic navigation, which may operate in GPS-denied environments. Recent advancements have resulted in the potential to develop highly-sensitive vector magnetometers, which would enable the consequent development of sensitive full-tensor gradient sensors. Such tensors offer more degrees of freedom than their scalar or vector counterparts and potentially provide additional information about the source of the magnetic field. ***FY 2024 Plans:*** - Design reduced size, weight, and power (SWaP) tensor magnetometer with sensor fusion and automation.	13.000	11.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Complete construction of reduced-SWaP tensor magnetometer system for field testing and validate sensitivity and functionality. - Perform field test of reduced-SWaP tensor magnetometer system. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.			
Title: Quantum Apertures (QA) ***Description:*** The Quantum Apertures (QA) program will develop novel radio receiver and aperture systems using quantum sensors as the receiving elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly-excited Rydberg states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. The receiver system's enhanced capabilities will be leveraged in this program to develop novel waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum receiving elements, lasers to program the sensor and read out radio signals, and processing electronics. Beginning in FY 2024, this program is funded in PE 0602716E, Project ELT-02.	8.209	-	-
Accomplishments/Planned Programs Subtotals	105.209	120.837	88.921

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

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COST ($ in Millions)	Prior Years	FY 2023	FY 2024	FY 2025 Base	FY 2025 OCO	FY 2025 Total	FY 2026	FY 2027	FY 2028	FY 2029	Cost To Complete	Total Cost
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	422.673	451.825	484.344	-	484.344	420.585	410.741	437.219	442.938	-	-

A. Mission Description and Budget Item Justification

The Beyond Scaling Technology project pursues electronics performance advancements that exploit new concepts in circuit specialization and three-dimensional heterogeneous integration (3DHI) by the optimization of materials, devices, architectures, and designs to achieve specific circuit function at high performance. Because electronics advancements must simultaneously make progress in performance and secure the foundation on which our microelectronics infrastructure relies, this envisioned specialization will require incorporation of security safeguards and advancing manufacturing tools and process automation. Accordingly, programs within the Beyond Scaling Technology project will reduce barriers to making specialized circuits in today's silicon hardware and 3DHI by improving producibility. This will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized microelectronics, particularly for operation in extreme environments. Programs also explore alternatives to traditional circuit architectures, for instance by exploiting 3DHI to optimize electronic devices and by incorporating novel materials and new techniques for securing DoD and commercial data and hardware.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
Title: Low Temperature Logic Technology (LTLT)	22.000	12.985	10.000
Description: The Low Temperature Logic Technology (LTLT) program is exploiting the unique device and material performance characteristics of state-of-the-art silicon transistors at cryogenic temperatures. Current silicon transistors are performance and power limited when operating at room temperature or higher. This program mitigates these limitations through modifying the design of existing silicon transistors to optimize their performance at cryogenic temperatures. These devices will be compatible with current complementary metal-oxide-semiconductor (CMOS) fabrication process flows and will offer significant increases in performance and power efficiency over room temperature devices. Basic research for this program is funded within PE 0601101E, Project ES-02.			
FY 2024 Plans: - Improve low-temperature device characteristics to enhance performance. - Demonstrate the performance/power improvement of the LTLT devices. - Demonstrate the performance/power improvement of a central processing unit with large on-chip static random access memory.			
FY 2025 Plans: - Further improve the performance/power of the LTLT devices. - Demonstrate the performance/power improvement of a larger scale central processing unit operating at low temperature.			
FY 2024 to FY 2025 Increase/Decrease Statement:			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
The FY 2025 decrease reflects the move from development and demonstration of the devices to optimization.			
Title: COmpact Front-end Filters at the ElEment-level (COFFEE)	14.000	14.000	14.000
Description: The COmpact Front-end Filters at the ElEment-level (COFFEE) program is developing and demonstrating compact, high frequency radio frequency (RF) filter technology without compromising performance, specifically low insertion loss and high-power handling. The new filtering technology will enable interference rejection capability, efficient spectral management, and coexistence with commercial 5G applications. It is projected that COFFEE filter technology will enhance the resilience of military microwave and mm-wave radar and communication systems for DoD spectral dominance into the future. For commercial applications, COFFEE will result in more efficient use of mm-wave frequency allocations for 5G networks. ***FY 2024 Plans:*** - Integrate the resonators into compact, low insertion loss filters demonstrated at microwave frequencies. - Construct filters with high power handling and, as required, integrable tuning. ***FY 2025 Plans:*** - Achieve repeatable manufacturability of high-performance filters with low device-to-device variability. - Integrate the low insertion loss filters into filter tiles with supporting architecture. - Demonstrate capabilities of filter tiles under operationally relevant conditions.			
Title: ELectronics for G-band ARrays (ELGAR)	18.000	19.000	11.000
Description: The ELectronics for G-band ARrays (ELGAR) program is developing the integration technologies needed to create compact, high-performance G-band (220 GHz) array front-end electronics to enable phased array antenna systems for DoD communications and sensing. ELGAR will address the key technical challenges that prevent III-V electronics from realizing high-performance G-band arrays, namely achieving efficient, compact G-band III-V monolithic microwave/millimeter wave integrated circuit power amplifiers (MMIC PAs) with high output power density, and achieving low loss off-chip interconnects between adjacent G-band array components. In particular, ELGAR will develop III-V compatible, silicon-like fabrication and integration approaches to enable compact, high power density, high efficiency G-band MMICs and arrays. The technologies developed will support applications including high data rate communications in size, weight, and power-constrained platforms. ***FY 2024 Plans:*** - Further improve the efficiency and output power of compact G-band III-V MMIC PAs that use the silicon-like multilayer interconnects. - Further reduce the power loss of array-level interconnects for integration of G-band PAs with other array components. - Design and fabricate circularly-polarized, medium-power transmit array test articles.			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Design and fabricate circularly-polarized, low-noise receive array test articles. ***FY 2025 Plans:*** - Further improve the efficiency and output power of compact G-band III-V MMIC PAs that use the silicon-like multilayer interconnects. - Further reduce the power loss of array-level interconnects for integration of G-band PAs with other array components. - Characterize circularly-polarized, medium-power transmit array test articles; design circularly-polarized, high-power transmit array test articles. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from initial design to fabrication and characterization of components.			
Title: Quantum Inspired Classical Computing (QuICC) ***Description:*** The Quantum Inspired Classical Computing (QuICC) program will implement quantum-inspired algorithms using classical dynamic systems in novel computing architectures for the efficient solving of complex optimization problems. Currently, too much computational energy is required to solve mission-scale optimization problems leading to sub-optimal solutions and excessive computation times. This program will create frameworks for analyzing the computational advantage provided by quantum-inspired algorithms and perform the hardware and algorithm co-design needed to reduce the required energy to optimally solve mission-scale problems. ***FY 2024 Plans:*** - Initiate development of analog subsystems for quantum-inspired solvers. - Perform initial hardware performance model development. - Demonstrate co-design framework for digital resource estimation. - Develop systematic methodologies for predictive benchmarks. ***FY 2025 Plans:*** - Demonstrate small-scale analog subsystem hardware and validate initial hardware performance models. - Demonstrate digital resource estimation in the co-design framework and initial predictive benchmarking techniques. - Implement and optimize solver algorithms to increase the accuracy of the framework estimates. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from algorithm and hardware design to subsystem development and design.	17.000	15.000	13.000
Title: Massive Cross Correlation (MAX) ***Description:*** The Massive Cross Correlation (MAX) program aims to develop a scalable wideband correlator that can simultaneously achieve the state-of-the-art dynamic range of a digital correlator with the power efficiency enabled by analog	18.000	19.000	13.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
electronics. Correlators are the core signal processing component used in critical DoD applications such as spread spectrum communications, passive coherent location, and synthetic aperture radar. Current correlator implementations use field-programmable gate arrays and general-purpose graphics processing units requiring thousands of watts of power and racks of supporting computer equipment for today's low frequency, low bandwidth applications, which creates challenges for their use in power-constrained platforms and in applications that require high frequency, high bandwidth solutions. The MAX program will leverage advances in analog signal processing and state-of-the-art fin field-effect transistor (FinFET) semiconductor processes to overcome these challenges. ***FY 2024 Plans:*** - Critical design review of analog correlators meeting high efficiency in simulation. - Fabricate initial designs of scalable, wideband analog correlators achieving high efficiency in a laboratory test environment. - Independent verification and validation of correlators meeting program metrics with government-furnished waveforms. ***FY 2025 Plans:*** - Implement proof-of-concept designs showing program efficiency goals at program dynamic range requirements meeting initial bandwidth metrics. - Critical design review of analog correlators meeting intrinsic hardware dynamic range in simulation. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from design completion to the start of device fabrication.			
Title: Robust Electronics for Radiative Environments (RE2)	4.000	7.000	8.000
Description: The Robust Electronics for Radiative Environments (RE2) program is developing advanced radiation-hardened (rad-hard) nonvolatile memories to meet the demands of emerging missions. Current rad-hard memories are many generations behind state-of-the-art commercial electronics and cannot meet the needs of future systems. In order to address these needs, RE2 will work to deliver high-performance memories for space and strategic systems. ***FY 2024 Plans:*** - Initiate design evaluation of candidate rad-hard and rad-tolerant processor and memory architectures. - Evaluate results of trade study and design evaluation to guide approaches to hardening memories to strategic levels while achieving key latency and density goals. - Initiate first cycle of design, fabrication, packaging and assembly, and test. ***FY 2025 Plans:*** - Execute first design review to evaluate architecture and design of first memory arrays. - Complete first cycle of design, fabrication, packaging and assembly, and test.			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Collect and analyze first data on radiation response and map the result into anticipated mission profiles. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from initial design to design finalization and fabrication.			
Title: H6 ***Description:*** The H6 program, building on technology developed in the Lasers for Universal Microscale Optical Systems (LUMOS) program (budgeted in this PE and Project), is developing the first tactical-grade clock. Tactical-grade clocks are ultra-small, low power, fieldable and can maintain the timing needed for DoD-relevant applications in challenging environments. Precise timing in a tactical package will decouple operations from GPS dependence, overcoming a significant operational vulnerability for the warfighter. Precise tactical-grade clocks from H6 will enable increased signal assurance and pervasive communications security in high-jamming regions. Additionally, H6 will enable real-time, physical monitoring and tracking of warfighters and special forces and will play a critical role in search and rescue through the ability to maintain precise time over a long mission duration without having to re-establish external communications. ***FY 2024 Plans:*** - Initiate construction of tactical-grade clock components. - Demonstrate temperature-insensitive operation in realistic environments. - Develop clock components towards miniaturization of the final system. ***FY 2025 Plans:*** - Develop hypotheses for long-term clock aging. - Demonstrate preliminary aging reduction techniques. - Initiate construction of miniaturized clock. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from initial design to initiating construction of tactical-grade clock components.	12.000	15.000	9.000
Title: Technologies for Heat Removal in Electronics At the Device Scale (THREADS) ***Description:*** The Technologies for Heat Removal in Electronics At the Device Scale (THREADS) program is developing technologies to overcome transistor thermal limits to realize robust, high power density transistors that operate near their fundamental electronic limit of radio-frequency (RF) output power. DoD's RF transmitters increasingly use high-power gallium nitride (GaN) wide bandgap (WBG) transistors, which provide a 5X improvement in RF power output compared to the legacy gallium arsenide (GaAs) technology. Achieving high RF power output while maintaining a transistor operating temperature below the nominal maximum reliable operation temperature faces two challenges. The first challenge is reducing thermal resistance within the device. This will be achieved by leveraging recent advances epitaxial growth processes and phonon bridges to reduce	14.000	26.000	15.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
semiconductor material thermal resistance. The second challenge is more efficiently moving heat away from the transistor hot spots. This will be achieved through novel transistor topologies and by leveraging recent advances in the integration of 2D and 3D cooling structures and high thermal conductivity materials, such as diamond, into the transistor. THREADS will demonstrate high efficiency X-band transistors and power amplifier (PA) test vehicles with an output power density of 16X higher than production GaN amplifiers. THREADS technology will enable increased range for radar, communications, and electronic warfare systems. ***FY 2024 Plans:*** - Finalize initial concepts for the reduction of transistor thermal resistance. - Fabricate thermal resistance test structures and measure a 2.5X reduction in thermal resistance. - Finalize preliminary concepts for robust RF PAs with increased output power density. - Fabricate transistors and PAs and measure a 5X increase in output power density. ***FY 2025 Plans:*** - Refine concepts for the reduction of transistor thermal resistance. - Design and fabricate thermal resistance test structures with a 5X reduction in thermal resistance. - Refine concepts for robust RF PAs with increased output power density. - Design and fabricate transistors and PAs with a 10X increase in output power density. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects a shift from initial development to design and fabrication.			
Title: Minitherms3D ***Description:*** Minitherms3D is developing thermal management solutions for the three-dimensional heterogeneous integration (3DHI) of microelectronics to accelerate the growth of compact, high-performance microsystems. 3DHI microsystems are enabling technologies for phased array systems and dense computing for artificial intelligence and machine learning applications. Minitherms3D will reduce the size, weight and power (SWaP) of high-performance 3DHI microsystems by developing novel methods to remove heat from within the 3D stack, transmit it to the outer boundaries of the stack, and reject it to outside the ambient environment. ***FY 2024 Plans:*** - Develop in-tier heat removal solutions. - Begin development of efficient thermal link to heat rejection components. - Begin development of low-SWaP thermal rejection components. ***FY 2025 Plans:*** - Provide a three-tier test vehicle to demonstrate improved thermal management capabilities.	9.341	18.000	18.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Refine thermal performance of developed solutions for both within stack and outside stack technical challenges. - Begin development of five-tier stack test vehicle to demonstrate improved thermal management capabilities.			
Title: Space Power Conversion Electronics (SPCE) ***Description:*** The Space Power Conversion Electronics (SPCE) program is developing highly-efficient, radiation-tolerant point of load (POL) converters for low-earth-orbit satellites. In today's space power systems, POL converters derate their operating voltage to maintain radiation tolerance, resulting in decreased efficiency and limiting the satellite's available power, capabilities, and battery lifetime. To address this deficiency, SPCE will develop high-performance, radiation-tolerant high voltage switches by exploiting advanced wide-bandgap semiconductor advanced material synthesis, novel device architectures, and 3D heterogeneous integration technology. ***FY 2024 Plans:*** - Complete analysis of candidate wide-bandgap material systems for radiation-tolerant, high-voltage transistors with increased switching performance. - Complete initial simulations of expected switching performance of advanced radiation-tolerant, high-voltage transistors enabled by wide-bandgap materials. - Perform design of high-performance radiation-tolerant, high-voltage switches enabled by wide-bandgap semiconductor transistors. ***FY 2025 Plans:*** - Optimize design and fabrication of radiation-tolerant, high-voltage transistors. - Demonstrate device integration technologies which enables high-efficiency, high-energy-density POL converters. - Perform initial characterization of the integrated, high-efficiency, high-energy-density POL converters.	12.000	18.000	18.000
Title: Faithful Integration Reverse-engineering and Emulation (FIRE) ***Description:*** The Faithful Integration Reverse-engineering and Emulation (FIRE) program will develop tools to find and patch vulnerabilities within cyber-physical systems. A cyber-physical system operates in the physical world using hardware sensors to perceive the analog environment, digital software for processing, and actuators to interact with the environment. Cyber-physical vulnerabilities arise from the composition of hardware, software, and physical components where each component may not be vulnerable in-and-of itself. FIRE will develop novel modeling and simulation techniques to help expedite finding and patching vulnerabilities in cyber-physical systems. ***FY 2024 Plans:*** - Creation of a surrogate cyber-physical test vehicle to demonstrate the tools.	3.000	14.040	24.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Proof-of-concept demonstration of tools on the surrogate cyber-physical test vehicle. ***FY 2025 Plans:*** - Evaluate results of the surrogate cyber-physical test vehicle. - Perform real-world demonstration of the approaches. - Scale the approaches to medium-complexity systems. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects a shift from initial development to proof-of-concept of tools.			
Title: NanoWatt Platforms for Sensing, Analysis, and Computation (NaPSAC) ***Description:*** Efficient, high-speed scientific computing architectures are a ubiquitous requirement for applications including modeling of complex physical systems, advanced device designs, and multiscale computations of dynamical phenomena such as climate models or turbulence. Current state-of-the-art computing systems requires prohibitive amounts of energy and time to perform such calculations. The NanoWatt Platforms for Sensing, Analysis, and Computation (NaPSAC) program aims to develop a novel computational architecture for massively parallel, ultralow power "in-memory" computation. NaPSAC-based computing architectures can potentially yield transformative impact by enabling beyond-state-of-the-art computational speed and accuracy. Applications of immediate relevance to the DoD include simulations of turbulent flows, multiscale electromagnetic simulations of plasma dynamics, advanced semiconductor device design, and the modeling of high-performance materials. ***FY 2024 Plans:*** - Develop computational algorithms to enable efficient computations of complex systems including high performance materials and advanced semiconductor devices. - Finalize nanoresonator-based computing architectures to enable massively parallel hyperspectral computations, optimize material parameters for tunability and precision, and initiate device fabrication. ***FY 2025 Plans:*** - Demonstrate preliminary proof-of-concept test articles of novel nanoresonator-based computing engines for high speed, energy efficient scientific computations. - Perform concept validation and preliminary benchmarking of computing accuracy, speed and power efficiency of nanoresonator computing modules. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects a shift from algorithmic and architecture design to component development and validation.	5.500	14.000	12.000
Title: Optomechanical Thermal Imaging (OpTIm)	5.000	12.300	16.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
Description: Advanced infrared (IR) detectors and thermal imaging systems underpin a vast DoD application space including biochemical detection; infrared Search-and-Track; and terrestrial and space-based Intelligence, Surveillance, and Reconnaissance. Current IR detectors suffer from numerous limitations including poor sensitivity, poor signal bandwidth, or the need for expensive cryogenic cooling. The Optomechanical Thermal Imaging (OpTIm) program will develop a new modality of low size, weight, and power, room temperature IR detectors capable of quantum-level sensitivity, thereby enabling transformative enhancements to DoD capabilities including, but not limited to, night vision, surveillance, multispectral detection, and remote detection of trace industrial pollutants and greenhouse gases. ***FY 2024 Plans:*** - Investigate technical and fundamental performance limits of this modality of infrared (IR) detection. - Execute device simulations and demonstrations of single-pixel test articles of a new modality of infrared detection. - Demonstrate design, simulation, and fabrication of novel detector surface coatings capable of identifying specific chemical or biological signatures in the infrared spectrum. - Develop integrated device designs of scalable IR detector concepts for IR imaging applications. ***FY 2025 Plans:*** - Demonstrate functionality and characterize performance of novel optomechanical IR detector devices. - Initialize fabrication, integration, and characterization of scalable optomechanical IR detectors. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects a shift from component fabrication and demonstration to system integration and demonstration.			
Title: Processor Reconfiguration for Wideband Sensing Systems (PROWESS)	16.732	17.000	16.000
Description: The Processor Reconfiguration for Wideband Sensing Systems (PROWESS) program is developing high-throughput streaming-data processors that change their programming at nanosecond timescales to detect novel radiofrequency (RF) signals. Sensing complex and unanticipated signals across wide RF bandwidths is limited by the computing capacity available at the tactical edge. Today's tactical spectrum sensors rely on field-programmable gate arrays (FPGAs) for low-latency, high-throughput signal processing. Since FPGA reconfiguration time (milliseconds) is much slower than RF signal dynamics (nanoseconds), FPGAs cannot optimize their signal processing in real time as new signals are observed. Recent advances in application-specific processing arrays, real-time task scheduling, and high-bandwidth input/output enable the development of new run-time reconfigurable array (RTRA) processors capable of reprogramming themselves as new signals are received. PROWESS is investigating RTRA processors and receiver integration approaches to enhance the performance of tactical RF sensors in congested spectrum. ***FY 2024 Plans:***			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Develop preliminary concept designs to integrate RTRA processors into complete spectrum sensing systems. - Finalize concept design for RTRA processor test chips. - Conduct design review of RTRA processor test chips and their integration into systems. ***FY 2025 Plans:*** - Develop concept designs to integrate RTRA processors into spectrum sensing testbeds. - Finalize concept design for RTRA processor test chips. - Develop initial compilers and related RTRA programming tools. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from initial concept designs to finalizing concept designs for the test chips and their integration into systems integration.			
Title: Digital RF Battlespace Emulator (DRBE)	20.000	23.500	14.000
Description: The Digital RF Battlespace Emulator (DRBE) program is developing a large-scale, interactive, emulated radio frequency (RF) environment, providing the DoD with the capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. DRBE is leveraging advances in massively multi-core computing hardware and high-bandwidth digital cross-connects to emulate realistic RF environments accounting for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. An electronics architecture supporting the power and latency requirements demanded by these emulation environments does not currently exist. DRBE is pursuing three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment will allow plug-and-play connections for hundreds of RF systems in a battlespace test. Multi-system exercises will then be quickly executed through many different combat scenarios and variations. DRBE is serving to develop concept of operations (CONOPS), inform battle plans, and fine-tune the performance of both individual and large groups of RF systems. Additional development started in 2024 greatly expands the input/output bandwidth of DRBE to support for much larger RF scenarios. ***FY 2024 Plans:*** - Demonstrate real-time RF emulation on computational accelerator chip. - Integrate High-Performance Computer (HPC) with RF interfaces. - Deliver DRBE components to DoD laboratory for integration. ***FY 2025 Plans:*** - Validate real-time HPC performance with a representative DRBE workload. - Develop DRBE HPC prototype with expanded input/output subsystem.			

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Assemble mechanical prototype to support large-scale integrated photonics. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the move from on-chip emulation to real-time HPC validation.			
Title: Next Generation Microelectronics Manufacturing (NGMM)* ***Description:*** *Formerly Next Generation Microelectronics Prototyping - Designs Next Generation Microelectronics Manufacturing (NGMM) creates new software design tools to enable the development of novel three-dimensional heterogeneous integration (3DHI) microsystems that are test articles with the NGMM program. The design tools developed will be validated through design challenges. These design challenges provide the opportunity to explore approaches that will improve and accelerate the adoption of 3DHI standardized chip-to-chip interfaces and package optimization. Leading-edge chip designs will be fabricated, and subsequently integrated into 3DHI designs in multi-project demonstration runs. Additional research related to this effort is funded within PE 0603739E, Project MT-16. ***FY 2024 Plans:*** - Create initial software components and establish baseline processes for multi-user assembly design kit. - Identify and initiate challenge problems for 3DHI microsystems and establish appropriate metrics. - Determine goals for design challenges for standardized 3D chip-to-chip integration practices. - Establish plan for utilizing leading-edge chips (or chiplets) to develop components for novel 3DHI test article designs. ***FY 2025 Plans:*** - Run two design challenges for 3DHI microsystems standardized chip-to-chip integration practices. - Complete two fabrication runs for leading-edge chips as components for novel 3DHI test article designs. - Assess and validate efficacy of initial assembly design kit based upon novel 3DHI test article designs from challenge runs. - Update goals for the next set of design challenges for standardized chip-to-chip integration practices, based on assessment of assembly design kit and the interface standard.	25.000	25.000	25.000
Title: Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI) ***Description:*** Next Generation Microelectronics - Advanced Manufacturing Approaches for three-dimensional heterogeneous integration (3DHI) addresses the unique manufacturing requirements for 3DHI microsystems, including design, fabrication, packaging, assembly, and security. New multi-chip, multi-technology assembly and packaging will advance beyond silicon-centric integration to include integration of radio frequency (RF), photonics, and compound semiconductors. In order to enable this diversity of materials and functions, integration technologies will be enabled by improving thermal management, improving inter-	27.000	4.000	-

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
chip power delivery, and improving the diagnostic capability of these complex microstructures. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2024 Plans:*** - Continue developing multi-chip, multi-technology assembly and packaging techniques consistent with high density interconnects (less than or equal to one-micron pitch). - Develop requirements for a distributed heterogenous processing architecture. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.			
Title: Optimum Processing Technology Inside Memory Arrays (OPTIMA)* ***Description:*** *Previously part of Next Generation Microelectronics - 3DHI The Optimum Processing Technology Inside Memory Arrays (OPTIMA) program aims to create a fast, small, energy-efficient, and adaptable compute-in-memory (CIM) accelerator using approaches compatible with very large-scale integration (VLSI) fabrication. Traditional accelerators based on von Neumann architecture have limitations in terms of computational power efficiency and speed. By demonstrating Multiply Accumulate Macros (MAMs) consisting of a large number of Multiply Compute Elements (MCE) into CIM architectures, these challenges can be overcome, leading to improved performance. The program goal is to showcase high-performance MAMs with innovative signal processing circuitry and architectures, with a focus on optimizing both space and power efficiency. ***FY 2024 Plans:*** - Develop a low-energy, single-transistor footprint MCE with improved energy efficiency and speed. - Optimize the size and footprint of the MCE to enhance compactness and integration capabilities. ***FY 2025 Plans:*** - Further enhance the energy efficiency and speed of the MCEs for improved performance. - Experimentally demonstrate a compact MAM with a high number of MCEs, showcasing scalability and potential for parallel processing. - Evaluate performance of compact MAM with high number of MCEs. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from development of the initial concept to enhancement and demonstration of an optimized device.	13.000	16.000	17.240
Title: Scalable On-Array Processing (SOAP)*	-	10.000	20.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
Description: *Previously part of Next Generation Microelectronics - 3DHI The Scalable On-Array Processing (SOAP) program is designed to achieve scalable algorithms and processing architectures to overcome the inherent digital bottlenecks that severely limit today's wideband operation on arbitrarily large elemental digital phased arrays. SOAP aims to reduce the computational complexity of array processing as a function of element count, from exponential to linear scaling. SOAP also seeks to move the processing from physically separated back-end processors to processors integrated into the array, in order to fully process all the information generated at the element level, with no elemental information loss. To achieve these aims, SOAP will design processors that can be distributed within the array, as close to the elements as possible. These processors should be connected and networked in such a way that the data from any element can be processed by any processor. ***FY 2024 Plans:*** - Development of two data sets for testing and demonstration. - Development of new adaptive array processing algorithms that maintain the performance of traditional algorithms but reduces the number of computational steps and scales more linearly as array size increases. ***FY 2025 Plans:*** - Design of processing elements necessary to move array processing onto the array. - Completion of new adaptive array processing algorithms. - Independent verification and validation of delivered algorithms. - Finalization of design of processing elements necessary to move array processing onto the array. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the program moving from initial design and data set development to design completion and verification.			
Title: Intensity-Squeezed Photonic Integration for Revolutionary Detectors (INSPIRED)* ***Description:*** *Previously part of Next Generation Microelectronics 3DHI The Intensity-Squeezed Photonic Integration for Revolutionary Detectors (INSPIRED) program will develop compact, ultra-low-noise optical detectors. Low-noise detection is vital to all optical science and technology, but the quantum nature of light imposes a fundamental quantum limit on a conventional optical detectors noise performance. Recent experiments have demonstrated that exotic quantum states called squeezed light can be harnessed to overcome the quantum limit, albeit from bench-scale apparatuses that ultimately restrict the application of squeezed-light-enhanced detectors to esoteric applications such as gravitational-wave astronomy. The INSPIRED program will leverage recent advances in chip-scale quantum optics and materials	-	9.000	17.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
to realize optical detector modules operating well below the quantum noise limit in form factors that enable deployment in applications such as biosensing, navigation, and communications. ***FY 2024 Plans:*** - Establish squeezed-light measurement methodology and procedure. - Complete design of chip-scale photonic components that will serve as basis for squeezed light generator. - Complete design of low-loss chip-scale photonic components that will serve as basis for low-loss interferometer circuit. ***FY 2025 Plans:*** - Complete fabrication process development for integrated photonics circuits that can create and manipulate quantum states of light. - Experimentally demonstrate squeezed light generation using chip-scale components. - Experimentally demonstrate components chip-scale low-loss interferometer circuits. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from design completion to fabrication and experimental demonstration.			
Title: Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics ***Description:*** Next Generation Microelectronics - Advanced Manufacturing for Extreme Environment Electronics addresses the design, fabrication, packaging, assembly, and testing of the next generation of microsystems targeted for use in extreme environments: high voltage, high current, high temperature, low temperature, and radiation exposure. New manufacturing methods will be created, with an emphasis on developing techniques to enable high survivability of these microsystems while operating in the extreme environments. This effort will also develop techniques to significantly improve the performance of these unique microsystems. Basic research related to this effort is funded within PE 0601101E, Project ES-02.	43.000	-	-
Title: Macaroni* ***Description:*** *Previously part of Next Generation Microelectronics - Extreme Environment Electronics Measurement and control of the electromagnetic spectrum is a key area of research for the Department of Defense (DoD). Spectrum dominance requires quick and efficient control of electromagnetic radiation from low frequencies to X-rays. In classical antenna theory, the sensitivity-bandwidth product is fundamentally limited by the physical shape and size of the antenna. This performance degrades significantly as the antenna becomes electrically small, that is, the physical size becomes much smaller than the electromagnetic wavelength of operation. The Macaroni program seeks to develop electrically-small receivers and transmitters with performance that exceeds the current state of the art (SoA). Recent advances in quantum sensors, materials science, electromagnetic shielding, laser technology, resonators, cryogenic systems, and vacuum components have pushed	-	20.000	24.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
the SoA in sensing technologies. For transmitters, new insights in active antenna technology, control schemes, methods of impedance matching, and strategies for volume filling present new opportunities. Furthermore, recent efforts in piezoelectrics, magnetoelectrics, high-index materials, and multiferroic materials may be leveraged. ***FY 2024 Plans:*** - Develop theory of electrically-small receiver and transmitter. - Perform design of concept test vehicle for validation of developed theory of electrically-small receiver and transmitter. - Experimentally validate theory of electrically-small receivers and transmitters. ***FY 2025 Plans:*** - Finalize design of concept test vehicle for validation of developed theory of electrically-small receiver and transmitter. - Demonstrate electrically-small receiver performance meeting program metrics in a laboratory environment. - Demonstrate electrically-small transmitter performance meeting program metrics in a laboratory environment. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from concept validation to demonstration of the electrically-small receiver and transmitter.			
Title: High Operational Temperature Sensors (HOTS)* ***Description:*** *Previously part of Next Generation Microelectronics - Extreme Environment Electronics The High Operational Temperature Sensors (HOTS) program seeks to develop high-temperature sensor microelectronics that can operate at extreme temperatures (800°C). The program is looking for innovative approaches that enable revolutionary advances in science and technology for integrated sensor module development. The current state of the art in high-temperature sensors is limited by the performance of transducers and signal-conditioning microelectronics. The HOTS program aims to overcome these limitations by developing new transducers and signal-conditioning microelectronics that can operate at high temperatures while still meeting the performance goals. ***FY 2024 Plans:*** - Perform multi-physics simulation and analysis of sensor performance. - Design and fabricate discrete high operational temperature transistors. - Design and fabricate discrete high operational temperature pressure transducers. ***FY 2025 Plans:*** - Verify and validate performance of high operational temperature transistors and transducers. - Design full circuits and simulate performance of the integrated sensor system based on measured component results.	-	12.000	22.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Integrate the discrete transducer and transistors to form high operational temperature sensor modules. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from design and fabrication of the discrete high temperature components to the design and integration of the components into the complex module.			
Title: Advanced Sources for Single-event Effect Radiation Testing (ASSERT)* ***Description:*** *Previously part of Next Generation Microelectronics - Extreme Environment Electronics 3D heterogeneously integrated (3DHI) microelectronics will be a key driver of the next wave in electronics performance. However, the nation's current single-event effect (SEE) radiation testing infrastructure lacks the ability to analyze and qualify emerging 3D devices for operation in high radiation environments. To fill this gap, the Advanced Sources for Single-event Effect Radiation Testing (ASSERT) program will develop new source technologies to create charge tracks with deep penetration depths for SEE qualification of 3DHI topologies and packaging, provide the means to selectively probe device topologies to inform engineering design, and generate data to validate developing models and codes and to provide training sets for optimization. ***FY 2024 Plans:*** - Commence development of radiation source design, verified through 3D simulation. - Develop predictive single-event effect testing methodology. ***FY 2025 Plans:*** - Finalize radiation source designs and initiate fabrication, procurement, and laboratory preparation. - Conduct proof-of-concept experiments to validate the ability of novel sources to reproduce single-event effect responses in representative electronic devices. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from initial concept design and development to design finalization and initiating fabrication of the sources.	-	15.000	17.000
Title: Next Generation Microelectronics - Advanced Manufacturing Tools ***Description:*** Next Generation Microelectronics - Advanced Manufacturing Tools addresses the development of new manufacturing tools for the design, fabrication, packaging, assembly, testing, and digital emulation of the next generation of advanced microsystems. Specifically, these advanced microsystems include three-dimensional heterogeneous integration (3DHI) and designs targeted for use in extreme environments such as high voltage, high current, high temperature, low temperature, and radiation exposure. New tools to improve manufacturing and testing will be designed, built, and characterized. These tools will enable cost-effective on-shoring of automated processes for packaging, assembly, and testing of advanced microsystems.	42.000	16.200	-

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
The software and hardware tools addressed in this program will advance integration techniques beyond current commercial capabilities to support national security needs. Design, verification, and security for 3DHI will be supported by coordinated investments that couple manufacturing and electronic design automation. Basic research related to this effort is funded within PE 0601101E, Project ES-02. ***FY 2024 Plans:*** - Develop tools for design, simulation, testing, and cost-optimization of 3DHI components and packages. - Continue developing multi-domain models for virtual prototyping of 3DHI components and packages. - Implement methodologies for design optimization for multi-chip, multi-technology packaging and assembly techniques consistent with high density interconnects. - Evaluate methods for implementing security features into 3DHI electronics and their associated interconnects. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.			
Title: Quantum Augmented Network (QuANET)* ***Description:*** *Previously part of Next Generation Microelectronics - Advanced Manufacturing Tools The Quantum Augmented Network (QuANET) program is developing quantum-augmented networks that add security and covertness properties inherent in quantum communications to classical, non-quantum, network infrastructures. Today, digital communication paradigms use a network stack that consists of a layered set of software protocols. The higher layers are closer to applications on computers and servers, while the bottom layers are closer to the physical channel implementation. State-of-the-art networks commonly rely on security at the top layers of the stack, assuming that this security also mitigates attacks on lower layers. Unfortunately, advanced persistent threat (APT) attacks are defeating many existing state-of-the-art security capabilities. The QuANET program seeks to augment existing software infrastructure and network protocols with quantum properties to mitigate these attack vectors. QuANET will develop the hardware, protocols, and software tools to enable quantum communications over classical, non-quantum, network infrastructures. QuANET algorithms, protocols, and software infrastructure will facilitate multiplexing quantum photons into classical optical streams, enabling the use of quantum timing and sensing information atop classical information. Integrating quantum photons into classical optical data streams will bring the event detection, node verification, and high-fidelity timing mechanisms of quantum communications into existing classical networks. If successful, QuANET will enable quantum-augmented networking that provides greater security than current classical networks. ***FY 2024 Plans:*** - Design specifications for a quantum network interface card (qNIC) that has the ability to send and receive quantum information, as well as sending and receiving quantum timing and sensing information.	8.000	12.000	19.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Develop initial algorithms, protocols, and software infrastructure for hybrid quantum-classical optical data streams, enabling the use of quantum timing and sensing information in synchrony with classical information. - Develop algorithms, protocols, and software infrastructure for integrating quantum secure communication links into a classical network infrastructure running Internet protocols. ***FY 2025 Plans:*** - Build a test article for quantum augmented network, utilizing fabricated qNICs and developed quantum communication algorithms, protocols, and software infrastructure. - Demonstrate initial capabilities of a test article for a quantum augmented network to send and receive quantum information. - Test and evaluate initial security capabilities of a test article for a quantum augmented network to detect and mitigate network attacks such as rogue or counterfeit nodes, unwanted listeners, route injections, and timing attacks. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects continued development of techniques to integrate quantum information in classical communication networks and expanded work to assess the capabilities of a test article for a quantum augmented network.			
Title: Continuous-correctness On Opaque Processors (COOP)* ***Description:*** *Previously part of Next Generation Microelectronics - Advanced Manufacturing Tools The Continuous-correctness On Opaque Processors (COOP) program will validate that continuous correctness of software enables adoption of the latest processors with low overhead. Instead of creating new threat-specific signatures to detect the threats, COOP detects the physical manifestations of software errors and continuously corrects the errors with mathematical guarantees. ***FY 2024 Plans:*** - Research hardware/software approaches for creating unique software signatures. - Research hardware/software approaches to detect and understand software signatures. ***FY 2025 Plans:*** - Develop proof-of-concept that errors detected can be corrected within a relevant timeframe. - Develop techniques to minimize overhead during error detection. - Validate proof-of-concept solutions to correlate signatures to software errors within a relevant timeframe. ***FY 2024 to FY 2025 Increase/Decrease Statement:***	-	5.000	20.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
The FY 2025 increase reflects the move from researching hardware and software to developing and validating proof-of-concept solutions.			
Title: Additive Manufacturing of MicrosystEms (AMME)* ***Description:*** *Previously part of Next Generation Microelectronics - Advanced Manufacturing Tools The Additive Manufacturing of MicrosystEms (AMME) program will revolutionize microsystem manufacturing by leveraging selective material synthesis and 3D patterning to enable a new class of microsystems. Additive Manufacturing (AM) has enabled complex single-material geometries that were previously impossible to produce via traditional manufacturing methods. However, microsystem manufacturing has not exploited AM due to fundamental limits of material quality, resolution, and print throughput. The AMME program will use selective material synthesis to create high-quality material precursors that permit simultaneous printing of conductors and insulators with high-resolution and high-volume throughput. Additionally, AMME will focus on commercialization of this technology such that the Department of Defense and intelligence community can quickly adopt the productized system to fabricate novel microsystems. ***FY 2024 Plans:*** - Initiate multi-material precursor development. - Initiate 3D synthesis modeling and analysis. ***FY 2025 Plans:*** - Develop 3D synthesis modeling and analysis. - Develop multi-material precursor. - Demonstrate simultaneous multi-material synthesis. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects the move from initial development to development and demonstration.	-	13.800	25.000
Title: Quantum Apertures (QA) ***Description:*** The Quantum Apertures (QA) program is developing novel radio receiver and aperture systems using quantum sensors as the receiving elements. These receiver systems will be portable, programmable over a very large frequency range, and more sensitive than classical systems at similar size and temperature. This will be achieved by exploiting quantum-based receiving elements composed of atomic vapor cells in highly-excited Rydberg states that have programmable sensitivity over a large range of frequencies and amplitudes. The program will require quantum engineering and traditional electro-mechanical systems engineering to overcome technical and application challenges that impede rapid adoption of a quantum aperture receiver by the defense industrial base. The receiver system's enhanced capabilities will be leveraged in this program to develop novel	-	12.000	7.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
waveforms while also being compatible with constraints imposed by real-world defense applications. The final receiver system will comprise a phase-sensitive array of quantum receiving elements, lasers to program the sensor and read out radio signals, and processing electronics. Initial funding for this program is funded in PE 0602716E, Project ELT-01. ***FY 2024 Plans:*** - Design an architecture for quantum aperture sensors in multiple-element arrays. - Demonstrate navigational waveform reception by quantum aperture. - Conduct quantum aperture sensor testing within a DoD-cleared facility. ***FY 2025 Plans:*** - Develop a specific test article for quantum apertures according to transition partner needs. - Demonstrate functional arrays of test articles for quantum apertures. - Receive operationally-relevant waveforms using quantum apertures. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects the shift from development of a specific architecture and system design to demonstration and testing.			
Title: Intelligent Generation of Tools for Security (INGOTS) ***Description:*** The Intelligent Generation of Tools for Security (INGOTS) program is developing techniques to identify and triage chainable vulnerabilities within widely used secure computing platforms and assess exploitability. Today, sophisticated cyber attacks link multiple vulnerabilities together into exploit chains that bypass software and hardware security measures to compromise critical, high-value systems. Accurately understanding risk is critical for both developers and defenders within cyberspace, but the metrics currently in use do not account for the multiple factors which differentiate an innocuous software flaw from a chainable vulnerability. INGOTS is developing semi-automated tools and techniques to characterize and measure the interdependent exploitability of vulnerabilities and will pioneer a new vulnerability severity metrology that characterizes and measures interdependent exploitability for the next generation of security vulnerabilities. INGOTS will also develop datasets capturing artifacts and features of vulnerabilities and exploits to further drive program analysis and AI approaches for rapid risk assessment. With the INGOTS vulnerability measurement pipeline, developers and defenders will improve software and hardware resiliency of pervasive commercial systems by rapidly identifying and prioritizing their most dangerous flaws. The INGOTS program is also funded in PE 0602303E, Project IT-03. ***FY 2024 Plans:*** - Formulate approaches to characterize and measure the interdependent exploitability of vulnerabilities as the basis for a new vulnerability severity metrology.	-	11.000	29.000

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
- Develop techniques to accurately quantify the severity of a vulnerability chain in software systems that have state-of-the-art defenses. - Explore and prioritize demonstrations of severity analysis on vulnerabilities of interest to transition partners. ***FY 2025 Plans:*** - Develop and demonstrate techniques to characterize and measure the interdependent exploitability of vulnerabilities in complex software systems. - Quantify the accuracy of vulnerability severity assessment for complex software systems that have state-of-the-art defenses. - Demonstrate the capability to identify and prioritize vulnerabilities in software of interest to transition partners. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects continued development of techniques to quantify the severity of individual and chained vulnerabilities and expanded work to assess the accuracy and utility of the techniques.			
Title: Supply Chain & Logistics in Electronic Technology ***Description:*** DARPA's Supply Chain and Logistics in Electronic Technology thrust will develop technologies to help ensure a robust and secure domestic supply chain for advanced microsystems. This includes the design, assembly, packaging, and testing technologies for advanced microsystems that exploits and extends beyond commercial activities. It takes advantage of innovations in photonics, optics, materials, and advanced three dimensional heterogeneous integration (3DHI) for the highest performance electronics technology. In doing so, the goal is to revolutionize domestic industry and enable safe and reliable access to disruptive technology. ***FY 2025 Plans:*** - Perform initial studies of automating the design of complex, 3D circuits to include advanced artificial intelligence / machine learning techniques. - Develop methodology for the built-in self-test of devices and circuits within 3DHI microsystems. - Develop novel processes for the heterogeneous integration of diverse materials at the atomic scale. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects thrust initiation.	-	-	20.600
Title: Warfighting Performance in Electronic Technology ***Description:*** DARPA's Warfighting Performance in Electronic Technology thrust seeks to develop technologies that will drive the next generation of electronic systems for the warfighter. This includes developing advanced active and passive sensor systems that will integrate efficient processing with exquisite detection. It also includes adaptive technologies with embedded machine	-	-	10.504

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
learning and cognitive behaviors that are then incorporated into electronic systems. These technologies will enable sensor systems with unprecedented performance and efficiency while minimizing size, weight, and power (SWaP). ***FY 2025 Plans:*** - Perform study of capabilities of current passive sensors and on techniques to improve their performance. - Perform initial design of sensor with integrated processing in an edge-relevant form factor. - Evaluate use of artificial intelligence / machine learning for use in adaptive sensors and systems. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 increase reflects thrust initiation.			
Title: Automatic Implementation of Secure Silicon (AISS) ***Description:*** The Automatic Implementation of Secure Silicon (AISS) program is enabling a design tool and Intellectual Property (IP) ecosystem where security is pervasive and can be incorporated naturally into chip design with minimal effort and expense. The program will enable rapid evaluation of architectural alternatives in platform integration where security can be optimized relative to the conventional design economic measure of power, area, and speed. The program will advance multi-level provenance and integrity validation techniques for design through improvement of current methods or invention of novel technical approaches, and will demonstrate new capabilities in the context of reduced instruction set computing (RISC) architectures or computer processors. AISS will protect advanced chips from known attack strategies by incorporating security into a highly automated system aimed at reducing design time while maximizing exploration of architectural alternatives. As a result, DoD applications will benefit from more secure chips becoming pervasive whether procured commercially or designed specifically for defense systems. ***FY 2024 Plans:*** - Develop design automation and optimization recommendations as a means to override/interact with defaults. - Simplify automation flow in consideration of third-party security techniques and cryptographic IP. - Develop two forms of documentation; one that will serve as a user guide, and one for the purposes of interfacing to AISS. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.	21.700	6.000	-
Title: Lasers for Universal Microscale Optical Systems (LUMOS) ***Description:*** The Lasers for Universal Microscale Optical Systems (LUMOS) program is integrating high-performance light sources into silicon integrated photonics enabling compact, rugged, high-performance systems for positioning, navigation, communications, 3D imaging, and quantum technologies. Silicon photonics today enables microscale integration of complex optical systems, but the platforms lack of optical gain precludes the creation of lasers and amplifiers through foundry processes.	18.000	10.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
LUMOS will deliver the missing capability to provide compact optical sources at wavelengths from the visible to the infrared, and will create a universal manufacturing platform that builds upon the current photonics ecosystem. To drive innovation and maintain DoD access to leading-edge deployable photonic solutions, LUMOS will establish a technology pathway connecting government, academic, commercial, and defense users of integrated photonics, and will provide multi-project wafer runs through an open-access foundry. ***FY 2024 Plans:*** - Incorporate device improvements and higher-complexity external designs in a second laser-enabled foundry run. - Construct system demonstrators utilizing high-power and visible-wavelength integrated platforms. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.			
Title: Data Privacy in Virtual Environments (DPRIVE) ***Description:*** The Data Privacy in Virtual Environments (DPRIVE) program will make secure processing on untrusted hardware feasible through the development of new hardware accelerators that allow the data to remain encrypted at all times, even during processing. The hardware developed under DPRIVE will accelerate several fully homomorphic encryption (FHE) schemes more than three orders of magnitude over commodity processors. The program plans to provide strong privacy protections at the tactical edge with no more than one order of magnitude penalty in computation time, and to enable very strong privacy at the enterprise level with no more than three orders of magnitude penalty compared to the corresponding unencrypted processing on commodity processors. The program will enable the development and deployment of these hardware accelerators to edge computing devices where power and time are a premium, as well as to enterprise computing facilities where the amount and sensitivity of the data requires increased protection. ***FY 2024 Plans:*** - Fabricate mother board to accommodate the homomorphic encryption coprocessor and appropriate interfaces to a central processing unit (CPU). - Submit tape-out of final chip designs to one or more foundries. - Package and test the DPRIVE coprocessor microcircuit for basic operations. - Execute pre-determined workloads and benchmarks to establish performance, speed, and accuracy of the coprocessor's homomorphic encryption capabilities. ***FY 2024 to FY 2025 Increase/Decrease Statement:*** The FY 2025 decrease reflects program completion.	16.000	10.000	-
Title: Guaranteed Architectures for Physical Security (GAPS)	12.000	-	-

Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency		Date: March 2024
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2023	FY 2024	FY 2025
Description: The Guaranteed Architectures for Physical Security (GAPS) program developed hardware security and software architectures with provable security interfaces. These interfaces physically isolated high-risk transactions during both system design and system build, and will ensure that such protections are enforced at run-time. GAPS reduced the inherent complexity through the development of hardware and software that is open, extendible, and compatible with size, weight, and power-constrained environments to enable security across DoD and commercial systems. The program substantially lowered the barrier to safely enabling high-risk transactions, thus allowing for fast computer-to-computer transactions, physical spatial isolation reducing the need for unreliable software partitioning solutions, and more complex missions without putting sensitive data at risk. Basic research for this program is funded within PE 0601101E, Project ES-02.			
Title: Structured Array Hardware for Automatically Realized Applications (SAHARA) ***Description:*** The Structured Array Hardware for Automatically Realized Applications (SAHARA) program developed technology for the secure development of custom chips for defense systems. Current DoD systems often employ field-programmable gate array (FPGAs), whose flexibility advantages are offset by lower performance. Structured application specific integrated circuits (ASICs) deliver significantly higher performance and lower power consumption, which makes them an efficient and effective alternative to FPGAs for defense electronic systems. Manually converting FPGAs to structured ASICs, however, is a complex, lengthy, and costly process. SAHARA developed automated technologies to reduce design time, optimize performance, and minimize the power dissipated by the secure, structured ASIC.	6.400	-	-
Accomplishments/Planned Programs Subtotals	422.673	451.825	484.344

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A