| Exhibit R-2, RDT&E Budget Item Justification: PB 2025 Defense Advanced Research Projects Agency | Date: March 2024 |
|---|---|
| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 3: *Advanced Technology Development (ATD)* | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* |

| COST ($ in Millions) | Prior Years | FY 2023 | FY 2024 | FY 2025 Base | FY 2025 OCO | FY 2025 Total | FY 2026 | FY 2027 | FY 2028 | FY 2029 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | - | 243.110 | 254.033 | 257.844 | - | 257.844 | 268.650 | 273.822 | 255.088 | 261.116 | - | - |
| MT-15: *MIXED TECHNOLOGY INTEGRATION* | - | 33.793 | 47.847 | 24.643 | - | 24.643 | 30.024 | 31.673 | 33.487 | 34.679 | - | - |
| MT-16: *BEYOND SCALING ADVANCED TECHNOLOGIES* | - | 209.317 | 206.186 | 233.201 | - | 233.201 | 238.626 | 242.149 | 221.601 | 226.437 | - | - |

**A. Mission Description and Budget Item Justification**

The efforts described in this Program Element (PE) address the Advanced Technology Development associated with the Advanced Electronics Technologies Program that seeks to design and demonstrate state-of-the-art manufacturing and processing technologies for the production of various electronics and microelectronic devices, sensor systems, integrated photonic-electronic components that have military applications and potential commercial utility. Introduction of advanced product design capability and flexible, scalable manufacturing techniques will enable the commercial sector to rapidly and cost-effectively satisfy military requirements.

The Mixed Technology Integration project funds the advanced development and demonstration of selected basic and applied electronics research programs. Examples of technologies with funded development and demonstration activities include, but are not limited to: reducing the size, weight, and power (SWaP) of components for laser weapon systems that will protect airborne platforms from emerging surface-to-air missiles; integrated photonic-electronic components for positioning, navigation and timing in GPS-denied environments; flexible, software-defined cameras that enable real-time image analysis of complex scenes to provide more actionable information; and optical communications systems that rely on no moving parts enabling their use on SWaP-restricted platforms. Funding under this project is intended to advance transitioning novel technologies to use, providing advanced components compatible with mid-term and other future warfighting requirements.

The Beyond Scaling Advanced Technologies Project supports activities to enable and accelerate the transition of disruptive microelectronics advancement, including those developed under the Beyond Scaling Sciences (ES-02) and Beyond Scaling Technology (ELT-02) projects. Funding under this project will include developing new technologies and capabilities in commercial settings, establishing access to these new processes and to commercial state-of-the-art foundries, enabling prototyping, developing manufacturable processes for three-dimensional heterogeneous integration (including integrated photonics), advancing new architectures and integration technologies for advanced field programmable gate arrays (FPGAs), and innovating back end of line technologies for wide bandgap semiconductors.

| Exhibit R-2, RDT&E Budget Item Justification: PB 2025 Defense Advanced Research Projects Agency | Date: March 2024 |
|---|---|
| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide I* BA 3: *Advanced Technology Development (ATD)* | **R-1 Program Element (Number/Name)**<br>PE 0603739E *I ADVANCED ELECTRONICS TECHNOLOGIES* |

| B. Program Change Summary ($ in Millions) | FY 2023 | FY 2024 | FY 2025 Base | FY 2025 OCO | FY 2025 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 250.917 | 254.033 | 248.628 | - | 248.628 |
| Current President's Budget | 243.110 | 254.033 | 257.844 | - | 257.844 |
| Total Adjustments | -7.807 | 0.000 | 9.216 | - | 9.216 |
| • Congressional General Reductions | 0.000 | 0.000 | | | |
| • Congressional Directed Reductions | 0.000 | 0.000 | | | |
| • Congressional Rescissions | 0.000 | 0.000 | | | |
| • Congressional Adds | 0.000 | 0.000 | | | |
| • Congressional Directed Transfers | 0.000 | 0.000 | | | |
| • Reprogrammings | 0.272 | 0.000 | | | |
| • SBIR/STTR Transfer | -8.079 | 0.000 | | | |
| • TotalOtherAdjustments | - | - | 9.216 | - | 9.216 |

**Change Summary Explanation**

FY 2023: Decrease reflects SBIR/STTR transfer offset by reprogrammings.

FY 2024: N/A

FY 2025: Increase reflects minor program repricing.

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | | Date: March 2024 |
|---|---|---|---|
| Appropriation/Budget Activity<br>0400 / 3 | R-1 Program Element (Number/Name)<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | Project (Number/Name)<br>MT-15 / *MIXED TECHNOLOGY INTEGRATION* | |

| COST ($ in Millions) | Prior Years | FY 2023 | FY 2024 | FY 2025 Base | FY 2025 OCO | FY 2025 Total | FY 2026 | FY 2027 | FY 2028 | FY 2029 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MT-15: *MIXED TECHNOLOGY INTEGRATION* | - | 33.793 | 47.847 | 24.643 | - | 24.643 | 30.024 | 31.673 | 33.487 | 34.679 | - | - |
| Quantity of RDT&E Articles | - | - | - | - | - | - | - | - | - | - | | |

**A. Mission Description and Budget Item Justification**

The Mixed Technology Integration project funds the advanced development and demonstration of selected basic and applied electronics research programs. Examples of technologies with funded development and demonstration activities include, but are not limited to: reducing the size, weight, and power (SWaP) of components for laser weapon systems that will protect airborne platforms from emerging surface-to-air missiles; integrated photonic-electronic components for positioning, navigation and timing in GPS-denied environments; flexible, software-defined cameras that enable real-time image analysis of complex scenes to provide more actionable information; and optical communications systems that rely on no moving parts enabling their use on SWaP-restricted platforms. Funding under this project is intended to advance transitioning novel technologies to use, providing advanced components compatible with mid-term and other future warfighting requirements.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| ***Title:*** Wideband Secured and Protected Emitter and Receiver (WiSPER) | 21.000 | 25.000 | 8.643 |
| ***Description:*** The Wideband Secured and Protected Emitter and Receiver (WiSPER) program aims to develop an ultra-broadband technology platform to demonstrate a robust, secure, and protected communication link. WiSPER technology provides high signal coding gain to deliver a secured and protected link with significantly enhanced capacity for next generation DoD communications. Current terrestrial tactical radios operate with limited bandwidth at prescribed low frequency bands, which are unable to support high capacity with multiple users and are vulnerable to interference and jamming. WiSPER technology addresses military needs for assured communications, throughput, security, and size, weight, and power limitations of future command, control, communications, computers, intelligence, surveillance and reconnaissance missions. The program will develop an ultra-broadband compact antenna, radio frequency front-end electronics, mixed-signal circuits, and waveform technologies. The WiSPER program will culminate with the integration and demonstration of a secured communication link. Technologies developed under the WiSPER program are planned for transition to the Services. | | | |
| ***FY 2024 Plans:***<br>- Begin implementation of second-generation functional test prototype secured radio transceiver doubling accessible bandwidth with increased dynamic range and diversity.<br>- Optimize the second-generation secured radio transceiver design using modeling and simulation.<br>- Integrate second-generation functional test prototype of the secured radio transceiver into a transportable unit. | | | |
| ***FY 2025 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | Date: March 2024 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 3 | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | **Project (Number/Name)**<br>MT-15 / *MIXED TECHNOLOGY INTEGRATION* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| - Demonstrate transportable prototype secured radio transceiver operating in clear weather environment, demonstrating spatial coding and second-generation featureless packet generation, transmission, and reception.<br>- Design third-generation functional test prototype of the secured radio transceiver.<br>- Begin implementation of third-generation functional test prototype secured radio transceiver reducing size, weight, and power to tactical levels and adapting for operation in harsh conditions and environments.<br>***FY 2024 to FY 2025 Increase/Decrease Statement:***<br>The FY 2025 decrease reflects the change from extensive development of the transceiver to fine-tuning optimization of the transceiver. | | | |
| ***Title:*** Modular Efficient Laser Technology (MELT) | 12.793 | 22.847 | 16.000 |
| ***Description:*** The Modular Efficient Laser Technology (MELT) program will demonstrate the first compact, high-power laser tile as the key building block to enable the next generation of scalable high energy laser (HEL) sources for laser weapon systems (LWS). Today's LWS use fiber laser array HEL sources, complex optical benches, and beam directors. These systems are large and heavy, contain large numbers of individual components, and require skilled labor to fabricate and integrate. This makes current LWS difficult and costly to manufacture, limiting their deployment and application. MELT will leverage recent advances in coherent beam combining and photonic integrated circuits (PICs) fabrication techniques to develop tiled arrays integrated with semiconductor-based optical systems, low-loss waveguides, optical interconnects, and application-specific integrated circuits (ASIC) into a compact laser tile that can be integrated with a supporting backplane to provide scalable HEL sources. This will provide the LWS developer a scalable HEL architecture that maintains excellent beam quality and allows LWS deployment on size, weight, and power (SWaP)-constrained platforms. MELT will leverage a mature industrial base for semiconductor manufacturing, as well as recent advances in photonic integrated circuits, coherent beam combining algorithms, semiconductor cooling techniques, and optical lithography to achieve its program goals. Technologies from this program are intended for transition to Army, Air Force, and Navy.<br>***FY 2024 Plans:***<br>- Perform design of thermal management system for semiconductor amplifier planar array.<br>- Simulate performance of thermal management system for expected range of electrical-to-optical efficiency.<br>- Hold laser tile design review and deliver design review package to include details of laser tile design, modeling, and simulation.<br>- Demonstrate a planar array of emitters in a laboratory, to include demonstrating coherent beam combination and non-mechanical beam steering, for traceability to a fully integrated laser tile.<br>***FY 2025 Plans:***<br>- Fabricate full laser tile array of semiconductor amplifiers with good electrical-to-optical efficiency.<br>- Design fully integrated laser tile with good beam quality. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | Date: March 2024 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 3 | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | **Project (Number/Name)**<br>MT-15 / *MIXED TECHNOLOGY INTEGRATION* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| - Hold panelized high energy laser (HEL) design review and deliver design review package to include details of panelized HEL, modeling, and simulation.<br><br>***FY 2024 to FY 2025 Increase/Decrease Statement:***<br>The FY 2025 decrease reflects a shift from finalizing designs to initiating fabrication and assembly. | | | |
| **Accomplishments/Planned Programs Subtotals** | 33.793 | 47.847 | 24.643 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | | Date: March 2024 |
|---|---|---|---|
| Appropriation/Budget Activity<br>0400 / 3 | R-1 Program Element (Number/Name)<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | Project (Number/Name)<br>MT-16 / *BEYOND SCALING ADVANCED TECHNOLOGIES* | |

| COST ($ in Millions) | Prior Years | FY 2023 | FY 2024 | FY 2025 Base | FY 2025 OCO | FY 2025 Total | FY 2026 | FY 2027 | FY 2028 | FY 2029 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MT-16: *BEYOND SCALING ADVANCED TECHNOLOGIES* | - | 209.317 | 206.186 | 233.201 | - | 233.201 | 238.626 | 242.149 | 221.601 | 226.437 | - | - |
| Quantity of RDT&E Articles | - | - | - | - | - | - | - | - | - | - | | |

**A. Mission Description and Budget Item Justification**

The Beyond Scaling Advanced Technologies Project supports activities to enable and accelerate the transition of disruptive microelectronics advancement, including those developed under the Beyond Scaling Sciences (ES-02) and Beyond Scaling Technology (ELT-02) projects. Funding under this project will include developing new technologies and capabilities in commercial settings, establishing access to these new processes and to commercial state-of-the-art foundries, enabling prototyping, developing manufacturable processes for three-dimensional heterogeneous integration (including integrated photonics), advancing new architectures and integration technologies for advanced field programmable gate arrays (FPGAs), and innovating back end of line technologies for wide bandgap semiconductors.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| ***Title:*** Next Generation Microelectronics Manufacturing (NGMM) | 175.000 | 175.000 | 203.000 |

***Description:*** The Next Generation Microelectronics Manufacturing program is creating a domestic capability for next-generation microsystems using three-dimensional heterogeneous integration (3DHI), including design, fabrication, packaging, assembly, and testing. This capability will emphasize design innovations to sustain U.S. leadership in semiconductors and enhance the use of manufacturing automation in the design, assembly, and testing of 3DHI test articles. The baseline capability will allow users from across the country to quickly and efficiently develop working test articles based on early-stage research and development. This will enable a wide range of organizations and stakeholders to accelerate a domestic 3DHI ecosystem, in the same way foundry access enabled fabless design companies and their associated ecosystems to proliferate.
This research service will feature a baseline fabrication capability for research test articles via a stable 3DHI assembly design kit. Users of the research service will have the ability to join multi-project demonstration runs or dedicated taxi runs. This national accelerator will remove a major impediment to the domestic development of next-generation three-dimensional microsystems and will extend research capabilities beyond those currently being developed worldwide. The research services will incorporate the ability to fabricate unique microsystem test articles using a wide range of devices and materials, integrating the most advanced manufacturing and assembly technologies across silicon, compound semiconductors, photonics, MEMS, and other advanced microelectronics technologies. Applied research associated with this effort is funded within PE 0602716E, Project ELT-02.

***FY 2024 Plans:***
- Establish capability for developing pre-competitive technologies that enable the next generation of manufacturing and accelerate the transfer of innovation from research to prototyping, by enhancing the ability of users to access design, metrology, assembly, and advanced packaging resources.

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | Date: March 2024 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 3 | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | **Project (Number/Name)**<br>MT-16 / *BEYOND SCALING ADVANCED TECHNOLOGIES* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| - Initiate establishing base capabilities for 3DHI prototyping including defined process modules for interconnect vias, bumping, and bonding.<br>- Conduct assessment to reduce cycle-time for die handling in the packaging and assembly processes.<br>- Establish process module validation procedures to include user-based assessments and conduct interim validation assessments.<br>- Create a development plan for automated assembly and advanced packaging toolsets.<br>- Create advisory board and convene biannually to ensure strategic alignment of technical objectives with emerging capabilities.<br>***FY 2025 Plans:***<br>- Release first version of assembly design kit for baseline process modules including interconnect vias, bumping, and bonding.<br>- Conduct first round of research collaboration to increase interconnect density and increase bonding material diversity.<br>- Conduct experiments to quantify the baseline to demonstrate reducing the cycle-time for die handling in the package and assembly processes.<br>***FY 2024 to FY 2025 Increase/Decrease Statement:***<br>The FY 2025 increase reflects SBIR hold and administrative costs. | | | |
| ***Title:*** Programmable Logic for Applications In Defense (PLAID) | 21.806 | 31.186 | 15.000 |
| ***Description:*** The Programmable Logic for Applications In Defense (PLAID) program is developing a heterogeneous compute platform that can support processing of large data arrays. Current computing architectures are subject to scaling, bandwidth, and memory limitations, and the large size of today's chips limits the movement of data resulting in a fundamental trade-off between circuit size and data throughput. The PLAID program will break this paradigm with new architecture development and will achieve more than a 10X increase in on-chip bandwidth. In addition to the development of this new device, the PLAID program will expedite deployment into DoD systems by engaging the defense industrial base to map DoD-relevant radio frequency (RF) processing problems onto the new architecture. These RF problems may include element-level digital beamforming, multi-target tracking radar applications, and synthetic aperture radar processing. Once applications are mapped onto the new processor, the implementation will be programmed and tested with the intent that the use of the new device developed by commercial industry will directly transition into an asymmetric advantage for the DoD and will be used by the defense industrial base in emerging applications.<br>***FY 2024 Plans:***<br>- Complete detailed device designs and begin device verification.<br>- Complete security design to include cryptography, key management, and secure boot.<br>- Complete DoD application initial mapping of trade-offs between problem size and device resources. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | Date: March 2024 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 3 | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | **Project (Number/Name)**<br>MT-16 / *BEYOND SCALING ADVANCED TECHNOLOGIES* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| - Initiate design of approaches to make computations verifiable on advanced computational hardware.<br><br>***FY 2025 Plans:***<br>- Complete device verification and tape-out engineering silicon.<br>- Complete validation and characterization plan for engineering silicon.<br>- Initiate pre-release of alpha programming software.<br>- Demonstrate implementations of DoD applications in simulation.<br><br>***FY 2024 to FY 2025 Increase/Decrease Statement:***<br>The FY 2025 decrease reflects the end of design activities and the move to fabrication, verification, and demonstration. | | | |
| ***Title:*** Supply Chain & Logistics in Electronic Technology<br><br>***Description:*** DARPA s Supply Chain and Logistics in Electronic Technology program is developing the technologies to help ensure a robust and secure domestic supply chain for advanced microsystems. This includes the design, assembly, packaging, and testing technologies for advanced microsystems that exploits and extends beyond commercial activities. It takes advantage of innovations in photonics, optics, materials, and advanced three-dimensional heterogeneous integration (3DHI) for the highest performance electronics technology. In doing so, the program is working to revolutionize domestic industry and enable safe and reliable access to disruptive technology.<br><br>***FY 2025 Plans:***<br>- Initiate trade study on the areas of biggest need and impact in the domestic supply chain of advanced microsystems.<br>- Perform initial design and development of new techniques in reliability testing of complex microsystems.<br>- Develop techniques for the reliable integration and packaging of electronics integrated with advanced photonic and optical interconnects.<br><br>***FY 2024 to FY 2025 Increase/Decrease Statement:***<br>The FY 2025 increase reflects program initiation. | - | - | 15.201 |
| ***Title:*** Technologies for Mixed-mode Ultra Scaled Integrated Circuits (T-MUSIC)<br><br>***Description:*** The Technologies for Mixed-mode Ultra Scaled Integrated Circuits (T-MUSIC) program developed an on-shore semiconductor foundry platform for very wide band radio frequency (RF) mixed-mode integrated circuit analog-to-digital converters for commercial and military systems. Mixed-mode circuits take analog and RF signals and transform them to digital data for processing in computing systems. As defense and commercial wireless applications move to higher frequencies in order to carry more data traffic, integrating the broadband mixed-mode circuitry with high-speed digital processing logic onto one chip becomes imperative to avoid data transfer bottlenecks. T-MUSIC worked to integrate high-speed, high-performance analog and digital electronics together in highly-scaled silicon complementary metal-oxide semiconductor (CMOS) foundries on-shore. This | 7.511 | - | - |

| Exhibit R-2A, RDT&E Project Justification: PB 2025 Defense Advanced Research Projects Agency | | Date: March 2024 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 3 | **R-1 Program Element (Number/Name)**<br>PE 0603739E / *ADVANCED ELECTRONICS TECHNOLOGIES* | **Project (Number/Name)**<br>MT-16 / *BEYOND SCALING ADVANCED TECHNOLOGIES* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2023 | FY 2024 | FY 2025 |
|---|---|---|---|
| process enabled the high levels of integration and performance needed for DoD-relevant and commercial 5G/6G applications. A goal of the T-MUSIC program was to enable very wide bandwidth wireless operations beyond 100 gigahertz (GHz) with low noise and high dynamic range. In addition, T-MUSIC aimed to develop next-generation terahertz (THz) mixed-mode devices based on the advanced digital CMOS fabrication platform. The T-MUSIC program established advanced on-shore foundry capabilities to establish a long-term domestic world-class RF mixed-mode system-on-chip technology for intended transition to DoD and commercial applications. | | | |
| ***Title:*** Photonics in the Package for Extreme Scalability (PIPES)<br>***Description:*** The Photonics in the Package for Extreme Scalability (PIPES) program developed optical signaling technologies for digital microelectronics. Distributed and parallel computing architectures are now pervasive across all size scales, from personal-scale multicore processing units to enterprise-scale high performance computing systems, and span application domains from consumer electronics to DoD systems. Increasingly, however, the benefits of parallelism are constrained not by the limits of computation at individual nodes but by the movement of data between nodes. PIPES advanced microelectronics capabilities by intimately integrating photonics with advanced integrated electronics to yield system connectivity with an unprecedented combination of high aggregate bandwidth, power efficiency, channel density, and link reach. Specifically, PIPES developed photonic input/output (I/O) capability for application-specific integrated circuits and field-programmable gate arrays (FPGAs) that are widely used in advanced DoD sensors and radio frequency systems. The goal of the program was improving I/O bandwidth density, efficiency, and reach by more than 100X to enable disruptive DoD system parallelism and performance scaling. As PIPES technologies matured, they proliferated into central processing units, graphical processing units, and emerging tensor-flow processing units that impacted a wide range of dual-use applications including artificial intelligence, machine learning, large scale emulation, and high-performance computing. To further mature the technology and assure domestic manufacturing ecosystem for DoD use, key PIPES technologies transitioned to the OUSD(R&E) program Co-Packaged Analog-Drive High-Bandwidth Optical Input/Output (KANAGAWA). | 5.000 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 209.317 | 206.186 | 233.201 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A