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**Exhibit R-2, RDT&E Budget Item Justification:** PB 2017 Office of the Secretary Of Defense **Date:** February 2016

<b>Appropriation/Budget Activity</b> 0400: <i>Research, Development, Test &amp; Evaluation, Defense-Wide I BA 5: System Development &amp; Demonstration (SDD)</i>	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z I <i>Trusted Foundry</i>
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COST (\$ in Millions)	Prior Years	FY 2015	FY 2016	FY 2017 Base	FY 2017 OCO	FY 2017 Total	FY 2018	FY 2019	FY 2020	FY 2021	Cost To Complete	Total Cost
Total Program Element	-	0.000	0.000	69.000	-	69.000	91.300	99.300	97.600	96.800	Continuing	Continuing
P837: <i>Trusted Mask Trust Approach</i>	-	0.000	0.000	2.000	-	2.000	2.000	2.000	2.000	2.000	Continuing	Continuing
P838: <i>V&amp;V Capabilities and Standards for Trust</i>	-	0.000	0.000	19.200	-	19.200	42.000	42.000	40.300	39.500	Continuing	Continuing
P839: <i>New Trust Approach</i>	-	0.000	0.000	47.800	-	47.800	47.300	55.300	55.300	55.300	Continuing	Continuing

**A. Mission Description and Budget Item Justification**

This Program Element (PE) supports activities to ensure critical and sensitive integrated circuits are available to meet the DoD's needs. It refines strategies and management planning activities that will (1) provide support to acquisition programs to address trusted microelectronics supply needs; (2) improve capability to evaluate and validate trust of microelectronic parts and advance standards to incentive the commercial marketplace to recognize trust as a competitive design standard; and (3) develop and demonstrate alternative approaches to the current DoD Trusted Supplier accreditation process and criteria to assuring the trust of the microelectronics supply chain in order to enable broader DoD access to commercial state-of-the-art (SOTA) microelectronics technology.

This activity will be coordinated by the Office of the Assistant Secretary of Defense for Research and Engineering, and will include performers from the DoD Components, the Defense Microelectronics Activity (DMEA), the Joint Federated Assurance Center (JFAC), the Defense Advanced Research Programs Agency (DARPA), other DoD and Intelligence Community science and technology (S&T) organizations and laboratories, defense industry, and the broader commercial industrial base. It will integrate the functions of the DoD Trusted Foundry Program, the Trusted Supplier accreditation program, JFAC, and related S&T activities.

This activity implements, maintains and updates the DoD's long-term microelectronics strategy. Recognizing that trusted and assured supply of microelectronics is a Government-wide concern, this activity will interface with interagency partners to take into account interagency requirements, opportunities for collaboration, and strategic decisions that can be made to limit the overall cost of these requirements to the government.

Funds in the amount of \$7M are being reprogrammed in FY 2016; consequently, these funds are not reflected in the current President's Budget. This add is for preparation activities supporting the initiation of Trusted Foundry activities in FY 2017; a \$47.8 million add in FY 2017 supports the initiation of the Trusted Mask Trust Approach, Verification and Validation (V&V) Capabilities and Standards, and New Trust Approach project activities planned across the Future Years Defense Program (FYDP).

Total PE funding from FY 2017 - FY 2021 is as follows:

FY 2017 = \$69.0M / FY 2018 = \$91.3M / FY 2019 = \$99.3M / FY 2020 = \$97.6M / FY 2021 = \$96.8M

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<b>Exhibit R-2, RDT&amp;E Budget Item Justification:</b> PB 2017 Office of the Secretary Of Defense	<b>Date:</b> February 2016
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<b>Appropriation/Budget Activity</b> 0400: <i>Research, Development, Test &amp; Evaluation, Defense-Wide I BA 5: System Development &amp; Demonstration (SDD)</i>	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z I <i>Trusted Foundry</i>
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<b>B. Program Change Summary (\$ in Millions)</b>	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017 Base</b>	<b>FY 2017 OCO</b>	<b>FY 2017 Total</b>
Previous President's Budget	0.000	0.000	0.000	-	0.000
Current President's Budget	0.000	0.000	69.000	-	69.000
Total Adjustments	0.000	0.000	69.000	-	69.000
• Congressional General Reductions	-	-			
• Congressional Directed Reductions	-	-			
• Congressional Rescissions	-	-			
• Congressional Adds	-	-			
• Congressional Directed Transfers	-	-			
• Reprogrammings	-	-			
• SBIR/STTR Transfer	-	-			
• Program Adjustments	-	-	69.000	-	69.000

**Change Summary Explanation**

This add is to support the initiation of Trusted Foundry activities.

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**Exhibit R-2A, RDT&E Project Justification:** PB 2017 Office of the Secretary Of Defense **Date:** February 2016

<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P837 / <i>Trusted Mask Trust Approach</i>
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COST (\$ in Millions)	Prior Years	FY 2015	FY 2016	FY 2017 Base	FY 2017 OCO	FY 2017 Total	FY 2018	FY 2019	FY 2020	FY 2021	Cost To Complete	Total Cost
P837: <i>Trusted Mask Trust Approach</i>	-	0.000	0.000	2.000	-	2.000	2.000	2.000	2.000	2.000	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

**A. Mission Description and Budget Item Justification**

This project develops a new secure (SECRET-level) photomask manufacturing capability down to 14 nanometer (nm) at an existing leading-edge commercial photomask manufacturing supplier to secure the masks and design Internet Protocol (IP) of acquisition programs. This capability can be used in conjunction with one or more leading-edge untrusted commercial foundries. This capability will address needs for trusted masks at technology node sizes < 130nm.

**B. Accomplishments/Planned Programs (\$ in Millions)**

	FY 2015	FY 2016	FY 2017
<b>Title:</b> Trusted Mask Trust Approach	-	0.000	2.000
<b>FY 2016 Plans:</b> In FY 2016, the Defense Microelectronics Activity (DMEA) will: (1) prepare the Defense Production Act (DPA) Title III case for the expansion and upgrade of the Trusted commercial photomask manufacturing supplier facilities and (2) prepare the solicitation and contracting package to extend the supplier's Trusted photomask capabilities as required to be compatible with other leading-edge and Trusted state-of-the-practice foundries supporting microelectronic technology node sizes < 130 nanometer (nm).			
<b>FY 2017 Plans:</b> In FY 2017, DMEA will conduct management and technical support, as required, to preserve secure mask data parsing services for the Department, as well as other Federal entities, with an existing Trusted leading-edge commercial photomask manufacturing supplier to ensure the integrity of the tape-in/mask release, mask manufacturing, and authentication process for photomasks. Over the Future Year Defense Program (FYDP), a new secure (SECRET-level) photomask manufacturing capability at a leading-edge Trusted Supplier facility will be equipped (\$7.2M is planned as a FY 2017 DPA Title III project) and staffed to provide the required critical Trusted photomask capabilities.			
<b>Accomplishments/Planned Programs Subtotals</b>	-	0.000	2.000

**C. Other Program Funding Summary (\$ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

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<b>Exhibit R-2A, RDT&amp;E Project Justification:</b> PB 2017 Office of the Secretary Of Defense		<b>Date:</b> February 2016
<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P837 / <i>Trusted Mask Trust Approach</i>

**E. Performance Metrics**

Performance for this project is monitored in the following ways:

- Number of photomasks created using the secure photomask manufacturing capability.
- Number of acquisition programs using the secure photomask manufacturing capability.
- Number of technology node sizes supported by the secure photomask manufacturing capability.
- Number of foundries supported by the secure photomask manufacturing capability.
- Initial Operational Capability (IOC) is planned for FY 2018 assuming the related DPA Title III project completion in FY 2017.





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**Exhibit R-4A, RDT&E Schedule Details:** PB 2017 Office of the Secretary Of Defense **Date:** February 2016

<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P837 / <i>Trusted Mask Trust Approach</i>
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Schedule Details

Events by Sub Project	Start		End	
	Quarter	Year	Quarter	Year
<b><i>Trusted Mask Trust Approach Program Support</i></b>				
Contract Award	1	2017	2	2017
Initial Operational Capability (IOC)	4	2018	4	2018
Management/Technical Support	1	2017	4	2021

**Note**

See attached chart.

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<b>Exhibit R-2A, RDT&amp;E Project Justification:</b> PB 2017 Office of the Secretary Of Defense										<b>Date:</b> February 2016		
<b>Appropriation/Budget Activity</b> 0400 / 5					<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>				<b>Project (Number/Name)</b> P838 / <i>V&amp;V Capabilities and Standards for Trust</i>			
<b>COST (\$ in Millions)</b>	<b>Prior Years</b>	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017 Base</b>	<b>FY 2017 OCO</b>	<b>FY 2017 Total</b>	<b>FY 2018</b>	<b>FY 2019</b>	<b>FY 2020</b>	<b>FY 2021</b>	<b>Cost To Complete</b>	<b>Total Cost</b>
P838: <i>V&amp;V Capabilities and Standards for Trust</i>	-	0.000	0.000	19.200	-	19.200	42.000	42.000	40.300	39.500	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

**A. Mission Description and Budget Item Justification**

This project improves microelectronics test and verification methodologies in support of verifying trust of untrusted parts and develops standards/practices to foster commercial development of secure and trusted parts. Verification and test technologies are required to provide direct program support for microelectronics trust verification when DoD Trusted Foundry Program options are not available. Core technical laboratories have recently been chartered as a Joint Federated Assurance Center (JFAC) to provide this support. Out-year demands will require an increase in capacity, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities. Challenges have been identified, to include the ability to analyze leading-edge technologies, throughput/time required for analysis, ability to analyze third-party IP contained in microelectronic components, and analysis of non-application-specific integrated circuit (ASIC) components that are increasingly being used for agility, e.g., Field-Programmable Gate Arrays (FPGAs). This project addresses these gaps in current technical capabilities in a collaborative nature amongst the core technical laboratories, driven by projected and realized out-year demand. Three capability areas core to microelectronics analysis and verification will be improved:

- Physical verification, i.e., destructive analysis of integrated circuits and printed circuit boards
- Functional analysis, i.e., non-destructive screening/verification of select, critical parts
- Design verification, i.e., verification/assurance of designs, IP, netlists, bitstreams, firmware, etc.

These improvements will address two primary attributes: (1) technical capability: laboratory equipment, analysis tools, such as imaging software, and highly skilled tradescraft, and (2) the capacity to perform assessments.

This project also develops standards/practices in support of trustworthy designs and supply chains.

**B. Accomplishments/Planned Programs (\$ in Millions)**

	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017</b>
<b>Title:</b> Verification and Validation (V&V) Capabilities and Standards for Trust	-	0.000	19.200
<b>FY 2016 Plans:</b> In FY 2016, at each core Joint Federated Assurance Center (JFAC) laboratory, i.e., Air Force, Army, Navy, and National Security Agency, will fund a dedicated technical government subject matter expert and provide support for identified JFAC acquisition program pilots and non-program-related assessments, e.g., suspicious parts acquired by law enforcement or that failed in the			

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<b>Exhibit R-2A, RDT&amp;E Project Justification:</b> PB 2017 Office of the Secretary Of Defense		<b>Date:</b> February 2016
<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P838 / <i>V&amp;V Capabilities and Standards for Trust</i>

<b>B. Accomplishments/Planned Programs (\$ in Millions)</b>	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017</b>
<p>field. In addition, utilizing the 2015 JFAC hardware assurance capability survey, develop a plan of action based on incremental technical improvement and capacity across participating JFAC laboratories in the following areas;</p> <ul style="list-style-type: none"> <li>• Equipment re-capitalization and new equipment</li> <li>• Data and imaging processing</li> <li>• Enhanced automation</li> <li>• Technology and IP licensing</li> <li>• Training and SME development</li> <li>• Maintenance support</li> <li>• Feasibility studies</li> <li>• Reimbursable (test fixtures, boards, parts, and supplies)</li> <li>• Direct program support (4) in related areas beyond the acquisition program's technical capability or capacity to address.</li> </ul> <p><b>FY 2017 Plans:</b> In FY 2017, the JFAC will: (1) improve its microelectronics test and verification methodologies in support of verifying trust of untrusted parts and (2) develop standards/practices to foster commercial development of secure and trusted parts.</p> <p>Verification and test technologies: Initiate:</p> <ul style="list-style-type: none"> <li>• Improvements to the core JFAC's (1) technical capability, i.e., laboratory equipment, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) the capacity to perform assessments. Out-year demands will continue to require an increase in capacity, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities.</li> <li>• Enhancement of automation needed to increase the throughput of information produced by individual JFAC laboratory tools as well as to facilitate information sharing across the families of tools used for analysis and testing.</li> <li>• Development of common SME training and protocols based on the existing tool base, to include both commercial and government-developed tools.</li> <li>• Funding of an additional SME per core laboratory in support of the microelectronics trust verification and other JFAC-related work.</li> <li>• Cost sharing of direct program support prioritized for FY 2017 focused on addressing technical gaps and trust-related findings.</li> <li>• Investment in the above technical areas based on priority and monitor and report increased technical capability from the baseline 2016 level.</li> </ul> <p>Standards and Practices: Initiate:</p> <ul style="list-style-type: none"> <li>• Development of standards and best practices, and relationships with industry, to foster commercial development of secure and trusted parts.</li> <li>• Establishment of formal relationships with FPGA vendors and other key commercial suppliers to improve device and IP security.</li> </ul>			

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<b>B. Accomplishments/Planned Programs (\$ in Millions)</b>	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017</b>
<ul style="list-style-type: none"> <li>• Acquisition of government access to proprietary designs, software, development, and quality assurance processes and test procedures to develop design practices that minimize security flaws and facilitate verification.</li> <li>• Establishment of government and industry working groups to develop test procedures to validate the trust of designs.</li> <li>• Documentation and promulgation of security-enhancing design practices across government, industry, and academia.</li> <li>• Development of industry-wide standards and practices to establish a common understanding of what constitutes verified and trusted hardware/software/firmware at both the component and systems level.</li> <li>• Development of a common lexicon for secure hardware/software/firmware in collaboration with the Committee for National Security Systems, National Institute of Standards and Technology, Society of Automotive Engineers (SAE) International, etc.</li> <li>• Definition of supply chain controls for assured chain of custody for critical and other microelectronics devices and IP.</li> <li>• Development of security training and educate government and industry system security engineers and material managers on supply chain and life-cycle management best practices using agreed-upon language, standards, and practices</li> <li>• Alignment of DoD Instruction 5200.44 (Protection of Mission Critical Functions to Achieve Trusted Systems and Networks (TSN)), related policies, and National Institute of Technology (NIST) 800-161 (Supply Chain Risk Management Practices for Federal Information Systems and Organizations) with industry standards identifying and addressing gaps in definition and criteria and establishing universally accepted levels of supplier and part trustworthiness.</li> </ul>			
<b>Accomplishments/Planned Programs Subtotals</b>	-	0.000	19.200

**C. Other Program Funding Summary (\$ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Performance for this project is monitored in the following ways:

- Increases in throughput in current JFAC laboratories, and stands-up of additional capability/capacity as required, so that at least two laboratories will have capability in physical verification, functional analysis, and design verification to increase the DoD's overall microelectronics trust verification and test capacity for analysis of state-of-the practice parts.
- Increased Probability of Detection of malicious insertion and/or counterfeit parts.
- Cost to evaluate components.
- Time to evaluate components.



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<b>Exhibit R-4, RDT&amp;E Schedule Profile:</b> PB 2017 Office of the Secretary Of Defense		<b>Date:</b> February 2016
<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P838 / <i>V&amp;V Capabilities and Standards for Trust</i>

FY 2015				FY 2016				FY 2017				FY 2018				FY 2019				FY 2020				FY 2021			
1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4

<b>V&amp;V Capabilities and Standards for Trust Program Support</b>																											
Joint Federated Assurance Center (JFAC) Hardware Assurance (HwA) Technical Working Group Support																											
JFAC HwA capability gap analysis																											
JFAC Subject Matter Expert (SME) training																											
JFAC technical capability improvements																											
JFAC assessments																											
JFAC direct program support																											
Microelectronics trust and supply chain standards and best practices development																											
Government and industry engagement																											
Intellectual Property (IP) access/acquisition																											
Microelectronics trust and supply chain training for Government and industry																											
Microelectronics trust and supply chain policy and guidance development/update																											
Management/Technical Support																											

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<b>Exhibit R-4A, RDT&amp;E Schedule Details:</b> PB 2017 Office of the Secretary Of Defense		<b>Date:</b> February 2016
<b>Appropriation/Budget Activity</b> 0400 / 5	<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>	<b>Project (Number/Name)</b> P838 / <i>V&amp;V Capabilities and Standards for Trust</i>

Schedule Details

Events by Sub Project	Start		End	
	Quarter	Year	Quarter	Year
<b><i>V&amp;V Capabilities and Standards for Trust Program Support</i></b>				
Joint Federated Assurance Center (JFAC) Hardware Assurance (HwA) Technical Working Group Support	1	2017	4	2021
JFAC HwA capability gap analysis	1	2017	4	2021
JFAC Subject Matter Expert (SME) training	1	2017	4	2021
JFAC technical capability improvements	1	2017	4	2021
JFAC assessments	1	2017	4	2021
JFAC direct program support	1	2017	4	2021
Microelectronics trust and supply chain standards and best practices development	1	2017	4	2021
Government and industry engagement	1	2017	4	2021
Intellectual Property (IP) access/acquisition	1	2017	4	2021
Microelectronics trust and supply chain training for Government and industry	1	2017	4	2021
Microelectronics trust and supply chain policy and guidance development/update	1	2017	4	2021
Management/Technical Support	1	2017	4	2021

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<b>Exhibit R-2A, RDT&amp;E Project Justification:</b> PB 2017 Office of the Secretary Of Defense										<b>Date:</b> February 2016		
<b>Appropriation/Budget Activity</b> 0400 / 5					<b>R-1 Program Element (Number/Name)</b> PE 0605140D8Z / <i>Trusted Foundry</i>				<b>Project (Number/Name)</b> P839 / <i>New Trust Approach</i>			
<b>COST (\$ in Millions)</b>	<b>Prior Years</b>	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017 Base</b>	<b>FY 2017 OCO</b>	<b>FY 2017 Total</b>	<b>FY 2018</b>	<b>FY 2019</b>	<b>FY 2020</b>	<b>FY 2021</b>	<b>Cost To Complete</b>	<b>Total Cost</b>
P839: <i>New Trust Approach</i>	-	0.000	0.000	47.800	-	47.800	47.300	55.300	55.300	55.300	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

**A. Mission Description and Budget Item Justification**

This project funds a technology demonstration and transition program to develop, demonstrate and pilot the next generation, technology-driven approach to microelectronics trust, to ensure continued access to leading-edge microelectronic technologies while maintaining the required level of trust in all environments. DoD's ability to access commercial technology for its custom trusted needs is diminishing as leading-edge suppliers become fewer and more focused on serving the global commercial market. DoD's technology needs are broad, and relying on a single source supplier is not feasible. Alternative, advanced manufacturing methods, technologies, and design tools are needed to produce trusted state-of-the-art (SOTA) parts from untrusted sources and to preserve access to these advanced nodes while protecting DoD and Defense Industrial Base IP from exploitation. It also is intended to dramatically improve the capabilities of the Joint Federated Assurance Center (JFAC) with regard to verification and validation of microelectronics trust.

This program will develop innovative design, manufacturing, imaging, tagging, and control and assessment approaches for protecting DoD's microelectronics supply chain and IP. It develops advanced imaging technologies and forensics, Design for Trust techniques, active hardware trust control, electronic component markers, and a data and analysis capability to enable auditing and independent verification and validation of commercial designs. It also develops, demonstrates, and implements concepts for the cost-effective production of custom microelectronics in low volumes and protection of sensitive Internet Protocol (IP) from exploitation.

Technologies that assure trust in a broad range of trusted and non-trusted environments can mitigate the risks associated with sole-source suppliers, allow DoD to quickly respond to the loss of a Trusted Foundry, and increase Government's ability to leverage commercial capabilities. The suite of developed technologies will enable DoD to obfuscate the purpose of sensitive devices, verify their origin and function, and protect sensitive IP from exploitation even while using the global supply chain for most hardware. In cases where the risk involved precludes that level of commercial collaboration, low-volume manufacturing technologies developed under this project would permit DoD to more cheaply produce low volumes of sensitive microelectronics in trusted environments. The project would also support using a repository of third-party IP to expedite circuit design and transition promising technologies to use.

**B. Accomplishments/Planned Programs (\$ in Millions)**

	<b>FY 2015</b>	<b>FY 2016</b>	<b>FY 2017</b>
<b>Title:</b> New Trust Approach	-	0.000	47.800
<b>FY 2016 Plans:</b> In FY 2016, studies and Broad Agency Announcements (BAAs) will be conducted to fully develop and initiate the program. In addition, FY 2017 acquisition program pilots and/or technology demonstrations of mature trust technologies and techniques will be identified and planned.			
<b>FY 2017 Plans:</b>			

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<b>B. Accomplishments/Planned Programs (\$ in Millions)</b>	FY 2015	FY 2016	FY 2017
<p>In FY 2017, initiate the conduct of identified acquisition program pilots and technology demonstrations in accordance with the FY 2016 plan and coordinate efforts across sponsored BAAs, government R&amp;D organizations, academia and industry. Initiate technology transition programs in the following technical areas:</p> <ul style="list-style-type: none"> <li>• Design-For-Trust Techniques</li> <li>• IP Protection</li> <li>• Low-Volume SOTA</li> <li>• Electronic Component Markers</li> <li>• Imaging Technologies and Forensics</li> <li>• Computing Infrastructure and Processing Methods.</li> </ul> <p>Primary efforts include maturing and demonstrating technologies enabling trusted (1) design, (2) access, (3) component integrity and (4) IP protection.</p> <p>Activities will assess and report technical progress against the FY 2016 plan. Engage early on with potential acquisition stakeholder to identify potential transition opportunities. Aid transition through joint collaboration between research teams and stakeholders with a focus on evaluations of prototype, test articles and beta versions of tools, techniques, methods, etc. and their use in operationally-realistic scenarios.</p>			
<b>Accomplishments/Planned Programs Subtotals</b>	-	0.000	47.800

**C. Other Program Funding Summary (\$ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Performance for this project is monitored in the following ways:

- Effectiveness of developed technologies, as measured by:
  - o The speed and reliability of new validation and verification techniques in identifying known microelectronics issues (e.g. tampering) in laboratory and non-laboratory situations;
  - o Successful testing of advanced, alternative manufacturing techniques such as disaggregated manufacturing; and
  - o Resilience of microelectronics protected by new trust approach technologies in red teaming exercises.
- Adoption of next-generation trust technologies, as measured by:

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0400 / 5	PE 0605140D8Z / <i>Trusted Foundry</i>	P839 / <i>New Trust Approach</i>

- o The number of DoD and other Government programs employing these trust technologies, design approaches, or best practices, possibly as facilitated by the provision of use models;
- o The volume and criticality of components employing these technologies, design approaches, or best practices; and
- o Promulgation in DoD guidance and program protection plans.





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Schedule Details

Events by Sub Project	Start		End	
	Quarter	Year	Quarter	Year
<b><i>New Trust Approach Program Support</i></b>				
Dielet authentication of chips and demonstration	2	2017	2	2019
Automated design and verification and demonstration	2	2017	2	2019
Validation of custom integrated circuits and demonstration	1	2017	2	2019
Heterogeneous integration for security and demonstration	1	2017	4	2019
Classified Technology Demonstrator	1	2018	2	2020
Third Party Intellectual Property (IP) Repository development and demonstration	1	2017	4	2021
JFAC technical capability improvement development and demonstration	1	2017	4	2021
Microelectronics trust and supply chain demonstrations	1	2017	4	2021
Government and industry engagement	1	2017	4	2021
Microelectronics trust and supply chain policy and guidance development/update	1	2017	4	2021
Management/Technical Support	1	2017	4	2021

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