Exhibit R-2, RDT&E Budget Item Justification: PB 2019 Office of the Secretary Of Defense	Date: February 2018
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 4: *Advanced Component Development & Prototypes (ACD&P)*	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*

COST ($ in Millions)	Prior Years	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total	FY 2020	FY 2021	FY 2022	FY 2023	Cost To Complete	Total Cost
Total Program Element	0.000	0.000	83.626	233.142	-	233.142	237.209	228.272	239.994	241.626	Continuing	Continuing
645: *Verification & Validation (V&V) Capabilities and Standards for Trust*	0.000	0.000	41.524	41.773	-	41.773	41.007	35.607	36.382	36.831	Continuing	Continuing
646: *New Trust Approach Development*	0.000	0.000	42.102	191.369	-	191.369	196.202	192.665	203.612	204.795	Continuing	Continuing

Note

Service Requirements Review Board (SRRB) efficiencies are included.

A. Mission Description and Budget Item Justification

This Program Element (PE) implements, maintains, and updates the DoD's long-term microelectronics strategy and places emphasis on incentivizing and proving new microelectronics technology solutions. FY 2019 funds in the amount of $2.000 million are being transferred from PE 0603826D8Z for the continuation of Joint Federated Assurance Center (JFAC) hardware and software assurance and integrity analysis activities planned across the Future Years Defense Program (FYDP).

Recognizing that a trusted and assured supply of microelectronics is a U.S. Government (USG)-wide concern, this activity will interface with interagency partners to take into account interagency requirements, opportunities for collaboration, and strategic decisions that can be made to limit the overall cost of these requirements to the USG. Its goal is to eliminate the Department of Defense (DoD)'s reliance on sole source foundries for trusted state-of-the-art (SOTA) microelectronics. It supports activities to ensure critical and sensitive integrated circuits are available to meet the DoD's needs. It refines strategies and management planning activities implementing three integrated, complementary solutions that: (1) protect the Intellectual Property (IP) of microelectronics components; (2) improve capabilities to evaluate and validate the trust and assurance of microelectronic parts and advance standards to incentive the commercial marketplace to recognize hardware assurance as a competitive design standard; and (3) develop and demonstrate alternative approaches to the DoD Trusted Foundry program to assure the microelectronics supply chain in order to enable broader DoD access to commercial SOTA microelectronics technology.

This activity is being led by the Under Secretary of Defense for Research and Engineering. This activity is conducted, in coordination with the JFAC Steering Committee and the Science and Technology (S&T) Advisory Board, by performers, such as the JFAC service providers, Defense Microelectronics Activity (DMEA), the Defense Advanced Research Programs Agency (DARPA), and other DoD and Intelligence Community S&T organizations and laboratories in the area of hardware assurance (HwA) and software assurance (SwA). It is integrating with, and supporting, the functions of the DoD Trusted Foundry Program, the Trusted Supplier accreditation program, JFAC, and related HwA and SwA S&T actions. This activity is also expected to maintain and update the DoD long-term microelectronics strategy based on feedback from the execution of this PE and enable and leverage commercial and academic relationships as necessary to fulfill this mission.

Exhibit R-2, RDT&E Budget Item Justification: PB 2019 Office of the Secretary Of Defense	Date: February 2018
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide I* BA 4: *Advanced Component Development & Prototypes (ACD&P)*	**R-1 Program Element (Number/Name)** PE 0604294D8Z *I Trusted and Assured Microelectronics*

B. Program Change Summary ($ in Millions)	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total
Previous President's Budget	0.000	83.626	81.712	-	81.712
Current President's Budget	0.000	83.626	233.142	-	233.142
Total Adjustments	0.000	0.000	151.430	-	151.430
• Congressional General Reductions	-	-			
• Congressional Directed Reductions	-	-			
• Congressional Rescissions	-	-			
• Congressional Adds	-	-			
• Congressional Directed Transfers	-	-			
• Reprogrammings	-	-			
• SBIR/STTR Transfer	-	-			
• Realignment of funds	-	-	2.000	-	2.000
• Other Program Adjustments	-	-	-0.025	-	-0.025
• Increase for Priority Requirements	-	-	151.020	-	151.020
• Economic Assumption	-	-	-1.565	-	-1.565

Change Summary Explanation

FY 2019 funds in the amount of $2.000 million are being transferred from PE 0603826D8Z for the continuation of JFAC hardware and software assurance and integrity analysis activities planned across the FYDP. An additional $151.020 million was added to support the following: secure design environments; electronic data automation (EDA) tools; third-party IP and USG IP development; persistent expertise; prototype development; advanced foundry research and development (R&D) access; state-of-the-practice (SOTP) foundry access; process IP procurement and transition; tool development; enabling integrated circuit manufacturing; and assessment of supply security and protection.

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense											Date: February 2018	
Appropriation/Budget Activity 0400 / 4					R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*				Project (Number/Name) 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*			
COST ($ in Millions)	**Prior Years**	**FY 2017**	**FY 2018**	**FY 2019 Base**	**FY 2019 OCO**	**FY 2019 Total**	**FY 2020**	**FY 2021**	**FY 2022**	**FY 2023**	**Cost To Complete**	**Total Cost**
645: *Verification & Validation (V&V) Capabilities and Standards for Trust*	0.000	0.000	41.524	41.773	-	41.773	41.007	35.607	36.382	36.831	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project improves microelectronics test and verification methodologies in support of verifying the trust and assurance of parts and develops standards and practices to foster commercial development of secure, trusted and assured parts. Verification and test technologies are required to provide direct program support for microelectronics assurance verification when DoD Trusted Foundry Program options are not available. Core technical laboratories and other HwA and SwA capabilities are chartered as a JFAC to provide this support. Out-year demands will require an increase in capacity, which will take the form of additional personnel and/or equipment to permit scaling of microelectronics assessment capabilities. Challenges have been identified, to include the ability to analyze leading-edge technology nodes (<45 nanometers (nm)), throughput/time required for analysis, ability to analyze third-party IP contained in microelectronic components, and analysis of non-application specific integrated circuit (ASIC) components that are increasingly being used for agility, e.g., Field-Programmable Gate Arrays (FPGAs). This project addresses these gaps in current technical capabilities, in coordination with the JFAC, which prioritizes this investment as required to meet the realized and projected out-year demand for JFAC services. Three capability areas core to microelectronics analysis and verification will be improved:

- Physical verification, i.e., destructive analysis of integrated circuits and printed circuit boards
- Functional analysis, i.e., non-destructive screening/verification of select, critical parts
- Design verification, i.e., verification/assurance of designs, IP, netlists, bitstreams, firmware, etc.

These improvements address two primary attributes: (1) technical capability including laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) the capacity to perform microelectronics assessments.

This project develops and matures assurance mitigations, evaluates the effectiveness of protections of IP in support of integrity, and develops and validates obfuscation and disaggregation technologies. The project will address physical validation tool and capability development, design software validation tool development, counterfeit detection and imaging techniques, and system vulnerability assessments and testbeds.

This project also develops standards and practices in support of assured designs and supply chains and formal relationships with industry to foster commercial development of secure, trusted, and assured parts and for acquisition of USG access to proprietary designs, software, development, and quality assurance processes and test procedures to develop practices that minimize security flaws in designs and facilitate verification. Two capability areas that are core to improved commercial designs will be improved, i.e., assured designs and supply chains.

This project enables JFAC to provide hardware and software assurance and integrity analysis tools, services, best-practices, contract language, and other help to programs that detect, assess, prioritize, and mitigate mission critical vulnerabilities to malicious hardware and software attacks and supply chain exploitation

vulnerabilities. Additionally, the JFAC will provide capabilities for programs to keep assessment findings throughout the life cycle of their systems for data mining (e.g., documentation on rationale for previous mitigation decisions regarding software, hardware, and firmware.) The collaboration between the JFAC and program offices will help mitigate existing and emerging critical threats and vulnerabilities in both software and hardware and yield secure architecture and design patterns available to all DoD programs.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Title: Verification & Validation (V&V) Capabilities and Standards for Trust	-	41.524	41.773

Description: The JFAC will: (1) improve its microelectronics test and verification methodologies in support of verifying trust and assurance of parts and (2) develop standards/practices to foster commercial development of secure, trusted and assured parts.

FY 2018 Plans:
Verification and test technologies activities will include:

• Improvements to the core JFAC's (1) technical capability, through the procurement of laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) capacity to perform microelectronics assessments. FY 2018 and out-year demands will require an increase in capacity supporting weapon system program engagement, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities.
• Enhancement of automation and standard processes needed to increase the throughput of information produced by individual JFAC laboratory tools as well as to facilitate information sharing across the families of tools used for analysis and testing.
• Development of common subject matter expert (SME) training and protocols based on the existing tool base, to include both commercial and USG-developed tools.
• Funding for additional SME support in each core laboratory in support of the microelectronics trust verification and other JFAC-related work.
• Increased direct program support focused on addressing technical gaps and trust-related findings.

Standards and practices activities will include:
• Development of standards and best practices, and relationships with industry, to foster commercial development of secure, trusted and assured parts.
• Establishment of formal relationships with FPGA vendors and other key commercial suppliers to improve device and IP security.
• Acquisition of government access to proprietary designs, software, development, and quality assurance processes and test procedures to develop design practices that minimize security flaws and facilitate verification.
• Establishment of government and industry working groups to develop test procedures to validate the trust of designs.
• Documentation and promulgation of security-enhancing design practices across government, industry, and academia.
• Development of industry-wide standards and practices to establish a common understanding of what constitutes verified and trusted hardware/software/firmware at both the component and systems level.

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
• Maintain infrastructure services and staff for the JFAC Coordination Center (CC), enabling the centralized assurance repository, assurance contract language, metrics, the JFAC Ticketing System for SwA tool license distribution, help-desk, and hard problem analysis. • Incorporate S&T, DARPA/ Intelligence Advanced Research Projects Activity (IARPA), Test & Evaluation (T&E), and Defense Acquisition University (DAU) products into the JFAC website. ***FY 2019 Plans:*** Continuation of FY 2018 verification and test technologies activities including: • Improvements to the core JFAC's (1) technical capability, through the procurement of laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) capacity to perform microelectronics assessments. FY 2019 and out-year demands will require an increase in capacity supporting weapon system program engagement, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities. • Enhancement of automation and standard processes needed to increase the throughput of information produced by individual JFAC laboratory tools as well as to facilitate information sharing across the families of tools used for analysis and testing. • Development of common SME training and protocols based on the existing tool base, to include both commercial and USG-developed tools. • Funding for additional SME support in each core laboratory in support of the microelectronics trust verification and other JFAC-related work. • Increased direct program support focused on addressing technical gaps and assurance-related findings. • Continue to maintain infrastructure services and staff for the JFAC CC, enabling the centralized assurance repository, assurance contract language, metrics, the JFAC Ticketing System for SwA tool license distribution, help-desk, and hard problem analysis. • Incorporate S&T, DARPA/IARPA, T&E, and DAU products into the JFAC website. Continuation of FY 2018 standards and practices activities including: • Development of standards and best practices, and relationships with industry, to foster commercial development of secure, trusted and assured parts. • Establishment of formal relationships with FPGA vendors and other key commercial suppliers to improve device and IP security. • Acquisition of USG access to proprietary designs, software, development, and quality assurance processes and test procedures to develop design practices that minimize security flaws and facilitate verification. • Establishment of USG and industry working groups to develop test procedures to validate the assurance of designs. • Documentation and promulgation of security-enhancing design practices across the USG, industry, and academia. • Development of industry-wide standards and practices to establish a common understanding of what constitutes assured hardware, software, and firmware at both the component and system level.			

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
• Development of a common lexicon for secure hardware, software, and firmware in collaboration with the Committee for National Security Systems, National Institute of Standards and Technology, and the broader USG, industry, and academia. • Definition of supply chain controls for assured chain of custody for critical and other microelectronics devices and IP. • Development of security training and education of USG and industry system security engineers and material managers on supply chain and life-cycle management best practices using agreed-upon language, standards, and practices. • Alignment of DoD Instruction 5200.44 (Protection of Mission Critical Functions to Achieve Trusted Systems and Networks (TSN)), and other related policies and guidance, with other USG, e.g., NIST 800-161 (Supply Chain Risk Management Practices for Federal Information Systems and Organizations), and industry standards identifying and addressing gaps in definition and criteria and establishing accepted levels of supplier and part assurance. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** Funds transferred from PE 0603826D8Z in FY 2019 to correctly align funding in support of the mission.			
Accomplishments/Planned Programs Subtotals	-	41.524	41.773

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

N/A

D. Acquisition Strategy

NA

E. Performance Metrics

Performance for this project is monitored in the following ways:

• Increases in throughput in current JFAC laboratories, and stand-up of additional capability and capacity as required, so that at least two laboratories will have capability in physical verification, functional analysis, and design verification to increase the DoD's overall microelectronics trust verification and test capacity for analysis of parts.
• Increased Probability of Detection of malicious insertion and/or counterfeit parts.
• Decreased cost to evaluate components.
• Decreased time to evaluate components.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2019 Office of the Secretary Of Defense			Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*	

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2017 Cost	FY 2017 Award Date	FY 2018 Cost	FY 2018 Award Date	FY 2019 Base Cost	FY 2019 Base Award Date	FY 2019 OCO Cost	FY 2019 OCO Award Date	FY 2019 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
V&V Capabilities and Standards for Trust	MIPR	Various (Air Force, Army, Navy, NSA) : Various	-	-		41.524	Mar 2018	41.773	Mar 2019	-		41.773	Continuing	Continuing	-
		Subtotal	-	-		41.524		41.773		-		41.773	Continuing	Continuing	N/A

Remarks

N/A

	Prior Years	FY 2017		FY 2018		FY 2019 Base		FY 2019 OCO		FY 2019 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	-		41.524		41.773		-		41.773	Continuing	Continuing	N/A

Remarks

NA

Exhibit R-4, RDT&E Schedule Profile: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

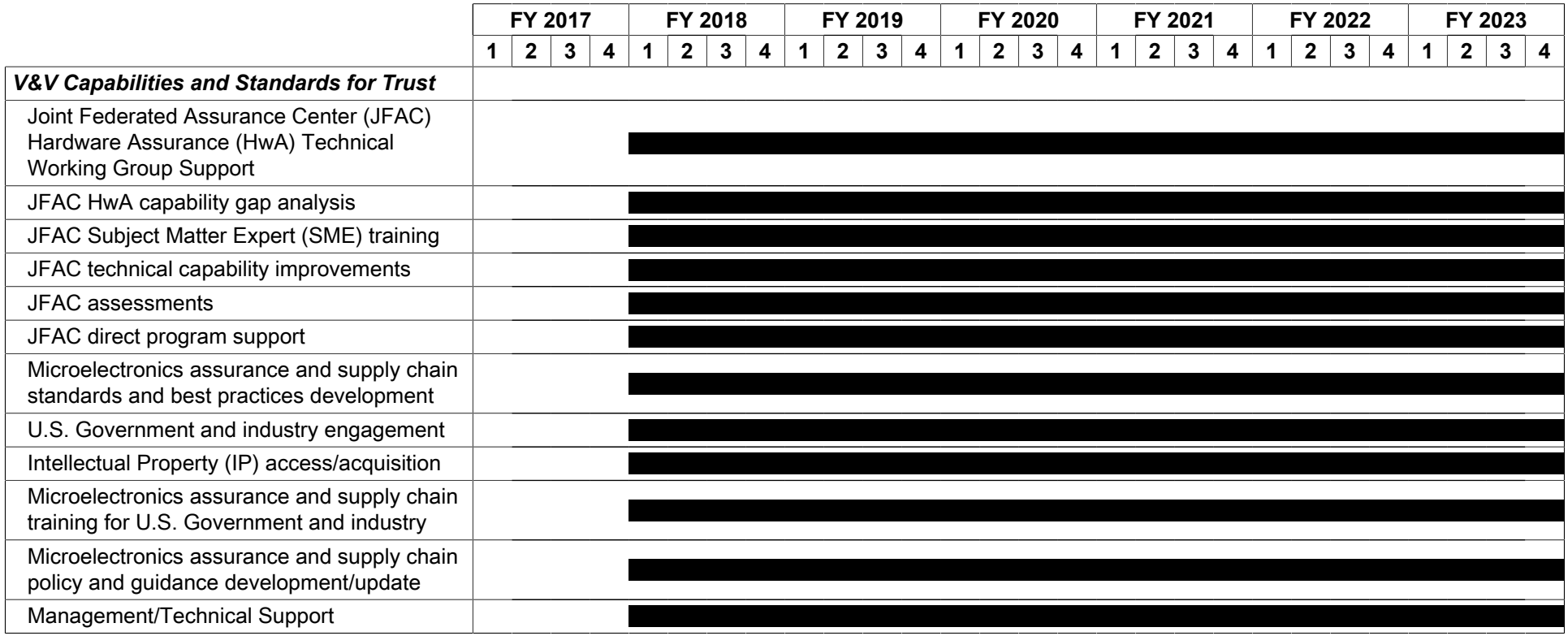

Exhibit R-4A, RDT&E Schedule Details: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
V&V Capabilities and Standards for Trust				
Joint Federated Assurance Center (JFAC) Hardware Assurance (HwA) Technical Working Group Support	1	2018	4	2023
JFAC HwA capability gap analysis	1	2018	4	2023
JFAC Subject Matter Expert (SME) training	1	2018	4	2023
JFAC technical capability improvements	1	2018	4	2023
JFAC assessments	1	2018	4	2023
JFAC direct program support	1	2018	4	2023
Microelectronics assurance and supply chain standards and best practices development	1	2018	4	2023
U.S. Government and industry engagement	1	2018	4	2023
Intellectual Property (IP) access/acquisition	1	2018	4	2023
Microelectronics assurance and supply chain training for U.S. Government and industry	1	2018	4	2023
Microelectronics assurance and supply chain policy and guidance development/update	1	2018	4	2023
Management/Technical Support	1	2018	4	2023

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense			Date: February 2018
Appropriation/Budget Activity 0400 / 4	R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*	Project (Number/Name) 646 / *New Trust Approach Development*	

COST ($ in Millions)	Prior Years	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total	FY 2020	FY 2021	FY 2022	FY 2023	Cost To Complete	Total Cost
646: *New Trust Approach Development*	0.000	0.000	42.102	191.369	-	191.369	196.202	192.665	203.612	204.795	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project funds a program of research to develop the next generation, technology-driven approach to microelectronics trust and assurance, to include state-of-the-art (SOTA) microelectronics, to ensure continued access to SOTA microelectronic technologies while maintaining the required level of assurance in all environments. DoD's ability to access commercial technology for its custom, secure, trusted and assured needs is diminishing as SOTA suppliers become fewer and more focused on serving the global commercial market. DoD's technology needs are broad, and relying on a single source supplier is not feasible. Alternative, advanced manufacturing methods, technologies, and design tools are needed to produce secure, trusted and assured SOTA parts from commercial sources and to preserve access to these advanced nodes while protecting DoD and Defense Industrial Base IP from exploitation. It is also intended to dramatically improve the capabilities of the JFAC with regard to verification and validation of SOTA microelectronics assurance.

This program of research will develop innovative design, manufacturing, imaging, tagging, and control and assessment approaches for protecting DoD's microelectronics supply chain and IP, including alternatives for trusted and assured strategic radiation-hardened electronics in advanced technology nodes for next-generation strategic systems, obfuscation and disaggregation technology development, and other assurance mitigations. It will develop advanced imaging technologies and forensics, Design for Assurance techniques, active hardware assurance controls, electronic component markers, and a data and analysis capability to enable auditing and independent verification and validation of commercial designs. It also develops, demonstrates, and implements concepts for the cost-effective production of custom microelectronics in low volumes and protection of sensitive IP from exploitation.

Assurance technologies that can be applied in a broad range of trusted and commercial environments can mitigate the risk associated with sole-source suppliers and increase the Government's ability to leverage commercial capabilities. The suite of developed technologies, e.g., alternative manufacturing methods and design tools, will enable DoD to obfuscate the purpose of sensitive devices, verify their origin and function, and protect sensitive IP from exploitation even while using the global supply chain for most hardware. In cases where the risk involved precludes that level of commercial collaboration, low-volume manufacturing technologies developed under this project would permit DoD to more cheaply produce low volumes of sensitive microelectronics in trusted environments. The project would also support using a repository of vetted third-party IP and EDA tools to expedite circuit design and transition promising technologies to use.

This project has received additional funding starting in FY 2019 to support microelectronics innovation efforts in the following focus areas: capture and secure microelectronics R&D; new microelectronics development, demonstration, and capability insertion; radiation hardening by process (RHBP) and radiation hardening by design (RHBD); and radio frequency (RF) and opto-electronics.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Title: New Trust Approach Development	-	42.102	191.369

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Description: This project's activities will mature and evaluate assurance technologies and techniques through efforts that may include the conduct of studies and Broad Agency Announcements (BAAs) and other efforts to coordinate research programs across USG R&D organizations, academia, and industry. In addition, the JFAC will initiate the conduct of identified acquisition program pilots and technology demonstrations in coordination with research programs across government R&D organizations, academia and industry. ***FY 2018 Plans:*** This project will initiate and support at least one R&D activity in each of the following technical focus areas: • Design-For-Trust techniques • IP protection • Low-volume SOTA manufacturing • Electronic component markers • Imaging technologies and forensics • Computing infrastructure and processing methods. Primary efforts will include reducing-to-practice technologies enabling trusted (1) design, (2) access, (3) component integrity and (4) IP protection. FY 2018 primary activities include development of these technologies, followed by transition of these capabilities to new programs in the following fiscal years under PE 0605294D8Z. This project will engage early on with potential stakeholders to identify potential transition issues and aid in transition through joint collaboration between research teams and stakeholders with a focus on evaluations of prototypes, test articles, and beta versions of tools, IP, techniques, methods, etc. and their use in operationally-realistic scenarios. ***FY 2019 Plans:*** This project will use the augmented funding in FY19 to initiate and support R&D activities in each of the following technical focus areas: • Capture and secure microelectronics R&D, including support and enhanced manufacturing at SOTP foundries. • New microelectronics development, demonstration, and capability insertion including supporting public/private co-development of new COTS programmable devices that address USG needs during their development by industry when it is the most cost-effective to do so. • RHBP and RHBD including supporting secure design of RHBD IP in all major domestic foundries and fabrication of SOTA test articles for evaluation and qualification.			

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
• RF and opto-electronics including supporting secure design of IP and access to SOTP government and commercial facilities for RF and optical devices. Primary efforts will include reducing-to-practice technologies enabling assured (1) design, (2) access, (3) component integrity and (4) IP protection. This project will engage early on with potential stakeholders to identify potential transition issues and aid in transition through joint collaboration between research teams and stakeholders with a focus on evaluations of prototypes, test articles and beta versions of tools, IP, techniques, methods, etc. and their use in operationally-realistic scenarios. Primary activities in FY 2019 will continue the development of these technologies, followed by transition of these capabilities to new programs in the fiscal years that follow under PE 0605294D8Z. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** FY 2019 increase supports additional efforts in this USG priority area.			
Accomplishments/Planned Programs Subtotals	-	42.102	191.369

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

N/A

D. Acquisition Strategy

N/A

E. Performance Metrics

Performance for this project is monitored in the following ways:

• Enhanced capability in physical verification, functional analysis, and design verification.

• Increased Probability of Detection of malicious insertion and/or counterfeit parts.

• Expanded access to leading SOTA technology and enhanced availability of essential SOTP design and fabrication capabilities.

• Successful transition demonstrations from commercial technology to modernized military applications, e.g., such as strategic radiation-hardened and RF-optical microelectronics.

• Effectiveness of developed technologies, as measured by:

Exhibit R-2A, RDT&E Project Justification: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

- The speed and reliability of new validation and verification techniques in identifying known microelectronics issues (e.g., tampering) in laboratory and non-laboratory situations.
- Successful demonstration of advanced, alternative manufacturing techniques, such as disaggregated manufacturing.
- Resilience of microelectronics protected by new trust approach technologies in red teaming exercises.

• Adoption of next-generation commercial technologies, as measured by:

- The number of DoD and other USG programs employing assured access to SOTP and SOTA technologies, design approaches, and best practices developed in cooperation with commercial partners.
- The volume and criticality of components employing these technologies, design approaches, or best practices.
- Promulgation in DoD guidance and program protection plans.

• Commercial partnerships established for, or enhanced by, the development and manufacture of DoD microelectronics using next-generation assurance technologies.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2017 Cost	FY 2017 Award Date	FY 2018 Cost	FY 2018 Award Date	FY 2019 Base Cost	FY 2019 Base Award Date	FY 2019 OCO Cost	FY 2019 OCO Award Date	FY 2019 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
New Trust Approach Development	MIPR	Various (DARPA, Air Force, Army, Navy, NSA) : Various	-	-		42.102	Mar 2018	191.369	Mar 2019	-		191.369	Continuing	Continuing	-
		Subtotal	-	-		42.102		191.369		-		191.369	Continuing	Continuing	N/A

	Prior Years	FY 2017		FY 2018		FY 2019 Base		FY 2019 OCO		FY 2019 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	-		42.102		191.369		-		191.369	Continuing	Continuing	N/A

Remarks

NA

Exhibit R-4, RDT&E Schedule Profile: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

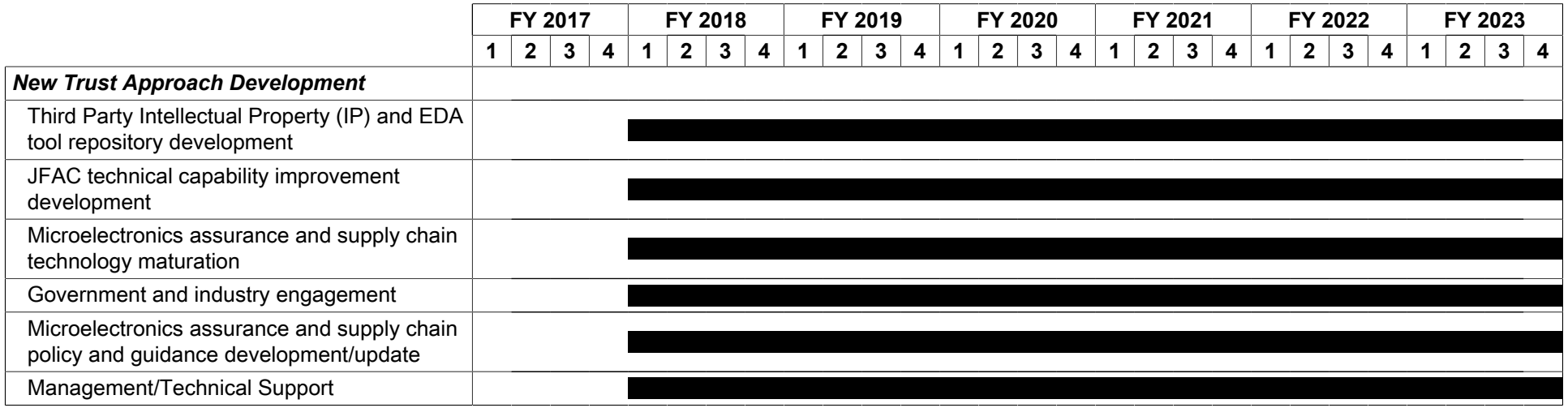

Exhibit R-4A, RDT&E Schedule Details: PB 2019 Office of the Secretary Of Defense		Date: February 2018
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
New Trust Approach Development				
Third Party Intellectual Property (IP) and EDA tool repository development	1	2018	4	2023
JFAC technical capability improvement development	1	2018	4	2023
Microelectronics assurance and supply chain technology maturation	1	2018	4	2023
Government and industry engagement	1	2018	4	2023
Microelectronics assurance and supply chain policy and guidance development/update	1	2018	4	2023
Management/Technical Support	1	2018	4	2023