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MAGNETIC AMPLIFIERS - TECHNICAL REPORT N° 12

AN APPLICATION OF MAGNETIC AMPLIFIER CIRCUITS TO PERFORM MULTIPLICATION AND OTHER ANALYTICAL OPERATIONS

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AN APPLICATION OF MAGNETIC AMPLIFIER CIRCUITS TO PERFORM MULTIPLICATION AND OTHER ANALYTICAL OPERATIONS

Synopsis: Circuits are described which yield an output voltage proportional to the product or quotient of any number of input voltages. The components used are magnetic cores of grain oriented nickel alloys, half-wave rectifiers and linear resistors. Experimental results and some design considerations are given. Circuits of the same kind are also suggested for performing indefinite integration and other analytical operations upon signal voltages which are functions of time.

INTRODUCTION

Conventional magnetic amplifiers are well suited to perform mixing of signals as the output depends on the total magnetomotive force of control provided jointly by any number of input windings. Over the linear range of the ampereturns transfer characteristic, the output is simply proportional to the algebraic summation of signals; other operations can also be performed, in a less straight forward manner, by proper use of non-linear regions of the characteristic.

The circuits described in this paper, however, operate on somewhat different principles. Their components are "single-core" amplifiers of the kind described by Ramey (Ref. 1, 2) and utilized also in many ways by the same author e.g. in digital computer applications (Ref. 3).

Although this kind of amplifier is known, a brief discussion of its essential features is given below; a proper appreciation of these features is essential for the understanding of the specific applications described further in this paper.

I. THE ELEMENTARY SINGLE-CORE AMPLIFIER

An amplifier of this type is shown in Fig. 1-a) in its simplest circuitry. The magnetic core is characterized by a sharply defined saturation at flux levels $\pm \Phi_{sat}$ reached with comparatively small magnetomotive forces as shown in Fig. 1-b) in an idealization which is adequate for grain-oriented nickel alloys commonly used in high grade amplifiers. A single winding links this core with N turns; r is the resistance of this winding and R_L is a load resistance. γ and σ are two half-wave rectifiers; it is assumed at first that forward rectifier conduction takes place with negigibly small voltage drops while infinte resistance is offered to the flow of current in the reverse direction.

v_g is the voltage of the power supply (or "gate voltage"); v_s is the signal voltage. For the sake of simplicity in Fig. 1-c) it is assumed that $v_g = V_{g\,max} \sin \omega t$, with $\omega = 2\pi f$ = angular velocity of the sinusoidal power source and $V_{g\,max} < \omega N \Phi_{sat}$ (that is, application of the gate voltage directly at the terminals of the winding N would not cause saturation in the steady-state). Also v_s is assumed to be a full-wave rectified sinusoidal voltage in phase with the gate voltage and with a crest $|V_{s\,max}| = \kappa V_{g\,max}$ where $0 \leq \kappa \leq 1$. This rectified signal voltage is acting constantly against the direction of forward conduction of the rectifier σ .

(Consistent algebraic conventions are established in text and drawings as instantaneous voltages are considered measured from one common reference or ground).

In positive half-cycles of the power supply voltage the core flux rises from some initial level towards saturation; in this process of varying fluxes the voltage v_g is balanced almost completely by the rate of change of flux linkages $N\, d\Phi/dt$ while a very small magnetizing current (dictated by the minor hysteresis loop described) flows with negligibly small voltage drops in R_L and r. At some time during this half-cycle saturation is reached; the process of flux changes terminates and in the remaining part of this half-cycle $i = v_g / (R_L + r)$. As v_g becomes zero, i becomes zero too and at the end of the positive half-cycle the core is left at the flux level $+\Phi_{sat}$. No current flows in the signal circuit throughout this half-cycle because of the blocking action of the rectifier σ .

In the next (negative) half-cycle v_g reverses its polarity; the rectifier γ blocks any flow of current through the load. But, as v_g now overrules v_s the rectifier σ becomes conducting and a process of flux changes initiates during which a reversed small magnetizing current flows in the winding. That is, the core flux is being brought down from the level $+\Phi_{sat}$, as the rate of change of flux linkages balances almost entirely the voltage $(v_g - v_s)$. In view of the limitation stipulated for the amplitude of v_g in no case negative saturation is reached in this half-cycle, that is, the process of flux decay from $+\Phi_{sat}$ extends throughout this "presetting" half-cycle, at the end of which a flux level Φ_p is reached expressed by

$$-N\left(\Phi_{sat} - \Phi_p\right) = \int_{-T/2}^{0} (v_g - v_s)\, dt = \text{volt-time area } A_I$$

with the notation used in Fig. 1-c).

In the next "gating" half-cycle the flux starts rising again from this "pre-set" level Φ_p under the action of the positive v_g as described initially. This process terminates at a "firing time" t_f at which saturation is reached, that is

$$\int_0^{t_f} v_g\, dt = N\left(\Phi_{sat} - \Phi_p\right) = \text{volt-time area } A_{III}.$$

From then on and for the rest of the gating half-cycle the voltage v_g appears across the circuit resistances with a volt-time area of gross output

$$A_{IV} = \int_{t_f}^{T/2} v_g \, dt = \int_{t_f}^{T/2} (R_L + r)\, i \, dt$$

(The volt-time area of net output into the load R_L is simply $A_{IV} \cdot R_L/(R_L + r)$.) Since $A_{III} = -A_I$ it follows that $A_{IV} = -A_{III}$. Thus the controlling action of the signal voltage acting in one pre-setting half-cycle upon the output of the immediately following gating half-cycle is fully evidenced.

Although Fig. 1-c) refers to the simple case of a sinusoidal gate voltage v_g and a full-wave rectified sinusoidal signal voltage v_s no use has been made of such particular restrictions throughout the reasoning. In fact for the type of operation described the gate voltage can have different wave forms and the durations of positive and negative half-cycles do not even need to be equal as long as the volt-time areas of v_g in one pre-setting half-cycle and in the subsequent gating half-cycle are equal in absolute value (and less than $2 N \Phi_{sat}$).

It is seen also that wave form and magnitudes of signal voltage v_s during a gating half-cycle are of no relevance on the operation as long, of course, as σ is kept blocked. (That is, v_s should not be allowed to become positive but it can well be zero).

During the pre-setting half-cycle the wave form of signal may also be irrelevant. If the gate voltage is able to overrule v_s throughout this half-cycle the fact remains that the spotted volt-time area A_{III} is equal and opposite to the time integral of $(v_g - v_s)$ over the pre-setting half-cycle . On the other hand unduly large instantaneous values of negative v_s may cause σ to block thus arresting the pre-setting process of flux changes temporarily. For instance no flux changes take place over the interval t' t" in the situation of Fig. 1-d). In this case A_{II} no longer is the total volt-time area of signal, but rather is the shaded area of the contour of least ordinates ("least" in absolute value) of both v_s and v_g as shown.

This consideration allows to predict the performance of an amplifier with sinusoidal gate voltage and d.c. signals and explains its lack of linearity. (Linearity, of course, can be obtained in the case of d.c. signals if the gate voltage is square-waved). Also an elementary use of this consideration can be made for the measurement of the phase angle Θ of two sinusoidal voltages of equal amplitude and frequency $v_1 = V_{max} \sin \omega t$ and $v_2 = V_{max} \sin (\omega t - \Theta)$. For this v_g is made equal to v_1 while v_s is obtained from half-wave rectification of v_2. As seen in Fig. 1-e) the volt-time area A_{II} of the contour of least ordinates is then $(\sin \Theta/2 - 1) V_{max}/\omega$. Therefore, Θ can be obtained from the readings of a D'Arsonval meter in the output circuit on a scale suitably marked.

The considerations above relate volt-time areas of pre-setting to volt-

time areas of gating. Thus the action of pre-setting signal substantially is related to cyclic averages of output currents or voltages. The wave form of the output voltage is also of interest in many instances; in the operation the wave form of the curve delimiting A_{II} is converted in the output into a wave form with ordinates equal to zero before firing and coinciding with the ordinates of the gate voltage after firing. This "conversion of wave forms" is utilized in one stage of the multiplying circuits described later in this paper.

II. THE MULTI-CHANNEL AMPLIFIER

A modification of the previous device is shown in the amplifier of Fig. 2-a) in which many input channels are provided for a corresponding number of signal voltages $v_{s1}, v_{s2} \cdots v_{sn}$. In gating half-cycles the operation is the same as before, the wave forms of the signals being irrelevant as long as proper polarities insure blocking of the corresponding σ rectifiers. On the other hand during pre-setting half-cycles the negative voltage v_g overrules whichever signal voltage happens to have the lowest absolute value, while γ and all the other σ rectifiers are blocking. That is, at any instant the rate of change of decaying core flux is dictated by the resultant of the gate voltage and of the weakest signal voltage. Accordingly, a magnetic coincidence counter (3) has been developed under the recognition that no output is found in the gating if even only one of the signal voltages has been zero through the pre-setting.

More generally it is seen here that the gated output area is equal to the area of the contour of least ordinates of gate and signal voltages during pre-setting as shown in Figure 2-b). This general property may have a number of interesting analytical applications. If an assigned voltage $v_{s1}(t)$ is applied periodically in the negative half-cycles in conjunction with a large signal $v_{s2}(t)$ dropping to zero at $t = t_1$ as shown in Figure 2-c), the reading of a D'Arsonval meter in the output is proportional to the integral

$$\int_0^{t_1} v_{s1}(t)\, dt$$

Thus if t_1 is gradually phase-shifted a writing d.c. meter of adequately large inertia can plot directly the indefinite integral function on a roll of paper moving synchronously with whatever organ controls the scanning phase shift of v_{s2}. (The periodical obliteration of the action of $v_{s1}(t)$ can be obtained and phase-shifted in various other ways e.g. by suitably timed mechanical contactors temporarily shorting the rectifier γ in a single-channel amplifier).

Useful analytical information on the function $v_{1s}(t)$ as shown in Fig. 2-d) can be obtained also by use of a scanning wave v_{s2} of any chosen width 2a (or by contactors timely shorting γ e.g. at all times but $t_1 - a \leq t \leq t_1 + a$.)

On the other hand, gross outputs equal to the areas shaded in Fig. 2-e) results from a scanning with progressively increased d.c. voltages v_{s2}; thus another type of information on the function v_{s1} is obtained. The simplicity of the circuits

and components needed to perform these and similar other analytical operations may be an incentive for actuale usage in analogue computer studies e.g. as applied to statistical problems.

III. MULTIPLYING CIRCUITS

(a) Two-stage multiplying circuits

A single-channel amplifier of the type described in Part I constitutes the converter stage shown in Fig. 3. This stage operates on a sinusoidal gate voltage $v_{gC} = \sqrt{2}\, V_{gc} \sin \omega t$ with a half-wave rectified signal voltage v_{s1}, of arbitrary wave form. This signal voltage is "converted" in the gross output voltage v_c absorbed by the resistances $(R_C + r_C)$ in the subsequent half-cycle after firing.

A two-channel amplifier of the type described in Part II constitutes the multiplier stage. Its sinusoidal gate voltage is v_{gM}. (For the sake of simplicity v_{gM} is assumed identical to v_{gC} in Fig. 3). A half-wave rectified sinusoidal signal voltage v_{s2} is one of the inputs, while the other input is the net converter output $v_c' = v_c \cdot R_c/(R_c + r_c)$ appearing across the load resistance R_c. In the time interval from 0 to t_f v_c' is zero (or nearly so) and therefore the pre-setting flux change of the multiplier core is dictated completely by v_{gM}, as the action of v_{s2} is obliterated over this interval. Therefore the total pre-setting over the half-cycle is limited only by the area A_{VI} of least ordinates, recognized with opposite sign as the area A_{VIII} of gross output of the multiplier in the next half-cycle. The various volt-time areas of the two stages are related easily to the readings of the rms voltmeter V_{gC} and of the d.c. voltmeters V_1, V_2, and V_M as shown in Fig. 3, with the result

$$V_M = \frac{R_M}{R_M + r_M} \cdot \frac{\pi}{\sqrt{2}} \cdot \frac{V_1 V_2}{V_{gC}} \qquad (1$$

Thus multiplication as well as division is performed by the system.

It can be noted that V_{gC} appears in the denominator because increases of V_{gC} increase t_f and thus reduce the area A_{VI} and A_{VIII}. On the other hand the crest of the multiplier gate voltage can be varied without any effect of first order on the results because such variations, while affecting the wave form of multiplier output voltage do not modify the volt-time area A_{VIII} and the reading of the meter V_M

It may be noted also that the two stages do not need to have cores of equal dimensions or magnetic characteristics, and their windings can also have different turns, provided, ofcourse, that in each stage the gate voltage satisfies the condition $V_g \max < \omega N \Phi$ sat.

The operating range of the device has evident limits; namely $|v_{s1}|$ must be less than $|v_{gc}|$ during converter pre-setting, and the crest of v_{s2} must be lower than both $\sqrt{2}\, V_{gC}\, R_c/(R_c + r_c)$ and $\sqrt{2}\, V_{gM}$ during multiplier pre-setting. Different levels of signals can be handled by substituting any one input channel of the converter or of the multiplier with a separate signal winding of suitable turns $N_s \neq N$ in series with one half-rectifier. (The signal applied to any such winding then must act against the pre-setting action of a voltage $v_g' = v_g N_s/N$ impressed in series in the same winding from the secondary of a transformer with this turns ratio. Such

known modifications of the elementary amplifier circuits of Fig. 1 and 2 do not modify in the least the basic operation of the multiplying system described here and do not need to be examined in detail).

Also it is recognized that the given signals U_{s1} and U_{s2} act upon the system in two subsequent half-cycles. Hence, a certain cross-correlation lag $\tau = 1/2f$ is inherent to the multiplication performed. (This lag may be increased, if so desired, for cross-correlation or auto-correlation studies, by the insertion of half-cyclic delay stages (Ref. 3) between converter and multiplier). One additional half-cycle lag affects the final output.

The considerations above are not necessarily limited to sinusoidal gate voltage and signals. It is sufficient to point out that the circuit of Fig. 3 performs also multiplication of d.c. signals if the gate voltages are square waves symmetrical about zero (as obtained e.g. from a d.c. power source through a rotating commutator); in this case the various volt-time areas A_I to A_{VIII} become rectangles and the behaviors of converter and multiplier are even more clearly seen.

(b) Multi-stage multiplying circuits

The output voltage U_M of the multiplier stage of Fig. 3 has a "converted" wave form of the same kind as U_c'. This suggests that a second multiplier stage can be added directly to the system of Fig. 3, one of its inputs being $V_M' = V_M$ while the other input is an assigned half-wave rectified sinusoidal signal voltage U_{s3}. The reasoning applied to the volt-time areas of the single multiplier stage of Fig. 3 can be extended to this new stage with the result

$$V_M'' = \frac{R_M''}{R_M'' + r_M''} \left(\frac{\pi}{\sqrt{2}}\right)^2 \frac{V_1 \, V_2 \, V_3}{V_{gC} \, V_{gM'}} \qquad (2$$

where V_1, V_2, V_3 are d.c. meter readings of the assigned signal voltages, V_M'' is the d.c. meter reading of output voltage across the load resistance R_M'' of the second multiplier stage and V_{gC} and $V_{gM'}$ are r.m.s. readings of the gate voltages of the converter and of the first multiplier. This idea can be extended, in principle, to the use of any number ν of multiplier stages, each one of which receives the output voltage of the immediately preceeding stage as a "converted" signal in conjunction with a new half-wave rectified sinusoidal signal independently assigned. The end output metered by $V_{M\nu}$ across the load resistance $R_{M\nu}$ of the last multiplier, is

$$V_{M\nu} = \frac{R_{M\nu}}{R_{M\nu} + r_{M\nu}} \left(\frac{\pi}{\sqrt{2}}\right)^{\nu} \frac{V_1 \, V_2 \cdots V_{(\nu+1)}}{V_{gC} \, V_{gM'} \cdots V_{gM(\nu-1)}} \qquad (3$$

where the numerator factors are d.c. meter readings of the assigned signals and the denominator factors are r.m.s. reading of gate voltages of all but the last stage. The various signals act upon the system in subsequent half-cycles, while one additional half-cycle lag affects the final output. Proper use of the concept of "areas of least ordinates" must be made to determine the upper limits of signal voltages allowable to effectively control each stage. The total number of stages practically usable in any such system may be limited, of course, by cumulative errors, some of which are discussed in the next pages.

c) Experimental results and critical comments

Figure 4 presents some experimental results of operations performed by the circuit of Figure 3 slightly modified as sketched with the following components:

- Magnetic cores - Hypernik V, DO = 2½" DI = 1½" Tape height = ½" Number of turns per core N = 2500, winding resistances $r_C = r_M = 65$ ohms.

- Rectifiers: Germanium G10, 130 volts rms reverse voltage, 400 mA (later use of selenium rectifiers yielded substantially identical results).

- Load resistances $R_C = 500$ ohms, $R_M = 410$ ohms.

On the left multiplications have been performed by keeping the gate voltages constant, by assigning some fixed value to the signal V_1 and by varying V_2, (V_M ceases to increase when V_2 becomes too large to further control the area of least ordinates of multiplier pre-setting).

On the right side divisions have been performed by varying the converter gate voltage V_{gC} for fixed values of $V_1 = V_2$. The multiplier gate voltage V_{gM} was constant (crossed points) or else was varied together with V_{gC} (encircled points); as should be expected crosses and circles fall on the same lines. (The rectifier σ_{s1} remains blocked during converter pre-setting half-cycles when V_{gC} is decreased below a certain value; then the hyperbolic trend breaks as the converted signal v'_C becomes a sinusoidal half-wave of amplitude decreasing with V_{gC} and the final output V_M decreases also accordingly.)

The experimental results show departures from the idealized behavior expressed by eq. 1. First of all the multiplier winding after firing possesses residual inductance; hence the metered output is somewhat lower than expected. Practically a calibration of the circuit (simply performed e.g. at some large value of V_1 and V_2) to determine the factor K in the formula written in Figure 4 disposes of this error quite well at all but low outputs.

In the experimentation it appeared of primary interest to extend the accuracy of eq. 1 as far as possible into the region of either signal approaching zero. For this more careful attention must be given to a different source of errors which really determines the practical design and performance of the system. The simplified reasoning presented has been focussed on voltages acting upon the cores and on their volt-time areas under the assumption that the magnetizing current flowing in the pre-setting and pre-firing intervals are negligibly small. But a more close scruting must be given to the voltage drops of these currents through the resistances of their various paths. Of course, in every given numerical situation these voltage drops are known and their influence upon the various phases of the operation is evaluated easily in terms of modified volt-time areas.

Now in the multiplication curves of Fig. 4 it is seen that for $V_1 = 0$ a certain output V_M, small but not quite zero, was metered. In fact with $v_{s1} = 0$, no firing of the converter occurs in its gating half-cycles, but still the flow of magnetizing current through R_C gives a certain converted signal v'_C to the multiplier;

the latter's area of least ordinates A_{V1} is not brought to zero, and the multiplier does fire at some time near the end of its gating half-cycle with an output substantially independent of V_2. A direct use of the original circuit of Figure 3 had caused an even larger error in the V_M reading because of the drop of pre-firing magnetizing current through R_M. To avoid this R_M was displaced in the position shown in the sketch of Figure 4; in this manner its drop of magnetizing current over the range of low multiplier outputs nearly averages to zero in consecutive half-cycles. In particular, for any V_1, zero output is truly obtained when $V_2 = 0$. In the experimentation the rectified signal voltages were obtained from two variable transformers each feeding through a half-wave rectifier into a resistor R_{s1} (or R_{s2}) connected between ground and signal rectifier σ_{s1} (or σ_{s2}). (This is needed to provide a path for the pre-setting magnetizing currents flowing <u>against</u> the signal voltages.) In the experimental circuit R_{s1} and R_{s2} were chosen as $R_{s1} = R_{s2} = 2{,}000$ ohms. As a consequence at full output the power level of either signal source was about $\frac{1}{4}$ of the gross output power. Since it is generally desirable to reduce the overall signal power requirements, tests were also performed with $R_{s1} = R_{s2} = 10{,}000$ ohms, with results not too different from those shown in Figure 4, except for low values of V_2. (At low values of V_2 the wave form of v_{s2} was significantly distorted from the sinusoidal by the drop of magnetizing current). Also with $R_{s1} = R_{s2} = 2000$ ohms, voltage measurements directly at the transformer terminals corresponded substantially to the readings of the meters V_1 and V_2 across the resistors. This was no longer true for $R_{s1} = R_{s2} = 10{,}000$ ohms; in this case the experimental results plotted in terms of transformer voltages departed badly from linearity over the first 1/3 of the scale of the abscissae.

A more proper design of the circuit components would improve all this as the magnetizing currents (about $\pm$ 1 mA) could be reduced e.g. by the use of cores of lesser mean length (the available cores had more than twice the diameter needed to accomodate the windings used.) The voltage drops in question could also be made less significant percentwise by the use of higher gate and signal voltage levels, allowed by the core cross-section but limited in the experimentation by rectifier ratings. And larger power outputs could have been obtained from a reduction of R_M. But the circuit described, while performing the operations assigned remarkably well, is not primarily a power amplifier.

Nevertheless a variety of means are available to circumvent this question. The operation from low level signal sources can be made possible by means of input cathode followers. Also, if d.c. signal voltages (and square-waved gate voltages) are available no need is felt for the resistors R_{s1} and R_{s2} as the magnetizing current then can flow directly into the signal source.

Finally one may aim more directly at a reduction of the magnetizing currents in question. Since the magnetomotive force required by a core over intervals of increasing or decreasing fluxes is practically constant, it may not be difficult to provide a large part of it by an auxiliary winding fed from some suitable current source during pre-setting and pre-firing or more simply during pre-setting only. Procedures of this kind are mentioned in the References quoted.

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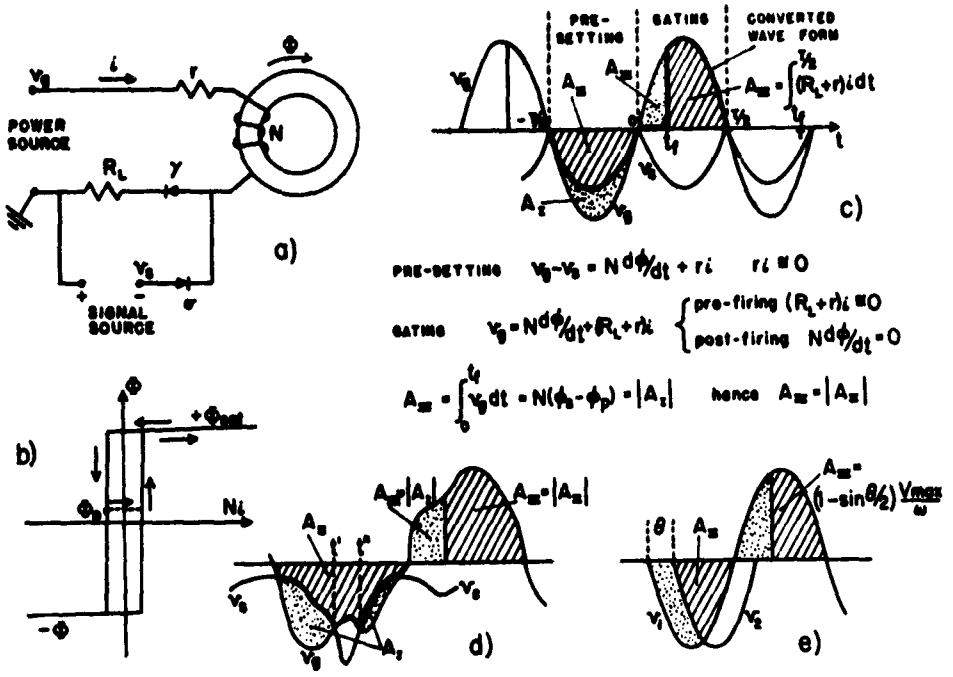


Figure 1. Elementary single-core amplifier

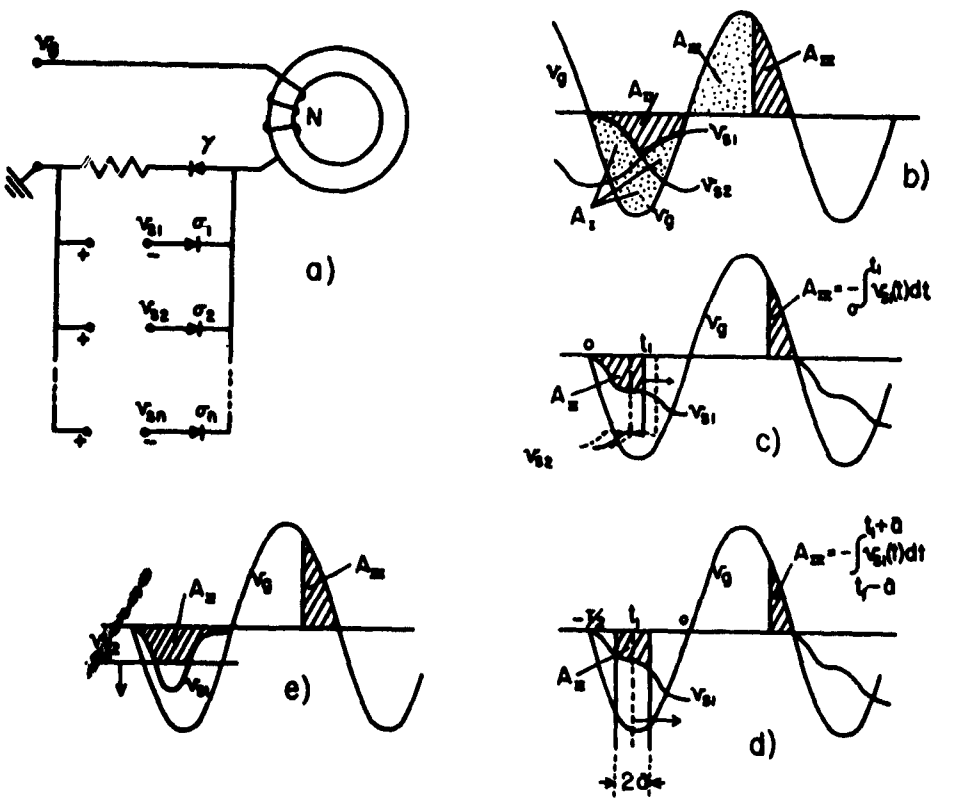
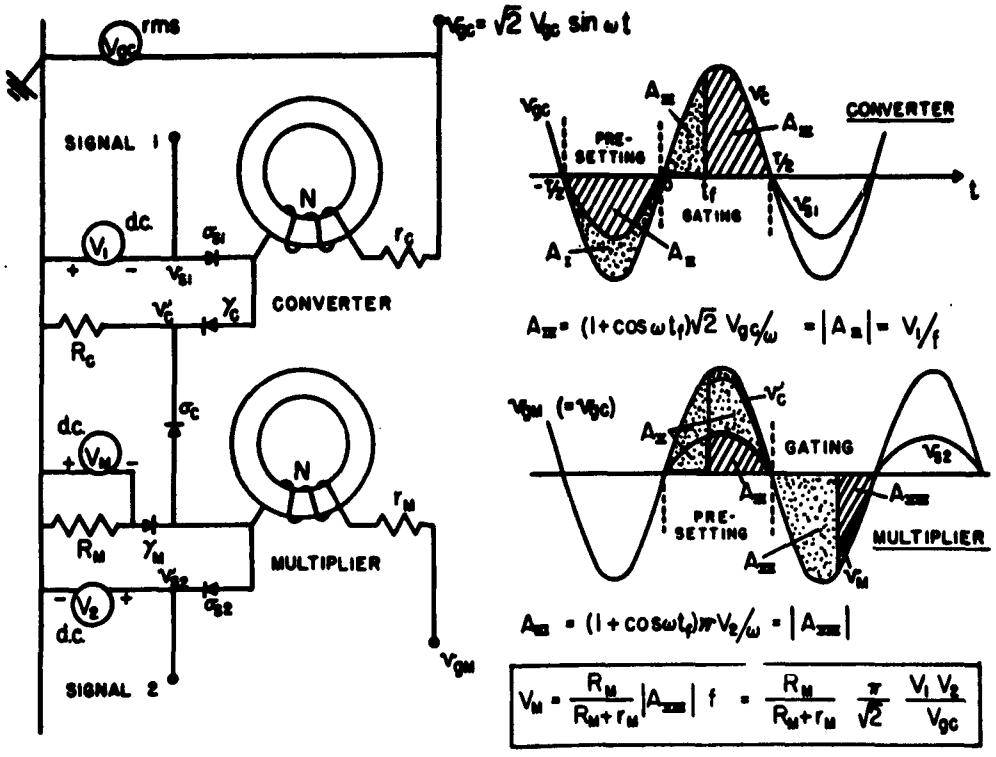


Figure 2. Multi-channel amplifier

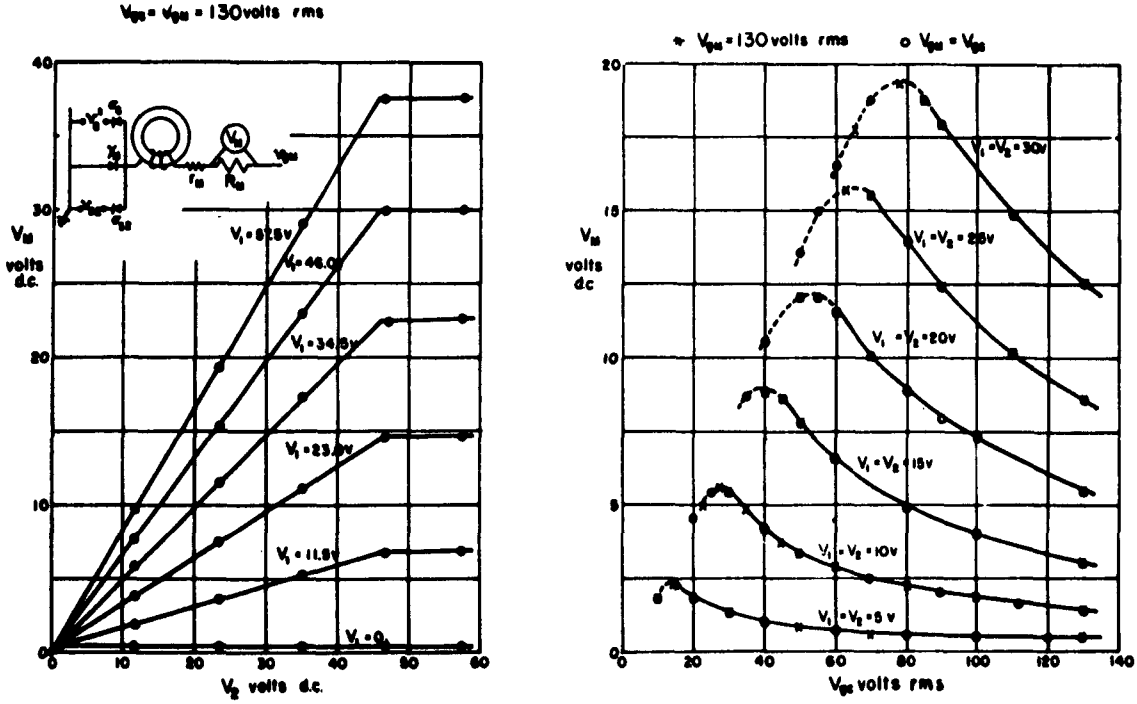


$$A_{II} = (1+\cos\omega t_f)\sqrt{2}\, V_{gc}/\omega = |A_I| = V_1/f$$

$$A_{III} = (1+\cos\omega t_f)\pi V_2/\omega = |A_{III}|$$

$$V_M = \frac{R_M}{R_M+r_M}|A_{III}|\, f = \frac{R_M}{R_M+r_M}\,\frac{\pi}{\sqrt{2}}\,\frac{V_1 V_2}{V_{gc}}$$

Figure 3. Basic multiplying circuit



$$V_M = K\,\frac{V_1 V_2}{V_{gc}}$$

Figure 4. Some experimental results