ENGINEERING SERVICES ON

TRANSISTORS

FOURTH INTERIM TECHNICAL REPORT

DATE OF THIS REPORT: 3 MAY 1961

PERIOD COVERED: JANUARY TO 3 MARCH 1961

Contract DA 36-039 sc-85352
U. S. Army Signal Research and Development Laboratories
Department of the Army Project Nos. 3A99-21-001-01/3G19-06-001-01

Prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company, Incorporated
120 Broadway, New York 5, N. Y.

ENGINEERING SERVICES ON TRANSISTORS FOURTH INTERIM TECHNICAL REPORT
CONTRACT DA 36-039 sc-85352

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U. S. Army Signal Research and Development Laboratories

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OBJECT

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report was prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company Incorporated
120 Broadway, New York 5, N. Y.

The following engineers and scientists participated in its preparation:

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SUMMARY OF STATUS

Work on this contract is a continuation of that carried out on Contract DA 36-039 sc-64618 and its predecessor contracts. As of this time, Tasks 2, 4 and 9 are active, and the work is summarized below. Tasks 1, 3, 5, 6 and 8 have been completed, as reported previously under the earlier contracts. Task 7 is now inactive by mutual agreement.

During the period covered by this report, 1 January to 3 March 1961, approximately 3000 engineering man hours were devoted to work on this project.

This contract was terminated as of 3 March 1961 but the work as outlined above will be continued on a new contract DA 36-039 sc-88962.

TASK 2 - TRANSISTOR RELIABILITY

Step-stress aging techniques are being applied to investigate the effects of various stresses on device reliability and to study in great detail the various modes of failure.

Work on both the fabrication of multiple diodes and the evaluation of their reliability is continuing. During this interval, aging studies have indicated the dominant importance of the encapsulation in determining the statistics of failure.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Work has continued on the M2260 germanium diffused base mesa transistor designed for a power output of 1 watt at 1 kmc. Effort has been concentrated on improving the stripe evaporation and alloying so as to obtain more uniform emitter penetration and more closely regulated surface geometry. Prototype units were assembled on a coaxial header and on a 3-pin single-ended header. No useful electrical results have been obtained as yet.

An M2107 transistor wafer was mounted on a modified TO-18 type header. Electrical measurements suggest that the structure is useable for common emitter circuitry up to at least 1000 mcps.

Theoretical studies have shown that careful measurement of collector current versus emitter-to-base voltage permit a simple calculation of the number of impurity atoms per unit area of base layer.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Work on the integrated logic gate is continuing. A structure consisting of a switching transistor and three computer diodes on a common substrate has been fabricated. In addition the individual diodes have also been fabricated using the same technology.

In conjunction with this program the storage time in epitaxial transistors has been analyzed. The storage time is much better understood and as a result it is a more easily designed parameter in epitaxial than in nonepitaxial transistors.

Preliminary results of step stress aging of multiple diodes have been completed and are reported under Task 2.

A base robbing effect in identical diffused base transistors which limit their use in DCTL has been recognized. An explanation is given which shows that the low α_I of these transistors leads to low logic gain or fanout.

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SECTION 1 - PURPOSE

The general purpose of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicality of their use in operating equipment. This contract is a successor to three preceding contracts of a similar nature: Contract W36-039 sc-44497, hereinafter referred to as the First Engineering Services Contract on Transistors; Contract DA 36-039 sc-5589, hereinafter referred to as the Second Engineering Services Contract on Transistors and Contract DA 36-039 sc-64618, hereinafter, referred to as the Third Engineering Services Contract on Transistors.

These contracts call for services, facilities, and material to be employed on mutually acceptable tasks. Of the nine tasks assigned, five have been completed. Task 1 involved the development of an oscillator of very low power drain; the Final Report on this task was issued on 1 June 1952. Task 3 covered a symposium on the circuit properties of transistors; the Final Report on this task was issued on 1 February 1952. Task 5 involved formulation of requirements for transistor test equipment and the fabrication of an experimental model: a final report on this task, dated 31 May 1960, was issued. Task 6 called for theoretical and experimental studies leading to the development of photocell blocks as set forth in the specifications for p-n junction photocells and photocell blocks (NRL Problem RO5.54); the Final Report on this task was issued on 31 January 1955. Task 7 covered studies and investigations of suitable miniaturized components for transistor circuit applications. It is now inactive by mutual agreement. Task 8 called for theoretical and exploratory work on Improved Crystal Rectifiers primarily intended for application to broadband microwave mixers. Since January 1957 work on this task has been carried on under Contract DA 36-039 sc-73224 and its successor DA 36-039 sc-85325. A resume of the earlier work appeared as an Addendum to the Tenth Interim Report on Contract DA 36-039 sc-5589 and was also included in the First Interim Report on Contract DA 36-039 sc-73224 dated 15 May 1957.

Tasks currently active under this contract are outlined below.

TASK 2 - TRANSISTOR RELIABILITY

The contract shall conduct a broad program in transistor reliability designed to accomplish the following objectives:

(a) Investigate quantitatively the factors governing stability of transistor and diode characteristics, e.g., the physics of semiconductor surfaces and films thereon.

(b) Study the application to practical devices of the knowledge obtained under (a) above.

(c) Refine criteria for determining stability of performance, e.g., improve test methods, establish relative importance of parameters in aging.

Work toward objectives (a) and (b) above involves investigation of the mechanism of formation, characteristics and application of protective silicon dioxide films on diodes and transistors. In connection with objective (c), the effects of variations of temperature and power dissipation stresses on the electrical characteristics of transistors and diodes are under investigation. Particular emphasis is placed on obtaining long-term predictions of stability from relatively small groups of units in relatively short times.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The contractor shall make theoretical and experimental studies leading to zero-order* exploratory development and, upon mutual agreement, to first-order* feasibility development of:

(a) New transistors using new or previously untried principles.

(b) New transistors obtained by studied modifications of existing types.

The new transistors shall be primarily intended and suitable for application to voltage, current, and power amplifiers, and to associated electronic transducers.

In general, transistors having ac amplifying properties in the following ranges are of interest:

(a) Germanium transistors from 100 mcps to 3000 mcps with as large power ratings as the state of the art permits.

(b) Silicon transistors from 10 mcps to 1000 mcps with as large power ratings and as high temperature ratings as the state of the art permits.

(c) Devices of other materials with specific attention to obtaining frequency, power, noise, or temperature advantages over germanium and silicon devices.

In particular, a germanium transistor of 25 to 50 mw power dissipation intended for service up to 3000 mcps is being developed. Another current specific objective is a transistor structure capable of one watt output at 1000 mcps with acceptable efficiency.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The contractor shall make theoretical and experimental studies leading to zero-order* exploratory development, and upon mutual agreement, to first-order* feasibility development and to second-order development of semiconductor components

* These terms are defined in the Final Report, Section 4, pages 5-6, Contract No. W-36-039-sc-44497, the First Engineering Services Contract on Transistors.

able to perform more complex functions than existing components can, thereby reducing the number of components needed in electronic systems with the ultimate objective of improving the reliability and reducing the cost of such systems. The components to be developed will include:

(a) Functional devices, namely devices designed from physical phenomena to perform as directly as possible desired systems functions.

(b) Integrated circuits, namely combinations of circuit elements, including, where appropriate, functional devices designed and fabricated as units to perform desired systems functions.

The work shall include:

(a) Evaluation of systems requirements and of possible components, with attention to such figures of merit as speed, gain, power dissipation, impedance, reliability, packing density, interconnection topology, etc.

(b) Evaluation of selected components as to universality with respect to a variety of systems.

(c) Fabrication of these selected exploratory components and determination of their measures of effectiveness.

Specific planned efforts include theoretical and experimental studies of the following integrated circuits and functional devices:

(1) Multiple diodes

(2) Multiple transistors

(3) Logic gates (diodes plus transistors)

(4) Flip-flops

(5) Turn-off gain p-n-p-n transistors.

Upon mutual agreement the Task may include second-order development, based on the information gathered in zero- and first-order development, applied to the design of one or more functional devices or integrated circuits. These components would be specific in the sense that they would be designed to perform selected systems functions useful in particular proposed types of systems. Particular attention would be given to the reproducibility and reliability of these components. Synthesis of complete systems from these components would not be part of this work.

This second-order development would include the gathering and writing of second-order design information and the supplying of 50 sample models of mutually agreed upon types.

SECTION 2 - ABSTRACT

TASK 2 - TRANSISTOR RELIABILITY

Chapter 1 discusses the effect of power and temperature step-stress aging on the 1N673 rectifier and the 1N669 voltage limiter diodes. The results suggest that for these devices, the primary accelerating stress is temperature with no significant aging due to either high field strength or high current density.

Chapter 2 reports step-stress aging studies with both temperature and power. The results indicate that the dominant cause of failure is related to the encapsulation rather than the wafer or the individual diodes.

Chapter 3 presents the correction factor for the effect of prior steps in a step-stress aging experiment. Curves are given for useful values of the various parameters so that this correction factor may be readily applied.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Fabrication of an M2107 transistor wafer on a modified TO-18 header is discussed in Chapter 4. Parasitic capacitance of the TO-18 and the standard coaxial header are nearly the same. Emitter lead inductance has not been measured for the TO-18 package. H parameter measurements indicate that electrical performance for common emitter service should be very similar to that obtained in the coaxial header.

Chapter 5 describes work on the M2260 germanium PNP diffused base mesa transistor designed for power output of 1 watt at 1 kmc. Prototype units have been assembled on a coaxial header and on a single-ended header. Included in the chapter are a description of the germanium processing and of the transistor structures together with a summary of initial measurements.

Chapter 6 describes how the number of impurity atoms per unit area base layer can be obtained from relatively simple electrical measurements.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The status of the integrated circuit program is discussed in detail in Chapter 7. Phase I of this work is concerned with the fabrication of standard general purpose modules (single and multiple arrays) to be used as basic building blocks for integration. The process of their fabrication using the limited diffusion technique producing oxide passivated devices is described and is shown to be applicable to various

types of diodes. Typical results are given on computer diodes demonstrating significant advantages in performance gained by using epitaxial silicon.

Progress is reported on Phase II of the program which is concerned with the integration of the low level logic gate. A process is described which has been developed and applied successfully for the fabrication of a switching transistor and three computer diodes on a common substrate.

The variation of storage time with circuit conditions is considered for both epitaxial and nonepitaxial diffused transistors. It is shown that the behavior of epitaxials is particularly simple and designable and that, in general, one measurement suffices for characterization. The complicated behavior of nonepitaxials is qualitatively explained.

An increase of saturated base voltage with increasing collector current in diffused-base transistors has been discovered which seriously impairs the use of these transistors in DCTL. This phenomenon is investigated and is found to be essentially concerned with inverse alpha. It is shown that the low α_I usually found in diffused-base transistors leads to severe base-robbing and resultant low fanout.

SECTION 3 - PUBLICATIONS AND REPORTS

During the period covered by this report, no publications or other reports were issued.

SECTION 4 - FACTUAL DATA

TASK 2 - TRANSISTOR RELIABILITY

Chapter 1

STEP-STRESS AGING OF SILICON DIODES WITH POWER AND TEMPERATURE

By G. A. Dodson and B. T. Howard

1.1 INTRODUCTION

In an earlier report (Ref. 1) some results, obtained by step-stress aging silicon diodes with both power and temperature as the stress, were presented. It is the purpose of this report to present some further results of power aging and to show the relationship between power and temperature which holds for the diodes which have been studied.

The discussion will fall into three main sections. First the results obtained by step-stress aging diodes with power in both the forward direction and the reverse breakdown region will be compared. Second, the relationship between the temperature of the diode and the applied power will be presented and lastly, the results of power and temperature aging will be compared.

1.2 POWER AGING

The silicon diodes in these experiments were IN669 voltage limiters with a power rating of 0.25 watts, obtained from the Western Electric Company. It should be mentioned here that this diode is identical in construction with the IN673 high voltage rectifier, used in the experiments to be discussed later, except for the starting resistivity of the silicon wafer used. The IN669 was used in the first experiment to facilitate reverse power aging. The specifications for both these devices and the failure criteria are shown in the Appendix.

Fig. 1 shows typical failure stress distributions obtained for the IN669 with d.c. power in the forward direction and also in the reverse breakdown region. The results obtained for two time intervals, 5 minutes and 1 day, are shown. It can be seen that the distributions are identical for both power conditions indicating that neither

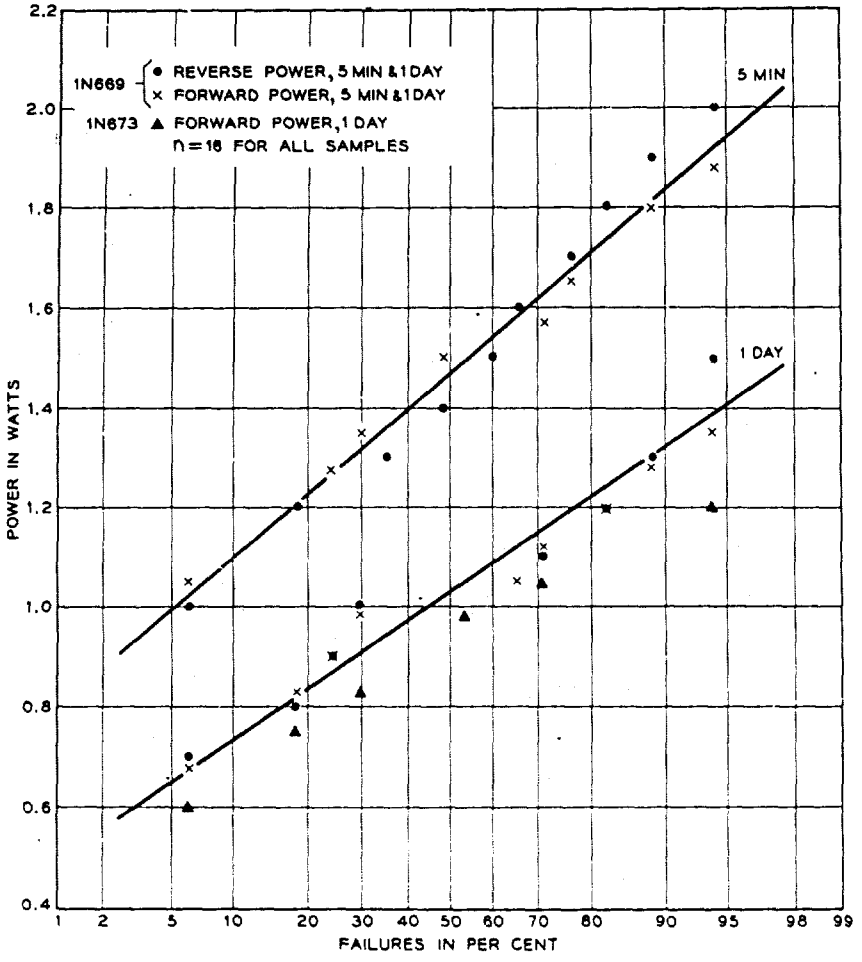

Fig. 1 - Failure distribution in power

the high current density in the forward aging condition nor the high field strength in the reverse power aging condition have a significant effect on the dominant failure mechanism in this case.

The failure stress distribution obtained with the IN673 rectifier under forward power conditions and a 1 day time interval is shown for comparison. As might be expected from the similarity of construction there is no significant difference between this distribution and that obtained with the IN669 under the same conditions. This similarity is seen further in Fig. 2 which shows the power acceleration curve obtained for both diodes.

Since these power aging experiments indicated that only the power level was important rather than the way in which the power was applied, it appeared likely that the significant effect of the power was to increase the temperature of the diodes. Thus it became important to determine the relationship between power and temperature so that aging results under these two conditions could be compared.

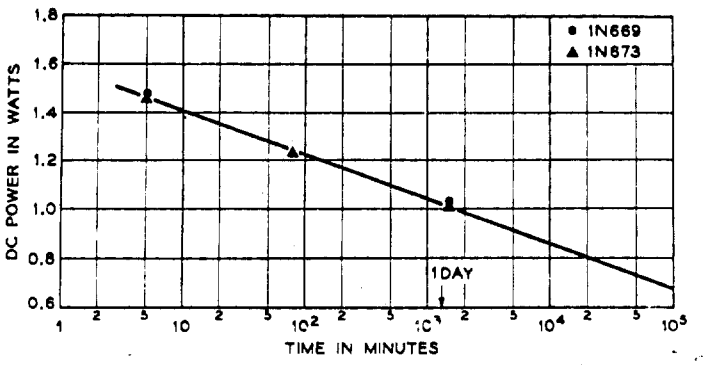

Fig. 2 - DC power acceleration curve
(50% failure)

1.3 POWER-TEMPERATURE RELATIONSHIP

The temperature rise caused by the application of power to these diodes was determined in two ways. First, the temperature of the encapsulation as a function of the applied power was measured by means of a small thermocouple which was attached to the base of the encapsulation. Second, the junction temperature was determined by a forward voltage technique. (Ref. 2).

The results of these two determinations are shown in Fig. 3 and can be seen to be essentially identical. This is not surprising since in these diodes the wafer is in excellent thermal contact with the encapsulation.

1.4 COMPARISON OF POWER AND TEMPERATURE AGING

The data shown in Fig. 3 was used to compare the results of step-stress aging the IN673 rectifier with power and oven temperature.

A typical comparison of failure stress distributions is shown in Fig. 4. The results of a forward power step-stress experiment have been converted to temperature and plotted with those of a temperature experiment having the same time interval. The two distributions can be seen to be essentially identical showing a good fit to a normal distribution with a mean of 1.90 and a standard deviation of 0.16 in units of reciprocal temperature ($10^3/T°K$).

The results indicate that the only effect of power is to raise the temperature of the diodes. This is reinforced by the data in Fig. 5 which shows the acceleration curve obtained with the median failure stresses of oven temperature experiments and of power experiments converted to temperature. The agreement can be seen to be excellent.

1.5 SUMMARY

Results of step-stress aging experiments in IN669 and IN673 silicon diodes have been presented to show that both forward and reverse power aging of these diodes has the same effect as aging with an equivalent temperature. This suggests that, in

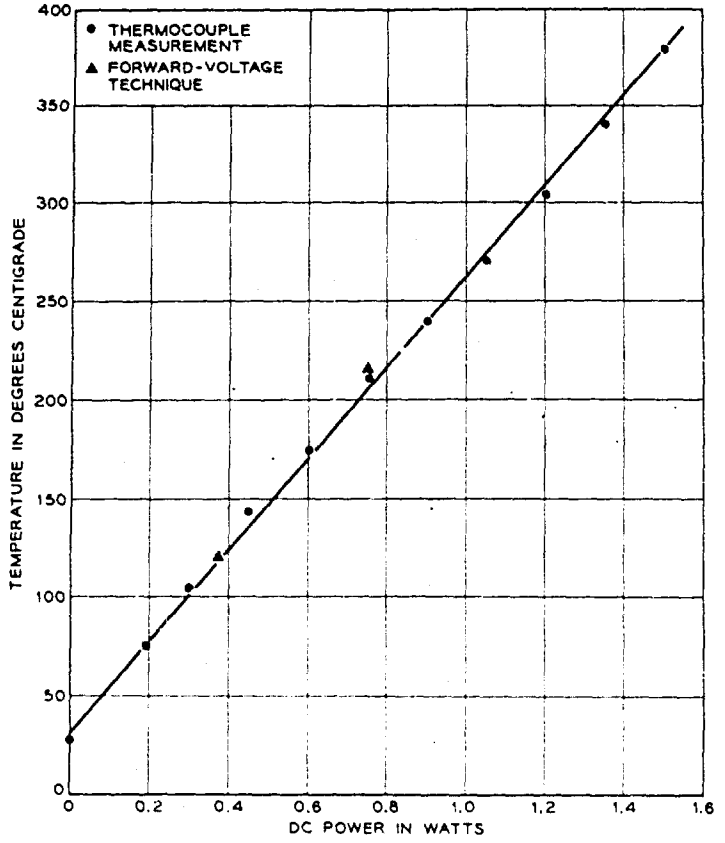

Fig. 3 - Temperature versus DC power

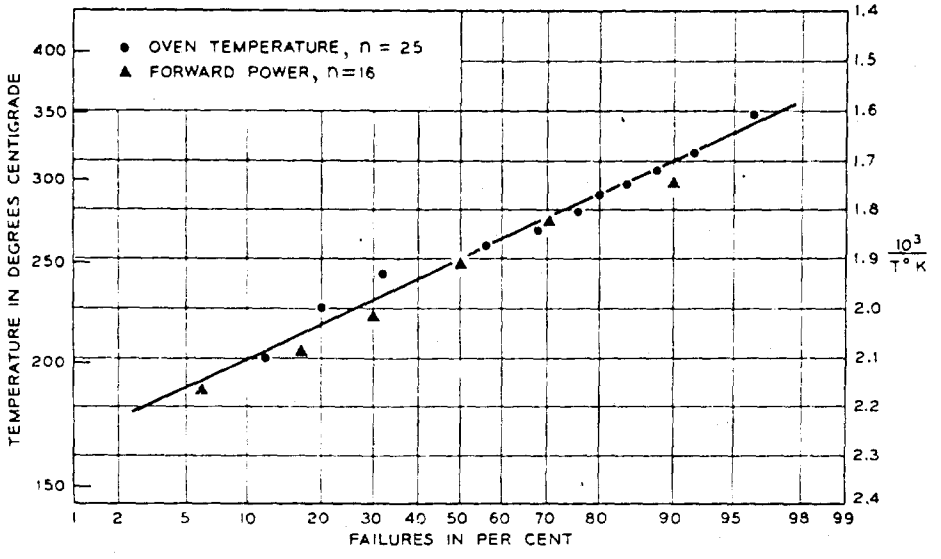

Fig. 4 - Failure distribution in stress, 1 day time interval

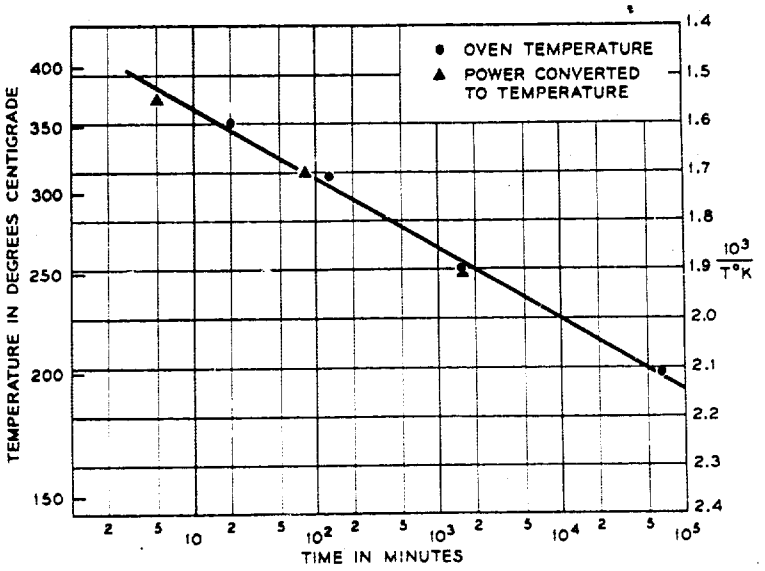

Fig. 5 - Temperature acceleration curve
(50% failure)

this case, the dominant failure mechanism may be accelerated by increasing temperature but is not significantly effected by either high field strength or high current density.

This in turn indicates that the devices are, at least initially, reasonably free of both ionic contamination and water vapor since it is well known that field effects can be observed under such circumstances. This, and other information, makes it necessary to state that while the results are true for the diodes studied they may be, by no means, regarded as universal. In fact, work is continuing to study the relationship between power and temperature aging on other devices, possibly with other failure mechanisms, which may well show singular electrical effects.

However, the equivalence of electrical and temperature aging, wherever it can be established, is obviously of importance because of the resultant possible economy in reliability testing and because of the information this equivalence gives about the dominant failure mechanisms.

APPENDIX

IN669

Specifications

	Min.	Max.
VB (at 2.0 ma.)	24.3 v.	29.7 v.
I_r (at 21.5 v.)	-	0.5 μa
V_f (at 250 ma.)	-	1.0 v.

Failure Criteria

I_r (at 20.0 v.) $\geq$ 1.0 μa

IN673

Specifications

	Min.	Max.
VB (at 10 μa)	350.0 v.	-
I_r (at 300 v.)	-	1 μa
V_f (at 250 ma.)	-	1.0 v.

Failure Criteria

I_r (at 300 v.) $\geq$ 1 μa

REFERENCES

1. Howard, B. T. and Dodson, G. A., Second Interim Technical Report on Transistors, DA 36-039 sc-85352, 30 November 1960, Chapter 2.
2. Lin, H. G. and Crosby, R. E., Jr., "A Determination of Thermal Resistance of Silicon Junction Devices." 1957 IRE National Convention Record, pt. 3., pp 22-25.

Chapter 2

A PRELIMINARY REPORT ON THE ACCELERATED AGING OF MULTIPLE DIODES

By B. T. Howard and W. F. J. Hare

2.1 INTRODUCTION

One of the most important questions to be answered concerning the reliability of multiple devices, or integrated circuits, placed in a single encapsulation is that of the existence of a correlation between the failure of the individual devices. In other words, will the devices inside a single encapsulation essentially fail together or will they fail essentially independently as in the case of separate encapsulations. The answer to this question obviously concerns the origin of the cause of failure. If failure mechanisms originate from the encapsulation or can travel freely between wafers we would expect to find a correlation between failure of the individual wafers, whereas if the failure mechanism is confined to the individual devices we would expect no such correlation.

A simple method of investigating this problem consists of first subjecting the multiple devices to aging experiments in which the stress is applied simultaneously to the encapsulation and to all the devices; in addition experiments are carried out in which individual devices within the encapsulation are stressed separately. This preliminary report will describe the results of such experiments. It will be shown that the dominant cause of failure is associated with the complete encapsulation, and applies to all devices within it.

2.2 EXPERIMENTAL TECHNIQUE

The multiple diodes used in these experiments have been described by R. W. MacDonald in an earlier report (Ref. 1). Ordinarily batches of sixteen multiple diodes, each containing six devices, were used in each experiment.

The aging experiments themselves were of two kinds:

(1) Temperature aging: The devices were aged at elevated temperatures in an oven in those experiments where it was desired to stress the encapsulation and all the diodes simultaneously. Both step-stress and fixed stress (Ref. 2) experiments were carried out.

(2) Power aging: Where it was desired to stress individual devices a single diode was stressed by applying power in the forward direction. All diodes were monitored during the test. In this case, the step-stress technique was used.

2.3 EXPERIMENTAL RESULTS

Failure criteria: In all experiments the following two failure criteria were used:

(a) Reverse current at 40 volts exceeding 20 mμA.

(b) Breakdown voltage at 1 μA decreasing by more than 2 volts.

Temperature aging:

(1) Single wafer experiments: In the first experiment, fifteen cans, each containing six diodes, were used in a temperature step-stress experiment with a 24 hour time interval and a temperature step of 0.05 in units of $10^3/T(^\circ K)$. The distribution of failure temperatures for diodes within a single encapsulation was characterized by a median and a range. The distribution of the median temperature of failure is shown in Fig. 6 and can be seen to fit well to a normal distribution with a mean value of 1.68 and a standard deviation of 0.10, both in units of reciprocal temperature. The median of the ranges for individual encapsulation was 0.05, or one temperature step, and in fact in 40 per cent of the encapsulations, all six diodes failed simultaneously. This strong correlation is clearly evident in Fig. 7 where the medians and ranges have been plotted on a standard control chart. The data is definitely not randomly distributed; since the spread within a can is much less than the spread between cans, there is a much stronger correlation for the failure of diodes within an encapsulation than between encapsulations.

The second experiment may be regarded as a companion to the first and was carried out to ensure that similar results would be obtained under fixed stress conditions. In this experiment, sixteen multiple diodes were aged under a constant stress of 300° C. The distribution of the medians is shown in Fig. 8 and can be seen to be a good fit to a log-normal distribution, with a mean of 820 hours and a standard deviation of a ratio of 2.0. The median range for individual encapsulations was a ratio of 1.5 and again 40 per cent of the encapsulations showed all six diodes failing

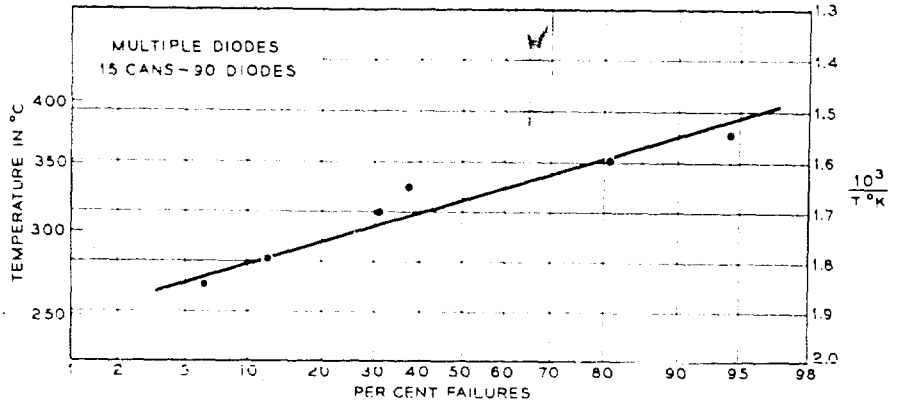

Fig. 6 – Failure stress distribution at oven temperature. time interval 1 day

simultaneously. Thus the same strong correlation between diode failures in a single encapsulation is observed under constant stress conditions.

(2) Double wafer experiments: The correlation observed in the preceding exriments could result from three situations:

(a) a dominant failure mechanism being associated with the encapsulation processing,

(b) a dominant failure mechanism associated with earlier processing steps which are common to all the diode mesas on the wafer (e.g. the wet chemical etching and cleaning), or

(c) a failure mechanism due to a single contaminated diode, provided the contamination is volatile and can spread to the other wafers during, or after, the assembly process (consideration of this case will be postponed until the discussion of power aging experiments).

To determine which of these alternatives was correct, an experiment was carried out in which two multiple diode wafers were placed in a single encapsulation. These two wafers would thus have only the encapsulation in common and hence a correlation between their failure levels would indicate that it was the encapsulation and its associated processing which was dominant.

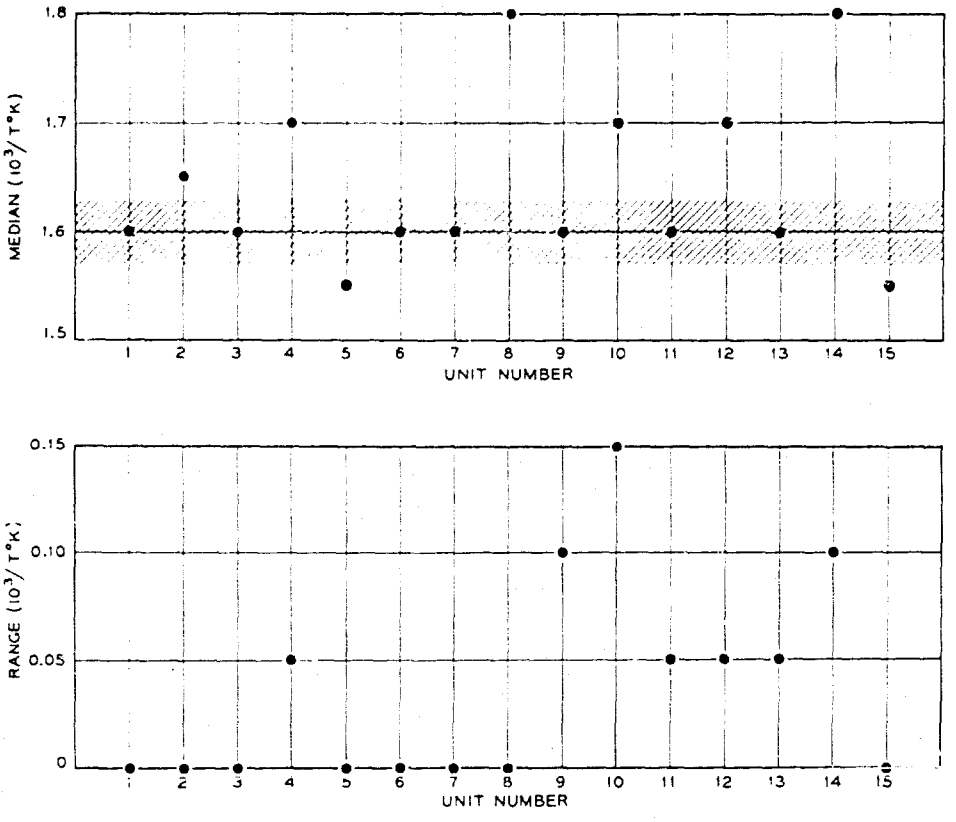

Fig. 7 - Control chart showing medium and range of failure stresses for diodes in a single encapsulation; stress = temperature, time interval 1 day

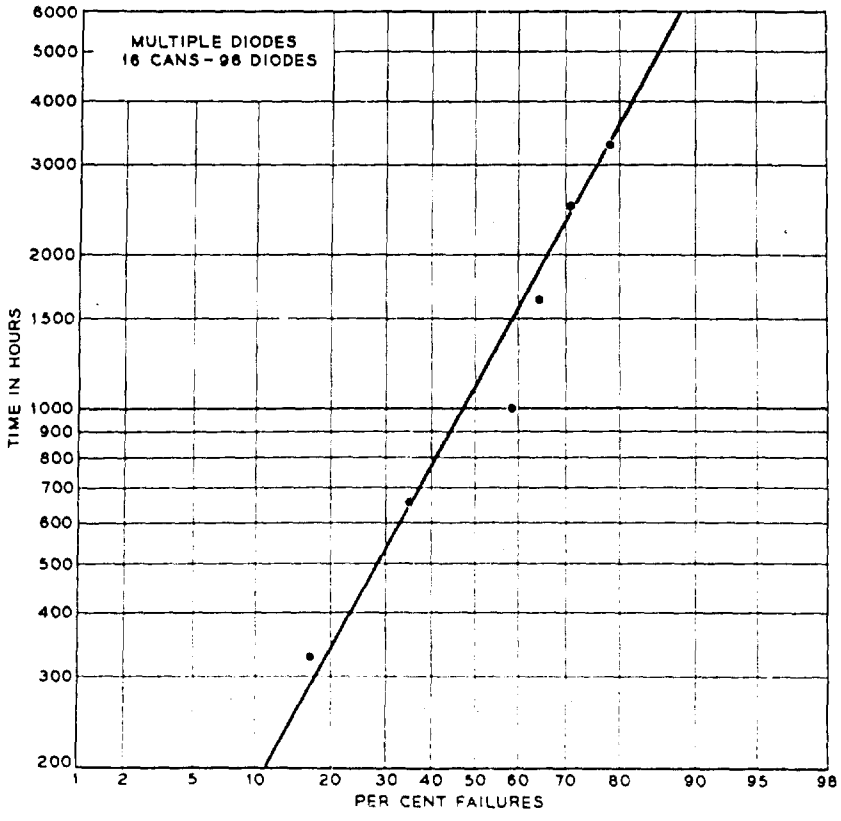

Fig. 8 - Failure distribution in time, stress = 300°C.

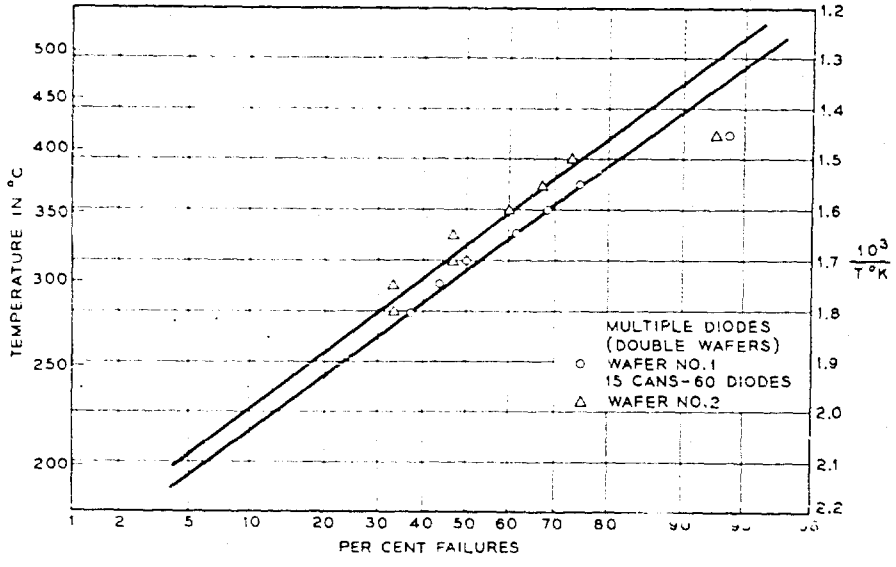

Fig. 9 - Failure stress distribution at oven temperature, double wafer, time interval 1 day

In this experiment, fifteen packages with two multiple diode wafers of four diodes each, were used in a temperature step-stress experiment with a 24 hour time interval and a temperature step of 0.05 in units of $10^3/T(^\circ K)$. The results for each wafer in the encapsulation were characterized, as before, by a median and a range, and the difference between the two wafer medians was also recorded. The distributions for the medians of the two wafers are shown in Fig. 9 and can be seen to be essentially identical with a mean of 1.68 and a standard deviation of 0.19 in units of reciprocal temperature. The median range for wafer #1 is 0.05 and for wafer #2 is 0.06; in both cases approximately 50 per cent of the wafers showed all diodes failing simultaneously. Lastly, 53 per cent of the encapsulations showed both wafers failing simultaneously (i.e. a difference between the median values of 0) and only 13 per cent showed a significant difference.

These results indicate that the mechanism dominant in causing failure is associated with the complete encapsulation.

Power aging: In this experiment sixteen multiple units of six diodes each were used in a forward power step-stress experiment with a 24 hour time interval and power steps of 200 mw. The experiment consisted of three parts:

(1) A single diode in each encapsulation was aged to failure while the remainder were monitored. The failure distribution of the stressed diodes was obtained.

(2) This procedure was repeated using one of the surviving diodes in each encapsulation.

(3) The procedure was repeated once more.

The failure distributions for all three cases is shown in Fig. 10. It can be seen that there is no significant difference between the three distributions, all of which reasonably correspond to a normal distribution with a mean of 2 watts and a standard deviation of 0.2 watts. This, coupled with the fact that in only 4 per cent of the cases was any other diode significantly degraded by the failure of the stressed diodes, shows that the failure of one diode in the encapsulation does not significantly affect another under these circumstances; i.e. no volatile contaminant is being evolved from the stressed diode. This fact eliminates the third possibility proposed earlier. It is of interest to note that an autopsy showed that in almost all cases the stressed diodes failed by alloying of the gold contact on the mesa. This result can be contrasted with the temperature aging results which show that, when the encapsulation as a whole is heated, failure occurs below this eutectic temperature of 373° C. Clearly, contamination from the enclosure rather than from the diodes is responsible for failures at elevated temperatures.

2.4 SUMMARY

The results of accelerated aging experiments on multiple diodes have shown:

(1) Under temperature stress all the diodes within a single encapsulation tend to fail together. This has been shown to be due to the encapsulation and its associated processing rather than earlier processing common to all the diodes. This suggests that the failure is due to the generation of volatile contamination from the encapsulation.

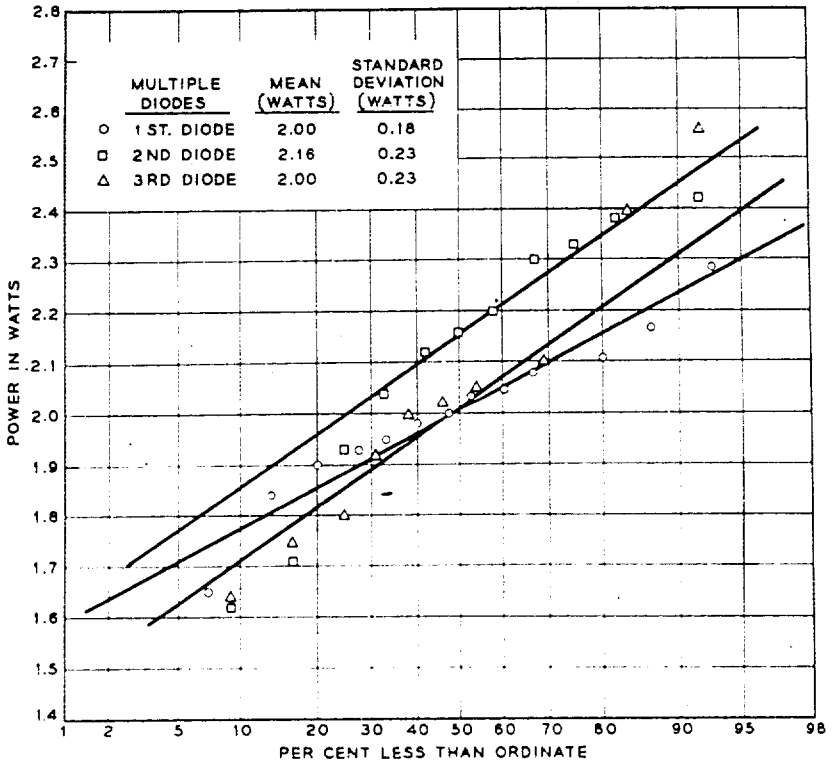

Fig. 10 - Failure distribution, forward power

(2) When individual diodes are subjected to power stress, they fail due to alloying of the contacts without significantly degrading the remaining diodes in the encapsulation. This suggests that there is, effectively, no volatile contamination on the wafer.

The generalization of these results to integrated circuits is not simple but they do indicate that two different kinds of failure may be expected, depending upon the nature of the stress applied. First, where the stress is common to the whole integrated circuit and encapsulation, all elements may fail together, and second, where the stress is localized to a single element of the integrated circuit, it may fail without affecting the remainder. This obviously will have significant bearing on the design of integrated circuits, particularly on the question of redundancy inside a single encapsulation.

Work is continuing to test these conclusions and to obtain a more definite evaluation of the reliability of the multiple diodes.

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1. E. G. Walsh, Second Interim Technical Report on Transistors, Contract DA 36-039 sc-85352, 30 November 1960, Chapter 10.

2. B. T. Howard and G. A. Dodson, Second Interim Technical Report on Transistors, Contract DA 36-039 sc-85352, 30 November 1960, Chapter 2.

Chapter 3

A CORRECTION FACTOR FOR TEMPERATURE STEP-STRESS AGING TO FAILURE

By Mrs. A. J. Siuta

3.1 INTRODUCTION

A new approach to aging test, step-stress aging, has been discussed in earlier reports (Ref. 1, 2).

This technique of stepping stress until failure occurs is, in the simplest case, used assuming that all previously applied stress steps have not caused any appreciable aging. This assumption is not always true, and it may be necessary, therefore, to correct the stress level data to account for the effect of prior stress levels during step-stress aging. This report will discuss the correction for temperature accelerated aging experiments only.

3.2 ACCELERATION CURVE

The primary objective of the accelerated aging experiment is to procure an acceleration curve; i.e., a plot of mean device life as a function of the stress level to which a device has been subjected.

The acceleration curve correlating temperature and time to failure is described by the following relationship (Ref. 3):

$$t = Ce^{B/T}$$

where t is aging time; C is a number representing the amount of aging; T is temperature in degrees absolute; and B is obtained from the following:

$$B = \frac{q(eV)}{k}$$

where q is the electron charge in Coulombs; (eV) is the activation energy in electron-volts; and k is the Boltzmann constant in joule degrees^{-1}.

3.3 TEMPERATURE STRESS STEPS

In the instance of equal 1/T (the reciprocal of temperature in degrees absolute) steps for temperature, the effect of the previously applied stress steps is a strong function of the activation energy of the acceleration curve and the size of the stress steps, and is also dependent, to a smaller degree, on the total number of preceding stress steps.

The "effective temperature"* for the n^{th} stress step is defined by the relationship

$$(1/T)_{n_{Eff}} = (1/T)_n - (\Delta 1/T)_n$$

where $(1/T)_{n_{Eff}}$ is the reciprocal of the effective absolute temperature for the n^{th} step; $(1/T)_n$ is the reciprocal of the absolute temperature for the n^{th} step; and $(\Delta 1/T)_n$ is the correction to be made on the n^{th} step for the n-1 previous stress steps.

The accelerated aging experiment is designed such that the aging time intervals between successive stress steps are equal:

$$t_1 = t_2 = t_3 = \ldots = t_n = t_{n_{Eff}}.$$

The size of the successive stress steps (δ) are also equal:

$$\delta = \frac{1}{T_{(n-1)}} - \frac{1}{T_n} .$$

In this case, where the stress steps are equal in units of 1/T, the expression for $(\Delta 1/T)_n$ is given by the following equation:

$$(\Delta 1/T)_n = \frac{1}{B} \log_e \left[\frac{1 - e^{-nB\delta}}{1 - e^{-B\delta}} \right]$$

where δ is the size of the equal 1/T stress steps; n is the number of stress steps; and B has the same meaning as before.

* That temperature which would produce the accumulated aging effect of n stress steps if applied once for the given time interval.

3.4 FIGURES AND TABLE

The following figures have been included to assist in determining $(\Delta 1/T)_n$ for the following activation energies and stress step sizes:

Fig.	Activation Energy (in eV)	Stress Step Size (in $1/T^\circ K$)
11	0.7 through 2.0	0.025×10^{-3}
12	0.7 through 2.0	0.05×10^{-3}
13	0.7 through 2.0	0.10×10^{-3}

A table has also been added which gives temperatures in degrees centigrade corresponding to equal stress steps of $0.05 \times 10^{-3}/T^\circ K$.

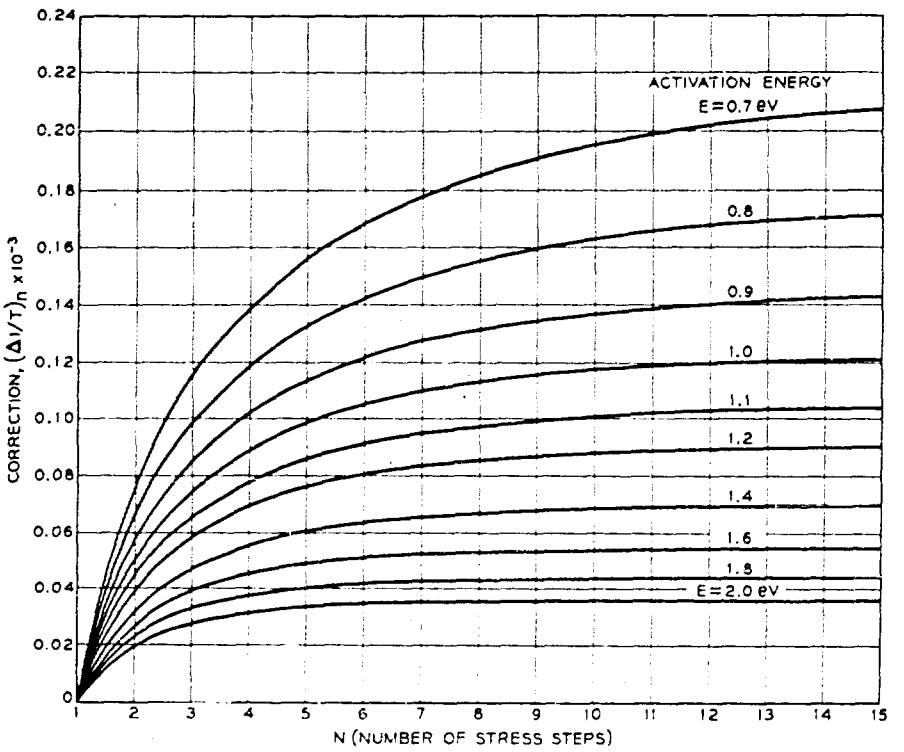

Fig. 11 - Correction factor as a function of number of stress steps for a step size of 0.025 ($10^{-3}/T^\circ K$)

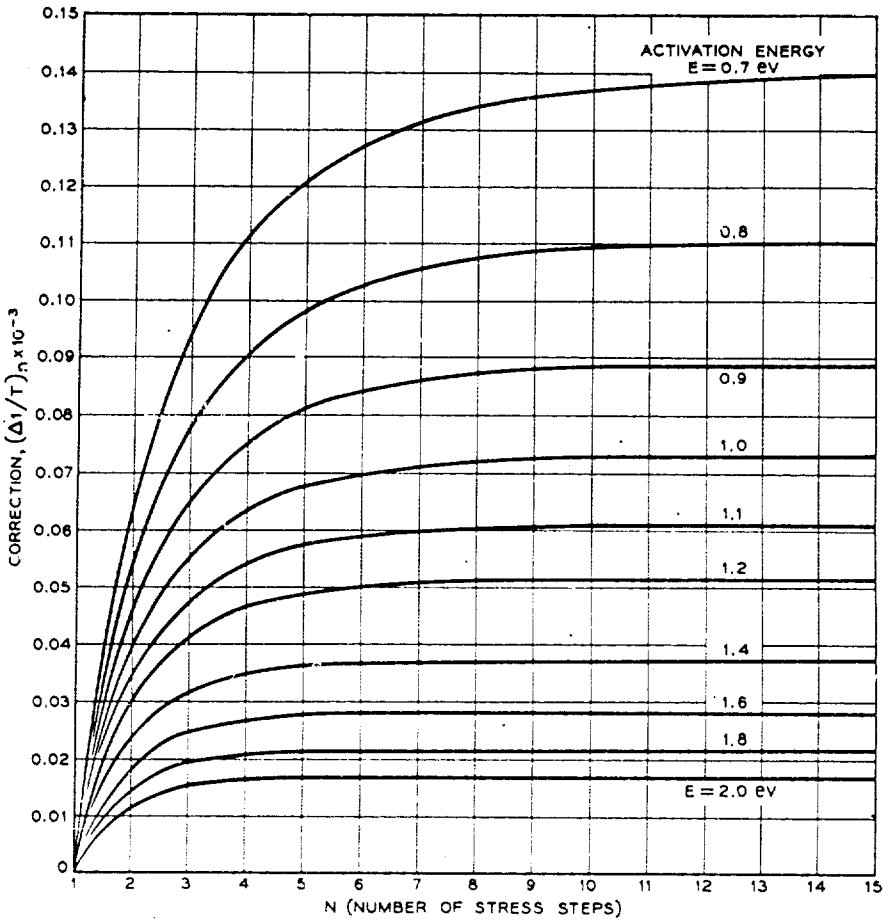

Fig. 12 - Correction factor as a function of number of stress steps for a step size of 0.05 ($10^{-3}/T°K$) activation energy

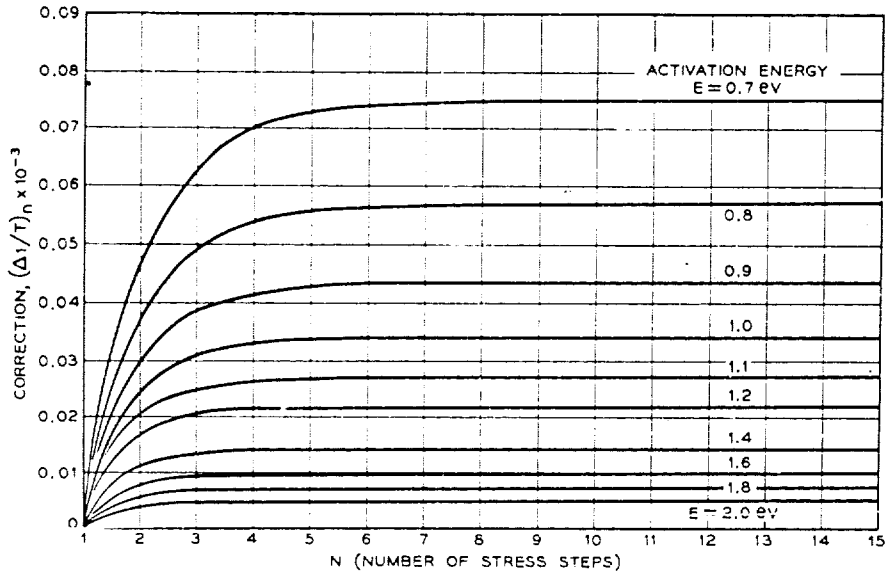

Fig. 13 - Correction factor as a function of number of stress steps for a step size of 0.10 ($10^{-3}/T°K$)

Table 3-1

Equal 0.05 x $\frac{10^{-3}}{T^{\circ}K}$ Stress Steps

T°C	$\frac{10^3}{T^{\circ}K}$	T°C	$\frac{10^3}{T^{\circ}K}$
26	3.35	192	2.15
30	3.30	203	2.10
35	3.25	215	2.05
39.5	3.20	227	2.00
44	3.15	240	1.95
50	3.10	253	1.90
55	3.05	268	1.85
60	3.00	283	1.80
66	2.95	298	1.75
72	2.90	315	1.70
78	2.85	333	1.65
84	2.80	352	1.60
91	2.75	372	1.55
97	2.70	394	1.50
104	2.65	417	1.45
112	2.60	441	1.40
119	2.55	468	1.35
127	2.50	496	1.30
135	2.45	527	1.25
144	2.40	560	1.20
153	2.35	597	1.15
162	2.30	636	1.10
171	2.25	679	1.05
182	2.20	727	1.00

3.5 SUMMARY

A correction factor, to account for the effect of step-stress aging prior to the stress step at failure, is given for the case of equal 1/T (the reciprocal of temperature in degrees absolute) temperature steps.

Three figures have been added to aid in determining the correction factor for several practical activation energies and stress step sizes. A table has also been attached correlating equal $0.05 \times 10^{-3}/T^{\circ}K$ stress steps and temperatures in degrees centigrade.

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1. B. T. Howard and G. A. Dodson, Second Interim Technical Report, Contract DA 36-039 sc-85352, 30 November 1960, Chapter 2.

2. G. A. Dodson, Third Interim Technical Report, Contract DA 36-039 sc-85352, 28 February 1961, Chapter 2.

3. G. A. Dodson and B. T. Howard, "High Stress Aging to Failure of Semiconductor Devices", Seventh National Symposium on Reliability and Quality Control.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 4

STATUS OF THE MICROWAVE GERMANIUM TRANSISTOR

By A. G. Foyt

4.1 INTRODUCTION

During the past quarter an M2107 transistor wafer was mounted on a modified TO-18 type header. This report describes the physical structure of this transistor and some simple electrical measurements on it. The measurements indicate that this modified header is suitable for use up to at least 1000 mcps.

4.2 DESCRIPTION OF THE HEADER

Fig. 14 shows a TO-18 header as modified for mounting of an M2107. In this structure the emitter has been fastened to the TO-18 shell. The transistor wafer is mounted on the collector lead as in the M2107, and the base is connected to a lead diametrically opposite to the collector lead.

To achieve low inductance in the emitter lead, a wire bridge has been brought from the ground shell, which is used as the emitter return, to as near the germanium wafer as possible. The 0.2 mil diameter wire that is normally bonded to the emitter stripe is connected to this wire bridge.

To achieve low inductance in the base lead, the input pin is bent as close to the germanium wafer as possible. The end of this pin is flattened in the plane of the wafer, and the 0.2 mil diameter wire bonded to the base stripes is connected to this flat.

As indicated in Fig. 14, the germanium wafer is bonded directly to the collector pin. The other pair of diametrically opposite pins are shorted to the transistor shell and employed as emitter leads. These two leads, in combination with the transistor shell and suitable external circuit shields, should provide adequate electrical and magnetic shielding between collector lead and base lead.

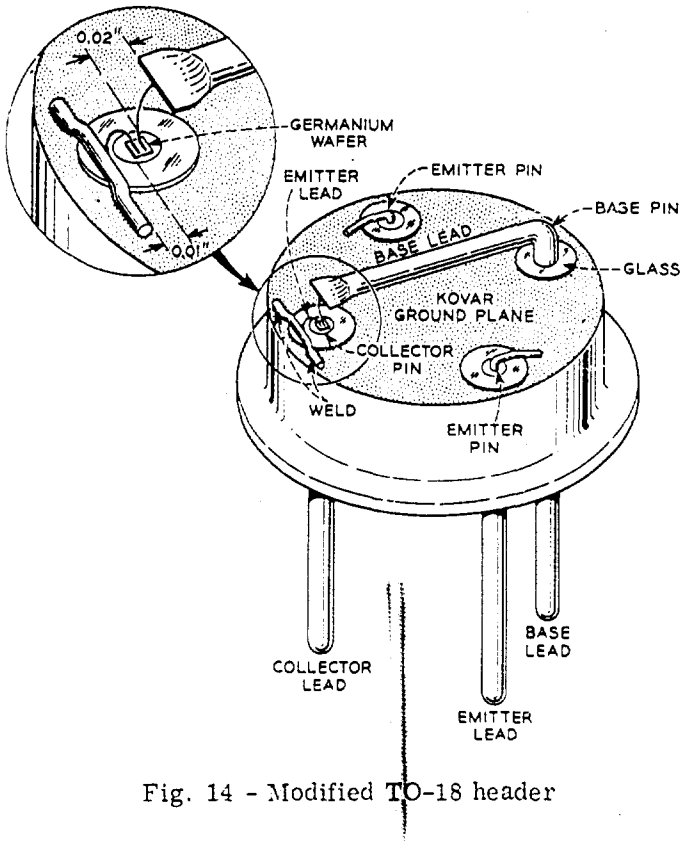

Fig. 14 - Modified TO-18 header

Table 4-1

	Modified TO-18 Header	Standard Coaxial Header
C_{EC}	0.50 pf	0.75 pf
C_{EB}	0.66 pf	0.55 pf
C_{BC}	0.016 pf	0.015 pf

4.3 ELECTRICAL MEASUREMENTS

The inter-pin capacitances of the header alone were measured with a Boonton 74-C Capacitance Bridge. Table 4-1 gives these data, together with the inter-pin capacitances of the standard coaxial header.

The feed-through capacitance C_{BC} is seen to be substantially the same for the two headers while input capacitance C_{EB} is somewhat increased in the TO-18 and output capacitance C_{EC} is somewhat decreased. No attempt has been made as yet to determine the emitter lead capacitance. It is believed that this is not much larger in the TO-18 than in the standard coaxial package.

A standard M2107 wafer mounted on this header had h-parameters which were very similar to those of coaxially mounted transistors. The f_T of the unit was approximately 2.0 kmcps as was expected for the base layer thickness and epitaxial layer thickness. The variation of the h-parameters with frequency showed no important differences between this unit and units made on the standard coaxial header.

4.4 CONCLUSIONS

Measurement of the inter-pin capacitances and of h-parameters of finished transistors suggests that a modified TO-18 type header is as suitable for the M2107 transistor as the standard coaxial header.

Chapter 5

STATUS OF THE M2260, A ONE WATT, 1 KMC TRANSISTOR

By A. G. Foyt

5.1 INTRODUCTION

The M2260 is to be a germanium pnp diffused-base mesa transistor with a power output of one watt at 1 kmc. During the past quarter, effort has been concentrated on improving the stripe evaporation and alloying to improve the surface geometry and obtain more uniform penetration. Prototype units were assembled on the coaxial header and a 3 pin single ended header. This report includes description of the germanium processing, a description of transistors, and a summary of measurements for the two transistors.

5.2 GERMANIUM PROCESSING

The first wafer processed was a 4 mil slice of p^+ (0.001 Ω-cm) germanium with a 2.4 micron layer of epitaxially grown germanium on the surface. The breakdown voltage of the wafer was about 30 volts.

The base layer was diffused into the epi layer to a depth of 1/2 micron. Its sheet resistance was 230 ohms/square. The surface concentration of the base impurity was 10^{18} atoms/cc. Diffusion processes have been unchanged during this quarter.

Emitter and base stripes were evaporated and alloyed. A stripe spacing of 0.2 mil has been achieved. The alloying was carried out such that there was very little change in surface contour, as shown in Fig. 15. Interference fringes over the stripes are straight, indicating no balling up of the alloying material while in a liquid phase. This results in a substantially more uniform base thickness after alloying with less loss from alloying through the base layer.

In order to determine the penetration of the emitter into the base layer, I_c was measured as a function of V_{EB}. This determines the doping of the base layer under the emitter and gives an estimate of the emitter penetration. (See Chapter 5 of this report for a description of this method.) For this wafer, the doping under the emitter was about 10^{12} atoms/cm^2, indicating an emitter penetration of about 0.1 microns. Fig. 16 is a cross section of the completed wafer. The common base DC collector characteristics are shown in Fig. 17.

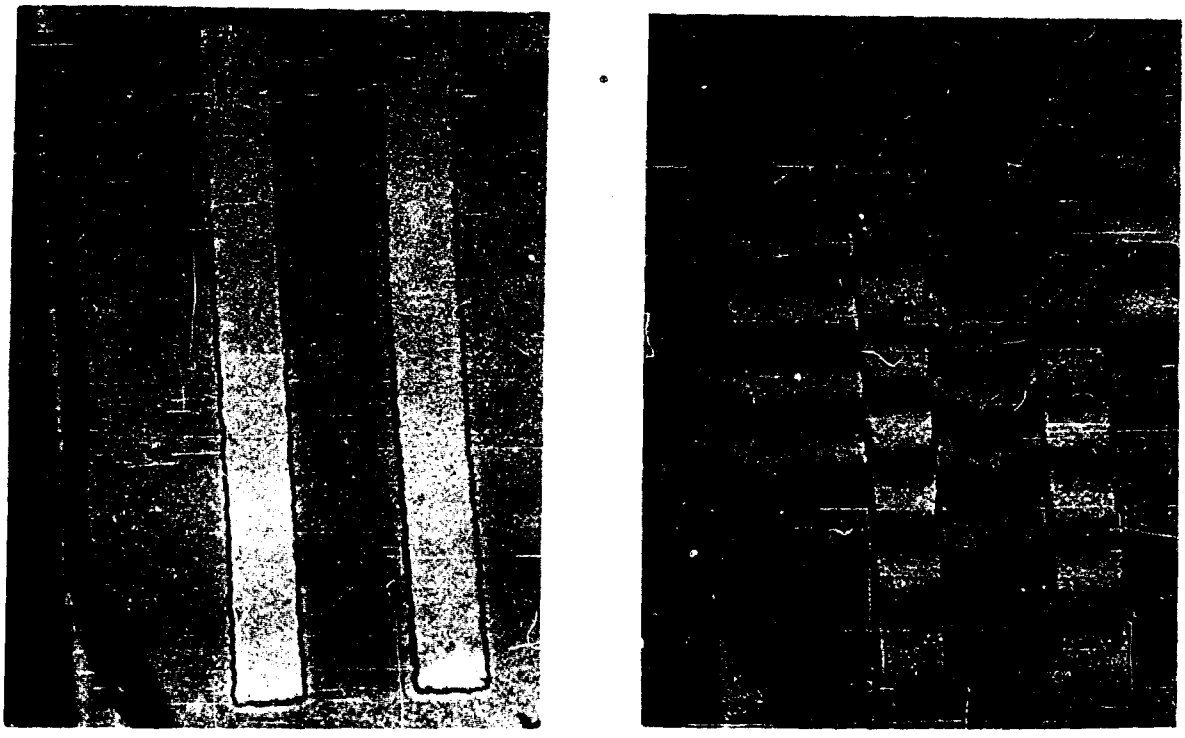

Fig. 15 - Photographs of alloyed emitter and base stripes

5.3 ELECTRICAL PERFORMANCE OF ONE UNIT WITH COLLECTOR ELECTRICALLY CONNECTED TO THE HEAT SINK

To explore the possibilities of making this transistor with the collector electrically connected to the heat sink, one model was made on a conventional power header with leads altered to minimize inductance. Two types of measurements were made on this unit. These were:

(1) Common Base power insertion gain, at one kmc, in a tuned amplifier.

(2) Common Emitter h parameters at frequencies from 300 to 900 mc.

T' is unit had power loss at all bias points in the common base amplifier. The h parameters were measured to determine the cause of the power loss. (See Figs. 18, 19, 20).

The following conclusions were reached on the basis of the h parameters:

(1) f_T is probably between 1200 and 1500 mc for this wafer.

(2) Reverse Transmission, probably due to capacity in the header, is much too large.

It appears from the h parameters that the cause of the power loss is probably reverse transmission which is caused by header capacity, and that this header will not be suitable for this transistor. However, h_{21} does indicate an f_T for the wafer of about 1.5 kmc which would make the germanium wafer suitable for this unit.

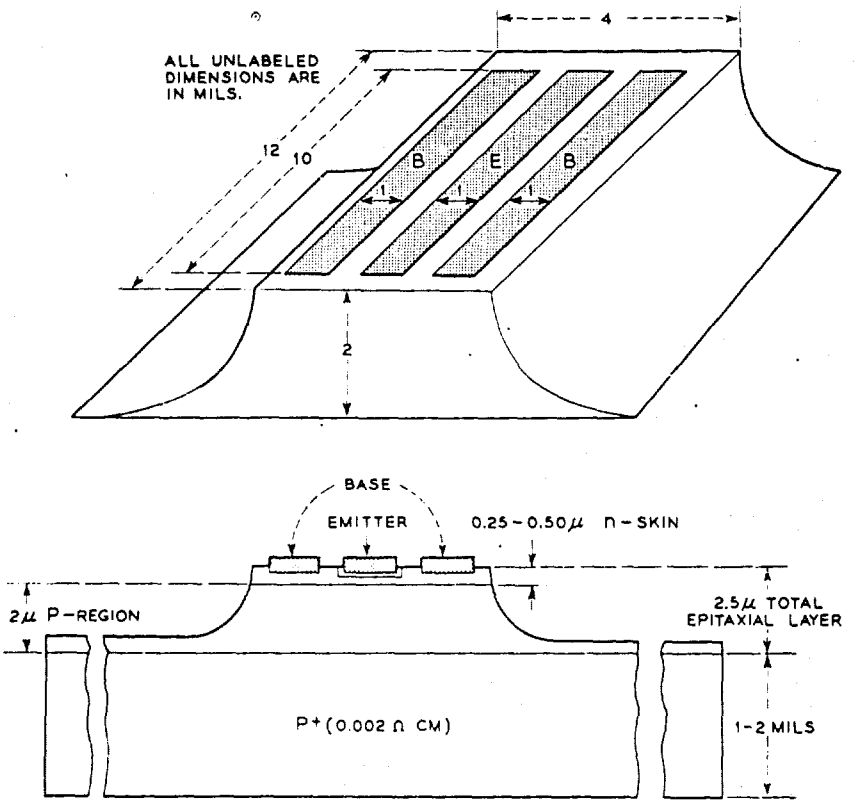

Fig. 16 - The germanium wafer

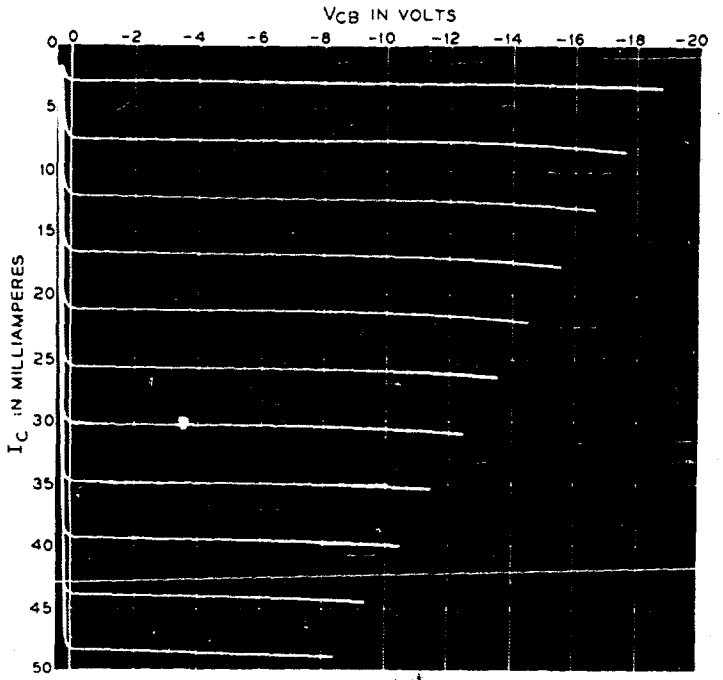

Fig. 17 - Common base collector characteristics of one wafer

5.4 DESCRIPTION OF A TRANSISTOR WITH COLLECTOR ELECTRICALLY INSULATED FROM THE HEAT SINK

The header for this transistor was described by J. T. Nelson in the Second Interim Report, Chapter 4. A diagram of this header is given in Fig. 21. Several transistors have been made on this header.

Two pictures showing one germanium wafer with leads attached are shown in Fig. 22. Units assembled on this header have been damaged in processing and were not suitable for electrical tests. However, the causes for the damage are known and it appears that a wafer can be mounted successfully on the header.

5.5 PROPOSED WORK FOR THE NEXT QUARTER

The fabrication and testing of the transistor type discussed above will continue during the next quarter.

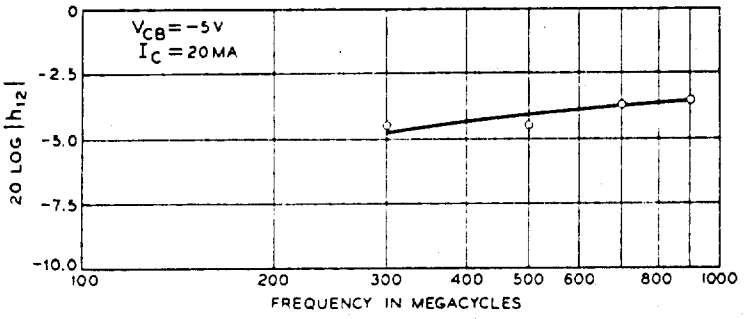

Fig. 18 - h_{12e} versus frequency

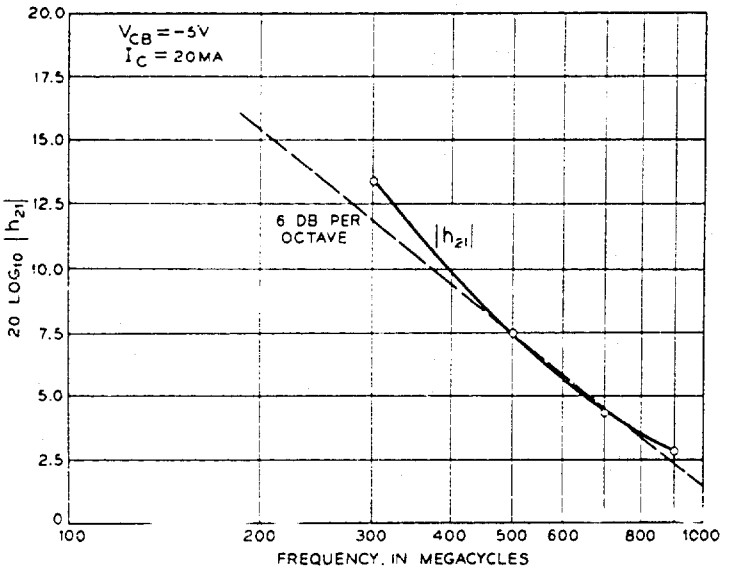

Fig: 19 - h_{21e} versus frequency

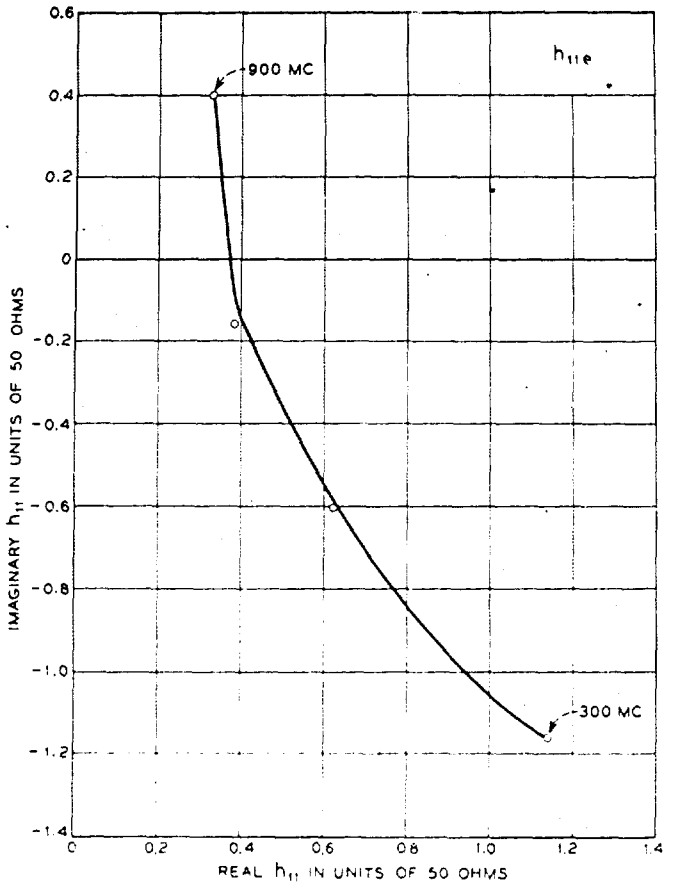

Fig. 20 - h_{11e}

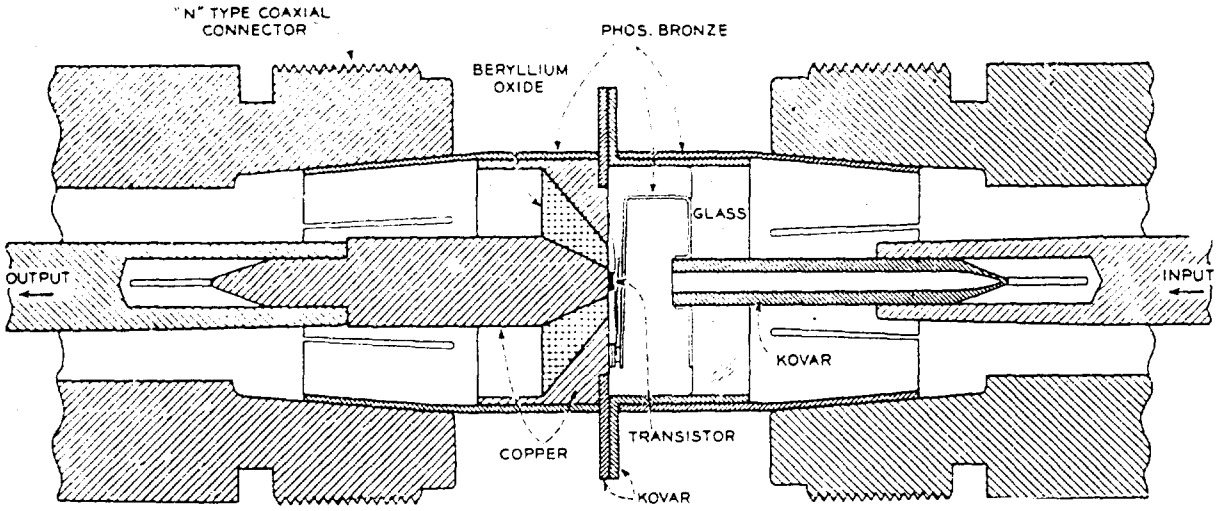

Fig. 21 - The coaxial header

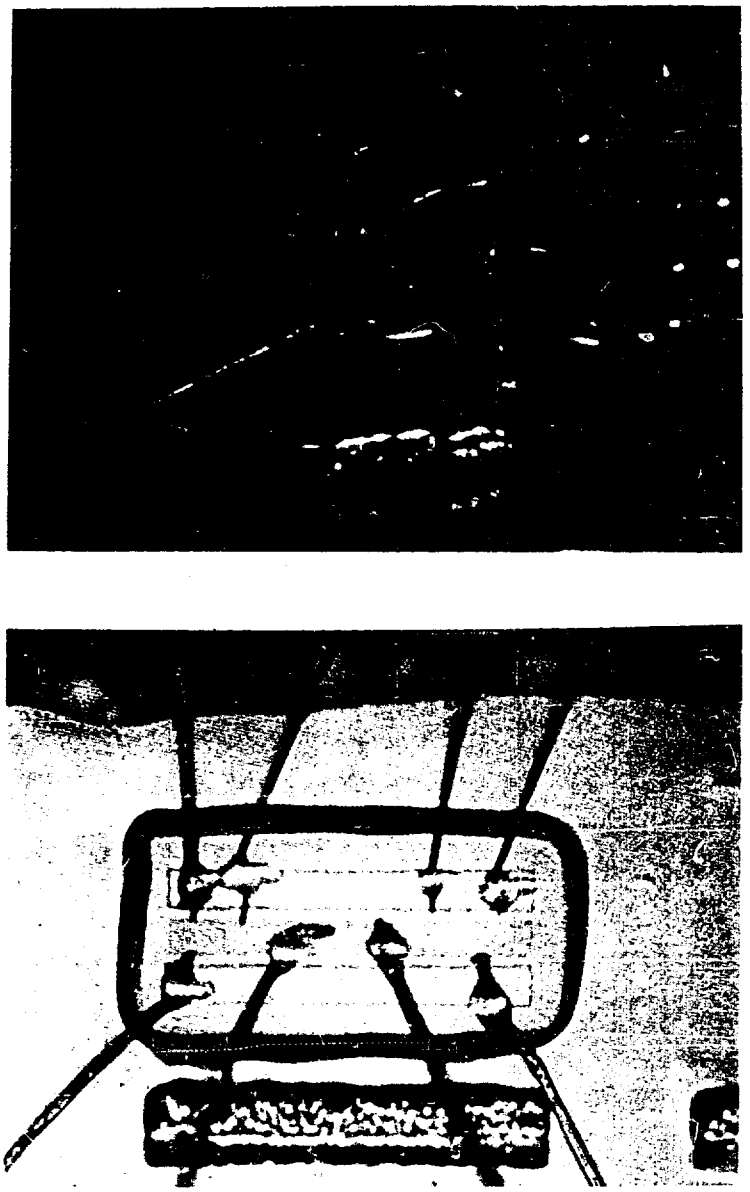

Fig. 22 - Photographs of a wafer mounted on the coaxial header

Chapter 6

MEASUREMENT OF THE NUMBER OF IMPURITIES IN THE BASE LAYER OF A TRANSISTOR *

By H. K. Gummel

The number of impurity atoms per unit area in the base region of a transistor is an important design parameter (Ref. 1). In diffused base transistors, the impurity distribution in the base is frequently calculated from measurements on the diffusion depth and the sheet resistivity of the diffused layer. If one then also knows the depth to which the emitter is diffused or alloyed, one can calculate the number of impurity atoms per unit area between emitter and collector.

We wish to point out that the latter quantity can be measured directly and very easily. The method consists of measuring the collector current as a function of emitter-to-base voltage. Diodes usually show deviations from the simple exponential law (Ref. 2).

$$I = I_0 \exp\left(\frac{qV}{kT} - 1\right) \tag{1}$$

because of space charge generation and recombination (Ref. 3), conductivity modulation (Ref. 4), series resistance, or other processes; however, in transistors having reasonable current gain, an exponential law of the form:

$$I_c = I_1 \exp \frac{qV_e}{kT} + I_2 \tag{2}$$

is very closely obeyed at currents low enough so that the voltage drop of base current flowing through base resistance is negligible. In the above equation I_c is the collector current, I_2 a saturation current, q the electronic charge, and kT the Boltzmann energy. If the base width is small compared to the diffusion length, i.e., if recombination in the base is negligible, which is usually the case for high frequency transistors, I_1 is given by (Ref. 1):

$$I_1 = \frac{qA D n_i^2}{\int N(x)\, dx} = \frac{qA D n_i^2}{N_B} \,. \tag{3}$$

*The work reported here was not done under this contract but is included because of its relevance.

Here A is the emitter area (or collector area if it should be smaller), D the diffusion constant of the minority carriers in the base, n_i the intrinsic carrier concentration, N(x) the base impurity concentration at a distance x from the emitter junction; the integral extends from the emitter junction to the collector junction and represents the number of impurities per unit area in the base, N_B, that we wish to find. The above Equation (3) was derived for a diffusion constant D that does not vary over the base width, whereas D actually depends to some extent on the impurity concentration. Equation (3) still applies if we interpret D as a properly averaged value.

The constant I_1 can be obtained with good accuracy by subtracting the saturation current I_2 from the measured collector current and plotting the difference in a semilog plot versus the emitter-to-base voltage. This plot results in a straight line whose intercept is I_1.

Equation (3) can now be solved for N_B and yields:

$$N_B = \frac{q}{I_1} A D n_i^2 . \qquad (4)$$

If the junction area is measured microscopically, then all quantities on the right hand side of Equation (4) are known. The greatest uncertainty is due to D whose value at high impurity concentrations is not known accurately. Subject to that uncertainty, this method should provide accurate measurements of N_B.

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1. J. L. Moll and I. M. Ross, Proc. of the I.R.E., 44, 72 (January, 1956).
2. W. Shockley, B.S.T.J., 28, 435 (1949).
3. C. T. Sah, R. N. Noyce, and W. Shockley, Proc. of the I. R. E., 45, 1228 (September, 1957).
4. R. N. Hall, Proc. of the I.R.E., 40, 1512 (November, 1952).

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Chapter 7

STATUS REPORT ON INTEGRATED CIRCUITS

By M. M. Atalla

evelopment work is continuing on the integrated circuits program. The main effort during this past period has been on the following two phases of the program.

I. Development and evaluation of processes, from the standpoint of yield, reliability and cost, for the fabrication of various devices which are of general applicability as active components in logic circuits. The thermal oxidation process has been used in all this work (Ref. 1, 2, 3, 4). All devices are provided with a surface passivating thermal oxide. The application of this process is believed to be one of the key factors on which may depend the practical feasibility of integrated circuits for the following reasons: (a) the process is basically a large scale batch process which eliminates the need for in-process individual testing and reprocessing, and (b) the resulting device stability makes possible, without further individual encapsulation, the storage of devices and their handling in such processes as mounting, lead attachment and interconnecting without the need for the usual clean-up etching, vacuum baking, etc.

II. Application of the processes outlined above to a more specific development of the integrated low level logic gate previously discussed in (Ref. 5).

The structure used is as described in (Ref. 6) which represents the output end of the gate circuit consisting of a transistor inverting amplifier and three computer diodes.

Work on phase I outlined above has included the evaluation of processes for the fabrication of various thermally oxidized computer or logic type silicon diodes with recovery times in the nano-second range. These included: (a) p+n diodes on common n-type substrates covering the range of breakdown voltages between 15 and 100 volts. The sheet resistance of the p-layer was also varied from a few ohms/square to 100 ohms/square. The higher sheet resistances were used primarily to demonstrate the feasibility of obtaining by a single diffusion both the computer diodes and the base regions of transistors to be incorporated on the same substrate. (b) n+p diodes on common p-type substrates.

Both epitaxial and nonepitaxial silicon has been used in the above work. The following is a brief description of the masked diffusion technique (in contrast to the diffused mesa technique) which has been applied to the fabrication of the various diode types outlined above.

(1) The starting silicon slice (for example an epitaxial film 1-10 ohm cm, about 10 microns thick on 0.001 ohm cm substrate of the same type as the film) is oxidized at 1200° C in water vapor to a thickness of 1/2 to 1 micron of silicon dioxide.

(2) Using photoresisting techniques, 0.004 inch diameter holes are opened up in the oxide in any desired array.

(3) Boron or phosphorus is predeposited using the box technique followed by a drive-in. The following ranges have been covered, all producing satisfactory results: predeposit temperatures 850-1100° C, drive-in temperatures 1000-1200° C in oxygen and/or water vapor. Diodes were obtained with junction depths of 1 to 10 microns and sheet resistances of a few ohms/square to over 100 ohms/square.

(4) The oxide is removed from the back side of the slice and a gold layer 2000Å thick is evaporated on this side. The gold is then driven in by heating the slice at 1050° C for 20 minutes followed by a quench to room temperature.

(5) Oxide is removed from the diffused diode areas by photoresisting and etching or by etching alone. The latter technique is obviously only applicable when the oxide grown over the diffused areas is substantially thinner than the original masking oxide (obtained in step 1).

(6) Contacts are applied by either evaporation through a metal mask or by the electroless deposition of nickel and/or gold followed by alloying.

(7) By sawing or etch cutting, the slice is cut up into individual units or into multiple arrays as desired.

An additional step, to precede step 7 which is currently being evaluated, is to deposit a 10 micron film of silicon monoxide over the entire top surface of the slice except for the device contacts. On this monoxide, 0.002 inch wide metal runners and 0.018 inch diameter contact areas are evaporated. The runners connect the device contacts with the 0.018 inch diameter final contact areas as shown in Fig. 23.

Shown in Fig. 23, is a proposed module for both diodes and transistors, when fabricated by the "limited diffusion" process as described above. These modules, used in singles or multiples, are the basic building blocks for circuit integration. In many cases, however, it may be desirable to fabricate arrays of dissimilar devices on a common silicon substrate. An example of this is an array of one transistor and several diodes on a common substrate providing an alternative means for integrating the low level logic gate. The feasibility of this is being investigated as discussed in the latter part of this chapter.

The following are typical results obtained from epitaxial p^+n computer diodes fabricated by the above process. The devices were mounted on a conventional header and the leads were thermal compression bonded directly to the device contact. No encapsulation was provided and the measurements were carried out in room air.

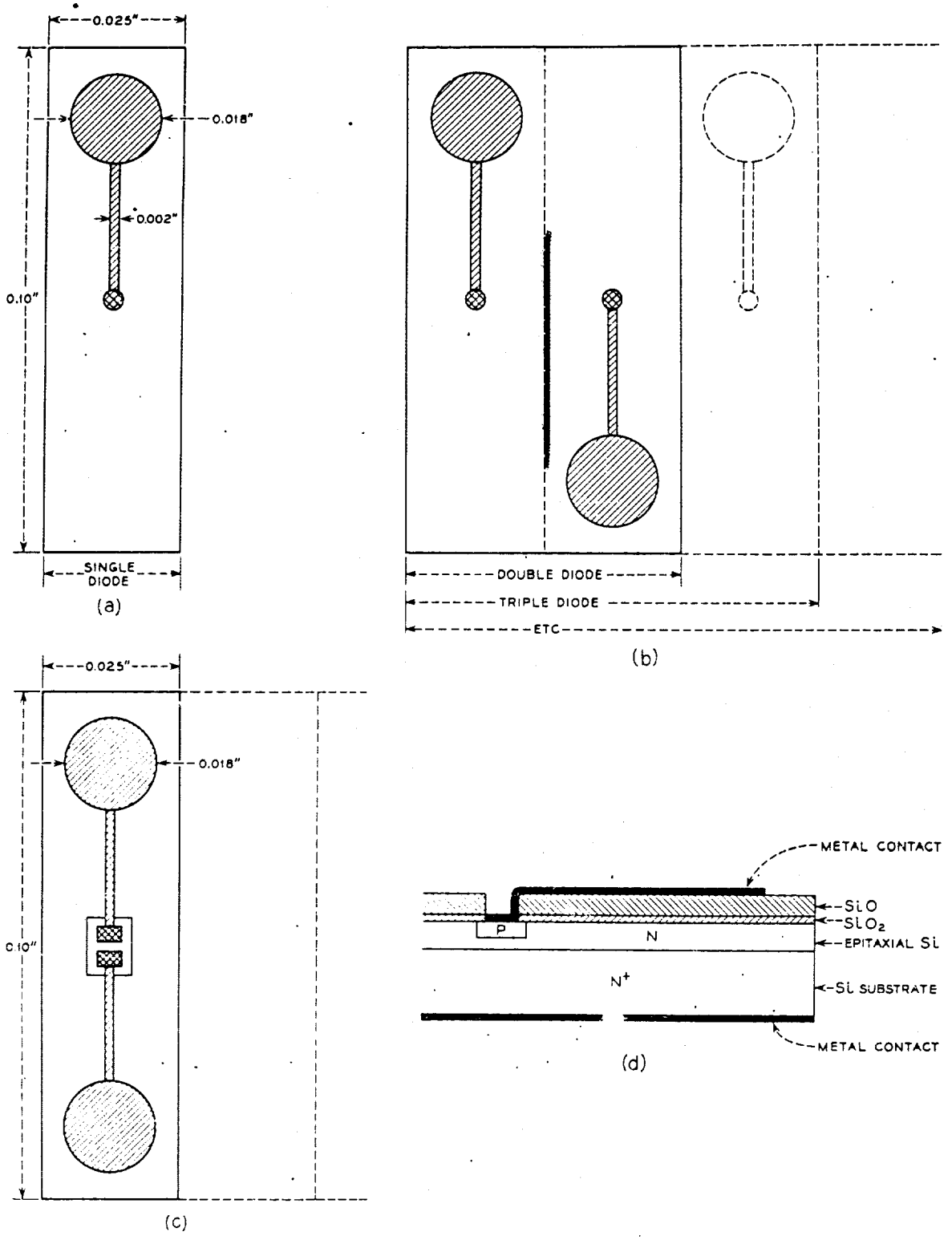

Fig. 23 - Standard module proposed for "limited diffusion" devices, as basic building blocks for integrated circuits. A: a single diode, B: multiple diodes, C: same module for single and multiple transistors (common collector), D: cross-section through a p+n epitaxial diode module

As shown in Table 7-1, and typically for all results obtained to date, the following are the significant features of the results: (a) through the use of thin epitaxial films, it was possible to reduce the diode capacity and forward drop to the low levels indicated. (b) The spread in zero bias capacity and breakdown voltage is relatively large (see columns 1 and 4 for their respective ranges). The cause, however, has been conclusively assigned to nonuniformities in doping of the epitaxial films used, where in general a higher capacity device invariably had a lower breakdown voltage. (c) Of particular significance to the integrated circuit program and as previously demonstrated for mesa-type devices fabricated by the thermal oxidation process (Ref. 1), the forward voltage drop and the recovery time are quite uniform both within one slice and from slice to slice.

Table 7-1

TYPICAL CHARACTERISTICS OF THERMALLY OXIDIZED EPITAXIAL COMPUTER DIODES ($P^+\nu N^+$) PRODUCED BY THE LIMITED DIFFUSION PROCESS (GOLD DOPED)

	(1)	(2)	(3)	(4)[a]		(5)[b]	
Run No.	Zero bias Capacity, pf	Forward Drop Volt at 10 ma	AC Resistance ohms at 10 ma	Reverse Breakdown Volts	(I_{120v}) μamp	Recovery Time: nano sec Storage	Total
EP #3, EP #4 (75 units)	0.6-1.2	0.77 (σ = 0.003)	#3 6.8 (σ=0.5) #4 10. (σ=1.7)	50-100	92% <0.015	2.0	5-6

(a) Breakdown Voltage is measured at 10 μamp.

(b) Measured under condition of equal forward and reverse current of 4 ma with a series resistance of 390 ohms. The total recovery time is the sum of the storage time given and the decay time to 10 per cent of initial current. Only 19 of the 75 Units were measured for recovery time.

From the work on this phase of the program, the following conclusions were drawn:

(1) The limited diffusion process is a batch process applicable to the fabrication of all types of oxide passivated diodes. (Detailed reliability studies on devices produced by this process are in progress using stress aging techniques).

(2) Gold doping and quenching was found equally effective in N^+P diodes as in P^+N diodes in reducing the diode recovery time to the 5 nano-second range.

(3) The advantages of the use of epitaxial material have been demonstrated particularly as reflected in low diode capacity and low forward drop.

During the past period considerable progress has also been made in integrating a transistor and three diodes on a single silicon substrate as an array representing the output end of the low level logic gate. A process has been developed for the fab-

rication of these arrays which is essentially an extension of the limited diffusion process described above for the fabrication of the diodes. The following is a summary of the process.

(1) The silicon slice is oxidized at 1200° C in water vapor to an oxide thickness of 1/2 to 1 micron.

(2) By photoresisting, holes are opened in the oxide to incorporate the diodes and the transistor base region.

(3) Boron is predeposited using the boron in the box technique followed by a drive-in in dry oxygen followed by water vapor. The exact cycle depends on the base sheet resistance and the collector junction depth desired. In this work these were 200 ohms/square and 4 microns respectively.

(4) The oxide grown during Step 3 is used as a mask which is photoresisted to incorporate an opening for the emitter.

(5) Using the box technique, phosphorus is predeposited at 1050° C for 30 minutes followed by a drive in to produce a junction depth of 3 microns and a base width of one micron.

(6) Gold doping is carried out as described in Step 4 for diode fabrication.

(7) A final photoresist is carried out to provide contact holes for emitters, bases and diodes.

(8) Contacting and cutting follows steps 6 and 7 of the diode process.

Several slices, each incorporating 9 arrays have been carried out through the entire process demonstrating the feasibility of simultaneous processing of the diodes and the transistors. For initial characterization purposes only, the units were mounted on 8 pin headers. The assemblies are yet to be incorporated in complete gate circuits and characterized as such. Furthermore, all the units completed to date were fabricated from nonepitaxial material. The process is currently being used to fabricate about 100 epitaxial assemblies from which more complete data on yield, gate characteristics and reliability will be obtained.

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Chapter 8

TRANSISTOR REQUIREMENTS FOR DCTL

By J. E. Iwersen

8.1 INTRODUCTION

Parallel Direct-Coupled Transistor Logic (DCTL) consists of current nodes such as that shown in Fig. 24, each transistor in the system having its base connected to one node and its collector to another. It still finds wide favor among logic circuit designers in spite of the fact that it uses more transistors than other common systems to perform a given logical function, because of its combination of structural simplicity, low power consumption, and high speed relative to other logic systems. The principle obstacle to the widespread use of DCTL has been the phenomenon of base-robbing (Ref. 1). When two or more transistor bases are driven from a common current source, the current tends to distribute unevenly among them unless the voltage-limiter-like (strongly temperature dependent) input characteristics of the parallel units are very closely matched. This uneven distribution can result in one or more transistors not receiving sufficient drive to go into saturation.

Experiments have shown that transistors will have properties sufficiently closely matched for DCTL if they are fabricated at adjacent spots of the same semiconductor slice. This leads to the natural proposal that an integrated circuit be made consisting of such transistors with their emitters connected together and their bases connected together. This circuit would be contained in a small (isothermal) enclosure so that temperature variations from one unit to another could not unbalance the inputs.

It is the purpose of this note to show that all the conditions for a solution of the base-robbing problem are not satisfied by this scheme. Diffused-base transistors in general have a dependence of input voltage on collector current which can unbalance the inputs sufficiently to prevent the use of DCTL.

8.2 THE DEPENDENCE OF INPUT VOLTAGE ON COLLECTOR CURRENT

Let us consider an epitaxial diffused-base transistor for simplicity; a cross-section through such a device is shown in Fig. 25, where we take for definiteness an n-p-n double-diffused silicon transistor. Since the collector is nearly an equipotential region, the most forward biased part of the collector junction is always under the base contact and it is here that most of the minority-carrier injection from the collector into the base layer takes place when the transistor is driven into saturation. This part of the junction is physically remote from the emitter,

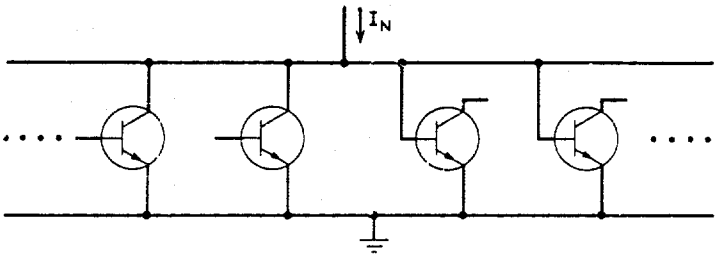

Fig. 24 - General node of parallel DC TL

thus the inverse alpha (α_I) of such structures is usually rather poor ($0 \longrightarrow 0.1$). Gold doping to lower collector-body lifetime also lowers α_I. α_I in nonepitaxial diffused-base transistors is also usually low for these reasons and because of the light to moderate doping of the collector body.

Epitaxial transistors in saturation give a fairly good fit to the Ebers-Moll (Ref. 2) relations, at least for moderate currents. This theory* gives:

$$V_{BE}\,(\text{sat}) = \frac{kT}{q} \log \frac{I_E - \alpha_I I_c}{I_{EO}} \qquad (1)$$

where V_{BE} (sat) = base emitter voltage in saturation

k = Boltzmann's constant

T = Absolute temperature

q = electronic charge

I_{EO}. = a parameter used to fit the curve

[= the reverse saturation current of the emitter junction for an ideal linear transistor]

α = the normal transistor alpha.

(The direction of positive current is shown in Fig. 25.)

Notice that for $\alpha_I \cong 0$, V_{BE} is a function of I_E only. This means that identical transistors in the same environment with their bases connected together, having the same V_{BE}, have the same I_E.

Now let us consider the circuit shown in Fig. 26 where transistors 1 and 2 are isothermal identical transistors each with $\alpha_I = 0$. A signal arrives on their (common) bases and they must saturate for the circuit to perform its function. Assume that transistor 1 is now the only conducting collector at node A so that it must draw the full node current (I_N) for the circuit to operate properly. Assume that at node B

*A more detailed and exact theory of input voltage and its implications for DCTL will be given in the next report.

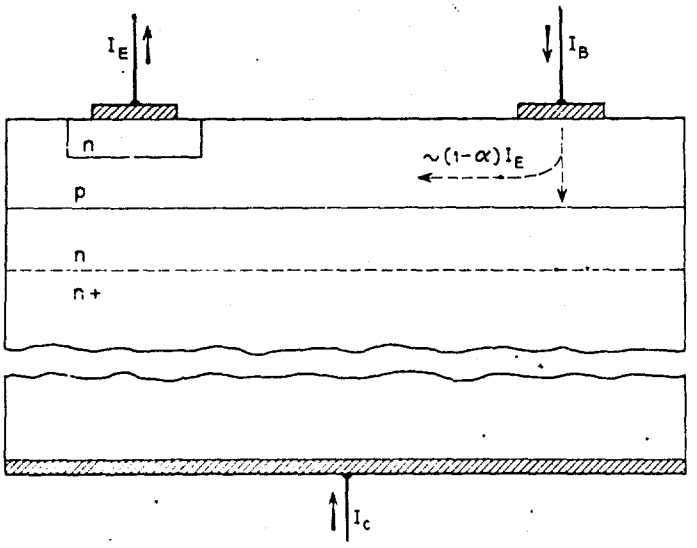

Fig. 25 - Generalized cross-section of a double-diffused epitaxial transistor (vertical dimension greatly exaggerated)

there are one or more saturated collectors in addition to transistor 2 and assume further that these collectors draw the full node current, leaving none available for transistor 2. (Parallel collectors are not necessarily identical or in the same environment). From the circuit and the identity requirement ($V_{BE1} = V_{BE2}$, $I_{E1} = I_{E2}$):

$$I_{C1} + I_N = I_{E1} + I_{E2} = 2I_{E1}$$

$$I_{C1} < I_{E1} = \frac{I_{C1} + I_N}{2}$$

$$I_{C1} < I_N$$

that is, transistor 1 will not saturate.

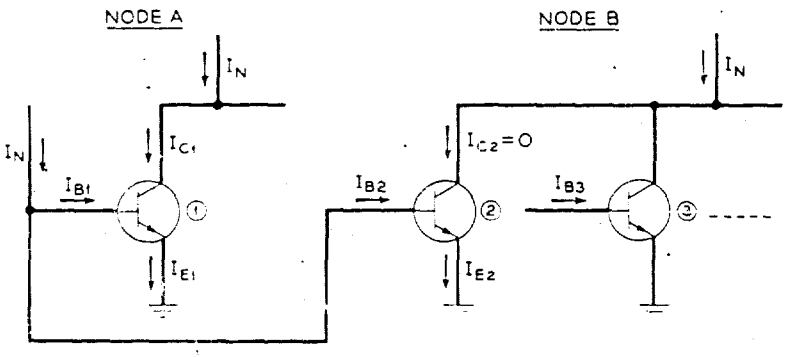

Fig. 26 - Circuit illustrating base-robbing between identical transistors

The result of the foregoing argument is that one cannot rely on circuits* with bases connected together or, in other words, the logical gain or fanout is limited to one. That is, Ebers-Moll transistors with $\alpha_I = 0$ cannot be used for DCTL. It should be pointed out that as α_I increases the possible fanout increases. In particular, for the limit of $\alpha_I = 1$ Equation (1) shows that V_{BE}(sat) is a function only of $I_E - I_C = I_B$. In this case there is no I_C dependence of V_{BE} and no limitation on fanout from this cause.

An examination of various codes of mesa and planar transistors shows that, in general, a fanout of two could be used but a fanout of three could not. This is due partly to α_I being > 0 and partly to deviations* from Equation (1), but remains a fairly inconvenient limitation.

The only practical way to increase this fanout is to add external base resistance to each transistor, the resistance being of such a value that the voltage drop across it is greater than or equal to the V_{BE} (sat) variations. The greater the fanout, the greater is the IR drop required. The addition of such resistors increases the power dissipation tending to make DCTL (or Resistance Coupled Transistor Logic, now) less attractive.

8.3 SUMMARY AND CONCLUSIONS

An increase of saturated base voltage with increasing collector current has been described. This phenomenon results in an unbalanced distribution of base current among transistors whose bases are connected together. A DCTL circuit, therefore, may not operate properly. This base-robbing effect puts a more stringent specification on transistors used for DCTL than the commonly assumed one of identicalness. The additional requirement is essentially that the inverse alpha be high.

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*See previous footnote.

Chapter 9

STORAGE TIME OF EPITAXIAL DIFFUSED TRANSISTORS

By J. E. Iwersen and W. R. Draper

9.1 INTRODUCTION

Storage time (t_s) of double-diffused non-epitaxial silicon transistors (Fig. 27) used in common-emitter switching circuits has been in a poor state of theoretical understanding. This situation is due to the fact that almost all the charge responsible for storage effects is stored in the collector body and changes not only its magnitude but also its spatial distribution with drive current. Analytically, this is a nonlinear two-dimensional problem which cannot easily be made tractable by any valid simplifying assumptions. Perhaps the best way to display the peculiar storage time behavior of non-epitaxial mesa and planar transistors is by means of Fig. 28 which shows a typical plot of t_s vs. collector current for such units for fixed drive currents. Notice especially the region (B) of increasing t_s with increasing I_c. This effect is totally unexpected on the basis of existing theory (Ref. 1); therefore, t_s has been effectively undesignable. In addition, since not even a generally valid empirical relationship between t_s and I_c has been found (although there is a qualitative explanation given later in this report) prediction of t_s in a given circuit from t_s in another circuit has been impossible, necessitating a proliferation of individual tests for specific applications.

The advent of the epitaxial process, which has resulted in the removal of most of the collector body resistance and most of the volume available for minority-carrier storage, has greatly simplified the carrier storage situation. With such transistors, it has become possible to characterize storage time for all circuits with one or two measurements.

9.2 STORAGE TIME OF EPITAXIAL DIFFUSED TRANSISTORS

The only important ohmic resistance in an epitaxial transistor being the base resistance (r_b'), the equivalent circuit shown in Fig. 29 is taken to represent the transistor. The transistor symbol stands for a transistor without any parasitic resistances (for which the Ebers-Moll [Ref. 2] relations would be expected to hold reasonably well); the diode is also free of parasitics. We will refer to the components of the equivalent circuit as the i-transistor and i-diode (i for intrinsic).

In most applications the IR drop in r_b' will be sufficient to insure that the bulk of the minority-carrier injection across the collector junction, during saturation,

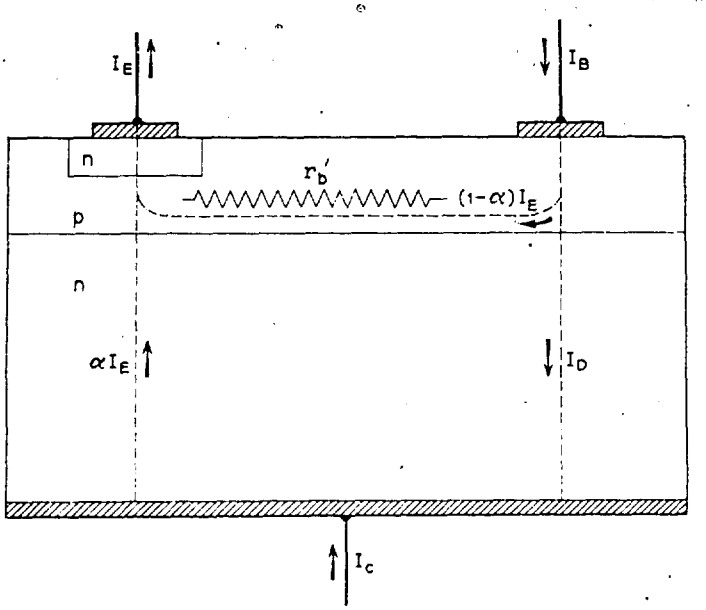

Fig. 27 - Generalized structure of a silicon double-diffused transistor showing general internal current paths

will be in the i-diode and not at the i-transistor collector. (This effect has been recognized before [Ref. 3]). Fig. 29 is thus an integrated Baker-Pressman circuit (Ref. 4).

Since the diode clamps the i-transistor out of saturation, the normal active-region current relations hold for the i-transistor and one can calculate the current in any leg of the equivalent circuit from Kirchoff's Law and the fact that the current in r_b' is always $(1-\alpha)I_E$. In particular, one can calculate the current in the i-diode for any arbitrary terminal currents during both the ON phase and the OFF phase and the storage time of the diode for these currents should equal the transistor storage time.

There is a limitation on this analysis. If I_{D2}* is greater than I_C [this is not very likely in typical circuits] I_{E2} becomes negative and the i-transistor currents are not given by the active-region relations.

In Fig. 30 we see t_s plotted versus I_C for a typical expitaxial transistor for various fixed values of I_{D1} and I_{D2}. These data were taken using a Tektronix Sampling Oscilloscope and a coaxial biasing jig. The value of α (d-c) used to calculate I_D was that extrapolated to $V_{CE}=0$ at the same I_E as existed in the switching circuit.

The lack of dependence of t_s on I_C is almost complete. In addition, we see on the left that the storage time of the diode alone done with the same values of I_{D1} and I_{D2}. During this measurement, the emitter was open-circuited ($I_E=0$). Considering the simplicity of the model and the measurement error, the agreement is very good. Many different types of epitaxial transistors (gold-doped and non-gold-doped, circular

*Subscript 1 refers to the ON phase and subscript 2 to the OFF phase.

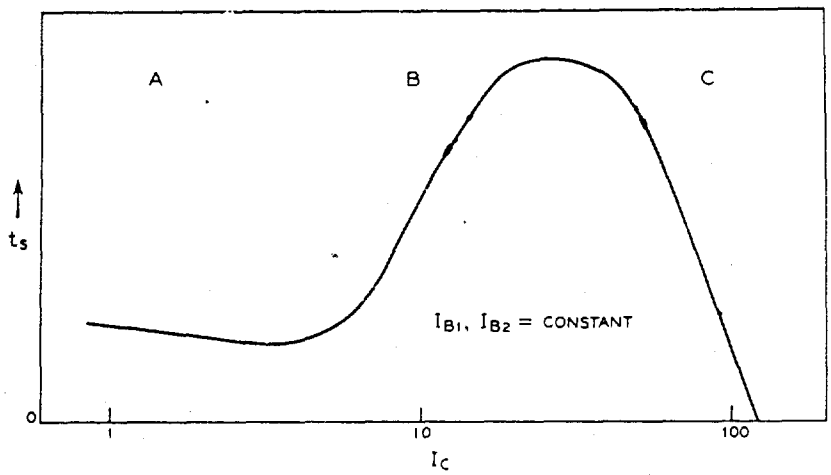

Fig. 28 - Typical variation of storage time with collector current for mesa and planar nonepitaxial transistors (arbitrary units - both scales)

and stripe electrodes) have been spot checked for diode and transistor storage time; the agreement has almost always been within the measurement error.

The argument and data given above have established that storage characterization of an epitaxial diffused transistor requires only storage characterization of the base-collector diode. This diode approximates structurally a p-i-n and, indeed, it is found in most cases that injected charge is fully recoverable and lifetime is approximately constant so that the diode law approaches that of a charge-controlled diode (where τ = lifetime)*:

$$t_S = \tau \log \left(1 + \frac{I_{D1}}{I_{D2}}\right) \qquad (1)$$

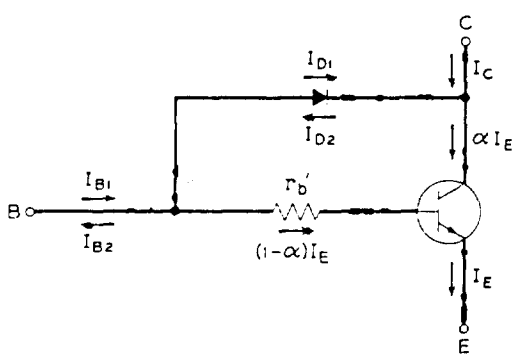

Fig. 29 - Equivalent circuit for epitaxial diffused transistor

*The charge-controlled diode and the meaning of the term "fully recoverable" are discussed in the Appendix.

This being the case, only one measurement to determine τ is necessary. Actually for the transistor whose characteristics are shown in Fig. 30, τ varies by about 20 per cent over a decade of drive current and, if precision better than this is required, a second measurement (at very different drive currents from the first) should suffice for adequate characterization.

If I_{D1} and I_{D2} are calculated in terms of the terminal currents and substituted in Equation (1) we get

$$t_s = \tau \log \frac{I_{B1} + I_{B2}}{I_c/\beta + I_{B2}} \tag{2}$$

which is Moll's (Ref. 1) original formula. This expression was also derived from less restrictive conditions by Beaufoy and Sparkes (Ref. 5). In fact, the essential conditions are just the ones made in deriving Equation (1), namely, the injected charge associated with the excess base current ($I_B - [1-\alpha] I_E$) decays with a constant lifetime and is fully recoverable.

We now see that, even if the excess charge is not all stored in the i-diode, Equation (2) can still hold. This will happen if the τ associated with excess charge in the i-transistor is approximately the same as in the i-diode. In this case Equation (2) can still be used to determine τ.

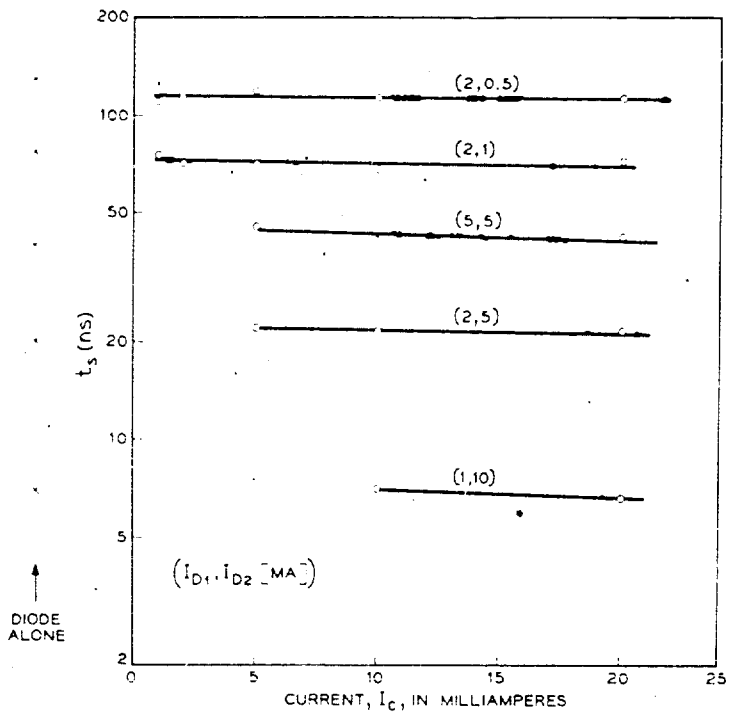

Fig. 30 - Dependence of storage time on current for an epitaxial diffused transistor

9.3 STORAGE TIME OF NONEPITAXIAL DIFFUSED TRANSISTORS

It is instructive at this point to consider again the behavior of nonepitaxial transistors (Fig. 28) in terms of what has been said so far. In such transistors where r'_c is not negligible there is a competition between the voltage drop in r'_c which tends to turn the collector junction on under the emitter and the lateral base drop which tends to turn it on under the base contact. We would expect that at relatively high I_C and low I_B (in light saturation) the turn on would occur under the emitter and for low I_C and high I_B (heavy saturation) under the base contact and indeed these are just the regions C and A respectively in Fig. 28, B being the transition region from one to the other. The variation of t_s with I_C is then a spatial variation of injected charge with current. Although one can account for some variation in effective lifetime from one region of the collector body to another by arguing that charge under the emitter is more recoverable (an electric field due to r'_c is driving it toward the junction) than that under the base contact, to fit Fig. 28 in most cases we require that the minority-carrier lifetime in the collector body under the base contact be less than the lifetime under the emitter (10:1 variations in t_s from peak to valley in Fig. 28 have been seen). The cause of this spatial lifetime variation is not understood.

9.4 CONCLUSION

Storage characteristics of epitaxial diffused transistors have been explained in terms of a simple equivalent circuit whose efficacy has been confirmed by experiment. It has been shown that such transistors are almost described by the formula given by Moll for an ideal linear transistor. As a result, storage time is now easily designed and characterized whereas this was an extremely difficult task in nonepitaxial mesa and planar transistors.

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APPENDIX

This section is concerned with the justification of Equation (1) of the text.

Let us consider a p-n junction diode that consists of two end regions, p-type and n-type, with a central region between them. This central region is where rectification, charge storage, etc. occur. The numbers of excess holes and excess electrons in the central region must be equal to each other so that overall neutrality is maintained. Let us assume that the excess carriers recombine with each other at a rate proportional to their number (Q), the proportionality constant being $1/\tau$, where τ is called the lifetime.

The diode current will consist of a recombination term and a charging term:

$$I = Q/\tau + dQ/dt \tag{3}$$

This equation is true for any diode with constant lifetime. It says, among other things, that the current depends only on the total charge in the device and not on its distribution. It is the voltage across the diode that, in general, depends on the charge distribution. (For instance, in the simple low-injection case, the voltage depends on the charge concentration at the junction).

A charge-controlled diode will be defined as one for which the voltage is in the forward-bias direction as long as the diode contains any injected charge. In such a diode, we can apply a constant reverse current (after a period of forward current) until Q drops to zero, since the voltage cannot rise to block the current flow until Q is zero. In this case, we say that the charge is fully recoverable since an arbitrarily small fraction of Q is lost to recombination for a sufficiently high value of reverse current.

If we have a steady forward current, $I_1 = Q_1/\tau$, flowing and suddenly apply a reverse current, $-I_2$, where I_2 is positive, integration of Equation (3) yields for the time for Q to drop to zero, the storage time:

$$t_s = \tau \log \left(1 + \frac{I_1}{I_2}\right) \tag{1}$$

If an injected charge, Q, is maintained in a (real) diode it will come to a certain steady-state distribution. The diode will be carrying a forward current, $I = Q/\tau$, and will be forward-biased. Thus we infer that when a diode contains (momentarily) a charge Q, there are internal forces which tend to rearrange the charge to the steady-state distribution. Thus the definition of a charge-controlled diode given

above essentially requires that the charge rearrange itself to its steady-state distribution instantaneously whenever a disturbance occurs. Any real diode will take a finite time to rearrange its charge but it can be treated as charge-controlled if one is not trying to measure transients of the order of or faster than the rearrangement time ($\overline{\tau}$).

Suppose that the injected charge is stored in a region of thickness W in the direction of current flow. A disturbance, say a delta-function pulse of charge, occurs in this region. The rearrangement time will be essentially the time it takes for this pulse to spread to thickness W. This is given by well-known diffusion theory as $\overline{\tau} \cong W^2/D$ (D the carrier diffusion constant).

For the simple step p-n junction (Ref. 6) W is approximately a lifepath ($\sqrt{D\tau}$) so that $\overline{\tau} \cong \tau$. In this case, the prediction of Equation (1) that $t_s = \tau$ for $I_1/I_2 = e^{-1}$ is too high by about a factor of two. The disagreement is, of course, worse for lower values of I_1/I_2 (shorter storage times). Since one is usually interested in recovery where I_1 is of the same order of magnitude as I_2, Equation (1) is not very useful for step junctions.

For p-i-n diodes, the injected charge is essentially all stored in the i-region. Its thickness (W) is normally much less than a lifepath, $W \ll \sqrt{D\tau}$, so that $\overline{\tau} \ll \tau$. In typical silicon switching transistors, $\overline{\tau}/\tau \lesssim 0.1$. Thus, Equation (1) is a good approximation for $I_1/I_2 \cong 1$ and often for $I_1/I_2 \ll 1$.

SECTION 5 - CONCLUSIONS

TASK 2 - TRANSISTOR RELIABILITY

Step-stress aging experiments on the 1N673 and 1N660 silicon diodes have shown that for these devices,

1) Power aging in the forward and reverse direction have the same effect.

2) Temperature aging and power aging may be related through measurements of the temperature rise under applied power.

A correction factor has been derived to compensate for the effect of prior steps in a step-stress aging experiment. Working curves have been developed for useful values of the various parameters involved so that the correction may be readily applied.

Accelerated aging experiments have shown that:

1) In temperature aging diodes within a single encapsulation fail together while the result between encapsulations show normal scatter.

2) Power aging of a single diode within an encapsulation does not significantly affect the remainder.

These results suggest that the dominant cause of failure is connected with the encapsulation rather than the wafer or individual devices on the wafer.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Measurements have shown that the M2260 1 watt 1 kmc transistor will require electrical isolation of the collector from the transistor header. Proposed headers appear feasible.

The common emitter version of the M2107 small signal germanium transistor can probably be mounted successfully on a modified TO-18 header.

The number of impurities per square centimeter of transistor base layer can be determined by a simple electrical measurement.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The masked diffusion technique provides an alternative batch process (to the thermally oxidized diffused mesa process) for the fabrication of many types of thermally oxidized diodes particularly suitable for integrated circuit work. The resulting device uniformity and stability may provide feasibility of key factors in es-

tablishing the practical common-substrate multiple device arrays as basic building blocks for circuit integration.

An extension of the above process was also developed and found feasible for the fabrication of transistor-diode arrays on a common substrate as a means for the integration of the low level logic gate.

An equivalent circuit for epitaxial diffused transistors in saturation has been proposed. Storage time of these transistors has been successfully described in terms of this circuit. As a result, storage time of epitaxials is easily characterized and designed. The complicated and undesignable behavior of nonepitaxials has been qualitatively explained.

It has been found that, for DCTL, it is not enough to require transistors to be substantially identical and isothermal. Transistors whose bases are to be driven from a common current source must have α_I substantially greater than zero in order that all units receive sufficient drive current to saturate. Because of their low α_Is, most diffused-base types are limited to a fanout of two in DCTL.

SECTION - 6 PROGRAM FOR THE NEXT INTERVAL

TASK 2 - TRANSISTOR RELIABILITY

Accelerated aging studies will continue to investigate the effect of various stresses on device reliability. Step-stress aging will be utilized to evaluate other devices and to extend knowledge of the effect of different failure criteria on the various device parameters of interest.

Work will continue to evaluate the reliability of multiple diodes in a single encapsulation with particular attention to the modes and mechanisms of failure and their relationship to device processing.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Fabrication and evaluation of the M2260 1 watt 1 kmc transistor will continue. Coaxial and improved single-ended headers will be evaluated together with prototype feasibility transistor wafers.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Devices fabricated by the limited diffusion technique will be subjected to an extensive reliability study using stress aging techniques. These will include high humidity reverse bias tests, forward and reverse power aging and elevated temperature aging.

The limited diffusion technique will be applied to fabricate a large number of epitaxial gates to examine in more detail such feasibility aspects as gate characteristics, yield and reliability.

Work will continue on the development of the p-n-p-n turn-off gain triode.

The simple explanation given in this report for DCTL fanout limitations of diffused-base transistors will be expanded to a more detailed and exact theory in the next interval.

SECTION 7 - IDENTIFICATION OF PERSONNEL

W. R. DRAPER

W. R. Draper received a B.S. degree in Mechanical Engineering from Colorado A & M College in 1951. He served in the U. S. Air Force from 1951 to 1955 as a pilot. From 1955 through 1957 he was employed at Convair as an instrumentation engineer. He attended San Diego State College from 1958 through 1959 and was awarded the M.S. degree in Physics in June 1960. He joined the Bell Telephone Laboratories in August 1960 and has been engaged in semiconductor device development.

ALDONA J. SIUTA

Aldona J. Suita joined the Bell Telephone Laboratories in 1958 where she has been engaged in mathematical and statistical evaluations associated with semiconductor devices and technology. She received the B.A. degree in mathematics from the New Jersey College at Montclair in 1958.

Earlier reports under this contract and its predecessor contracts have identified other engineers and scientists whose work has contributed materially to this program.

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Fourth Interim Technical Report on
TRANSISTORS

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G. A. Dodson H. K. Gummel J. E. Iwersons
W. R. Draper W. F. J. Hure A. J. Sluta

Report No. 4, 30 April 1961,
64 pp, 30 illus., 3 tables

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Unclassified Report

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices with a view toward demonstrating and increasing the practicability of their use in operating equipment.
This report contains status reports on (1) accelerated step-stress aging of diodes, (2) a 3000-mcps microwave germanium transistor, (3) a 1-watt, 1000 mcps germanium transistor, (4) integrated circuit development, (5) transistor requirements for DCTL, and (6) an analysis of storage time behavior of diffused epitaxial silicon transistors.

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Prepared by M. M. Atalla A. G. Foyt B. T. Howard
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Report No. 4, 30 April 1961,
64 pp, 30 illus., 3 tables

(Contract DA 36-039 sc-85352) DA Proj. 3A99-21-001-01 3119-06-031-01
Unclassified Report

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices with a view toward demonstrating and increasing the practicability of their use in operating equipment.
This report contains status reports on (1) accelerated step-stress aging of diodes, (2) a 3000-mcps microwave germanium transistor, (3) a 1-watt, 1000 mcps germanium transistor, (4) integrated circuit development, (5) transistor requirements for DCTL, and (6) an analysis of storage time behavior of diffused epitaxial silicon transistors.

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1. Engineering Services on Transistors

2. DA 36-039 sc-85353

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Bell Telephone Laboratories, Inc., Murray Hill, N.J.

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