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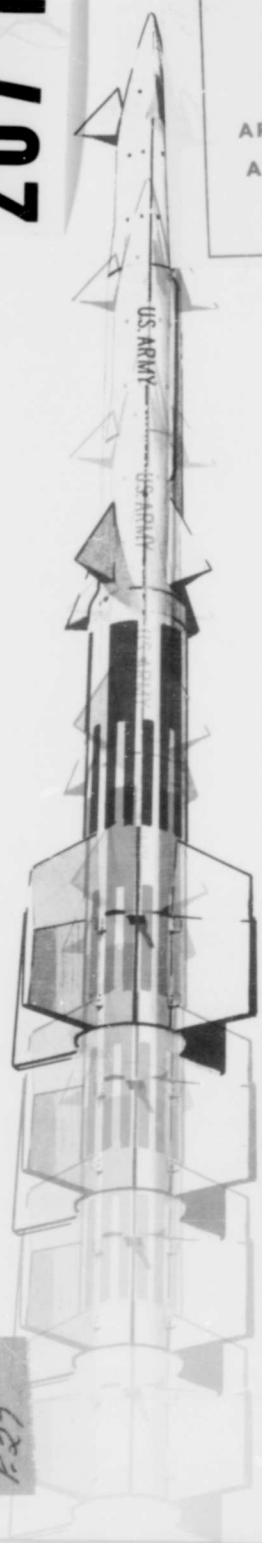
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BALLISTIC CAMERA SYNCHRONIZATION & CONTROL SYSTEM

CONTRACT NUMBER DA-30-069-ORD-3291

Progress Report No. 5



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LINK DIVISION
GENERAL PRECISION, INC.

**BALLISTIC CAMERA SYNCHRONIZATION
& CONTROL SYSTEM**

Contract Number DA-30-069-ORD-3291

Progress Report No. 5

**Link Division
General Precision, Inc.**

August 15, 1961

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FOREWORD

This progress report is submitted in accordance with Article I, paragraph c(1) of Contract No. DA-30-069-ORD-3291. This second report documents the period from 1 August 1961 to 31 August 1961.

SUMMARY

Link, Palo Alto, has received the electrical enclosure and the unit is partly wired. The circuits for the Time Base Generator, Precision Delay Circuit, Pulse Generator and One Millisecond Delay, and Camera Shutter Detector have been designed. Block diagrams of the above circuits are included in the report. The Camera Shutter Detector system is described in detail. A tentative layout of the racks is included in the report.

1. Introduction

This is the fifth in a series of monthly reports covering the progress of the Ballistic Camera Synchronization and Control System. These reports will provide a technical record of the development program. The work completed in the previous month will be covered, and an outline given of the work to be done for the next reporting period. Major problems that arise will also be reported.

2.0 Present Program Status

During the month of August, 1961, the designs of the Time Base Generator, Precision Delay Circuit, Pulse Generator and One Millisecond Delay and the Camera Shutter Detector were firmed up. A tentative layout of the racks was also completed during this month. All components and manufactured parts are on order to complete the prototype resolver servo system.

The Ballistic Camera Synchronization and Control System project is on schedule at this time. Technical Exhibit B changes the scope of the project. A change in the schedule of the Ballistic Camera Synchronization and Control System will be determined by the date of the approval of Technical Exhibit B and the delivery schedule of the component required by Technical Exhibit B.

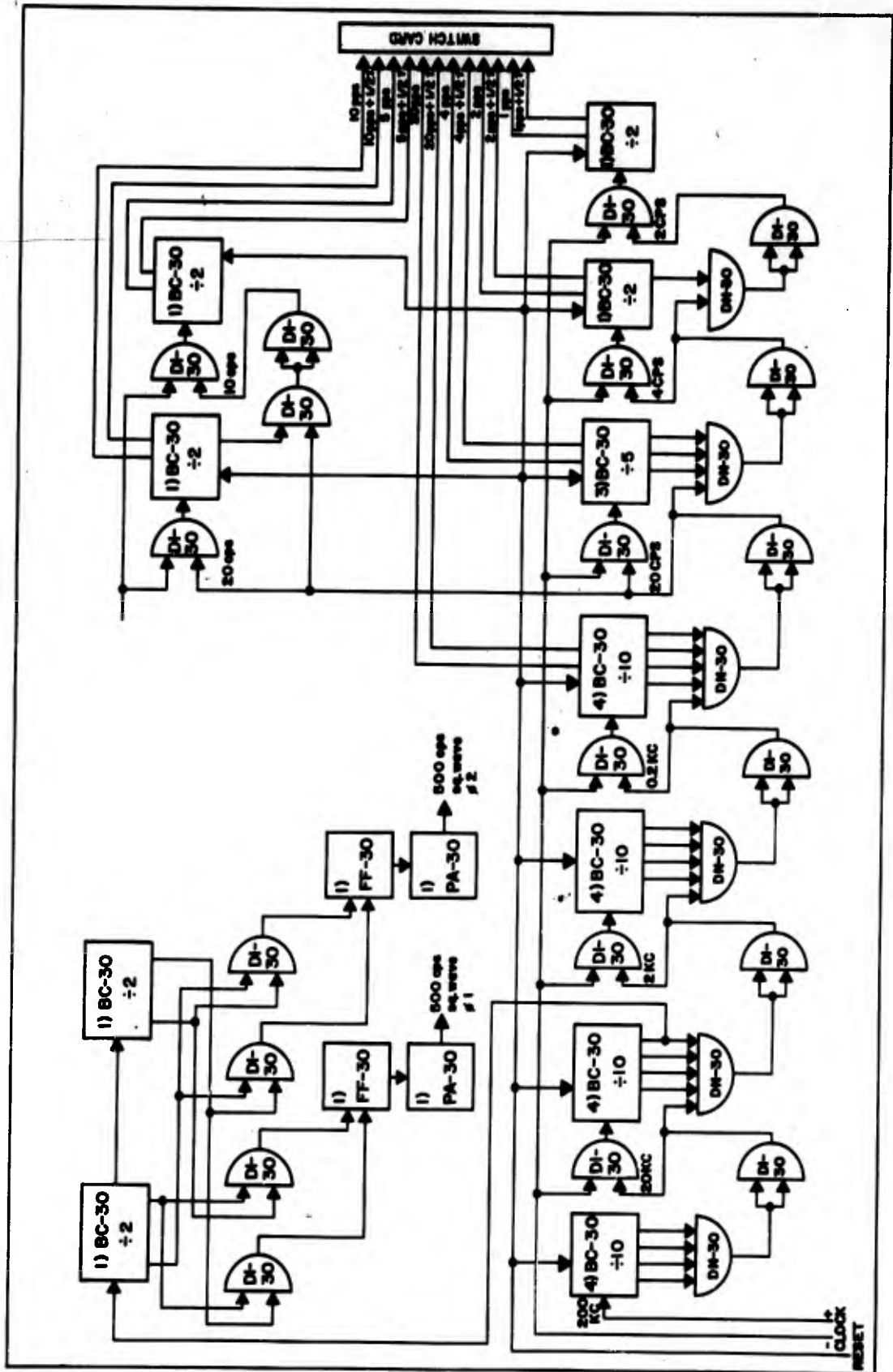
The electrical enclosure arrived August 9, 1961 and is now partly wired.

3.0 Time Base Generator

The Time Base Generator generates the pulse outputs at the basic camera exposure rates of 20, 10, 5, 4, 2 and 1 per second. It also provides the 500 cps square wave frequency reference for the camera shutter drive motor.

Each basic pulse rate is provided with two outputs, the second output giving pulses delayed by half the pulse period. Similarly, the 500 cps square wave is provided at two outputs, the second output being delayed by one fourth period. The two 500 cps outputs thus provide an accurate 2 phase frequency source for the shutter drive motor.

Figure 1 shows the block diagram of the Time Base Generator Circuit. The time base pulses are derived from the 200 KC clock input by pulse count divider circuits which are reset to zero count one millisecond before time zero by the reset pulse from the Precision Delay Circuit. (Refer to Section 3.0 of Progress Report No. 4.) All circuit functions are performed by 3C-Pac Series-S Digital Module plug-in cards, as indicated in the block diagram. The basic pulse rate output will be selected by inserting a switch card in the card rack. A separate card for each rate will be fabricated from blank 3C-Pac cards.



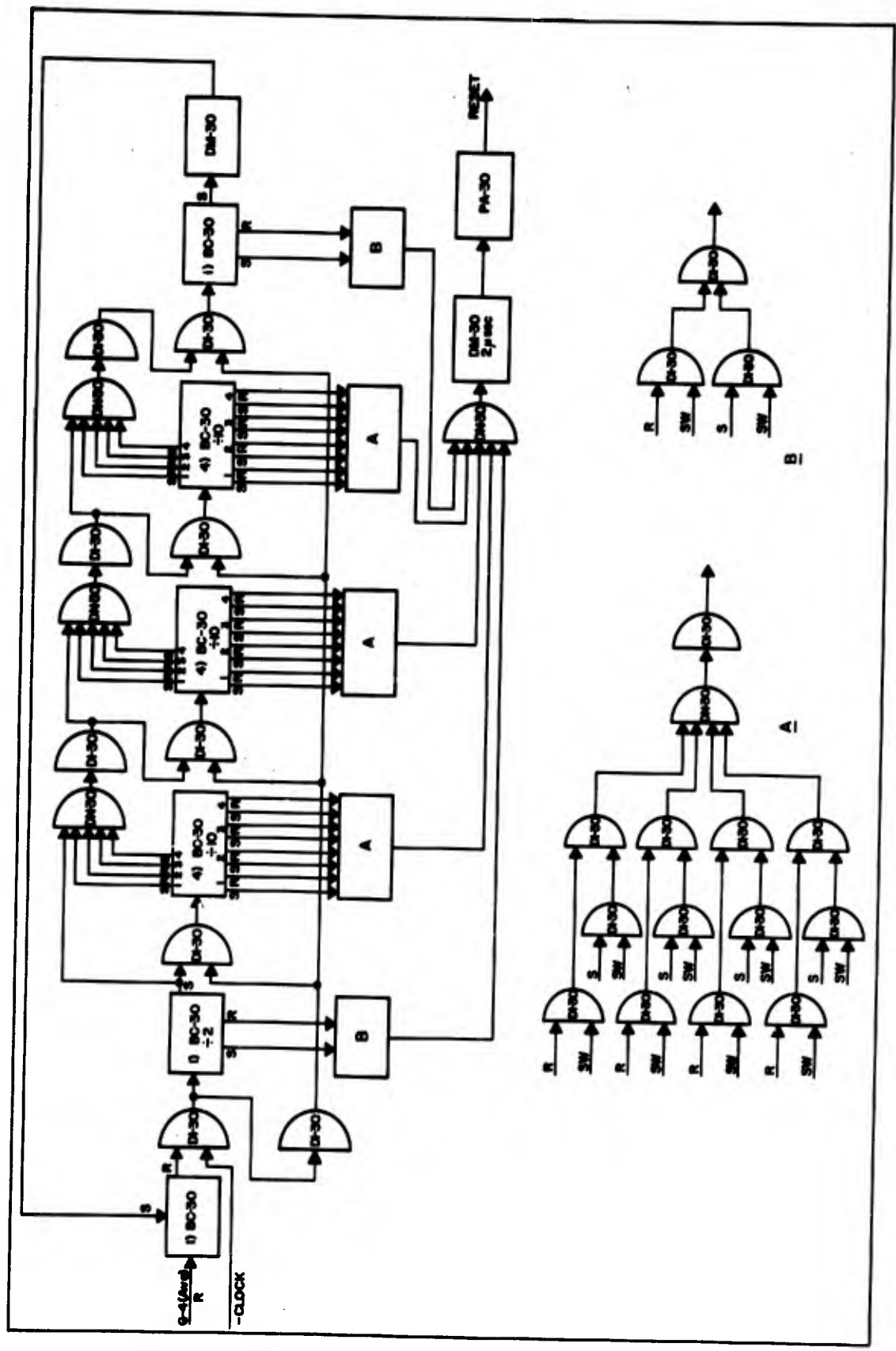
Time Base Generator
Figure 1

4.0 Precision Delay Circuit

Figure 2 is the block diagram of the Precision Delay Circuit. The basic circuit is a gated 4000-count counter that is gated on by a pulse from the G-4 Averaging Circuit and gated off by last count of the counter. The clock input is 200 KC, hence each count represents 5 microseconds. To obtain a delay of from 0 to 20 milliseconds requires the picking out of the 0 to 4000th counts. This is done by gates that are on the set and reset output of each binary counter. The gates are controlled by DC logic from Daven switches. The switches will be wired in such a way that the delay can be set into the system directly.

The first switch will be 0 or 10 milliseconds, the second switch will be 0 through 9 in 1 millisecond steps, the third switch will be 0 through 9 in 100 microsecond steps, the fourth switch will be 0 through 9 in 10 microsecond steps, and the fifth switch will be 0 or 5 microseconds.

The precision delay can be set into the system by the operator in less than 10 seconds.



Precision Delay Circuit
Figure 2

5.0 Pulse Generator and One Millisecond Delay

The reset pulse from the Precision Delay Circuit resets the Time Base Generator to zero count at one millisecond before time zero. The time base output pulses of the Time Base Generator are therefore generated one millisecond before time zero. The basic pulse rate outputs, selected by the Switch Card inserted in the rack, are fed to the Pulse Generator and One Millisecond Delay Circuits. The block diagram of these is shown in Figure 3.

The Pulse Generator Circuit consists of a pulse count divider and pulse shapers. Starting with the basic rate pulses, P, from the Time Base Generator, 200 KC clock pulses are gated into the Pulse Generator and it proceeds to count to 400, i. e., for 2 milliseconds. Pulse outputs are provided at ± 100 , ± 500 and ± 1000 microseconds from time zero, corresponding to counts of 220 and 180, 300 and 100, and 400 and 0, respectively, in the chart in Figure 3. The ± 100 microsecond pulses are for the coincidence checking circuit; the others are for the Camera Shutter Synchronization System.

The One Millisecond Delay Circuit similarly consists of a pulse count divider and a pulse shaper. Starting with the basic rate pulses, which are delayed a half period, $(P + 1/2 T)$, 200 KC clock pulses are gated in and the circuit proceeds to count to 200, or 1 millisecond and an output pulse is provided at time zero plus a half period of the selected basic pulse rate.

All circuit functions are obtained with 3C-Pac S-series Digital Module Cards, as indicated in the block diagram.

6.0 Frequency Standard

The following information was supplied to Link, Palo Alto, by Mr. Bill Wilson of Neely Enterprises:

Hewlett Packard Company 101A 1MC Oscillator will be 1 part in 10^7 in 6 to 8 hours and within specification in 24 hours after being turned on.

Hewlett Packard Company 103AR Quartz Oscillator will be 1 part in 10^7 in 3 hours and within specification in 24 hours after being turned on.

Link, Palo Alto, plans on using the Model 101A in the Ballistic Camera and Synchronization System as the cost is one fifth the cost of the 103AR.

7.0 Camera Shutter Detector

7.1 General

Further tests with the Camera Simulator have been made to determine the output signal characteristics of the variable reluctance pickup at both 10 and 40 exposures per second rates. Particularly at the slower rate, it was found that the tentative method for shutter pulse detection, as described in Progress Report No. 4, would not be feasible because of the sensitivity of that method to any noise that would be introduced in the connecting cables at the low signal levels involved.

Therefore, a new tentative method has been chosen in which the signal from the fast shutter pickup is amplified, the crossover point is detected, and a synchronizing pulse of adequate amplitude is generated at the camera location for transmission over 50 ohm coaxial cable. Except for the slow shutter detection and gate functions, this new method has been built and tested in a breadboard version and was found to perform satisfactorily.

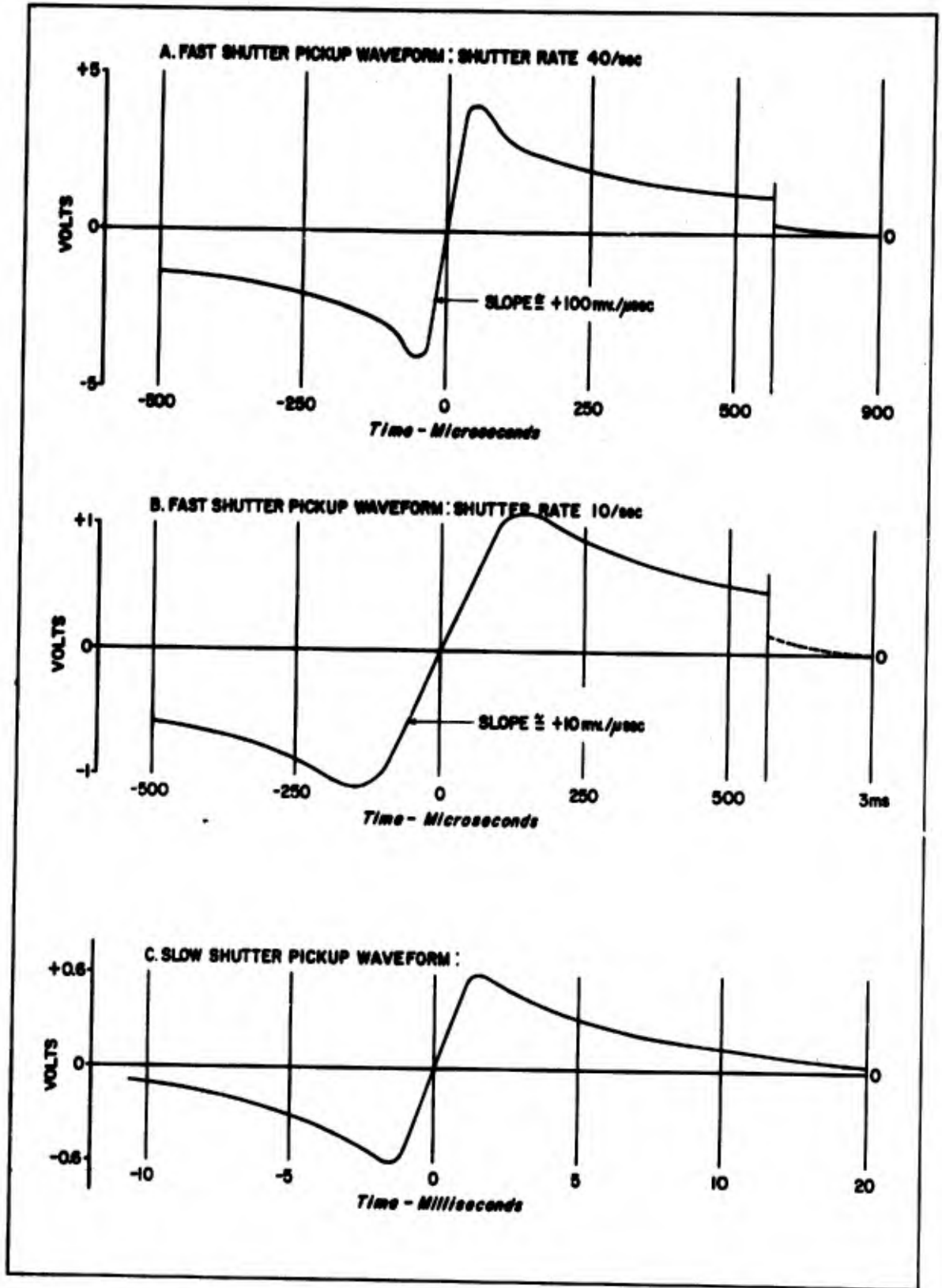
Although this new method is more elaborate than the first method proposed, the elaboration is considered desirable to ensure the required timing accuracy of the shutter sync pulse, on which is based the accuracy of the entire Camera Synchronization System.

7.2 Pickup Signals

In Figure 4-1 are shown the expected waveforms of the camera shutter variable reluctance pickups. In Figure 4-1a and 4-1b are shown the approximate waveforms as obtained with the Camera Simulator for the 40 and 10 per second shutter rates. The slope of these waveforms in the crossover region are approximately +100 millivolts-per-microsecond for the 40 per second rate and +10 millivolts-per-microsecond for the 10 per second rate.

At the 10 per second rate, the output of the fast disc pickup of the Simulator contains about 1 millivolt peak-to-peak noise comprising stray pickup and random variations arising primarily from mechanical jitter of the shutter disc. The effect of this noise is to produce multiple zero crossover points of the waveform, and cause jitter of the first one detected.

Effects of loading on the pickup waveform were observed. It was found that a minimum load resistance of 5000 ohms is required to



Waveforms of Camera Shutter Variable Reluctance Pickups

Figure 4

prevent waveform distortion caused by the inductance of the pickup coil.

7.3 Shutter Detector and Sync Pulse Generator

The block diagram of the new tentative Camera Shutter Detector and Sync Pulse Generator is given in Figure 5 and its operation is illustrated graphically by the waveforms shown in Figure 6. In Figure 6, the waveforms are identified by letters which correspond with the lettered locations on the block diagram of Figure 5.

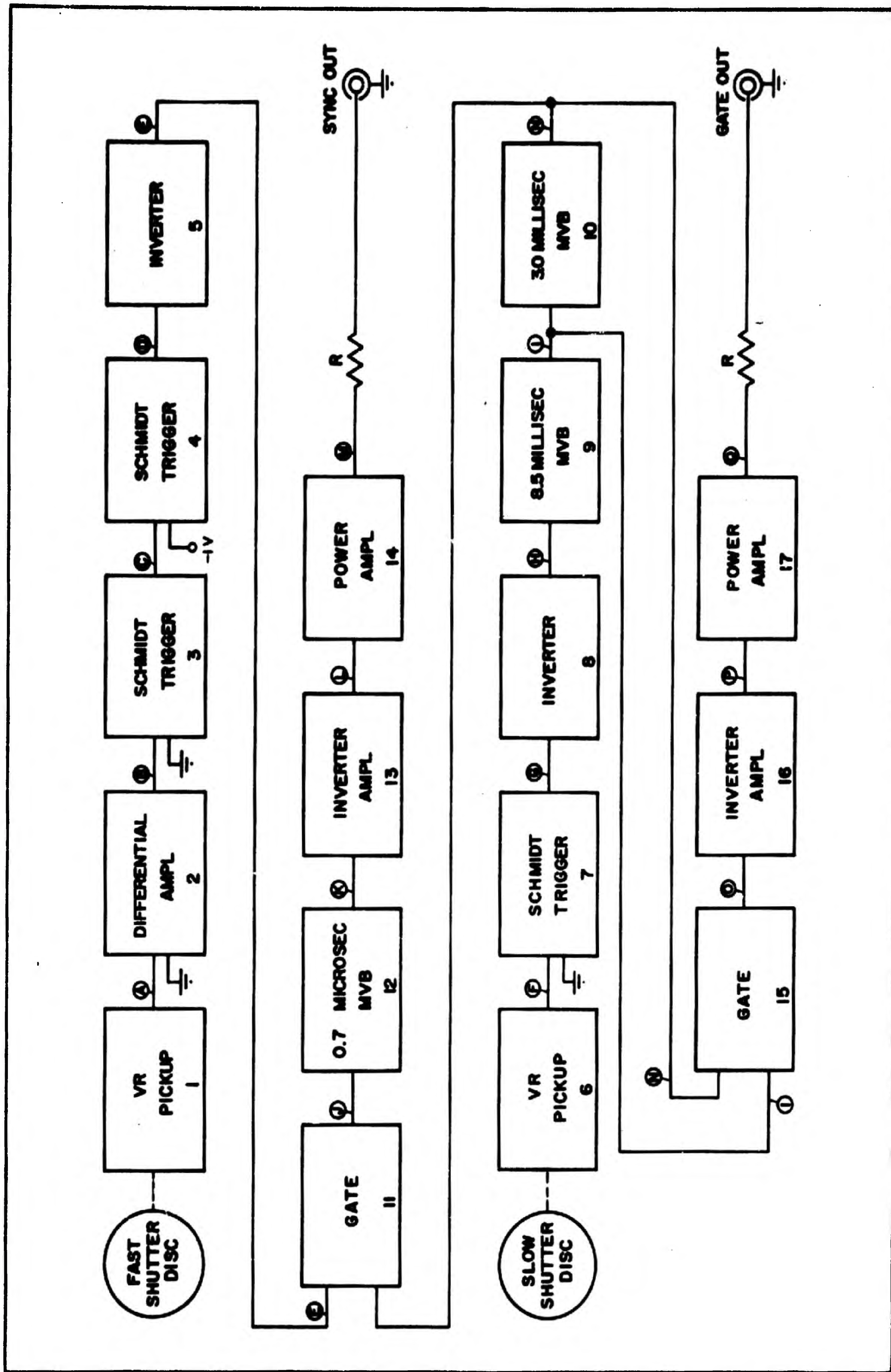
All circuit functions shown in Figure 5 are obtained with Computer Control Company 3C-Pac Series S Digital Module Plug-in Cards - except for the Differential Amplifier. The Differential Amplifier, which has been designed, constructed and tested in breadboard fashion will be fabricated for the prototype on a plug-in card similar to the 3C-Pac cards. All cards will be inserted in a card cage, which, together with a 3C power supply, will be mounted in available rack space in the Camera Astrodome.

The following ten plug-in cards will be required:

<u>Quantity</u>	<u>Type No.</u>	<u>Module Type</u>	<u>Circuits Per Board</u>
1 ea	Link	Differential Amplifier	1
2 ea	3C ST-30	Schmidt Trigger	2
1 ea	3C DI-30	Inverter/gate	8
2 ea	3C DM-30	Delay Multivibrator	2
2 ea	3C PA-30	Power Amplifier	4
1 ea	Link	Resistor Board	-
1 ea	Link	Capacitor Board	-

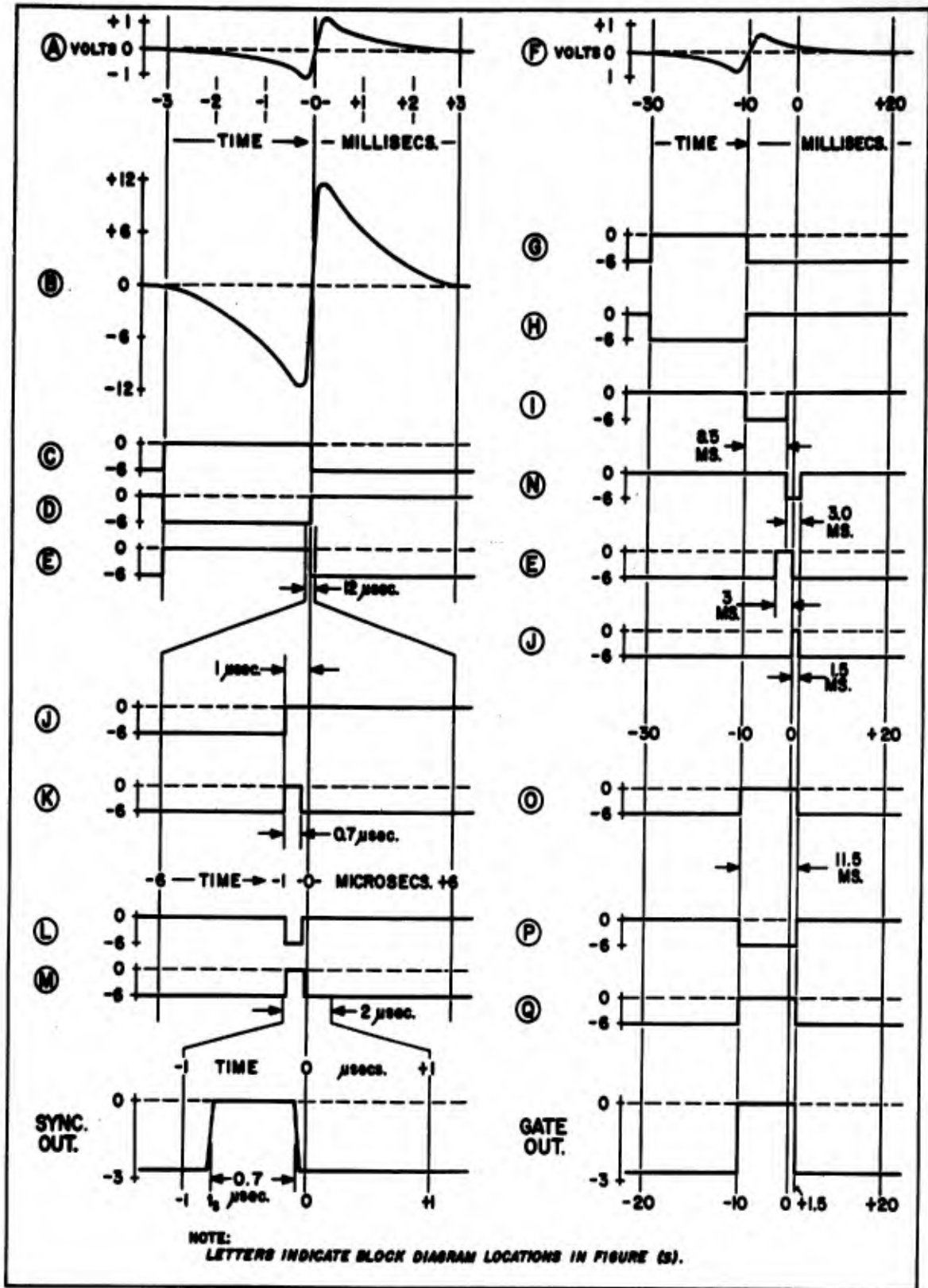
7.4 Differential Amplifier (Block 2, Figure 5)

With the proposed method, a preamplifier is required to amplify the pickup output, particularly at the slower shutter disc speeds and to prevent loading



Proposed Camera Shutter Detector and Sync Pulse Generator Block Diagram

Figure 5



Signal and Pulse Waveforms

Figure 6

the pickup output. The signal must be amplified sufficiently to provide a slope of at least 100 millivolts per microsecond in the zero crossover region and have a total drift and distortion of less than 100 millivolts at the input to the Schmidt Trigger to obtain the required detected timing accuracy of 5 microseconds (± 2.5 microseconds).

A preamplifier circuit meeting these requirements has been designed and a breadboard version using germanium transistors has been tested and found satisfactory, but with marginal stability. A silicon transistor version is being designed and no difficulty in achieving adequate stability is expected. The preamplifier design utilizes a direct-coupled differential amplifier in an operational amplifier circuit with overall negative feedback. The feedback stabilizes the input impedance and gain and reduces drift and output impedance.

It is planned that a separate preamplifier card will be furnished for each fast shutter disc rate. Each card will have the amplifier gain adjusted to correspond with the pickup signal amplitude obtained at that shutter disc rate.

7.5 Sync Pulse Generation

A 0.7 microsecond sync pulse will be produced at the SYNC OUT jack for each fast shutter crossover occurring between 8.5 and 11.5 milliseconds after a slow shutter crossover. Referring to Figures 5 and 6, the zero crossover of the slow shutter pickup output (F) is detected by the Schmidt Trigger (7) to initiate the 8.5 millisecond delay (I) followed by a 3.0 millisecond pulse (N). This is applied to the gate (11) to permit the detected zero crossover (E) of the fast shutter pickup output (A) to trigger the 0.7 microsecond pulse-forming multivibrator (12).

The zero crossover of the amplified output (B) of the fast shutter pickup (1) is detected by the two Schmidt Triggers (3 and 4). For accurate zero crossover detection, the first Schmidt Trigger must be operated with minimum hysteresis, making it sensitive to multiple crossovers caused by noise (see Section 7-2). Noise immunity is obtained with the second Schmidt Trigger by giving it a greater hysteresis.

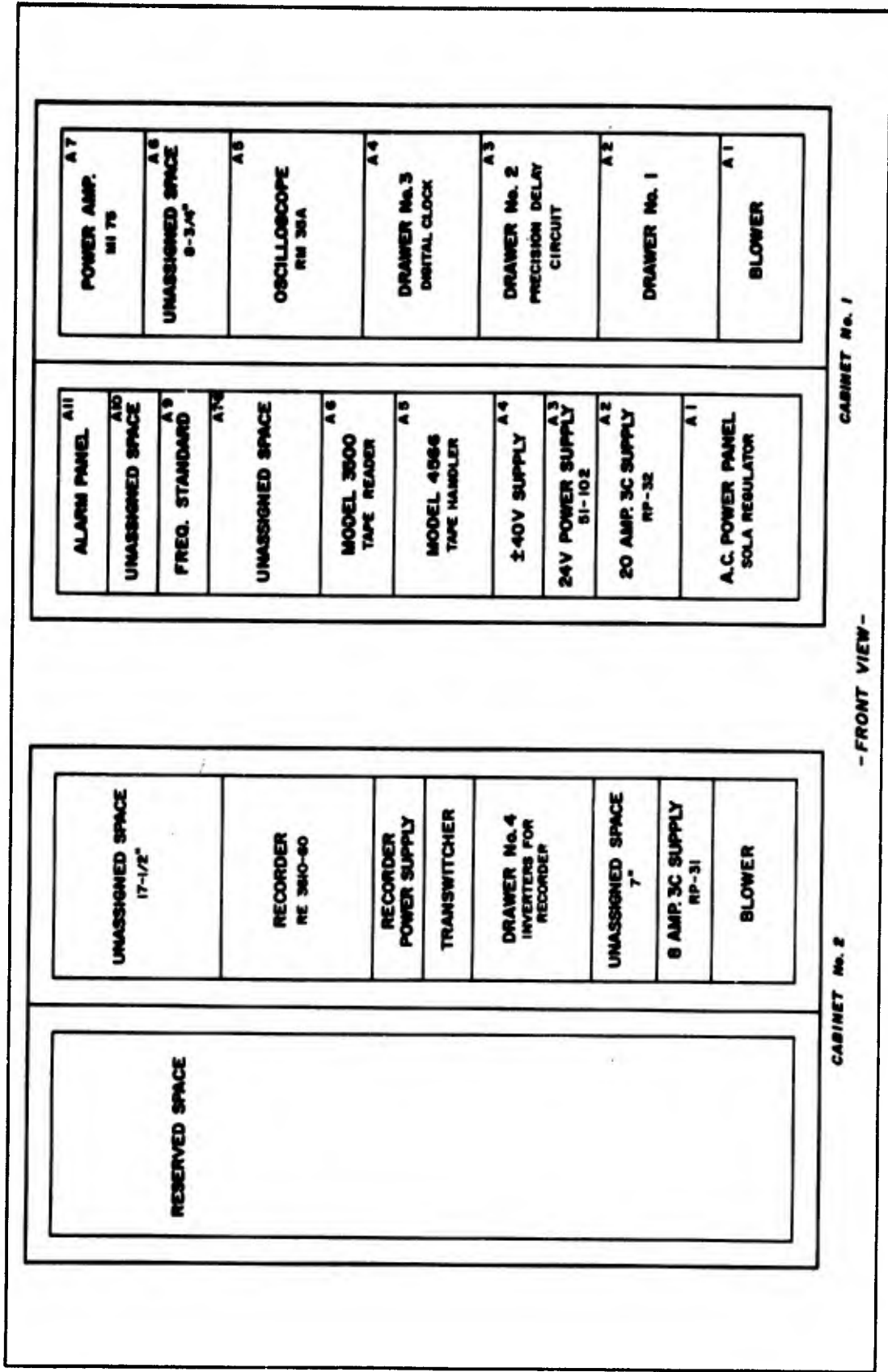
The 8.5 millisecond delay (I) and 3.0 millisecond delay (N) are added in the gate (15), to form a combined pulse of 11.5 milliseconds duration for transmitting to recording equipment. The start of this pulse corresponds to the slow shutter crossover and the end indicates the closing of the fast pulse gate (11).

Both the 0.7 microsecond sync pulse and the 11.5 millisecond gate pulse are passed through power amplifiers (14 and 17), the outputs of which are impedance matched by resistors (R) to the 50 ohm coax outputs.

Referring to Figure 6 (SYNC OUT waveform), the leading edge of the sync pulse will be used as the synchronous time (t_s) for camera synchronizing. By bias adjustment of the differential amplifier or Schmidt Trigger, the trigger time can be advanced with respect to the actual fast shutter crossover time, as indicated, to compensate for accumulated delays in the switching circuits and transmission cable.

8.0 Layout of the Racks

Figure 7 is the proposed layout of the racks. The position of the units in the racks was chosen to insure optimum operation of the equipment and to minimize the signal lead lengths. This layout is not final; the layout will be finalized after White Sands Missile Range has given its comments on the proposed layout.



Layout of Racks
Figure 7

9.0 Program for Subsequent Reporting Period

If all of the components are received on time, the Resolver Servo will be assembled. The circuits mentioned in this progress report will be tested further to insure their reliability. Link Division, General Precision, Inc., Palo Alto, will respond to the White Sands Missile Range Technical Exhibit B during the month of September, 1961.

10.0 Program Schedule

Figure 8 shows the planned program for the design and construction of the prototype of the Ballistic Camera Synchronization and Control System as of August 31, 1961.

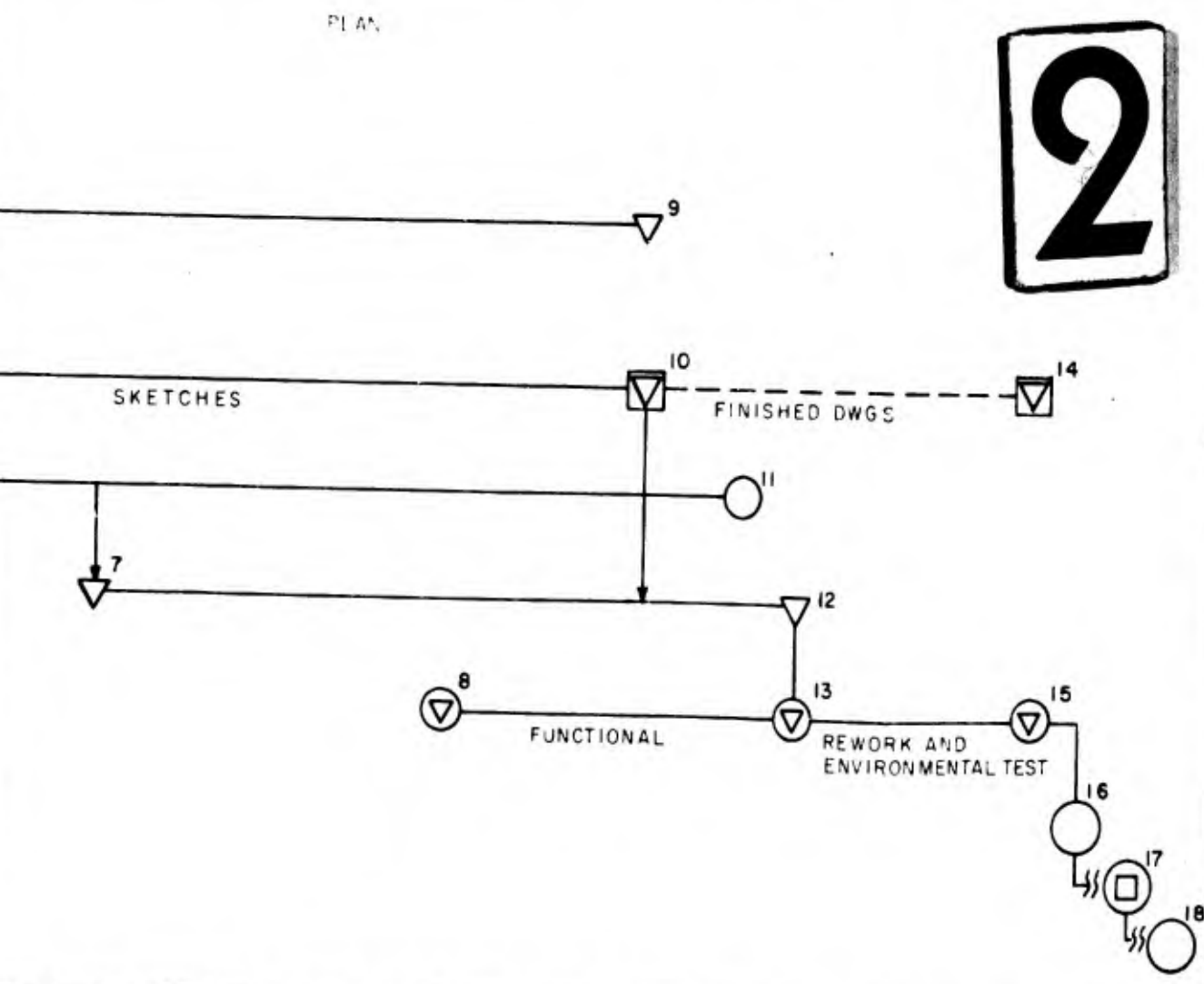
4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

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-  CUSTOMER SUPPORT
-  CUSTOMER ACTION
-  VENDOR OR SUB-CONTRACT ACTION
-  CONTRACTUAL ACTION
-  PROCUREMENT ACTION
-  FABRICATION OF ASSEMBLY
-  PURCHASE PARTS
-  COMPANY MADE PARTS
-  REPORT TO CUSTOMER
-  TEST OR INSPECT
-  STUDY OR ANALYSIS
-  SYSTEMS DESIGN OR DEVELOPMENT
-  DETAIL DESIGN
-  INTERNAL TRANSFER
-  RAW MATERIAL



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 SEPT 1 8 15 22 29
 OCT 6 13 20 27
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 DEC 1 8 15 22 29
 JAN 5
 60 DAYS AFTER CUSTOMER ACC

WORKING PERIOD PRIOR TO SHIPMENT

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