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IONOSPHERIC RESEARCH

Scientific Report No. 153

PHASE DISTORTION IN HIGH FREQUENCY TRANSISTOR AMPLIFIERS

by

T. A. Seliga

December 1, 1961

MOTHER-DAUGHTER PROJECT



IONOSPHERE RESEARCH LABORATORY



University Park, Pennsylvania

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Scientific Report

on

"Phase Distortion in High Frequency
Transistor Amplifiers"

by

T. A. Seliga


1 December 1961

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Ionosphere Research Laboratory

Mother-Daughter Project

Submitted by:



J. S. Nisbet, Assistant Professor of
Electrical Engineering, Project Supervisor

Approved by:



A. H. Waynick, Professor of Electrical
Engineering, Director, IRL

The Pennsylvania State University
College of Engineering and Architecture
Department of Electrical Engineering

ABSTRACT

An analysis of phase distortions occurring in high frequency transistor amplifiers resulting from the application of automatic gain control is presented.

The analysis is based on the expression for the current gain of the amplifier. Verification of the theory is made by comparing calculated and measured phase shifts in single amplifiers and a receiving system.

The problems of choosing the most suitable type of automatic gain control system, and transistor, based on a minimum phase distortion criteria are also considered.

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CHAPTER 1

INTRODUCTION

1.1 ORIGIN OF THE PROBLEM

In a high altitude rocket experiment proposed by Nisbet (1960) to measure electron density in the ionosphere, accurate phase measurements are required at three harmonically related frequencies. The signals received at each frequency vary independently in amplitude due to ionospheric propagation effects.

It is necessary to measure the amplitude of the signal strength at each frequency and to insure that the outputs of the receivers fall within the operating ranges of the phase comparators connected to their outputs. An automatic gain control (AGC) system is thus required for each receiver.

Restrictions on size, weight and power of the rocket payload necessitate the use of transistorized receivers. Unfortunately, phase shifts are introduced by the transistor amplifiers when the input signal strength fluctuates. Because of the importance of the phase measurements, it is necessary to be able to calculate and minimize the phase shifts introduced by transistorized receivers having AGC.

1.2 RELATED FIELDS OF APPLICATION

The importance of determining and analyzing the phase characteristics of transistor amplifiers is not limited to the proposed rocket experiment. For example, phase modulation receivers must be free of any phase shifts caused by

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by selecting a suitable automatic gain control system
and transistor are considered.

A bridge-type AGC circuit, used to control the amplitude of vacuum tube crystal oscillators, is described in the M.I.T. Radiation Laboratory Series. The circuit, which provides phase stability as well as AGC, was used in an oscillator circuit as part of the original Loran equipment.

2.2 CHARACTERISTICS OF VACUUM TUBE AGC CIRCUITS

In order to understand and/or analyze the characteristic behavior of a vacuum tube AGC system, the effects of DC bias on the tube parameters must be known. Ballantine (1919) was the first to investigate variations in mutual conductance (g_m), plate resistance (r_p), and internal impedance of a vacuum tube with bias. Ballantine and Snow (1930) measured the effects of increasing negative control-grid bias on amplitude modulated RF signals. They discovered distortion and increased intermodulation effects due to a nonlinear relationship between the input and output of the amplifier.

Llewellyn (1934) analyzed and measured the relationship between the phase angle of g_m and plate current, filament current, and grid potential. Strutt and Van Der Ziel (1939), Jones (1937), and Freeman (1938), investigated capacitance and conductance changes in vacuum tubes as functions of bias. Freeman discussed the effects which input capacitance has on the tuning of the IF stages of a superheterodyne receiver, and suggested compensating for the changes in capacitance with negative feedback.

2.3 AGC IN TRANSISTOR AMPLIFIERS

Several methods of controlling the gain of transistor amplifiers are available. The commonest methods depend on the variation of transistor parameters with bias; lowering the emitter current or collector voltage causes a reduction in gain. Other means of gain control which are not dependent on changing transistor bias have also been devised. Electrically controllable circuit elements effect gain control by using them as variable attenuators.

Blecher (1953) described a method for controlling the gain of a junction transistor by changing the emitter current. A common base stage was analyzed and it was shown that under certain circumstances the voltage gain was proportional to the emitter current.

Stern and Raper (1954) indicated that the gain can be controlled by varying the collector voltage. Chow and Stern (1955) discussed both emitter current and collector voltage control, and gave a qualitative analysis of the gain dependence on these parameters using the experimentally observed behavior of the hybrid (h) parameters. They also considered the effects of gain control on distortion and bandwidth. When using emitter current as the controlling parameter, they found an increase in both input and output impedance which resulted in an increase in effective Q and a decrease in bandwidth. Collector voltage control, on the other hand, was accompanied by a decrease in transistor impedances which caused a decrease in effective Q

and an increase in bandwidth. In both cases detuning was observed because of changes in the reactive components of the transistor impedances.

Dement'Yev (1959) examined the influence of the emitter current and collector voltage on gain and non-linear distortions. It was shown that for small emitter currents the non-linearity was dependent on the emitter characteristics while in the region of small collector voltage the collector characteristics predominate.

Hurtig (1955) compensated input resistance variations with AGC current by shunting the emitter-base junction with an oppositely polarized diode, which acted as a variable resistor. Hopper (1960) improved Hurtig's circuit, presented an analysis of the input circuit, and measured bandshape distortion and compression characteristics.

Shea illustrates a circuit which uses a normally reverse-biased diode in parallel with the load of a common emitter IF stage. For low input levels AGC is obtained by collector voltage control; strong signals cause the diode to become forward-biased and shunt the load.

Brown (1959) discussed a gain control system which used the insertion of electrically controllable impedances as attenuators. The semiconductor diode with its small signal reactance is used as the electrically controlled impedance. AGC characteristics are given for several diode resistance configurations.

CHAPTER 3

HIGH FREQUENCY TRANSISTOR AMPLIFIER DESIGN

In the analysis discussed in this and subsequent sections, the hybrid-pi equivalent circuit of the transistor as developed by Giacoletto (1954), is used. Since the hybrid-pi parameters are almost independent of frequency and are simply related to the DC bias currents and voltage, they are well adapted to this problem. In their original form the parameters are somewhat cumbersome. Therefore the Y parameters derived from the hybrid-pi circuit are also employed.

Appendix A contains a discussion of the Giacoletto hybrid-pi circuit and the relations between its parameters and operating conditions. The effects of neutralization and the relationships between the Y parameters are also given.

3.1 CHOICE OR AMPLIFIER CONFIGURATION

The common emitter amplifier configuration was used in this study because it neutralizes easily and provides less variation in gain and bandwidth for given transistor parameter variations than are obtained using the common base configurations, (Gray and Lawson).

3.2 TRANSISTOR OPERATING CONDITIONS

The optimum DC operating conditions for a transistor are generally recommended by the manufacturer. In this bias state the transistor usually exhibits the largest practicable

gain. Included in the manufacturer's specifications are input and output resistance, input and output capacitance, and the matched, neutralized power gain as a function of frequency. From these characteristics and specified design criteria a high frequency tuned amplifier can be designed.

3.3 ASSUMPTIONS

Autotransformer coupling is used to obtain a conductance match between source and input, and output and load. Figure 1 illustrates a typical high frequency single tuned amplifier circuit. It is assumed that the input terminals are fed from the output of an equivalent amplifier, and that the amplifier output is connected to the input of an equivalent amplifier. The DC operating conditions, frequency, and loaded Q of the interstage network are specified. Tuning is accomplished by adjusting C_T , the tuning capacitance.

3.4 GAIN

To obtain maximum power gain the turns ratio of the autotransformer is chosen to effect a conductive match between output and input,

$$n^2 = \frac{G_1'}{G_2'} \quad (1)$$

where G_1' and G_2' are the equivalent input and output conductances respectively of the neutralized amplifier. The power available from the transistor, assuming no losses, is then

$$P = \frac{|I^2|^2}{4G_2'} \quad (2)$$

where I is the equivalent output current source of the amplifier.

3.5 EFFECTIVE Q OF INTERSTAGE (Q_L)

The effective Q of the interstage or loaded Q referred to the primary is determined from the required bandwidth (B) and operating frequency (f) by

$$Q_L = \frac{f}{B} \quad (3)$$

Figure 2 illustrates the equivalent output circuit of a HF single tuned transistor amplifier under matched conditions. In terms of the parameters of this circuit the loaded Q becomes

$$Q_L = \frac{1}{\omega L' G_2' (2 + \alpha)} \quad (4)$$

where L is the inductance of the autotransformer winding referred to the transistor output terminals and $\alpha G_2'$ represents the equivalent loss conductance of the transformer.

For reasonable values of the unloaded Q factor (Q_u) of the autotransformer winding,

$$L' = L \left(1 + \frac{1}{Q_u^2} \right) \approx L$$

where L is the inductance of the winding. Also, for design purposes it may be assumed that $\alpha G_2'$ is negligible compared with $2G_2'$. Therefore, the desired autotransformer winding inductance is

$$L = \frac{1}{2G_2' \omega Q_L} \quad (5)$$

The total capacitance (C') required to tune the circuit is then given by

$$C' = \frac{1}{\omega^2 L} \quad (6)$$

and includes the transistor output capacitance, the input capacitance of the following stage transferred to the primary, and a tuning capacitance (C_T).

3.6 LOSSES IN AUTOTRANSFORMER

As mentioned in Section 3.5 the equivalent loss conductance of an autotransformer may be written as $\alpha G_2'$. Defining Q_L' as the loaded Q of the output circuit when $\alpha G_2' = 0$.

$$Q_L' = \frac{1}{\omega L \alpha G_2'} \quad (7)$$

α and the effective loaded Q become

$$\alpha = \frac{2Q_L'}{Q_u} \quad (8)$$

and

$$Q_L = \frac{Q_u Q_L'}{Q_u + Q_L'} \quad (9)$$

It is desirable to determine the effect of a finite Q_u on the power transfer efficiency (η) of the coupling network. η is defined as the ratio of P_L , the power delivered to the load, to P_A , the power available from the source;

$$\eta = \frac{P_L}{P_A} = \left(1 - \frac{Q_L}{Q_u}\right)^2 \quad (10)$$

The important implication of Equation 10 is that maximum

efficiency occurs when the ratio $\frac{Q_L}{Q_u}$ is a minimum. Therefore large Q_L or a very narrow bandwidth specification requires a very large unloaded Q of the transformer in order to effect a reasonable η . Obviously these are conflicting requirements, because of physical limitations of components, and a compromise must be found.

3.7 SAMPLE DESIGN PROBLEM

A transistor amplifier is to be designed using a 2N1271 transistor and operated at a center frequency of $f = 6$ mc/s. The transistor quiescent conductances are known. The effective Q of the interstage coupling network is 10. It is necessary to determine L , the inductance of the autotransformer; C_T , the tuning capacitance; n , the turns ratio; and the minimum Q_u required to obtain an $\eta > 0.8$.

$$\text{Output Conductance} \quad G_2' = 1.6 \times 10^{-4} \text{ mhos.}$$

$$\text{Input Conductance} \quad G_1' = 1.9 \times 10^{-3} \text{ mhos.}$$

$$\text{Output Capacitance} \quad C_2' = 15 \text{ pf.}$$

$$\text{Input Capacitance} \quad C_1' = 30 \text{ pf.}$$

The turns ratio of the autotransformer is obtained from Equation (1):

$$n^2 = \frac{G_1'}{G_2'} = \frac{1.9 \times 10^{-3}}{1.6 \times 10^{-4}} \approx 11.8$$

$$n \approx 3.5$$

The inductance is found from Equation (5):

$$L = \frac{1}{2G_2' Q_L \omega} = \frac{1}{3.2 \times 10^{-4} ((10)(6)(6.28 \times 10^6))}$$

$$= 8.3 \times 10^{-6} = 8.3 \mu\text{h.}$$

The lower limit on Q_u is determined by making

$$\eta = \left(1 - \frac{Q}{Q_u}\right)^2 > 0.8$$

$$1 - \frac{Q}{Q_u} > .894$$

$$Q_u > \frac{10}{.106} = 94.5$$

The required total capacitance to tune is

$$C' = \frac{1}{\omega^2 L} = \frac{1}{(1.41 \times 10^{15})(8.3 \times 10^{-6})}$$

$$C' \approx 94 \text{ pf.}$$

Since

$$C = C_2' + \frac{1}{n^2} C_1' + C_T,$$

the required tuning capacitance

$$C_T = C - C_2' - \frac{1}{n^2} C_1'$$

$$\approx 94 - 15 - \left(\frac{1}{11.8}\right) 30$$

$$\approx 94 - 15 - 2.5 = 77 \text{ pf.}$$

CHAPTER 4

INPUT AND OUTPUT IMMITTANCE VARIATIONS OF A
TYPICAL TRANSISTOR

4.1 HYBRID-PI PARAMETERS OF 2N1271

The transistor type used in this work was the Philco 2N1271, a silicon n-p-n Surface Alloy Diffused Base transistor having an f_{max} of approximately 100 mc/s, and 150 mw. total power dissipation at 25°C. The average hybrid-pi parameters at 25°C, as derived from the manufacturer's data sheets are:

$$r_{b'1} = 200 \text{ ohms}$$

$$r_{b'e} = 390 \text{ ohms}$$

$$C_{b'e} = 47 \text{ pf}$$

$$r_{b'c} = 1M \text{ ohms}$$

$$C_{b'c} = 1 \text{ pf}$$

$$r_{ce} = 30K \text{ ohms}$$

$$g_m = 25,000 \text{ } \mu\text{mhos.}$$

Bias Conditions

$$I_e = 2\text{ma}$$

$$V_c = 10 \text{ volts}$$

From these values the constants relating the parameters to I_e and V_c (Appendix A) were determined, and the variations in parameters calculated. The results are given in Figures 3 through 9, and illustrate the dependence of the hybrid-pi parameters on bias.

4.2 INPUT AND OUTPUT IMMITTANCES

Using the assumptions that the amplifier is unilateralized for all bias conditions, the equivalent parallel output and input impedances and mutual conductance were calculated from Equations (A34), (A35) and (A36) of Appendix

A7 as a function of emitter current for the circuit of Figure 1. The results are illustrated in Figures 10 through 14 for two different frequencies — 184.7 kc/s and 6.133 mc/s. Because of the presence of R_c , the values of the parameters for $I_e > 2\text{ma}$ represent the condition for forward AGC (collector voltage control). When $I_e < 2\text{ma}$, the operating range of collector voltage is normal, and the condition represents reverse AGC (emitter current control).

The frequency characteristics of the impedances and mutual conductance were also determined and are given in Figures 15, 16 and 17.

CHAPTER 5

ANALYSIS OF TRANSISTOR AMPLIFIER

PHASE CHARACTERISTICS

Figure 18 illustrates a transistor amplifier connected in cascade with similar amplifiers having the same characteristics. The amplifier is represented by its Y parameters. A coupling network, consisting of an ideal transformer and a tuning admittance, is connected to the output to effect an impedance match between stages. Each amplifier is assumed unilateralized, regardless of any changes in bias which are used to obtain gain control. This approximation is discussed in Section A6. Following is a list of definitions pertaining to the Figure:

$Y_{11} = G_1 + jB_1$ - input admittance.

Y_{12} - reverse transfer admittance; equals zero when the amplifier is unilateralized.

Y_{21} - forward transfer admittance; mutual conductance.

$Y_{22} = G_2 + jB_2$ - output admittance.

Y - admittance connected to the output of each stage; consists of a conductance, representing the losses in the coupling network, and a susceptance required to tune out the quiescent susceptive components of Y_{22} and $\frac{1}{n^2} Y_{11}$. $\frac{1}{n^2} Y_{11}$ is the input admittance transferred to the output.

n - turns ratio of ideal transformer; it is equal to the ratio of the quiescent input and output conductances.

I_1 - output current of the preceding stage.

I_2 - output current.

Primed values are used to represent the initial parameters. From these the values of n and Y are found to be:

$$n = \sqrt{\frac{G_1'}{G_2'}} \quad (11)$$

and

$$Y = \frac{2G_2'}{\frac{Q_u}{Q_L} - 1} - j \left(B_2' + \frac{1}{n^2} B_1' \right) \quad (12)$$

$$= \alpha G_2' - j \left(B_2' + \frac{1}{n^2} B_1' \right)$$

where Q_u is the Q of the coupling transformer, Q_L is the initial loaded Q referred to the primary, and $\alpha = \frac{2}{Q_u/Q_L - 1}$.

Expressions for the phase shift in amplifier (T_1), due to changes in the parameters, are derived from the current gain ($\frac{I_2}{I_1}$) for three cases:

- A. T_1 varying; T_2 not varying.
- B. T_1 and T_2 varying.
- C. T_1 not varying; T_2 varying.

For this particular study the parameter variations are due to the application of AGC to the stages.

The current gain ($\frac{I_2}{I_1}$) is given by

$$\frac{I_2}{I_1} = \frac{+Y_{21} Y_L}{n \left(Y + \frac{1}{n^2} Y_{11} \right) (Y_L + Y_{22})} \quad (13)$$

where Y_L is the load admittance,

$$Y_L = Y + \frac{1}{n^2} Y_{11} \quad (14)$$

The phase shift ($\Delta\phi$), relative to the phase in the quiescent state, is obtained by calculating the phase of the current gain (ϕ) and subtracting from it the phase of the quiescent current gain (ϕ'). Therefore, the phase shift can be written as

$$\Delta\phi = \phi - \phi' = \angle \frac{I_2}{I_1} - \angle \frac{I_2'}{I_1'} \quad (15)$$

Since the current gain is equal to a product of several factors, the phase is just the sum of the phases of each of the factors, i.e.,

$$\phi = \angle Y_{21} + \angle Y_L - \angle \left(Y + \frac{1}{n^2} Y_{11} \right) - \angle Y_{22} \quad (16)$$

5.1 CASE A: T_1 VARYING, T_2 NOT VARYING

In this case the parameters which change are Y_{11} and Y_{22} , and the phase shift in the amplifier is given by

$$\Delta\phi = - \angle \left(Y + \frac{1}{n^2} Y_{11} \right) - \angle Y_{22} + \angle \left(Y + \frac{1}{n^2} Y_{11}' \right) + \angle Y_{22}' \quad (17)$$

Appropriate substitution of the parameters in Equation (17) gives

$$\Delta\phi = - \tan^{-1} \frac{\frac{1}{n^2} (B_1 - B_1') - B_2'}{\frac{1}{n^2} G_1 + G_2'} \alpha - \tan^{-2} \frac{B_2 - B_2'}{G_2 + G_2'} (1 + \alpha) + \tan^{-1} \frac{-B_2'}{G_2' (1 + \alpha)} \quad (18)$$

5.2 CASE B: T_1 AND T_2 VARYING

The dependent variables are Y_L , Y_{11} , and Y_{22} .
However, since

$$Y_L = Y + \frac{1}{n^2} Y_{11},$$

the expression for the current gain reduces to

$$\frac{I_2}{I_1} = \frac{Y_{21}}{n(Y_L + Y_{22})} \quad (19)$$

and the phase shift becomes

$$\Delta\phi = - \angle Y_L + Y_{22} + \angle Y_L' + Y_{22}'$$

or

$$\Delta\phi = - \tan^{-1} \frac{(B_2 - B_2') + \frac{1}{n^2}(B_1 - B_1')}{\frac{1}{n^2} G_1 + G_2 + \alpha G_2'} \quad (20)$$

5.3 CASE C: T_1 NOT VARYING, T_2 VARYING

The phase shift in this case is due to changes in Y_L only;

$$\Delta\phi = \angle Y_L - \angle Y_L' - \angle Y_L + Y_{22}' + \angle Y_L' + Y_{22}' \quad (21)$$

In terms of the parameters,

$$\Delta\phi = \tan^{-1} \frac{\frac{1}{n^2} (B_1 - B_1') - B_2'}{\frac{1}{n^2} G_1 + \alpha G_2'} - \tan^{-1} \frac{-B_2'}{G_2' (1 + \alpha)} - \tan^{-1} \frac{\frac{1}{n^2} (B_1 - B_1')}{\frac{1}{n^2} G_1 + G_2' (1 + \alpha)} \quad (22)$$

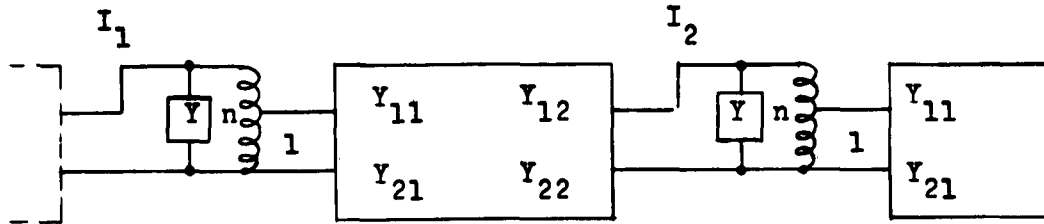
5.4 SUMMARY OF ANALYSIS

The results of the three cases are summarized in Table 1. The method employed here to obtain expressions for the phase shift in transistor amplifiers is also applicable to other types of coupling and when the assumption of unilateralization no longer valid. The condition for unilateralization is that the product $Y_{12}Y_{21}$ be negligible compared with $(Y + \frac{1}{n^2} Y_{11})(Y_L + Y_{22})$. Consequently, for the case where this assumption is not valid the phase contribution from the denominator of the current gain expression is

$$\phi_D = \frac{(Y + \frac{1}{n^2} Y_{11})(Y_L + Y_{22}) + Y_{12}Y_{21}}{\quad} \quad (23)$$

where D signifies the denominator. A second assumption in the analysis was that Y_{21} did not alter its phase. If Y_{21} should change phase, its phase shift contribution is simply added to the derived phase shifts.

TABLE 1



Current Gain:

$$\frac{I_2}{I_1} = \frac{Y_{21} Y_L}{n(Y + \frac{1}{n^2} Y_{11})(Y_L + Y_{22})}$$

Note:

$$Y_{11} = G_1 + jB_1$$

$$Y_{12} = 0$$

$$Y_{22} = G_2 + jB_2$$

$$Y_{21} = G_m + j0$$

$$n^2 = G_1' / G_2'$$

Primed Values are Quiescent

Q_u = Q of Coupling Autotransformer

Q_L = Loaded Q Referred to Primary

$$\alpha = \frac{2}{Q_u / Q_L - 1}$$

Case AGC Applied To

Phase Shift in T_1 ($\Delta\phi$)

$$-\tan^{-1} \frac{\frac{1}{n^2}(B_1 - B_1') - B_2'}{\frac{1}{n^2}G_1 + \alpha G_2'} \quad -\tan^{-1} \frac{B_2 - B_2'}{G_2 + G_2'(1 + \alpha)}$$

$$+\tan^{-1} \frac{-B_2'}{G_2'(1 + \alpha)}$$

A T_1

Phase Shift Formulae for A Transistor Amplifier Connected in

Cascade with Similar Amplifiers

Table 1 - continued

<u>Case</u>	<u>AGC Applied To</u>	<u>Phase Shift in T_1 ($\Delta\phi$)</u>
B	T_1 and T_2	$-\tan^{-1} \frac{(B_2 - B_2') + \frac{1}{n^2} (B_1 - B_1')}{\frac{1}{n^2} G_1 + G_2 + \alpha G_2'}$
C	T_2	$\tan^{-1} \frac{\frac{1}{n^2} (B_1 - B_1') - B_2'}{\frac{1}{n^2} G_1 + \alpha G_2'} - \tan^{-1} \frac{-B_2'}{G_2(1+\alpha)}$ $-\tan^{-1} \frac{\frac{1}{n^2} (B_1 - B_1')}{\frac{1}{n^2} G_1 + G_2'(1+\alpha)}$

CHAPTER 6

COMPARISON OF ANALYSIS AND EXPERIMENTAL RESULTS

6.1 APPLICATION OF THEORY

The phase shifts in typical single tuned amplifiers at 184.7 kc/s and 6.133 mc/s were calculated as a function of emitter current using the 2N1271 transistor characteristics. The basic amplifier circuit is shown in Figure 1. The change in bias is accomplished by applying a control current to the base through a high impedance source.

The reference quiescent state of the transistor was chosen as $I_e = 2$ ma and $V_c = 7$ volts.

The specifications for each of the amplifier's interstage coupling networks are:

	$f = 184.7$ mc/s	$f = 6.133$ mc/s
Loaded Q	$Q_L = 10$	$Q_L = 10$
Unloaded Q of Autotransformer Winding	$Q_u = 150$	$Q_u = 80$
Loss Coefficient	$\alpha = 0.143$	$\alpha = 0.287$

Unilateralization was assumed to hold over the entire range of emitter current.

R_c , the external collector resistance, was assumed equal to 2K ohms and R_e , the emitter resistance, was made equal to 470 ohms. Due to the voltage drop in these resistors an increase in emitter current caused a decrease in collector voltage. Decreasing the emitter current increased the collector voltage, but this had little effect on the transistor parameters. Thus, emitter currents greater than about 2 ma corresponded to forward AGC, and emitter

currents less than about 2 ma corresponded to reverse AGC.

The phase shift in each amplifier was calculated using the following procedure:

1. The hybrid-pi parameters were calculated as a function of emitter current for the particular amplifier circuit, taking into account any change in collector voltage due to R_c and R_e .
2. The Y parameters, Y_{11} , Y_{22} , and Y_{21} , of the amplifier were calculated from Equations (A34), (A35), and (A36) (Appendix A7) as a function of emitter current.
3. The turns ratio of the autotransformer was calculated using Equation 1.
4. The equivalent admittance Y connected at the output of each stage was calculated. This represents the losses of the coupling network and the susceptance necessary to tune out the quiescent susceptive component of the output and transferred quiescent input admittances. This is a constant of the interstage networks used to couple the amplifier stages.
5. The appropriate values of the Y parameters were substituted into Equations 18, 20, and 22 to obtain the phase shift as a function of emitter current for each of the cases, A, B, and C.

The results of these calculations for the two amplifiers are given in Figures 19 and 20. In each type of AGC the sense of the phase shifts is different. For forward AGC and equal changes in emitter current the 6.133 mc/s amplifier experienced a maximum phase shift of -60° while the 184.7 kc/s amplifier had a maximum phase shift of -20° . For reverse AGC and a decrease in the emitter current from 2 ma to 0.1 ma the phase shifts were approximately 80° and 48° for the 6.133 mc/s and 184.7 kc/s amplifiers respectively. The above values correspond to Case A, T_1 varying.

The phase shifts for Case B were nearly the same as those for Case A, while Case C's phase shifts were much smaller and of opposite polarity to Cases A and B.

6.2 VERIFICATION OF PHASE SHIFT CALCULATIONS (SINGLE AMPLIFIER)

In order to verify the results of the calculations and analyses of the previous sections the phase and gain characteristics of two similar amplifiers were measured. Figure 21 shows a block diagram of the system used to measure the characteristics of a single amplifier. The signal generator provided a phase reference, and the attenuator enabled the input to the amplifier to be varied without changing the source impedance. The output was kept constant by varying the gain control signal. Changes in the output phase of the amplifier were measured by driving identical horizontal and vertical amplifiers of a Tektronix

536 Oscilloscope with the signal generator and amplifier output signals respectively, and recording the resultant Lissajous patterns. In this way it was possible to measure the variations of phase shift and gain as a function of emitter current.

The two amplifiers whose characteristics were measured were tuned to 5.9 and 11 mc/s. The phase - emitter current and gain - emitter current characteristics are given in Figure 22. The shape of the phase shift characteristics are similar to the calculated phase shifts which were made at 184.7 kc/s and 6.133 mc/s for Case A.

The curves illustrate the difference in the sense of the phase shifts between forward and reverse AGC. The validity of the analysis is well demonstrated by comparing the measured phase shifts of the 5.9 mc/s amplifier with the calculated phase shifts of the 6.133 mc/s amplifier. In going from an emitter current of 0.1 ma to 4.7 ma and using 2 ma as a reference the phase shift of the 6.133 mc/s amplifier went from $+80^\circ$ to -60° while the 5.9 mc/s amplifier went from $+55^\circ$ to -46° . The differences may be attributed to dissimilarities between actual and average transistor characteristics, losses in the coupling networks, and experimental error.

6.3 VERIFICATION OF PHASE SHIFT CALCULATION (SYSTEM PERFORMANCE)

To establish the validity of the analyses to a more complex system, a complete receiver was constructed. A

block diagram of the receiver is given in Figure 23. The signal frequency is 6.133 mc/s. The receiver amplifies and converts the input signal to an intermediate frequency of 184.7 kc/s. Forward gain control was applied simultaneously to three stages to achieve AGC in the receiver.

In order to measure the characteristics of the receiving system, it was necessary to construct a similar system whose input and local oscillator signals were common to the receiver being tested. Figure 24 illustrates the test setup used. The input to the similar receiver was taken directly from the signal generator output while the test receiver's input was variable through the insertion of a controllable attenuator between it and the signal generator.

By applying the technique used for single amplifier characteristic measurements, discussed in Section 6.2, the receiver's gain and phase shift as a function of control current were measured, and are shown in Figure 25. The results indicate that for a reduction in gain of 80 db the total receiver phase shift was -120° .

The phase shift characteristics were compared with the calculated results of Section 6.1 by appropriate consideration of the origin of the phase shifts in the receiver:

1. 1st RF due to control of 2nd RF.
2. 2nd RF due to control of 2nd RF.
3. 1st IF due to control of 1st and 2nd IF's.
4. 2nd IF due to control of 2nd IF.

Any phase shift contributed by the mixer due to controlling the 1st IF was assumed to be negligible, because of the loose coupling between the states which is necessary to maintain a large loaded Q at the mixer output.

The phase shift - emitter current characteristics were obtained by summing the contributions from each stage. By assuming that the bias state of each controlled stage is equal for any input signal level, and that the change in the emitter current from its quiescent value is proportional to the total control current required to obtain the necessary gain control, a predicted phase shift was found and plotted in Figure 25. The characteristics indicate a close similarity between measured and predicted phase shifts.

The differences between the predicted and measured values may be attributed to several factors. In the calculation it was assumed that the transistor is described by its average characteristics, while in actual practice the transistor parameters may vary as much as 20% from one transistor to the next. The assumptions that the emitter currents are equal in each of the three controlled stages and that the change in emitter current is proportional to control current are also possible sources of error.

6.4 PHASE - GAIN CHARACTERISTICS

The problem of selecting the best type of AGC, forward or reverse, in an application which requires a minimum amount of phase distortion was examined by plotting

the phase shift as a function of amplifier gain. The gain of the 6.133 mc/s amplifier was calculated from the current gain for the case in which the amplifier and the following stage were controlled. The power gain (A_p) in this case is given by

$$\begin{aligned} A_p &= 10 \log \left[\frac{I_2}{I_1} \right]^2 \text{ db} \\ &= 20 \log \frac{Y_{21}}{Y_L + Y_{11}} \text{ db,} \end{aligned} \tag{24}$$

since the conductance part of the admittances fed by the input current (I_1) and output current (I_2) are equal. Plots of gain versus phase shift are given in Figure 26 for both measured and calculated characteristics. The measured characteristics are for the 5.9 mc/s amplifier. Both curves illustrate that the phase shift from the point of maximum gain to a point of equal gain reduction is nearly equal for forward and reverse control. Thus, no general conclusion can be made concerning the choice of AGC, based on a minimum phase shift criterion.

The curves also illustrate that there is a range of emitter current over which very little change in gain occurs. Therefore, regardless of the type of AGC used, the quiescent point should be chosen to take advantage of the gain response to changes in emitter current. This can be done by biasing the transistor near the edge of the constant gain portion of the characteristics.

6.5 CHOICE OF TRANSISTOR

It is desirable to establish a method of selecting transistor types based on their relative merits, when phase distortion is of importance. For this purpose a figure of merit is desirable which depends only on the transistor characteristics, and is applicable to general gain control applications.

The phase shift expression for cascaded controlled stages may be used to obtain a figure of merit, since it is only a function of the transistor and is generally applicable. The criterion for minimum phase shift is the smallest value of the term

$$\frac{(B_2 - B_2') + \frac{1}{n^2} (B_1 - B_1')}{G_2 + \frac{1}{n^2} G_1} \quad (25)$$

in Equation 20. Equation 25 may be rewritten by letting $n^2 = G_1' / G_2'$ and $B = \omega C$

$$\omega \frac{(C_2 - C_2') + \frac{G_1'}{G_1} (C_1 - C_1')}{G_2 + \frac{G_2'}{G_1} G_1} \quad (26)$$

Most manufacturer's data sheets contain input and output immittances as a function of emitter current at constant collector voltage. Since the phase shift due to reverse AGC requires only a small decrease in emitter current from its value at the quiescent state, a phase figure of merit

at a particular operating frequency may be defined as

$$F = \left| \frac{G_2 + \frac{G_2'}{G_1} G_1}{(C_2 - C_2') + \frac{G_2'}{G_1} (C_1 - C_1')} \right| \cdot \quad (27)$$

The unprimed values correspond to the parameters when the emitter current equals some fraction of the emitter current in the quiescent state; the primed values correspond to the parameters in the quiescent state. The larger F , the better suited is the transistor for application where minimum phase distortion is desirable.

Several figures of merit were calculated for different transistors at 15 mc/s and based on a fractional decrease in emitter current of $\frac{1}{2} I_e$ /quiescent state. The results of these are:

<u>Transistor</u>	<u>F</u>
2N1270	1.16 millimhos/pf.
2N1271	1.33
2N1272	1.74

From these factors it is seen that the 2N1272 transistor is preferred over the 2N1270 or 2N1271.

6.6 COMPENSATION OF PHASE SHIFTS

The phase shift occurring in transistor amplifiers due to changes in bias may be compensated in several ways.

Phase compensation in a system having more than one

gain controlled stage may be achieved by using forward AGC in one stage and reverse AGC in another. As the sense of the phase changes is different, a control network may be designed to produce equal and opposite phase changes in successive stages. This type of AGC system would require two control signal systems.

A second solution lies in the application of variable impedance elements to the input or output of a controlled stage. Elements whose impedance varies with control signal would be employed in such a way that the phase function is maintained constant.

CHAPTER 7

CONCLUSIONS

The purpose of this investigation was to determine and analyze the phase shifts in HF transistor amplifiers, when the transistors undergo changes in DC bias in order to effect gain control. The analysis was based on the expression for the current gain in terms of the equivalent Y parameters. Three different cases were considered - a) the phase shift due to bias changes in the amplifier itself; b) the phase shift due to bias changes in the amplifier and the following stage; and c) the phase shift due to bias changes in the following stage.

Calculation of the phase shift in a 184.7 kc/s and a 6.133 mc/s amplifier were made for a single tuned HF common emitter configuration. Experimental verification of the calculated results was made by measuring the phase characteristic of two separate amplifiers. The sense and shape of the curves agreed with the theoretically expected characteristics. A receiver having a carrier frequency of 6.133 mc/s and an intermediate frequency of 184.7 kc/s was built, and its phase characteristics measured and compared with a predicted value derived from the calculated phase shifts. The results showed good agreement between the theoretical analysis and the observed behavior.

The relative merits of forward and reverse automatic gain control were examined. The magnitudes of the phase shifts were nearly equal for equal changes in gain; however, the

senses of the phase shift were different and this suggested a possible method of compensation.

The results of the analysis and measurements indicated that the phase shifts are due primarily to changes in the input and output immittanced.

A phase figure of merit

$$F = \left| \frac{G_2 + \frac{G_2'}{G_1} G_1}{(C_2 - C_2') + \frac{G_2'}{G_1} (C_1 - C_1')} \right|,$$

was proposed. In this formula G_1 and G_2 are the input and output conductances of the amplifier in millimhos at some fraction of the quiescent current, and C_1 and C_2 are the input and output capacitances in picafarads at the same current. The primed values correspond to the parameter values in the quiescent state. Transistors with larger figures of merit would be judged more suitable in applications where it is desirable to keep the change in phase shift with change in gain small.

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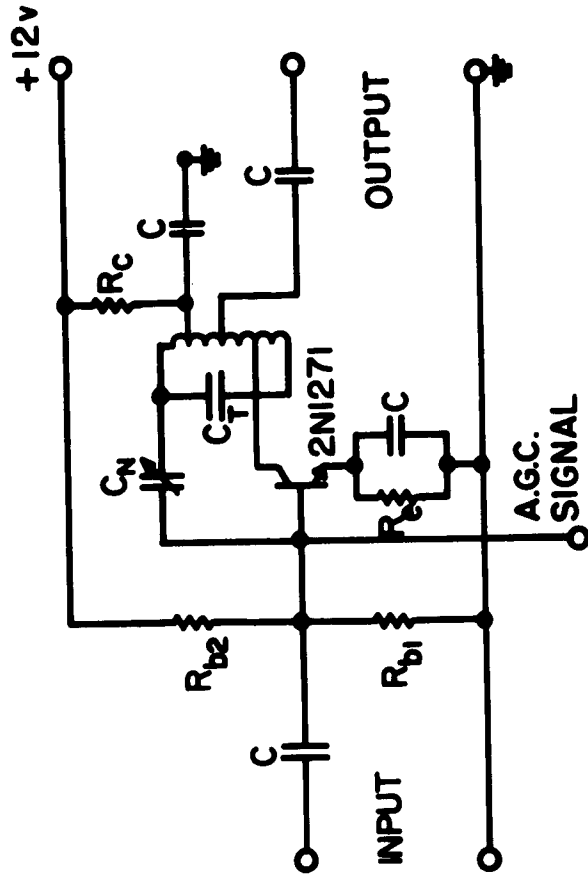
NOMINAL VALUES

R_{b1} — 4.7 K

R_{b2} — 10 K

R_e — 470

R_c — 2 K



R_{b1}, R_{b2}, R_e — BIAS RESISTORS

C — BY PASS OR DECOUPLING CAPACITANCES

C_n — NEUTRALIZING CAPACITANCE; EFFECTS NEARLY COMPLETE UNILATERALIZATION

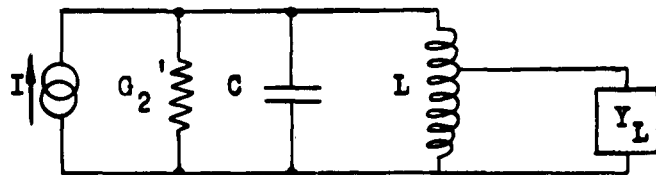
R_c — DECOUPLING RESISTANCE; ALSO USED AS FORWARD A.G.C. MECHANISM, i.e., REDUCTION IN V_c OCCURS WHEN I_e IS INCREASED

C_T — TUNING CAPACITOR

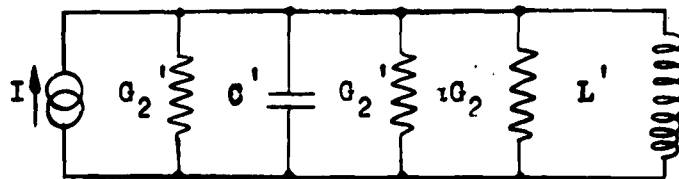
TYPICAL HF TRANSISTOR AMPLIFIER

FIGURE 1

Figure 2



Output Circuit of HF Single Tuned Transistor Amplifier



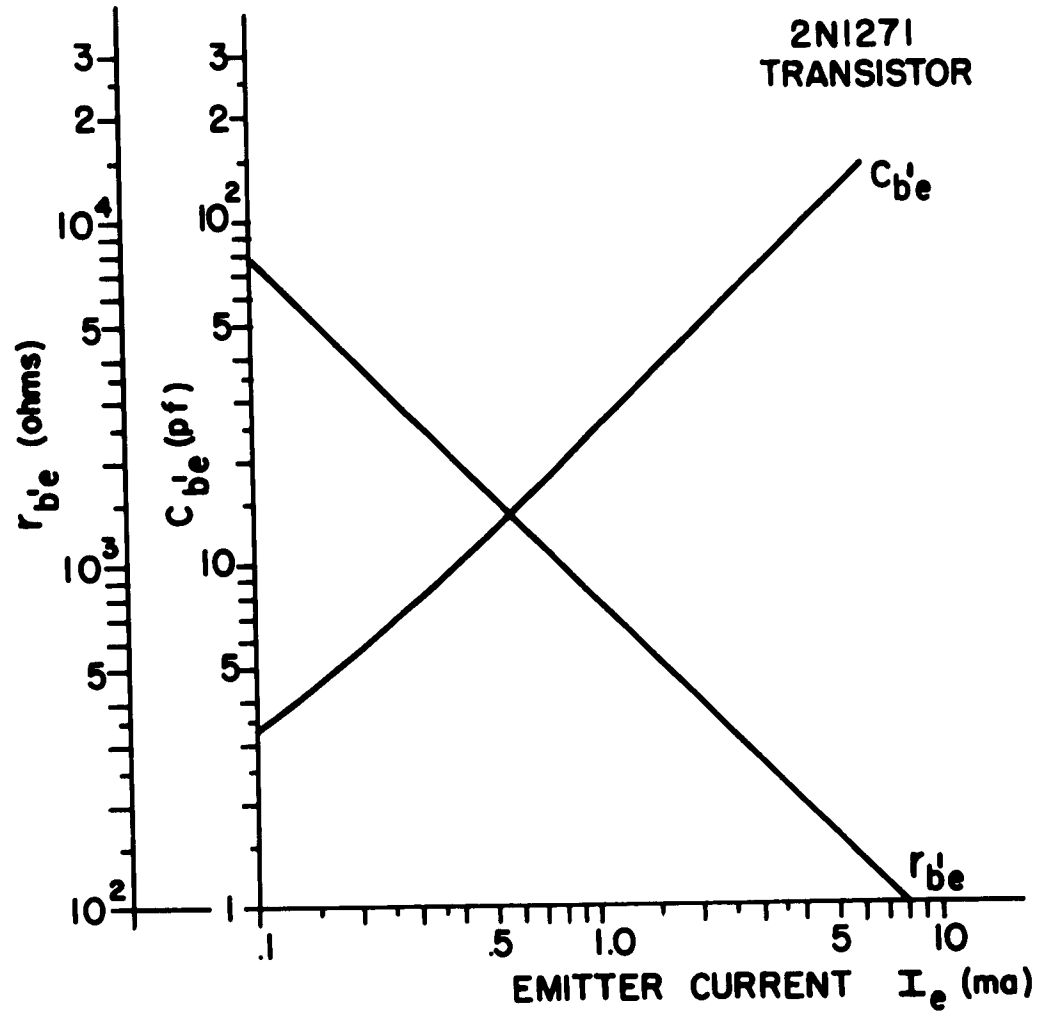
Equivalent Output Circuit of HF Single Tuned Transistor Amplifier Under Matched Conditions

- I = Output Current Generator
- G_2' = Output Conductance of Transistor Amplifier
- L = Inductance of Transformer
- C = Capacitance Required to Tune L and Reflected Susceptance of Y_L
- Y_L = Load Admittance; Input Admittance of Following Stage
- L' = Inductance of Transformer Referred to Transistor Output Terminals
- C' = Capacitance Required to Tune L' to f , the Operating Frequency
- $\alpha G_2'$ = Loss Conductance of Transformer
- Q_u = Unloaded Q of Transformer Winding
- Q_L' = Loaded Q Referred to Transistor Output Terminals When Q_u is Infinite
- Q_L = Loaded Q Referred to Transistor Output Terminals

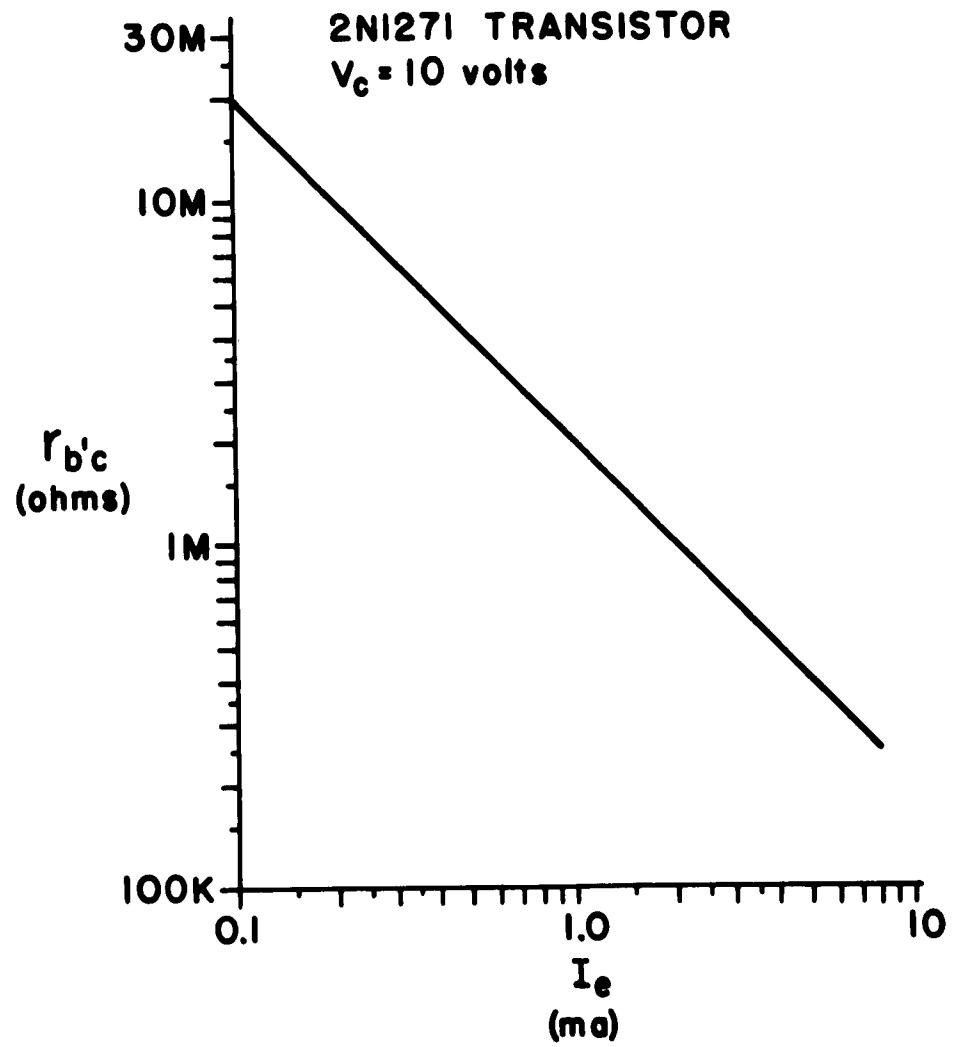
Appropriate Relationships:

$$L' = L \left(1 + \frac{1}{Q_u^2} \right) \approx L \text{ for Reasonable Values of } Q_u.$$

$$Q_L' = \frac{1}{\omega L' 2G_2'} ; Q_L = \frac{Q_u Q_L'}{Q_u + Q_L'} ; \alpha = 2 \frac{Q_L'}{Q_u} ; \alpha G_2' = \frac{1}{\omega L' Q_u}$$

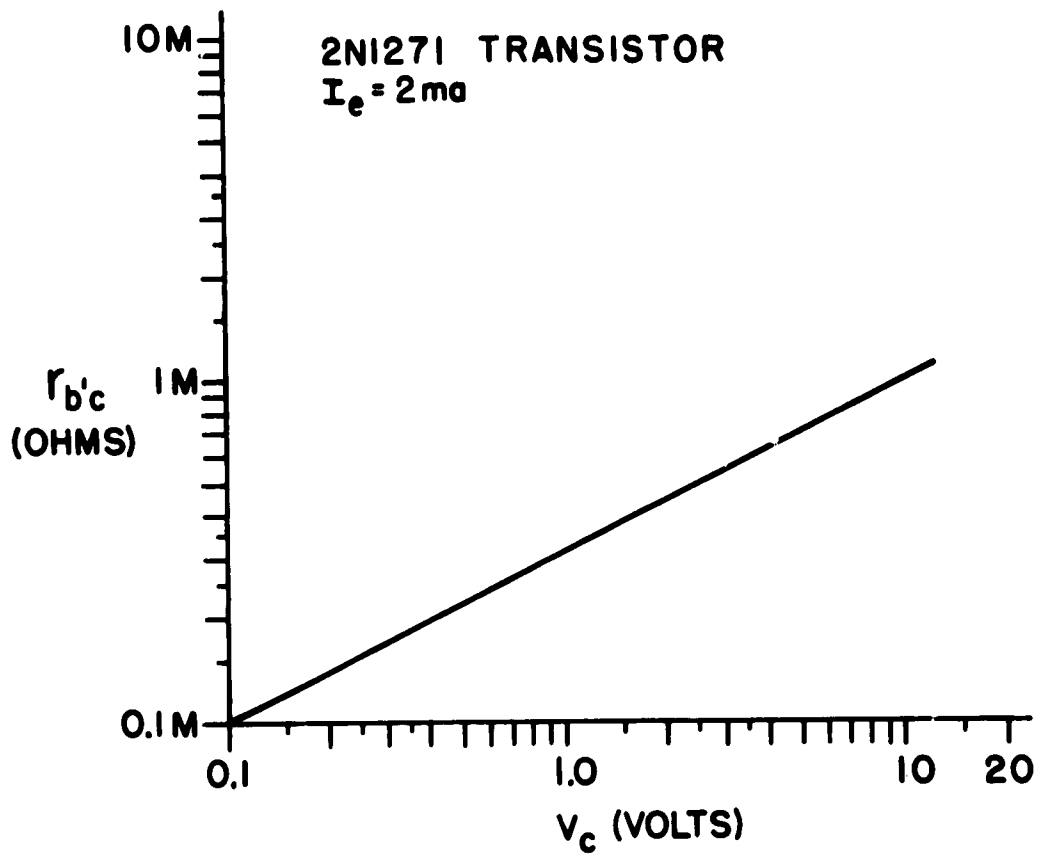


r'_{be} AND C'_{be} vs EMITTER CURRENT
FIGURE 3

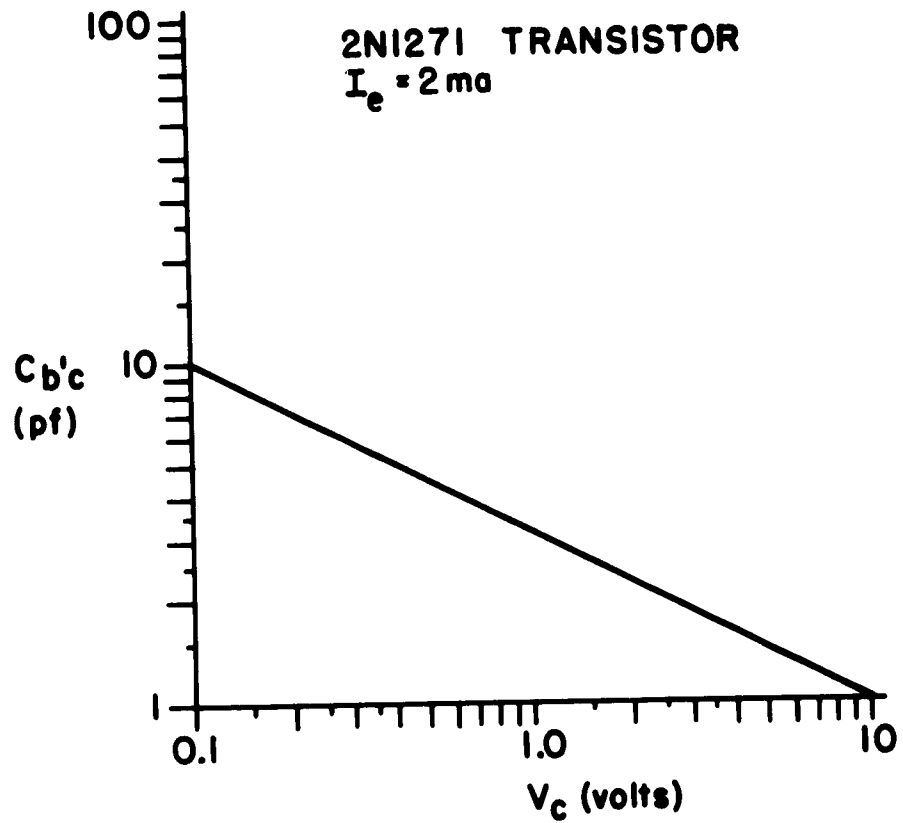


r'_{bc} vs EMITTER CURRENT

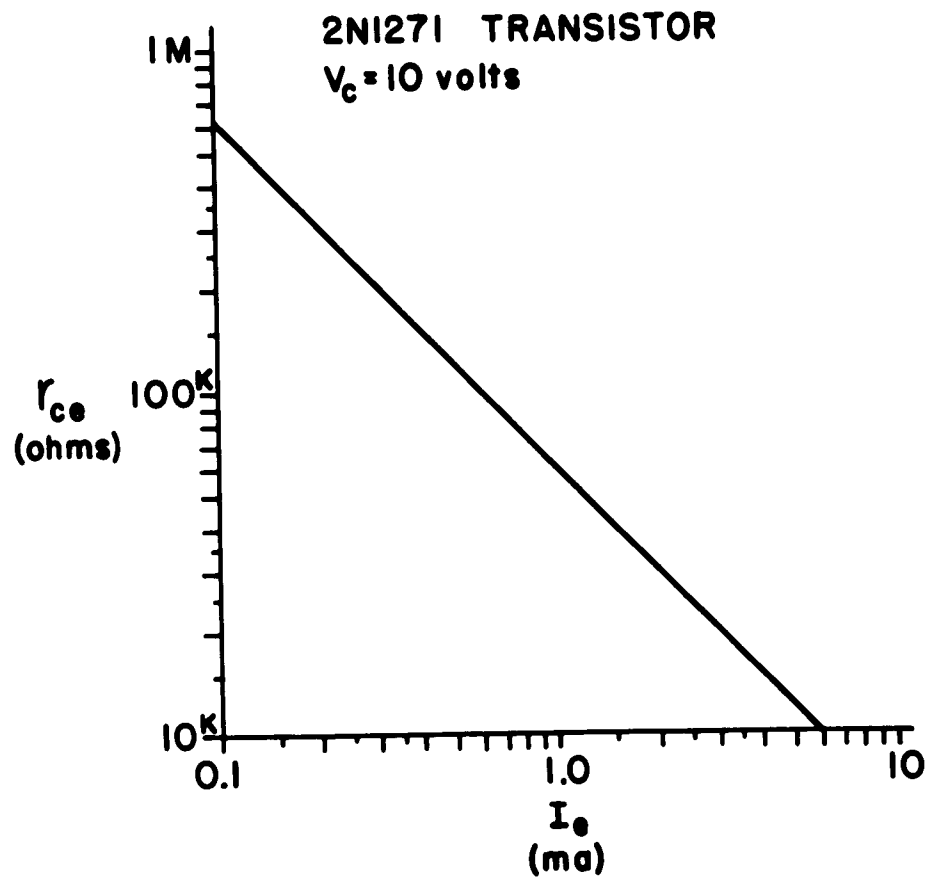
FIGURE 4



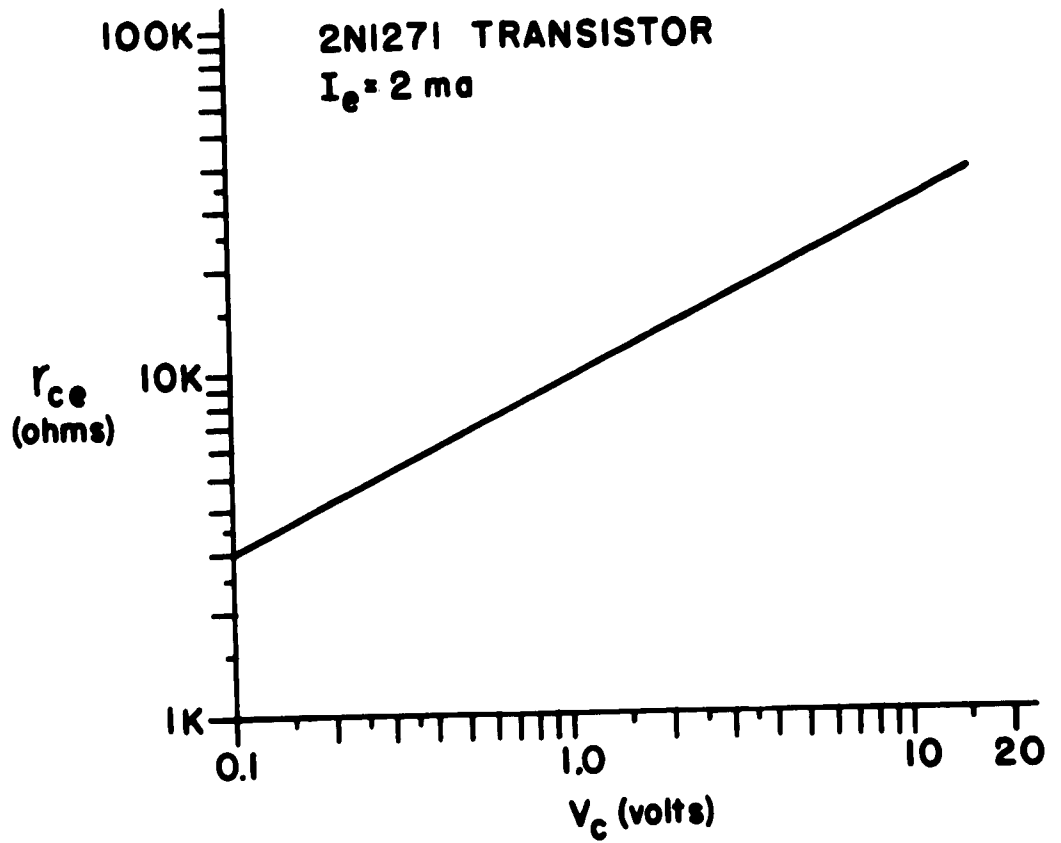
$r_{b'c}$ vs COLLECTOR VOLTAGE
FIGURE 5



$C_{b'c}$ vs COLLECTOR VOLTAGE
FIGURE 6



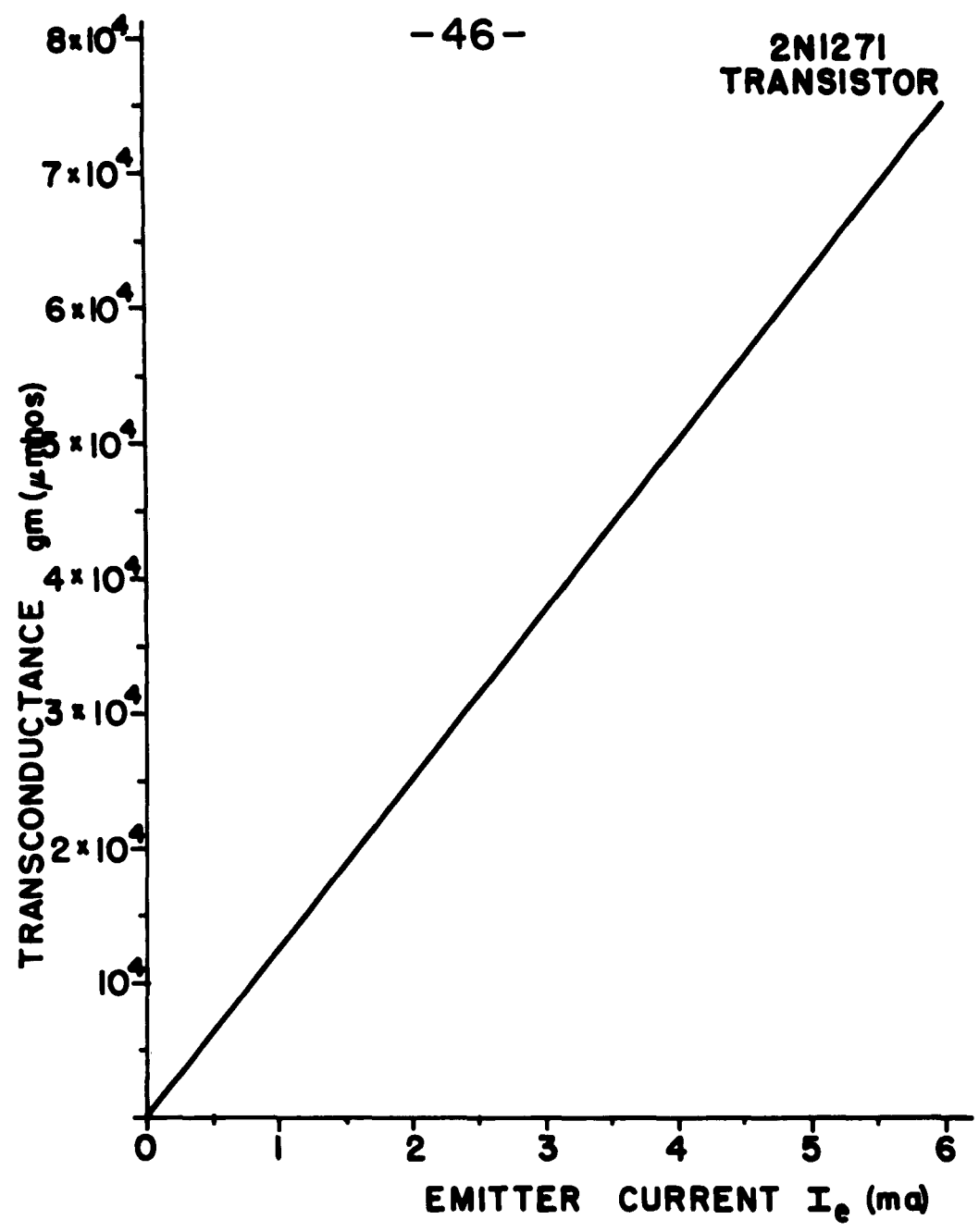
r_{ce} vs EMITTER CURRENT
FIGURE 7



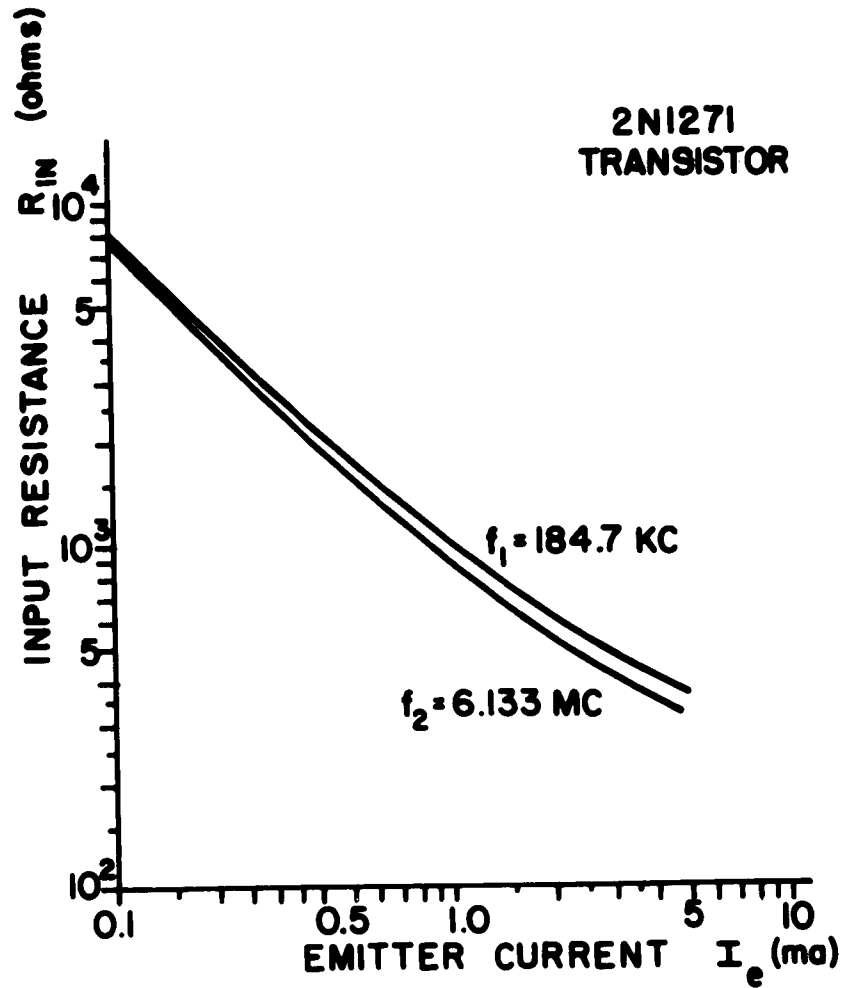
r_{ce} vs COLLECTOR VOLTAGE

FIGURE 8

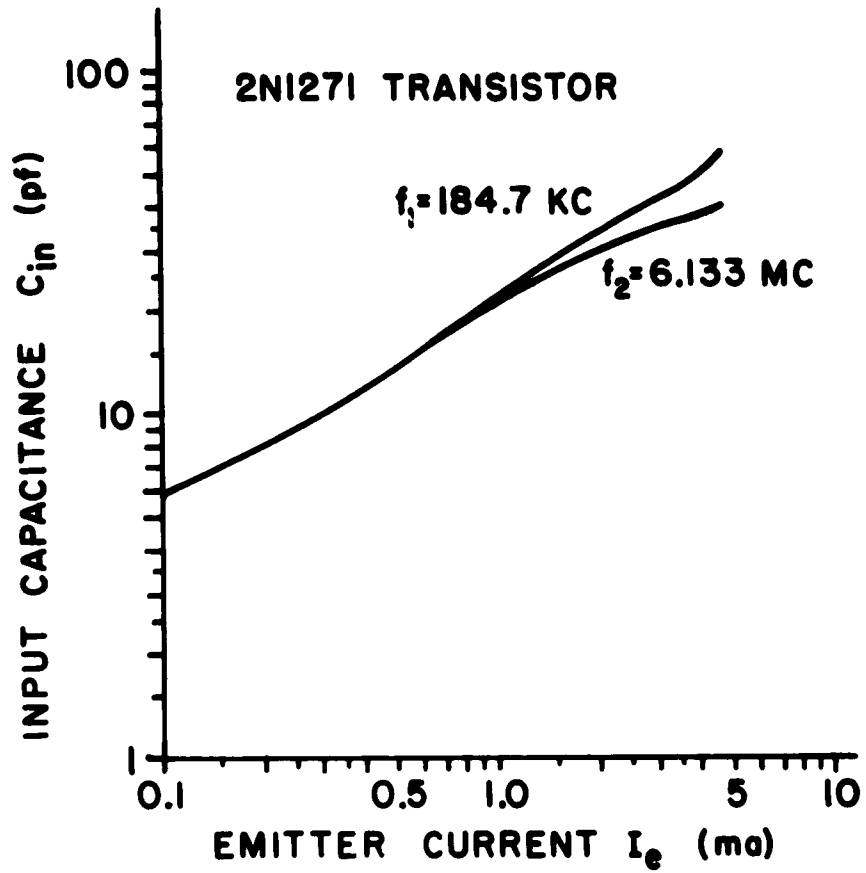
2N1271
TRANSISTOR



TRANSCONDUCTANCE vs EMITTER CURRENT
FIGURE 9

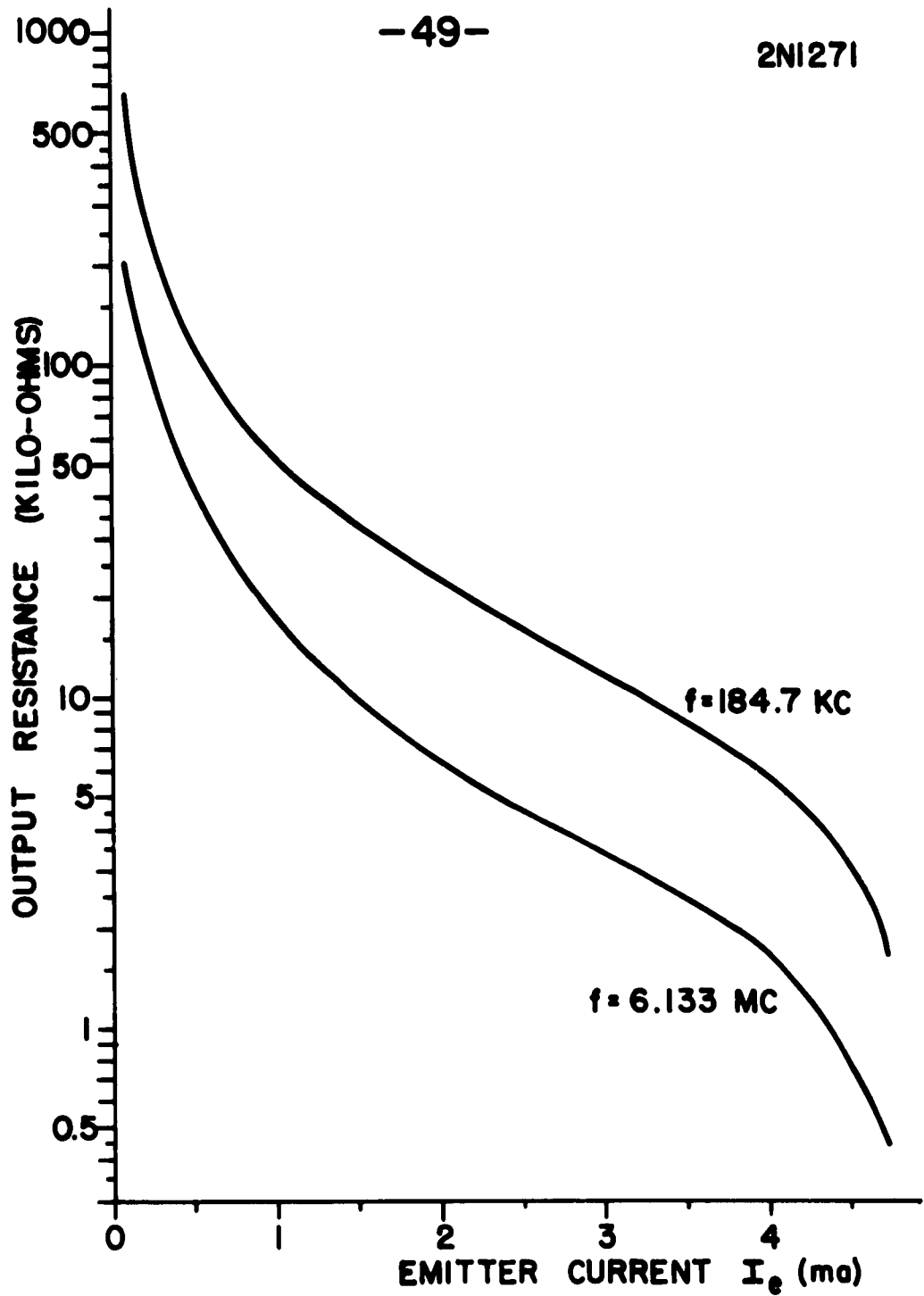


INPUT RESISTANCE
vs
EMITTER CURRENT
FIGURE 10

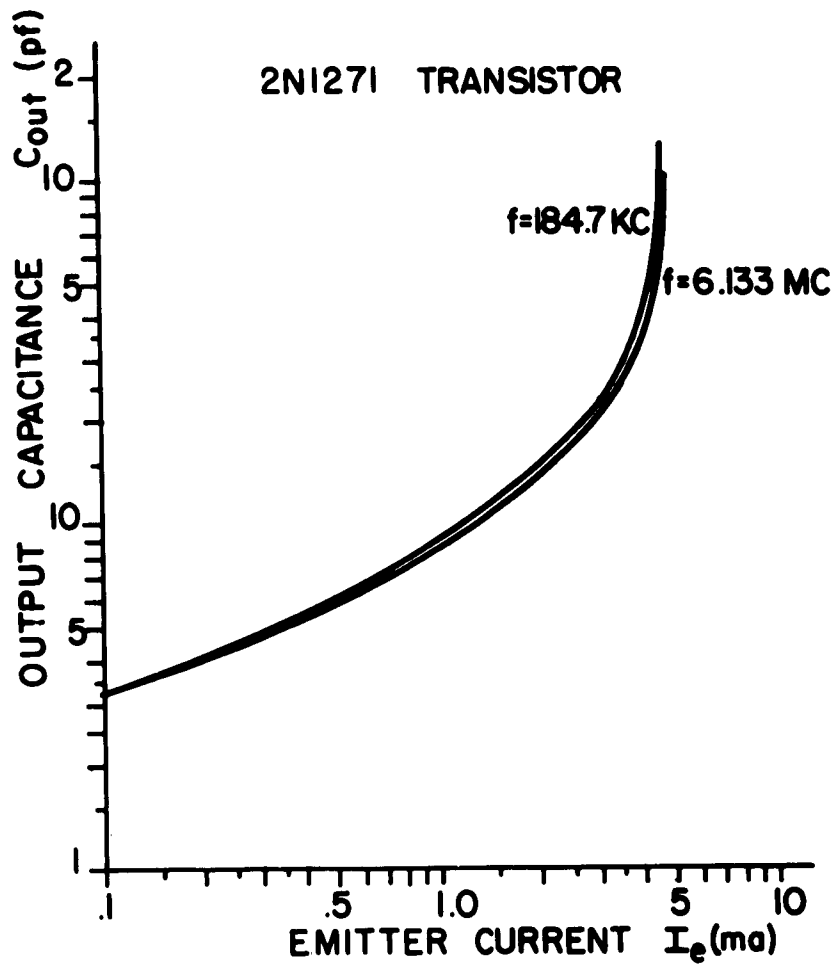


INPUT CAPACITANCE
VS
EMITTER CURRENT

FIGURE II

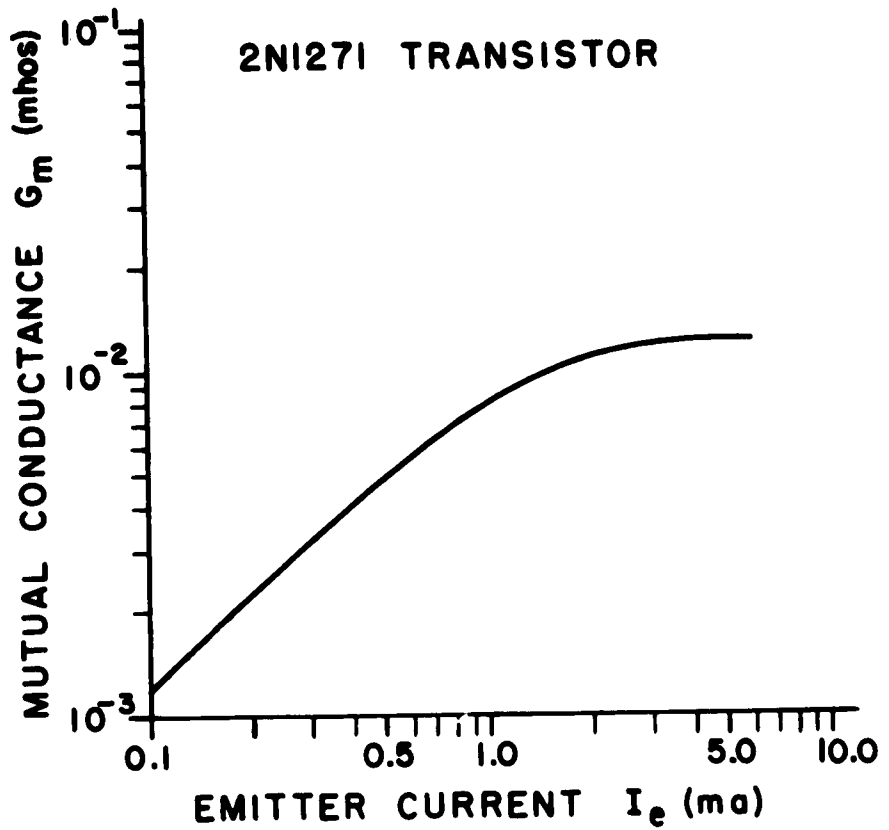


OUTPUT RESISTANCE vs EMITTER CURRENT
FIGURE 12



OUTPUT CAPACITANCE
VS
EMITTER CURRENT

FIGURE 13



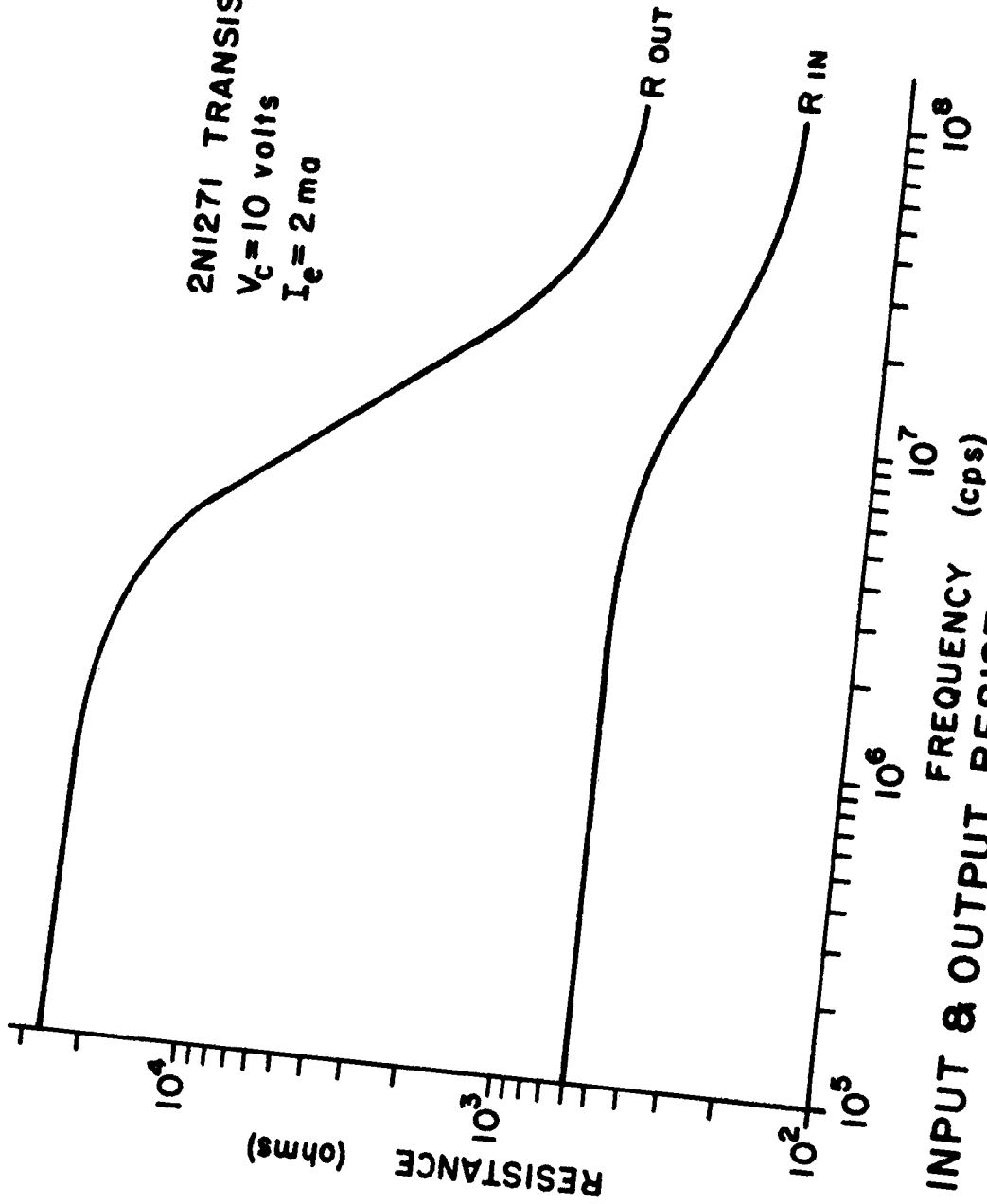
MUTUAL CONDUCTANCE

vs

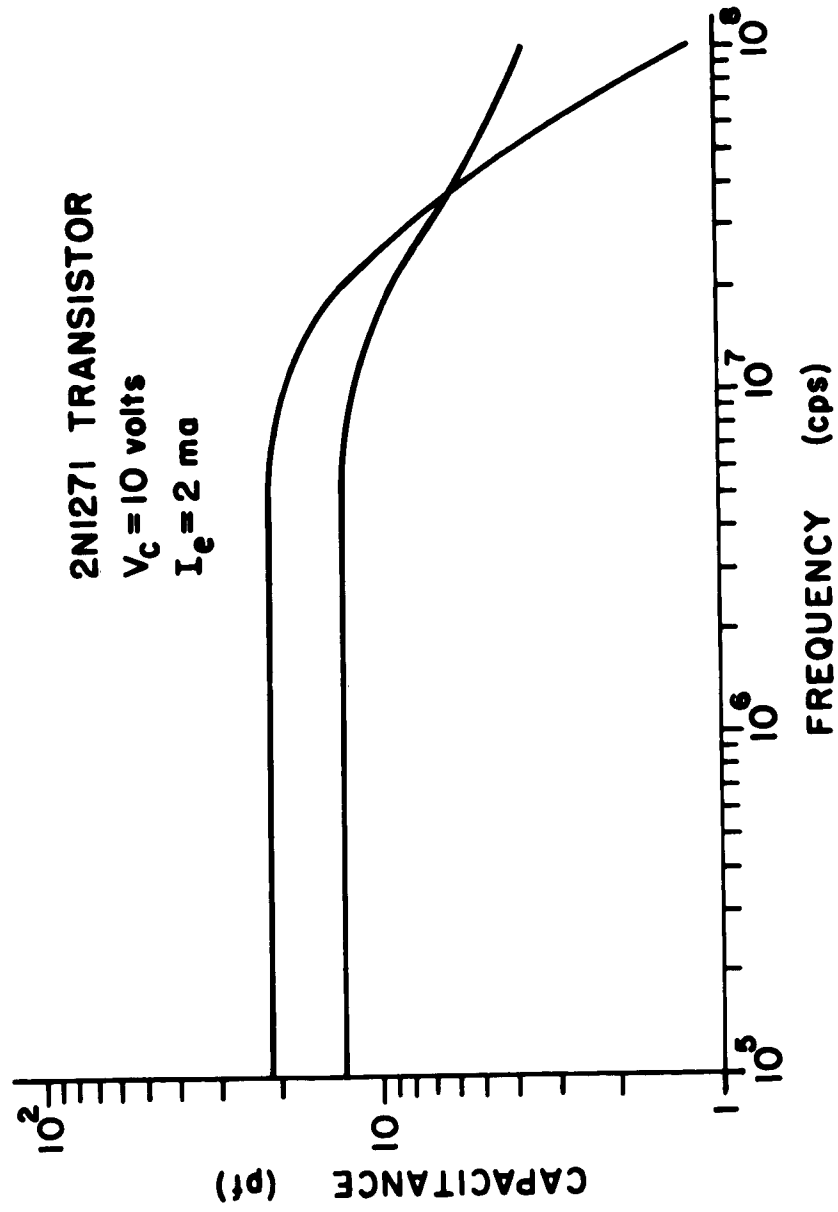
EMITTER CURRENT

FIGURE 14

2N1271 TRANSISTOR
 $V_c = 10$ volts
 $I_e = 2$ ma

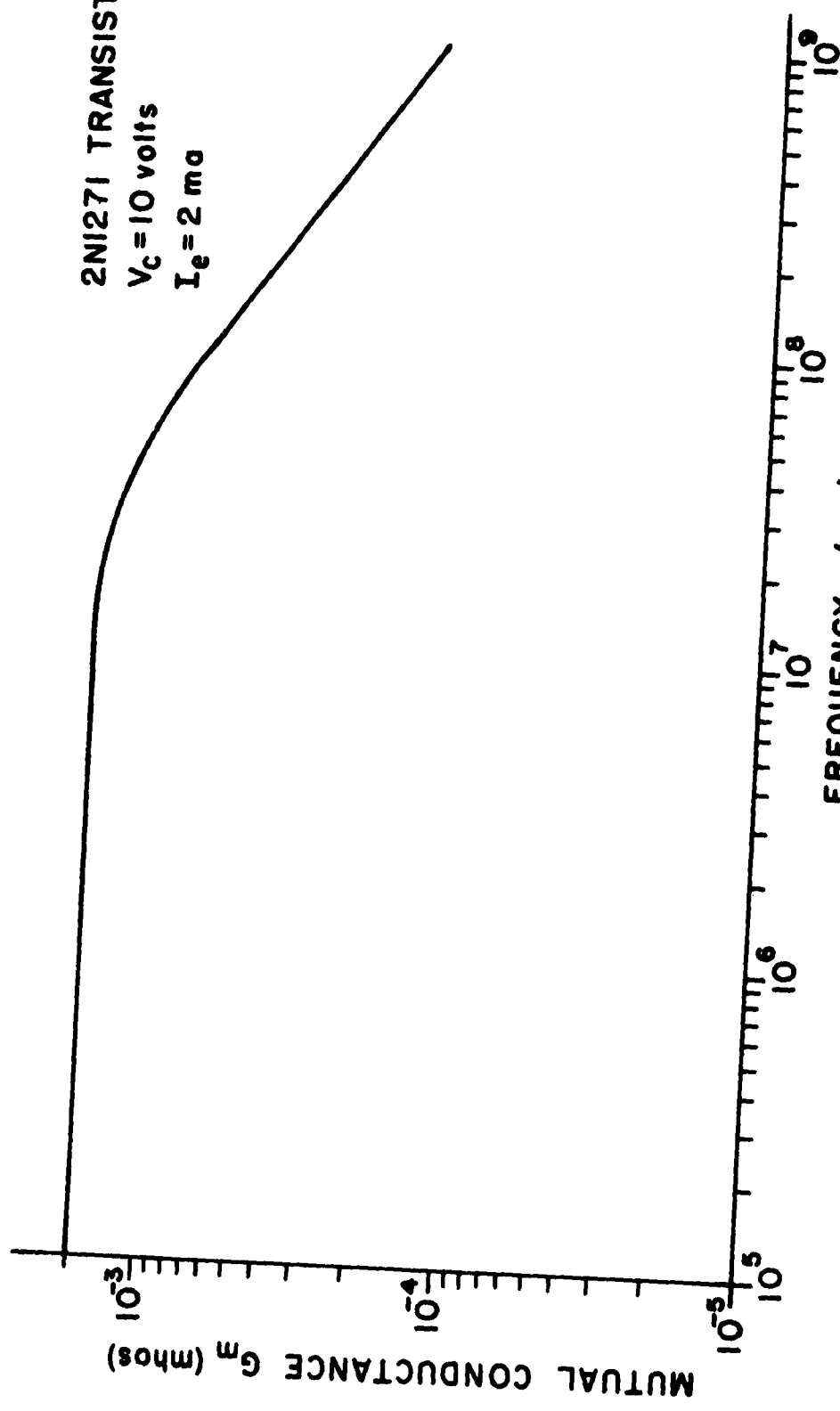


INPUT & OUTPUT RESISTANCE vs FREQUENCY
FIGURE 15

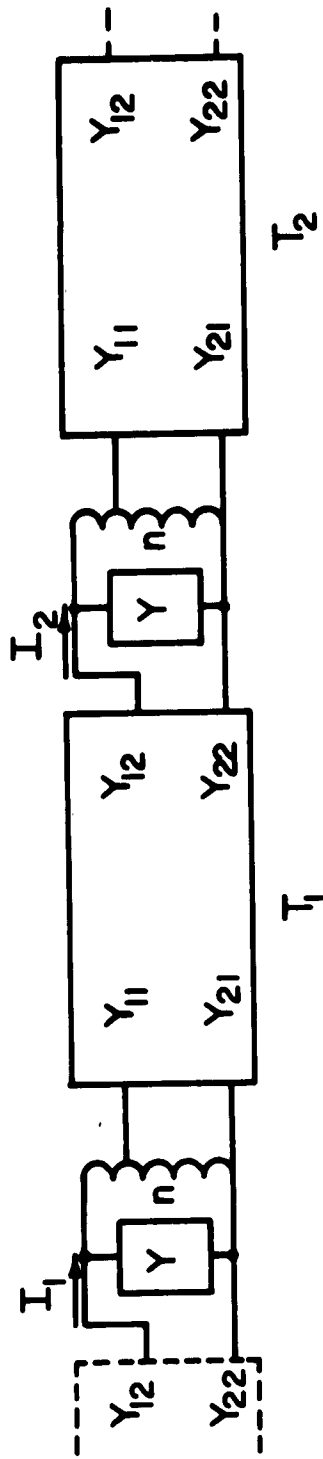


INPUT & OUTPUT CAPACITANCE vs FREQUENCY

FIGURE 16



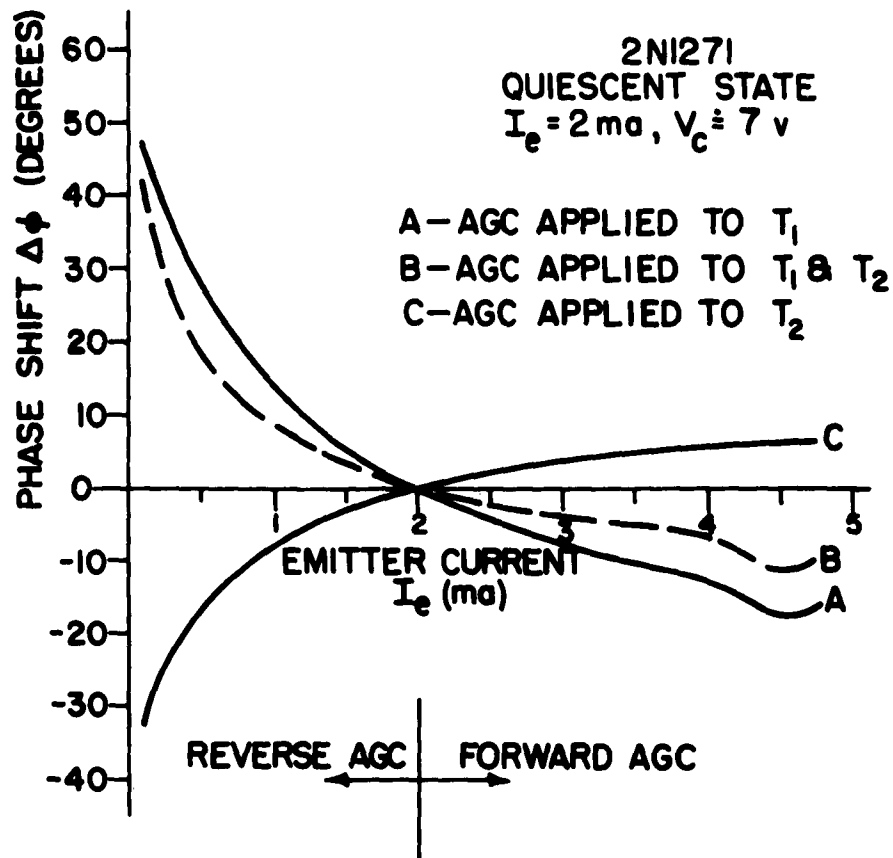
MUTUAL CONDUCTANCE vs FREQUENCY
 FIGURE 17



SCHMATIC DIAGRAM OF A TRANSISTOR AMPLIFIER (T_1)
CONNECTED IN CASCADE WITH SIMILAR AMPLIFIERS

FIGURE 18

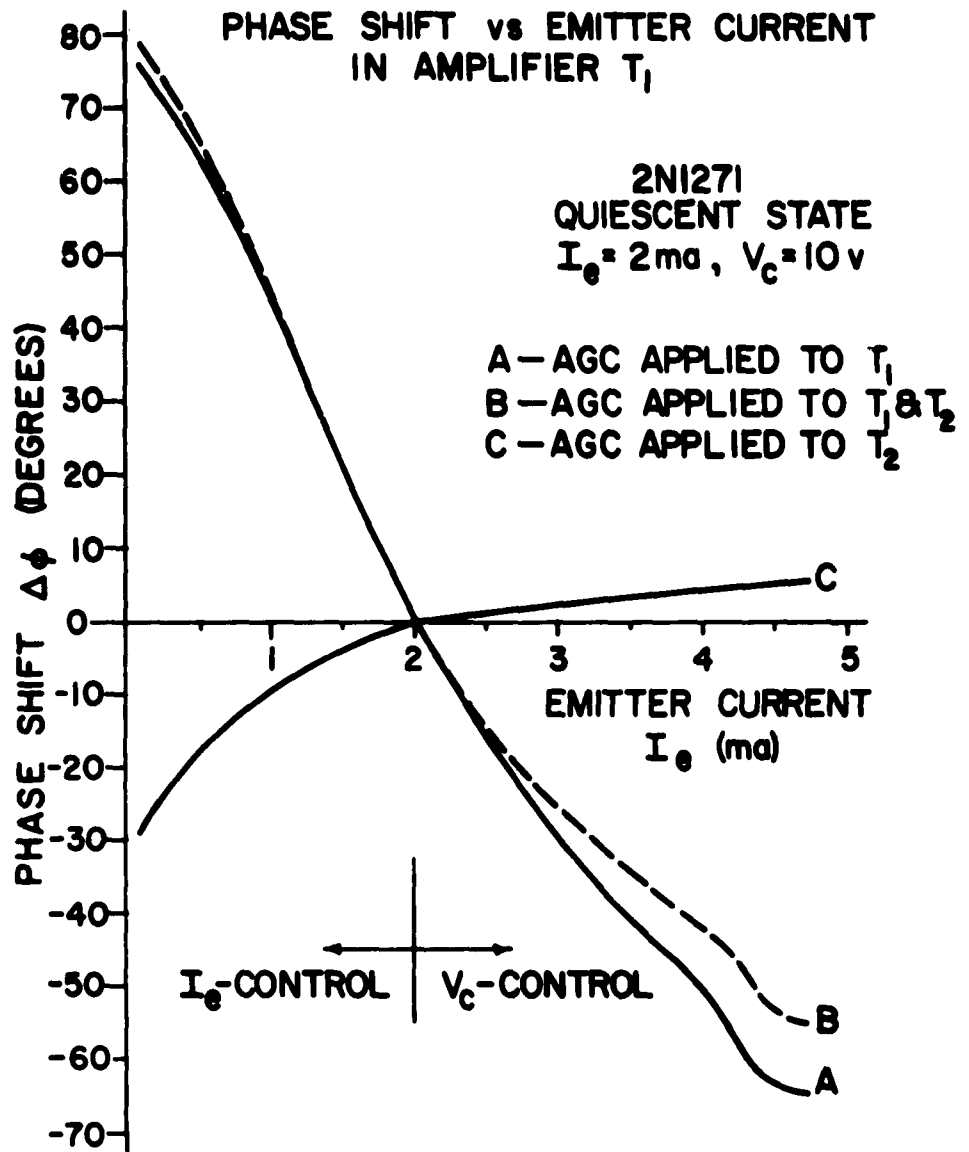
PHASE SHIFT vs EMITTER CURRENT
IN AMPLIFIER STAGE T_1



CALCULATED PHASE SHIFT CHARACTERISTICS
OF A CASCADED AMPLIFIER

($f = 184.7 \text{ kc/s}$)

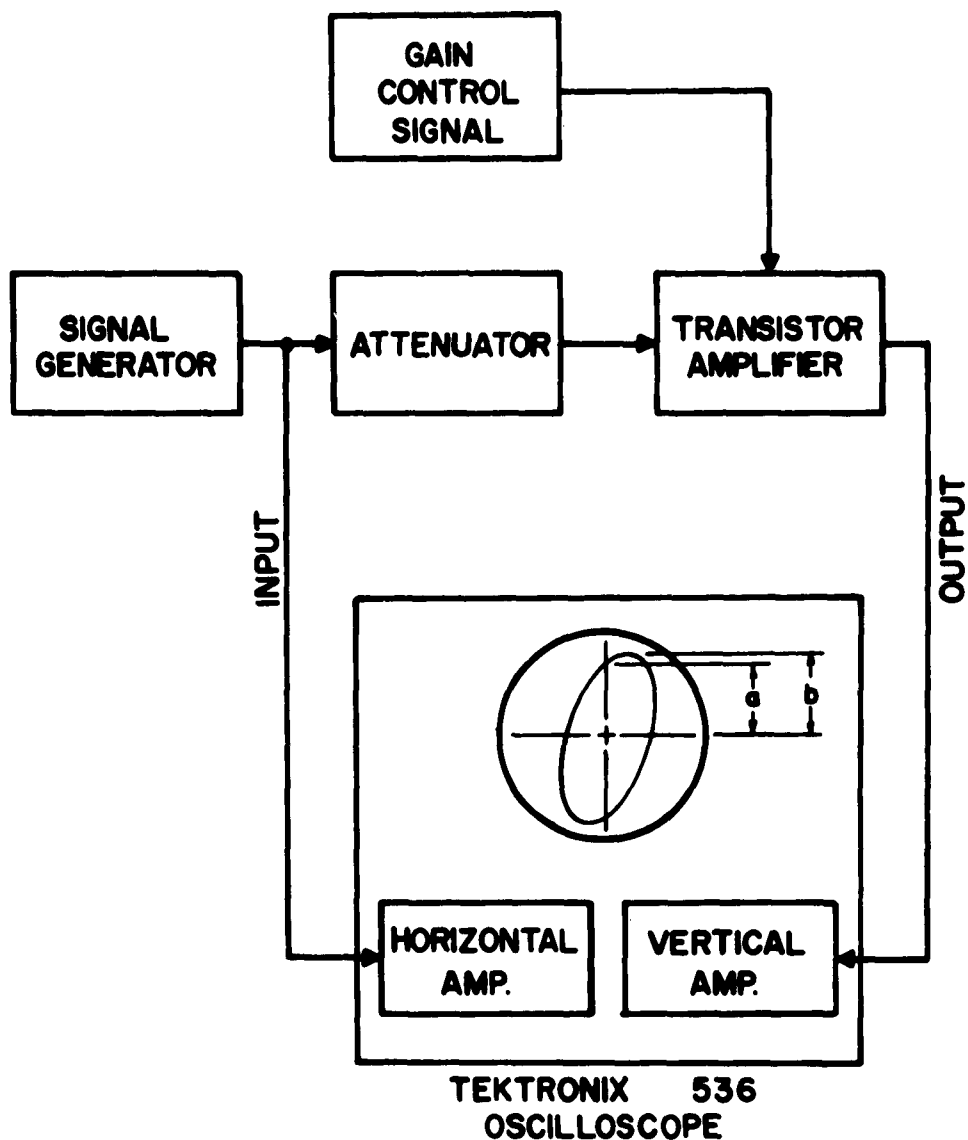
FIGURE 19



CALCULATED PHASE SHIFT CHARACTERISTICS OF
A CASCADED AMPLIFIER

($f = 6.133\text{ mc/s}$)

FIGURE 20



NOTES:

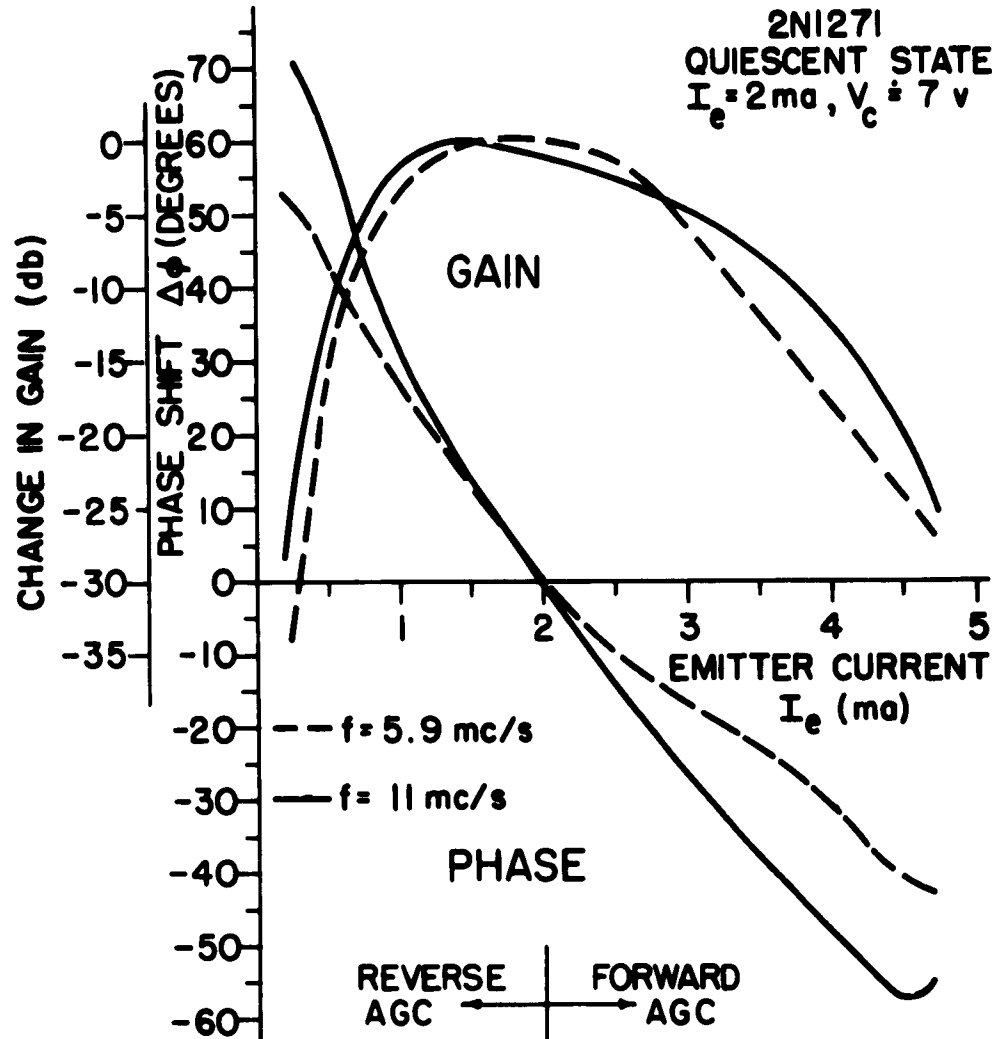
b—OUTPUT SIGNAL STRENGTH

$\phi = \sin^{-1} \frac{a}{b}$ PHASE OF OUTPUT SIGNAL WITH RESPECT TO INPUT

TEST SETUP FOR MEASURING GAIN AND PHASE CHARACTERISTICS

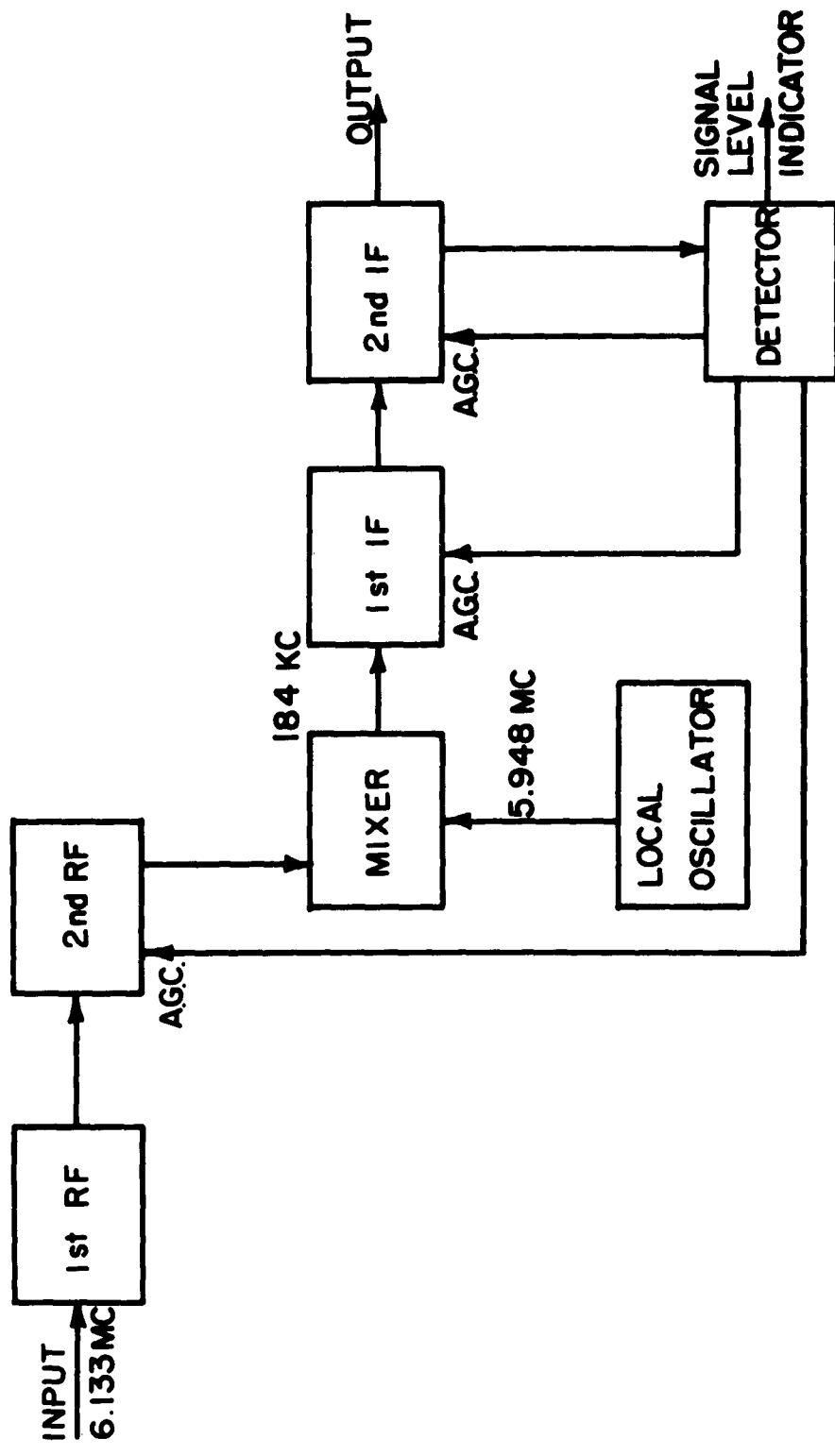
FIGURE 21

CHANGE IN GAIN AND PHASE SHIFT vs
EMITTER CURRENT

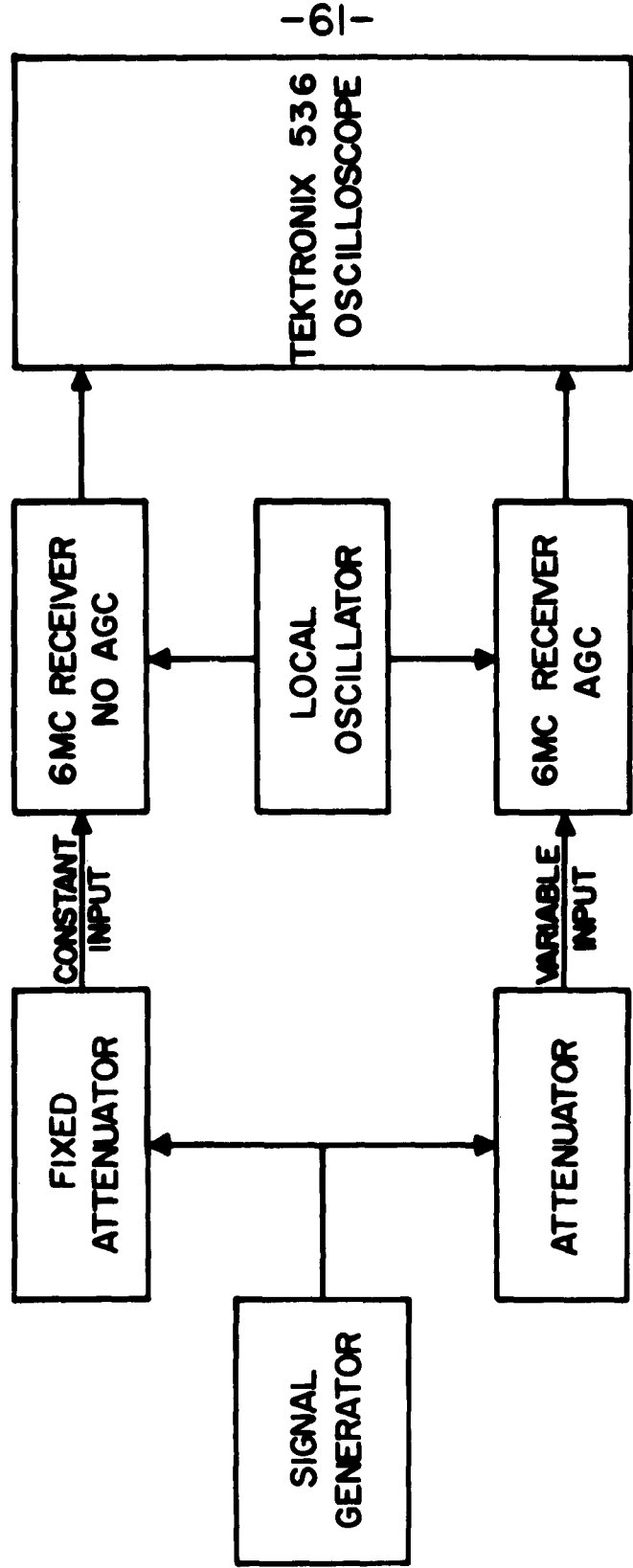


MEASURED GAIN AND PHASE
CHARACTERISTICS OF TWO TYPICAL
HF TUNED AMPLIFIERS

FIGURE 22

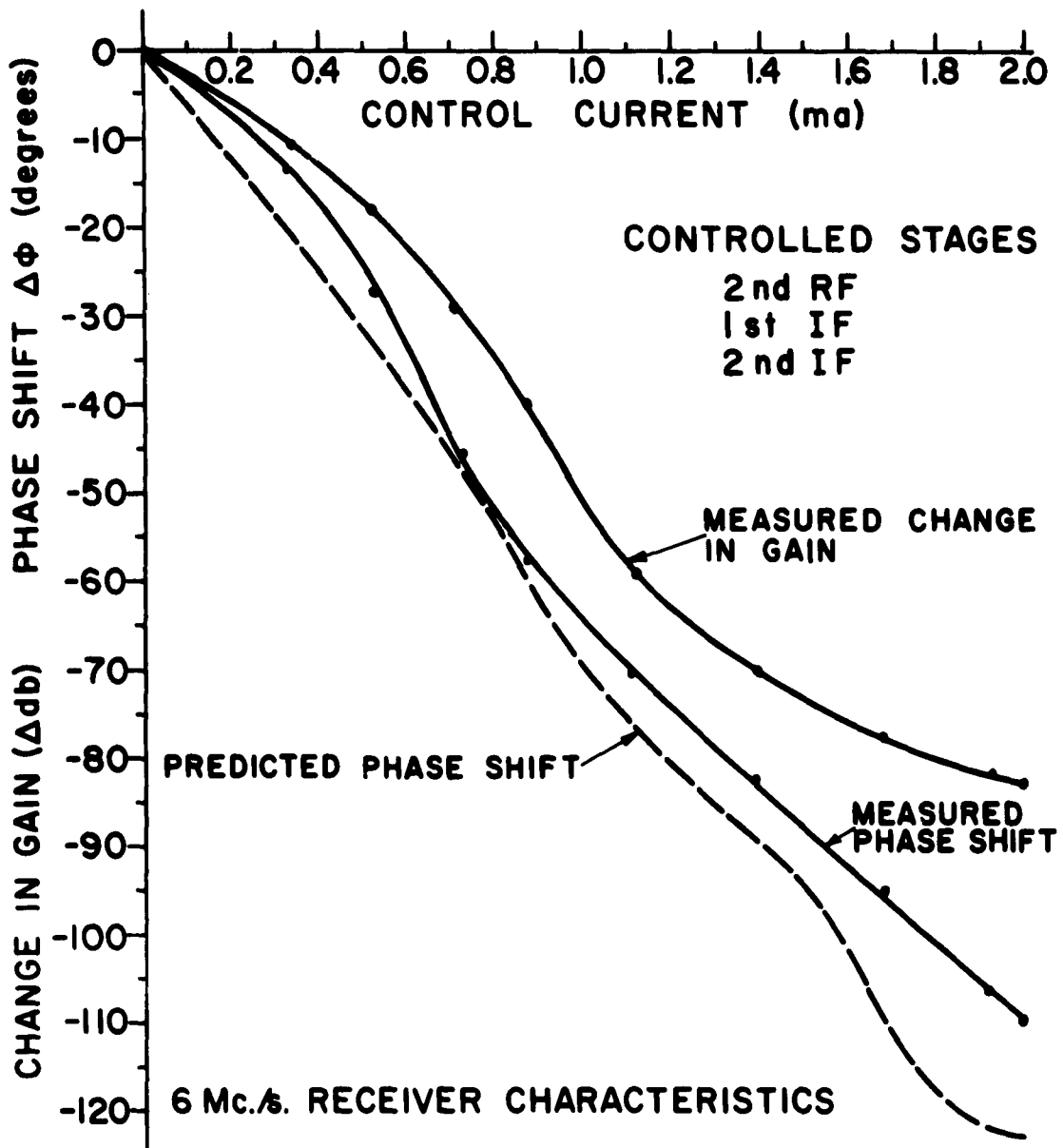


BLOCK DIAGRAM OF 6 MC RECEIVER
FIGURE 23

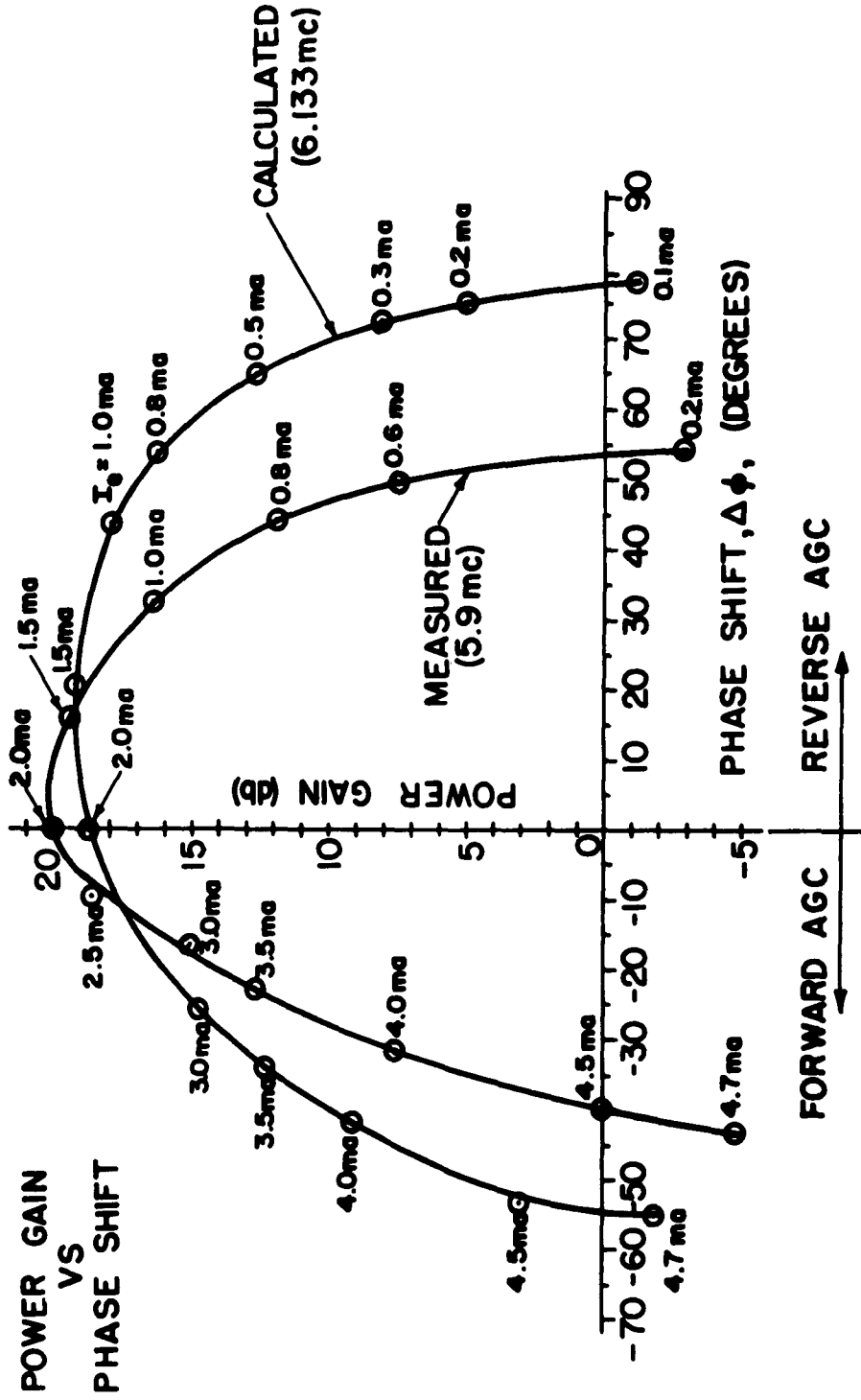


6MC RECEIVER TEST SETUP FOR MEASURING GAIN AND PHASE CHARACTERISTICS

FIGURE 24



CHANGE IN GAIN and PHASE SHIFT
vs
AGC CONTROL CURRENT
FIGURE 25



PHASE CHARACTERISTICS AS A FUNCTION OF GAIN

FIGURE 26

APPENDIX A

HYBRID-PI, NORMAL-PI, AND Y EQUIVALENT CIRCUITS

A.1 HYBRID-PI EQUIVALENT CIRCUIT

The hybrid-pi transistor equivalent circuit is illustrated in Fig. A1. b, e, and c designate the base, emitter, and collector respectively. b' is the intrinsic base terminal and is connected to b through $r_{b'}$. The names of the parameters, their physical significance, and their dependence on the bias state of the transistor are summarized:

$r_{b'}$ - base-spreading resistance; the physical resistance between the base lead and the active base region. Usually assumed independent of bias.

$r_{b'e}$ - emitter shunt resistance; the effective AC resistance of the forward-biased emitter-base diode. It is inversely proportional to emitter current.

$$r_{b'e} \propto 1/I_e$$

$C_{b'e}$ - emitter shunt capacitance; sum of a transition capacitance (C_{tr}) and a diffusion capacitance (C_D) at the emitter-base diode. C_{tr} is assumed constant while C_D is proportional to emitter current.

$$C_{b'e} = C_{tr} + K_1 I_e$$

$r_{b'c}$ - collector to base resistance; consists of a diffusion resistance and a leakage resistance between the collector-base reverse-biased diode. The leakage resistance is assumed to be negli-

gable for normal operating temperatures. The diffusion resistance is given by

$$r_{b'e} \propto \frac{(V_C)^{\frac{1}{2}}}{I_e}$$

where V_C is the collector voltage.

$C_{b'c}$ - collector to base capacitance; almost entirely made up of a transition capacitance caused by the potential barrier at the reverse-biased collector-base junction;

$$C_{b'c} \propto \frac{1}{(V_T + V_C)^{\frac{1}{2}}}$$

where V_T is the originally thermally-generated electrostatic transition potential ($V_T \approx 0.25$ volts for Ge and 0.75 volts for Si).

r_{ce} - collector to emitter resistance; primarily a diffusion resistance between the collector and emitter junctions.

$$r_{ce} \propto \frac{(V_C)^{\frac{1}{2}}}{I_e}$$

g_m - forward transfer conductance or transconductance; the ratio of the short-circuited output current to $V_{b'e}$, the voltage across the intrinsic base region.

$$g_m \propto I_e$$

Expressions for input and output admittances in terms of the hybrid-pi parameters are cumbersome and difficult to handle. Therefore, the equivalent Y and normal-pi circuits

of Figures A2 and A3 are preferred for analysis purposes.

A.2 Y EQUIVALENT CIRCUIT

The Y parameters of the transistor are defined by the equations

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \quad (A1)$$

and

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \quad (A2)$$

The relationships for the input and output admittances and voltage and current gains follow:

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L} \quad (A3)$$

$$Y_{out} = Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_S} \quad (A4)$$

$$A_i = \frac{I_2}{I_1} = \frac{Y_{21}Y_L}{Y_{11}(Y_{22} + Y_L) - Y_{12}Y_{21}} \quad (A5)$$

$$A_v = \frac{V_2}{V_1} = \frac{-Y_{21}}{Y_{22} + Y_L} \quad (A6)$$

A.3 THE NORMAL-PI EQUIVALENT CIRCUIT

The normal-pi equivalent circuit (Figure A3) is used as a conversion artifice in deriving the Y parameters in terms of the hybrid-pi equivalent. It is related to the hybrid-pi circuit through the formulae:

$$Y_1 = \frac{Y_{b'e} Y_{b'c}}{Y_{b'c} + Y_{b'e} + Y_{b'c}} \quad (A7)$$

$$Y_2 = Y_{ce} + \frac{Y_{b'c} (Y_{b'e} + g_m)}{Y_{b'c} + Y_{b'e} + Y_{b'c}} \quad (A8)$$

$$Y_3 = \frac{Y_{b'c} Y_{b'c}}{Y_{b'c} + Y_{b'e} + Y_{b'c}} \quad (A9)$$

$$G_m = \frac{Y_{b'c} g_m}{Y_{b'c} + Y_{b'e} + Y_{b'c}}, \quad (A10)$$

where

$$Y_{b'c} = g_{b'c} = \frac{1}{r_{b'c}}, \quad Y_{ce} = g_{ce} = \frac{1}{r_{ce}},$$

$$Y_{b'e} = g_{b'e} + j\omega C_{b'e} = \frac{1}{r_{b'e}} + j\omega C_{b'e}$$

$$Y_{b'c} = g_{b'c} + j\omega C_{b'c} = \frac{1}{r_{b'c}} + j\omega C_{b'c}$$

A.4 CONVERSION FROM HYBRID-PI TO Y EQUIVALENT CIRCUIT

In going from the hybrid-pi to the Y equivalent circuit, the input and output admittances of the normal-pi circuit are equated to the corresponding admittances given in terms of the Y parameters.

In terms of the normal-pi circuit the input and output admittances are

$$Y_{in} = Y_1 + Y_3 + \frac{Y_3 (G_m - Y_3)}{Y_2 + Y_3 + Y_L} \quad (A11)$$

and

$$Y_{out} = Y_2 + Y_3 + \frac{Y_3 (G_m - Y_3)}{Y_1 + Y_3 + Y_S} \quad (A12)$$

Comparing Equations (A11) and (A12) with (A3) and (A4), it is obvious that

$$Y_{11} = Y_1 + Y_3 \quad (A13)$$

$$Y_{22} = Y_2 + Y_3 \quad (A14)$$

$$Y_{12} = Y_3 \frac{Y_3 - G_m}{Y_3 + G_m} \quad (A15)$$

and

$$Y_{21} = G_m + Y_3 \quad (A16)$$

Substituting the hybrid-pi equivalent of Y_1 , Y_2 , Y_3 , and G_m in Equations (A13), (A14), (A15), and (A16) the Y parameters may be rewritten as

$$Y_{12} = \frac{Y_{b'}(Y_{b'e} + Y_{b'c})}{Y_{b'} + Y_{b'e} + Y_{b'c}} \quad (A17)$$

$$Y_{22} = Y_{ce} + \frac{Y_{b'c}(Y_{b'} + Y_{b'e} + g_m)}{Y_{b'c} + Y_{b'} + Y_{b'e}} \quad (A18)$$

$$Y_{21} = \frac{Y_{b'}(g_m + Y_{b'c})}{Y_{b'} + Y_{b'e} + Y_{b'c}} \quad (A19)$$

and

$$Y_{12} = \frac{Y_{b'}Y_{b'c}(Y_{b'c} - g_m)}{(Y_{b'} + Y_{b'e} + Y_{b'c})(Y_{b'c} + g_m)} \quad (A20)$$

A.5 EFFECTS OF UNILATERALIZATION ON CIRCUIT PARAMETERS

For most high frequency common emitter applications, the transistor is unilateralized. Unilateralization may be defined as the use of an external feedback network which connects the input to the output in such a way that the equivalent feedback current generator $Y_{12}V_2$ is made equal to zero.

Consider the circuit of Figure A4; Y_f is a feedback admittance and KV_2 is a voltage generator whose potential is proportional to the output voltage V_2 . Unilateralization is obtained by making the input circuit equation

$$I_1 = (Y_1 + Y_3 + Y_f)V_1 + (KY_f - Y_3)V_2 \quad (A21)$$

independent of V_2 . Therefore, for unilateralization

$$KY_f - Y_3 = 0$$

or

$$KY_f = Y_3. \quad (A22)$$

Under this condition

$$Y_{in} = Y_1 + Y_3 + Y_f$$

and

$$Y_{out} = Y_2 + Y_3.$$

It is seen from Equation (A22) that the condition for unilateralization is dependent only on the value of Y_3 . Consequently, when Y_3 changes due to changes in transistor bias or ambient temperature the transistor is no longer completely unilateralized, and the input and output admittances

are given as

$$Y_{in} = Y_1 + Y_3 + Y_f + \frac{(Y_3 - KY_f)(G_m - Y_3)}{Y_2 + Y_3 + Y_L} \quad (A23)$$

and

$$Y_{out} = Y_2 + Y_3 + \frac{(Y_3 - KY_f)(G_m - Y_3)}{Y_1 + Y_3 + Y_f + Y_S} \quad (A24)$$

Comparing Equations (23) and (A24) with (A3) and (A4), the Y parameters of the unilateralized network are given by the following expressions:

$$Y_{11} = Y_1 + Y_3 + Y_f \quad (A25)$$

$$Y_{22} = Y_2 + Y_3 \quad (A26)$$

$$Y_{21} = G_m + Y_3 \quad (A27)$$

and

$$Y_{12} = (Y_3 - KY_f) \frac{(Y_3 - G_m)}{(Y_3 + G_m)} \quad (A28)$$

A.6 ASSUMPTIONS USED FOR SIMPLIFYING THE Y PARAMETERS

The complexity of the Y equivalent circuit parameters suggests making as many assumptions as possible in order to simplify the relationships. The admittances Y_{in} and Y_{out} are reducible to

$$Y_{in} = Y_1 + Y_3 + Y_f$$

and

$$Y_{out} = Y_2 + Y_3,$$

when the transistor is unilateralized.

These relationships also hold when

$$\left| \frac{(G_m - Y_3)(Y_3 - KY_f)}{Y_2 + Y_3 + Y_L} \right| \ll |Y_1 + Y_3 + Y_f| \quad (A29)$$

and

$$\left| \frac{(G_m - Y_3)(Y_3 - KY_f)}{Y_1 + Y_3 + Y_f + Y_S} \right| \ll |Y_2 + Y_3| \quad (A30)$$

are satisfied.

For most transistors operating at normal emitter current and collector voltage

$$G_m \gg Y_3 \quad (A31)$$

$$Y_2, Y_L \gg Y_3 \quad (A32)$$

and

$$Y_S + Y_1 \gg Y_3 \quad (A33)$$

Under these circumstances, the conditions set forth in Equations (A29) and (A30) reduce to

$$\left| \frac{G_m(Y_3 - KY_f)}{Y_2 + Y_L} \right| \ll |Y_1|$$

and

$$\left| \frac{G_m(Y_3 - KY_f)}{Y_1 + Y_S} \right| \ll |Y_2|$$

A.7 Y PARAMETERS IN TERMS OF HYBRID-PI PARAMETERS

When the state of a transistor amplifier is limited by the conditions of Equations (A29) and (A30), the Y parameters in terms of the hybrid-pi parameters are:

$$Y_{11} = \frac{g_{b1}(g_{b1e}+g_{b1c})(g_{b1}+g_{b1e}+g_{b1c})+\omega^2 g_{b1}(C_{b1e}+C_{b1c})^2}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}+C_{b1c})^2} + j\omega \frac{g_{b1}^2(C_{b1e}+C_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}+C_{b1c})^2} + Y_f \quad (A34)$$

$$Y_{22} = g_{ce} + \frac{g_{b1c}(g_{b1}+g_m+g_{b1e})(g_{b1}+g_{b1e}+g_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2+\omega^2(C_{b1e}+C_{b1c})^2} + \omega^2 \frac{C_{b1c}g_m(C_{b1e}+C_{b1c})+C_{b1e}^2 g_{b1c}+C_{b1c}^2(g_{b1}+g_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}+C_{b1c})^2} + j\omega \frac{C_{b1c}(g_{b1}+g_{b1e})(g_{b1}+g_m+g_{b1c})-C_{b1e}g_{b1c}(g_m-g_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}C_{b1c})^2} + \frac{\omega^2 C_{b1c}C_{b1e}(C_{b1e}+C_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2+\omega^2(C_{b1e}+C_{b1c})^2} \quad (A35)$$

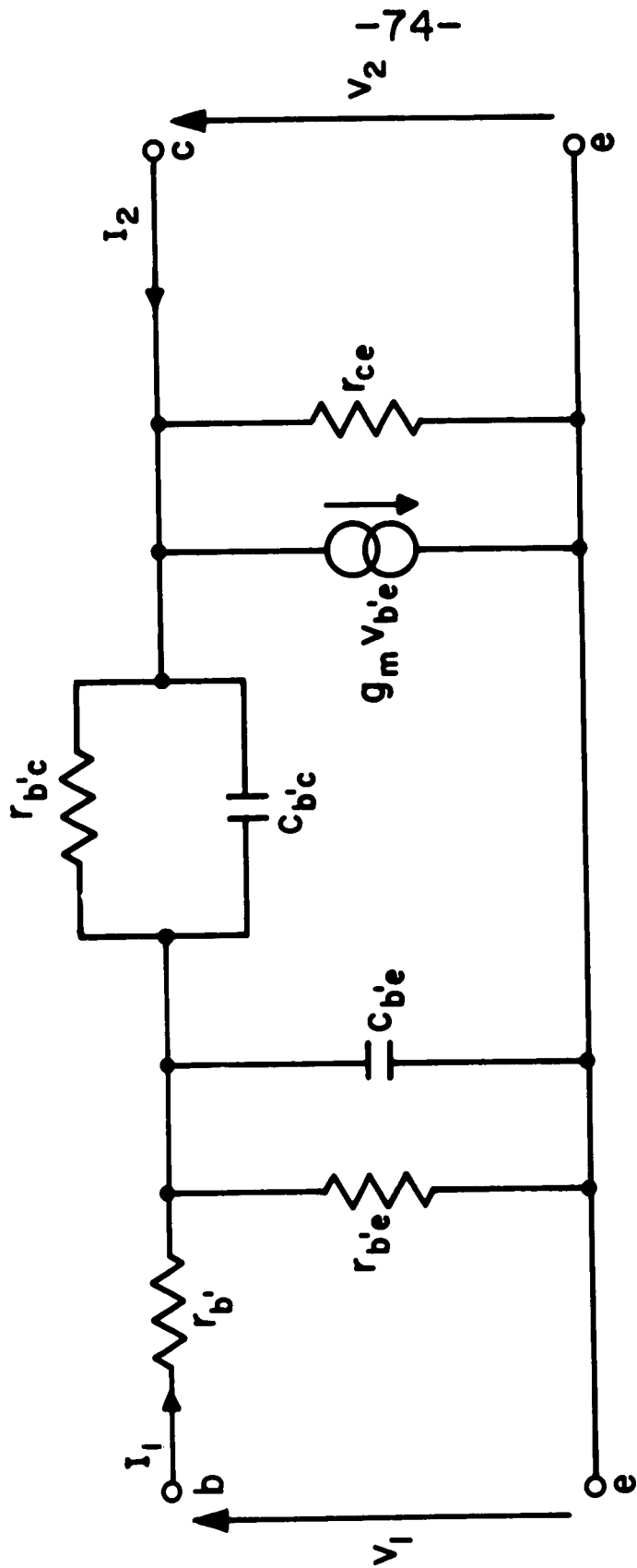
$$Y_{21} = \frac{g_{b1}g_m(g_{b1}+g_{b1e}+g_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2+\omega^2(C_{b1e}+C_{b1c})^2} - j\omega \frac{g_{b1}g_m(C_{b1e}+C_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2+\omega^2(C_{b1e}+C_{b1c})^2} \quad (A36)$$

and

$$\begin{aligned}
 Y_{12} = KY_f - & \frac{g_{b1}g_{b1c}(g_{b1}+g_{b1e}+g_{b1c})+g_{b1}\omega^2C_{b1c}(C_{b1e}+C_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}+C_{b1c})^2} \\
 & - j\omega \frac{g_{b1}C_{b1c}(g_{b1}+g_{b1e}+g_{b1c}) - g_{b1}g_{b1c}(C_{b1e}+C_{b1c})}{(g_{b1}+g_{b1e}+g_{b1c})^2 + \omega^2(C_{b1e}+C_{b1c})^2} .
 \end{aligned}$$

(A37)

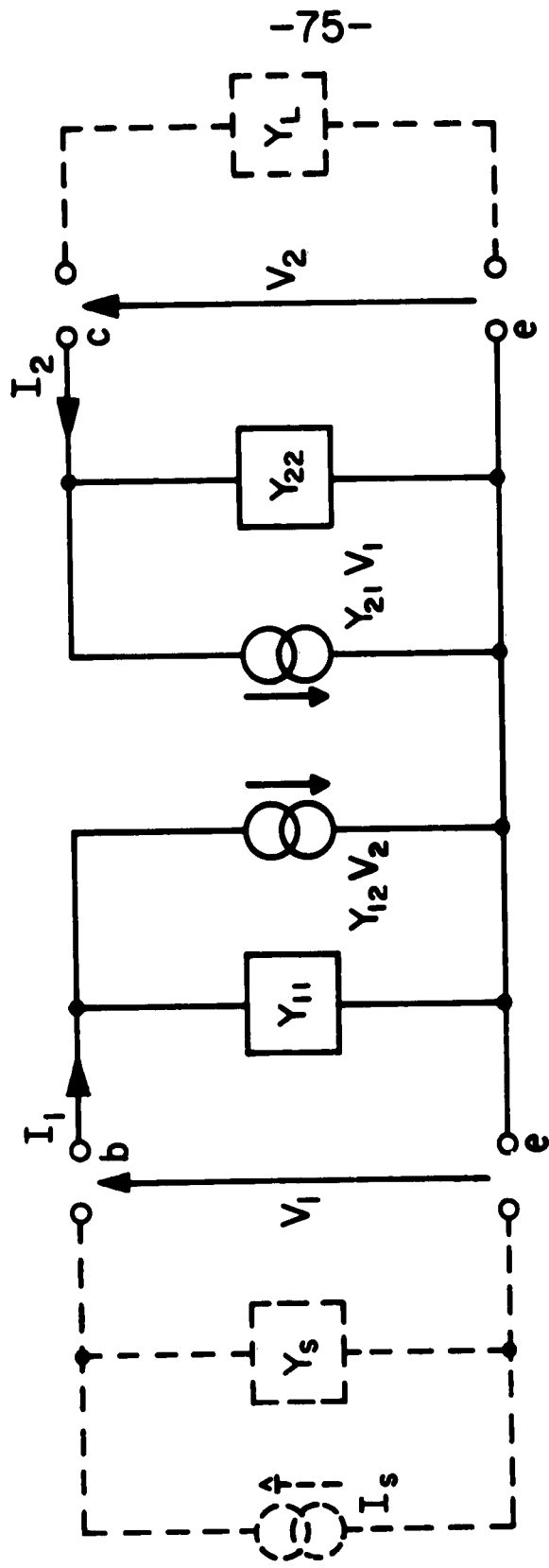
Simplification of these equations depends on the relative magnitudes of the hybrid-pi parameters and the particular operating frequency.



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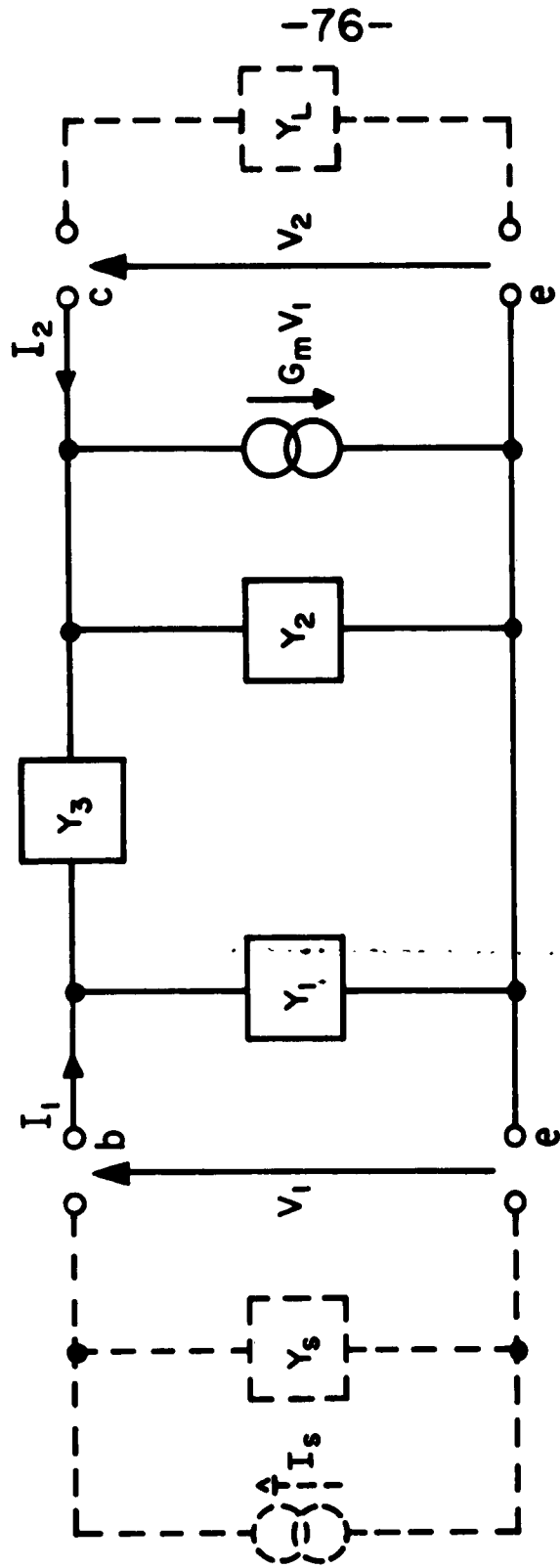
HYBRID-PI EQUIVALENT

FIGURE A1



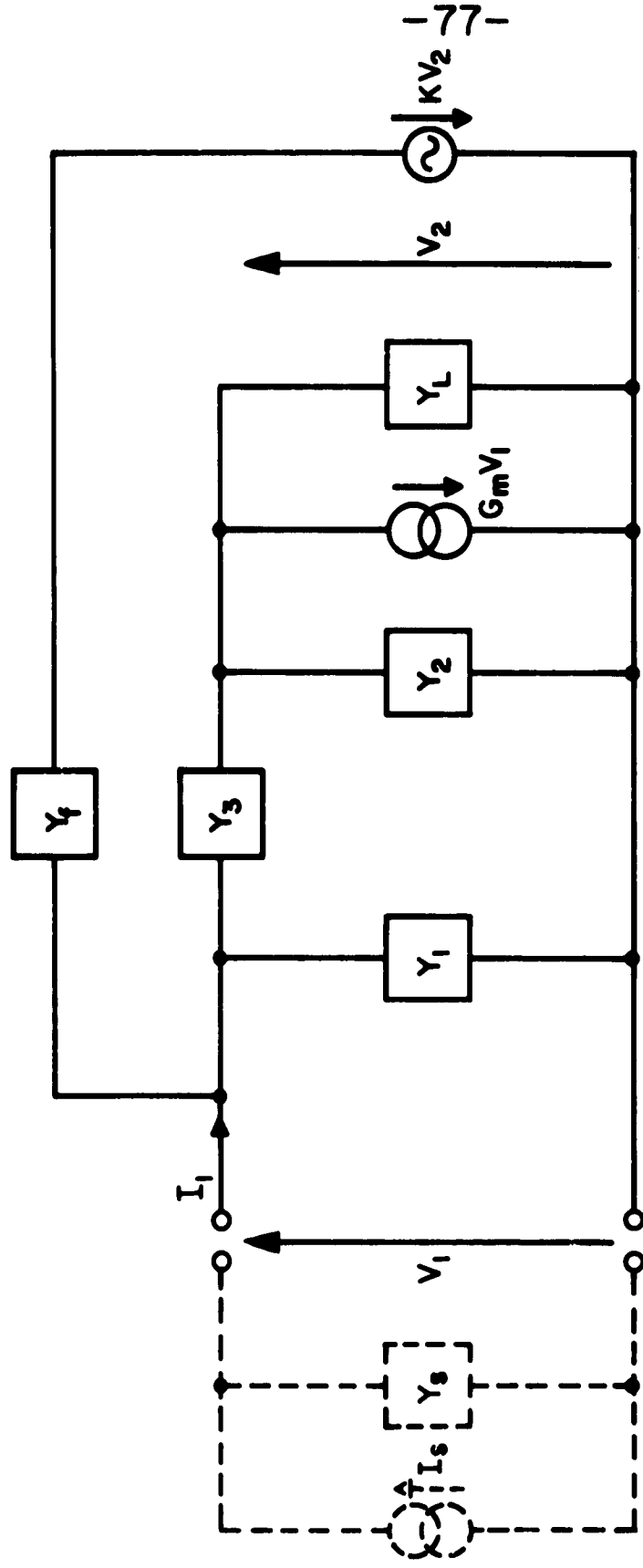
Y EQUIVALENT CIRCUIT

FIGURE A2



NORMAL-PI EQUIVALENT

FIGURE A3



UNILATERALIZED NORMAL-PI EQUIVALENT

FIGURE A4