U.S. ARMY SIGNAL RESEARCH AND DEVELOPMENT LABORATORY, FORT MONMOUTH, NEW JERSEY

STUDY OF MICROJUNCTION FORMATION TECHNOLOGY

SECOND QUARTERLY PROGRESS REPORT
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CBS LABORATORIES

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ABSTRACT

An investigation of the experimental method of determining the built-in voltage of abrupt pn junctions by capacitance vs. voltage measurements is given and possible errors are discussed.

Preliminary results on the lithographic use of the electron beam for fabricating semiconductor devices are presented.

A scaled down plasma torch for semiconductor applications is described.

The report closes with a summary and discussion of the electron beam work performed under this contract.

PURPOSE

The purpose of this contract is to investigate the effects of electron and/or ion-beam bombardment on treated and untreated silicon surfaces. The technology utilizing beam effects shall be developed in order to fabricate semiconductor structures, especially p-n junctions of small area with emphasis on a heavily doped surface layer. The attempt to fabricate device structures possessing useful electrical parameters shall be made to demonstrate the capabilities of techniques developed.

I. INTRODUCTION

A successful alloying of a predeposited impurity layer into the surface of a silicon base material by means of an electron beam was established during the first year of the investigation, which was concentrated mainly on the metallurgy and physics of the metal/silicon system and the electrical evaluation of the produced junctions isolated by mesa-etching. Diodes with excellent electrical characteristics were found. The purpose of the second year of the investigation was to refine the technology in order to get reproducible results and control over small dimensions which would transfer the new technology into a device fabrication stage. Work was confined to the Al-Si system, because most experience during the first year was gained in that field. As a high impurity doping level in the regrowth layer is important for the feasibility of the new technology for device fabrication, also an investigation of this problem, especially in relation to a possible non-equilibrium alloy-process as caused by the relatively short heating times of the electron beam, was carried out.

After the first quarter of attempting the above outlined goals a rather large complexity of the electron beam process was revealed, especially concerning surface conditions before impurity deposition, heat transfer between sample and surroundings during electron beam heating, control of the available electron gun machine, and doping level in the regrowth layer. This complexity would have made necessary a long range research program and disturbed the hope of rapidly developing the new inexpensive transistor and diode fabrication tool, which was desired by the sponsor of the project. During a meeting with engineers of the U.S. Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey, it was therefore decided to finish the study of the electron beam alloy process in the second quarter and to commence the investigation of the effects of ion bombardment on semiconductors leading to p-n junctions and ohmic contacts[1]. It was decided to use as a first approach to the ion beam work a simple plasma torch representing a source of heating and impurity coating. Especially, in the opinion

1. F. Brand, H. Jacobs, and A. Ramsa, U.S. Patent No. 2,854,362, "Formation of Junctions in Semiconductors", Sept. 30, 1958.

of the sponsor of the project, the change in the technology used for producing p-n junctions was necessary and more promising in respect to the purpose of the contract of rapidly developing the new device technology. It was also decided at the meeting mentioned above, to use the electron beam machine for lithographic techniques as applied to the photoresist method of fabricating semiconductor devices, with the inherent advantage in the control of dimensions and the ultimate resolution.

The main emphasis of work in the second quarter was therefore:

1. Completion of the doping level investigations by studying the feasibility of the built-in voltage measurement method for this purpose
2. The use of the electron beam for lithographic purposes on silicon
3. Construction of a plasma torch feasible for the ion beam investigation on semiconductors.

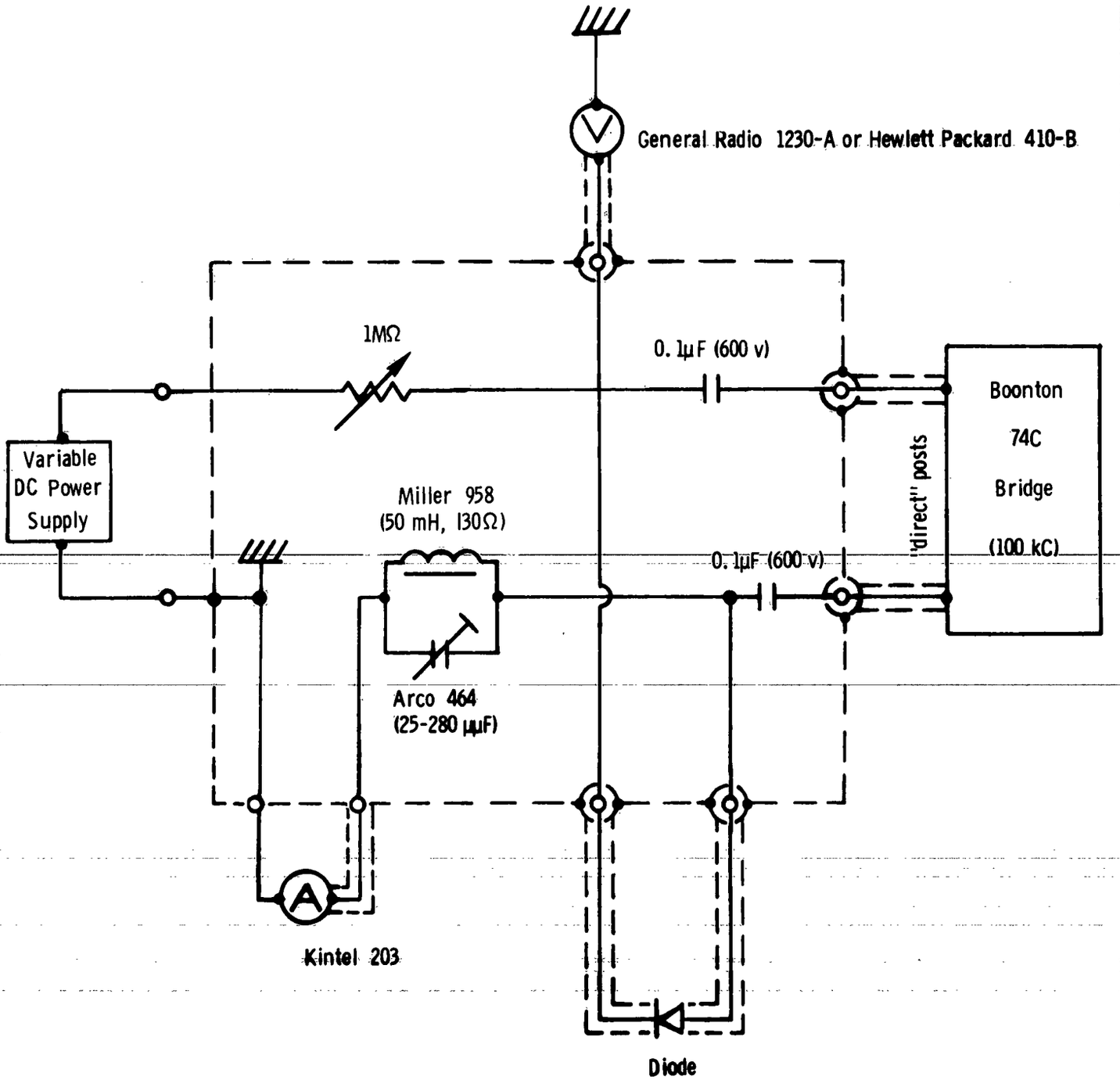
II. ELECTRICAL MEASUREMENTS ON ELECTRON BEAM ALLOYED JUNCTIONS

II.1 Aim of Measurements

As reported on in the First Quarterly Progress Report, discrepancies were found during investigating the Al doping level (N_p) in the regrowth layer formed by electron beam heating, by means of capacitance vs. voltage measurements of the produced pn junctions. The two methods for determining the doping level (N_p) are 1) evaluating the diffusion voltage (V_D), as found by extrapolating the $\frac{1}{C^2}$ vs. voltage line: $V_D = \frac{kT}{q} \ln \frac{N_n N_p}{n_i^2}$; 2) evaluating the slope K of the $\frac{1}{C^2}$ vs. voltage line: $K = \frac{2\varepsilon}{q} \frac{1}{A^2} \frac{N_n+N_p}{N_n N_p}$. For the first method the question arose as to whether or not the experimentally found diffusion voltage is really equal to the theoretical value calculated for a step junction or if there are some possible errors inherent to the experimental procedure effecting the measured value? The second method requires an accurately determined junction area (A) and, in case of $N_p > N_n$ which is to be expected, yields only a rough estimate of N_p or even just a statement $N_p \gg N_n$. Preliminary measurements indicated difficulties in finding an accurate value for the junction area for the second method. To enlighten the whole amount of problems a series of thoroughly prepared experiments were carried out.

II.2 Electrical Circuit Used for Capacitance Measurements

It was found in previous experiments that a change in the reverse current of a diode apparently caused by alterations of the surface conditions, was correlated with a change in the capacitance of the diode. As most experiments were performed on unpackaged units a change of surface conditions was rather frequent and it seemed desirable to measure capacitance and reverse current simultaneously. For this purpose a more sophisticated circuit for the capacitance measurements was designed (seen in Fig. 1). This circuit has two principal features, namely, 1) the shielding of the dc part from the ac bridge by the two capacitors of 0.1 μF that are high enough not to effect the measured small diode capacitance, and 2) the shielding of the ac part from the dc power supply and ammeter by the



Circuit used for capacitance measurements

Fig. 1

1M ohm resistor (usually kept in full) and the resonant circuit tuned to the bridge frequency (100 KC). Because of the second feature, an inductance change behind the ac blocking units was not seen by the bridge (as a matter of fact the capacitance change measured by the bridge that was caused by alterations of the dc power supply output or the range switch of the ammeter was smaller than 0.001 pF) and it was even possible to use a grounded ammeter, despite of the "direct" (that means ungrounded) mode of the capacitance measurements. The use of the grounded ammeter had also the advantage of eliminating fluctuations in the voltage of the dc power supply caused by insufficient insulation. The voltage was measured across the diode + the resonant circuit + the ammeter which was necessary because a grounded voltmeter was used. As the diode reverse currents are very low, a voltage drop across the low resistance of the ammeter and the choke of the resonant circuit is negligible. Range switching at the voltmeter had no influence on the capacitance measurements because of the high input impedance of the meter. The ac output level of the bridge was kept low (about 10 mv) in order not to effect the dc bias of the diode. With all these precautions mentioned and using well shielded connecting cables it was believed that highly accurate capacitance measurements for diodes could be performed. Contacts to the diode were made by a micromanipulator arrangement. All stray capacitances of the circuit were balanced out by the bridge before making contact. (In case of packaged units the stray capacitance has to be determined by extrapolation of the capacitance vs. voltage curve to infinite voltage.)

II.3 Equivalent Circuit for the Diode

For the theoretical evaluations the knowledge of the depletion layer capacitance (junction capacitance) is necessary. The capacitance seen by the bridge, however, is not necessarily the junction capacitance. An analysis of the electrical behavior of the diode is required. Fig. 2a and 2b show two possible equivalent circuits for the diode. r_s is the series resistance given by the resistance of the bulk and the contacts. R_{dc} may be called the dc parallel resistance as it is determined by the slope of the dc current-voltage characteristic. For a relationship $V \sim I^k$ it is given by $R_{dc} = k \frac{V}{I}$. R_a and R_b respectively describe a possible ac dissipation of the junction capacitor C_a and C_b in the series and parallel representation respectively. For small dissipation factors $\tan\delta < 0.1$, where:

$$\tan\delta = R_a \omega C_a = \frac{1}{R_b \omega C_b} \qquad (1)$$

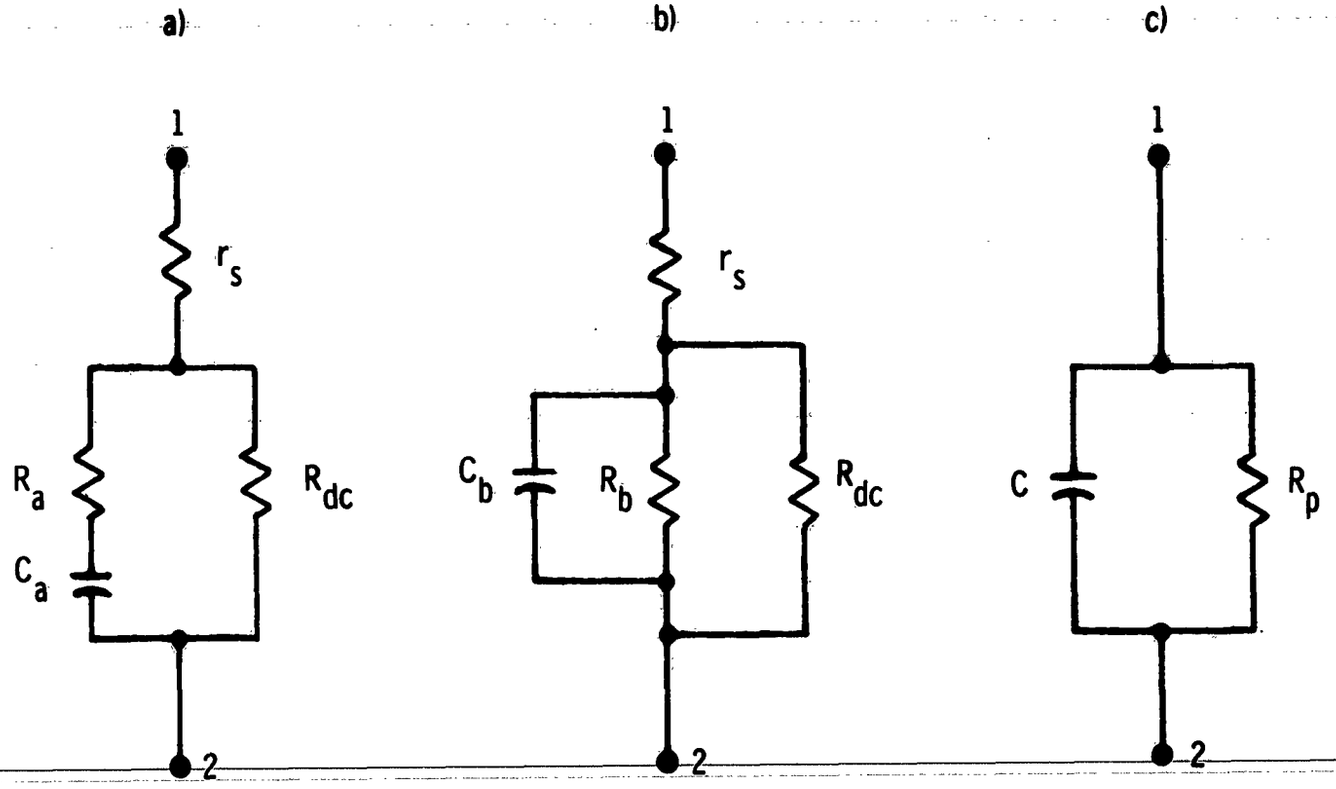


FIG 2 a) AND b) ASSUMED EQUIVALANT CIRCUIT OF THE DIODE IN SERIES AND PARALLEL REPRESENTATION RESPECTIVELY: r_s SERIES RESISTANCE
R_{dc} RESISTANCE OF THE DIODE AS GIVEN BY THE SLOPE OF THE dc CHARACTERISTIC
Ca OR C_b JUNCTION CAPACITANCE
R_a OR R_b DISSIPATION RESISTANCE (ZERO OR INFINITE RESPECTIVELY FOR dc)
c) CAPACITANCE C AND RESISTANCE R_p AS SEEN BY THE BRIDGE BETWEEN POINTS 1 AND 2.

C_a and C_b are practically equal and the choice of the equivalent circuit is left free for calculating the junction capacitance. We chose the series representation, despite the fact that the tang δ was larger in some cases of our measurements, because we felt that the physical situation is represented better in this way. The capacitance C and parallel resistance R_p seen by the bridge, on the other hand, is given by the circuit shown in Fig. 2c. The mathematical translation from circuit (a) to (c) yields:

$$\frac{C_a}{C} = \left(\frac{1}{\omega C}\,\frac{1}{R_p}\right)^2 \left(1 - \frac{R_p - r_s}{R_{dc}}\right)^2 + \left(1 + \frac{r_s}{R_{dc}}\right)^2 \qquad (2)$$

$$\tan\delta = R_a \omega C_a = \frac{\frac{1}{\omega C}\,\frac{1}{R_p}\left(1 - \frac{R_p - r_s}{R_{dc}}\right) - r_s \omega C_a}{1 + \frac{r_s}{R_{dc}}} \qquad (3)$$

In case of $r_s \ll R_{ds}$ which usually holds we get the simplified relations ($R_p \ddagger R_{cd}$):

$$\frac{C_a}{C} - 1 = \left(\frac{1}{\omega C}\,\frac{1}{R_p}\right)^2 \left(1 - \frac{R_p}{R_{dc}}\right)^2 \qquad (4)$$

$$\tan\delta = R_a \omega C_a = \frac{1}{\omega C R_p}\left(1 - \frac{R_p}{R_{dc}}\right) - r_s \omega C_a \qquad (5)$$

As seen from Eq. (4) the measured capacitance C is only equal to the junction capacitance C_a if $R_p \approx R_{dc}$ or $\frac{1}{\omega C} \ll R_p$, in which case also the dissipation factor is small.

II.4 Measurements and Results

Table 1 shows some results received from diodes on 1 ohm cm n-type silicon ($N_n = 5.4 \times 10^{15}\,cm^{-3}$) fabricated by evaporating a definite area with Al and subsequent electron beam alloying. After alloying the diode area A_{meas} was double checked by microscopic means. The measured built-in voltage values V_D would give doping levels (N_p) from 2×10^{14} to $2 \times 10^{16}\,cm^{-3}$. On the other hand, evaluation of the slope K with A_{meas} leads to discrepancies. One would have to assume $N_p \gg N_n$, but even the N_n calculated in this case gets too small. This suggests that the measured diode area is smaller than the real junction area.

#	A_{meas}/cm^2	$I_r(1V)/a$	$\frac{I_r(1V)}{A_{meas}\ a\ cm^2}$	V_D/V	$K/F^{-2}V^{-1}$	A_{calc}/cm^2	$\frac{A_{calc}}{A_{meas}}$
1	3.9×10^{-5}	1.5×10^{-7}	3.8×10^{-3}	0.58	1.26×10^{23}	1.28×10^{-4}	3.3
2	8.5×10^{-4}	8.7×10^{-6}	1.0×10^{-2}	0.68	1.08×10^{21}	1.42×10^{-3}	1.67
3	1.07×10^{-3}	1.0×10^{-5}	1.0×10^{-2}	0.62	8.8×10^{20}	1.57×10^{-3}	1.61
4	1.25×10^{-3}	4.0×10^{-6}	3.2×10^{-3}	0.69	6.2×10^{20}	1.88×10^{-3}	1.50

Table 1. Electron beam alloyed diodes on 1 ohm cm n-type silicon

We have therefore calculated A from K with the assumption $N_p \gg N_n$ yielding the smallest value possible. This leads to values A_{calc} considerably larger than A_{meas}, especially in the case of the smallest area (# 1). The reason for this discrepancy seems to be given by two phenomena which are also responsible for the relatively high reverse currents: 1) nonplanarity of the junction caused by non-uniform alloying because of an accumulation of liquid Al on surface imperfections and/or non-equilibrium regrowth; angle lapping and staining of one of the diodes revealed a nonplanarity; 2) an increased effective junction area caused by surface inversion channels resulting in high reverse leakage currents. This phenomenon is clearly seen in Table 2 for mesa diode 2d (columns 6 through 10, lines 16 and 17). It is believed that the especially high value of A_{calc}/A_{meas} for # 1 in Table 1 is caused by this effect because of the especially high value of the diode boundary to diode area relation of the strip geometry in this case (this relation also increases with decreasing area).

Table 2 comprises a series of measurements taken with electron beam alloyed mesa diodes on 10 ohm cm n-type base silicon ($N_n = 4.9 \times 10^{14} cm^{-3}$). The samples were freshly etched in HCL, rinsed in deionized water and then heated for about 1 minute to $400^{\circ}F$ in ambient air. Whereas a short heating improved the reverse characteristic a more intense heating caused a deterioration (Fig. 11). This deterioration could be abolished by a new etching. The series was made mainly to investigate effects causing an alteration of the diffusion voltage (V_D) as determined from the $\frac{1}{C^2}$ vs. voltage line, where C is the measured capacitance. (Examples are seen in Figs. 3 through 6.) The results are as follows:

A bad contact to the diode causing a high series resistance r_s increases the measured V_D (Fig. 3). This effect was also demonstrated by inserting external series resistors of 10 K ohm and 47 K ohm (Fig. 4). The effects on the C vs. voltage relationship itself are rather weak. The K values are increasing a little bit, the influence being larger in case of a bad contact, whereas the power n in the relationship $C \sim (V + V_D)^{-n}$ decreases slightly from 1/2 only in case of a bad contact (Figs. 7 and 8). The reason for the different behavior of an external series resistor and the contact resistance is apparently given by the non-linearity of the latter one. The bracketed values of r_s in Table 2,

	Sample	r_s/Ω	V_D/v	$\frac{K}{10^{22}\varepsilon^{-2}v^{-1}}$	n	$A_{meas.}$ $10^{-3}cm^2$	$A_{calc.}$ $10^{-3}cm^2$	$\frac{A_{calc.}}{A_{meas.}}$	I_r / a at - 5v	$\frac{I_r}{A_{meas}}$ $10^{-5}a/cm^2$	R_{p}/Ω at - 1v	R_{dc}/Ω at - 1v	tang δ
1	1 a	(20k)	0.61	1.57	0.498	1.37	1.21	0.88	7.7×10^{-8}	5.6	2.2M		
2	b	(20k)	0.60	1.01	0.496	1.85	1.51	0.82	2.5×10^{-8}	1.4	2.1M		
3	b	(25k)	1.00	1.22	0.472	"	1.38	0.75	2.6×10^{-7}	1.4	1.2M		
4	b	300	0.52	0.970	0.496	"	1.54	0.83	5.4×10^{-8}	2.9	12M	96M	0.013
5	b	10k	0.55	0.985	0.496	"	1.53	0.83	5.2×10^{-8}	2.8	2.4M	96M	0.028
6	b	47k	0.88	1.02	0.496	"	1.51	0.82	8.1×10^{-8}	4.4	600k	54M	0.12
7	b	forward biased diode	0.48	0.964	0.500	"	1.55	0.84	7.3×10^{-8}	3.9	6.0M	59M	0.026
8	c	(12k)	0.56	1.70	0.492	1.37	1.17	0.85	5.7×10^{-8}	4.2	4.4M		
9	d	(7k)	0.55	3.63	0.500	0.91	0.80	0.88	5.4×10^{-8}	5.8	8M		
10	e	(12k)	0.78	3.47	0.467	1.15	0.82	0.71	5.1×10^{-8}	4.4	4.8M		
11	e	(15k)	0.55	2.73	0.500	"	0.92	0.80	5.4×10^{-8}	4.7	5.5M		
12	f	(7k)	0.58	5.64	0.504	0.71	0.64	0.90	2.7×10^{-8}	3.8	22M		
13	f	(20k)	0.83	6.64	0.480	"	0.59	0.83	8.5×10^{-8}	12.0	14.5M		
14	2 d	500	0.52	0.498		1.30	2.16	1.66			220k	675k	0.45
15	d	10k	0.60	0.650		"	1.88	1.45			240k	795k	0.40
16	d	290	0.53	0.488	0.581	"	2.18	1.68	4.2×10^{-6}	320	195k	800k	0.55
17	d	290	0.53	1.05	0.513	"	1.48	1.13	2.8×10^{-8}	2.2	2.7M	160M	0.072

Remarks: Col. 2: Series resistance to the diode; in brackets: contact resistance measured at 4 ma forward current. Line 7: a forward biased Zenerdiode is in series.

Col. 3: Built-in voltage as measured by extrapolating the $\frac{1}{C^2}$ vs. voltage line, where C is the measured capacitance

Col. 4: K = slope of the $\frac{1}{C^2}$ vs. voltage line

Col. 5: Slope n of C vs. $(V + V_D)$ in log-log representation

Col. 6: Mesa area measured by microscopic photographing

Col. 7: Junction area calculated from K with the assumption $N_p \gg N_n$

Col. 9: Reverse current at -5 v

Col. 11: R_p = parallel resistance as measured with the bridge at 100 KC

Col. 12: R_{dc} = resistance of the diode as given by the slope of the d-c characteristic

Col. 13: Tang δ = dissipation factor without concerning R_{dc} at 100 KC.

Table 2.

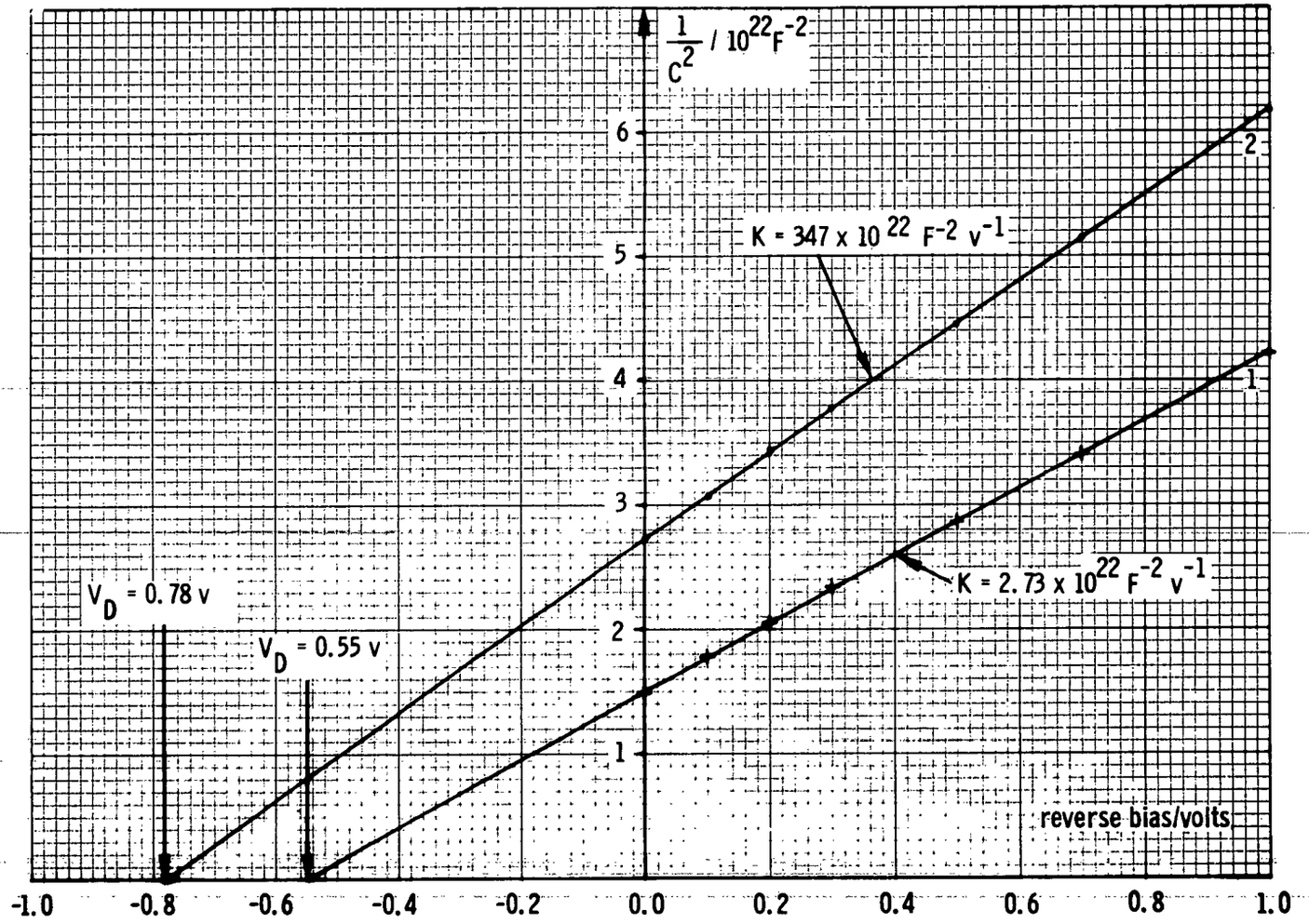


Fig. 3 $\frac{1}{C^2}$ vs. voltage for diode 1e: 1 contact resistance low, 2 contact resistance high

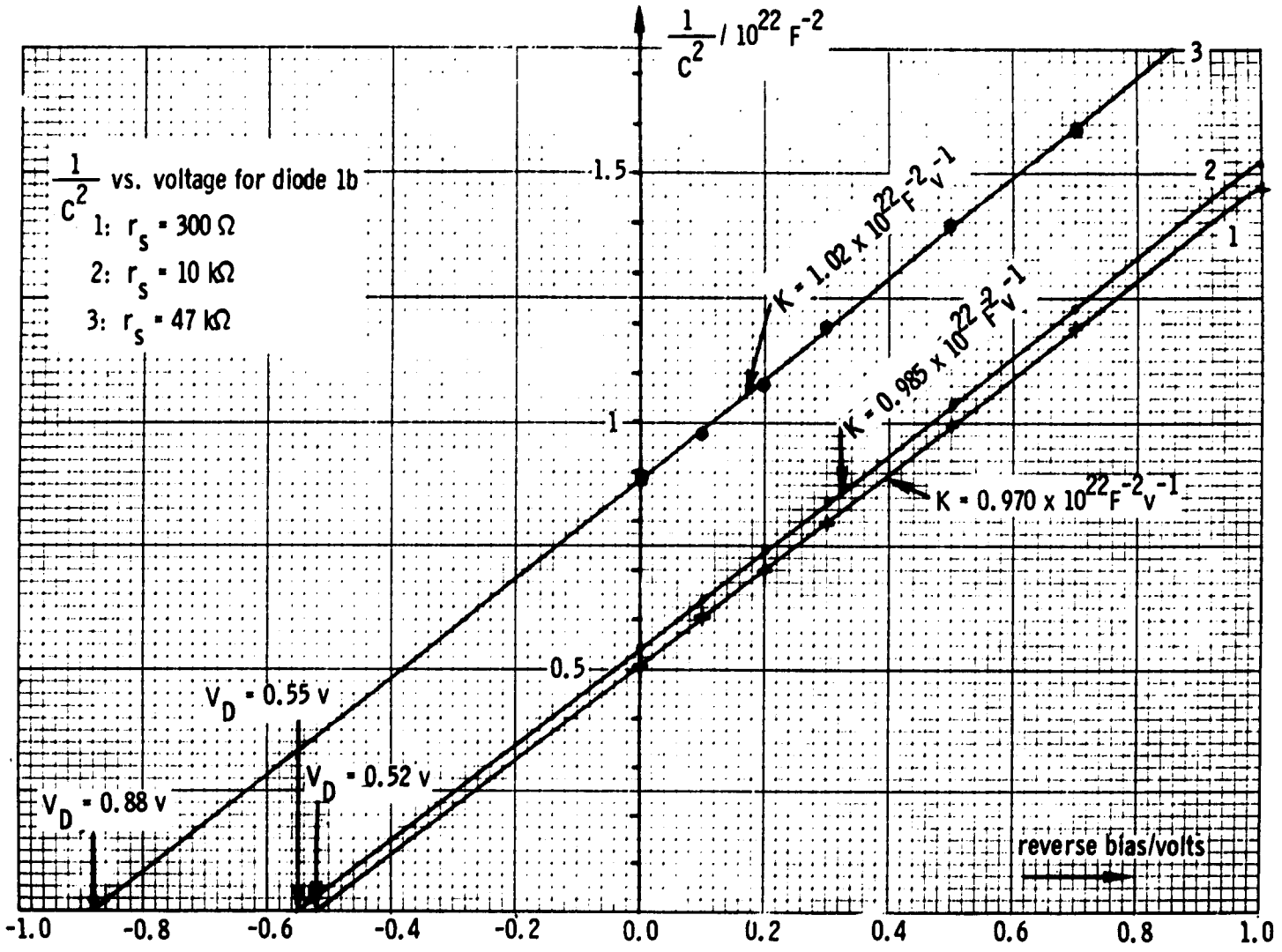

$\frac{1}{C^2}$ / 10^{22} F^{-2}
$\frac{1}{C^2}$ vs. voltage for diode 1b
1: r_s = 300 Ω
2: r_s = 10 kΩ
3: r_s = 47 kΩ
K = 1.02 x 10^{22} F^{-2} v^{-1}
K = 0.985 x 10^{22} F^{-2} v^{-1}
K = 0.970 x 10^{22} F^{-2} v^{-1}
V_D = 0.55 v
V_D = 0.52 v
V_D = 0.88 v
reverse bias/volts
3
2
1
1.5
1
0.5
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4

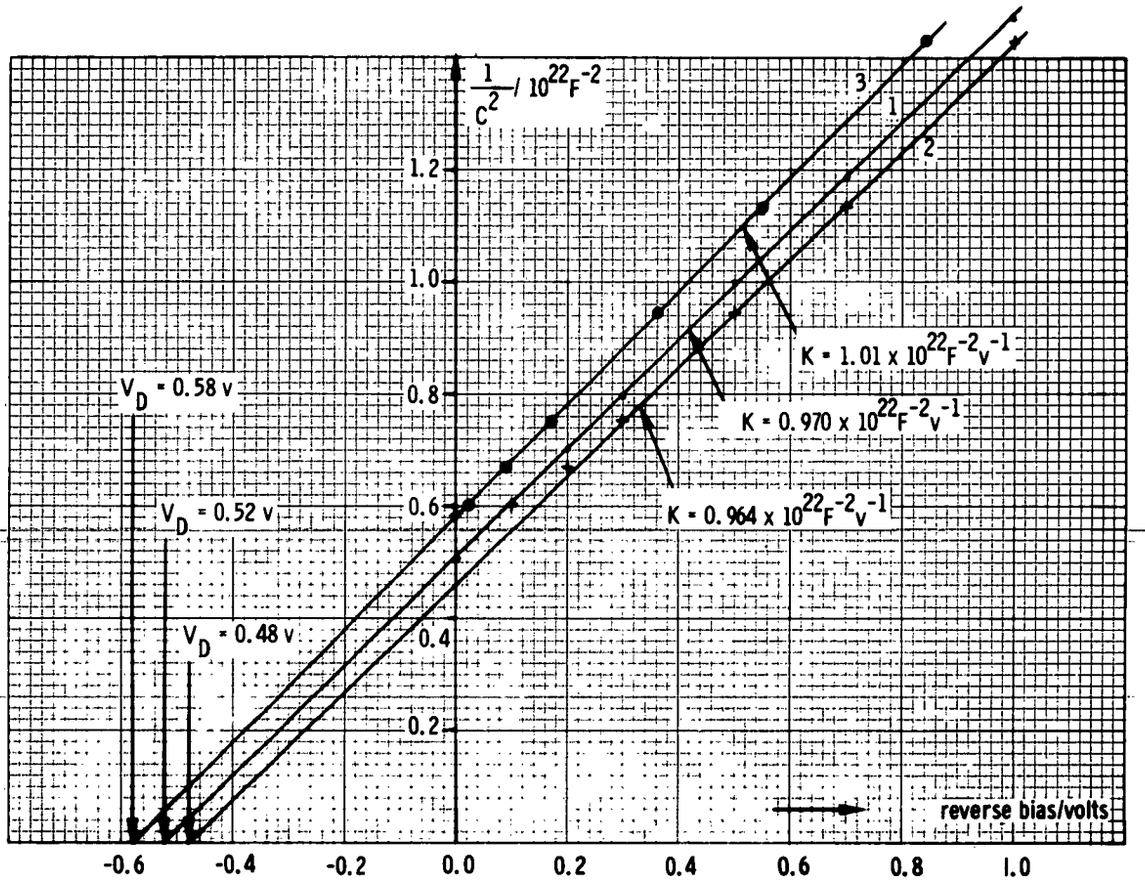


Fig. 5 $\frac{1}{C^2}$ vs. voltage for diode 1b: 1 r_s = 300 Ω, 2 with forward biased zener diode in series, 3 same as 2 but voltage drop across forward biased diode corrected

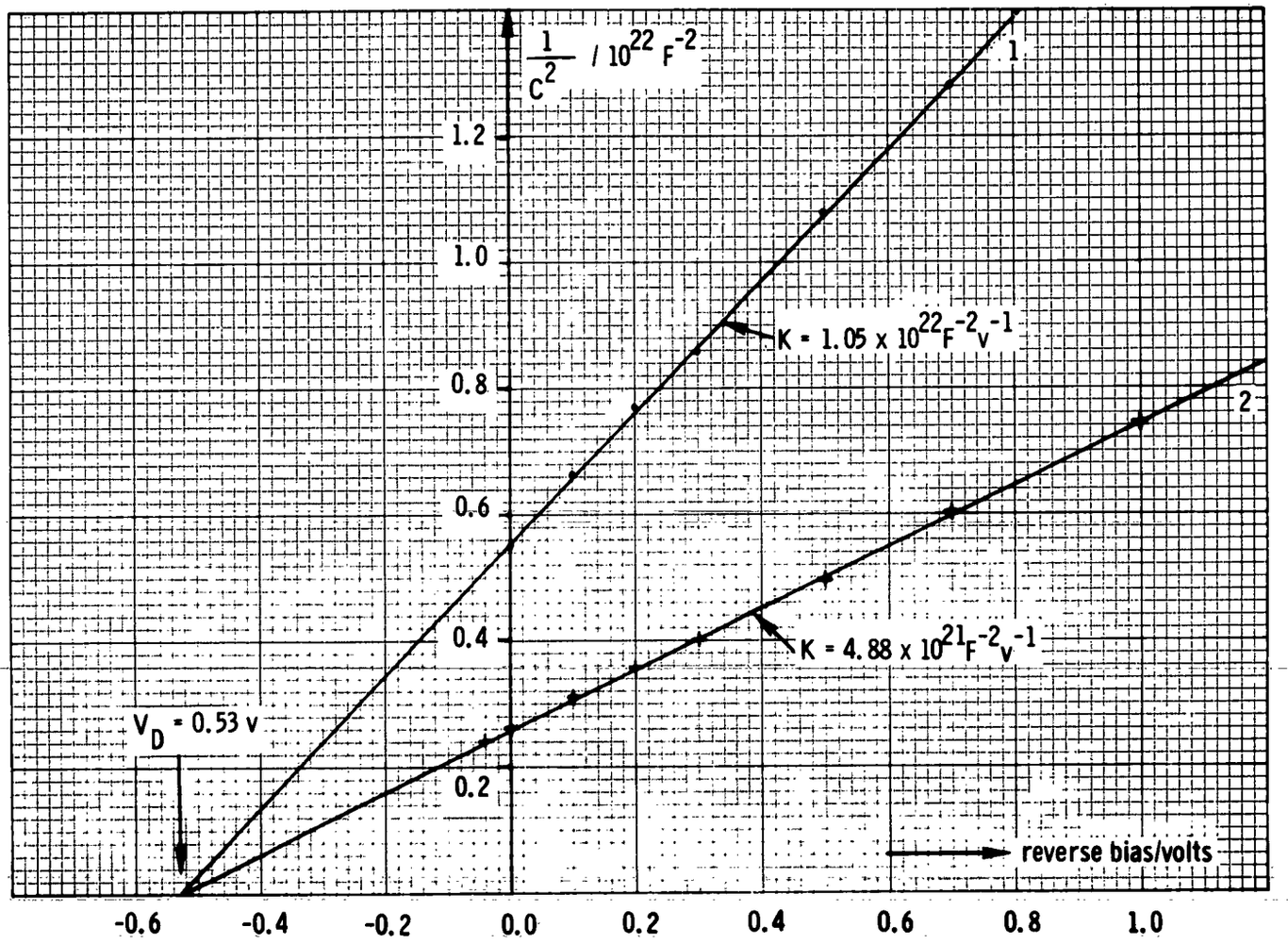
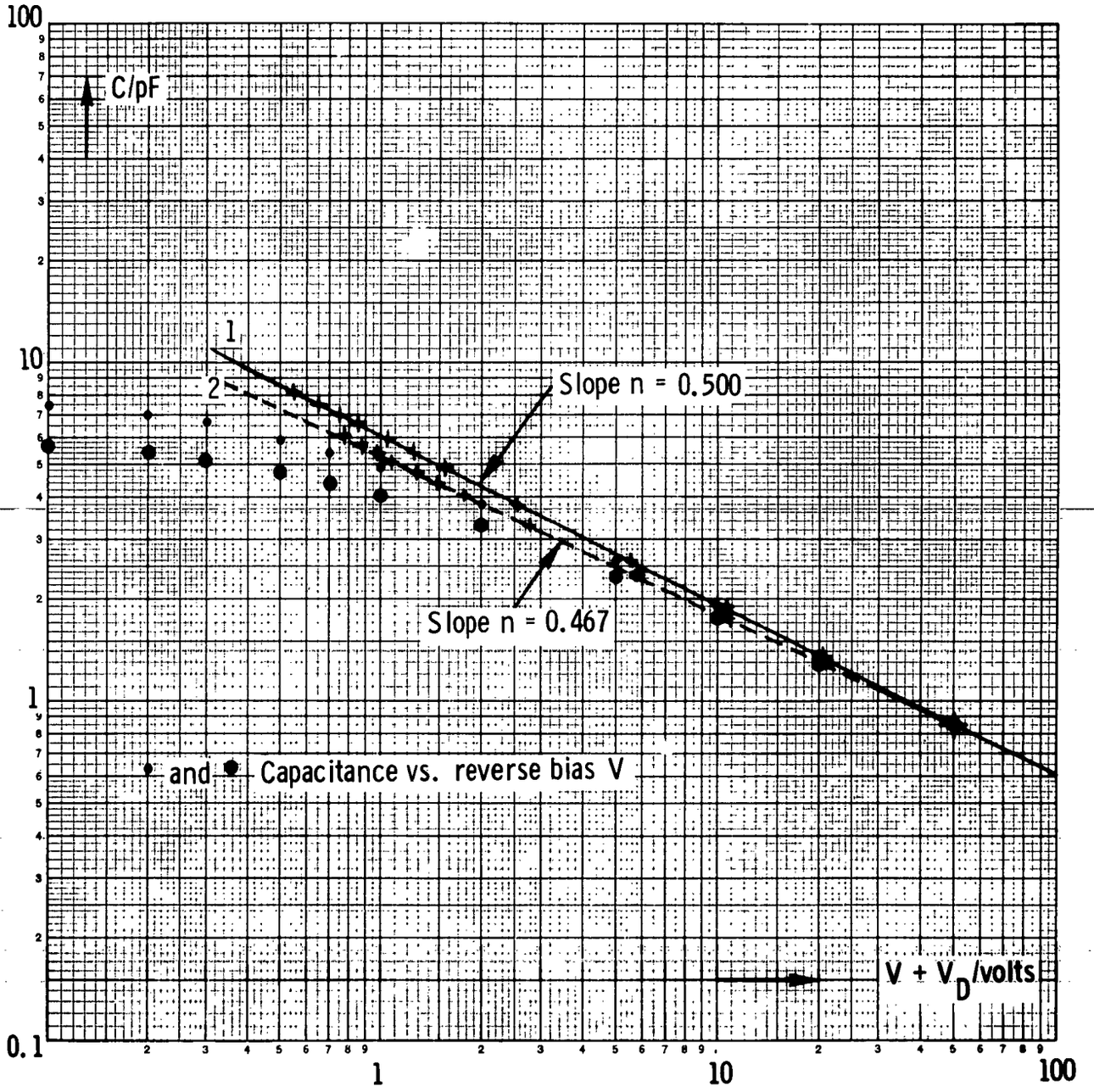
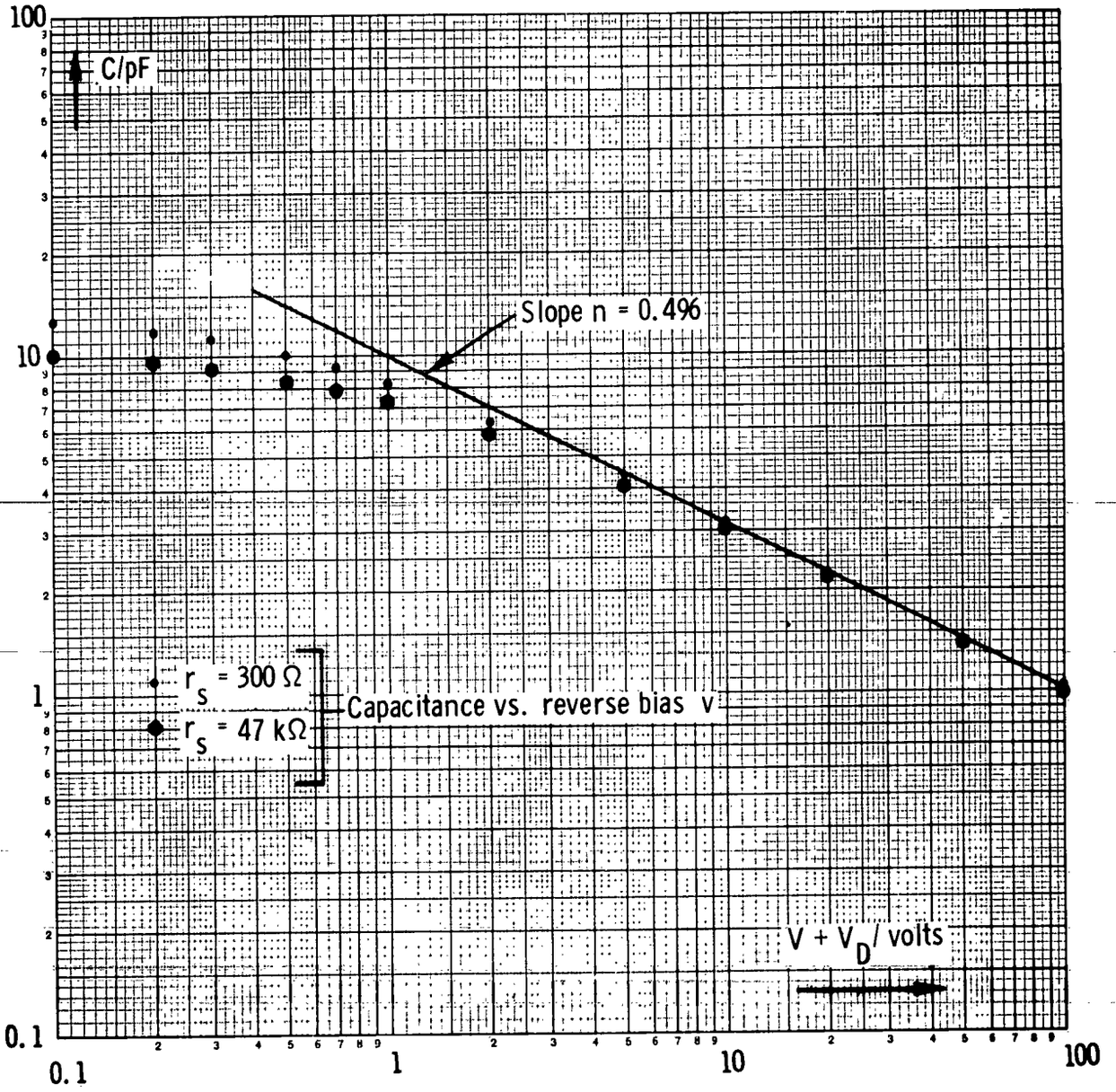


Fig. 6 $\frac{1}{C^2}$ vs. voltage for diode 2d: 1 low reverse current, 2 high reverse current



Capacitance vs. voltage characteristic for diode 1c
1. low contact resistance: V_D = 0.55 v
2. high contact resistance: V_D = 0.78 v

Fig. 7



Capacitance vs. voltage characteristic for diode 1b:all 3 cases of Fig. 4 give the same line.

Fig. 8

column 2, are measured at 4 mA forward current and, therefore, may serve only as an orientation value for the effective series resistance (line 10 for instance should be expected to have a higher r_s than line 11). The increase of the measured V_D, and the other effects, are caused of course by a decrease of the measured capacitance C according to formula (2). Table 3 shows that the calculated junction capacitance C_a is equal for each r_s within about 1%. A possible voltage drop at r_s that might have an effect on the measurements is still negligibly small because of the very low reverse currents or in other words, because of $R_{dc} \gg r_s$.

A forward biased Zener diode in series to the diode caused a slight decrease in the measured V_D (Fig. 5) but no change in K and n. This is due to the voltage drop across the forward biased diode. There should be expected a larger effect but this is partly balanced out by the drop of the measured C due to the resistance of the diode in series (correcting the voltage drop one gets: $V_D = 0.58$ v; $K = 1.01 \times 10^{22}$; and $n = 0.496$).

In case of a deterioration of the reverse characteristic of the diode caused by increased surface leakage, as it was observed for mesa diode 2d, see Fig. 11, no change in the measured V_D value was found (Fig. 6). This suggests that the surface inversion layer responsible for the high leakage has about the same doping as the recrystallized region. The quantity K shows a considerable decrease which is due to the increase of the effective diode area represented by the surface channels, (see Table 2, Column 8). Another striking feature is a rather large increase of the power n in the C vs. $(V + V_D)$ relationship (Fig. 9). This is not quite understood because by assuming a voltage dependence of the surface-channel (increase with increasing voltage) one would rather expect the opposite effect. There was found, for example, an increased capacitance at zero voltage after higher voltages had been applied; the capacitance recovered after a while to the original value.

The investigation of the ac dissipation of the mesa diodes (at 100 KC) by an analysis of the equivalent circuit (a) of Fig. 2 is shown in Tables 3 and 4 (see also Table 2). The incrimental d-c resistance was determined by the equation $R_{dc} = k \frac{V}{I}$, where k is the slope to the d-c characteristic in a log-log representation, as seen, e.g., in Figs. 10 and 11. The main results are a

	r_s = 300 Ω					r_s = 10 KΩ					r_s = 47 KΩ				
Reverse Bias V/volts	R_p/Ω	R_{dc}/Ω	$\frac{1}{\omega C}$/Ω	$\frac{1}{\omega C_a}$/Ω	tangδ	R_p/Ω	R_{dc}/Ω	$\frac{1}{\omega C}$/Ω	$\frac{1}{\omega C_a}$/Ω	tangδ	R_p/Ω	R_{dc}/Ω	$\frac{1}{\omega C}$/Ω	$\frac{1}{\omega C_a}$/Ω	tangδ
0.1	4.3M	25 M	124K	124K	0.022	1.0 M	25 M	127K	125K	0.042	300K	17 M	158K	124K	0.139
0.2	5.2M	39 M	134K	134K	0.020	1.15M	38 M	137K	135K	0.041	340K	24 M	165K	134K	0.130
0.3	6.4M	49 M	142K	142K	0.017	1.31M	48 M	146K	144K	0.039	360K	29 M	173K	141K	0.141
0.5	8.2M	67 M	159K	159K	0.015	1.6 M	64 M	162K	160K	0.036	430K	36 M	188K	158K	0.135
0.7	9.5M	83 M	173K	173K	0.014	1.85M	78 M	176K	174K	0.036	500K	42 M	201K	173K	0.127
1.0	12 M	96 M	193K	193K	0.013	2.2 M	96 M	196K	194K	0.035	600K	54 M	219K	193K	0.116
2.0	20 M	123M	247K	247K	0.0092	3.1 M	128M	250K	249K	0.039	900K	89 M	272K	250K	0.112
5.0	32 M	166M	365K	365K	0.0084	6.0 M	176M	369K	367K	0.032	1.7M	138M	389K	369K	0.099
10	50 M	230M	502K	502K	0.0072	10 M	245M	507K	506K	0.029	2.7M	167M	528K	509K	0.100

Table 3. Diode 1b (See also line 4 through 6 of Table 2)

	$I_r(5v) = 2.8 \times 10^{-8}$a				$I_r(5v) = 4.2 \times 10^{-6}$a				
Reverse Bias V/volts	R_p/Ω	R_{dc}/Ω	$\frac{1}{\omega C} = \frac{1}{\omega C_a}/\Omega$	tang δ	R_p/Ω	R_{dc}/Ω	$\frac{1}{\omega C}/\Omega$	$\frac{1}{\omega C_a}/\Omega$	tang δ
0.1	1.5 M	28 M	129K	0.079	120K	530K	88.4K	66.7K	0.57
0.2	1.65M	46 M	140K	0.080	128K	550K	94.7K	72.0K	0.56
0.3	1.8 M	61 M	147K	0.078	137K	590K	101 K	76.8K	0.56
0.5	2.1 M	88 M	165K	0.075	154K	650K	112 K	85.6K	0.55
0.7	2.3 M	112M	180K	0.075	170K	710K	123 K	94.3K	0.55
1.0	2.7 M	160M	201K	0.072	195K	890K	138 K	106 K	0.55
2.0	4.0 M	270M	260K	0.063	260K	1.3M	181 K	138 K	0.56
5.0	8.5 M	480M	389K	0.044	500K	2.55M	288 K	237 K	0.46
10	15 M	750M	542K	0.035	900K	4.8M	427 K	370 K	0.39

Table 4. Diode 2d: $r_s = 290\Omega$, corresponding reverse characteristics (see Fig. 11, also see Table 2, line 17 and 18).

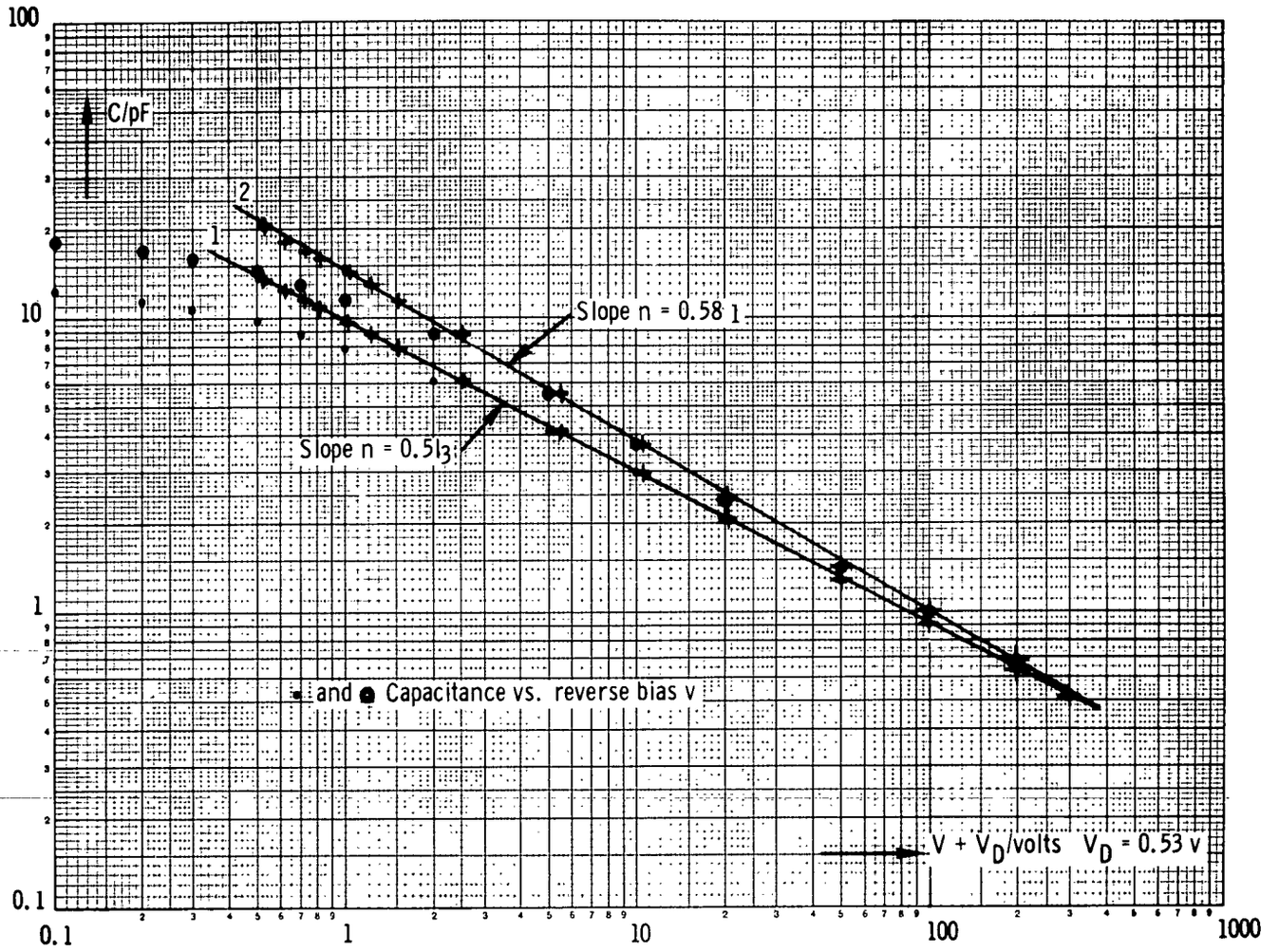
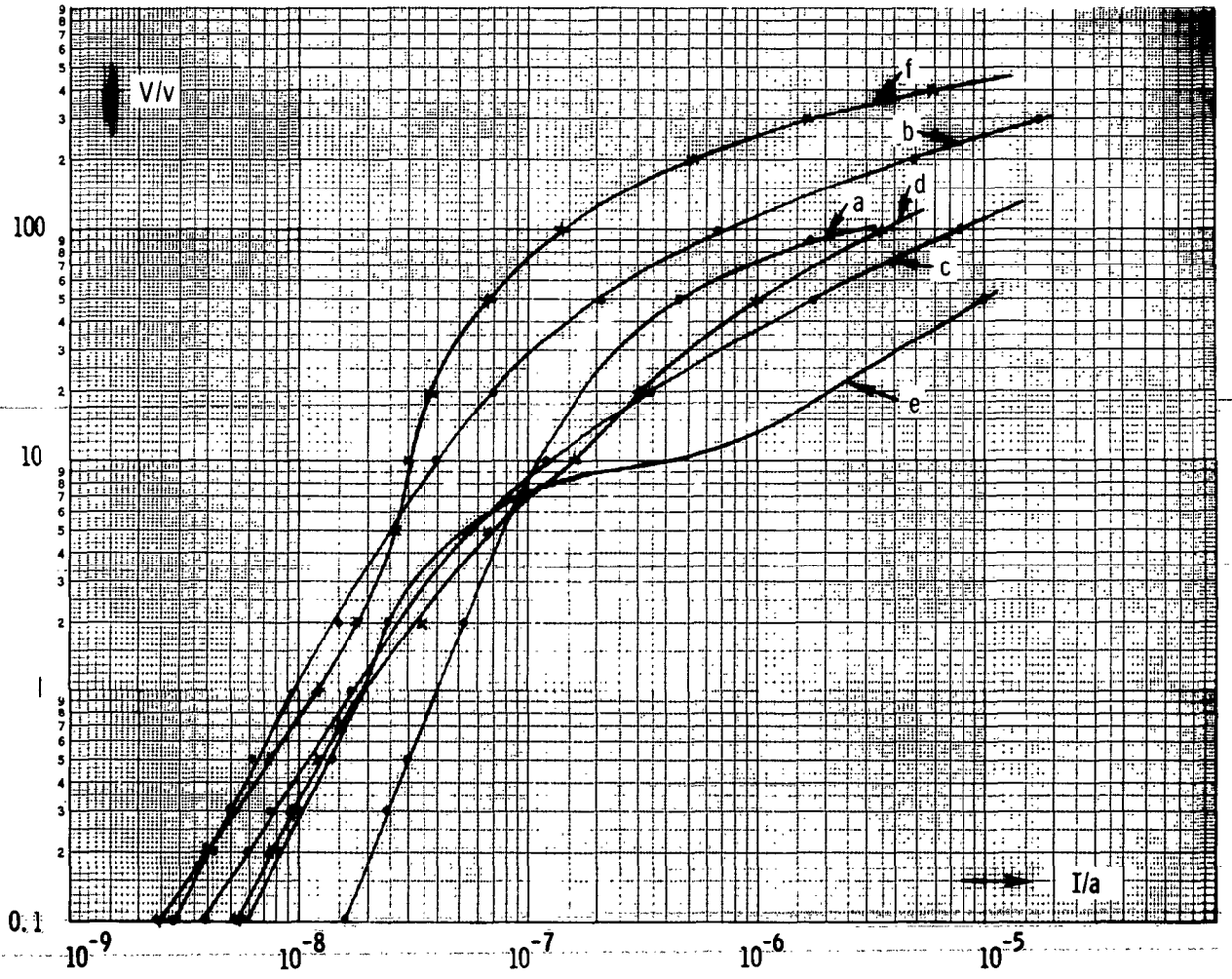


Fig. 9 Capacitance vs. voltage characteristic for diode 2d

1 small reverse current

2 large reverse current



Reverse characteristics (dark currents)

Fig. 10

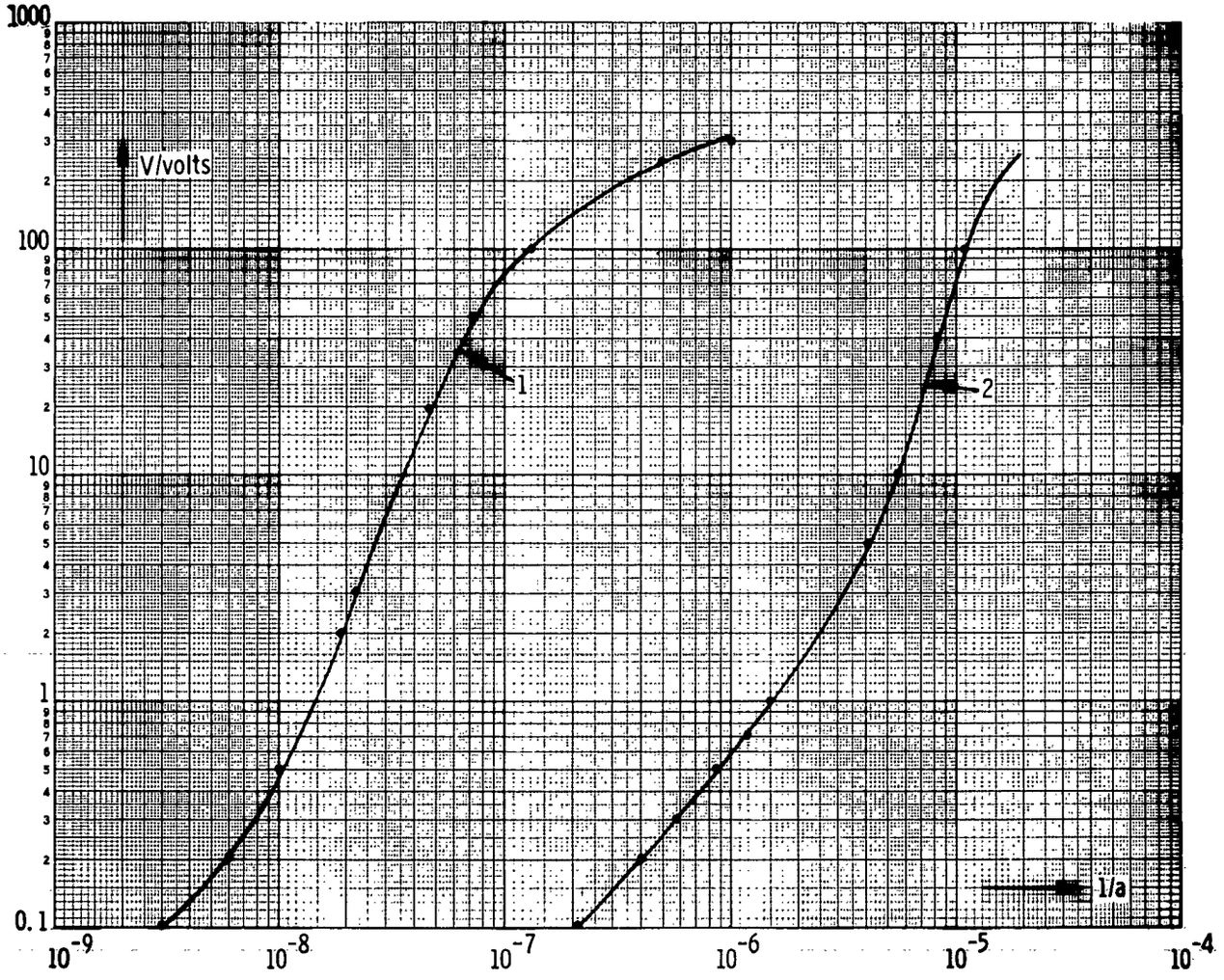


Fig. 11 Reverse characteristic of diode 2d:
1 after short heating to about 400°F,
2 after long heating to about 600°F in ambient air.

decrease of the dissipation factor tang δ with increasing voltage, an increase in the case of a high external series resistance, and a considerable increase for the deteriorated reverse characteristic of Fig. 11. Whereas the second effect is rather strange and seems to indicate that the underlined equivalent circuit is too rough a simplification of the real diode behavior, the two other effects may be explained by the assumption that the dissipation is mostly caused by the surface channels rather than by the bulk. The decrease with voltage suggests a decreasing influence of the surface channels which is consistent with the increased power n of the C vs. $(V + V_D)$ relationship (Fig. 9).

For all investigated cases the junction area has been calculated from K assuming $N_p \gg N_n$ and was compared with the microscopically measured mesa area A_{meas} (see Column 7 and 8 of Table 2). Comparison of the results in case of small r_s (influences of r_s negligible) show the influence of the surface channels very clearly (lines 4, 16 and 17): The higher the ratio A_{calc}/A_{meas}, the higher tang δ gets and the more n increases from the 1/2 power. In case of line 4 a surface channel effect seems to be practically absent; here even is $A_{calc} < A_{meas}$ from which one has to conclude that the assumption $N_p \gg N_n$ is not valid in this case. The conditions $A_{calc} = A_{meas}$ leads to $N_p = 10^{15} cm^{-3}$ which would correspond to a $V_D = 0.56$ v (measured value 0.52 v yielding $N_p = 5 \times 10^{14} cm^{-3}$). The discrepancy is not too large, especially if one considers that the implied assumption of planarity of the junction and absence of surface channels might not have been fully established.

II.5 Conclusions

The investigation of possible errors inherent in the determination of the diffusion voltage (V_D) by capacitance measurements essentially yielded only an increased value in case of bad contact to the diode. The decrease found in case of the forward biased diode series due to the voltage drop across it is only small because of the opposite effect of the increased effective series resistance. The forward biased diode in series may be a model for a non-ohmic contact to the diode. So no severe effect could be found that would explain a too low measured V_D and hence the doping level N_p. The investigation of the slope K of the $\frac{1}{C^2}$ vs. voltage line led to the conclusion that nonplanarity of the junction or surface inversion layers might increase the effective junction

area. The evaluation of K for the doping level N_p is therefore only possible in the absence of those complicating phenomena. The doping level of Al into silicon for equilibrium alloying should be in the order of 10^{18} to $10^{19} cm^{-3}$, corresponding to V_D = 0.75 v for 10 ohm cm base material. A drop from 0.75 v to about 0.50 v is hard to explain by inherent errors of the experimental procedure with the above analysis in mind. So our conclusion is that either the alloy process is a non-equilibrium one, yielding low doping levels (order $10^{15} cm^{-3}$), or the theory for the capacitance vs. voltage relationship is not adequate. The latter conclusion is supported by measurements on alloyed junction transistors prepared by Hughes which yielded too low V_D values and hence doping levels, despite the rather high current amplification ratio α.

III. ELECTRON LITHOGRAPHY

The conventional method of photochemical etching is to coat the work with Kodak Photo-Resist, place an opaque master pattern in front of it, and expose it to ultraviolet light. The photo-resist becomes polymerized and hardened where the UV strikes it, and cannot be removed by the developer. In this report period work was done on the use of an electron beam to expose and harden the photoresist.

The conventional process with ultraviolet light has the following characteristics, which it was hoped to improve with the electron beam:

(1) The master pattern must be pulled very tightly against the photo-resist in order to obtain good resclution and sharp edges. This is usually done by suction; that is, the master pattern and the coated surface are squeezed together by air pressure when the air between them is pumped out.

(2) A long exposure is required to polymerize the photo-resist, even with a powerful source of ultraviolet such as a mercury arc lamp.

The study showed that the electron beam has several advantages over ultraviolet light. The electron gun comes very close to being a point source of electrons, while a mercury-arc floodlamp is a very broad source of ultraviolet. The pattern therefore does not have to be pulled tight against the photo-resist when an electron beam is used, but can be simply laid on top of the coated surface. Electrons travel in straight lines from the gun, so that a sharp pattern is obtained even if the master is not close to the coated surface. This eliminates one of the problems in the ultraviolet method and at the same time assures that good resolution will be obtained every time.

The exposure time to an electron beam required to polymerize the photo-resist was found to be much shorter than the exposure to ultraviolet. The reasons for this are probably that ultraviolet light sources are not very efficient in producing ultraviolet, and that the electron beam is more effective than ultraviolet light in polymerizing the photo-resist. The result is that the process can be done faster with electron beam exposure than with ultraviolet.

Another point, which was anticipated, became apparent from the study. The photographs in Fig. 12 show the edges of an exposed pattern in the photoresist, in which the exposure was made by ultraviolet in one case (A and C) and by an electron beam in the other case (B and D). The electron beam exposure was for one second at 5 KV and .5 microampere per cm^2. The edge is poorly defined when exposed with ultraviolet. This appears to be due to the scattering or diffusion of ultraviolet light by the photoresist, which causes the light to spread out after it passes through the mask and undercut the desired pattern. The edges thus become tapered and a loss of definition is observed. It appears that the electrons travel in straight lines even through the photoresist, so the edge remains sharp when electron-beam exposure is used. The result of this is that much better resolution is obtained with electron lithography than with ultraviolet lithography.

In order to follow up this finding, masks were ordered with 1 micron to 5 micron holes. The high resolution obtainable with the electron beam should make it possible to produce much smaller patterns in the photoresist than can presently be made. These new masks will be used to demonstrate the feasibility of producing patterns in the micron range with electron lithography.

Fig. 12. Photoresist exposed by UV (A,C) and electron beam (B,D).

IV. PLASMA TORCH FOR SEMICONDUCTOR APPLICATIONS

As commercially available plasma torches are operating at rather high powers (10 K watts) and large diameters, it was decided to construct a scaled down plasma torch for low energy metal ion generation feasible for semiconductor applications. This torch has already been fabricated, a technical drawing is shown in Fig. 13 and a photograph of the device in Fig. 14. Upon completion of power, gas, and water feeds, experiments will be carried out to determine first, the feasibility of scaled down operation of plasma torch in the 100 to 500 watt range, and secondly, the rate of metal deposition of suitable metals and alloys for diode application at this level of operation.

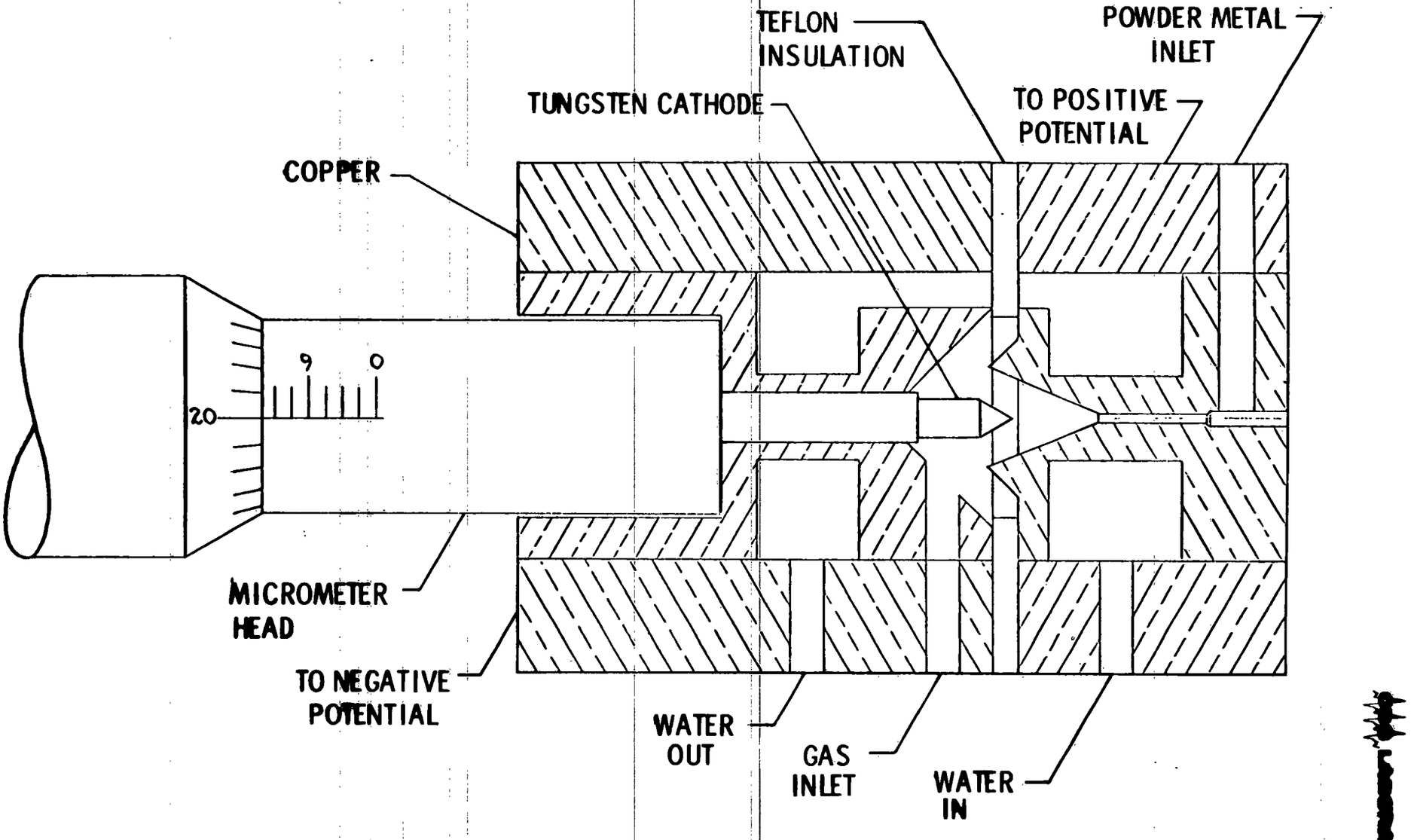
The sketch and photograph (Fig. 13 and 14) show the physical configuration of the miniaturized plasma torch.

This version of the torch was simplified to its essentials with only one mechanical variable for striking and adjusting the arc by means of the micrometer head which controls the cathode to anode spacing.

Principally, the operation of the plasma gun depends on the axial flow of gas through the dc arc region and emerging as a jet of high temperature plasma.

The gas enters the arc chamber at slightly more than atmospheric pressure and escapes through the torch nozzle opening. The gas or gas mixtures should be inert and of low atomic mass, and preferably non-reacting with the metals used in the arc region.

The cooling of the torch is provided for by ordinary tap water circulation.



PLASMA FLAME TORCH
FIG. 13

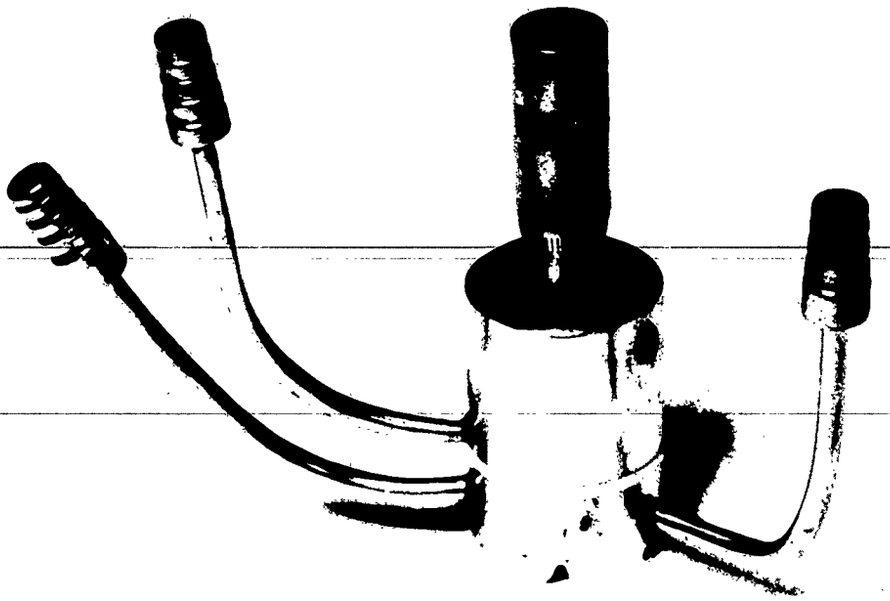


Fig. 14 Photograph of scaled down plasma torch with feed throughs for gas, water and metal vapor.

V. PLANS FOR THE NEXT PERIOD

In the following quarter, main emphasis will be placed on the operation of the scaled down plasma torch. The feasibility of the cleaning and alloying capabilities of the torch for semiconductor device fabrication will be investigated. In addition, work on electron beam lithography of semiconductors aimed at control over dimensions in the micron range will continue.

VI. APPENDIX: SUMMARY OF ELECTRON BEAM WORK ON SILICON

VI.1 Experimental Results

a. Ohmic Contacts

Ohmic contacts to silicon were made by bombarding the silicon with electrons and simultaneously evaporating a metal film onto the surface. Ohmic contacts were successfully made with aluminum, tin, gold, and silver. Both n-type and p-type silicon were used.

Adherent films of metal were evaporated onto silicon to yield ohmic contacts provided that the surface was bombarded with electrons during deposition. Adherent, ohmic contacts could not be formed without electron beam cleaning of the silicon surface during evaporation of the metal.

b. Welded Wires

Wires were welded directly to a silicon wafer with the electron beam to demonstrate the feasibility of a new method of attaching leads to semiconductors as a potential alternative to thermocompression bonding. Wires of gold, silver, aluminum, and nickel were successfully welded to silicon with the beam.

c. Machining of Silicon

With a high-power electron-beam (voltage 15 KV, current 200 μa, diameter $\approx$ 0.02") it was possible to machine grooves into the silicon surface of a 0.025" thick sample to a depth of about 0.0005". At still higher powers (30 KV, 200 μa, $\approx$ 0.02" diameter) holes could be drilled in a 0.007" thick wafer.

d. Alloyed Diodes

Aluminum films were evaporated onto n-type silicon and were then alloyed into the surface by an electron beam. Film thickness was investigated in the range from 0.1 to 1 μ. Good rectifying junctions were made on 10 ohm.cm silicon; these had reverse leakages of less than 5 microamperes at 100 volts. These low leakages proved that really a p-n junction was formed because a mere surface barrier usually shows high reverse leakage currents (see e.g. Transistor Technology, Vol. 3, D. van Nostrand Co., Princeton, N.J., 1958, pg. 220). Anglelapping and staining techniques also proved the formation of p recrystalized region. Capacitance vs. voltage measurements on these diodes showed them to be step junctions, which proves that they were true alloyed junctions and not the result of surface impurity diffusion.

VI.2 Conclusions From the Study

The study proved the feasibility of the electron beam technique for cleaning a semiconductor surface, such as silicon, which is one of the most essential conditions for proving a suitable metal to silicon interface for the fabrication of ohmic contacts or alloyed p-n junctions. This new cleaning technique was first proposed by Jacobs, et al.[2] During the investigation it became apparent that the most satisfying results are obtained by simultaneously bombarding the silicon surface with electrons and evaporating the metal layer onto it. This is explained by the fact that a completely clean surface is maintained only for a very short time even in high vacuum. The first atomic layer of contamination for instance, in a vacuum of 10^{-6} mm Hg is formed in a couple of seconds.

The use of the electron beam as a heating source to form alloyed p-n junctions, as it was proposed first by Shockley[3], was also found feasible during this study. But on the other hand, with the rather rough electron gun machine available for this project, it was not possible to demonstrate impurity diffusion induced by an electron beam, also suggested first by Shockley[3], in order to form p-n junctions. For this purpose long heating times (in order of hours) are needed, during which the electron beam operation has to be stable, so that a sophisticated electron beam control becomes necessary. The sputtering effects of the beam which were also found during these experiments may raise some difficulties in achieving diffusion because of a too fast removal of the surface impurity layer. But with better beam control one should be able to minimize these effects. The main problems that arose during the study of forming alloyed p-n junctions with Al and n-type Si were: (1) Achieving planarity of the junctions which was found to be necessary in obtaining low reverse leakages was combined with difficulties. The non-planarity of junctions that occurred especially with lower resistivity, 1 ohm.cm n-type silicon is explained by an insufficient clean surface before Al evaporation and/or imperfection in the polished silicon

2. H. Jacobs, J. Leibowitz, and A. Ramsa, U.S. Patent No. 2,803,569, "Formation of Junctions in Semiconductors", August 20, 1957.

3. W. Shockley, U.S. Patent No. 2,816,847, "Method of Fabricating Semiconductor Signal Translating Devices", December 17, 1957.

surface itself. So the melted Al accumulated at different spots on the surface during alloying and caused a non-planar solution of Si. Also the thickness of the Al layer may have an influence on this phenomenon. The fact that the electron beam technique itself was not responsible for the non-uniformity of the achieved junctions is proven by the good results obtained with the 10 ohm.cm silicon. But the indicated difficulties show that a perfect and clean surface is much more important for the electron beam alloying than it is for the conventional method. The reason for this is believed to be represented by the comparatively fast heating and recrystallization cycles created by the electron beam so that non-equilibrium conditions prevail.

(2) A control over small dimensions was not possible. This is mainly due to the badly controllable simple electron gun machine provided for the investigation. The attempt to achieve spot alloying by bombarding the silicon sample through masks proved to be unsatisfactory because the whole temperature pattern on the sample apparently was influenced by the heated and consequently radiating mask. A better control of the sample temperature pattern by providing a defined substrate temperature for the sample also did not succeed in the expected degree. This was due especially to bad heat contact between sample and substrate that apparently changed from sample to sample, and also, because of the low power output of the electron gun, to the impossibility of operating the substrate at low temperatures which is necessary for obtaining steep temperature gradients in the sample.

(3) Evaluation of the Al doping levels in the regrowth layer indicated very low values. This fact could be explained in terms of non-equilibrium regrowth caused by the short heating up and cooling down times as created by the electron beam technique. On the other hand, the built-in voltage measurement method used for evaluating the doping level yielded low results also for conventionally alloyed junctions. An analysis of the experimental method of determining built-in voltages revealed no serious errors adherent to the procedure which led us to the conclusion that the theoretical formulae of the capacitance-voltage relationship for an abrupt pn junction are not adequate for calculating the doping level. It should be stated, however, that the saturation doping level, as it is obtained by equilibrium alloying or as it is represented by the surface concentration in the diffusion technique with infinite impurity source, cannot be surmounted by any means. This is concluded from theoretical considerations of the metallurgy of binary systems governed by the phase diagram. An increase in the doping level by the electron beam technique, as it was expected at the beginning of the research work, therefore, is not possible.

AD CBS Laboratories, Stamford, Connecticut Study of Microjunction Formation Technology by A. Ramsa and R. Engelmann, Report for October, 1961 through December, 1961, Dated 8, February 1962. 39 pp. including illus. (Contract DA 36-039 SC- 88900) Unclassified. An investigation of the experimental method of determining the built-in voltage of abrupt pn junctions by capacitance vs. voltage measurements is given and possible errors are discussed. Preliminary results on the lithographic use of the electron beam for fabricating semiconductor devices are presented.	UNCLASSIFIED 1. Electron and ion beam technology 2. Semiconductors - technology 3. P-n junctions - devices I. Ramsa, A and Engelman, R. II. U.S. Army Signal Research & Development Laboratory III. Contract DA-36-039 SC 88900 UNCLASSIFIED

AD A scaled down plasma torch for semiconductor applications is described. The report closes with a summary and discussion of the electron beam work performed under this contract.	UNCLASSIFIED UNITERMS Microjunction Formation Technology Built-in Voltage P-N junction Capacitance Lithographic Electron Beam Plasma Torch Semiconductor UNCLASSIFIED

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