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# PROJECT LIGHTNING

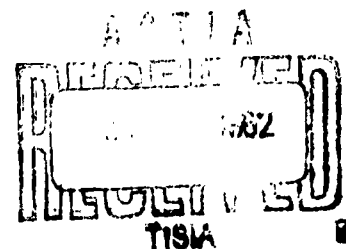
*Third Phase*

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## FIFTH QUARTERLY PROGRESS REPORT

VOLUME I

NObsr 77521



RE M I N G T O N R A N D  
**UNIVAC**  
DIVISION OF SPERRY RAND CORPORATION

PROJECT LIGHTNING  
THIRD PHASE  
NObsr 77521

FIFTH  
QUARTERLY REPORT  
VOLUME I

This report covers the period from  
1 June 1961 to 31 August 1961

PX 1599-5

***Remington Rand Univac***<sup>®</sup>

DIVISION OF SPERRY RAND CORPORATION

UNIVAC PARK, ST. PAUL 16, MINNESOTA

## INTRODUCTION

Project Lightning was established at the Sperry Rand Corporation in June, 1957, under Contract NObsr 72728. This project has performed research to indicate the feasibility of and to serve as the basis for the evolution of an ultrahigh-speed data-processing system. Several divisions of the Corporation have carried out the project work in geographically separated laboratories to make the best use of personnel and facilities.

For some time prior to this Contract, the St. Paul Laboratory had been investigating the possibility of using vacuum-deposited uniaxially-anisotropic ferromagnetic film elements for the development of computer components. Project Lightning has continued this work, emphasizing the development of rapid-access memories and arrays of film-core elements whose states may be switched rapidly at low power for logical operations.

In the Third Phase of Project Lightning, beginning in June, 1960, Remington Rand Univac proposed to design, construct, and test a Lightning Test Machine. This machine is expected to demonstrate the feasibility of operating magnetic film search memories and shift matrices under controlled conditions so that their capability may be evaluated. Remington Rand Univac also proposed to continue research efforts to improve the preparation of magnetic film elements and the measurement of their properties. Also to be continued is investigation of the application of magnetic film elements in search memories and shift matrices as well as in other devices which might also contribute to the development of ultrahigh-speed data-processors. Mathematical and logical research will continue, particularly with respect to majority-decision logic and systems organization.

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## ABSTRACT

### 1. SEARCH MEMORY

This report describes the following aspects of the search memory as it is now planned. Detailed descriptions are given of the physical arrangement including d-c bias windings, the read driver, the sense amplifier, the digit write, the word write, and the search memory test system.

### 2. JDU CLOCKING

Results obtained in the June Demonstration Unit (JDU) with the circuits described in the previous quarterly report are covered in this report. During the checkout period the memory start pulser has been operating at about 3 Mc, and the four-phase logic clock at 10 Mc. Waveforms at key points in the clocking circuits are presented. It appears that the response of the delay lines used is the limiting factor in the higher frequency operation of the logic clock.

### 3. POWER SUPPLY SYSTEM FOR THE JDU

In the power supply system for the JDU individual regulation and adjustment of all voltages for logic and memory was considered advisable. Since the last report some changes have been made in the higher current regulators. Those changes involve current limiting, voltage control, and heat sink. Results of initial tests of the power supply system are given. Further power supply tests will be made after checkout of logic and memory has been completed.

### 4. PACKAGING

Assembly of the JDU has been completed. This unit includes approximately 275 circuit modules, six interconnection multilayer modules, power supply regulators, and a cabinet. Logic checkout has been completed and test work is proceeding. Principal errors encountered during checkout are shorts and opens. Such shorts and opens were

repaired by using twisted pair wiring. Flow solder techniques will replace hand soldering in LTM construction. Four identical 256-word memory modules are planned for the LTM. These individually pluggable units will be individually cooled. Memory circuits will be isolated from noise generated by the logic circuitry. Circuit model layouts for LTM logic have been started.

#### 5. JDU LOGIC MODULE TEST

Results of JDU logic module tests are given. Average rise, fall, and delay times are within limits specified for the JDU.

#### 6. FILM SPOT OUTPUT SIGNAL

This report contains data obtained in an attempt to correlate an optimum signal output from thin film spots for various reasonable word drives and film spot thicknesses. A single-bit system was used for the basic driver and amplifier requirements. It appears that although the output signal from thinner films is greater at low currents, more signal is obtained from the thicker films at a reasonable (400 to 500 ma) word drive. A film spot thickness of 1000 to 1500 A and a word drive of 400 to 500 ma should provide a usable signal.

#### 7. INPUT-OUTPUT EQUIPMENT FOR THE LTM

Input-output equipment for the LTM will consist of a photoelectric tape reader and a paper tape perforator, together with the necessary logic and control. The transistorized tape reader will operate at a reading speed of 60 characters per second. The high-speed tape punch will operate at 110 characters per second. Logic and control of the external equipment will require about 300 circuit cards.

#### 8. PHILADELPHIA PROGRESS REPORT.

This report describes the design of a thin-film memory read amplifier, a test of machine clock design, and a study of tunnel diode logic circuits.

## DETAILED DATA

### 1. SEARCH MEMORY

a. **PHYSICAL ARRANGEMENT.** The basic memory cell of the search memory will be 0.035 inch in diameter and spaced at 70-millinch intervals in both directions. The end terminations may be staggered slightly to be compatible with a 0.1-inch grid. The digit and word lines will follow the same basic pattern being used in other NDRO memories. Basically, 256 x 48 cells are required to make the 128-word, 24-digit search memory. The printed wiring overlay must be made in four pieces. It is planned that the assembly will be essentially in two layers (i.e., each layer will be 48 x 128 cells). Without end terminations, each layer will be 3.4 inches x 9 inches. A schematic side view of the digit winding is shown in Figure 1.

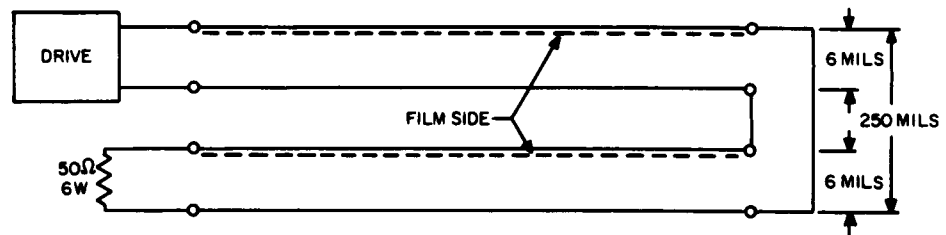


Figure 1. Digit Winding, Side View

Film substrates will be 6 millinches thick. The separation between layers will be perhaps 0.25 inch. Digit lines are spaced at 70 millinches. Twenty-four "1" lines and twenty-four "0" lines are required.

Initially the optimistic view is assumed that 24 digits can be sensed correctly with one sense amplifier. If a split-up of the word line is required, it will be necessary to make two 24 x 256 cell arrays rather than one 48 x 256 cell array. In either case, the sense line will be at 0.14-inch intervals with one of the following arrangements (Figure 2). In the optimistic case there will be 64 sense amplifiers for each of the two layers.

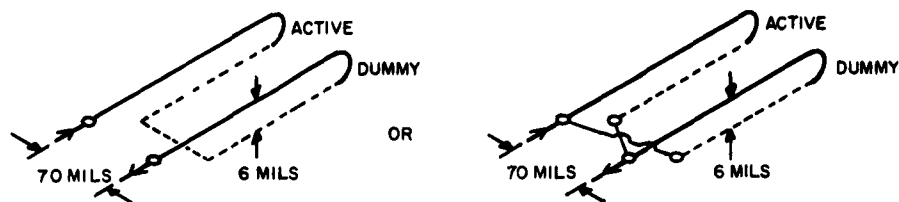


Figure 2. Possible Sense Line Arrangements

Two d-c bias windings at right angles will be provided to surround the two layers of memory. The windings might be 0.08-inch strip lines at 0.1-inch intervals, series-connected top-to-bottom and bottom-to-top to form one complete turn every 0.1 inch.

The bias "windings" should be separated from the main digit and word lines by perhaps 0.1 inch or more and extend beyond the edge of the films by an inch or more. The lines will provide: 1) a transverse d-c field for read, 2) a longitudinal erase field to bias all cells to produce a small output, and 3) a d-c longitudinal field to aid in writing. The currents into the two windings will be equal or nearly equal in magnitude.

b. READ DRIVER. The current read driver (Figure 3) is essentially a JDU word driver driving into a grounded base 2N1509. The maximum duty cycle on any one driver will be about 30 percent. The maximum average dissipation of the 2N1509 will be about 0.9 watt so that very little additional heat sinking will be required. The read drive will require 48 read drivers. Half of these drivers will be pulsed every time the search memory is referenced. The read pulse will be about 20 nsec long. The enable to the driver will be provided from a flip-flop register. Measurements indicate that the optimum drive for best large-to-small output signal ratio is with a 1.5-oe transverse field and about 550 ma of read current. However, this may not turn out to be optimum when the noise introduced by the 24 digit drivers is added. The trend in this case would be for lower pulsed longitudinal drive and higher d-c transverse field. Final determination will be made when 24 digit drivers have been built and tested on the array. If the digit drive requirement goes down, a simpler drive will be possible.

The read operation will apply a 20-nsec read pulse to the 48 digit drivers. Half of the digit drivers will be enabled from the 24 digit information registers.

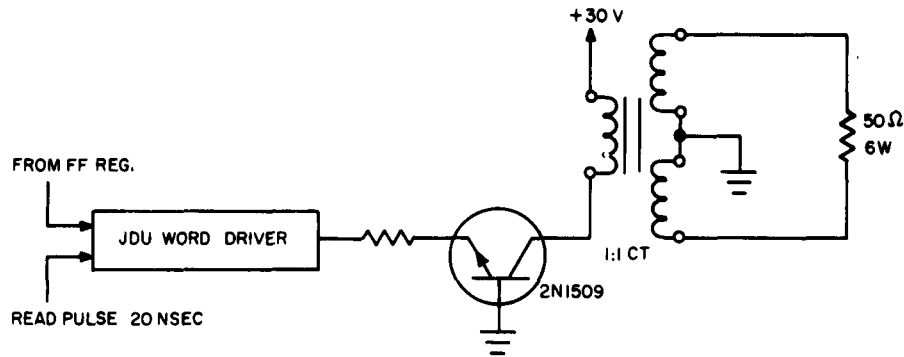


Figure 3. Read Driver

It is assumed that if the strobe pulse arrives at all the sense amplifier outputs simultaneously, a strobe pulse of 28-nsec duration will be required when these conditions obtain:

Driver delay	5 to 11
Sense amp delay	7 to 13
Digit line delay	0 to 6
	12 to 30.

The strobe pulse should appear about 12 nsec after application of the read pulse to the driver. This will allow about 70 nsec for recovery after terminating the strobe pulse.

c. **SENSE AMPLIFIER.** The sense amplifier will have about the same complexity as the DRO sense amplifier except that only one-output polarity will be required. A very good common-mode rejection is required since 24 drivers are turned on simultaneously. The sense amplifier must be capable of providing a logic level output for a unit signal and still recover from 24 times a unit signal to permit 10-Mc operation. The rise time requirements for the search sense amplifier need not be as good as those for the DRO sense amplifier. A rise time of 10 nsec will probably be satisfactory. It may be necessary to split the word lines (short lines) into two parts, in which case twice as many (256) sense amplifiers would be required.

The sense lines will be spaced at 0.14-inch intervals. One of the following schemes will be used for connecting the active and dummy sense lines (Figure 4).



Figure 4. Possible Connections for Active and Dummy Sense Lines

The active and dummy sense lines are on 70-millinch centers. The total delay through the sense line for case A will be less than 2 nsec, permitting a heavily loaded sense line. Case B in effect does provide heavy loading of the sense line at the expense of losing 50 percent of the signal. The d-c resistance of the sense line in case B must be high enough so that only a small counter field is set up by current flow in the sense line. If a unit signal is 5 mv and the sense line has 0.5-ohm resistance, 10 ma of current will flow in the sense line. This amount (about 2 percent of the 500-ma drive) is negligible.

d. **DIGIT WRITE.** Forty-eight digit writers will be required. Many possibilities exist for writing. It is proposed that a large longitudinal field be applied first via the bias windings to put the memory cells all into the small signal state. This can be accomplished with a field of 42 oe or more.

The next step would be to alter selectively one-fourth of the cells to produce a large output. It is further planned to use a d-c field via the bias windings or cube coil of 14 oe in the direction to produce a small output. For each digit pulsed, a field of 28 oe (about 2 amp) will be applied to the "1" line if a "0" is to be stored, or to the "0" line if a "1" is to be stored. This field will be in the direction to produce a large output. If no word drive is applied, the net field will be 14 oe (insufficient to write). The word drive will also produce a field of 28 oe in the direction to produce a large signal on the active line but in the direction to produce a small signal on the dummy line. The total field where there is word current will be only 14 oe. The total field when there are both digit and word write currents will be  $28 + 28 - 14 = 42$  oe.

With this procedure it will be necessary to rewrite the whole 128 words if rewrite is required.

The digit write might be accomplished in the following manner (Figure 5).

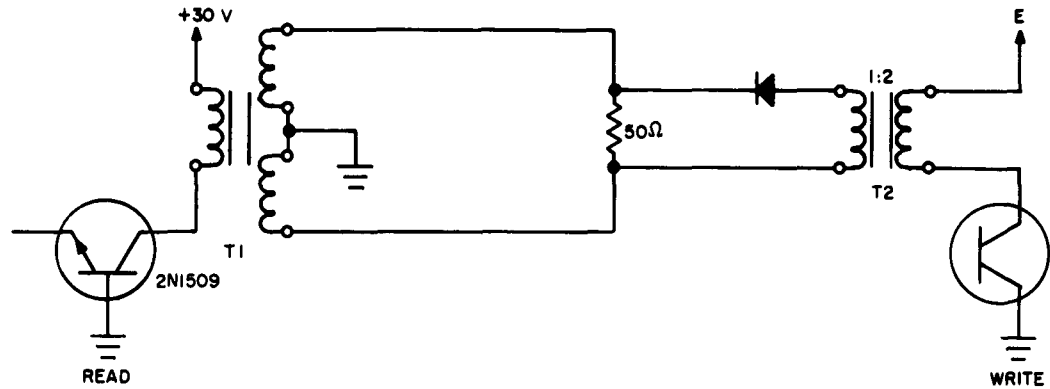


Figure 5. Digit Write

The inductance of T1 should not be greater than  $20 \mu\text{h}$ . With a 2-amp pulse having a  $2\text{-}\mu\text{sec}$  rise, the  $L \frac{di}{dt}$  drop would be 20 volts. If transformer T2 has a current step-up of 2, the supply for the write transistor would have to be 40 volts or more. A write pulse having a  $2\text{-}\mu\text{sec}$  rise,  $2\text{-}\mu\text{sec}$  flat, and a  $2\text{-}\mu\text{sec}$  fall is planned. The maximum frequency of writing will be 40 kc. The diode shown is intended to reduce the capacitive loading on the terminating resistor. Two to four 1N920 diodes in parallel might be suitable.

The logical arrangement for digit read and write is shown in Figure 6.

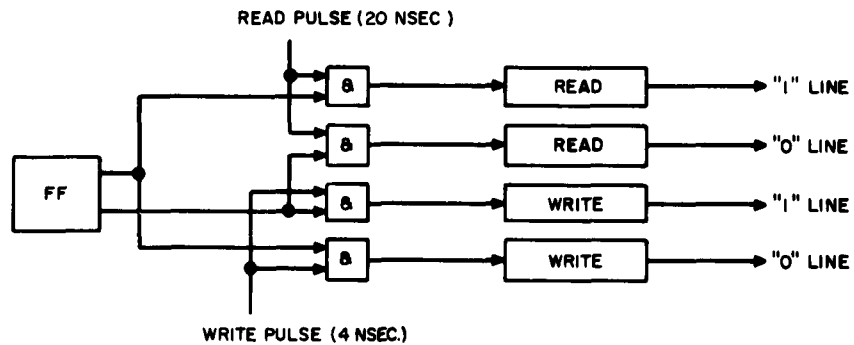


Figure 6. Digit Read and Write

e. **WORD WRITE.** The word write (Figure 7) will consist of an  $8 \times 16$  selection matrix, a transformer, and a diode per word. In one way the word write will be easier than the digit write because the drive will be a shorted line.

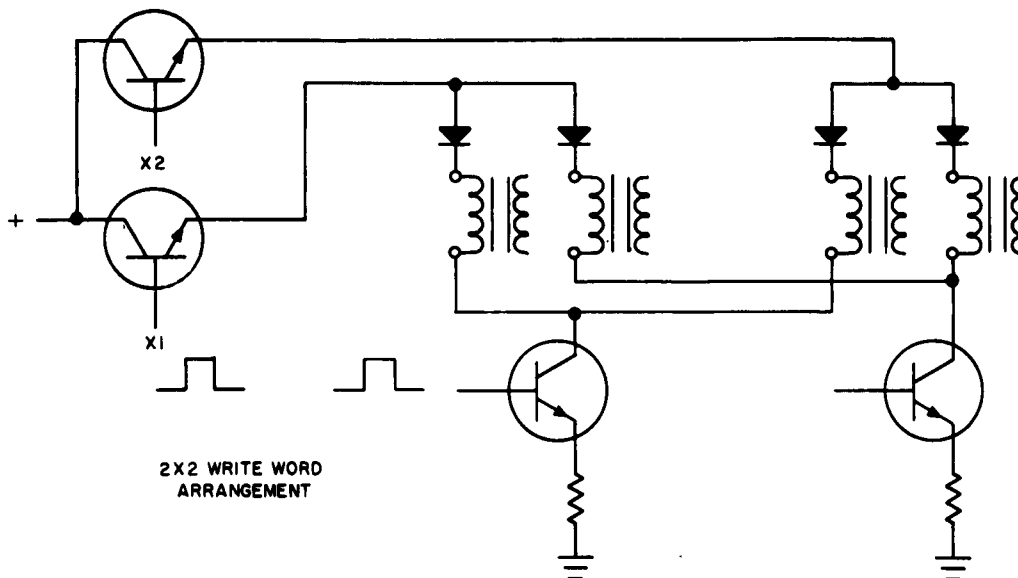


Figure 7. Word Write

The arrangement shown will be expanded to 8 x 16. The transformer will be tied into the word lines at the sense amplifier input terminals. If sense line arrangement A is used, the transformer output will be 2 amp and about 1.4 volts. If arrangement B is used, the current required will be 4 amp and 0.7 volt. A 5:1 transformer for case A or a 10:1 transformer for case B would result in about 10 volts across the primary and about 400 ma of current. The word pulse should coincide with the digit pulse.

This is the writing sequence:

- 1) Turn off d-c transverse field of 1 to 3 oe.
- 2) Erase with d-c longitudinal field of 42 oe.
- 3) Set up 14-oe d-c field in erase direction.
- 4) Write all words with 6- $\mu$ sec write pulse at maximum 40-kc rate. Pulse digit write and word write at the same time.
- 5) After completion of writing, remove longitudinal bias and restore transverse bias.

f. SEARCH MEMORY TEST SYSTEM. Previous quarterly reports specified that the NDRO search memory in the Lightning Test Machine (LTM) would contain a complement and non-complement memory consisting of 48 digit lines and 256 word lines. During

a readout operation 24 of the 48 digit lines are always activated simultaneously, while two interconnected words lines are sensed.

Simulation of the actual signal-noise conditions has been accomplished through a test system with 24 read drivers and a sense amplifier. Each digit line is terminated in its characteristic impedance of 50 ohms simulating long digit lines. A twisted pair transformer with a 1:1 turns ratio couples each read driver to its digit line and isolates the line from ground for common-mode signal balance. These transformers are wound to give a 30 percent flyback to restore the permalloy film of the BICORE film element fully in 100 nsec.

Each BICORE film element receives a longitudinal field contribution from the digit line over the top of the BICORE film element and from the return line below the film. This longitudinal field is applied during both read and write time.

The word line also produces a longitudinal field from above and below the BICORE film element but only during write time. The word line is used for sensing during a readout.

A third line was added to the array to produce a transverse field from above the film during a readout. A 1.0-amp current was required in each transverse line. This current can be reduced by using a return line below the film.

Figure 8 illustrates the circuit used in the test system. "Write in" was accomplished by using 3-amp direct current in the digit lines to write all cobalt films to "0's." An SKL pulse generator was used on the word line producing a 3-amp pulse to write the active films to "1's" while at the same time writing the dummy films to "0's." The LTM will use coincident write pulses on the digit and word lines to write a particular film to a "1." Experimental tests proved a minimum current of 2.9 amp necessary in either the word or digit line to switch the cobalt film completely. Correspondingly, a maximum current of 1 amp is allowed in either digit or word lines to leave each film element undisturbed in its "0" or "1" state.

Dotted lines shown in Figure 8 represent the return lines below the films. Two word lines are interconnected opposing for each sense amplifier. Connections are made in this manner so that capacitive coupled digit noises cancel. The series transformer in the sense line is an 18-turn twisted pair wound on an "H" material toroid. This transformer was used to balance common-mode signals. The 100-ohm variable resistor terminating the sense line compensates for any physical unbalance of the word lines.

The sense amplifier input transformer is a 1:4 voltage step-up twisted pair. This transformer was wound on a "T1" toroid with a 3-turn primary and 12-turn secondary.

Switches were provided to take the sense amplifier out of the circuit during write time and to take write circuits out during read time.

Three stages of amplification were used in the sense amplifier with only the first stage illustrated in Figure 8. An approximate gain of 6 is obtained from each stage.

Digit read pulses measured 30 nsec in width. Signal outputs for twelve "0's" and one "1" were plotted as digit read current was varied in amplitude. Figure 9 shows the optimum "1"/"0" ratio obtained when using a 300-ma read pulse.

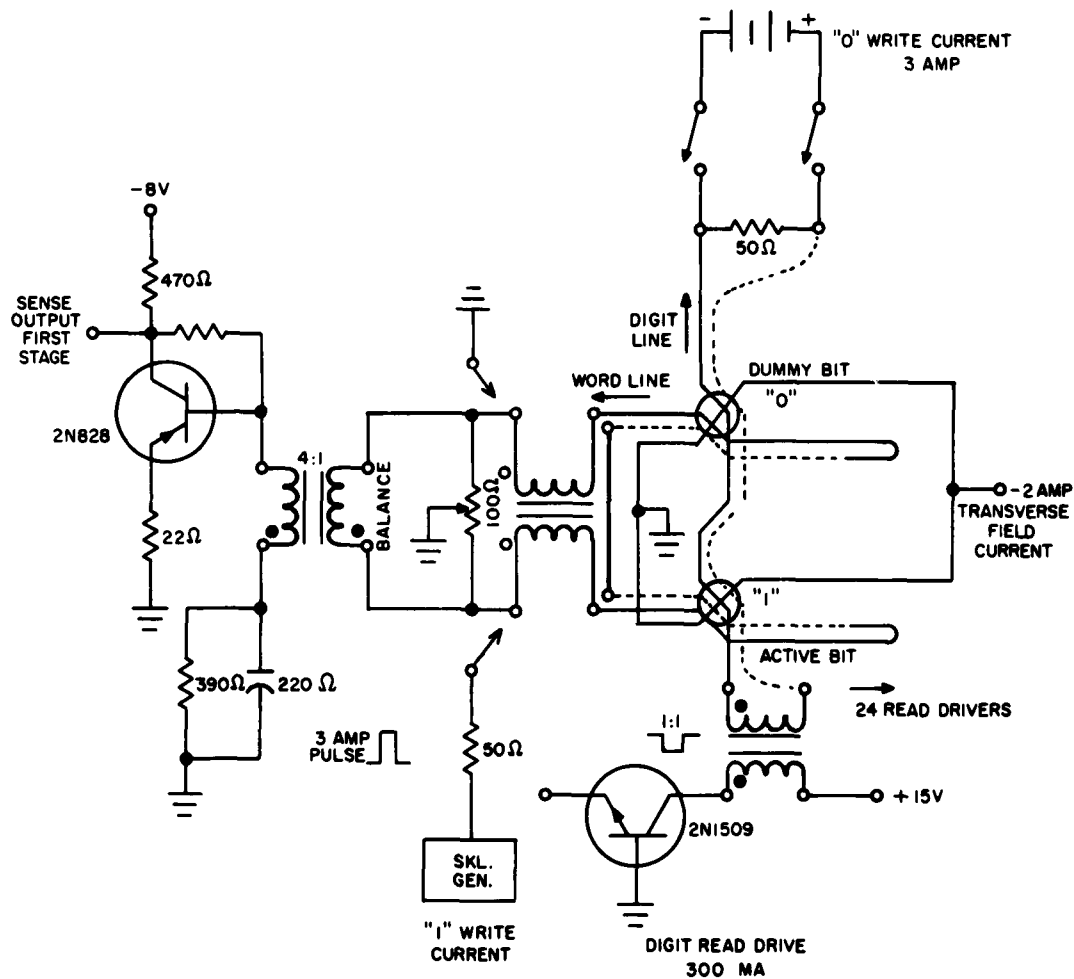


Figure 8. Search Memory Test System

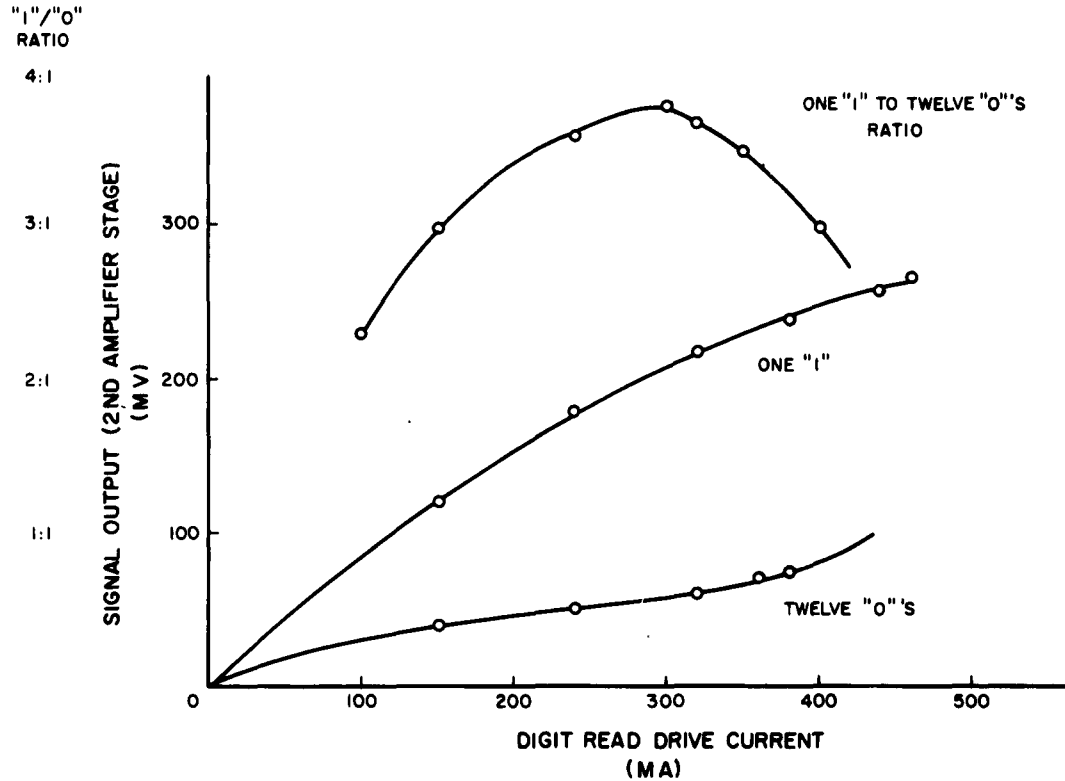


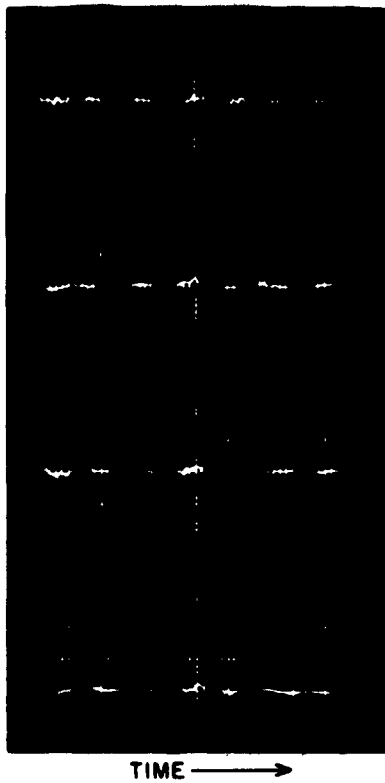
Figure 9. Signal Output versus Read Current

Figure 10 waveforms represent worst case conditions comparing signal-to-noise ratio when reading out 24 "0's" in (a) and (b) or when reading out 23 "0's" with one "1" in (c) and (d). A good signal-to-noise ratio was achieved which proves the feasibility of the search memory mode of operation.

## 2. JDU CLOCKING

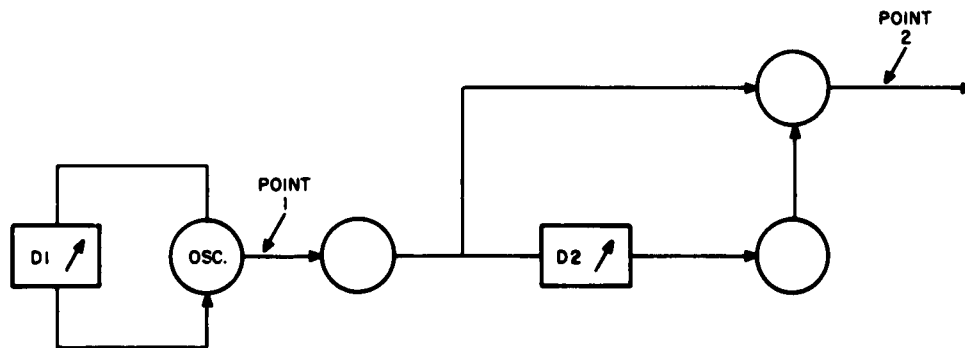
This report covers the results obtained in the June Demonstration Unit (JDU) with the memory start pulser and the four-phase logic clock circuits described in the previous quarterly report.

a. MEMORY START PULSER. Figure 11 is a block diagram of the memory start pulser as it appeared in the previous quarterly report. The pulser was designed to produce negative pulses varying between 3 and 15 Mc. The pulser is now operating at the 3-Mc rate, cycling memory every 350 nsec.



- (a) Twenty-Four "0's"  
(Output of First Amplifier Stage)  
Vertical Calibration: 100 mv/div  
Horizontal Calibration: 50 nsec/div
- (b) Twenty-Four "0's" (Output of Third Amplifier Stage)  
Vertical Calibration: 1 volt/div  
Horizontal Calibration: 50 nsec/div
- (c) Twenty-Three "0's" with One "1" (Output of First Amplifier Stage)  
Vertical Calibration: 100 mv/div  
Horizontal Calibration: 50 nsec/div
- (d) Twenty-Three "0's" with One "1" (Output of Third Amplifier Stage)  
Vertical Calibration: 1 volt/div  
Horizontal Calibration: 50 nsec/div

Figure 10. "1" and "0" Outputs of Search Memory Test System



NOTES:

- = Logic Card ( $\overline{OR}$  inverter).  
D1 = 0- to 200-nsec delay.  
D2 = 0- to 50-nsec delay.

Figure 11. Memory Start Pulser

Reproductions of waveforms at key points appear in Figure 12a and b. The oscillator waveform at point 1 appears in Figure 12a, showing the square wave output at about 3 Mc. The resultant output pulses at point 2, occurring every 350 nsec, are in Figure 12b. The waveforms appear fuzzy mainly because of poor grounding of the Hewlett-Packard sampling oscilloscope used. Noise in the system also contributes to the fuzz at the steady state levels. The output pulse is about 50 nsec wide, with rise and fall times of about 3 nsec. The output supplies two logic loads.

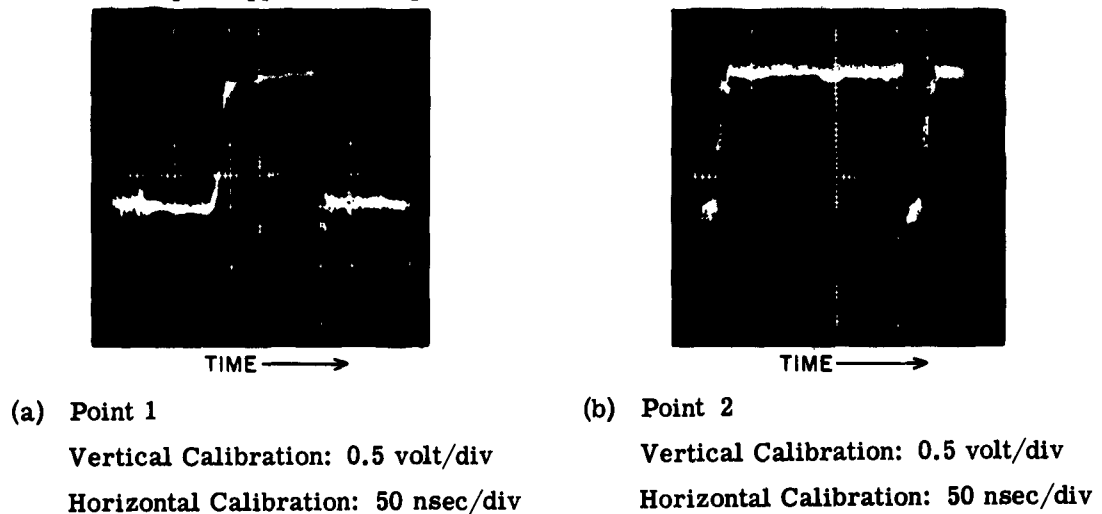


Figure 12. Memory Start Pulser Waveforms

b. **FOUR-PHASE LOGIC CLOCK.** The four-phase logic clock was designed to operate between 10 and 15 Mc mainly as a logic clocking device used in conjunction with the memory start pulser. During the checkout period in the JDU, the clock frequency has been held at the 10-Mc rate.

Figure 13 is a block diagram of the logic clock with key points numbered to correspond with the waveforms of Figure 14. Figure 14c shows the waveform from the delay line oscillator. The steady state levels indicate a mismatch in impedance levels between the transmission lines, logic card, and the delay line. The reshaped signal at point 4 appears in Figure 14b. The signal at point 4 is delayed and inverted, then ANDed with the original signal to produce negative pulses at point 5. These negative pulses are progressively delayed and inverted to produce the four phases at the output points 9 to 12. Waveforms at the key points appear in Figure 14. All output phases have two logic loads except phase 2, which has four. The waveforms of the output phases, Figure 14 g to j show positive pulses occurring every 100 nsec, with a pulse duration at the base of about

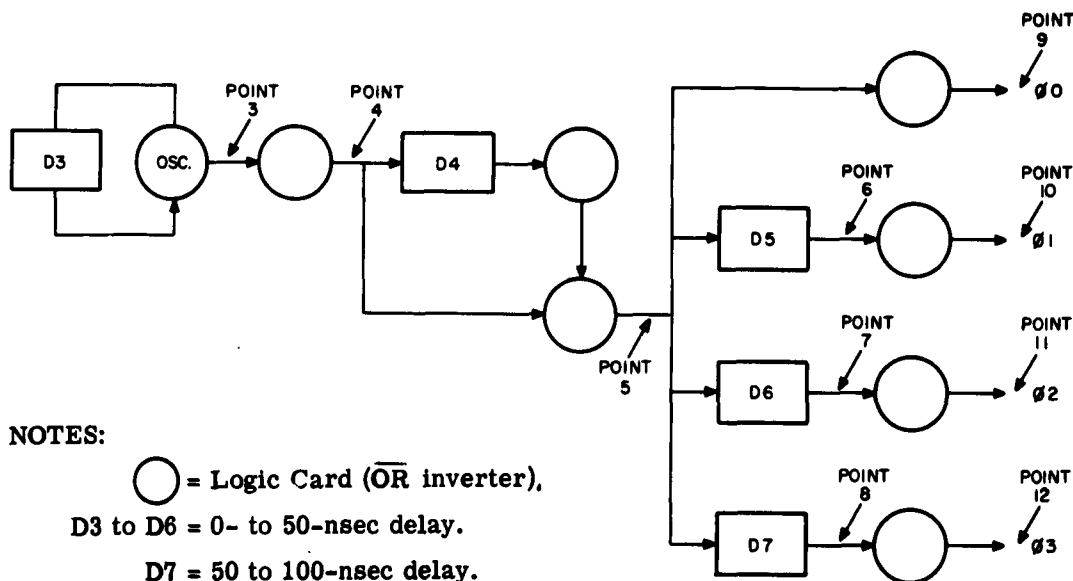


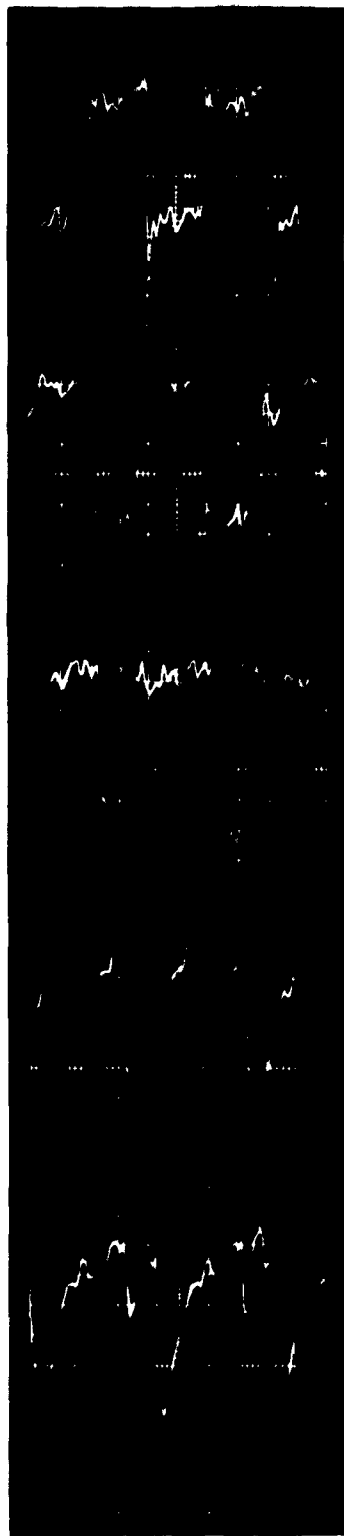
Figure 13. JDU Four-Phase Master Clock

25 nsec. Observed rise and fall times are on the order of 4 nsec. Phase 2, having four loads, has a slightly sloping rise time caused by additional shunt capacity loading. Logic thresholds are reached before this sloping occurs, thus causing no harm.

The delay lines being used are the distributed constant type with the coil wound on metallized glass forms with 40 longitudinal lines for the ground plane. Delay lines were designed in 50-nsec sections and can be either fixed or variable over this range. The delay-to-rise-time ratio observed is about 6 for a 50-nsec section. As observed in Figure 14 d to f, there is a mismatch of impedance levels between the delay lines and the transmission lines. When properly matched, these reflections do not occur. It appears that the response of the delay lines is the limiting factor in the higher frequency operation of the logic clock.

### 3. POWER SUPPLY SYSTEM FOR THE JDU

a. GENERAL SYSTEM. The power supply system for the June Demonstration Unit (JDU) is illustrated in Figure 15. Individual regulation and adjustment of all voltages for logic and memory was considered advisable. The ground planes of the computer interconnection modules were used as the central ground for all power supplies



(a) Logic Clock, Point 4

(f) Logic Clock, Point 8  
 $\phi_3$ , Input

(b) Logic Clock, Point 3

(g) Logic Clock, Point 9  
 $\phi_0$ , Output

(c) Logic Clock, Point 5  
 $\phi_0$ , Input

(h) Logic Clock, Point 10  
 $\phi_1$ , Output

(d) Logic Clock, Point 6  
 $\phi_1$ , Input

(i) Logic Clock, Point 11  
 $\phi_2$ , Output

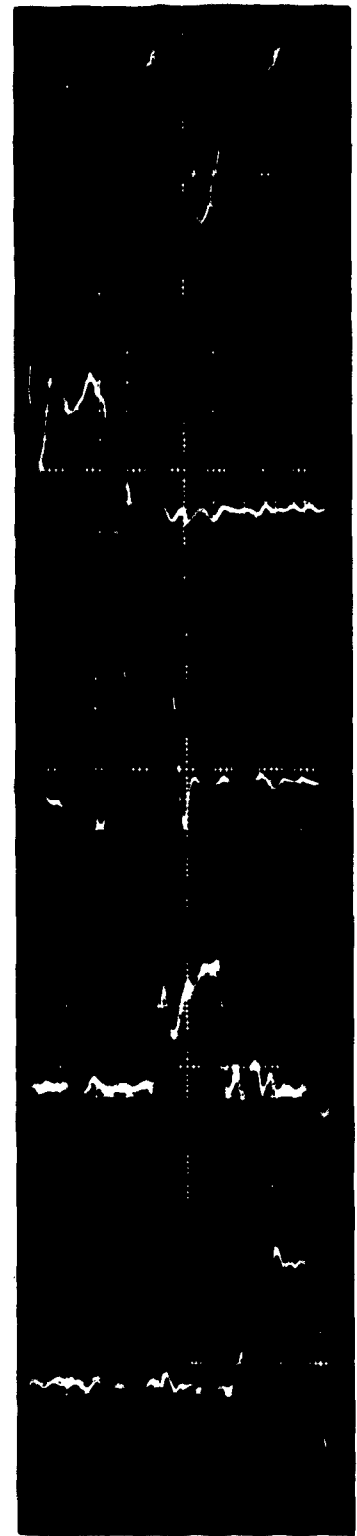
(e) Logic Clock, Point 7  
 $\phi_2$ , Input

(j) Logic Clock, Point 12  
 $\phi_3$ , Output

TIME →

Vertical Calibration: 0.5 volt/div

Horizontal Calibration: (a) to (f), 25 nsec/div; (g) to (j), 10 nsec/div



TIME →

Figure 14. Waveforms, Four-Phase Logic Clock

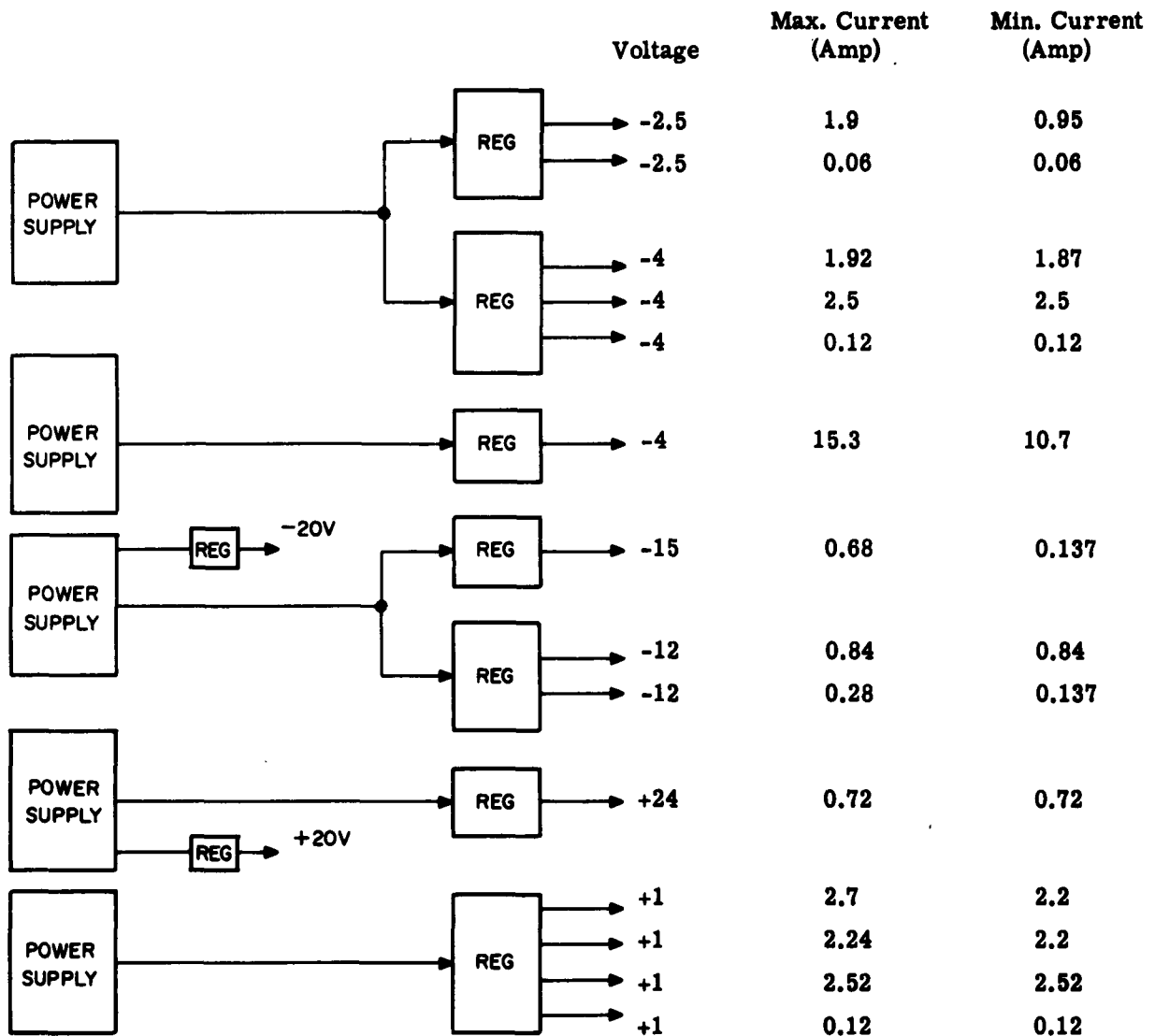


Figure 15. Regulator and Power Supply Layout

and regulators. Ground wires from each power supply and from the sense circuit of each regulator were terminated at the computer ground planes.

b. **POWER SUPPLY REGULATORS.** Some changes have been made in the higher current regulators since the last report. Changes were made in current limiting, voltage control, and heat sink. Figure 16 shows a typical voltage regulator.

The method for current limiting the regulators has not changed greatly. The chief difference is that a transistor is used instead of a diode. The current is cut off faster at

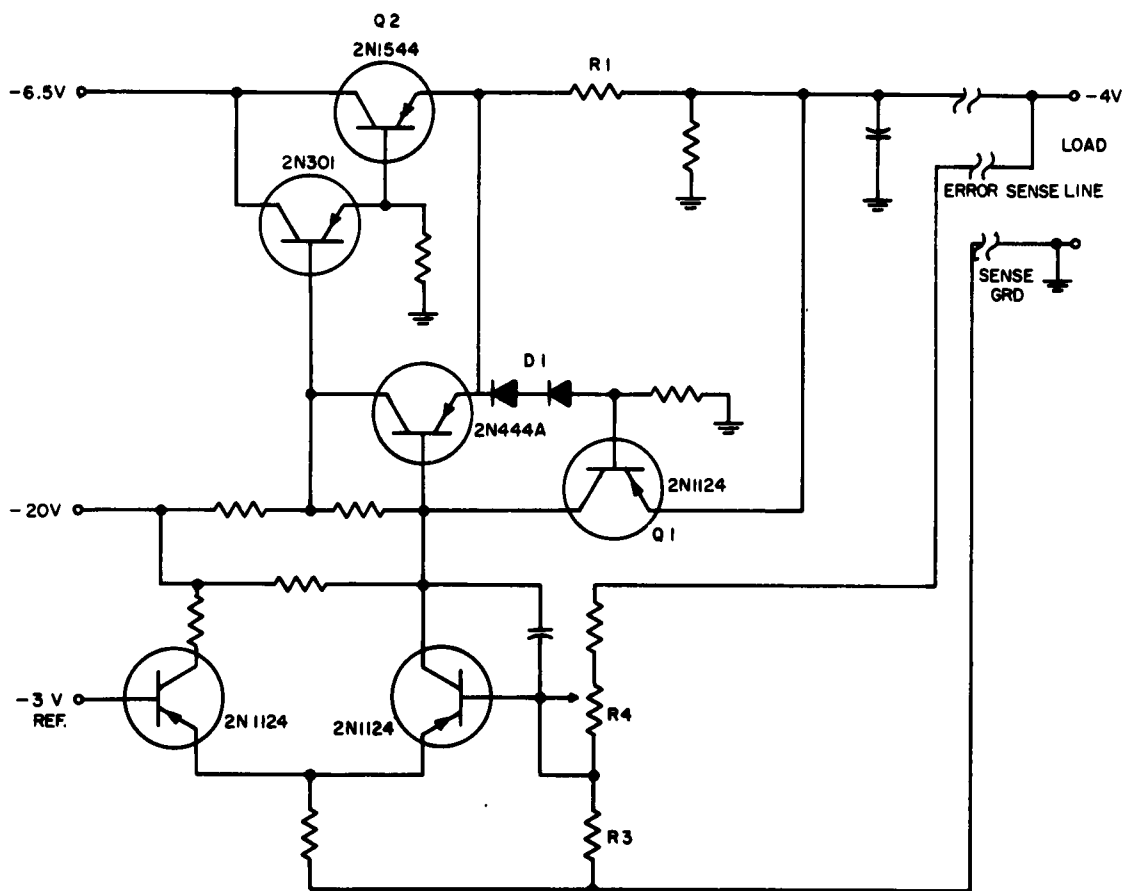


Figure 16. Series Regulator

a more defined current. In Figure 16, when the voltage across the series resistor R1 exceeds the forward voltage drop of diode D1, transistor Q1 turns on. The current through R2 is approximately constant. Therefore the base current of the 2N301 must decrease, thus limiting the current through the series transistor Q2.

The output voltage was designed to be variable without having to vary the -3-volt reference. A potentiometer (R4) was placed in the base circuitry of the differential amplifier. A constant current is drawn through R3 because of the constant reference source. When R4 is increased, the output voltage is decreased because of the constant current.

The heat sink, to which the 2N1544 and 2N301 are attached, was changed to a Verma-line heat sink, which has almost twice as much radiating surface as the 4 x 6-inch plate previously used. This gives a higher power dissipation rating to the series transistor Q2.

The power dissipation of Q2 was measured for all voltage regulators of higher current. It was within the safe limits of the maximum calculated power dissipation.

Some regulators which have small loads were designed without all the features of the higher current regulators. These lower current regulators include the +20, -20, -12, -15, and +24-volt regulators. They use a simple one-transistor amplifier instead of a differential amplifier.

c. **POWER SUPPLY TESTS AND OPERATION.** Initial tests of the supply system included regulation, range of voltage adjustment, and power dissipation in the series regulator transistors. Voltages were adjusted for nominal with estimated maximum computer load as indicated in Figure 15. Regulation was measured between no load and maximum computer load. The results of the test are shown in Table 1.

Interaction tests were also made during the initial testing period. The load was removed from individual voltages and the effects upon other voltages measured when supplying full computer load. This d-c change in load on individual regulators had negligible effect on other voltages.

Further power supply tests will be completed after checkout of logic and memory has been completed. Included will be load current measurements, regulation, and noise measurements.

#### 4. PACKAGING

a. **STATUS OF JDU.** Since the last report, the assembly of the June Demonstration Unit (JDU) has been completed. This unit includes approximately 275 circuit modules, six interconnection multilayer modules, power supply regulators, and a cabinet.

Figures 17 to 21 show the JDU in various views. A complete set of modules is inserted except for sense amplifiers of which only two have been made. A better amplifier has been designed and is being manufactured.

One change was made in the use of materials for electrical connections of the grid boards. It was intended that wire pigtailed with female sockets attached would be soldered in the grid holes. This scheme was replaced with spring pins which were described in

TABLE 1. LOAD REGULATION, JDU POWER SUPPLY SYSTEM

Regulator		Voltage Measured at Computer	
		Zero Computer Load	Full Computer Load
+ 1	Log.	1.035	0.972
+ 1	W.D.	1.028	0.976
+ 1	D.D.	1.027	0.984
+ 1	S.A.	1.007	0.999
+ 24	S.A.	24.026	23.990
- 12	S.A.	12.124	11.920
- 12	W.D.	12.139	11.967
- 15	W.D.	15.207	14.976
- 2.5	Log.	2.288	2.227
- 2.5	S.A.	2.298	2.227
- 4	Log.	4.145	3.973
- 4	W.D.	4.058	3.979
- 4	D.D.	4.069	3.986
- 4	S.A.	4.035	3.986

Abbreviations:

- Log. : Logic
- W.D. : Word Driver
- D.D. : Digit Driver
- S.A. : Sense Amplifier

the last report under the title "Spring Pin Connectors." One of the advantages hoped for was ease of repair of a complete module stack. This was not the case as the large number of pins prevented a complete grid board from being pried off. Although all pins could be removed individually, the plated holes were subjected to possible damage. However, it was felt that the spring pin is successful and is an improvement over the soldered approach for this prototype work.

Test work is now proceeding with logic checkout completed. Errors uncovered during checkout fall into two chief categories — shorts and opens. Shorts due to layout errors (seven) were in most cases burned out with a power supply. New connections

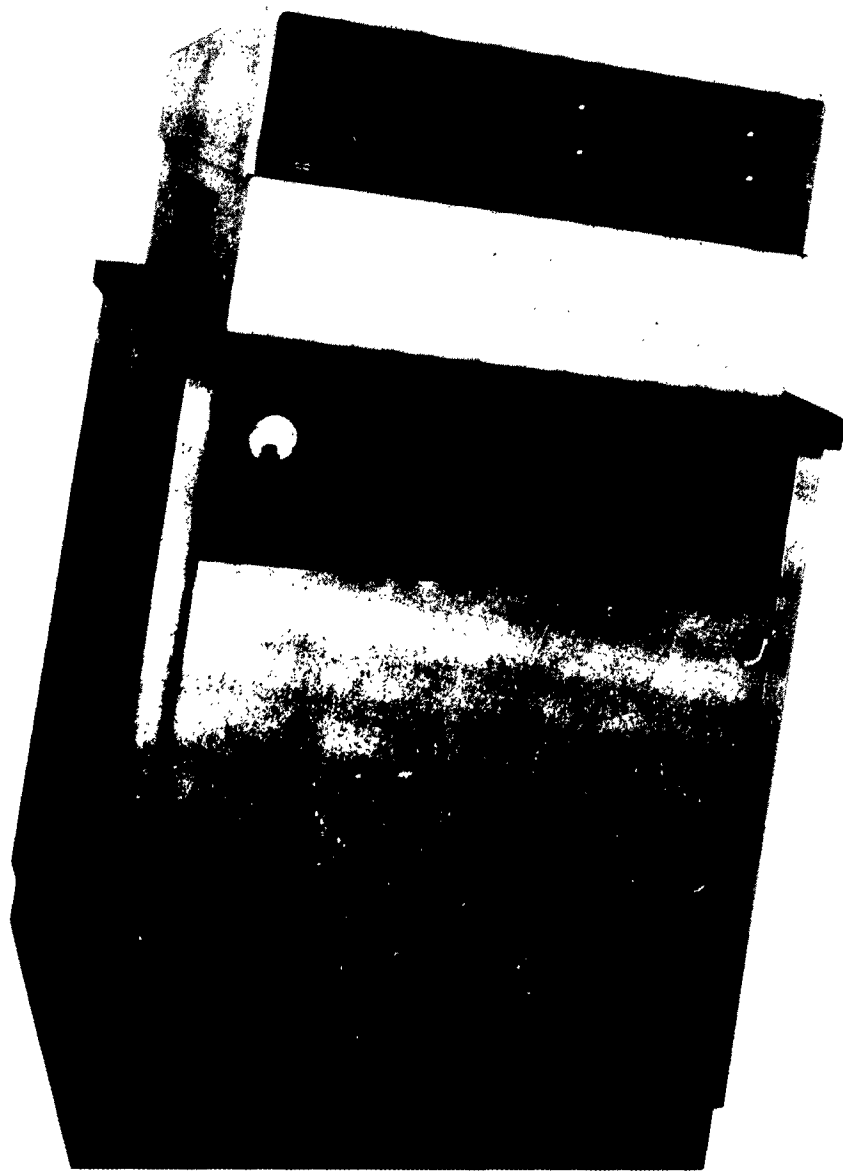


Figure 17. June Demonstration Unit, Front View

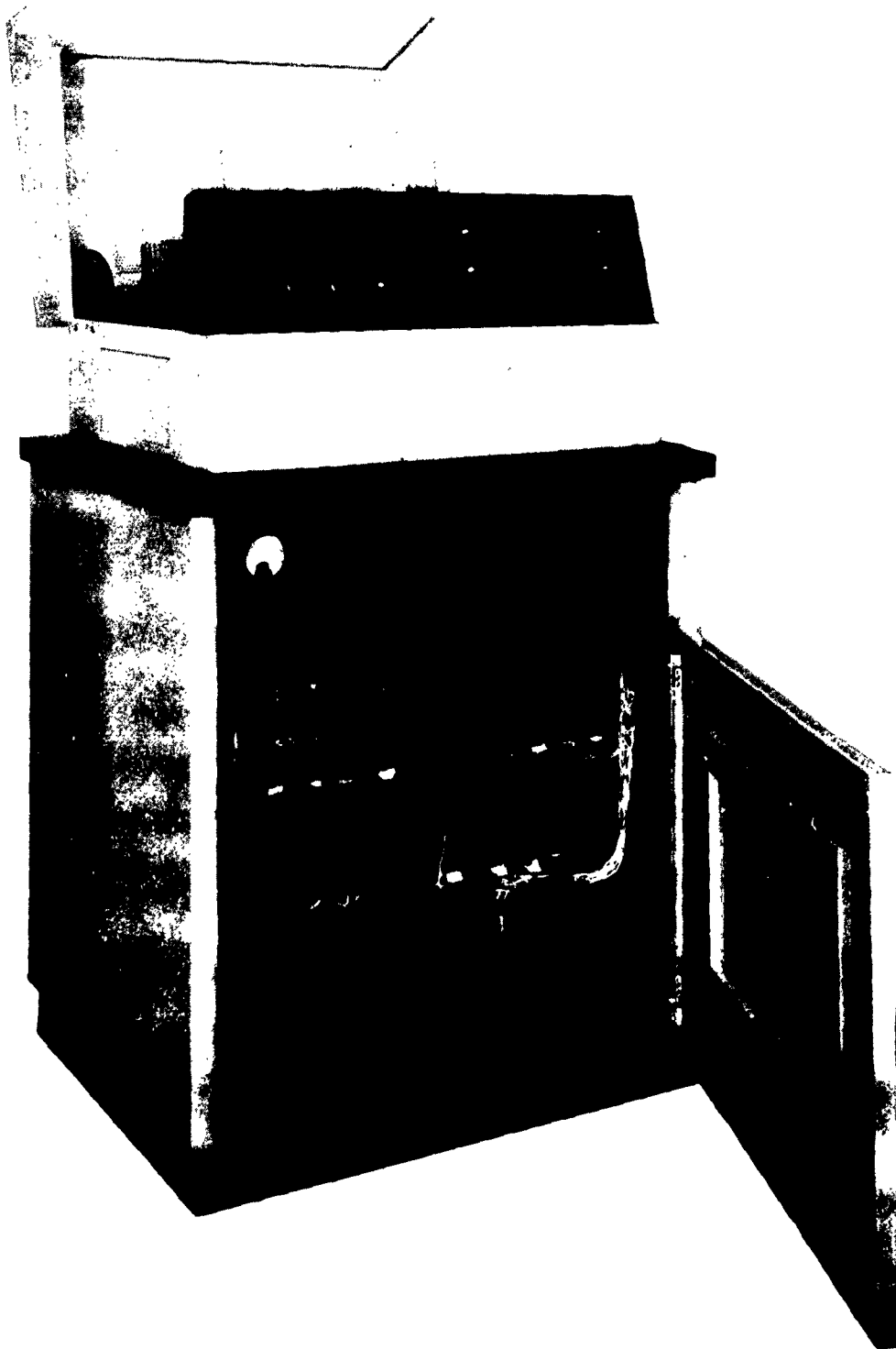


Figure 18. June Demonstration Unit, Front Exposed

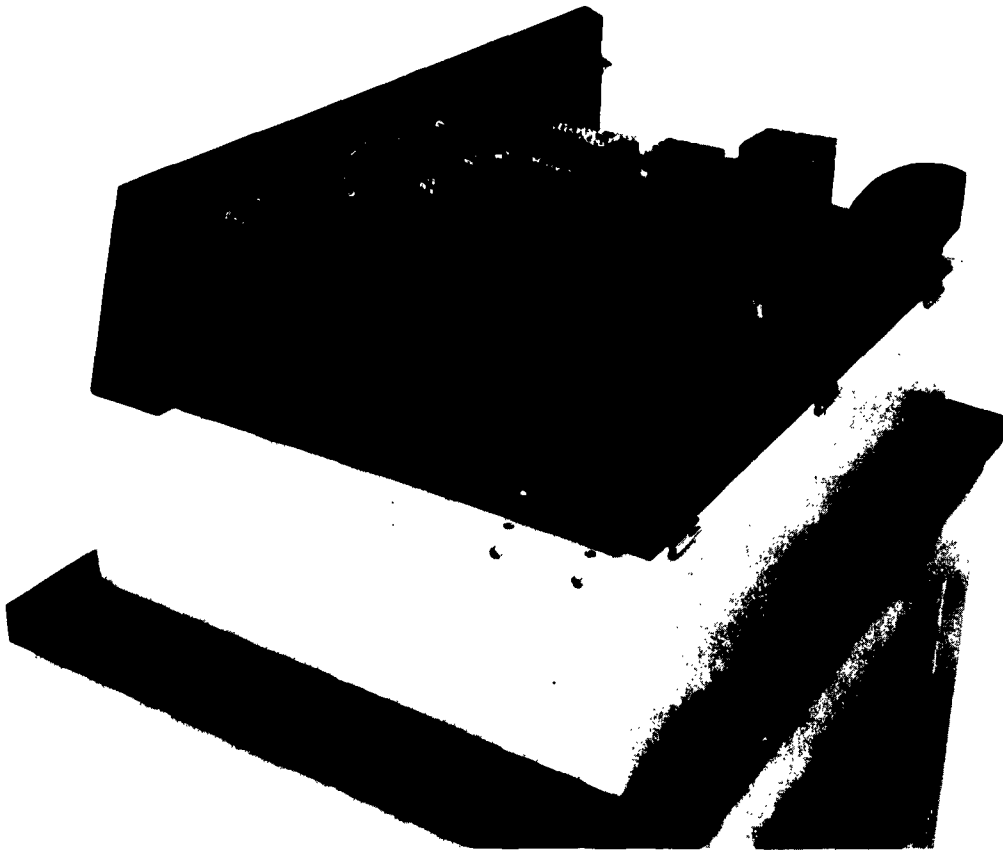


Figure 19. June Demonstration Unit, Left Rear View

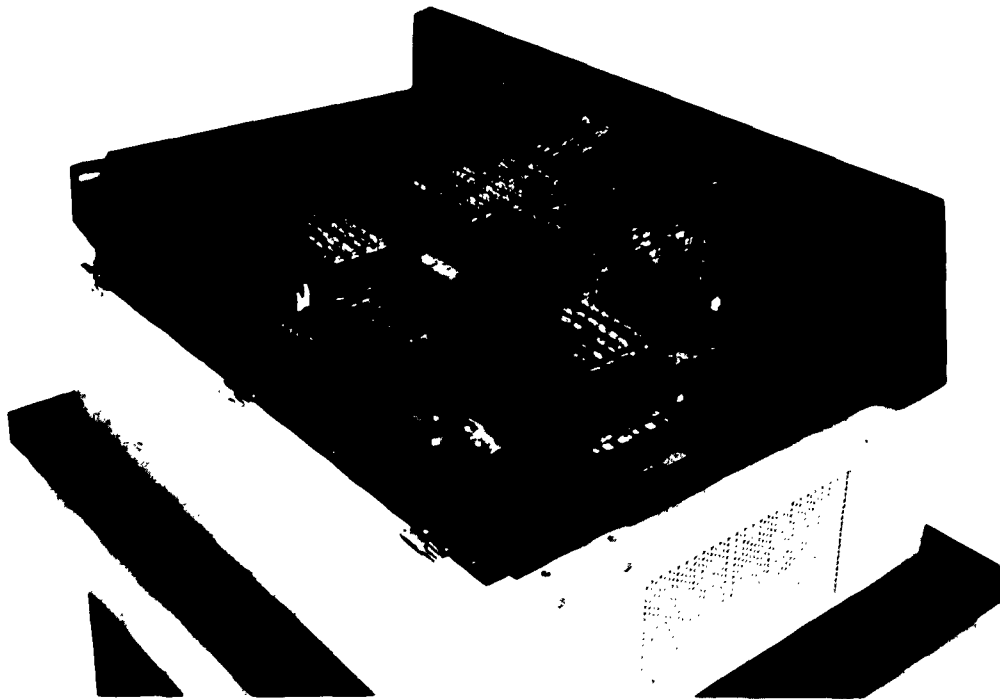


Figure 20. June Demonstration Unit, Right Rear View



Figure 21. Internal Components of the June Demonstration Unit

were made using a twisted pair of wires soldered to the bottom of the connection roll pins. Insertion of roll pins caused some flaking of gold plate on the pin. These flakes caused shorts in the stack, a condition which will be corrected in the future. The shorts were also burned out using a battery or power supply. Open lines due to worksheet layout omissions or oversights in tape-up (20) were repaired by point-to-point twisted pair wiring as above.

The cordwood style package used for the circuit module was assembled with relative ease. Experiments with a flow solder machine proved very successful and will replace hand soldering for the LTM. Lead connections with plated-through holes on 22-mil glass epoxy stock tested out exceptionally well in a pull test. Holes tested resulted in lead breakage averaging 25 lbs. with no indication of failure at the soldered hole.

b. STATUS OF LTM. Figure 22 indicates the present plan for the physical layout of the Lightning Test Machine.

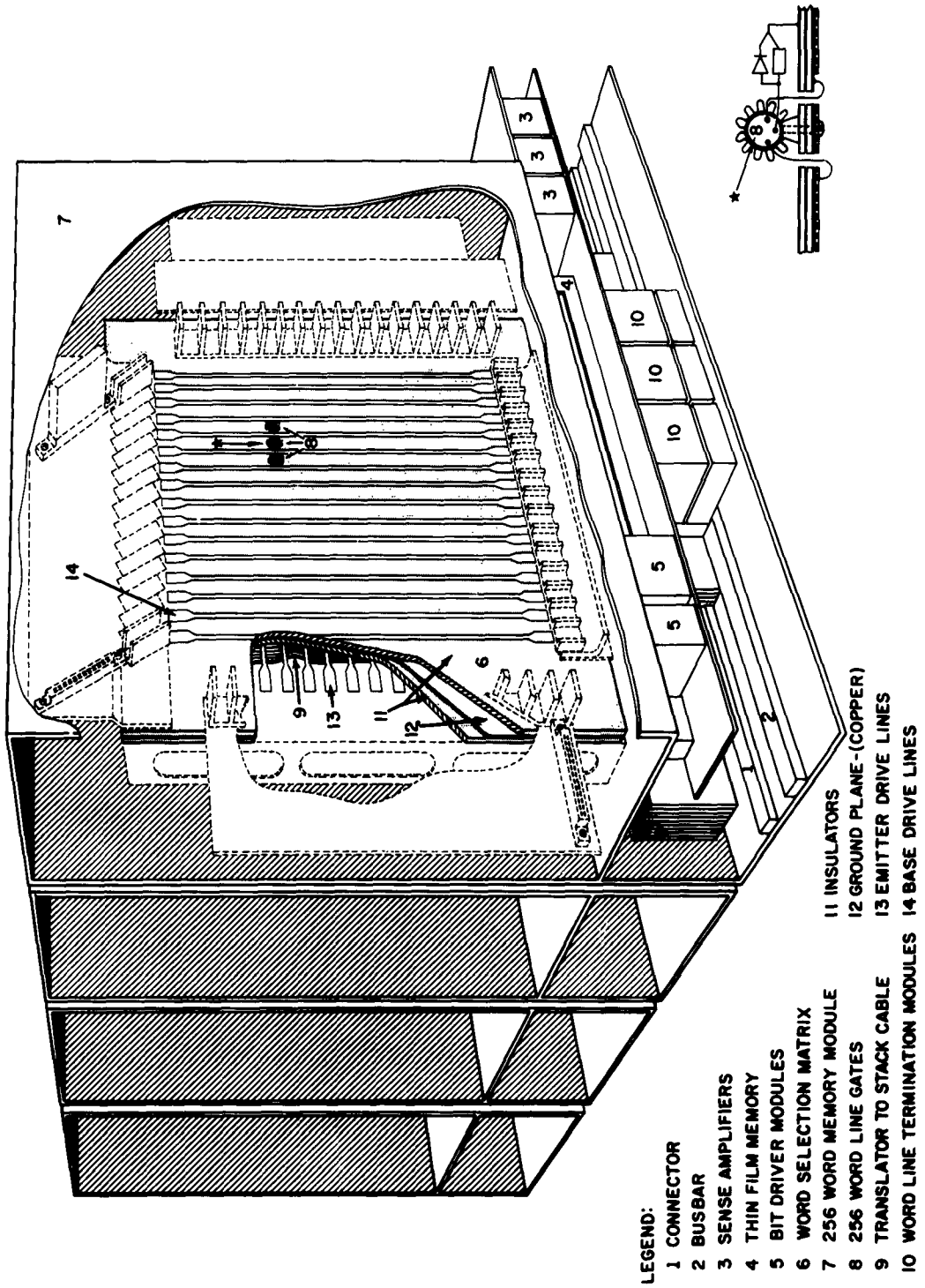


Figure 22. Present Plan for LTM Physical Layout

Four identical 256-word memory modules are planned; these will be individually pluggable units. These modules are shown at the top of Figure 17. Directly below the memory modules is a metal plate which acts as a shield and also supports the connectors into which the memory modules will be plugged. Beneath the shield are two trays of logic which will be individually removable from the computer. The bottom or third tray will contain the shift matrix and search memory.

By shielding and location this layout will isolate the memory circuits from noise generated by the logic circuitry. The layout also permits each memory module to be cooled individually. This provision seems to be essential since each 256-word module dissipates approximately 395 watts.

Circuit module layouts for LTM logic have been started. Even though an effort will be made to reduce module height, it appears unlikely that much can be done. Pin arrangement, test point locations, and special cooling considerations have been resolved for layout work. Tooling to adapt the assembly to flow solder techniques has been tested and is being fabricated.

#### 5. JDU LOGIC MODULE TEST

Testing of the logic modules for the June Demonstration Unit (JDU) has been completed. All defective modules were repaired; rise, fall, and delay times were measured. Figure 23 shows the module test circuit.

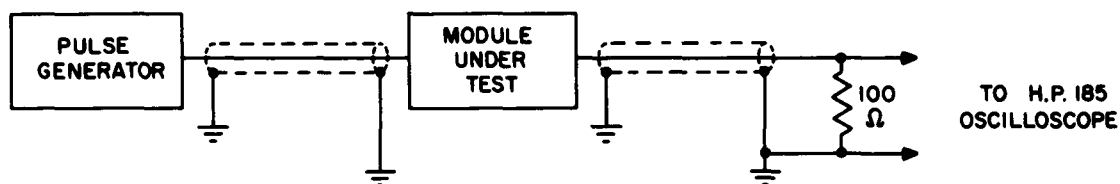
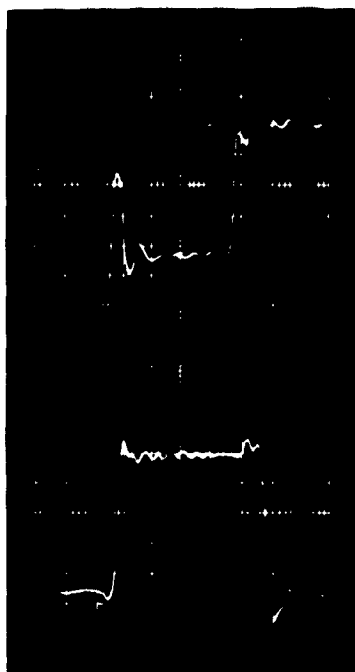


Figure 23. Breadboard Module Tester Circuit

A delay line generator was used which provided a 30-nsec pulse to the module under test. Input waveforms were taken from the pin connections at the module socket, while output waveforms were taken at the end of an 8-inch length of 90-ohm coaxial cable terminated with 100 ohms of resistance. Table 2 summarizes test data for the JDU logic modules. Waveforms are shown in Figure 24.

TABLE 2. SUMMARY OF TEST DATA FOR JDU LOGIC MODULES

Type	Minimum (nsec)			Average (nsec)			Maximum (nsec)		
	Tr	Tf	Td	Tr	Tf	Td	Tr	Tf	Td
4056327	2.2	2.1	5.0	2.6	2.8	5.6	3.2	5.0	6.3
4056308	2.0	1.9	4.8	2.2	2.3	5.3	2.5	3.2	5.6
4056302	1.8	1.8	4.8	2.2	2.3	5.5	3.0	3.1	6.1
4056311	1.9	1.9	5.1	2.2	2.2	5.4	2.6	2.3	5.6
4056305	2.1	2.3	5.1	2.4	2.6	5.7	3.0	3.8	6.0



(a) Input Waveform — At Module Socket Pins

Vertical Calibration: 0.5 volt/div

Horizontal Calibration: 10 nsec/div

(b) Output Waveform — After Passing through Module and 8 Inches of Coaxial Cable

TIME →

Figure 24. Typical Input and Output Waveforms

The most common defects encountered were solder bridges in the printed circuits and open solder connections. Other defects included reversed diode polarities, open diodes, open transistors, feed-through holes etched open, and a plated bridge in the printed circuit.

#### 6. FILM SPOT OUTPUT SIGNAL

In an attempt to correlate an optimum signal output from thin film spots, for various reasonable word drives and film spot thickness, the following plotted data were taken. To obtain these data, the single-bit system was used for the basic driver and amplifier requirements.

The digit bias was maintained at about  $\pm 100$  ma: the word pulse rise time was held at less than 10 nsec, although the magnitude of the word pulse was varied from 230 ma to 545 ma; and the voltage gain of the sense amplifier was approximately 800. All the plotted data for each film thickness and word drive value consisted of the average of the "1" and "0" signal, to cancel the effects of word noise, at two locations in the memory stack. For the 1200 A film spots, the output signal was less than expected from the pattern established by the output from the other films. Although this smaller signal could be due to poor positioning of the film spot pair over the intersection of the digit and word lines, another factor to be considered for these particular films is the plastic coating sprayed on the substrate to prevent scratching or chipping of the film spots. This coating resulted in a greater spacing between the film spot pair and thus less coupling to the sense line.

From the graphs (Figures 25 to 28) it can be seen that although the output signal from thinner films is greater at low currents, more signal is obtained from the thicker films at a reasonable (400 to 500 ma) word drive. Therefore, the use of films from 1000 A to 1500 A with a word drive current of about 500 ma should give satisfactory results.

## 7. INPUT-OUTPUT EQUIPMENT FOR THE LTM

Input-Output equipment for the Lightning Test Machine (LTM) will consist of a photoelectric tape reader and a paper tape perforator, together with the necessary logic and control.

a. **GENERAL LOGIC DESIGN.** Communication between the computer and the input-output equipment will be accomplished with a 24-bit register in each unit. A parallel transfer of the 24 bits of binary data is possible in either direction. Information on paper tape used as input, will be coded in Flexowriter code with the conversion to binary code being completed in the input-output logic. In similar manner, binary data received from the computer is converted to Flexowriter code before being punched on paper tape.

Control and resynchronizing will be accomplished with ready-resume pulses. The signal sent from the LTM to the external equipment will be designated a **READY** pulse. This signal will appear whenever the LTM has accepted data. A **RESUME** signal will originate in the external equipment whenever the equipment is prepared either to accept or send new data.

b. **PHOTOELECTRIC TAPE READER.** A photoelectric tape reader has been selected for use as the input equipment. This transistorized unit, relatively simple to operate and control, will be operated with a reading speed of 60 characters/sec.

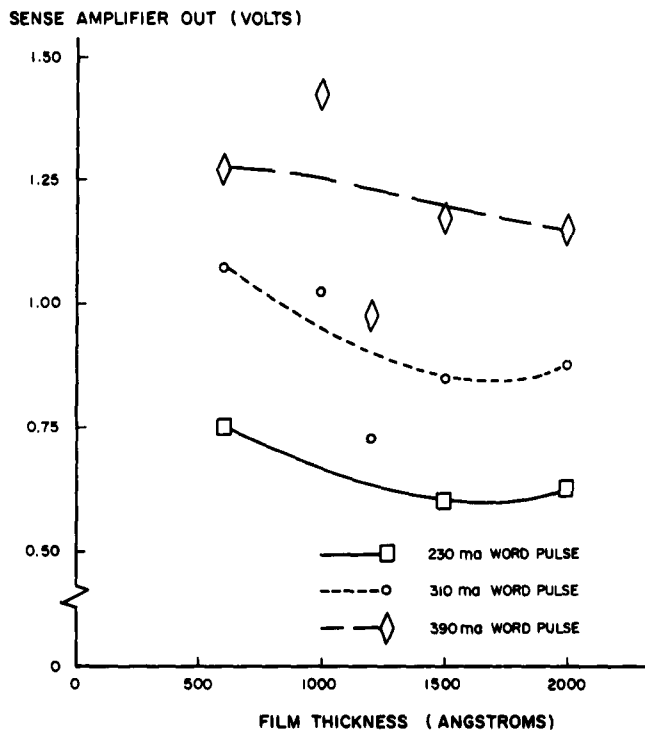


Figure 25. Film Spot Output Signals (240-ma, 310-ma, and 390-ma Word Pulse)

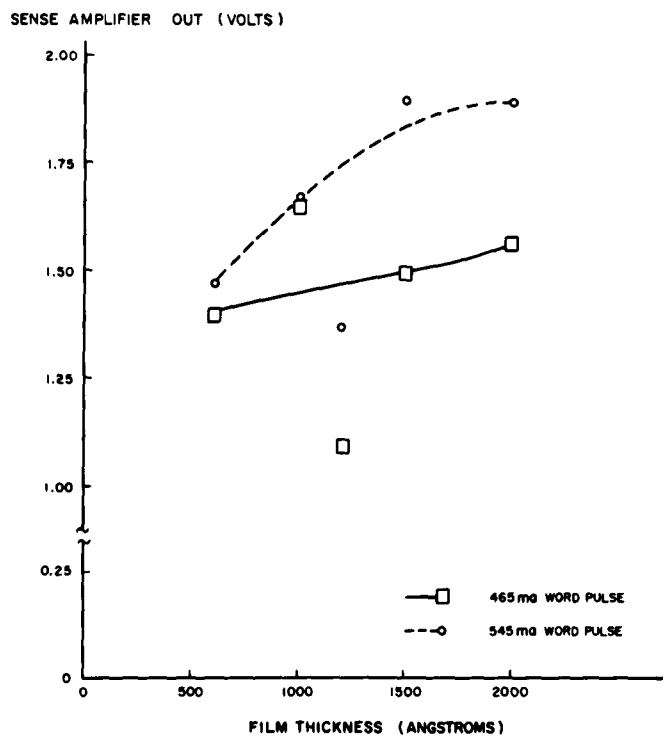
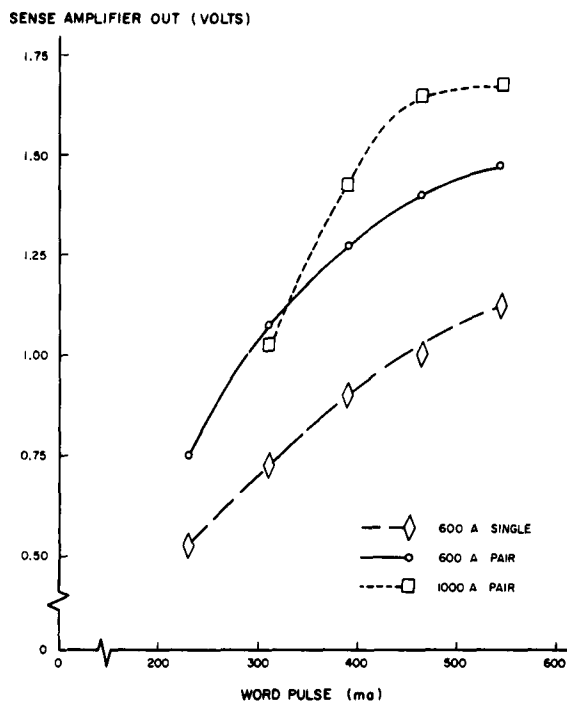
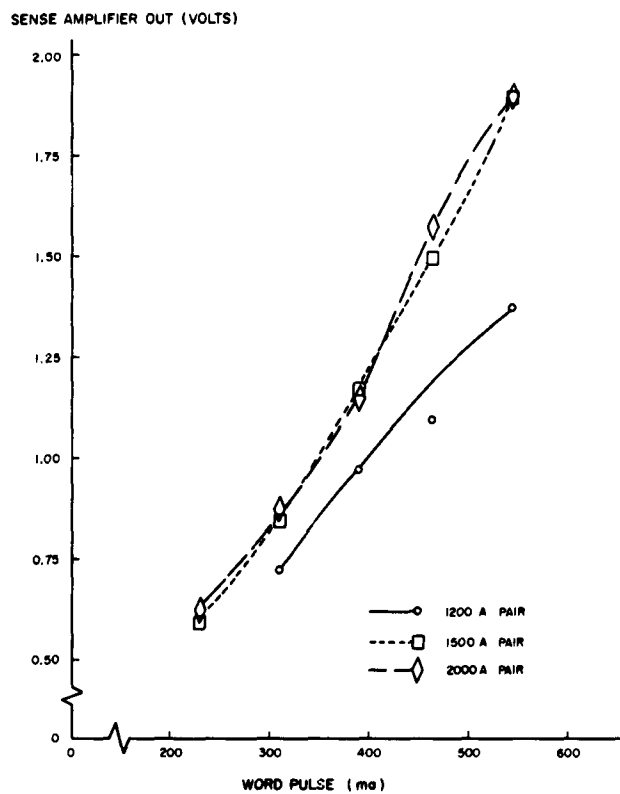


Figure 26. Film Spot Output Signals (465-ma and 545-ma Word Pulse)



**Figure 27. Film Spot Output Signals  
(600-A to 1000-A Thickness)**



**Figure 28. Film Spot Output Signals  
(1200-A to 2000-A Thickness)**

c. **TAPE PERFORATOR.** A Teletype BRPE11 high-speed tape punch has been selected as the output equipment. The unit is designed for operation with signal levels adaptable to transistor control circuitry. Punch speed will be 110 characters/sec.

d. **INPUT-OUTPUT CABINET.** About 300 circuit cards will be required for logic and control of the external equipment. The reader, punch, the above cards, and other control equipment will be housed in one cabinet as an integral unit.

## 8. PHILADELPHIA PROGRESS REPORT

Among the tasks of UEC, Philadelphia, Project Lightning work are the design of a thin-film memory read amplifier, a test of machine clock design, and a study of tunnel diode logic circuits.

a. **READ AMPLIFIER.** An abbreviated task definition for read amplifiers is to study the feasibility of the following tasks:

- 1) Design an amplifier using conventional approaches.
- 2) Design an amplifier using non-conventional approaches.
- 3) Design and build a one-bit Project Lightning film model for read amplifier testing.
- 4) A guide for the read amplifier performance is:
  - a) Input: 0.5 to 3.0 mv, 5 nsec rise and fall time.
  - b) Impedance of sense line: 20 to 30 ohms to ground.
  - c) Common mode rejection: 10:1 minimum during read. Common mode signal during write is 0.2 volt.
  - d) Delay through the amplifier less than 15 nsec.
  - e) Recovery from overload signal of 0.2 volt common mode and 0.1 volt unbalance in 15 nsec.
  - f) Amplifier must present both polarities of input signal for positive AND gating with logic.
  - g) Final output is approximately 2 volts across 100 ohms (i.e., ref. logic circuit input specs).

A GBW evaluator has been built for transistors which may be used in the read amplifier. This equipment uses a 100-Mc constant-current source which has a source impedance of approximately 1 K. The current is standardized by observing a voltage drop of 1 mv across 10 ohms. The GBW product is measured assuming that the input

impedance of the transistor under test can be ignored compared to the source impedance. This appears reasonable since the input impedances are the order of 60 ohms. GBW products for the three best transistors measured to date are 1300 for the TI 2000, 700 for the 2N769 and 600 for the 2N917. Unfortunately, the TI 2000 is at present experimental and not available on the commercial market.

Various schemes are being considered for using tunnel diodes in amplifiers. In one scheme, a tunnel diode in the switching mode was used after the third stage. With the amount of drive available from the third stage, the delay in switching the tunnel diode was excessive (10 nsec). However, some decrease in rise time of the fourth stage output was obtained. Use of the tunnel diodes in a Goto pair configuration for low-level strobing is being considered.

A one-bit closed loop system is being fabricated in order to allow realistic testing of the read amplifier. It had been found in previous work that the GBW of the equipment necessary to generate a realistic inhibit noise pulse was excessive and that the best way of realizing the inhibit noise was to go to the actual configuration that is to be used with the read amplifier. A pair of Project Lightning overlays is being used to construct the closed system. The setup has been made and now being checked out with the impedances of various lines measured prior to fabrication of driving transformers.

b. **HIGH-SPEED CLOCK INVESTIGATION.** An abbreviated task definition for the clock is to study the feasibility of the following tasks:

- 1) Improve the present delay line oscillator-amplifier.
- 2) Study a solid state clock.
- 3) Use as a guide for the clock work:
  - a) Rise and fall time: less than 2 nsec each.
  - b) Repetition rate: four-phase under lap clock, 6.25 nsec per phase.
  - c) Output: 2-volt swing from 0 to -2 volts.
  - d) Output current: 15 amp/phase (i.e., for logic system of over 6000 circuits).
  - e) Load: nonlinear comprised of a set of logic circuits. Any branch current may vary from near zero to maximum depending on logic usage.
  - f) Jitter may be 1 nsec maximum.
  - g) Distribution system involves an area approximately 4 feet in diameter.

An analysis of the delay line oscillator indicates that the use of a hyperbolic tapered line will probably be preferable to the exponential tapered line. This is because transmission coefficient of the exponential line has zeros every half wave length while the hyperbolic line is monotone with frequency. Thus, the hyperbolic line allows for more manipulation with external tuning to handle properly the second and higher order harmonics of the waveform than the exponential line. With the exponential line, frequency jumping can be obtained and has been observed on occasion.

A simple d-c restoration circuit has been made which allows for a compensation of 150 ma in load in approximately 100  $\mu$ sec. The circuit is of a straightforward type using a grounded base stage to drive a grounded emitter stage.

Attention is also being focused on the miniaturization of the matching transformer from the plate of the driving tube to the load. Two approaches have been outlined:

- 1) A helical transformer miniaturized by using some of the techniques developed by the Materials Lab at UEC-Whitpain. Possible parameters of such a transformer are:

Tape width	36.3 mils
Dielectric thickness at 100-ohm end	16.6 mils
Dielectric thickness at 6-ohm end	1 mil
Number of turns	30
Axial length	Approx. 1 1/2 inches
Axial diameter	1 inch.

If the tape width is varied for the impedance transformation, the parameters are:

Dielectric thickness	1 mil
Tape width at 100-ohm end	2.18 mils
Tape width at 6-ohm end	36.3 mils
Number of turns	30
Axial length	1/2 to 1 inch
Axial diameter	1 inch.

Whether these small dimensions can be held is yet to be ascertained.

- 2) An approach in which the helix is collapsed into a cylinder. It is estimated that such an approach will result in a transformer with an inner radius of 1/2 inch, an outer radius of 3 inches and approximately 1 inch in axial length.

The impedance transformation is obtained by tapering the hot conductor of the rolled-up transmission line. This spiral technique appears more promising than the helical technique at this time.

c. TUNNEL DIODE LOGIC CIRCUITS. The three logic circuits considered were: 1) voltage mode tunnel diode circuits, 2) emitter-follower tunnel diode circuits, and 3) monostable threshold circuits.

(1) VOLTAGE MODE TUNNEL DIODE CIRCUITS. This is a series connection of two tunnel diodes and a coupling diode to prevent reverse flow of signal. The clock voltage equals the sum of the tunnel diode peak voltage and the coupling diode forward drop. With either tunnel diode in the high-voltage state, the other must therefore be in the low-voltage state. The result for either diode is two states or bistable operation.

Two transfers are proposed in this system (Figures 29a and 29b): An A to B stage transfer or a B to A stage transfer. The circuit which provides OR or AND operation will depend upon the logic levels specified.

If it is assumed that a "1" will be a negative level and a "0" a positive level, then a "1" is represented by a low state in an A diode and a high state in a B diode. The operation from A to B is therefore an OR function and the operation from B to A is an AND function.

In the A to B transfer (Figure 29a) any one A stage in the low state, coupled to a B stage, will switch the B stage to its high state when the clock voltage is applied. If, therefore, a "1" is specified for an A stage as the low state and a "1" for the B stage as the high state, the OR function is obtained.

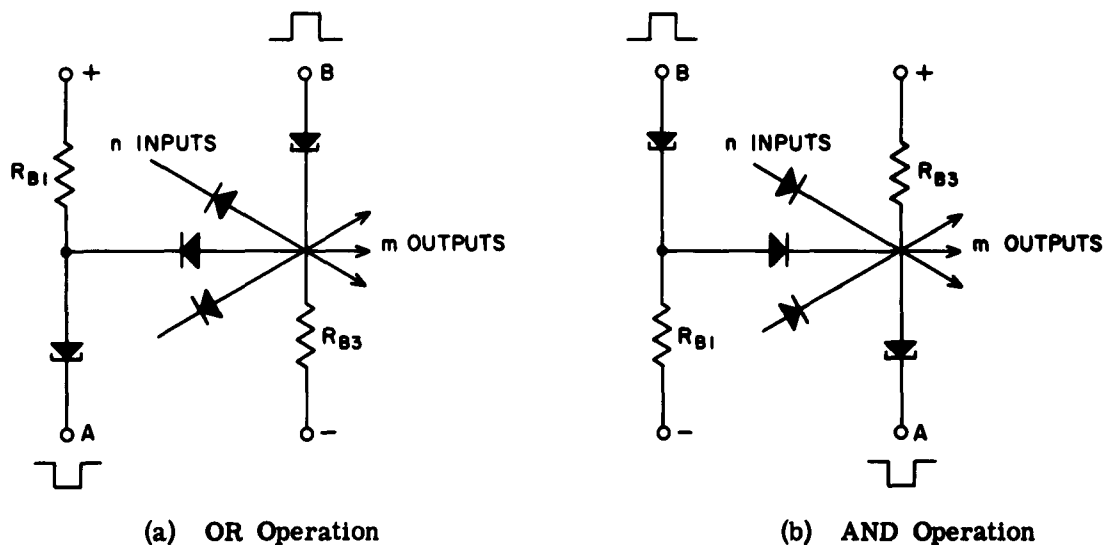


Figure 29. Voltage Mode Tunnel Diode Circuits

In the B to A transfer (Figure 29b), in order to obtain a "1" at the A stage (that is, the low state of A) using the logical levels specified in the A to B transfer, all the B stages connected to A must be in the high state. Any "1" B stage in its low state will switch the A stage to a "0" or high-level state; therefore, A inputs at the "1" level put the B stage at the "1" level giving the AND function.

A typical arrangement of AND, OR logic is shown in Figure 30. For the logic to propagate correctly through this system, a clock of the form shown in Figure 31 is required. This is a four-phase clock arranged in two pairs. During the operating period,

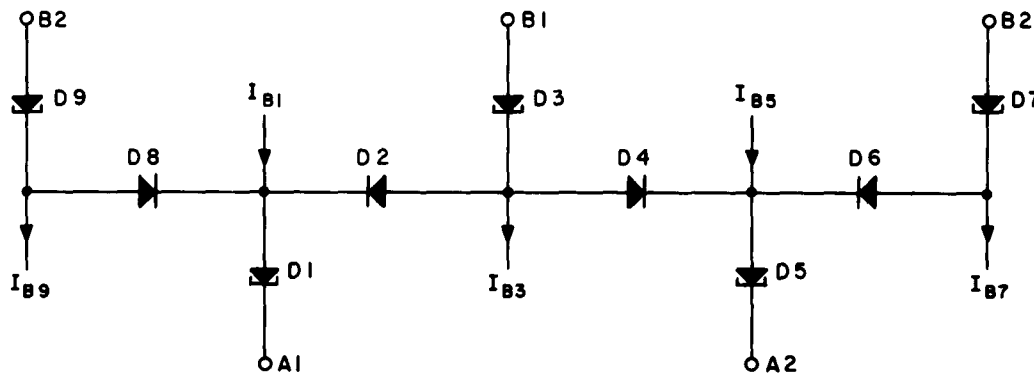


Figure 30. Sequence of AND, OR Operation

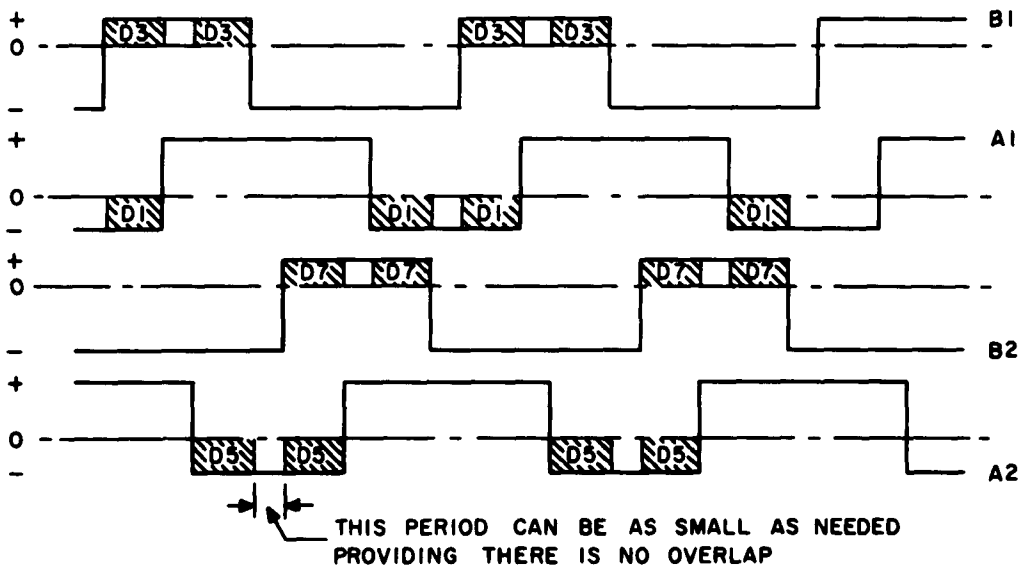


Figure 31. Clock Timing Diagram

an A-phase clock will be negative and a B-phase clock will be positive, thus giving conduction through an A diode, a B diode, and the coupling diode; e.g., A-phase diode D1, coupling diode D2 and B-phase diode D3. During the non-operating period, the diodes must reset to the low state. Therefore, the A-phase clock must go positive and the B-phase clock negative.

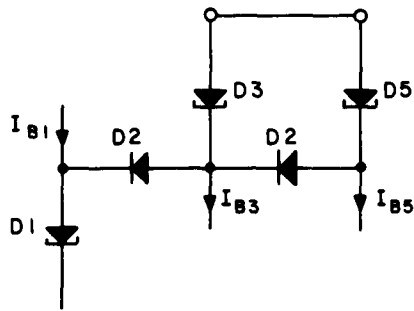


Figure 32. Buffer Stage

Research was directed to the problems of the limit on the number of stages in cascade, tolerance required for the clock, and transient analysis to indicate the speed to be expected for this circuit.

In this system, a diode D1 in its low state will transfer information to the next diode D3 by forcing this diode to switch to its high state. To ensure that this will happen under all worst case conditions, the bias current  $I_{B3}$  must be greater than  $I_{B1}$ . The difference between  $I_{B3}$  and  $I_{B1}$  will depend upon fan-in, fan-out and tolerances. Thus, we can say that the

bias current in each stage will increase successively between a lower and upper limit. When the upper limit is reached, revert to the lower limit as simply as possible. This can be achieved by adding another tunnel diode, D5, to the circuit (see Figure 32). If a large fan-in and fan-out is required, then D5 will be needed after every stage; but for a small fan-in and fan-out, D5 will only be needed after several stages.

If a tolerance of 2 percent on peak and valley current, components and voltages is reasonable, the results are as follows:

Number of Stages Between Buffer Stages	Fan-in and Fan-out
13	1
2	2
1	4

When this tolerance is raised to 10 percent, a fan-in and fan-out of only 1 is operable, and a buffer is required between each stage.

From the normalized diode characteristics assumed, the voltage limits on the clock indicate a suitable voltage to be 850 mv  $\pm$  15 percent, for a symmetrical settling system.

Transient calculations were made, using the circuit of Figure 33.  $C_{D1}$  and  $C_{D2}$  were neglected since their effect would be to speed up the switch of diode D3. D1 remains in the low state, and the clock is a square wave of internal resistance  $R_C$ .

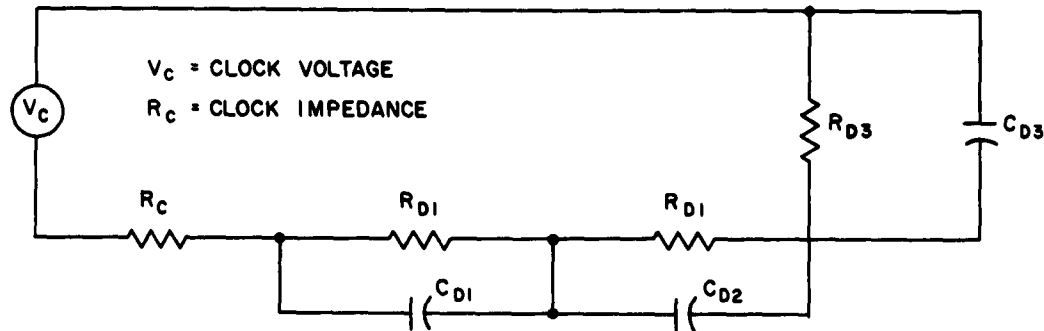


Figure 33. Transient Equivalent Circuit

The clock impedance could be reduced considerably, to give a faster switching time; however, an overlapping clock system would have to be used to ensure that when the clock goes off, it does not reset the tunnel diode to which the information has been transferred. Unfortunately, an overlapping clock system would mean that two A stages could conduct through a B stage and two B stages could conduct through an A stage at the same time. Although this is possible, the fan-in and fan-out would be reduced considerably for this type of system.

Using a piecewise linear approximation for the characteristic of diode D3, the calculated switch time for a GE1N2941 is 4.523 nsec for these parameters:

$V_C = 720$ mv	$C = 25$ pf
$R_C = 50$ ohms	$R_{D3}$ (Region 1) = 7.4 ohms
$R_{D1} = 7.4$ ohms	$R_{D3}$ (Region 2) = $\infty$
$R_{D2} = 11.7$ ohms	$R_{D3}$ (Region 3) = -19 ohms
	$R_{D3}$ (Region 4) = $\infty$

Another limiting factor on the high-frequency performance is the reverse recovery time for the coupling diodes. One of the fastest diodes available is the Qutronics Q5-100. The maximum capacitive effect in the circuit under reverse recovery conditions is 4.98 pf reverse recovery capacitance and 0.98 pf geometric capacitance. These capacitances

are calculated from the charge under the switching curve when the diode is switched from a forward current of 20 ma to a reverse voltage of -3. For the Q5-100, the charge is approximately  $15 \times 10^{-12}$  coulomb.

For the example discussed, the forward bias is in the order of 5 ma before switching. Therefore, let us assume that the total charge to be dissipated in CR is  $15/4 \times 10^{-12}$  coulomb. If this charge were transferred instantaneously, the change in voltage across C would be given by:

$$V = \frac{Q}{C} = 0.15 \text{ volt.}$$

Maximum change allowable = 0.08 volt

This change in voltage is enough to switch D3 below the valley voltage and cause a malfunction, since maximum change allowable is  $V_1 - V_V = 80$  mv. By applying the charge in the form of a ramp function, i.e., a certain number of coulombs per CR, the charge can be dissipated without increasing the voltage V severely.

Therefore, providing the clock rise time did not exceed 1 nsec, this circuit would function correctly. As the switching time for the GE 1N2941 is in the order of 4.4 nsec, this does not present a limitation on the system.

Comparing this system with the analog threshold and the Goto pair circuits, it may be noted that:

- 1) For similar component tolerances, this circuit has a larger fan-in and fan-out and a much wider tolerance on clock voltage than the analog threshold gates.
- 2) The Goto pair circuit has the same order of tolerance fan-in and fan-out magnitudes.
- 3) For the same fan-in and fan-out, the switching time for the analog threshold is approximately twice the switching time of one stage of this system.
- 4) To compare switching speed with the Goto pair, we must consider maximum clock operation, as the Goto pair circuit switching time was not easily defined.

The maximum operating frequency of the voltage mode circuits using the 1N269 is 150 Mc. If higher frequency tunnel diodes are used, the rectifier coupling diodes will limit high-frequency performance. For the rectifier diodes discussed here (Qutronics Q5) the clock frequency will be restricted to less than 500 Mc. Thus, the Goto pair upper frequency limit of 1000 Mc will be superior.

In summary, the voltage mode system has an improved performance over the analog threshold but does not have the high-frequency performance of the Goto pair circuit.

(2) **EMITTER-FOLLOWER/TUNNEL DIODE LOGIC CIRCUIT.** This section evaluates logic circuitry utilizing transistors (emitter-follower mode) and tunnel diodes. The transistors are used to provide unilateral asynchronous propagation as an alternative to a multiphase clock system. By acting as the coupling element between input signal and the tunnel diode, the transistor provides good isolation between input and output as well as an increase in available drive current. The emitter-follower configuration is chosen since it is suitable for high-speed operation and gives compatible voltage levels. At present, the transistor limits the speed of these circuits.

Two AND - OR circuits are proposed. Both accomplish compatible input-output levels for AND - OR operation. In conjunction with tunnel diodes, one uses PNP-NPN complementary transistors. The other has only NPN transistors with diodes to restore the d-c level.

The first circuit proposed (Figure 34) is an AND - OR pair, using complementary NPN and PNP transistors to compensate for the change in d-c level which occurs across an emitter-follower due to the  $V_{BE}$  drop.

The inputs to the N-stage transistors are connected to P-stage tunnel diodes which are biased positively giving a positive input of 0 to  $V_P$  or  $+V_V$  to  $V_{FP}$ . Conversely, the inputs to the P-stage transistors will be negative values of  $-V_P$  and  $-V_V$  from N-stage tunnel diodes biased negatively with respect to ground.

Figure 34 shows that the  $V_{BE}$  drop has to be large enough to switch the output tunnel diode into its high state when the input tunnel diode is in its low state. This puts a lower bound on  $V_{BE}$ . If the  $V_{BE}$  drop is too large when the input tunnel diode goes to its high state, it will not switch the output tunnel diode back to the low state. This puts an upper bound on  $V_{BE}$ .

To obtain the AND and OR functions from this pair of circuits, the logical levels must be specified.

Let the high level ( $V_V$  to  $V_{FP}$  region) represent a "0" for an N-stage output tunnel diode and a "1" for a P-stage tunnel diode. Thus, the low level or 0 to  $V_P$  region must represent a "1" for an N-stage tunnel diode and a "0" for a P-stage unit. In magnitude and direction, this is shown in Table 3.

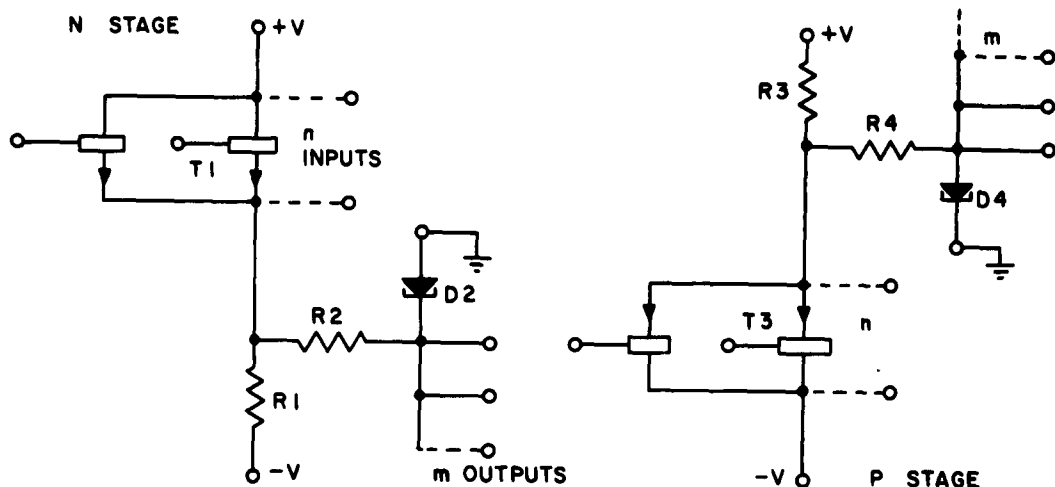


Figure 34. NPN, PNP Complementary AND-OR Logic Circuit

TABLE 3. LOGICAL SIGNIFICANCE OF OUTPUT LEVELS

Stage	Output Level	Logical Definition
N	$-V_p$	1
N	$-V_v$	0
P	$+V_p$	0
P	$+V_v$	1

If any one of the NPN input transistors has a "1" ( $+V_v$ ) applied to the base, the output tunnel diode D2 will be switched to the low state of  $-V_p$  value. This gives the OR function.

If all the inputs to the P stage at the "1" ( $-V_p$ ) level, the output tunnel diode D4 will be switched to the high ( $+V_v$ ) level. When  $(n-1)$  inputs are at  $-V_p$  and one input is at  $-V_v$ , the output tunnel diode will be switched to the low state giving the AND function.

The N stage of an alternate scheme (Figure 35) is identical to the N stage of the PNP-NPN arrangement (Figure 34). In order to get the output voltage from tunnel diode D2 at the same d-c level as the input voltage to the N stage, a transistor and a coupling diode have been added. The transistor is used in the emitter-follower configuration to give a low-impedance drive to the output, and the rectifier diode has a drop across it to compensate for the negative output level and the transistor  $V_{BE}$  drop. Thus,  $V_a$  of

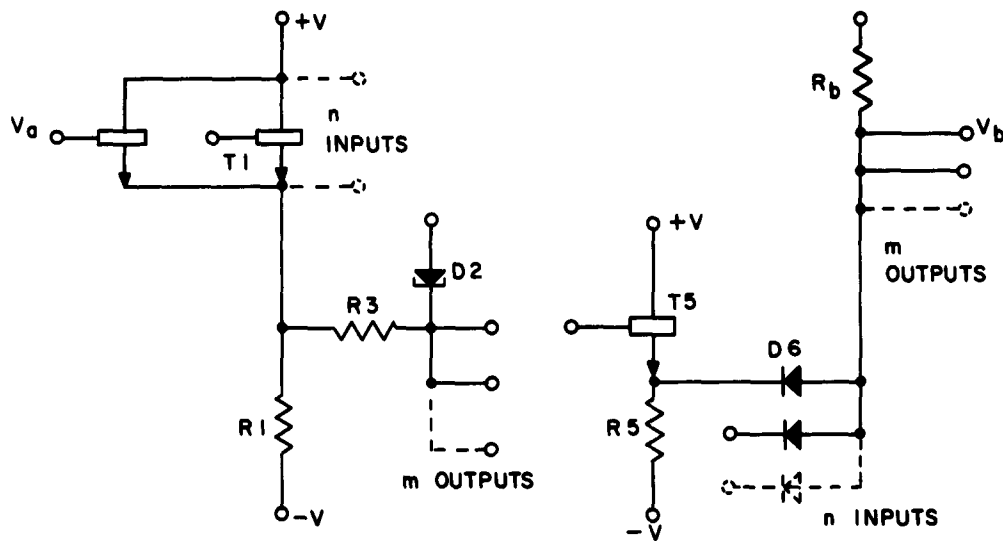


Figure 35. NPN, Diode AND-OR Logic Circuit

Figure 35 is at the same level as  $V_b$ . The OR function is performed by T1 and D2, and the AND function by T5 and D6.

In analyzing the complementary transistor tunnel diode circuit,  $I_e$  (transistor emitter current) was chosen to be  $1.3 I_p$  (tunnel diode peak current). The circuit tolerances were:

$I_p \pm 5$ percent	$I_B$ (transistor base current) $\pm 100$ percent
$I_V \pm 5$ percent	Resistors $\pm 2$ percent
$V_P + V_V \pm 5$ percent	Maximum allowable change in $V_{BE} \pm 5$ percent

Choose:

$$V_p = 50 \text{ mv} \quad V_V = 350 \text{ mv} \quad M = 3$$

Table 4 presents the results of this calculation for the worst case. The difficulty of matching complementary transistor base-emitter characteristics in the 600- to 800-mv range suggests the alternate transistor diode scheme for d-c restoration may be more easily built. The fan-in is limited by the leakage of the transistors, and at 100 C this limit is 14. In a high-speed circuit, capacity would limit the fan-in to less than 14, so there is apparently no leakage problem.

TABLE 4. LOGIC CIRCUIT DESIGN FACTOR

$V_{BE}$ (mv)	$\frac{I_P}{I_V}$	$\frac{G_2}{I_P} = \frac{1}{R_2 I_P}$ (mho/amp)	$\frac{I_B}{I_P}$ max. value	Beta min.
675	7.5	2.815	0.143	9.1
675	8	2.65	0.113	11.5
675	10	2.11	0.02	65
700	5	2.68	0.133	9.8
700	6	2.213	0.0554	23.5
700	7	1.893	0.00332	392
725	4	2.435	0.115	11.3
725	5	1.945	0.0212	61.3

The switching time of these circuits may be taken in two parts, the transistor switching time and the tunnel diode switching time.

(a) TRANSISTOR SWITCHING TIME. The transistor is operated in the grounded collector configuration and it can be assumed that the transistor will never saturate because of the low voltage swings. Therefore, the turn-on time constant is one of major interest. If it is assumed that the output rise and fall time will depend only on the time constant

$$T_{T1} = \frac{R_{T1} R_L C_0}{R_L + \frac{R_{T1}}{n}}$$

where  $n$  is the fan-in factor;

$$R_L = R_3 + \frac{R_B R_D}{R_B + R_D}$$

in parallel with  $R_1$  and  $C_0$  is the total output capacitance including strays for one transistor.

$C_0$  was measured for two 2N743's and two 2N744's; the results show an average capacitance of 45 pf at 100- $\mu$ a bias current.

Using the following nominal values, the 10 to 90 percent rise time was calculated:

$$R_{T1} = 30 \text{ ohms}$$

$$R_L = \infty \text{ as the tunnel diode can be in the valley current region and } \frac{V}{R_1} \text{ can be assumed to be a constant current sink.}$$

$$C_0 = 40 \text{ pf average.}$$

The 10 to 90 percent rise time is  $2.2 CR$ . In this case, the rise time is equal to 2.6 nsec for  $n = 1$ . Thus, the transistor rise time is comparable to the total switching time of the tunnel diode. Therefore, if a 100-Mc system were required with the components chosen above, the fan-in would be limited to less than 5. Much faster tunnel diodes are available with low peak currents (Sylvania D-4168 series) and total switching times significantly less than 1 nsec. The delay time of present-day transistors alone would then be the speed-limiting components.

(b) TUNNEL DIODE SWITCHING TIMES. To simplify the analysis, several assumptions are made:

- 1) Idealized line segments are used for the tunnel diode (Figure 36).
- 2) The equivalent circuit (Figure 37) is valid over the range of interest.

The differential equation for the circuit in Figure 37 is:

$$\frac{V_0(t) - V_1(t)}{R_3} + \frac{V_0(t)}{R_B} + \frac{V_0(t)}{R_D} + \frac{C dV_0(t)}{dt} + I_D = 0. \quad (1)$$

Solving for  $V_0(t)$  for a step input  $V_1(t)$ ,

$$V_0(t) = (I_1 - I_D) R - (I_1 - I_D) R - V_0 e^{-\frac{1}{CR} t} \quad (2)$$

where  $I_1 = \text{input current } \frac{V_1}{R_3}$  and  $\frac{1}{R} = \frac{1}{R_3} + \frac{1}{R_B} + \frac{1}{R_D}$

Solving for  $t$ , equation (2) becomes

$$t = CR \ln \frac{(I_1 - I_D) R - V_0(t)}{(I_1 - I_D) R - V_0(t)}$$

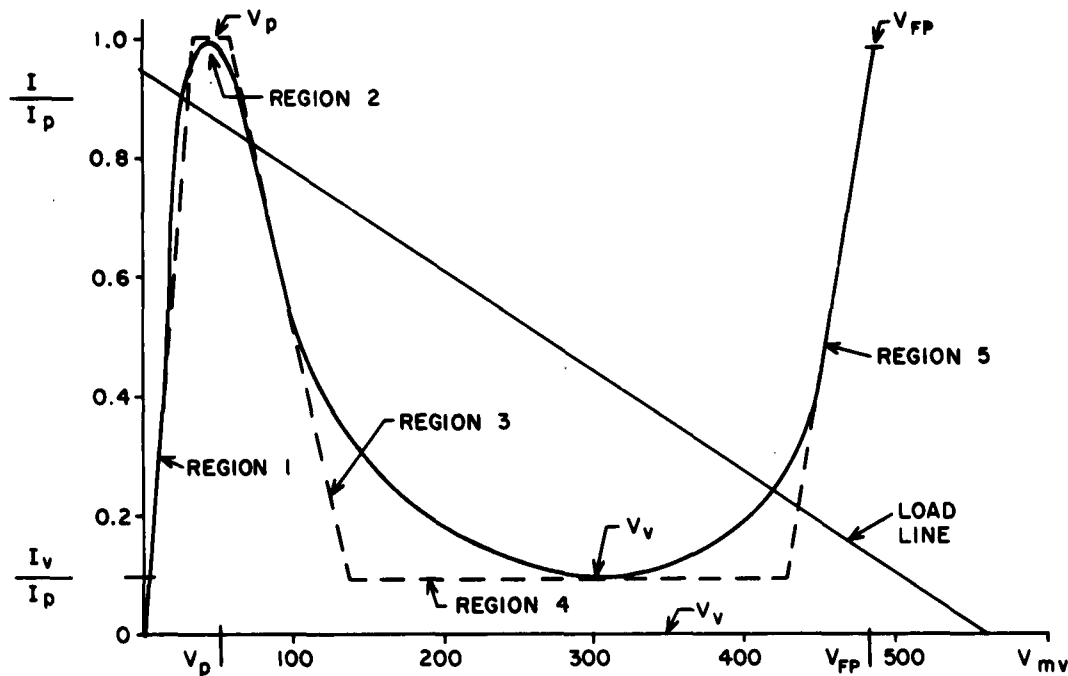


Figure 36. Tunnel Diode Normalized Characteristic Curve

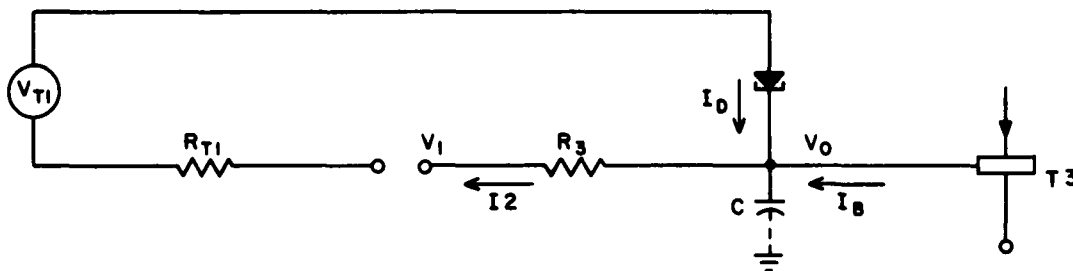


Figure 37. D-C Worst Case Equivalent Circuit

The switching speeds of the 2N2941 in this application are shown in Table 5. The emitter-follower tunnel diode circuits described above accomplish asynchronous logic. The tunnel diode acts as a voltage-sensitive bistable element whose fast switching characteristic, with low-impedance drive, provides reshaping of the logical signal. Of the two forms of the logic, the one using PNP-NPN transistors is undesirable since it requires matched  $V_{BE}$  using silicon transistors only. By using epitaxial NPN silicon transistors

TABLE 5. SWITCHING SPEEDS OF 2N2941

Region	Time Nsec
1	0.0784
2	0.203
3	0.262
4	2.02
Total	2.5634

NOTE: Region (5) is not calculated as at the end of Region (4), the voltage is greater than 90% of the output voltage.

and PNP germanium units, the matching can be obtained. However, the voltage levels are unsuitable for germanium tunnel diodes. Where diodes are used to maintain the required voltage levels (Figure 35), the circuit becomes more practical. In both cases, it is necessary to specify upper and lower tolerance limits on the transistor  $V_{BE}$  as well as the tunnel diode peak to valley ratio. Selection of such transistors and tunnel diodes is difficult and expensive. Assuming such components are available, the tolerance and fan-in and fan-out of the emitter-follower tunnel diode logic is better than the analog threshold type.

The maximum speed of operation is limited by the transistor switching time and the large values of emitter-to-base capacitance in the active region. With components considered in the present analysis, a 100-Mc logic system is practical but further improvement in speed requires higher speed transistors. At the present state of the art, tunnel diode circuits of the Goto-pair type or diode-coupled type offer much higher speed of operation and greater simplicity.

(3) **MONOSTABLE THRESHOLD LOGIC.** Tunnel diode monostable circuits are used to provide a high-speed unlocked logic system. Fast rise times are obtained with the RCA high-speed tunnel diodes, but the system repetition rate is slowed down by the recovery time of the circuit. Two tunnel diodes are used per stage, one acting as an amplifier, thereby giving increased tolerances. The rise and reverse recovery time are investigated.

The circuit (Figure 38) uses the analog threshold principle to obtain the logic and relies on the time constant of the inductance in series with the tunnel diode and backward diode (Figure 39) to hold the tunnel diode in the high state for a period long enough to transfer the information before resetting.

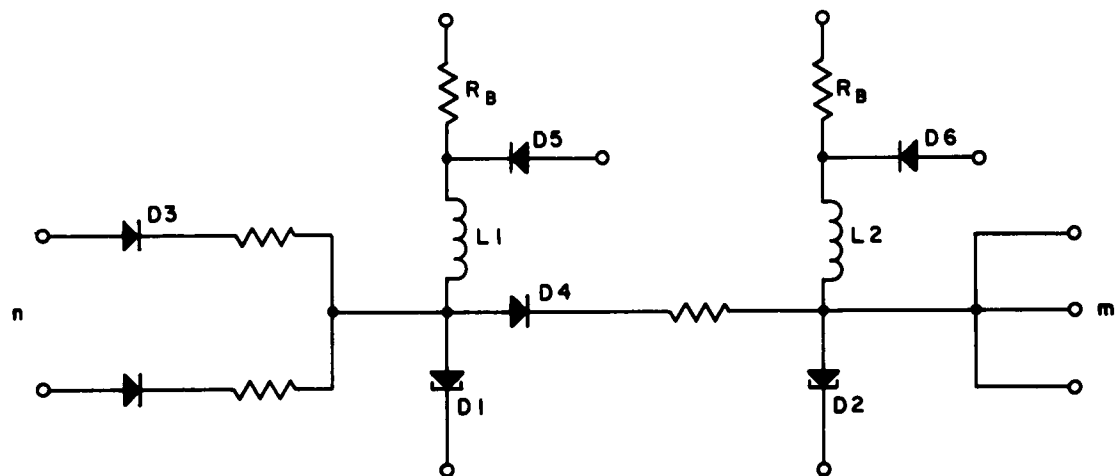


Figure 38. Tunnel Diode Monostable Circuit

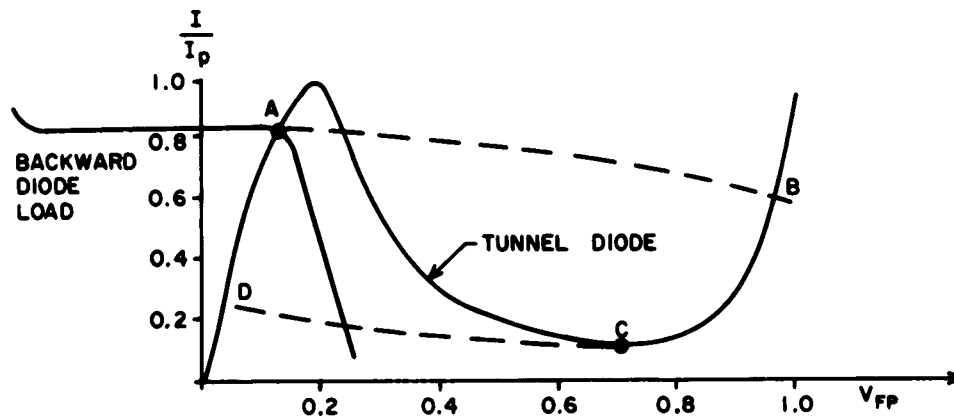


Figure 39. Normalized Plot of Tunnel Diode and Backward Diode and Load Line

(a) **TRANSIENT RESPONSE.** Before the rise and fall times can be calculated, a suitable choice of inductive time constant must be made. The tolerance requirement on the output voltage of the tunnel diode specifies that it must remain within a given percentage of its maximum value for the duration of the rise time of the succeeding stage. A long time constant is therefore desirable. On the other hand, this will give an excessively long recovery time which is undesirable for a high-speed system. An optimum is obviously reached when the output voltage changes from one end of its tolerance band to the other in the duration of the rise time,  $t_r$ .

For the purpose of this report, values will be assumed and on the basis of these assumptions, the recovery time will be calculated.

- 1) The rise time is 0.4 nsec for the 25-ma and the 50-ma tunnel diodes. This has been verified as quite practical from the standard calculation of rise time used previously. (Period A to B.)
- 2) The minimum time in the high state is 0.5 nsec. This ensures that the output current will be maintained within the tolerance for enough time to operate the reset stage. (Period B to C.)
- 3) The fall time is 0.317 nsec. This was calculated from the capacitive time constant only by the standard method previously outlined. (Period C to D.)
- 4) The recovery time is determined by the time constant  $L/R$  where  $L$  is 4 nh for the 50-ma stages and 8 nh for the 25-ma stages and  $R$  is the resistance of the backward diode of 1 ohm in series with the resistance of the tunnel diode in region 1 (0.8 ohm for 50-ma diode and 1.6 ohms for the 25-ma diode). The recovery time is 2.2 nsec per time constant for the 50-ma diode and 3.1 nsec per time constant for the 25-ma diode. (Period D to A.)

For the bias current to get within 90 percent of its original value, the order of 3 time constants is necessary for the recovery time.

On this basis, one complete cycle of the monostable circuit will take 7.8 nsec for the 50-ma diode and 10.5 nsec for the 25-ma diode.

(b) **COMPARISON WITH TRANSISTOR NOR CIRCUIT.** A comparison of tunnel diode high-speed logic circuits and transistor high-speed logic circuits can be made on the basis of the gain-bandwidth product expressed as:

$$F.M. = \frac{\text{fan-in} \times \text{fan-out}}{\text{switching time}}$$

Since extensive experimental data is available only on the monostable threshold logic circuitry, the comparison is made between that and the high-speed transistor NOR circuit. Table 6 shows a direct comparison where switching time is defined as the turn-on time of the tunnel diode circuit and the delay and rise time or saturation and fall time of the transistor circuit. This comparison emphasizes the fan-in and fan-out factors.

TABLE 6. FIGURE OF MERIT BASED ON RESPONSE TIME  
(DELAY & RISE)

Circuit	Fan-in	Fan-out	$t_d + t_r$	F. M. Max.
Monostable AND	2	3	0.56 nsec	10.72
Monostable OR	2	2	0.56 nsec	7.15
Monostable Inverter	2	2	4 nsec	1.0
Transistor NOR Circuit	10	10	12 nsec	8.34

The monostable circuit requires time to recover to the the initial bias point before which no logic can be performed.

Table 7 gives a Figure of Merit comparison where switching time is defined as the time required to switch the circuit and to provide recovery until another logical operation can be performed.

TABLE 7. FIGURE OF MERIT BASED ON RECOVERY TIME

Circuit	Max. Fan-in	Max. Fan-out	Switching Time & Recovery Time	F.M.
Monostable OR	2	3	8.36 nsec	0.72
Monostable AND	2	2	11.1 nsec	0.36
Monostable Inverter	2	2	11.8 nsec	0.34
Transistor NOR Circuit	10	10	10 nsec	10.00

In logical systems where large fan-in and fan-out is required, (such as decoding) comparison can be made by constructing the equivalent NOR circuit from the monostable building blocks. Discounting the limitation imposed by the monostable logic in that only pulse inputs to an OR gate are allowed, the NOR equivalent is shown in Figure 40. The total delay through the array (assuming cascaded delays are directly additive) is 17.33 nsec compared to 10 nsec for the transistor NOR circuit. In a logical array where only low fan-in and fan-out is required, such as a half adder shown in Figure 41 for the monostable circuit and Figure 42 for the transistor NOR circuit, the total delay using the



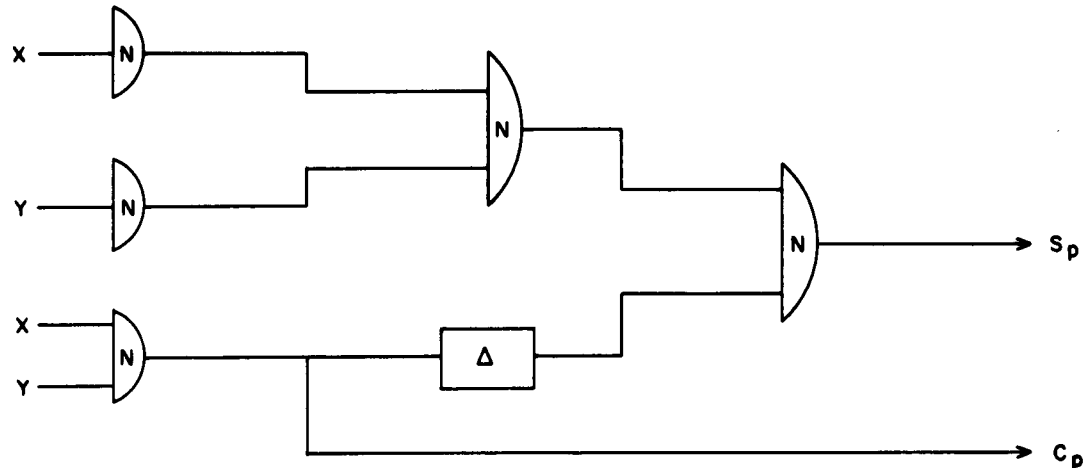


Figure 42. Half-Adder Using Transistor NOR Logic

monostable circuit, where the maximum number of pulse inputs to an AND gate is one, is 17.9 nsec including recovery time. The delay through the transistor NOR circuit is 18.9 for a delay or storage time per stage of 4 nsec and a rise or fall time per stage of 4 nsec.

In a logic array where a large number of stages are cascaded, the monostable tunnel diode technique can operate at higher speeds since the recovery time becomes a small portion of the total delay. However, the logical restrictions on the monostable system with respect to allowable pulse or level inputs and the operation of the bistable hinder full utilization of the switching speed of the tunnel diode. In an application where encoding and decoding of an eight-bit code and five cascaded logical operations (e.g., half adder) are used, the monostable tunnel diode logic will require 43.8 nsec (1.57 nsec/stage). For the application, the transistor NOR logic requires 106 nsec (6.25 nsec/stage). The comparisons of tunnel diode and transistor NOR logic do not consider the factors of cost, reliability, noise, tolerances, and layout, which can be evaluated only for a particular application.

(4) SUMMARY AND CONCLUSIONS. Analog threshold and balanced pair circuits were discussed in previous Project Lightning progress reports. These and the voltage mode, emitter-follower/tunnel diode, and monostable threshold circuits may be classified with respect to clocking mode and coupling devices.

Three clocking arrangements have been discussed. In the first type, the clocking source is used as a parallel input and the same order of magnitude of source impedance as the logical inputs as in the threshold circuitry. In the second type, the clock has a low source impedance and is used to switch the tunnel diode in conjunction with a high impedance logical input used to bias a balanced circuit. The third arrangement uses a series connection of the driving stage, the clock, and the output stage and the total driving impedance are determined by the coupling element.

The characteristics of the coupling device are also a primary factor in determining the power gain and the speed of tunnel diode logic. Resistors provide the most reliable, best specified and highest frequency coupling element. However, the reverse coupling causes low power gain and increases the tunnel diode driving impedance. Diode coupling reduces the reverse fan-out in the speed range where diode reverse recovery and diode capacitance are not appreciable. Higher power gain can be achieved in the appropriate speed range. With the lower driving impedances of the diode, the tunnel diode switching speed can be increased. Transistors are more limited than diodes in high-speed circuits and their d-c characteristics are the most difficult to specify. In the appropriate speed range, much higher power gain can be achieved.

Of the resistance coupled circuits, the analog threshold type uses relatively high impedance coupling to limit reverse fan-out and provides accurate threshold detection; consequently, low power gain and slower speed of response can be expected for a given tunnel diode type. The balanced pair circuit uses high impedance logic coupling, but the switching source is a low impedance clock and the speed of switching is determined by the lowest practical clock impedance that can be obtained and the tunnel diode time constants. The power gain is a function of the unbalanced circuit effects and mismatch between diodes. Diode coupling in threshold circuitry improves performance by reducing the reverse fan-out and lowering the drive impedance. In the voltage mode circuit, the diode coupling provides a very low impedance switching. The logical gain is severely limited, and the reverse recovery and diode capacitance limit the speed of response. In the transistor coupled circuits, the emitter-follower provides a low driving impedance for the tunnel diode switching. The source impedance must be sufficient to prevent d-c operation in the negative impedance region. The speed is limited by the transistor switching time, and the fan-out is limited by the emitter-base capacitance and the tight two-sided specifications required for the transistors.