MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

52 G - 1

A SOLID STATE BUFFER-MEMORY SYSTEM TO HANDLE RANDOMLY TRANSMITTED INFORMATION

Richard M. Horowitz

13 February 1962

The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology; this work was supported by the U. S. Air Force under Air Force Contract AF 19(604) - 7400.

LEXINGTON MASSACHUSETTS

plt-1350a

AFESD - TDR - 62- 69

This report is a condensation of a Thesis of the same title presented to the Graduate School of Northeastern University, in partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering.

Introduction

The digital data handling section in the West Ford receiver system performs the specific functions of temporarily storing and then transferring error and certain special data to a high speed magnetic tape unit for ultimate computer data processing. A fixed 16-bit binary word is repeatedly transmitted over the dipole channel. The returning bits of information are sequentially compared for errors with reproductions of the transmitted word. Discrepancies between the transmitted and received bits thus derived by comparison are assembled for subsequent storage and recording. In addition to the error word just mentioned, three other word types --- parameter, measurement and radar, each containing 96 bits of information pertinent to other aspects of the communication experiment, are also assembled for processing.

General System Function

The system is outlined in the block diagram (Figure 1). Incoming data from the West Ford receiver is compared serially with a preset toggle register. The results of this comparison are transferred to Register A. The presence of a "1" in Register A connotes an error in the particular words just received and sampled. Should a "1" exist in A, the ensuing three 16-bit words are channeled into Register B. B functions as a temporary store while other data such as time and word type identification tags (hereafter called "tag") associated with the particular word in error (stored in A), are determined and assembled. The assembly of these data, together

with the word in error occurs in the central core memory associated with this system. During the time that A may be filling with error data, one of the other possible word types mentioned previously may be assembled and stored in memory. When the memory has been nearly filled, its contents are transferred to magnetic tape for subsequent computer processing. The various operations described above occur under the control of the Master Control Counter (M) and its associated diode matrix. If desired, live data may be stored on tape, bypassing the comparison circuits and all other auxiliary information pertaining to other operational modes.

Error Detection

The normal mode of operation of the detection and storage system is in the "error" mode shown in Figure 2. In this mode each returning data bit, Q, is sequentially compared with the corresponding known transmitted bit, T, (of a 16-bit word) in a sum modulo 2 circuit. A "1" is placed in the particular bit position in which an error has occurred; a "0" signifies no error. These outputs are sequentially shifted into the data storage flip-flop shift register, A, 16 bits long. A check of A is made to determine the presence of an error by sampling the error detection circuit (F). When an error is detected, the contents of A together with the ensuing 48 bits are stored in memory. Tag and time associated with the error(s) detected in A are stored together with the word in error. A 29-bit flip-flop "ready register" is provided to store temporarily the time at which the first error in a word has been detected. At the time A is sampled, the time is

shifted in parallel into the ready register for use, if necessary.

An 8-bit data storage shift register, B, is used to store the continually incoming data while tag, time and the contents of A are transferred to memory.

A control flip-flop, E, channels the flow of information from A to B when an error has been detected in A. The next 48 bits (3 words) following a 16-bit word in which an error has been detected, are taken for storage from B in 6-bit groups each time B becomes full. At this time, an error word cycle has been completed and the data flow reverts to A.

Synchronization is maintained at the sum modulo 2 circuit between the incoming data and the known transmitted word stored in a toggle switch register by means of the input sample ring counter, C. The toggle register is sequentially sampled at the data clock rate B_C, by ring counter C and its associated diode nets (Figure 2).

Core Memory and Transfer to Tape

The control store for this system is a sequential access coincident current core memory having a capacity of 1092, 8-bit words. Information may be written in at a maximum rate of 100 kc. Interlacing of load and unload operation may reduce this rate to approximately 50 kc depending upon the length of the record to be loaded or unloaded. The memory may either load or unload a variable length block using 4 magnetic switches, two for the load cycle and two for the unload cycle. Each independent set, (load and unload pair) operated in ring counter fashion, consists of a 28 x 39

switch for the X and Y lines; each buffer load or unload pulse advances its respective switch by one. Clearing the memory resets these address registers to zero address; otherwise they remain at the address to which they were last pulsed.

Each tape record is of constant length, consisting of 864 6-bit words. This particular length and format was the result of the following considerations:

1. Compatibility with IBM tape units, consistent with the 16-bit word length (6 x 16n = 864).
2. Desirability of reasonably long records for purposes of tape economy.
3. Data, when entering at its fastest rate, should not overflow the memory during the interval that the tape unit is accelerating to recording speed or decelerating.

To insure a constant length record a buffer memory load pulse counter, P, counts 864 load pulses and inserts a "1" as a marker on the 7th memory input line. The counter also sets a tape control flip-flop, L_W, enabling the tape accelerate instruction to bring the unit to recording speed. When the "1" is read out of memory, it resets the tape control flip-flop initiating a stop tape machine instruction. It is only while L_W is set that information is transferred to the tape unit (See Figure 3).

Synchronization between the buffer memory and the tape unit is maintained with the use of a sync circuit which provides one synchronized buffer unload pulse for every "next word level" signal from the tape unit. The "next word level" also resets the memory

output register after each word has been transferred to tape.

The unique nature of the particular 6 bits selected for storage is determined by the Memory Input Selection Matrix. The details of this matrix are shown in Figure 4. The various inputs and their functions are defined in Appendix A.

Timing and Control

The central timing for the error word and special word cycles is handled by a 7 flip-flop series-parallel master control counter and AND matrices (Figure 5). The counter is allowed to count 68 states and is reset. Thirty-three of the possible 68 matrix outputs are used to perform logic functions in the system. The outputs M_0 through M_{67} are divided into 2 categories. M_0 through M_{16} are used when storing special words, and the counter does not cycle above M_{16} unless an error has been detected in A at time M_{16}. M_{17} through M_{25} and M_{31}, M_{38}, M_{44}, M_{51}, M_{57}, M_{63}, and M_{67} are used only during an error cycle. In this case, M_{67} resets the counter. The gaps between the last 7 matrix outputs used is due to the nature of the unloading of the B shift register; there is a delay of 6 bits (6 clock pulses) until B is full with data each time. The clock, D, for the master control counter is a function of B_C and P_S, the sync pulse. The clock D is available even if synchronization is lost, allowing the system to continue functioning.

The basic system clock is derived from a stable 1 mc oscillator. Counters are used to generate sub-multiples of this frequency to provide clock pulses at 100 kc, 10 kc, 1 kc and 100 cps (Figure 6).

Time, as recorded in this system, is obtained from a 29-stage serial counter, clocked at 5 kc. The counter may be preset by a set of switches (Figure 7).

Special words need be stored frequently enough to provide a continuous behaviour pattern of the parameters being measured. A 5 flip-flop serial counter and a "seconds between special word" switch determine the recording frequency of special words. The clock rate to this counter is 50 cps. The time between special words and their associated switch settings are shown below.

Switch Setting	Actual Time (second)
4	.64
8	1.28
16	2.56
32	5.12

Provision is made for assuring synchronization (W and M flip-flop sync circuit) between an incoming special word and the appropriate time for storing such word as determined by the Master Timing Control. (See Figure 8). With this sync circuit special words can be stored only during a specific interval in the error word cycle. The output of the sync circuit clocks a 3 flip-flop tag counter, which, together with code generating diode matrices and a 3-bit diode OR matrix, select and identify which of the three composite special words should be stored in that particular error word cycle. These OR gates have as inputs the radar code RC, the measurement code MC, and the parameter code PC (Figure 8 also). A 3-bit tag is stored

initially with every type of composite word to distinguish between the possible different types. For every complete cycle of the tag counter, the composite measurement word is stored 6 times, the radar word once and the parameter word once.

In the live mode, the live/error mode switch inhibits tag and time from being stored in the input selection AND gates (Figure 4). It also prevents the generation of the special word codes (Figure 5) as well as inhibiting the error detection AND gate, F, (Figure 2) preventing the master control counter from cycling above M_{16}. Returning live data by-passes the sum modulo 2 circuit and is stored directly in B. Corresponding to every 6 data bits a live word pulse, LW, is generated in a 3 flip-flop live word counter (Figure 9) to select this data for storage. This counter, clocked by B_C, is reset after counting to 6; it replaces the Master Control Counter for this operation. The live mode of operation involves only the B register, the live word counter and the memory.

Summary

The digital data handling section of the receiver system has been designed incorporating the following features:

1. Under no conditions must data be lost due to storage overflow. Sufficient temporary buffering must be provided while data is stored on tape.

2. The system must be inherently error free so that data received and compared is a function of the channel alone.

3. The tape records should be neat and compact. In this

system the tape unit is used only when a tape record is written. It does not operate in the error free intervals; therefore no tape or computer processing time is wasted.

4. Time and much auxiliary data is stored to make data evaluation more meaningful.

Using a simulated channel, a sample of the results obtained are shown in Figure 10. Each line is a composite word. The first 3 bits are tag, followed by 29 bits of time and 64 bits of data - either error or special.

Figures 11 through 14 illustrate portions of the system.

Appendix A

Referring to the Input Selection Scheme in Figure 4, the following notations have been used:

1. M_x (where $x = 0, 1, \ldots, 67$) $\equiv$ outputs of the Master Control Counter. Each of these outputs gate 1 six-bit word onto the 6 memory input lines.

2. $L_{1-6} \equiv$ 6 memory input lines.

3. LE $\equiv$ the live/error word switch. In the error mode (+ 5 v) it allows tag and time to be stored. In the live mode (- 5 v) it inhibits this data.

4. Tag 1, 2, 3 $\equiv$ the 3-bit word identification tag. Throughout the system, the most significant bit of information of a register or tag is stored first.

5. $R.R_{1-29} \equiv$ the ready register where time is temporarily stored prior to storage in memory.

6. $A_{1-16} \equiv$ the outputs of the 16-bit A shift register. This register contains the first error(s) of a 96-bit composite error word.

7. $B_{1-8} \equiv$ the outputs of the 8-bit auxiliary B shift register utilized while tag, time and the contents of A are being stored in memory. In B, the last 48 bits of a composite error word are briefly stored.

8. LW $\equiv$ the output of the live word counter. It is every sixth pulse from this counter which gates live word data onto the memory lines.

9. PC, RC, and MC ≡ the parameter, radar and measurement word codes, respectively. Only one can be set high (+ 5 v) at one time. Therefore, only one of the three types of words can be stored during a portion of the error word cycle.

10. PB_{33-96}, RB_{33-96}, MB_{33-96} ≡ the data bits of the parameter, radar and measurement words, respectively. They occupy bits 33 through 96 of a composite special word.

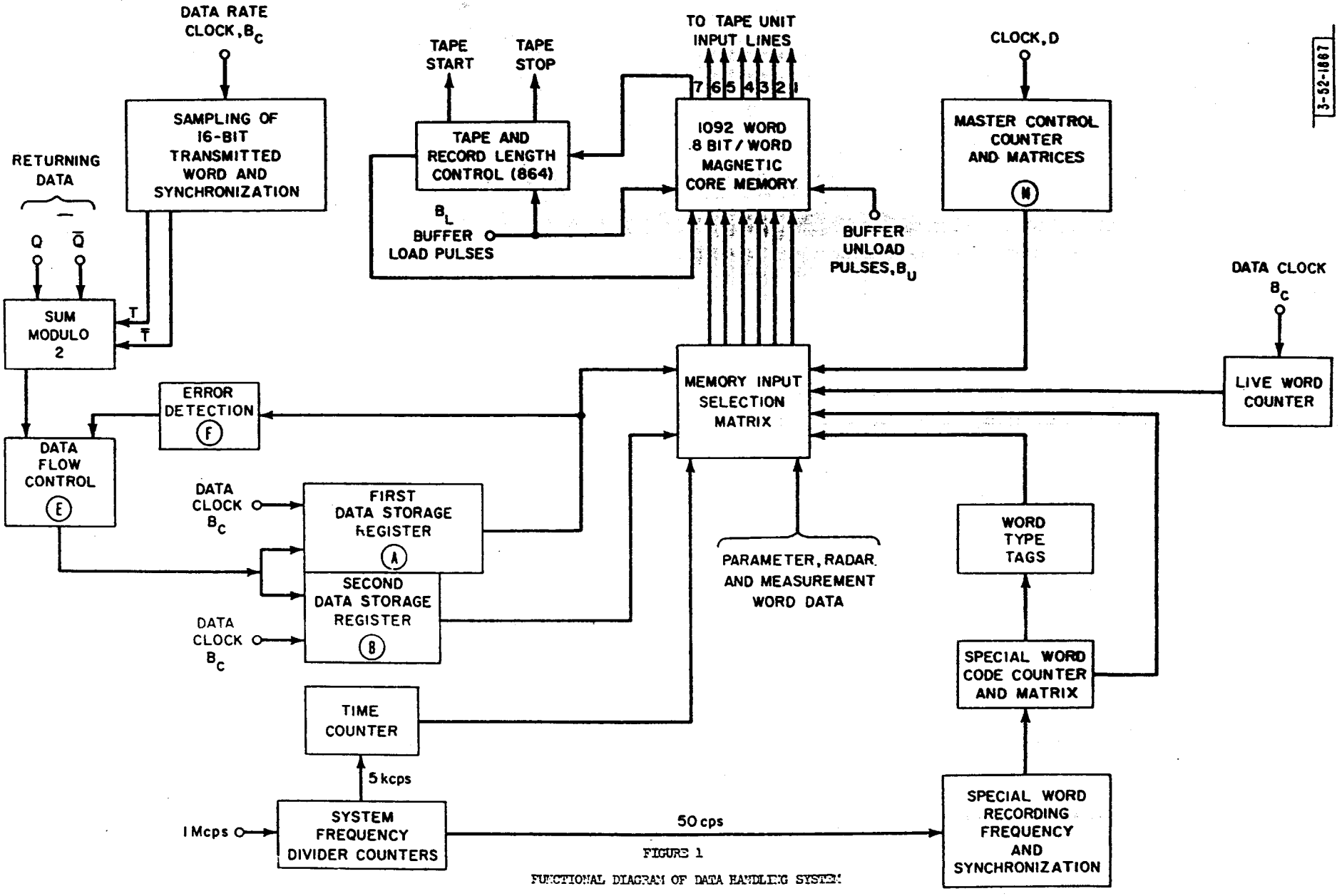
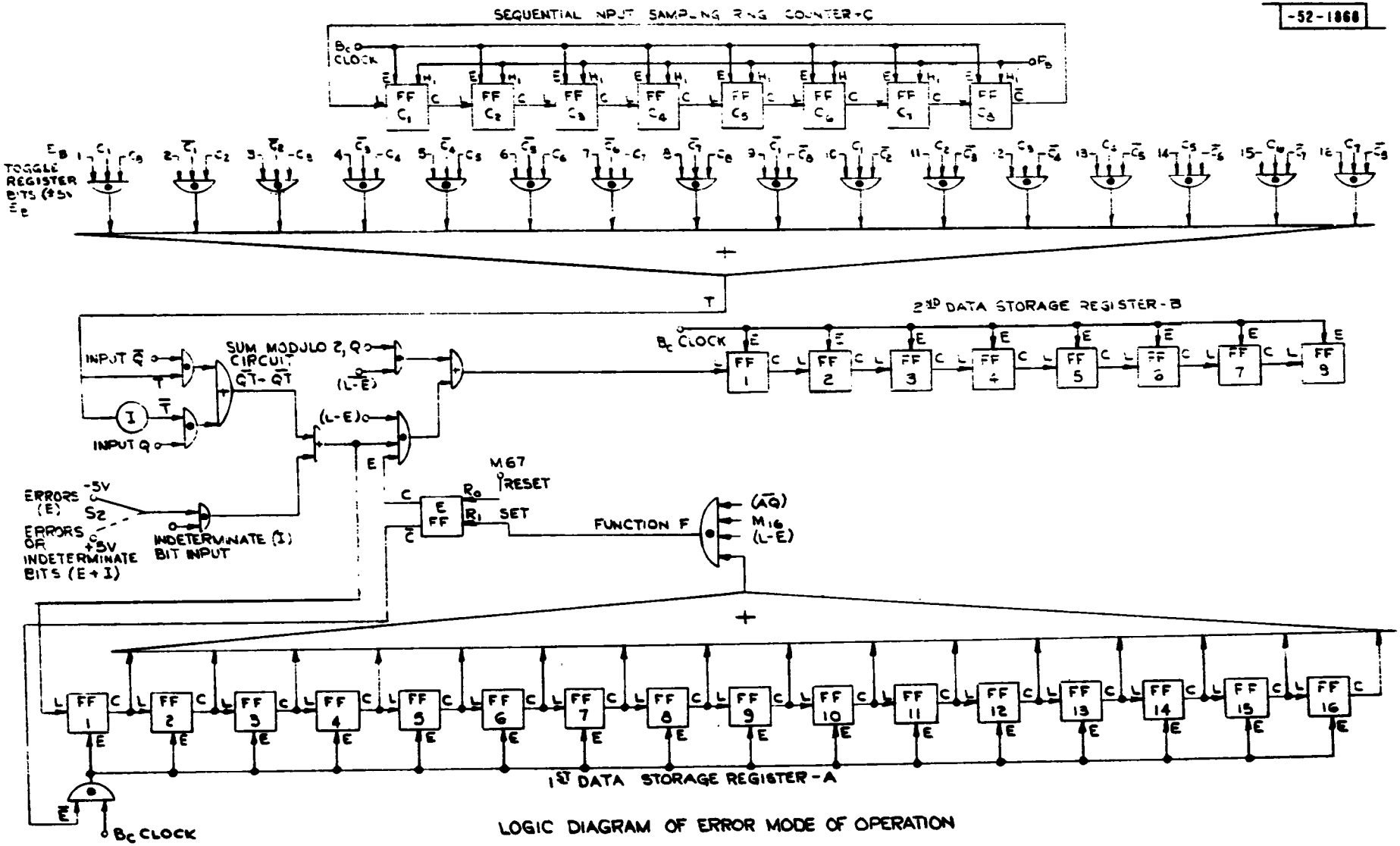


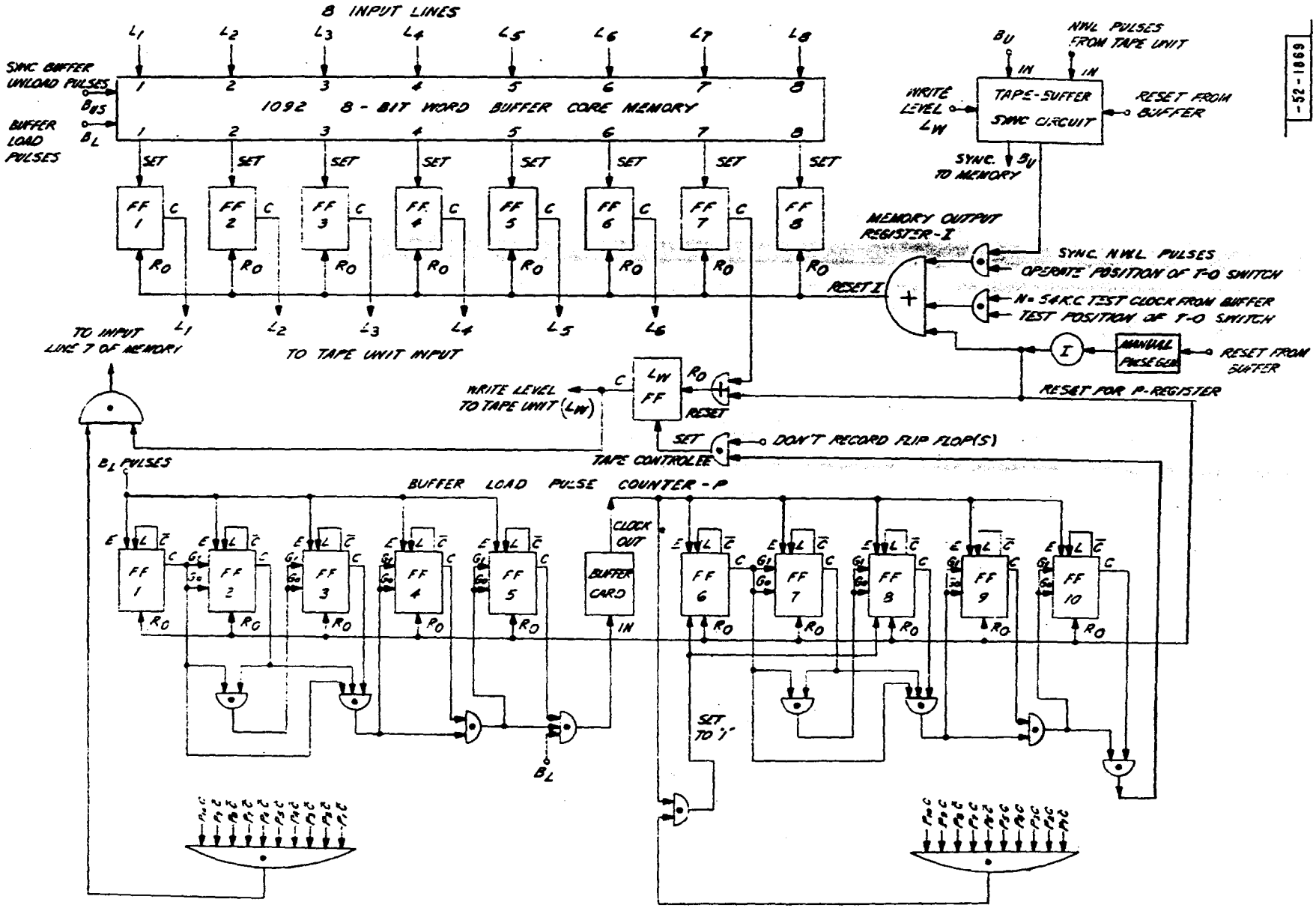
FIGURE 1

FUNCTIONAL DIAGRAM OF DATA HANDLING SYSTEM



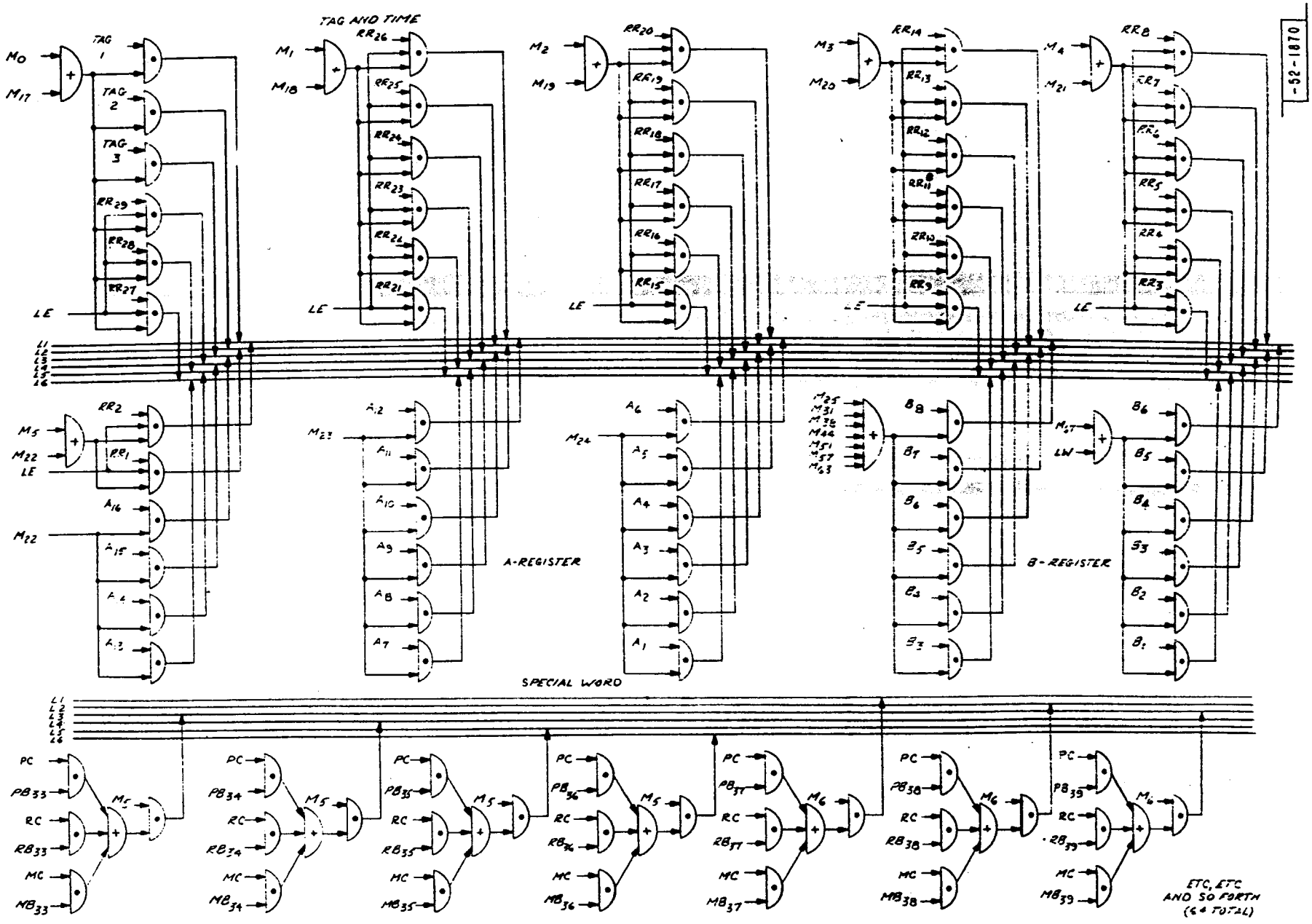
LOGIC DIAGRAM OF ERROR MODE OF OPERATION

Figure 2



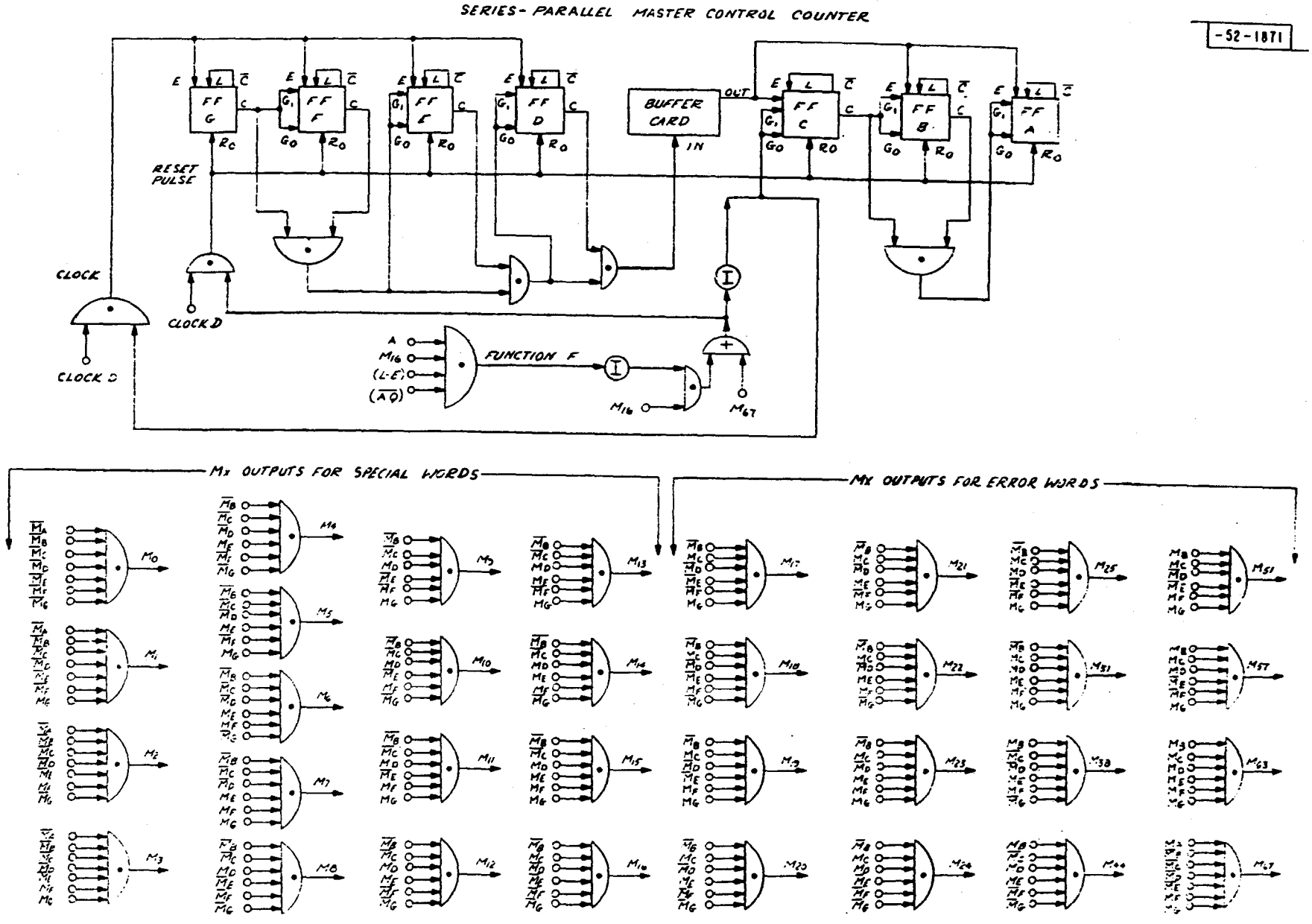
LOGIC DIAGRAM OF BUFFER CORE MEMORY ASSOCIATED ELECTRONICS

Figure 3



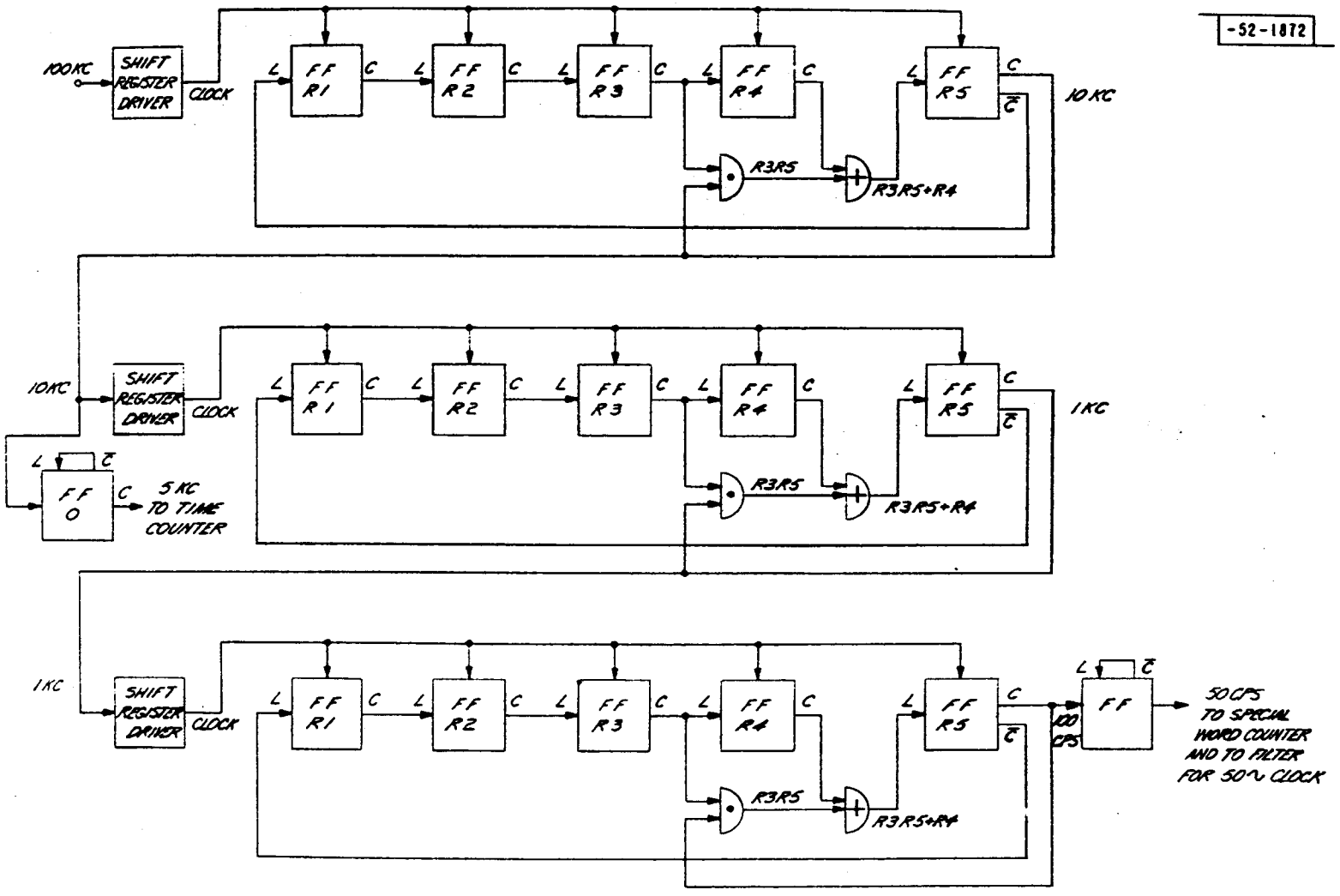
INPUT SELECTION SCHEME FOR ERROR, SPECIAL AND LIVE WORDS

Figure 4



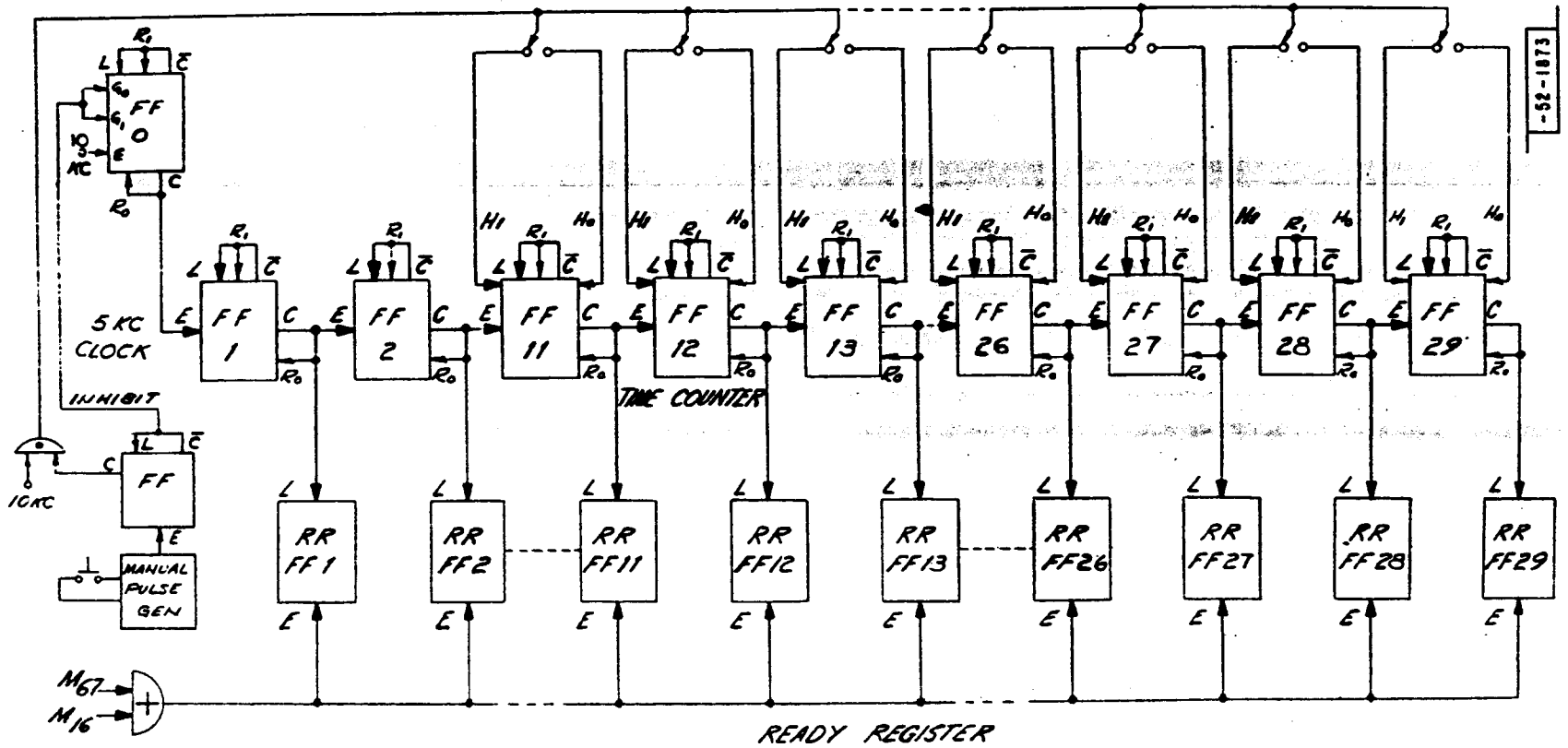
LOGIC DIAGRAM OF MASTER CONTROL COUNTER AND MATRICES (M_0 - M_{67})

Figure 5



LOGIC DIAGRAM OF 3 TIME RING COUNTERS

Figure 6

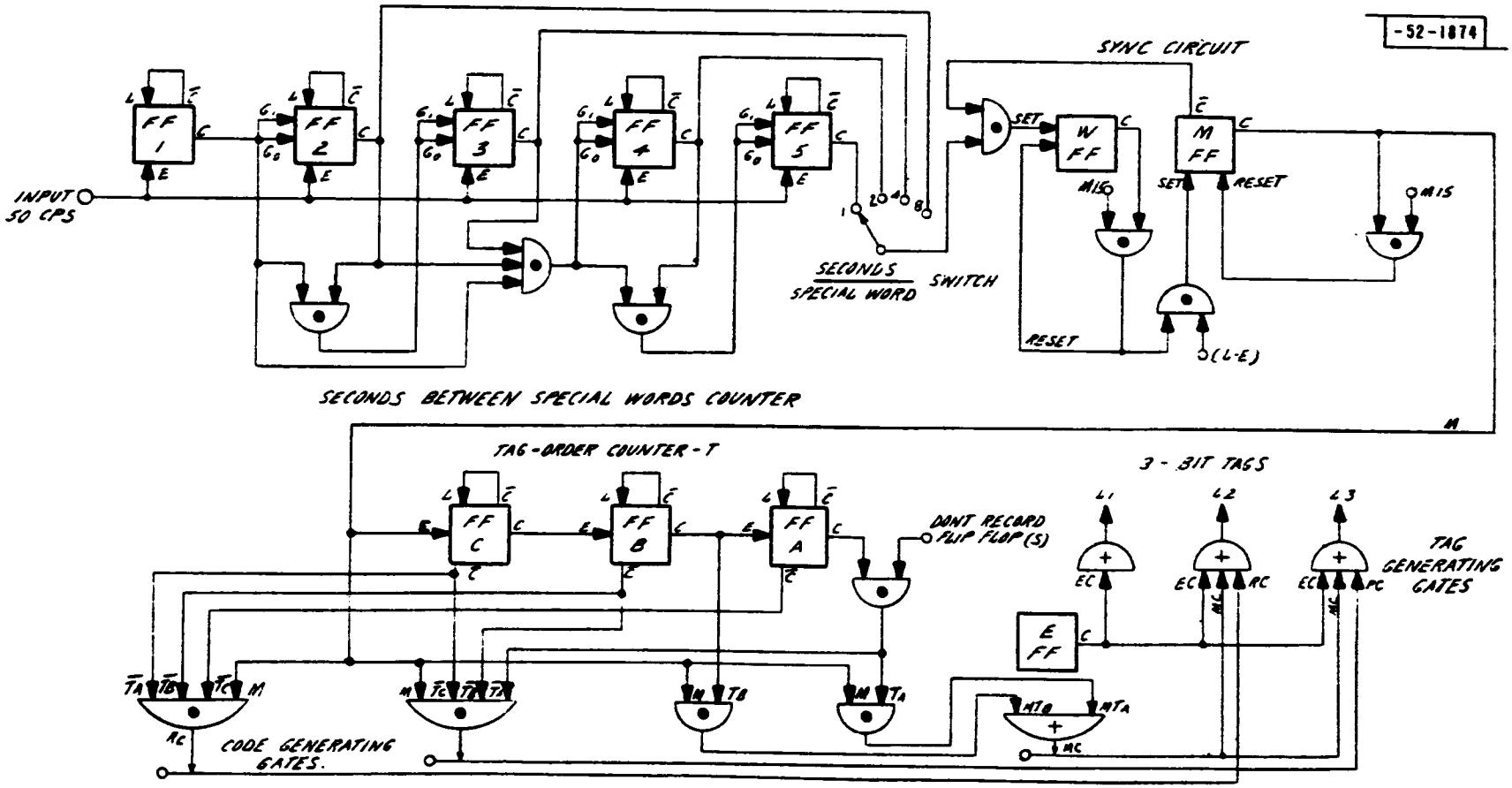


FLIP-FLOP CONNECTIONS:

E - CLOCK INPUT
L - LOGIC INPUT
R_1, H_1 - SET TO "1" INPUT
R_0, H_0 - SET TO "0" INPUT
C, $\bar{C}$ - OUTPUTS

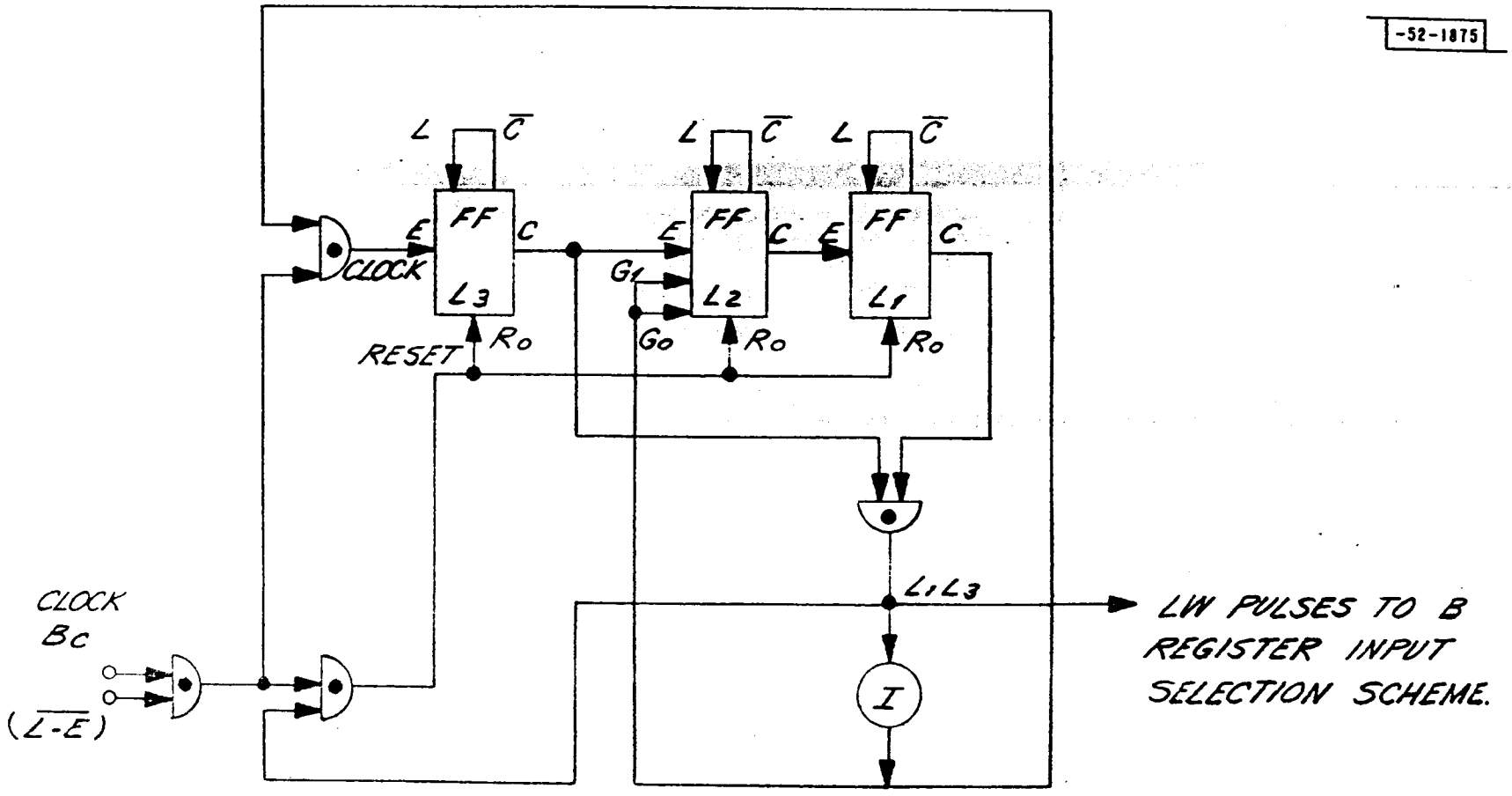
LOGIC DIAGRAM OF TIME COUNTER AND READY REGISTER

Figure 7



HANDLING OF SPECIAL WORDS IN WEST FORD.

Figure 8



LOGIC DIAGRAM OF THE LIVE WORD COUNTER

Figure 9

TAG	TIME	ERROR DATA OR SPECIAL WORD INFORMATION				
111	0100000010111111011100001111	0000 000000 000001	[illegible]	[illegible]	[illegible]	[illegible]
111	0100000010111111011111110110101	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111100011000011011	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111100110100000010	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
011	0100000010111111101000010100000	1111 111010 111111	111111 111111 1111	11 010000 000111 01	0110 000000 000111	
111	0100000010111111101001111101000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111101011001111	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111100010110101	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111101000011011	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
011	0100000010111111101001101011	1111 111010 111111	111111 111111 1111	11 010000 000011 10	1011 000000 000100	
111	0100000010111111101111000010	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111101011101000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000010111111111001001111	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
011	0100000011000000000101001111	1111 111010 111111	111111 111111 1111	11 010000 000011 10	1010 000000 000011	
111	0100000011000000000110110101	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000001010001011	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000010001000010	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000010111101000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
001	0100000011000000011011010010	1000 111111 111111	011111 001001 0101	11 111111 000000 11	0100 000000 011001	
111	0100000011000000011110100111	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000010010101101	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000010110000011	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000000011001100000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
011	0100000011000000011010010011	1111 111010 111111	111111 111111 1111	11 010000 000111 01	0110 000000 001000	
111	0100000011000000011100111101000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000001000000100111	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000001000011101101	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
011	0100000011000001001	1111 111010 111111	111111 111111 1111	11 010000 000011 10	1011 000000 000011	
111	0100000011000001001110011011	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000001010101000010	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	
111	0100000011000001011011111001000	0000 000000 000001	000000 000000 0000	00 000000 000000 00	0000 000000 000000	

Figure 10 Data Taken From Early Experimental Run

Figure 11 Photograph of West Ford Receiver System

Figure 12 Portion of West Ford Covered in the Thesis

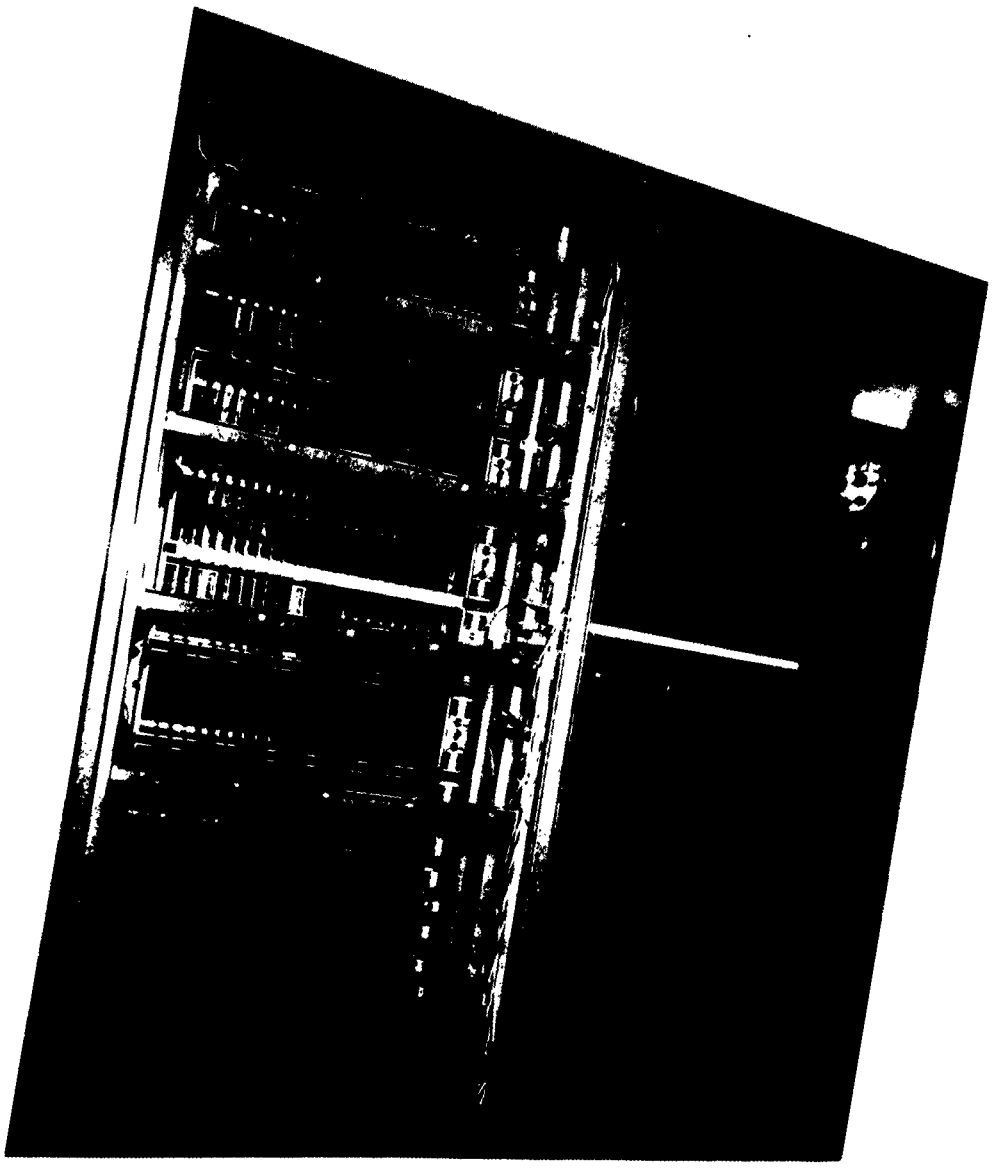


Figure 13 Rear View of Doors Containing Plug-In-Type Cards

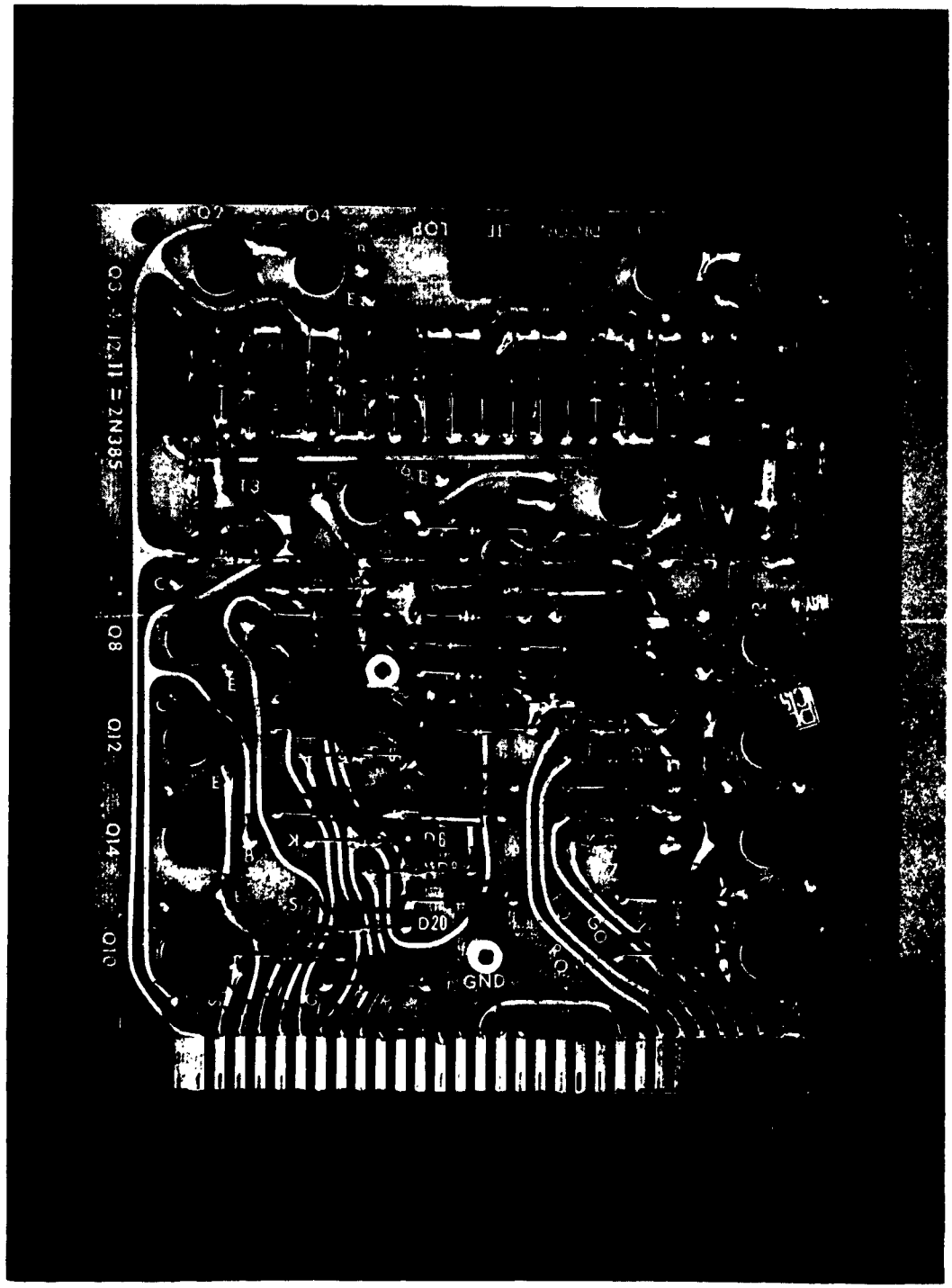


Figure 14 Typical Card Used in the System--Flip Flop