63-1-5

FINAL ENGINEERING REPORT

on

DETERMINATION OF REQUIREMENTS FOR OVERVOLTAGE AND OVERLOAD PROTECTION OF TRANSISTORS

to

BUREAU OF SHIPS

December 9, 1960

by

H. T. Gruber and S. T. Klapp

BATTELLE MEMORIAL INSTITUTE
505 King Avenue
Columbus 1, Ohio

January 6, 1961

Chief, Bureau of Ships
Department of the Navy
Main Navy Building
Washington 25, D. C.

Attention Code 691B2

Dear Sir:

Contract No. NObsr-77579

This is the Final Engineering Report on the project entitled "Determination of Requirements for Overvoltage and Overload Protection of Transistors". This report covers the period from May 20, 1959, to December 9, 1960.

The objective of this project was to determine the design requirements for transistor protective devices. The objectives of the project were to have been achieved by conducting a survey of information from transistor manufacturers and transistorized-equipment manufacturers. Shortly after the survey was started, it became apparent that the survey would not supply all of the desired answers required to achieve the objectives of the project. It was reasoned that the necessary design requirements for transistor protective devices were defined by the capabilities of the transistors to withstand transient pulses. These transistor capabilities were accordingly determined by means of a study of thermal operation of the transistors. In the course of this thermal study, a transistor thermal analog was developed for the purpose of obtaining data which would be useful to an equipment designer.

The original project objective was then expanded and additional funds were supplied for conducting experimental work to verify the results obtained from the transistor thermal analog.

All of the project work has now been completed, and the results are presented in this report. One microfilm copy of the engineers' notebook, which contains all of the raw data from the project and copies of all calculations performed, is being sent under separate cover.

It should be noted that the transistor thermal analog developed to achieve the objectives of the project also has far-reaching capabilities as a circuit-design tool. This aspect should not be overlooked.

Very truly yours,

H. T. Gruber
Reliability Engineering Division

HTG:nb
Enc. (9)

DISTRIBUTION LIST

Advisory Group on Electronic
Parts (3 copies)
103 Moore School
200 South 33rd Street
Philadelphia 4, Pennsylvania

Commanding Officer (1 copy)
Diamond Ordnance Fuze Laboratory
Attention Mr. W. M. Piper
Washington 25, D. C.

Chief, Bureau of Ordnance (2 copies)
Department of the Navy
Room 4203 - Main Navy Building
Attention Mr. R. P. Biglow
Washington 25, D. C.

Chief, Bureau of Aeronautics (2 copies)
Department of the Navy
Room 1W29 - Main Navy Building
Attention Mr. D. Knapp
Washington 25, D. C.

Commander (2 copies)
Wright Air Development Center
Attention Mr. I. S. Mayer, WCLKM-2
Wright-Patterson Air Force Base, Ohio

Canadian Joint Staff (1 copy)
2450 Massachusetts Avenue, N. W.
Attention Defence Research Member
Washington 8, D. C.

Commander (1 copy)
Rome Air Development Center
Griffiss Air Force Base
Rome, New York

Commander (3 copies)
New York Naval Shipyard (Material
Laboratory)
Attention Code 933
Brooklyn 1, New York

Commanding General (2 copies)
U. S. Army Signal Research and
Development Laboratory
Attention Mr. W. J. Fontana
SIGFM/EL-PEE
Fort Monmouth, New Jersey

Chief, Bureau of Ships (8 copies plus 1 reproducible)
Department of the Navy
Main Navy Building
Attention Code 691B2
Washington 25, D. C.

Mr. C. G. Jacobsen (1 copy, letter only)
ONR Resident Representative
The Ohio State University Research
Foundation
1314 Kinnear Road
Columbus 8, Ohio

TABLE OF CONTENTS

DETERMINATION OF REQUIREMENTS FOR OVERVOLTAGE AND OVERLOAD PROTECTION OF TRANSISTORS

by

H. T. Gruber and S. T. Klapp

INTRODUCTION

Operational requirements for military equipment demand that such equipment operate reliably, occupy a small space, be of minimum weight, and consume a minimum of power. For these reasons, extensive use is being made of transistors in military electronic equipment. But, no matter how well the transistors are designed and manufactured, they must be operated within their capabilities and protected from various transient overload conditions if reliable operation is to be achieved. Maintaining ideal operating conditions for transistors is difficult under laboratory and ground-base operating conditions, and under mobile and extreme environmental conditions the problem is amplified many orders of magnitude.

Years of experience with vacuum tubes has taught us how to protect vacuum tubes against unusual operating conditions, and, in addition, the vacuum tube is generally a more rugged device than the transistor with respect to electrical misuse and thermal environments. The use of the transistor has grown much more rapidly than the use of the vacuum tube, and as a result, there is a lag in the state of knowledge about the use and reliable application of transistors.

OBJECTIVE OF THE PROJECT

The objective of this project is to determine the design requirements for transistor protective devices. The exact nature of the protective devices is not to be determined as they may be either additional devices incorporated in the circuit, additional protective circuits, or the proper choice of the basic circuit parameters. What are desired are discrete values of voltage, current, power, time constants, and any other necessary parameters that an equipment designer might readily use.

GENERAL OUTLINE OF THE PROJECT WORK

The thinking at the beginning of the project was that the necessary information might be obtained from transistor manufacturers, transistorized equipment manufacturers, and the equipment users. Accordingly, a survey was planned and started to obtain this information.

The designers of transistorized equipment are aware of the need for protecting the transistors from transient overload. However, the equipment designers do not know specifically to what level the transistors must be protected. Along these lines, the manufacturing concerns have set up company procedures which call for derating of the transistor parameters from 50 to 90 per cent of rated values. They know that in many cases the safety margin thus obtained in probably more than is necessary, but lacking detailed information they prefer to play it safe. This procedure results in increased equipment costs, complexity, and weights that are higher than necessary. In some cases it is thought that the increased complexity may even reduce the reliability of the equipment. Here, engineering "judgment" plays an important part in the equipment design.

It is generally felt throughout the industry that present transistor specifications are not sufficient to completely describe the transistors. The present 2N type designations describe the transistor at 25 C, whereas transistors from two manufacturers with the same 2N number may be entirely different at elevated temperatures. These differences may be large enough to cause equipment malfunction or failure when a transistor is replaced by a transistor of the same 2N type but manufactured by a different company. This condition has led to user specifications which in effect name the manufacturers of the transistors to be used. All agree that this is a poor state of affairs.

The equipment designers are requesting additional thermal information on transistors such as thermal time constants. Many manufacturers presently supply thermal resistances from the transistor junction to the mounting base or case, but this figure is useful only for d-c operation or linear derating with increased ambient operating temperatures. Work done on this project has indicated that even thermal time constants do not sufficiently describe the transistor for high-reliability circuits. The thermal response of transistors is a convergent, infinite, exponential series which has very short initial rise times, of the order of microseconds, and long tails on the response characteristics, of the order of from 1 to several hundred seconds. What are needed are data describing the shape of the thermal response and not just the time constant.

There are several methods by which the necessary thermal-response information may be obtained but the most practical method is the experimental determination of the transistor-junction thermal response and the use of a transistor thermal analog for the solution of specific design problems.

The basic approach of the experimental work performed as part of this project is sound, but experience gained concerning the thermal operation of transistors has indicated that the experimental technique must be refined to obtain more accurate results. The experimental procedure used during this project gave an adequate description of the thermal response of transistor junctions 1 millisecond after the power was removed from the transistor. A refinement of the experimental equipment is needed which will give a more accurate description of the thermal response of transistors during the first millisecond. It is desirable that this description be complete from the time after the first 10 microseconds. When this information is available, it will be possible to construct much more accurate transistor thermal-analog networks. Recommendations for specific refinements of the experimental technique and equipment are given in Appendix E.

The transistor thermal analog constructed for use of this project is technically sound. Experience gained during the course of the project has indicated that the equipment must be further refined to improve the accuracy of the results attainable.

The results from the transistor thermal analog, presented in Appendix B of this report, are useful to a limited extent. The inaccuracies produced by errors in the network representing the transistors, and errors of the same nature encountered in the experimental work intended to verify the results of the transistor thermal analog, make it impossible to place any figure of merit on the results obtained from the transistor thermal analog. It is the opinion of the persons operating the transistor thermal analog and performing the experimental work that derating 50 per cent from the analog results should result in reliable transistor operation and reasonable definition of the design parameter for transistor protective devices.

The following recommendations are made as a result of the work performed on this project.

(1) More adequate transistor specifications are required, such as specifications which describe transistor operation at several temperatures rather than the present 25 C only.

(2) Transistor manufacturers should supply more thermal information about their products. The increased cost would be outweighed by the more reliable transistor operation that would result.

(3) Further work should be performed for the express purpose of designing the equipment necessary to determine accurately the thermal response of transistor junctions. Once this equipment has been designed, the cost of reproducing the equipment should be nominal to the extent that transistor manufacturers might supply the thermal-response information on the transistors.

(4) Further work should be performed for the express purpose of designing the equipment necessary for a more accurate transistor thermal analog. Once this equipment has been designed, construction costs would be nominal and transistorized equipment manufacturers might use the transistor thermal-analog techniques to improve the reliability of their equipment. This analog technique would certainly be less expensive than some of the techniques presently being used to produce very reliable transistor equipment.

PROJECT WORK

Survey of Equipment Manufacturers

Questionnaire

A questionnaire was sent to manufacturers of transistorized equipment recommended by the Bureau of Ships. The purpose of this questionnaire was to obtain specific data from which the requirements of protective devices for transistors might be determined. In order to obtain the maximum use of the experience and thinking of these manufacturers, it was pointed out that, if in their judgment the type of information being

The designers of transistorized equipment are aware of the need for protecting the transistors from transient overload. However, the equipment designers do not know specifically to what level the transistors must be protected. Along these lines, the manufacturing concerns have set up company procedures which call for derating of the transistor parameters from 50 to 90 per cent of rated values. They know that in many cases the safety margin thus obtained in probably more than is necessary, but lacking detailed information they prefer to play it safe. This procedure results in increased equipment costs, complexity, and weights that are higher than necessary. In some cases it is thought that the increased complexity may even reduce the reliability of the equipment. Here, engineering "judgment" plays an important part in the equipment design.

It is generally felt throughout the industry that present transistor specifications are not sufficient to completely describe the transistors. The present 2N type designations describe the transistor at 25 C, whereas transistors from two manufacturers with the same 2N number may be entirely different at elevated temperatures. These differences may be large enough to cause equipment malfunction or failure when a transistor is replaced by a transistor of the same 2N type but manufactured by a different company. This condition has led to user specifications which in effect name the manufacturers of the transistors to be used. All agree that this is a poor state of affairs.

The equipment designers are requesting additional thermal information on transistors such as thermal time constants. Many manufacturers presently supply thermal resistances from the transistor junction to the mounting base or case, but this figure is useful only for d-c operation or linear derating with increased ambient operating temperatures. Work done on this project has indicated that even thermal time constants do not sufficiently describe the transistor for high-reliability circuits. The thermal response of transistors is a convergent, infinite, exponential series which has very short initial rise times, of the order of microseconds, and long tails on the response characteristics, of the order of from 1 to several hundred seconds. What are needed are data describing the shape of the thermal response and not just the time constant.

There are several methods by which the necessary thermal-response information may be obtained but the most practical method is the experimental determination of the transistor-junction thermal response and the use of a transistor thermal analog for the solution of specific design problems.

The basic approach of the experimental work performed as part of this project is sound, but experience gained concerning the thermal operation of transistors has indicated that the experimental technique must be refined to obtain more accurate results. The experimental procedure used during this project gave an adequate description of the thermal response of transistor junctions 1 millisecond after the power was removed from the transistor. A refinement of the experimental equipment is needed which will give a more accurate description of the thermal response of transistors during the first millisecond. It is desirable that this description be complete from the time after the first 10 microseconds. When this information is available, it will be possible to construct much more accurate transistor thermal-analog networks. Recommendations for specific refinements of the experimental technique and equipment are given in Appendix E.

The transistor thermal analog constructed for use of this project is technically sound. Experience gained during the course of the project has indicated that the equipment must be further refined to improve the accuracy of the results attainable.

sought could be supplied better in some other form, the person answering the questionnaire should feel free to deviate from the questionnaire. A list of the questions from the questionnaire is given below, with the spaces for answering the questions omitted.

"The purpose of this questionnaire is to obtain data from which the requirements for protective devices for transistors may be determined. If the answers to the questions involve classified information, indicate only that the information is classified. Feel free to deviate from the questionnaire whenever in your judgment the type of information being sought can be supplied better in some other form. It is necessary that we have the benefit of your experience and thinking. The source of all information will remain confidential.

Please use additional sheets of paper where necessary and reference the answers to the question number. Please return the completed questionnaire by January 15, 1960, to:

H. T. Gruber
Battelle Memorial Institute
505 King Avenue
Columbus 1, Ohio

(1) The name of your company.

(2) The department in which you work.

(3) Your name and title.

(4) What types of transistors do you use in the equipment you manufacture and what are the applications of these transistors?

(5) Do you consider transistors a problem?

(6) What types of transistor failure or malfunctions have you experienced? (Please indicate failure details, probable cause of failure, levels of voltage or current causing failure, and electrical and environmental conditions associated with the failure.)

(7) What types of mechanisms do you use to protect individual transistors?

(8) What types of mechanisms do you use to protect combinations of transistors? (For example, series or parallel combinations of transistors directly connected.)

(9) How effective have these mechanisms proven and what level of overstress will override the protective mechanism?

(10) (a) What types of protective mechanisms do you provide against surges produced by external devices such as radio transmitters and radars?

(b) What types of protective mechanisms do you provide against electromagnetic radiation from relays and switches, both external and within the equipment?

(11) What line-voltage variations and surges will your equipment tolerate?

(12) Are the transistors you use preselected and, if so, by what criteria?

(13) Do you derate the transistors and, if so, how much and by what criteria?

(14) What types of heat sinks do you use and how are the heat-sink requirements determined?

(15) What type of information do your designers find useful for the reliable application of transistors?

(16) What types of information would your designers like to have for the reliable application of transistors?

Please add any additional information on the reliable application of transistors. Your thinking and experience will be of great assistance to the Bureau of Ships."

Results From the Questionnaire

The methods of protecting transistors, as indicated by the returned questionnaires, are specific to the application. The major need of equipment designers is additional information about the transistors themselves. Much of this information is of the type that should be supplied by the manufacturer of the transistor. The manufacturers of transistorized equipment are aware of the importance of thermal considerations in the design of their equipment, but more thermal information about transistors is required in such a form as to be generally usable for many applications.

The following is a summary of the answers from the returned questionnaires. The first four questions have been omitted since these questions supply information used only to sort out the returned questionnaires. Where possible, the answers have been summarized. Some information returned with the questionnaires is presented because it was felt that this information should be valuable to the Bureau of Ships in the preparation of equipment specifications.

"In particular, the operating characteristics... are required... over the normal military temperature range. This is not given... even for transistors listed in MIL Standard 701."

"Maximum tolerable neutron irradiation for 3db permanent gain loss might also be of interest."

"There may be no way out of this, but one of our problems is the expense of the approved types BuShips insists on. An allowance for equivalent or replacement types would often help out the cost situation."

Question Number 5 was: Do you consider transistors a problem? At one end of the scale we have the answer that "when applied with reasonable care........ (transistors)...... are no more a problem than any other circuit component". Three of the seven replies stated that the specifications (especially military) are poorly defined and incomplete. Other problems with transistors are:

(1) Insufficient design data

(2) Poor availability of approved types

(3) Current drift because of temperature

(4) Fast thermal time constants

(5) Breakdown voltages too low

(6) Wide variation of characteristics over extended temperature ranges

(7) Poor vendor quality control

(8) Extensive testing required to select transistors for extremely low- and high-temperature operation.

Question Number 6 was: What types of transistor failures or malfunctions have you encountered? One of the major causes of failures listed in the returned questionnaires (and learned from personal contacts) was accidental overload caused by shorting load resistors (particularly emitter follower circuits) or the applications of excessive voltages through test probes during maintenance. Failures because of moisture leaking into the transistor case seem to be common. It was pointed out that failure within specific temperature ranges resulted from dew-point problems within the transistor case. Thirty per cent failures of 2N167 at temperatures below 0 C, and 50 per cent failures of 2N333 because of high leakage current at temperatures above 40 C (total number of transistors involved was not given) were reported. Failures because of inductive voltage spikes from the circuits were reported, but no voltage or current values are available (the trouble is corrected and the magnitudes involved are ignored). Thermal-runaway failures were also reported. There were no avalanche failures reported, and because of the close relationship with thermal runaway there is a possibility that the avalanche-type failure was not recognized.

Question Number 7 was: What types of mechanisms do you use to protect individual transistors? The answers received may be summed up by the following listing:

(1) Diodes to limit collector voltages

(2) Stabistors to limit base-emitter voltages

(3) Fuses for large power transistors

(4) Emitter resistors

(5) Design circuits for worst-case power dissipation

(6) Line filters to limit transients

(7) Conservative circuit design

(8) Thermistors to prevent thermal runaway

(9) Thyristors to prevent overvoltage

(10) Output-circuit series resistors (emitter follower circuits)

(11) Circuits to pull the transistor into saturation with loss of plus voltage.

Question Number 8 was: What types of mechanisms do you use to protect combinations of transistors? The answers to this question were the same as the answers to Question Number 7, with the additional use of separate emitter resistors in the case of parallel drivers to insure splitting of the load, and the use of matched current-gain transistors.

Question Number 9 was: How effective have these protective mechanisms proven? The answers ranged from "apparently 100 per cent" to no answer because of lack of data.

Question Number 10 was: (a) What types of protective mechanisms do you provide against surges produced by external devices, and (b) what types of protective mechanisms do you use to provide against electromagnetic radiation from relays and switches? In most cases the equipment is within metal cabinets and all interconnecting cables are shielded. This is to keep radiation in as much as it is to keep radiation out. Line filters and voltage-limiting devices are used to limit transients from the power sources. Shielding is used to control radiation from devices within the equipment, and switches and relays have arc-suppression circuits. The best protection is good circuit design and good layout.

Question Number 11 was: What line-voltage variations and surges would your equipment tolerate? The answers to this question varied from 2 per cent to 20 per cent. In most cases the contract for the construction of the equipment specifies the line-voltage variation which must be tolerated. Battery-operated equipment usually must be capable of tolerating considerable battery-voltage variation caused both by aging and temperature variation.

Question Number 12 was: Are the transistors you use preselected and, if so, by what criteria? The answers ranged from "generally not" to selection on specific parameters (beta, I_{co}, gain, low-temperature characteristics, breakdown voltage) which are dependent on the specific circuit application.

Question Number 13 was: Do you derate transistors and, if so, by what criteria? The answers, with one exception, were that derating is used. The derating factors given were:

(1) 70 per cent of rated power and voltage

(2) 65 to 90 per cent of rated junction temperature

(3) 50 per cent for all parameters

(4) Variable amounts depending on the application and operating conditions.

No reasons were given for the magnitudes of these derating factors. The answer is probably engineering judgment.

Question Number 14 was: What types of heat sinks do you use and how are the heat-sink requirements determined? The answers ranged from mounting the transistors on the heavier chassis structural members to cooling fins and forced air, determined experimentally for the specific application.

Question Number 15 was: What type of information do your designers find useful for reliable application of transistors? The answers to this question were summed up by the tables of Figures 1 to 5 which were supplied as an answer to one questionnaire. In addition to this, characteristic curves and thermal information are found useful. One answer included "end of life characteristics".

Question Number 16 was: What types of information would your designers like to have for reliable application of transistors? Some of the parameters listed for Question Number 15 are not available for all transistor types. Thermal characteristics are needed. The table of Figure 6, which was received with one of the returned questionnaires, indicates areas of missing or incomplete specifications that equipment designers would like to have.

The additional comments from the returned questionnaires are given below. These comments are valuable in that they indicated the areas of insufficient information and indicated the general feelings of six manufacturers of military equipment.

> "In no case should the base or emitter be connected to the case of the transistors. Only in cases where actual dissipations are affected should collectors be tied to the case. Several expensive transistors have been lost during developmental work by not noting that the emitter was connected to the case."

> "As a general rule, most semiconductors failures can be averted if the maximum junction temperature (power) is never exceeded. This may be accomplished by suitable current limiting in the event of an input voltage surge to line transients, or high power coordination from radars or transmitters. This is not always easily done if high efficiency circuits are required; however, few, if any, electrical failures will be encountered if circuits are designed such that semiconductors are never allowed to exceed their maximum junction temperature and tolerate the widest parameter variations specified by the semiconductor manufacturer."

Two Approaches to the Thermal Study of Transistors

From the returns of the questionnaire given in the previous section, it is seen that there is considerable information available concerning the protection of transistors, but this information is specific with respect to the transistor type, the application of the transistor, and many other factors concerning individual pieces of equipment. In order to comply with the objectives of the project, it was necessary to try some other approach to the problem so that the resulting information might be generally applicable to many different transistor applications.

The material presented in this section follows the chronological progress of the project. This method of presentation is being used because if is felt that the reader will get a more complete understanding of the problems involved.

General Purpose and Audio Amplifiers

Maximum Ratings

Symbol	P_c	BV_{CEO}	BV_{CER}	BV_{CBO}	BV_{EBO}	I_{Cmax}	I_{Bmax}	I_{Emax}	T_{jmax}	T_{opg}	T_{stg}	θ_{J-C}
Units	mW	V	V	V	V	mA	mA	mA	°C	°C	°C	mW/°C
	Note 20	Note 1	Note 1	Note 2	Note 2							Note 8

Acceptance Tests (high AQL)

Test	h_{ie}	h_{oe}	h_{re}
Units	ohms	umhos	
Minimum			
Maximum			
Conditions	Notes 4, 9, 11		

* This specification is adequate for power devices if a test for LV_{CER} is substituted for NF.

Acceptance Tests (low AQL)

Test	I_{CEO}	I_{CER}	I_{CBO}	I_{EBO}	h_{FE}	h_{FE}	h_{fe}	h_{fe}	f_{ae}	r_b	r_{CE}(SAT)	NF *	NR	V_{BE}(sat)
Units	uA	uA	uA	uA					mc	ohms	ohms	db	%	V
Minimum														
Maximum														
Conditions	Note 7				Notes 4, 9	Notes 4, 12	Notes 4, 9, 11	Notes 4, 11, 12	Note 9	Notes 9, 10, 21	Notes 4, 14	Notes 4, 9, 11,23	Note 6	Note 4, 14
	$V_{CE}=BV_{CEO}$	$V_{CE}=BV_{CER}$	$V_{CB}=BV_{CBO}$	$V_{EB}=EB_{EBO}$										

Figure 1

RF and Video Amplifiers

Maximum Ratings

Symbol	P_c	BV_{CEO}	BV_{CER}	BV_{CBO}	BV_{EBO}	I_{Cmax}	T_{jmax}	T_{opg}	T_{stg}	Θ_{J-C}	V_{RT}
Units	mW	V	V	V	V	mA	°C	°C	°C	mW/°C	V
	Note 20	Note 1	Note 1	Note 2	Note 2					Note 8	Note 3

Acceptance Tests (high AQL)

Symbol	h_{fe}	h_{ie}	h_{oe}	h_{re}	NF	h_{fe}
Units		ohms	umhos		db	
Minimum						
Maximum						
Conditions	Notes 4, 11, 9				Notes 4,9,24	Notes 4,9,22

Acceptance Tests (low AQL)

Symbol	I_{CEO}	I_{CER}	I_{CBO}	I_{EBO}	h_{FE}	h_{fe}	h_{fe}	h_{ie}	h_{oe}	h_{re}	f_{ae}	r_b	C_{ob}	NF	NR
Units	uA	uA	uA	uA				ohms	umhos		mc	ohms	uuf	db	%
Minimum															
Maximum															
Conditions	Note 7				Notes 4, 9	TA=25°C									
						Notes 9,22	Notes 11, 9				Note 9	Notes 9,10, 21	Note 5	Notes 9, 24	Note 6
	$V_{CE}=BV_{CEO}$	$V_{CE}=BV_{CER}$	$V_{CB}=BV_{CBO}$	$V_{EB}=BV_{EBO}$											

Figure 2

High Speed Switches and Computer Applications

Maximum Ratings

Symbol	P_c	BV_{CEO}	BV_{CER}	BV_{CBO}	BV_{EBO}	I_{Cmax}	I_{Bmax}	I_{Emax}	T_{Jmax}	T_{opg}	T_{stg}	Θ_{J-C}	V_{RT}
Units	mW	V	V	V	V	mA	mA	mA	°C	°C	°C	mW/°C	V
	Note 20	Note 1	Note 1	Note 2	Note 2							Note 13	Note 3

Acceptance Tests (high AQL)

Symbol	Q_b	Q_b	t_d	t_r	t_f	t_s
Units	uucoulombs	uucoulombs	usec	usec	usec	usec
Minimum						
Maximum						
Conditions	Note 4, 17	Note 4, 18	Note 4 - Figure 5			

Acceptance Tests (low AQL)

Symbol	I_{CEO}	I_{CER}	I_{CBO}	I_{EBO}	h_{FE}	h_{FE}	$r_{CE}(sat)$	Q_b	Q_b	t_d	t_r	t_s	t_f	V_{BE}	LV_{CER}	NR
Units	uA	uA	uA	uA			ohms	uucoul.	uucoul.	usec	usec	usec	usec	V	V	%
Minimum																
Maximum																
	Note 7				Notes 4, 15	Notes 4, 16	Notes 4, 14	Note 17 TA=25°C	Note 18 TA=25°C	Figure 5 TA=25°C				Notes 4, 14	Notes 4, 19	Note 6
Conditions	$V_{CE}=BV_{CEO}$	$V_{CE}=BV_{CER}$	$V_{CB}=BV_{CBO}$	$V_{EB}=BV_{EBO}$												

Figure 3

Figure 4

Note 1. Minimum breakdown voltage over T_{opg} is to be measured for some specified value of collector current.

Note 2. " " " " " " " " " " " " " leakage current.

Note 3. If punch-through limits the maximum collector-emitter voltage which may be applied, a minimum V_{RT} should be specified.

Note 4. Maximum and/or minimum values over T_{opg} should be specified as applicable, T should be specified.

Note 5. Suggested bias conditions $V_{CB} = BV_{CER}/3$, $I_E = 0$, $f = 1.0$ megacycle.

Note 6. Applicable to grown silicon devices only. Observe negative resistance region of collector characteristics near saturation on scope. NR (negative resistance) is calculated as $(I_C\text{max}-I_C\text{min})/I_C\text{max} \times 100$.

Note 7. $T_J = T_{opg}$ maximum, suggested 85°C for germanium and 150°C for silicon.

Note 8. Derating curve may be specified instead of θ_{J-C}.

Note 9. Suggested bias conditions: $V_{CE} = BV_{CER}/3$, $I_C = I_C\text{max}/20$.

Note 10. r_b is the measured ohmic resistance between the external base connection and base area where transistor action takes place.

Note 11. Suggested frequency of measurement; 1000 cps.

Note 12. Suggested bias conditions; $I_C = I_C\text{max}/2$, $V_{CE} = P_c/I_C$.

Note 13. Derating curve relating pulse duration, duty cycle and case temperature should be given.

Note 14. Suggested bias conditions $I_C = I_C\text{max}/2$, $I_B = (I_C/h_{FE}\text{ minimum}) \times 2$.

Note 15. Suggested bias conditions $I_C = I_C\text{max}/2$, $V_{CE} = r_{CE}(\text{sat}) \times I_C \times 2$.

Note 16. Suggested bias conditions $I_C = I_C\text{max}/10$, $V_{CE} = r_{CE}(\text{sat}) \times I_C \times 2$.

Note 17. Suggested bias conditions $I_C = I_C\text{max}/2$, $I_B = (I_C/h_{FE}\text{ min}) \times 3$.

Note 18. Suggested bias conditions $I_C = I_C\text{max}/10$, $I_B = (I_C/h_{FE}\text{ min}) \times 3$.

Note 19. Minimum voltage at which $m\alpha = 1$ occurs.

Note 20. This power dissipation is for 1000 hours expected life at an ambient temperature of 25°C.

Note 21. Suggested frequency of measurement $= f_{ae}\text{ max} \times (2)^4 = 16\, f_{ae}\text{ max}$.

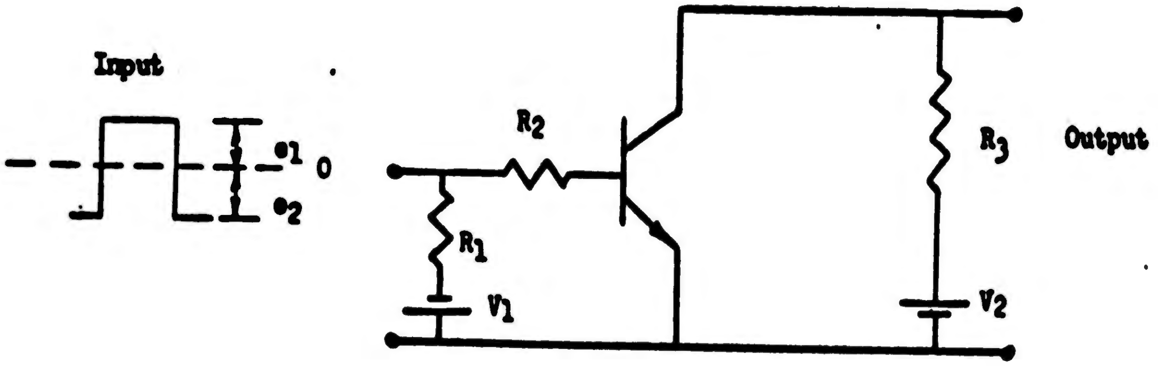
Note 22. Suggested frequency of measurement $= f_{ae}\text{ max} \times 2$.

Note 23. $R_g = r_b\text{ ave} + \dfrac{h_{fe}\text{ (ave)} \times 25}{I_E\text{ in mA}}$, $R_L = \dfrac{(BV_{CER}/3)}{(I_C\text{ max}/20)}$, bandwidth = 1 cycle, $h_{fe}(\text{ave})$ is average for device when biased as per Note 9.

Note 24. $R_g = r_b\text{ ave} + 1/2\ (h_{fe}(\text{ave}) \times 25)/I_E$ in mA, $R_L = (BV_{CER}/3) / (I_C\text{max}/20)$, bandwidth $= \dfrac{2\, f_{ae}}{10}$, $h_{fe}(\text{ave})$ is the average current gain at $f = 2\, f_{ae}$ when device is biased per Note 9.

Suggested resistance from base to emitter for voltage breakdown tests:
$P_c \geq 1$ watt, R = 100 ohms; $P_c < 1$ watt, R = 1000 .

Circuit for Measuring Pulse Characteristics



Notes: V_1, V_2, e_1, & e_2 polarities, as shown, are for NPN; polarities to be reversed for PNP.

$R_1 = 100$

$R_2 = \frac{10\ h_{FE}\ \text{min}}{I_C\ \text{max}}$ (h_{FE} min as determined in Note 15)

$R_3 = \frac{2(V2 - V_{CE}\ \text{sat})}{I_C\ \text{max}}$

$e1 = 4.4$ volts for silicon

$e_1 = 4.7$ volts for germanium

$e_2 = 10.9$ volts for silicon

$e_2 = 10.5$ volts for germanium

V_1 = variable

$V_2 = 0.8\ BV_{CER}$

Figure 5

EVALUATION OF MILITARY SPECIFICATIONS
FOR TRANSISTORS INCLUDED IN MIL-STD-[illegible]

POWER

	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
P_C	X	X	X	X	X	X	X	X	X			NO SPECIFICATION				
BV_{CBO}		●	●	●	●		●	V_{PT}								
BV_{CER}					●											
BV_{CEO}	●	●			●	●		●	●							
BV_{EBO}	●	●	●	●		●	●	●	●							
I_C max																
I_B max		X						X								
I_E max		X				X			X							
T_J max		X														
T_{opr}																
T_{stg}	X	X	X	X	X	X	X	X	X							
θ_{J-C}	●	●	●	●	●	●	●	●	●							
h_{ie}	●															
h_{oe}	●															
h_{re}	●															
I_{CEO}					●											
I_{CES}																
I_{CBO}	X	●	X	X	X	X	X	●	X							
I_{EBO}	●	●	●	●	●	X	X	●	●							
h_{FE}		●	●	●	●	●	●	●	●							
h_{fe}	●		●	●												
f_{ab}		●				●	●	●	●							
r_b																
V_{CE}(sat)	X	X	X	X	X	X	X	X	X							
V_{BE}(sat)	X	X			X	X	X		X							
BV_{CEO}																
[illegible]																

LOW POWER, AUDIO

	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
P_C	X	X	X	X	X	X	X	No Spec.
BV_{CBO}								
BV_{CER}			●					
BV_{CEO}	●	●	●	●	●	●	●	
BV_{EBO}	●	●	●	●	●	●	●	
I_C max								
I_B max								
I_E max								
T_J max								
T_{opr}								
T_{stg}	X	X	X	X	X	X	X	
θ_{J-C}	●	●		●	●	●	●	
h_{fe}	●	●	●	●	●	●	●	
h_{ie}	●	●	●	●	●	●	●	
h_{oe}	●	●	●	●	●	●	●	
h_{re}	●	●	●		●	●	●	
I_{CEO}								
I_{CES}								
I_{CBO}	●	●	●	●	X	X	X	
I_{EBO}	●	●	●	●	●	●	●	
h_{FE}								
f_{ab}		●	X	●	●	●	●	
r_b								
V_{CE}(sat)								
NF	●	●	●	●	●	●	●	
[illegible]								
V_{BE}(sat)								

SWITCHING

	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
P_C	X	X	X	X	X	X	X	X						NO SPECIFICATION						
BV_{CBO}	●	●	V_{PT}																	
BV_{CER}			●	●																
BV_{CEO}	●	●	●	●	●	●	●	●												
BV_{EBO}	●	●	●	●	●		●	●												
I_C max		X		X			X	X												
I_B max																				
I_E max								X												
T_J max				X			X													
T_{opr}																				
T_{stg}	X	X	X	X	X	X	X	X												
θ_{J-C}	●	●	●	●	●		●	●												
[illegible]																				
t_d			●	●	●															
t_r	●		●	●	●															
t_s	●		●	●	●															
t_f	●		●	●	●			●												
I_{CEO}	●		●																	
I_{CES}		●	●	●																
I_{CBO}	X	X	●	●	X	●	●	X												
I_{EBO}	●	●	●	●	●	●														
h_{FE}	X	●	●	●	●	●														
V_{CE} (sat)	X	X	X			X		X												
V_{BE}	X		X	X				X												
BV_{CEO}																				
[illegible]																				

LOW POWER, RF

	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
P_C	X	X	X	X	No Spec.	
BV_{CBO}			●	●		
BV_{CER}	●					
BV_{CEO}	●	●	●	●		
BV_{EBO}	●	●	●			
I_C max			X			
T_J max			X			
T_{opr}						
T_{stg}	X	X	X	X		
θ_{J-C}	●	●	●	●		
h_{fb}	●		●	●		
h_{ib}	●	●				
h_{ob}	●	●				
h_{rb}		●				
h_{fe}		●		●		
h_{FE}		●				
I_{CEO}			●			
I_{CES}						
I_{CBO}	●	X	●	X		
I_{EBO}	●	●	●			
f_{ab}	●	●				
r_b						
C_{ob}	●	X	X			
NF			●	●		
[illegible]						

X Specified
● Specified, but not adequately
(e.g. no temperature extremes, single-ended limit, etc.)

Figure 6

Theoretical Approach

The theoretical approach to the problem involves a mathematical description of the thermal operation of a transistor. This approach leads to a better visualization of what happens inside a transistor, but it has its limitations. In order to describe mathematically what happens, it is necessary to develop models (paper models) of the transistor. Simple models lead to simplified mathematical solutions, but only approximate solutions. More accurate solutions require more complicated models and more complex mathematics. Research along these lines has been conducted at the University of New Mexico. The models developed at the University of New Mexico impose the following limitations: operating conditions such that the leakage power dissipation of the transistor can be neglected, application under switching conditions and frequencies below 100 cycles per second, and other specific conditions for high-frequency operation. In addition to these conditions, it must be possible to represent the wave shape of the power pulses mathematically and to transform the mathematical expression. The more complicated the wave shape, the more complicated the mathematical expression. In addition, it might not be possible to invert the solution back into the time domain. The solutions to the problems are infinite, convergent, exponential series. Substitution into these series involves considerable mathematical drudgery and often the use of sophisticated digital computers to obtain the desired answers in a reasonable length of time.

The research work conducted at the University of New Mexico is an extremely valuable contribution and is an aid in the understanding of the problem. A summary of this work is presented below. A more detailed treatment is given in the original reports.

Case I[*]. The first analysis is that of an alloyed junction power transistor. To simplify the model, the first assumption is that radiation, convection, and conduction through the gases surrounding the crystal are negligible. The second assumption is that the emitter and collector can be represented by semi-infinite slabs, which is a good approximation for narrow pulses. Therefore, for Case I the pulse widths are limited to less than 0.02 second. Since no allowance is made for the power dissipation of the leakage current, Case I is also limited to operating conditions where the leakage-current power dissipation is negligible.

The thermal model for Case I is shown in Figure 7. The Fourier heat-flow equation for this one-dimensional model is given by Equation (1).

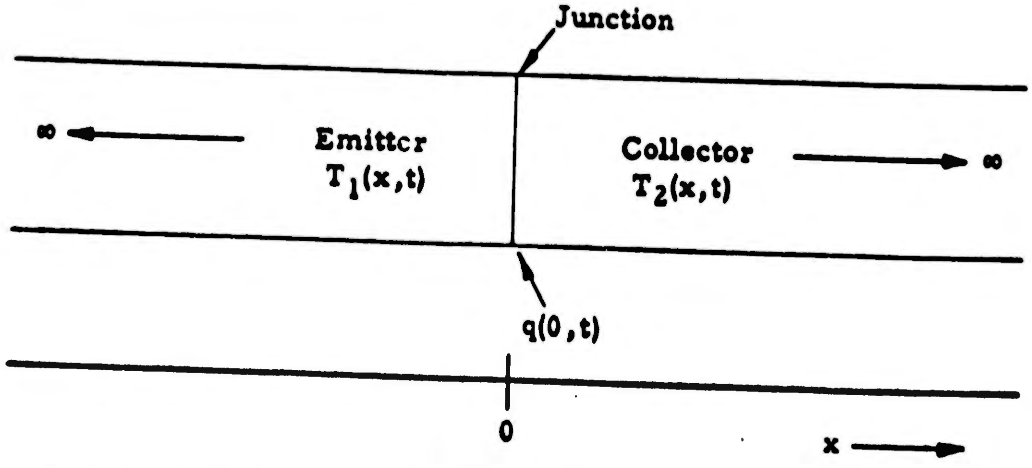


FIGURE 7. ONE-DIMENSIONAL THERMAL MODEL FOR CASE I.

---

[*] Reese, J. D., and Grannemann, W. W., "Transient Junction Temperature in Power Transistors", Technical Report EE-17, University of New Mexico Engineering Experiment Station.

$$\frac{\partial^2 T(x,t)}{\partial x^2} - \frac{1}{a}\frac{\partial T(x,t)}{\partial t} = 0, \qquad (1)$$

where

$T(x,t)$ = crystal temperature – degrees centigrade

$1/a = RC$

R = reciprocal of thermal conductivity – cm-°C-sec/cal

C = thermal capacity per unit volume – cal/°C-cm^3.

The boundary conditions for the model are:

(1) $Rq(0,t) = \frac{\partial T(0,t)}{\partial x}$

(2) $T(x,t)$ remains finite as x approaches infinity.

The solution for repetitive rectangular pulsed input is:

$$T_j = \sqrt{\frac{R}{C}}\,\frac{2P}{4.186A}\sum_{n=0}^{\infty}\left\{\sqrt{\frac{t - n\tau}{\pi}}\,[u(t - n\tau)]\right.$$

$$\left. - \sqrt{\frac{t - (n\tau + a)}{\pi}}\left\{u[t - (n\tau + a)]\right\}\right\} + T_o, \qquad (2)$$

where

T_j = junction temperature – degrees centigrade

P = peak input power – watts (emitter plus collector area)

A = area of slabs – cm^2 (emitter plus collector area)

a = pulse width – seconds

τ = time between pulses – seconds

t = time – seconds

T_o = initial junction temperature – degrees centigrade.

The expression $u(x - y)$ is equal to zero when the term within the parentheses is negative, and is equal to unity when the term within the parentheses is positive.

Equation (2) may be used to solve for the junction temperature for any time, provided the width of the input pulse is less than 0.02 second. A solution for steady-state conditions will yield the maximum instantaneous junction temperature. This steady-state solution would be slow and laborious, so an approximation method is used which yields the following expression for the maximum instantaneous junction temperature:

$$T_{max} = T_o + P\frac{a}{\tau}\theta + \sqrt{\frac{R}{c\pi}}\frac{2P}{4.186A}\left[\sqrt{a} - \frac{2\sqrt{\tau}}{3} + \frac{2(\tau - a)^{3/2}}{3\tau}\right], \tag{3}$$

where

T_{max} = maximum instantaneous junction temperature – degrees centigrade

T_o = ambient junction temperature – degrees centigrade

θ = thermal resistance from the collector junction to ambient – °C/watt

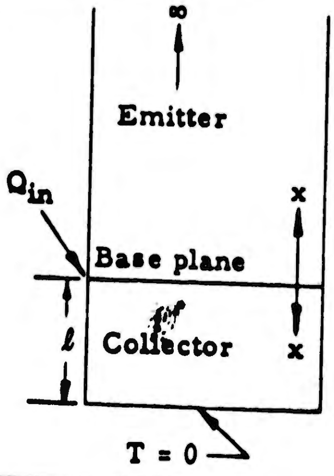
The following expressions are obvious from the derivation:

$$\overline{T} = T_o + \overline{P}\theta = T_o + P\frac{a}{\tau}\theta ,$$

$\overline{T}$ = average junction temperature – degrees centigrade

$\overline{P}$ = total average power input – watts.

Case II[*]. The thermal model for Case II is shown in Figure 8. The emitter region is represented by a semi-infinite slab, the face of which is in intimate contact with the base plane. The base region is represented by a plane over which heat is generated evenly according to the power input to the transistor. The collector region and the thermal path to ambient temperature is represented by a finite slab, whose upper face contacts the base plane and whose lower face is held at ambient temperature.



$\alpha_e = \alpha_c = \alpha$

$k_e = k_c = k$

FIGURE 8. THERMAL MODEL FOR CASE II

---

[*] Swain, G. R., and Grannemann, W. W., "Safe Thermal Operation of Power Transistors Under Pulse Excitation", Technical Report EE-18, University of New Mexico Engineering Experiment Station.

The heat-flow equations for the Case II thermal model are:

$$\frac{\partial^2}{\partial x^2} T_c(x,t) = \frac{1}{\alpha}\frac{\partial}{\partial t} T_c(x,t) \quad 0 \leqslant x < \ell,\ 0 \leqslant t \tag{4}$$

$$\frac{\partial^2}{\partial x^2} T_e(x,t) = \frac{1}{\alpha}\frac{\partial}{\partial t} T_e(x,t) \quad 0 \leqslant x,\ 0 < t. \tag{5}$$

The boundary conditions for the Case II thermal model are:

$T_c(x,0) = 0$

$T_e(x,0) = 0$

$T_e(0,t) = T_c(o,t)$

$T_c(\ell,t) = 0$

$T_e(x,t)$ is finite as x approaches infinity

$$q(t) = \left[- k \frac{\partial}{\partial x} Tc(x,t) - k \frac{\partial}{\partial x} T_e(x,t) \right] x = 0.$$

Solution for the runaway temperature yields the following:

$$T_{rw} = L_o \ln \frac{L_o}{P_{co}\ \theta S} \tag{6}$$

$$I_{co}(T) = I_{co}\ e^{\left(\frac{I}{L_o}\right)} \tag{7}$$

where

T_{rw} = runaway temperature - degrees centigrade above ambient

L_o = a constant - degrees centigrade

P_{co} = saturation current dissipation at ambient temperature - watts

θ = thermal resistance collector junction to ambient - °C/watt

S = stability factor*

T = junction temperature - degrees centigrade above ambient.

---

*Shea, R. F., Principles of Transistor Circuits, John Wiley & Sons, Inc., New York, pp 97-108.

To make the above expressions more clear, the following sample solution for runaway temperature is offered.

Manufacturer's specifications state that I_{co} will double for every 15°C increase in temperature.

$$I_{co}\,(T) = I_{co}\, e^{\left(\frac{I}{L_o}\right)}$$

$$I_{co} \times 2 = I_{co}\, e^{\left(\frac{15}{L_o}\right)}$$

$$e^{\left(\frac{15}{L_o}\right)} = 2$$

$$\frac{15}{L_o} = 0.694$$

$$L_o = 21.6.$$

Manufacturer's specifications state that

$$I_{co} = 0.1 \text{ ma at } 25°\text{C}$$

$$V_c = 45 \text{ volts}$$

$$\theta = 1.5°\text{C/watt.}$$

Circuit constants are such that

$$S = 2.0$$

$$T_{rw} = L_o \ln \frac{L_o}{P_{co}\,\theta\, S} = 21.6 \ln \left[\frac{21.6}{(0.1 \times 10^{-3})(45)(1.5)(2)}\right]$$

T_{rw} = 159°C above ambient or 184°C .

The maximum permissible peak power input may be computed from Equations (8) and (9).

$$P_i < \frac{T_{max}}{\theta}\,(1 - F) \tag{8}$$

$$F = \frac{\theta}{T_{max}}\, P_{co}\, S\, e^{\left(\frac{T_{max}}{L_o} - 1\right)} , \tag{9}$$

where

P_i = maximum permissible peak power input - watts

F = a constant

T_{max} = maximum permissible junction temperature - degrees centigrade.

T_{max} is determined by either the runaway temperature, materials melting point, or the temperature at which the electrical characteristics become overly distorted for the particular application.

The following example is offered to clarify the determination of maximum permissible peak power input. Constants which also appear in the example used to compute runaway temperature have the same values in this example.

T_{max} = 120°C - chosen from the electrical characteristics

$$F = \frac{\theta}{T_{max}} P_{co} S e^{\left(\frac{T_{max}}{L_o} - 1\right)} = \frac{(1.5)(0.1 \times 10^{-3})(45)(2)}{120} e^{\left(\frac{120}{21.6} - 1\right)}$$

$$F = .011$$

$$P_i = \frac{\theta}{T_{max}} (1 - F) = \frac{120}{21.6} (1 - .011)$$

$$P_i = 5.49 \text{ watts.}$$

The solutions for Case II are limited to switching applications and frequencies below 100 cycles per second.

Case III*. Under transistor operating conditions of high magnitude power pulses at low duty factors, if one satisfies the conditions of Equations (8) and (9) using average power, the peak junction temperature will exceed the maximum permissible junction temperature (T_{max}). If one satisfies the conditions of Equations (8) and (9) using peak power, the results will be conservative. If the margin between the assigned maximum permissible temperature and the runaway temperature exceeds $3L_o$ degrees, the change in leakage-current dissipation and the thermal feedback effects may be neglected.

The conditions for the application of Case III are the above, in addition to the condition that the junction temperature must return to very nearly its original value (ambient) between pulses. These conditions allow the use of a transistor model consisting of two semi-infinite slabs which meet at a boundary (the junction) over which the heat is generated. Any heat generated at the emitter junction is neglected. The heat-flow equation for this model is Equation (10).

---

*Swain, G. R., and Grannemann, W. W., "Safe Thermal Operation of Power Transistors Under Pulse Excitation", Technical Report EE-18, University of New Mexico Engineering Experiment Station.

$$\frac{\partial^2}{\partial x^2} T(x,t) = \frac{1}{\alpha} \frac{\partial}{\partial t} T(x,t) \quad 0 \leqslant x,\ 0 \leqslant t \ . \tag{10}$$

The boundary conditions for Equation (10) are:

$T(x,0) = 0$

$T(x,t)$ is finite as x approaches infinity

$$- k \left[\frac{\partial}{\partial x} T(x,t) \right]_{x = 0} = \frac{1/2\, P_i}{4.186A} \quad t > 0$$

$T(x,t)$ = temperature as a function of distance from the junction and time – degrees centigrade above ambient

x = distance from the junction – centimeters

t = time – seconds

α = thermal diffusivity – cm^2/sec

k = thermal conductivity – cal/sec-cm-°C

P_i = total power dissipation at the junction – watts

A = transistor junction area – cm^2.

Solution for the junction temperature ($x = 0$) as a function of time yields:

$$T(t) = \frac{P_i}{4.180kA} \sqrt{\frac{\alpha t}{\pi}} \ . \tag{11}$$

If the maximum permissible junction temperature is known, the permissible peak power and the average power are given by:

$$P_{max} = 4.180kA\ T_{max} \sqrt{\frac{\pi}{\alpha D \tau}} \tag{12}$$

$$P_{av} = 4.186kA\ T_{max} \sqrt{\frac{\pi D}{\alpha \tau}} \ , \tag{13}$$

where

P_{max} = permissible peak power - watts

P_{av} = average permissible power - watts

T_{max} = maximum permissible junction temperature - degrees centigrade above ambient

D = duty factor (pulse width/pulse period)

τ = pulse period - seconds

α = thermal diffusivity - cm^2/sec

k = thermal conductivity - cal/sec-cm-°C

A = transistor junction area - cm^2.

Equations (12) and (13) are conservative for very small duty factors. The results from Equations (12) and (13) can be over 20 per cent lower than necessary for $D > 0.05$.

The response of Equation (11) to the first cycle of a train of pulses shows that

$$T_{max}/T_{av} = \frac{3/2\sqrt{D}}{1-(1-D)^{3/2}} . \qquad (14)$$

The average junction temperature may be computed from

$$T_{av} = P_{av}\,\theta , \qquad (15)$$

where

T_{max} = peak junction temperature - degrees centigrade above ambient

T_{av} = average junction temperature - degrees centigrade above ambient

P_{av} = average pulse power - watts

θ = thermal resistance from the collector junction to

The approximate upper limit of duty factor for fairly accurate solutions for Case III is 25 per cent duty factor for frequencies above 100 cycles per second.

More sophisticated thermal models naturally lead to more accurate results. The limiting conditions for the more sophisticated thermal models are also more restricting for discrete solutions. The calculations involved in the evaluations of the solutions for the more sophisticated thermal models require the use of a high-speed computer to obtain the results within a reasonable length of time. Accordingly, the presentation of the more sophisticated thermal models is beyond the scope of this report, since the results of this report are intended for the use of individual equipment designers.

Reference is made to the original reports for a detailed development of the material presented in summary here, and for the development of the more sophisticated thermal models.

Analog Approach

The analog approach to the solution of the problems involves the determination and construction of a physical model of the thermal operation of the transistors. Through the use of such models we may avoid the complex mathematics and extensive arithmetic, and the restrictions imposed by simplifications. The response times of transistors suggest that the use of an electrical model would be most satisfactory. The current flowing in Battelle's electrical model represents the heat flow in the transistor. The voltage that appears across this electrical model represents the temperature gradient across the transistor.

To construct this electrical model, we must determine a thermal equivalent circuit for the transistor, determine a method of substituting electrical parameters in this equivalent circuit, and determine some sort of electrical circuit to drive the electrical model.

Transistor Thermal-Equivalent Circuit

There are probably many thermal-equivalent circuits for transistors. Only two thermal-equivalent circuits were considered: the transmission-line thermal-equivalent circuit and the series string of parallel RC pairs equivalent circuit.

Transmission-Line Thermal-Equivalent Circuit

The transmission-line thermal-equivalent circuit is derived from the physical geometry of the transistor. Figure 9 is a simplified sketch of a power transistor. The various parts (collector die, mounting base, etc.) are divided into sections. The thermal mass of each section is considered lumped at the center of the section. The thermal capacitances of these lumped thermal masses are connected by thermal resistance. Each series string of resistors from the transistor junction to ambient temperature is a thermal transmission line. The four thermal transmission lines shown are cross connected with thermal resistances to account for any lateral heat flow within the transistor which would result from nonsymmetrical construction. The values of thermal resistances and capacitances are determined from the thermal properties of the several materials involved. The electrical network for this model is shown in Figure 10. This model, however, is oversimplified because more tee sections would be required nearer the transistor junction where the time constants involved are smaller and the thermal frequency response higher.

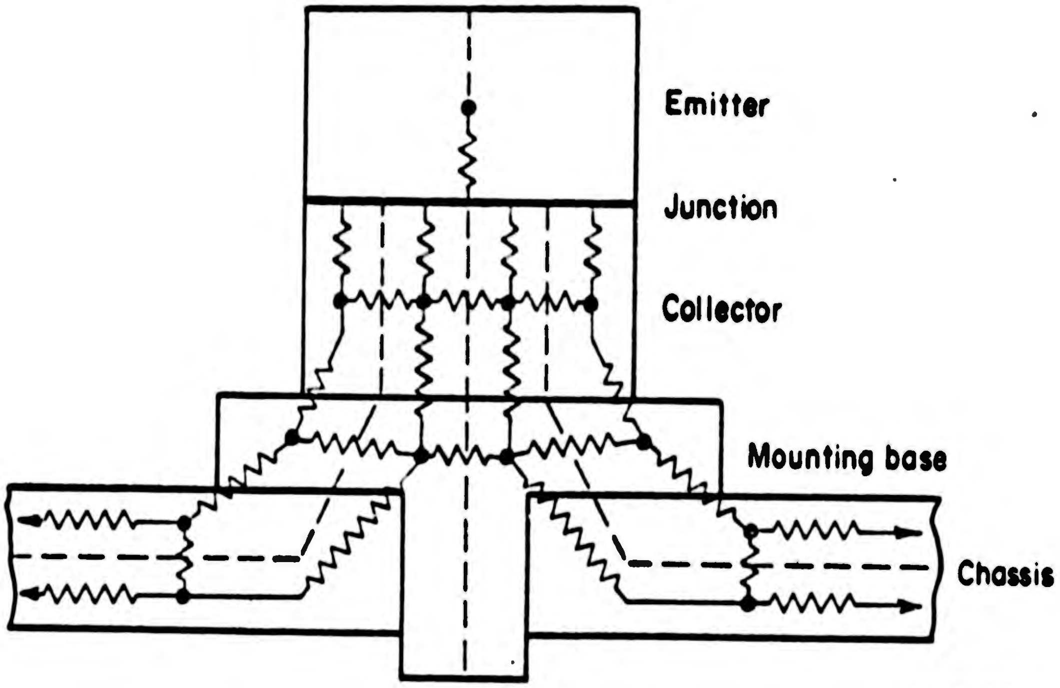


FIGURE 9. SKETCH OF A POWER TRANSISTOR FOR THE DEVELOPMENT OF A THERMAL ANALOG

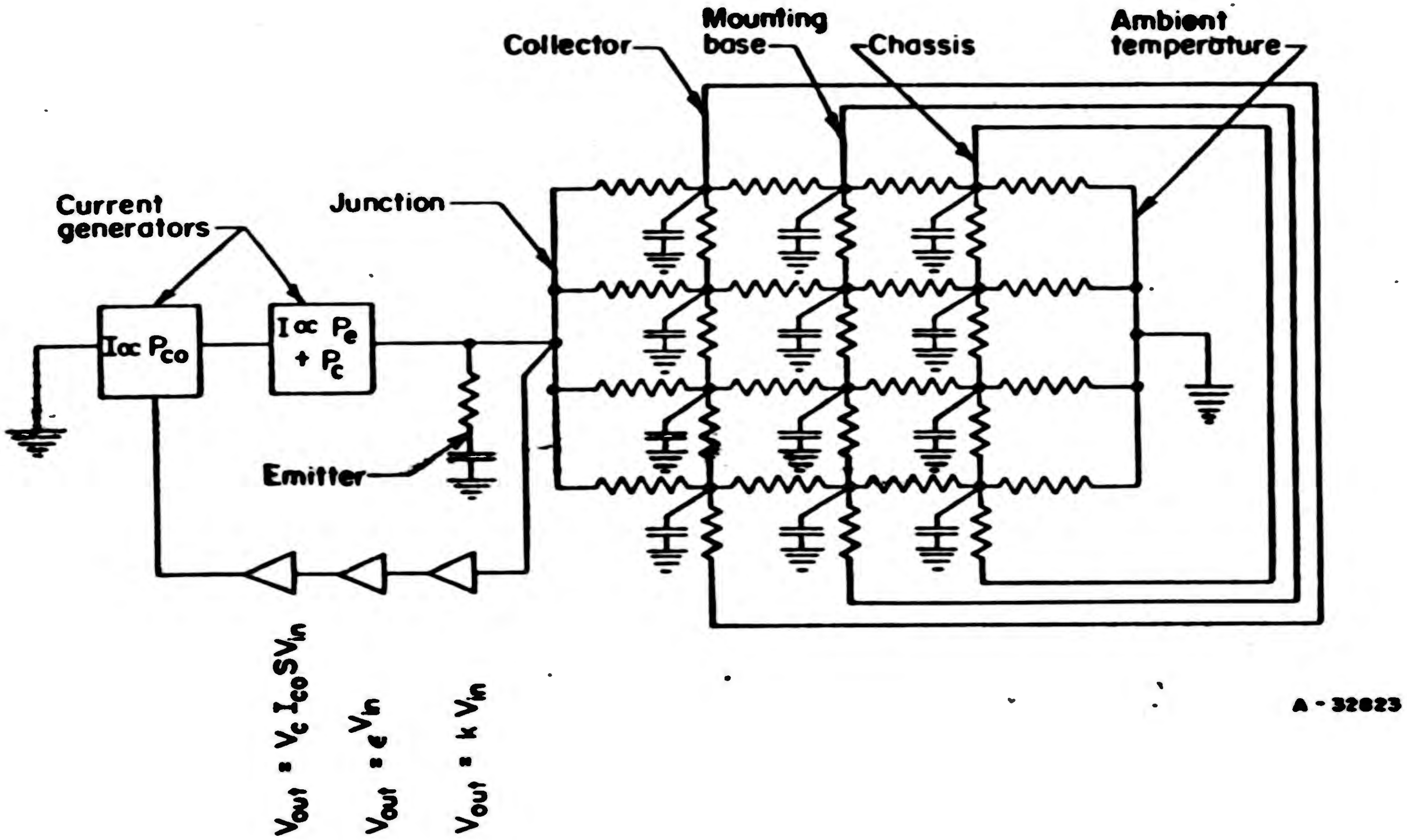


FIGURE 10. THERMAL ANALOG OF A POWER TRANSISTOR

A tapered transmission line thermal analog was constructed by the University of New Mexico*. This thermal analog consisted of 60 tee sections and was constructed and operated to verify the theoretical thermal analysis discussed earlier in this report.

Figure 10 also indicates a method by which the transmission-line thermal-equivalent circuit might be driven. Two current generators are used: one current generator to supply a current equivalent to the input power to the transistor, and the other current generator to supply a current equivalent to the leakage power of the transistor. The leakage-power current generator is driven by a feedback signal from the transistor-junction portion of the equivalent circuit. This feedback loop operates on the basis that the leakage power of a transistor is represented by:

$$P_{co} = I'_{co}\ V_c\ S_e kT_j\ ,$$

where

P_{co} = leakage power

I'_{co} = leakage current at ambient temperature

V_C = collector voltage

S = circuit stability factor

k = a constant characteristic of the transistor, and

T_j = junction temperature in centigrade degrees above ambient temperature.

The use of the transmission line thermal equivalent circuit has both advantages and disadvantages. The major advantage is that it is not necessary to have the actual transistor to perform an analysis of the transistor thermal operation. This would be of considerable use to transistor manufacturers. The major disadvantage is the inaccuracy introduced by the unknown thermal properties of any mechanical or soldered joints. A study of such joints could yield the necessary information, and this would be a very worthwhile undertaking for a transistor manufacturer and should result in an improved product. It is also felt that with some experience it should be possible to compensate for this missing information.

Series String of Parallel RC Pairs Equivalent Circuit

The series string of parallel RC pairs equivalent circuit is suggested by the manner in which a transistor junction cools i.e., exponential cooling. The mathematical basis for the use of this thermal-equivalent circuit is given by P. R. Strickland.** The validity of the circuit is based on the Cauer extension of Foster's reactance theorem which states in part that any network of RC elements has a driving point impedence that can be constructed of a series string of parallel RC pairs. Strickland gives a method of obtaining the circuit parameters based on the cooling characteristic of the transistor junction.

---

*Reese, J. D., and Grannemann, W. W., "An Electric Analog of Heat Flow in Power Transistors", Technical Report EE-11, University of New Mexico Engineering Experiment Station, June, 1958.

**Strickland, P. R., "The Thermal Equivalent Circuit of a Transistor", IBM Journal of Research and Development, 3 (1), January, 1959.

He also shows that, if a network is constructed that will exhibit electrical decay in the same manner as a transistor junction cools, this network, when driven, will behave in the same manner as the transistor junction when heated.

Thus, the series string of parallel RC pairs equivalent circuit parameters are derived directly from the transistor itself by experimental means. No knowledge of the physical construction or of the materials of the transistor is necessary. A complicated, nonsymmetrical configuration presents no additional problems. The unknown characteristics of mechanical or solder joints are automatically taken into account.

The series string of parallel RC pairs equivalent circuit was the circuit used in the analog that was constructed.

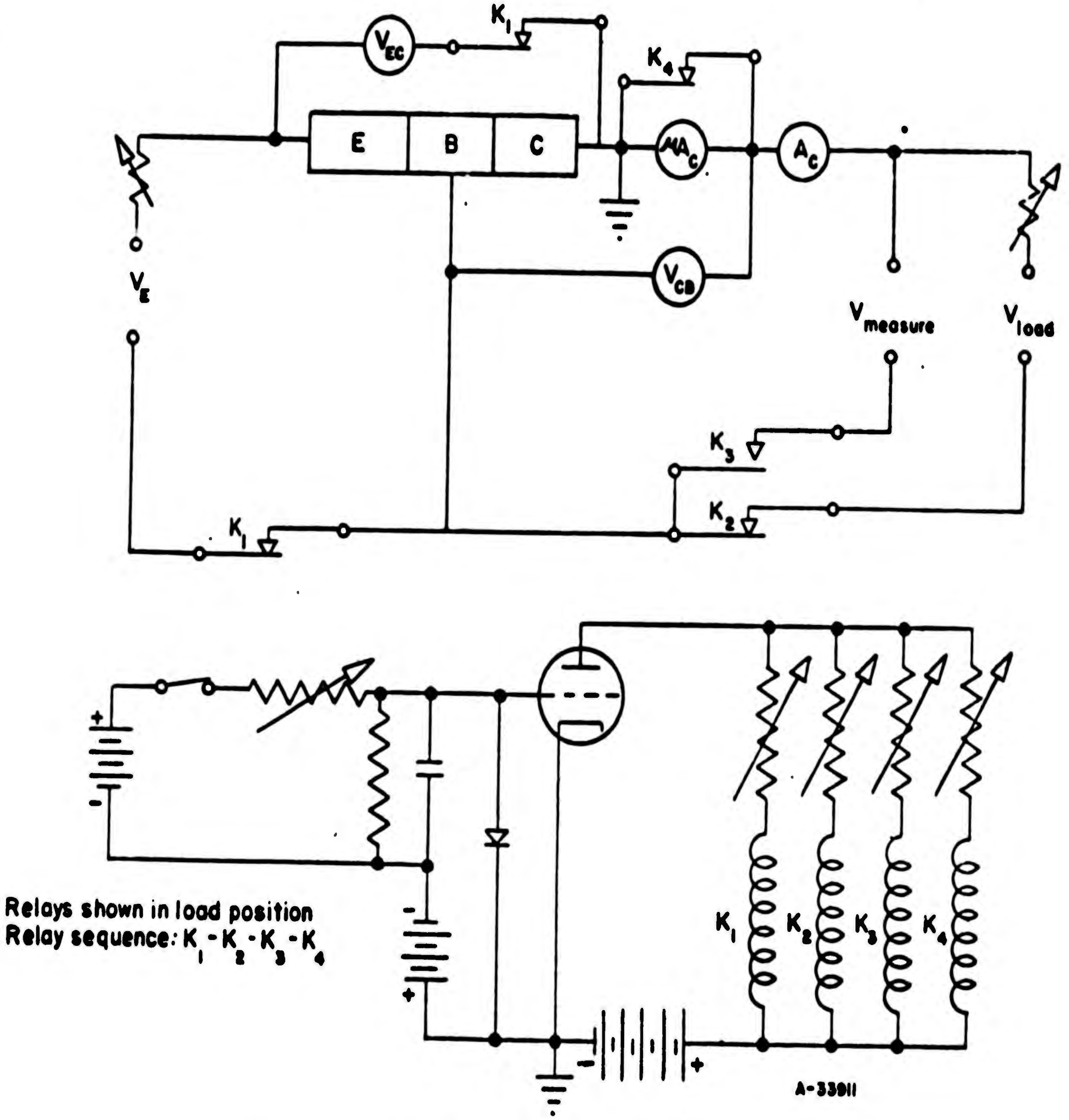
Determination of Thermal-Equivalent Circuit Parameters

The thermal circuit parmaters for the series string of parallel RC pairs equivalent circuit are determined experimentally using the transistor type being evaluated or an average of several transistors of that type.

The first step is the temperature calibration of the reverse biased collector leakage current. This is done by placing the transistor in an oven, heating the transistor to the desired temperatures, and measuring the leakage current for various values of collector voltage. It is advisable to use five or six values of collector voltage because some individual transistors will exhibit I_{co} temperature characteristics which actually show a decrease in leakage current with an increase in temperature, for specific values of collector voltage. This type of characteristic is useless for a temperature calibration. The results obtained from this temperature calibration showed considerable variation of the actual values of leakage current among transistors of the same 2N type number. The shapes of the characteristics were consistent, however.

The second step is to heat the transistor junction, remove the heating power, and measure the decay of I_{co} as the junction cools. The circuit used is shown in Figure 11. Mercury wetted relays were used in this circuit. The relays were actuated by a sawtooth voltage so that the sequence of relay operations could be maintained and so that the time between the operation of each of the relays could be very closely spaced. For power transistors, where the load current is considerable and the emitter and collector resistors are small, it is possible to measure I_{co} with the loading voltage because the voltage drop across the collector resistor is very small when I_{co} is the only current flowing. The microammeter shown in the circuit was an oscilloscope with a shunt resistor. The oscilloscope was operated without horizontal sweep, and the vertical trace was recorded with a 35-mm camera using continuous film motion and an open shutter. A time base was supplied by a neon lamp which recorded directly on the edge of the film.

The I_{co} decay curves were translated into temperature decay curves. The temperature of the heat sink used during the experiment was then subtracted from the decay curve, and the results plotted on semilog graph paper were similar to the curve shown in Figure 12. Here, the horizontal axis is time and the vertical axis is temperature change in centigrade degrees. This curve is an infinite exponential series which converges very rapidly. The straight-line extension of the flat portion of the curve represents the first term of the exponential series. The difference between the straight line



Relays shown in load position
Relay sequence: $K_1 - K_2 - K_3 - K_4$

FIGURE 11. LOADING AND MEASURING CIRCUIT USED TO OBTAIN THE JUNCTION COOLING CHARACTERISTICS

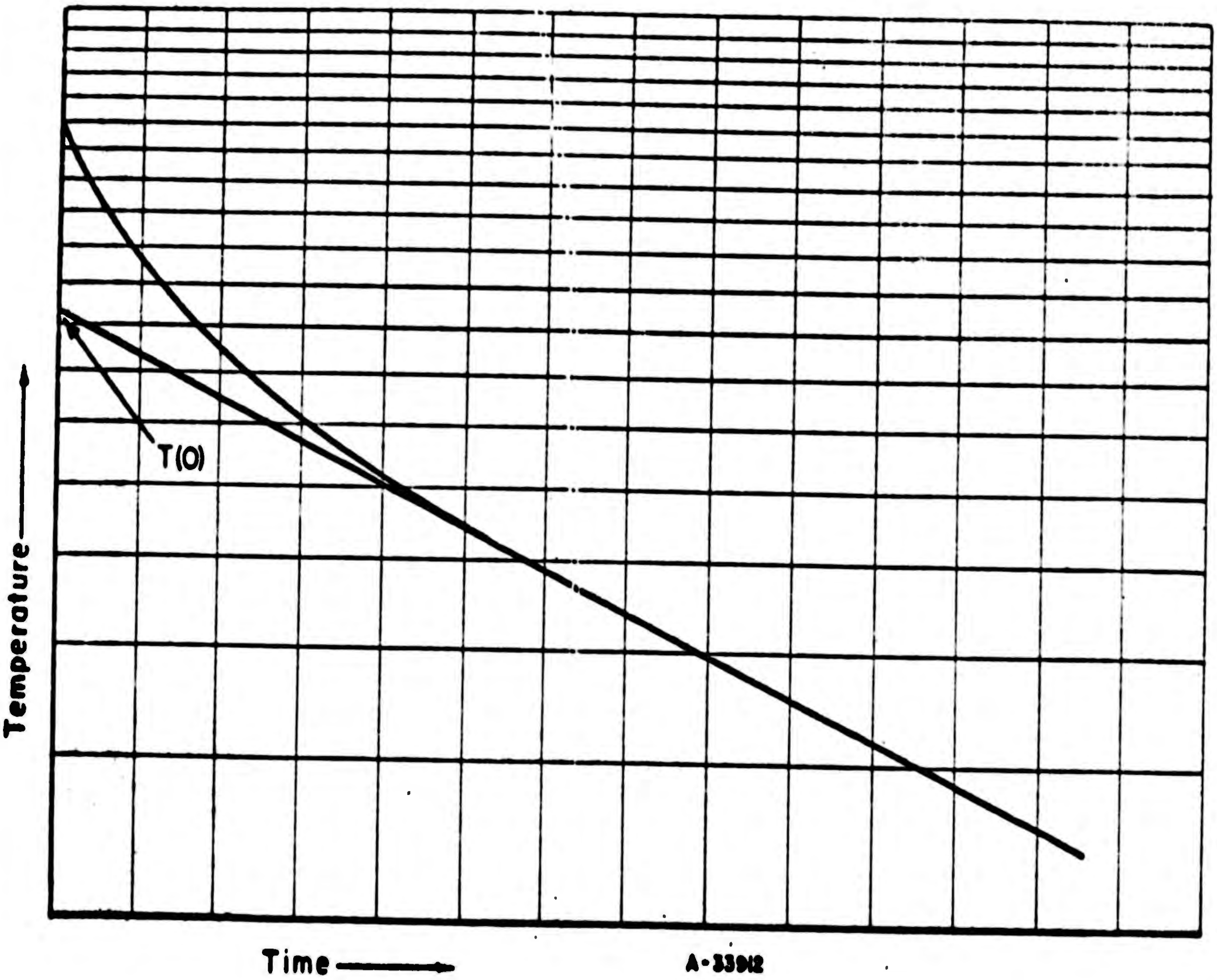


FIGURE 12. TRANSISTOR JUNCTION COOLING CURVE

and the curve represents the contribution of the remaining terms of the exponential series. The difference between the straight line and the curve was then plotted on semilog graph paper. This second curve has the same general shape as the curve shown in Figure 12. Here, the straight-line extension of the flat portion of the curve represents the second term of the exponential series. This process is repeated until there is no difference between the straight line and the curve, within the desired limits of accuracy. So far this has occurred after 3 to 5 terms of the exponential series have been determined.

For the sake of clarity, let us go through the calculation of the equivalent circuit constants for a 2N697 transistor. Figure 13-A is a plot of the junction cooling characteristic of the 2N697 transistor. From Figure 13-A it can be seen that the temperature across the first of the parallel RC pairs of the equivalent circuit was 98.7°C at time zero. The temperature had dropped to 93.0°C 100 milliseconds later. The temperature decay across the RC pair is described by the equation:

$$T(n) = T(0)e^{-t/RC} ,$$

where

$T(n)$ = the temperature at time t

$T(0)$ = the temperature at time zero.

Thus:

$$93.0 = 98.7e^{-0.1/RC} .$$

Solving for RC:

$$RC = 1.689 \text{ seconds} .$$

The value of R may be determined from the initial temperature across the RC pair, which is actually the temperature at the end of the loading period, when the temperature across the RC pair reaches steady-state condition. Thus:

$$R = T(0)/P ,$$

where

P = power applied during loading, in watts.

Substituting:

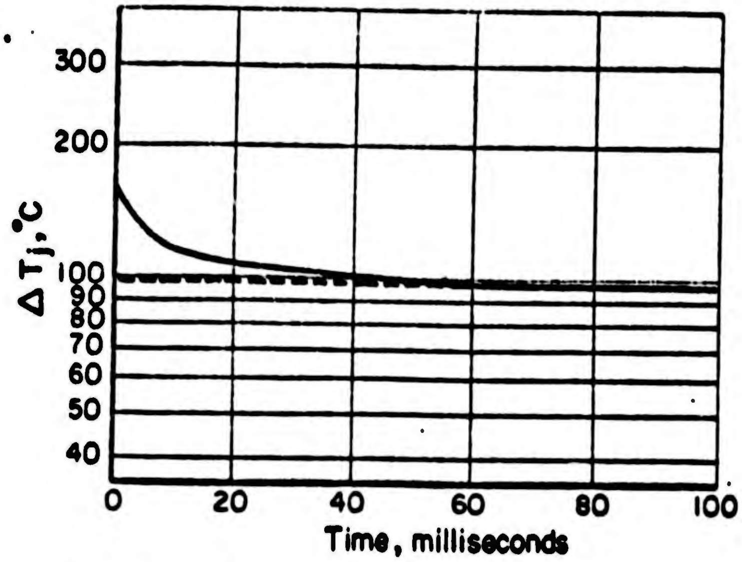
$$R = 98.7/2 = 49.35\text{°C/watt} .$$

Substituting the value of R in the time-constant equation above gives:

$$C = 3.42 \times 10^{-2} \text{ watt-seconds/°C} .$$

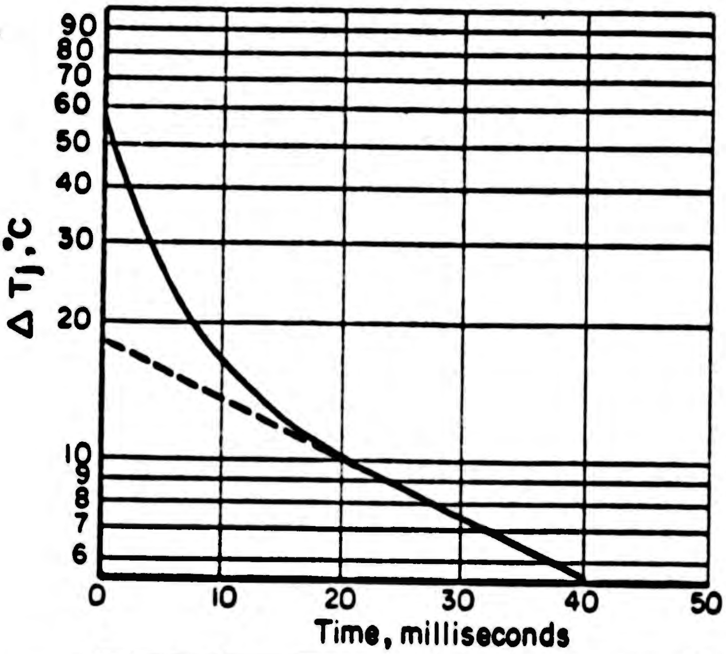
The difference between the curve and the straight line of Figure 13-A is plotted in Figure 13-B. From Figure 13-B:

FIGURE 13-A.



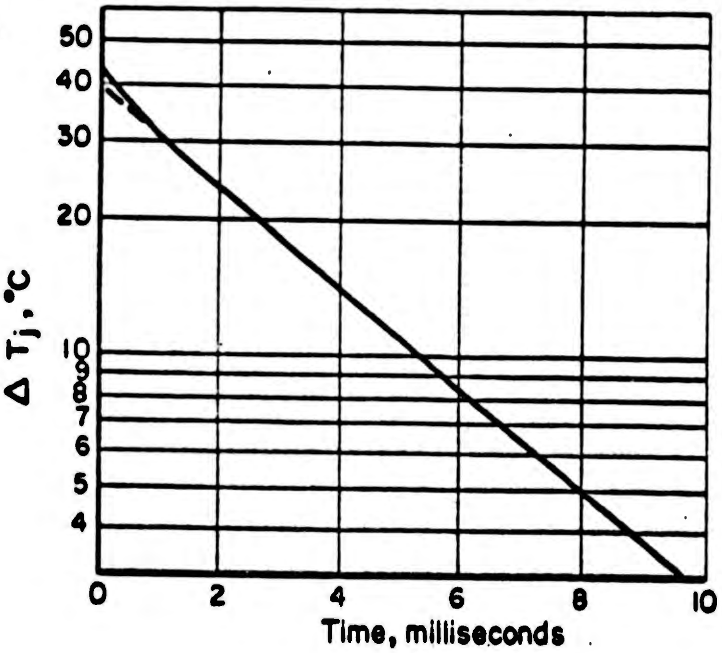
2N697 Network 1 calculations

FIGURE 13-B.



2N697 Network 2 calculations

FIGURE 13-C.



2N697 Network 3 calculations

A-35084

$$T(0) = 17.9°C$$

$$T(n) = 4.01°C$$

$$t = 0.05 \text{ second.}$$

From these values the following may be computed:

$$RC = 0.0334 \text{ seconds}$$

$$R = 8.95°C/\text{watt}$$

$$C = 3.735 \times 10^{-3} \text{ watt-seconds}/°C.$$

The difference between the straight line and the curve of Figure 13-B is next plotted as shown in Figure 13-C. From Figure 13-C:

$$T(0) = 41.0°C,$$

$$T(n) = 2.91°C,$$

$$t = 0.01 \text{ second,}$$

$$RC = 0.00378 \text{ second}$$

$$R = 20.5°C/\text{watt}$$

$$C = 1.844 \times 10^{-4} \text{ watt-second}/°C$$

The difference between the straight line and the curve of Figure 13-C was considered insignificant, so no further networks were computed. Conversion of the above thermal units to electrical units will be discussed after some of the limiting conditions imposed by the analog driving circuit are given.

Transistor Thermal-Analog Driving Circuit

The complete transistor thermal analog is shown in Figure 14. The analog network is shown on the right. The current through this network is equivalent to the heat flow in the transistor. The voltage that appears across the network is equivalent to the junction-temperature rise above ambient temperature.

The current for the analog network is supplied by a 6AU6 vacuum tube. The 6AU6 is operated so that for a given voltage input the current output is constant from almost zero to 90,000 ohms load impedance. Here is the first limiting factor for the conversion from thermal to electrical circuit constants: the total resistance must be less than 90,000 ohms. The 6AU6 current source delivers a current made up of three parts: (1) P_c is a current equal to the input power to the transistor, (2) P_{co} is a current equal to the leakage power of the transistor, (3) P_q is the quiescent current delivered by the current source. Thus, the voltage which appears across the analog network equals the junction-temperature rise and a voltage caused by the quiescent current flow.

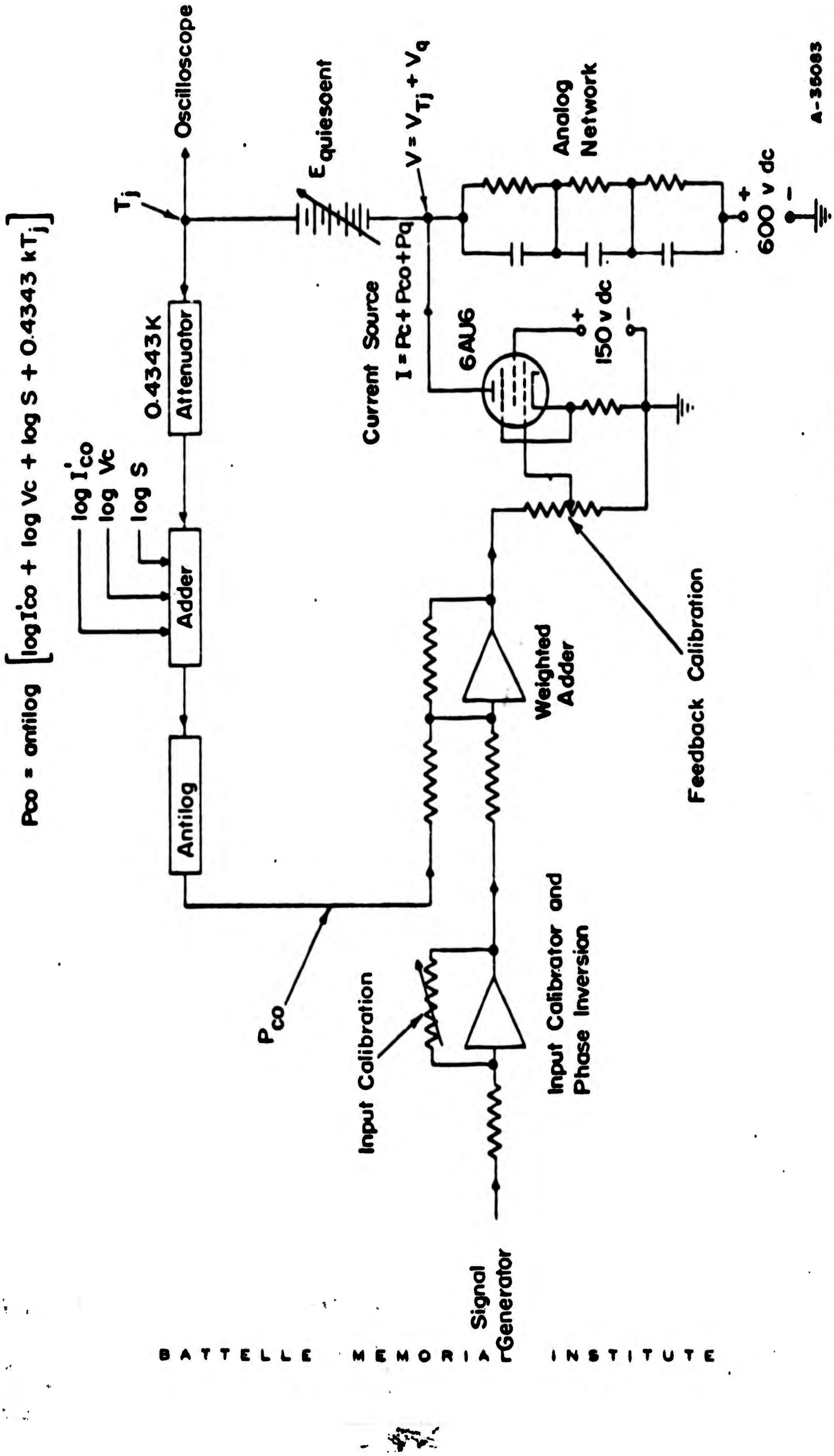


FIGURE 14. TRANSISTOR THERMAL ANALOG

The leakage power of the transistor is produced by a feedback loop in the analog. The feedback loop is based on the assumption that the leakage-current temperature characteristic is closely approximated by:

$$I_{co} = I'_{co}\, e^{kTj} ,$$

where

I_{co} = leakage current at junction temperature T_j

I'_{co} = leakage current at ambient temperature

Tj = junction temperature in centigrade degrees above ambient temperature

k = a constant characteristic of the transistor.

Thus, the leakage power is:

$$P_{co} = I'_{co}\, V_c\, S\, e^{kTj} ,$$

where

V_c = collector voltage

S = stability factor.

This equation for leakage power may be rewritten:

$$P_{co} = \text{antilog}\,[\log I'_{co} + \log V_c + \log S + 0.4343\, kT_j] .$$

A voltage equivalent to T_j is obtained from the high side of the analog network by balancing out the quiescent voltage with battery E_q. The quantity 1/k is equal to the temperature rise of the transistor junction required to double I_{co}, and this is usually of the order of about 11°C. Therefore, the quantity 0.4343 k is obtained through the use of an attenuator. The quantity 0.4343 kT_j is added to voltages equivalent to log I'_{co}, log V_c, and log S with an adding amplifier. The antilog of this sum is obtained through the use of an arbitrary-function generator. The output of the function generator is a voltage equivalent to P_{co}. This voltage is added to a voltage equivalent to the input-signal power, and the sum of the two voltages is used to drive the current source.

Calibration is accomplished in the following manner (using a 2N697 transistor as an example). The 2N697 transistor is a 2-watt silicon transistor with a maximum junction temperature of 175°C.

The arbitrary-function-generator input and output are disconnected, and the attenuator is set for zero output. The log I'_{co} voltage source is set for the value of I_{co} at 170°C. The voltage output of the adder is measured and recorded. The log I_{co} voltage source is then adjusted to the minimum I_{co} value. For a 2N697 transistor, this is equal to a junction temperature of 90°C (about 1 microampere of leakage current). A d-c voltage is then applied to the signal-generator input which will produce a voltage across the analog network equivalent to an 80°C junction temperature rise (170-90 = 80). The attenuator is then adjusted so that the adder voltage output equals the voltage recorded for I_{co} at a junction temperature of 170°C.

The arbitrary-function generator (previously adjusted so that the output is the antilog of the input) is now connected into the circuit. The log V_c and log S voltage sources are then set for convenient values, and the value of P_{co} is computed. With zero signal input, the feedback calibration attenuator is adjusted so that the current flowing in the analog network is equivalent to the computed leakage power plus the quiescent current flow.

With the feedback loop disconnected, a d-c voltage is applied to the signal-generator input. The input calibration potentiometer is then adjusted so that the current flowing in the analog network is equivalent to the desired power equivalent for the voltage input. The analog is now calibrated and ready to operate.

Conversion of Circuit Parameters From Thermal to Electrical Units

The conversion from thermal- to electrical-equivalent circuit parameters must include consideration of the limitations of the circuit used to drive the analog network. It has already been stated that the maximum resistance of the analog network must be less than 90,000 ohms. The maximum current the 6AU6 can deliver and still maintain linear operation is about 9 milliamperes, while the quiescent current value is 1 milliampere. Thus, the two major limiting conditions that must be considered when computing thermal-electrical equivalencies are a maximum resistance of 90,000 ohms and a current swing of 8 milliamperes.

The total thermal resistance of the 2N697 transistor is 78.8°C/watt (obtained by adding the thermal resistance from each of the three networks). The numbers come out better if some multiple of 418 (conversion from g-cal/sec to watts) is used for the number of ohms equivalent to 1°C/watt. Therefore, define

$$836 \text{ ohms} = 1°\text{C/watt}. \tag{16}$$

From this we get the total resistance of the three networks equal to 65,877 ohms, which is within our 90,000 ohms limitation.

By definition:

$$1 \text{ g-cal/sec} = 4.18 \text{ watts}.$$

From equation (16) we get

$$836/4.18 \text{ ohms} = 1°\text{C}/4.18 \text{ watts}$$

or

$$200 \text{ ohms} = 1°\text{C/g-cal/sec}. \tag{17}$$

The 2N697 transistor has a power rating of 2 watts. Let us define the maximum power the transistor thermal analog must operate at as ten times the rating or 20 watts. Therefore, let us define

$$20 \text{ watts} = 8.0 \text{ ma}$$

or,

1 watt = 0.4 ma.

By definition.

1 watt = 0.239 g-cal/sec.

From this we get

1 watt = 0.4 ma = 0.239 g-cal/sec

or,

1 g-cal/sec = 1.674 ma.

Ohm's Law applied to both the electrical and thermal circuit. Thus

$$E = IR = (1.674 \times 10^{-3})(200) = 0.3348 \text{ volts} = 1°C$$

or,

1 volt = 2.987°C.

By definition:

$$1.674 \times 10^{-3} \text{ amperes} = 1.674 \times 10^{-3} \text{ coulombs/second}$$

or,

$$1.674 \times 10^{-3} \text{ coulombs/second} = 1 \text{ g-cal/second}.$$

Thus:

1 coulomb = 597.4 g-cal.

By definition:

1 farad = 1 coulomb/volt.

Thus:

1 farad = 597.4 g-cal/2.987°C,

or,

1 farad = 200 g-cal/°C.

By definition:

1 watt-second = 0.239 g-cal,

so,

1 watt-second/°C = 1196 microfarads.

Summarizing the above:

1°C/watt = 836 ohms

1°C = 0.3348 volt

1 watt = 0.4 milliampere

1 w-sec/°C = 1196 microfarads.

The thermal-electrical equivalencies may now be used to compute the electrical equivalent circuit. The results of this computation are given in Table 1. It may be seen from Table 1 that the values of the capacitances are rather large. We may reduce these capacitances values by a factor of 10 by operating the thermal analog ten times faster than the transistor operates thermally.

TABLE 1. 2N697 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistances		Capacitance	
	°C /watt	K-Ohms	W-Sec/°C	Microfarads
1	49.35	41.26	0.03420	40.93
2	8.95	7.48	0.003735	4.46
3	20.50	17.14	0.0001844	0.221

1°c/watt = 836 ohms.
1°C = 0.3348 volts.
1 watt = 0.4 milliamperes.
1 w-sec/°C = 1196 microfarads.

Analog-Verification Experiment

The purpose of the analog-verification experiment was to obtain data directly from transistors which would provide a means of placing a figure of merit on the results obtained from the transistor thermal analog.

This verification experiment involved measuring the peak power that must be dissipated at the collector junction to raise the temperature of the junction a specified number of degrees above the heat-sink temperature under various conditions of pulse length, duty factor, and repetition rate. The collector junction temperature was monitored by measuring the reverse bias collector leakage current (I_{co}) between power pulses. Power dissipated at the collector junction is given by the product of the measured collector current and the base-to-collector voltage during the power pulses.

Measurement Circuit

The measurement is accomplished by use of the circuit shown in Figure 15 which was first suggested in the principle by Mortenson*. Although Figure 15 shows the circuit used for NPN transistors, the same arrangement with all voltage polarities and diodes reversed can be used for PNP units. All measurements are made by means of a calibrated oscilloscope.

During the period of time in which power is to be dissipated in the transistor, a positive driving signal is produced by the wave-form generator. This voltage is applied to the base-emitter junction of the transistor through the forward biased diodes, D_1 and D_2. This causes collector current to flow, and the amount of power given by the product of I_c (measured across R_c) and V_{cb} is dissipated in the collector-base junction. Control of the dissipated power can be obtained by varying the emitter resistance, R_e and/or by changing the amount of driving signal by varying the setting of potentiometer R_g.

During the period when no power is being dissipated in the transistor, the wave-form generator is producing no voltage signal, and the transistor is cut off. Diode D_1 is reverse biased by the action of battery V_B, so that the emitter is isolated. Collector cutoff current (I_{co}) is now flowing through battery V_{cc} and the collector-base junction. This current, measured across R_b and the reverse biased diode, D_2, is used as an indication of junction temperature. The function of D_2 is to limit the $I_b R_b$ drop during the power pulse so as not to overdrive the oscilloscope, which has been set for high gain to measure the small voltage $I_{co} R_b$. This is necessary since $I_b \gg I_{co}$, and because I_b and I_{co} flow in opposite directions.

The wave-form generator must be isolated from ground, and, indeed, no part of the circuit is grounded. This permits a grounded oscilloscope to be used for making measurements. Of course, only one such oscilloscope may be connected into the circuit at any one time, or else two points in the circuit will be simultaneously grounded.

The wave-form generator used was a Tektronix Type 162 which was triggered by a square-wave generator through an isolation transformer. The square-wave triggering generator is used to control the repetition rate of the driving signal, while the wave-form generator controls pulse length.

The oscilloscope used to make the measurements was triggered by the same square-wave generator that was used to trigger the wave-form generator. If the temperature rise produced by a single, nonrepetitive pulse is to be examined, the wave-form generator is manually triggered. The scope trigger signal is then taken from the output of the wave-form generator through an isolation transformer with a small resistor in series with the primary winding.

Resistor R_b is selected so as to give a suitable oscilloscope deflection for reading I_{co}. However, excessively high values of R_b when shunted by the oscilloscope input capacitance lead to an excessive RC time constant. This causes considerable delay before the transient caused by the forward voltage drop across diode D_2 during the power pulse can die out, permitting the reverse polarity $I_{co} R_b$ drop to be read. In general, values for R_b of 1 megohm or less will be fairly satisfactory. Diode D_2 should combine high speed and low forward voltage drop.

---

*Mortenson, K. F., "Transistor Junction Temperature as a Function of Time, IRE Proceedings, 508 (April, 1957).

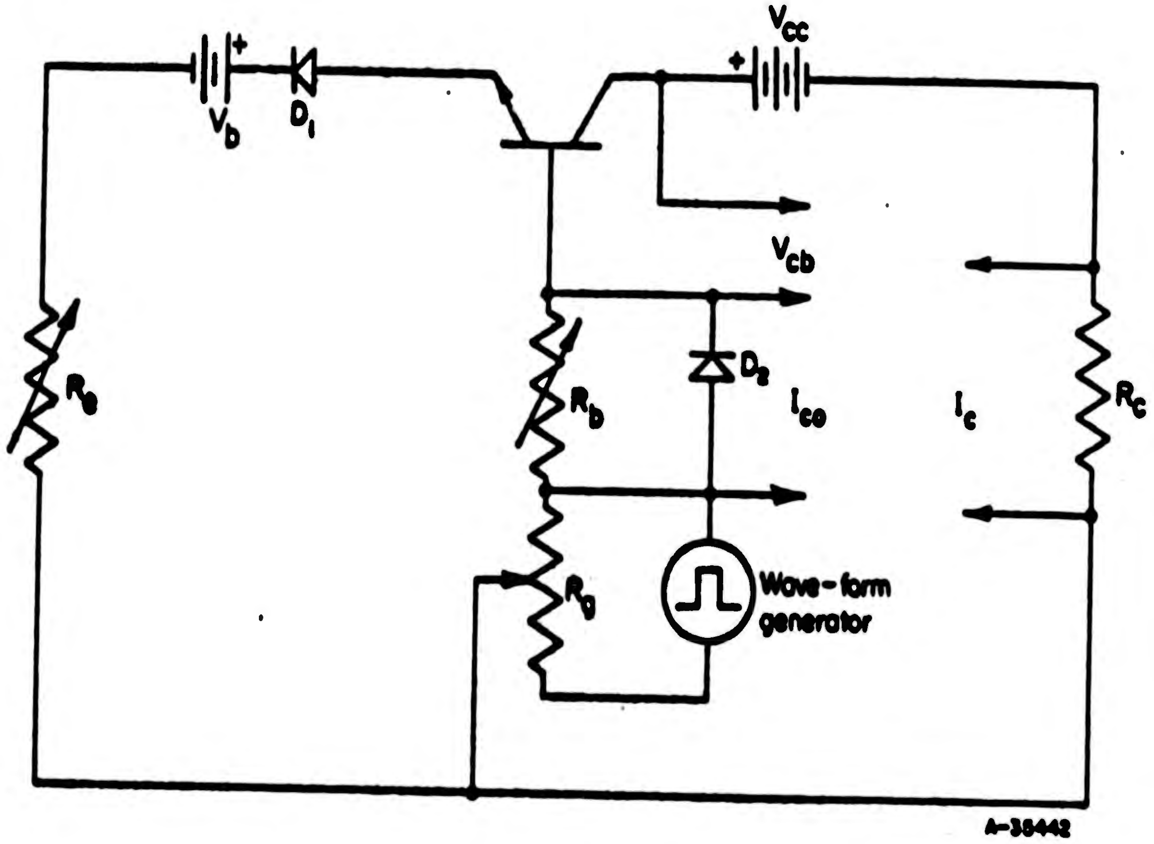


FIGURE 15. VERIFICATION-EXPERIMENT MEASURING CIRCUIT

Resistor R_c should be small, 10 ohm or 1 ohm. A precision resistor was used since I_c is measured across R_c. Battery voltage V_{cc} is chosen to be slightly less than the collector-base breakdown voltage for the transistor under test. Lead storage batteries proved to be a satisfactory source. Battery V_B was 2 volts, one cell of a storage battery. Resistor R_e is variable up to 2 K-ohms. Diode D_1 must be capable of carrying the required I_c, while providing maximum isolation. The oscilloscope used should have d-c sensitivity to at least 0.05 volt per centimeter of deflection. The test transistor is mounted in a heat sink in thermal contact with a water bath maintained at 25 C. The oscilloscope wave forms for the input pulse, I_{co}, I_c, and V_{cb} are shown in Figure 16.

Measurement Procedure

It is first necessary to obtain collector cut-off current (I_{co}) as a function of voltage at the temperature desired for each individual transistor. This is done by first heating the transistor in an oven until thermal equilibrium at the desired temperature is reached, and then measuring I_{co} vs. applied voltage.

Then, for a given V_{cc}, the I_{co} corresponding to the desired temperature rise above 25 C is known. Resistor R_b is adjusted (calibrated) so that when this amount of current is made to flow through it (by an external battery and resistor) the oscilloscope will show a desired known deflection.

With the repetition rate and duty factor set at the desired values, the input power is increased until the oscilloscope deflection produced by $I_{co}R_b$ is at the previously calibrated amount. Some time must be allowed for the transistor to reach equilibrium. Then I_c and V_{cb} are measured, and the values recorded. Each set of measurements was repeated two or three times, and the average power input calculated.

Difficulties Encountered

Several difficulties arise when actual measurements are attempted. These difficulties may be summarized as follows:

(1) Destruction of the transistor

(2) Spurious oscillations and 60-cycle a-c pickup

(3) Inabaility to monitor I_{co} accurately.

In a previous report, other difficulties are mentioned. These problems do not exist when the revised circuit shown in Figure 15 is used.

Destruction of Transistor. The basic problem encountered in operating the transistors at, or near, their maximum allowable junction temperatures is the destruction of the transistors as the result of thermal runaway. The collector current is the sum of the reverse leakage current and the current transferred from the emitter, as shown by the expression:

$$I_c = I_{co} + h_{fe}I_e .$$

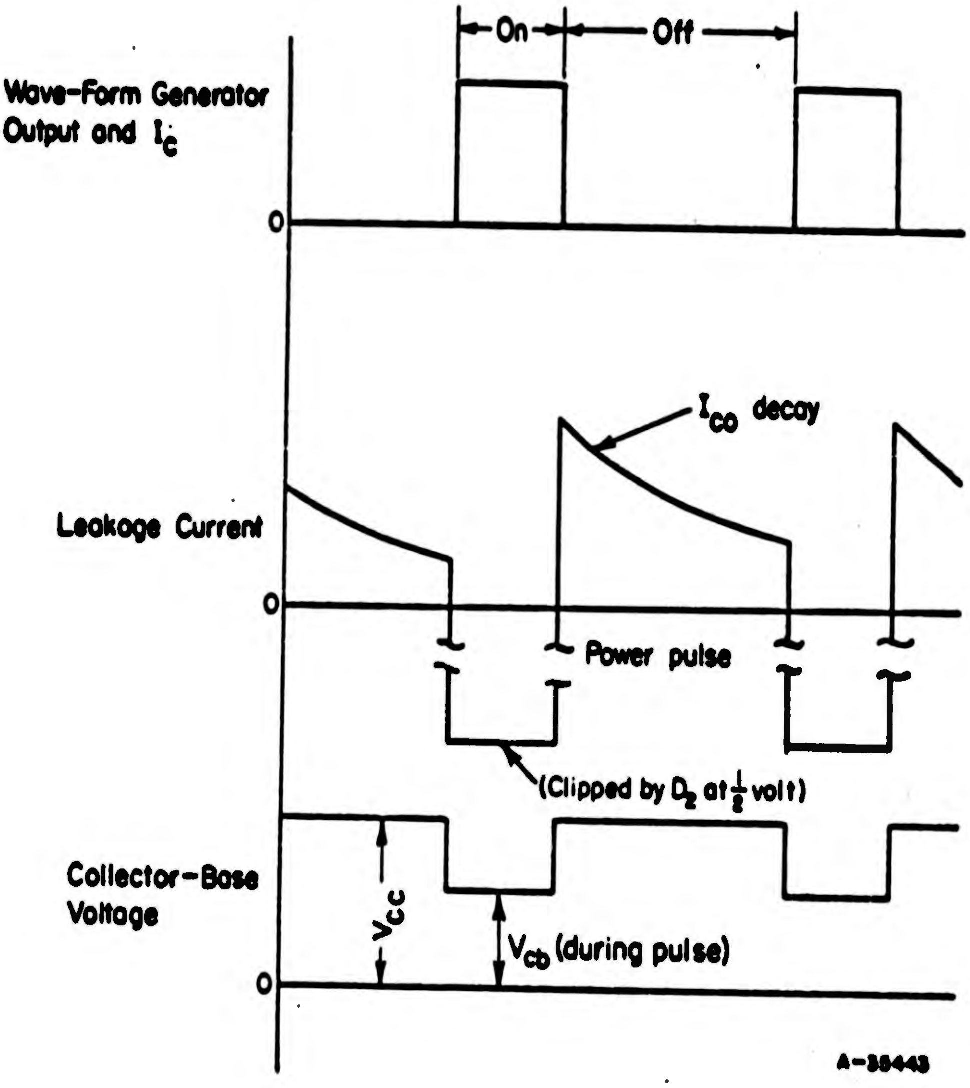


FIGURE 16. MEASURING-CIRCUIT WAVE SHAPES

At high junction temperatures, I_{co} is a large portion of the total collector current. This makes the transistor highly susceptible to thermal runaway. An instantaneous increase in I_c from pickup or other sources results in an instantaneously higher junction temperature and thus, a greater I_{co}. The point is reached where the value of the product of I_{ce} and the collector voltage (leakage power) is sufficient to raise the junction temperature without any power dissipation from other sources. This process "snowballs" and the transistor is destroyed.

Two basic approaches can be used to eliminate or reduce the problem of thermal runaway: the maximum-junction-temperature test condition may be reduced, or the transistor may be protected by an external circuit.

It has been found that measurements in which the peak junction temperature is raised only to 115 C for silicon transistors or to 55 C for germanium transistors will eliminate the instability which occurs at peak junction temperatures approaching the manufacturer's recommended maximum. Several approaches were tried to develop protective circuits which would enable measurements to be made involving higher peak temperatures. Such attempts were not successful.

Spurious Oscillation and 60-Cycle Pickup. The measurement circuit seems to be prone to oscillations in various modes and at various frequencies. No universal cure for this problem has been found. However, for each individual transistor type measured it was possible to eliminate the oscillation through careful lead placement (different for each type), grounding procedures, and capacitive shunting. It was also possible to eliminate 60-cycle pickup by various grounding methods, but here again the procedure required varied for different transistor types.

Inability to Monitor I_{co} Accurately. The success of the experiment depends on the precise monitoring of I_{co}. It would be desirable to measure I_{co} at the exact instant that the driving power is removed from the transistor. After that time I_{co} decreases as the junction heat flows away. However, a delay of 100 to 200 microseconds was experienced before I_{co} could be measured. The delay is the result of the forward voltage drop across D_2 occurring during the power pulse which must die out before the reverse polarity $I_{co}R_b$ voltage becomes readable. The magnitude of this delay is determined by the time constant of R_b and the oscilloscope input capacitance. As was mentioned earlier, this consideration is important in selecting the value for R_b.

It is possible to extrapolate the I_{co} decay curve back to the time of switching to obtain a more nearly correct value of I_{co}max. This procedure was used in all reported experimental work.

Comparison of Experimental and Analog Data

To facilitate comparison of the experimental data and the analog data, a special set of readings was taken from the analog to exactly correspond with the conditions of the experiment. The experimental and analog data are presented in Figures 17 through 21. The analog results are shown by the dashed curves, and the experimental results are shown by the solid curves. The experimental data for several specimens of each transistor type are shown. For the single pulse data, the analog data are shown by the circles and the experimental data are shown by the x's.

In each case, the analog cooling curve and the verification measurements are made on transistor samples supplied by the same manufacturer, although different sets of transistors were used for obtaining the average cooling curve and for the individual experimental measurements. This occurred because the original samples used for obtaining the analog cooling curves were destroyed by thermal runaway when attempts were first made to obtain experimental data.

For transistor types 2N335, 2N341, and 2N697, no analog data could be obtained at 1000 cycles per second repetition rate because it was necessary to change the time base of the analog to get reasonable analog network circuit constants. For transistor type 2N341, no experimental data could be taken at 1000 cycles per second repetition rate because of the masking effects of the I_{co} decay curves.

It can be seen from the curves of Figures 17 through 21 that some of the analog results lie above and some below the experimental results. This raises the question: what are the possible sources of error in both the experimental and the analog data?

Sources of Error in the Verification Experiment

Three types of possible sources of error were present.

(1) Incorrect Estimation of Peak Junction Temperature

As explained above, it was necessary to project the exponential I_{co} decay curve visually presented on the oscilloscope back to its point of origin the instant at which the driving-power pulse was removed from the transistor. The value of I_{co} is used as an indicator of transistor junction temperature. If the estimated projection of the I_{co} curve is incorrect, the assumed peak junction temperature is also incorrect. For example, if I_{co} is projected so as to indicate a peak value lower than it actually is, the temperature as measured is lower than it actually is, the temperature to which the operator will raise the junction prior to measurement of required power will be excessively high, and therefore, the measured power input will be higher than it should be for the assumed junction temperature. The reverse is also true; if the I_{co} curve is projected higher than it actually is, the measured input power will be lower than it should be.

This problem could be a source of considerable error, but as yet it has not been possible to determine the magnitude of this error as it has been impossible to observe the first part of the I_{co} decay curve. All indications, both theoretical and experimental, point to an exponential I_{co} curve, and this was assumed in making the projections. It should also be pointed out that, at higher temperatures, I_{co} changes very rapidly as temperature varies and hence, a fairly large error in monitoring I_{co} will lead to a relatively small error in junction temperature.

(2) Oscilloscope-Reading Errors

Because all measurements were concerned with the magnitude of certain parts of a complex wave form, it was necessary to take all measurements by means of a

1

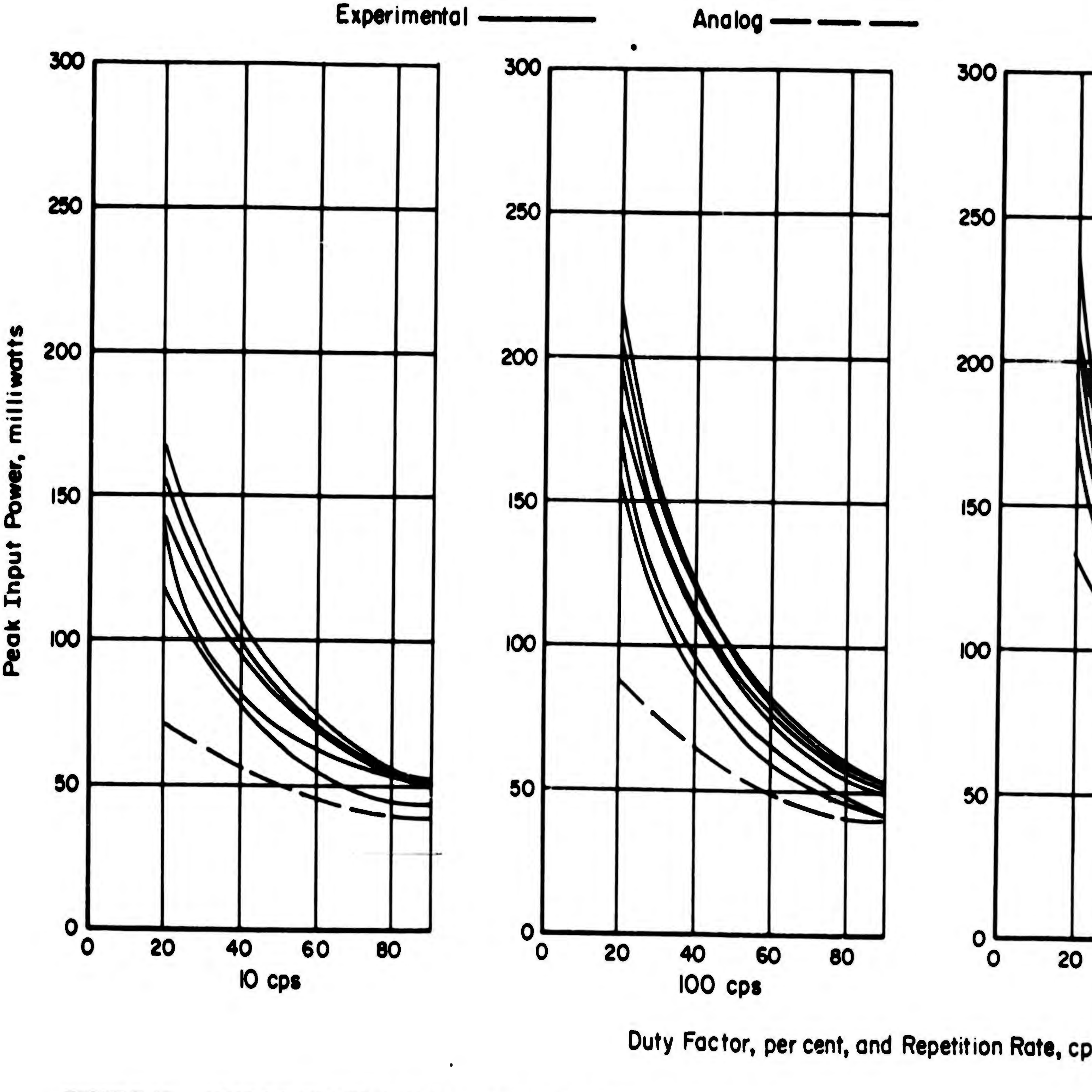
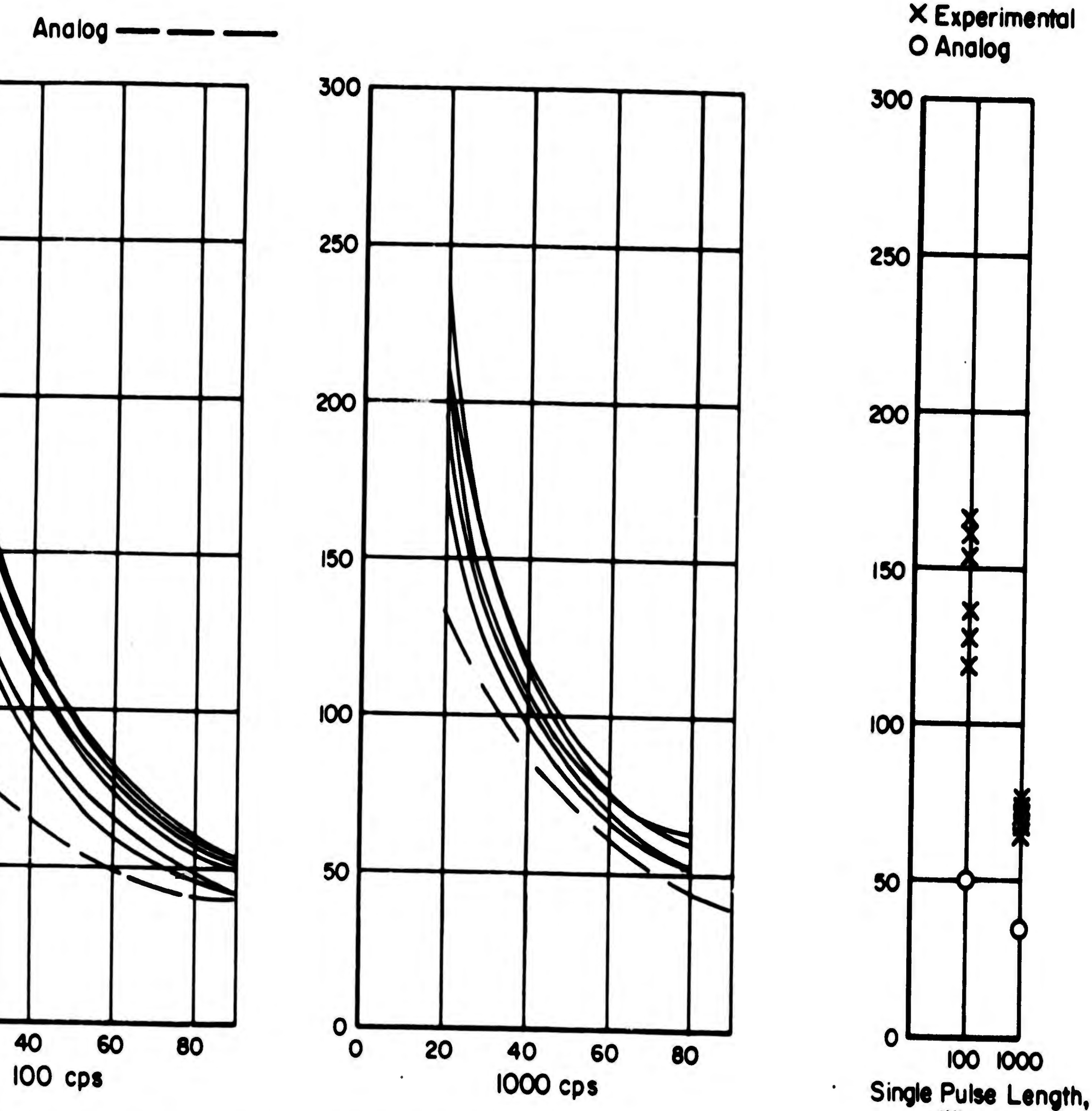


FIGURE 17. ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N167

2



y Factor, per cent, and Repetition Rate, cps

A-36188

YPE 2N167

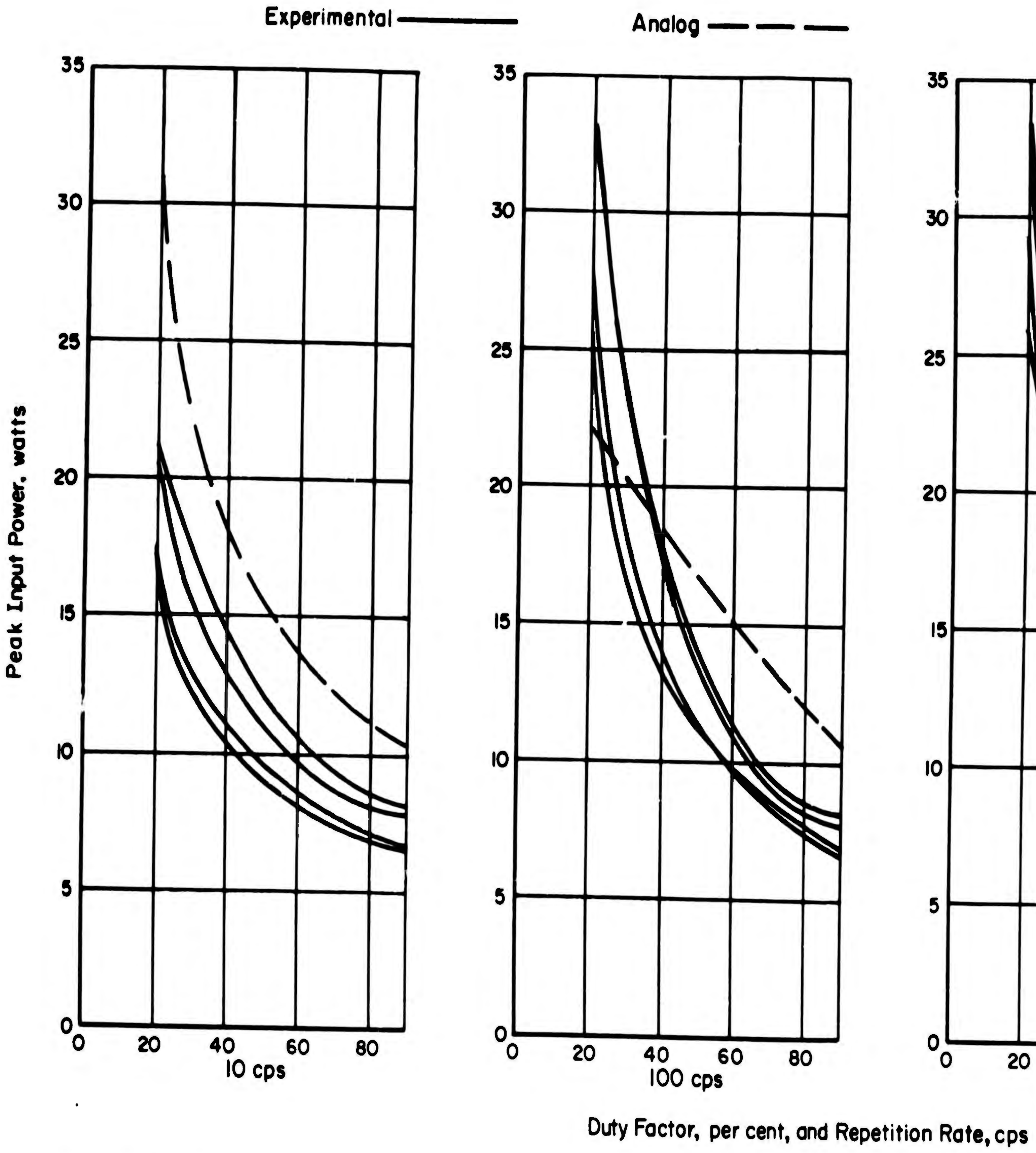
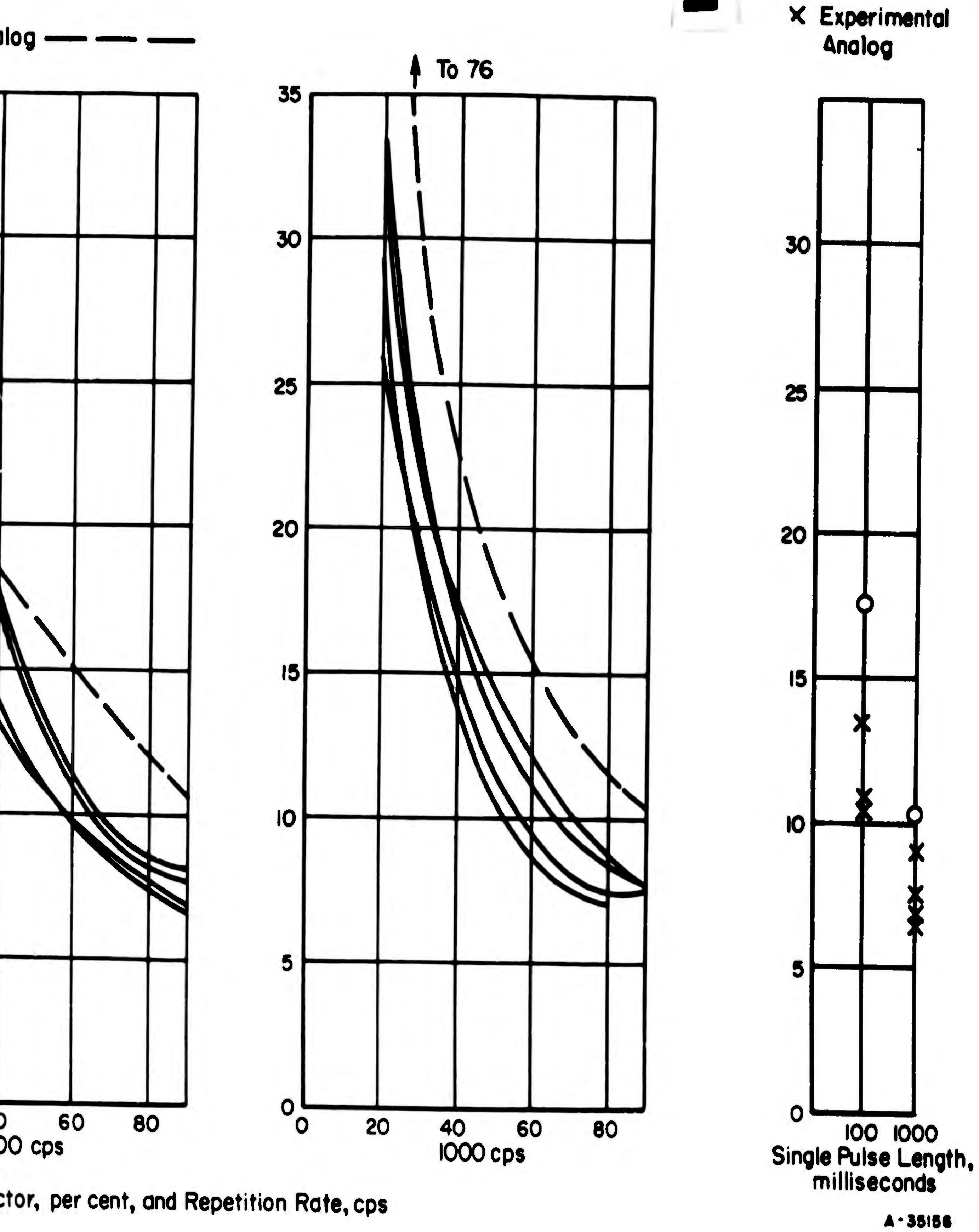


FIGURE 18. ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N326

2



A-35156

E 2N326

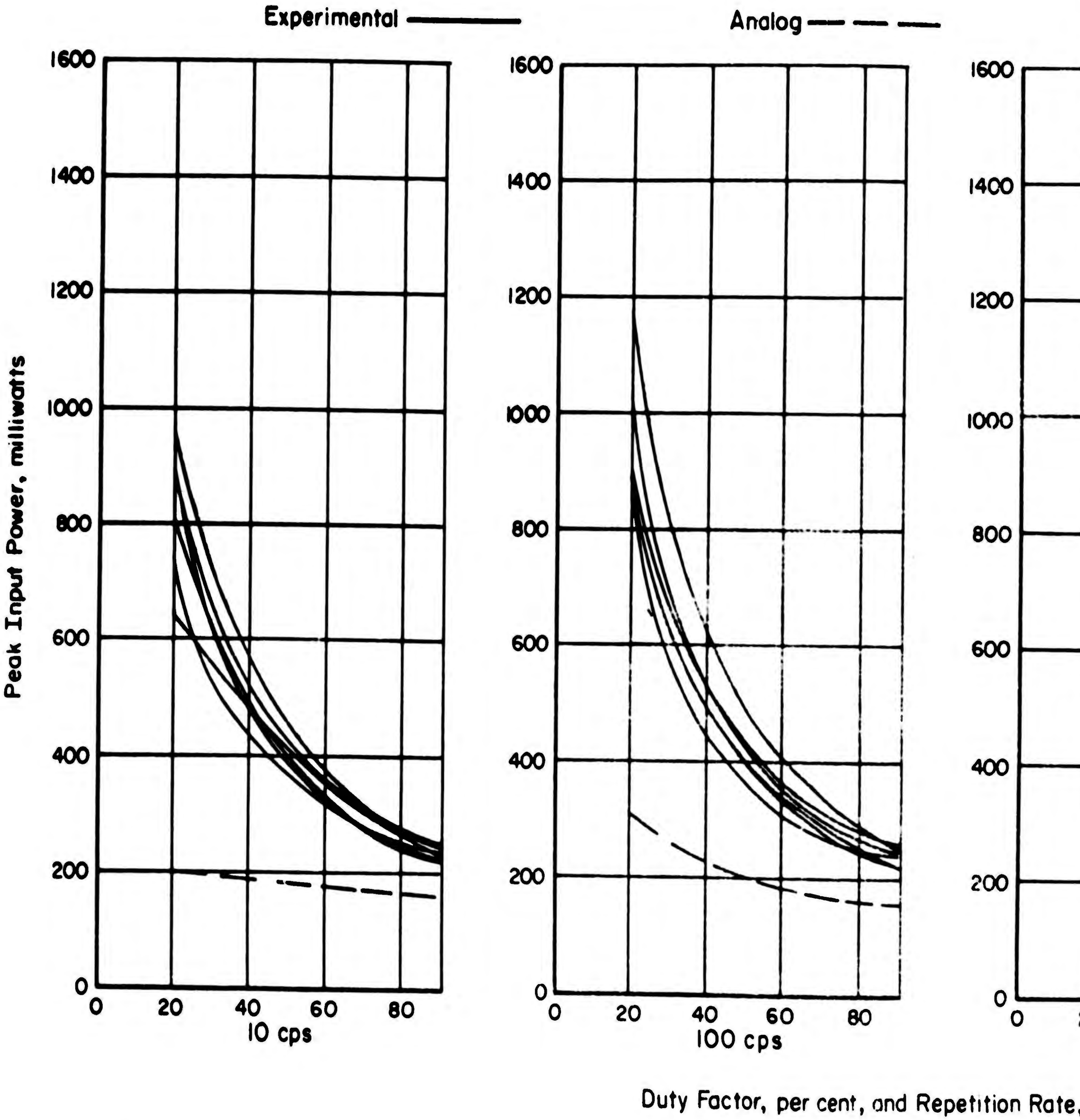
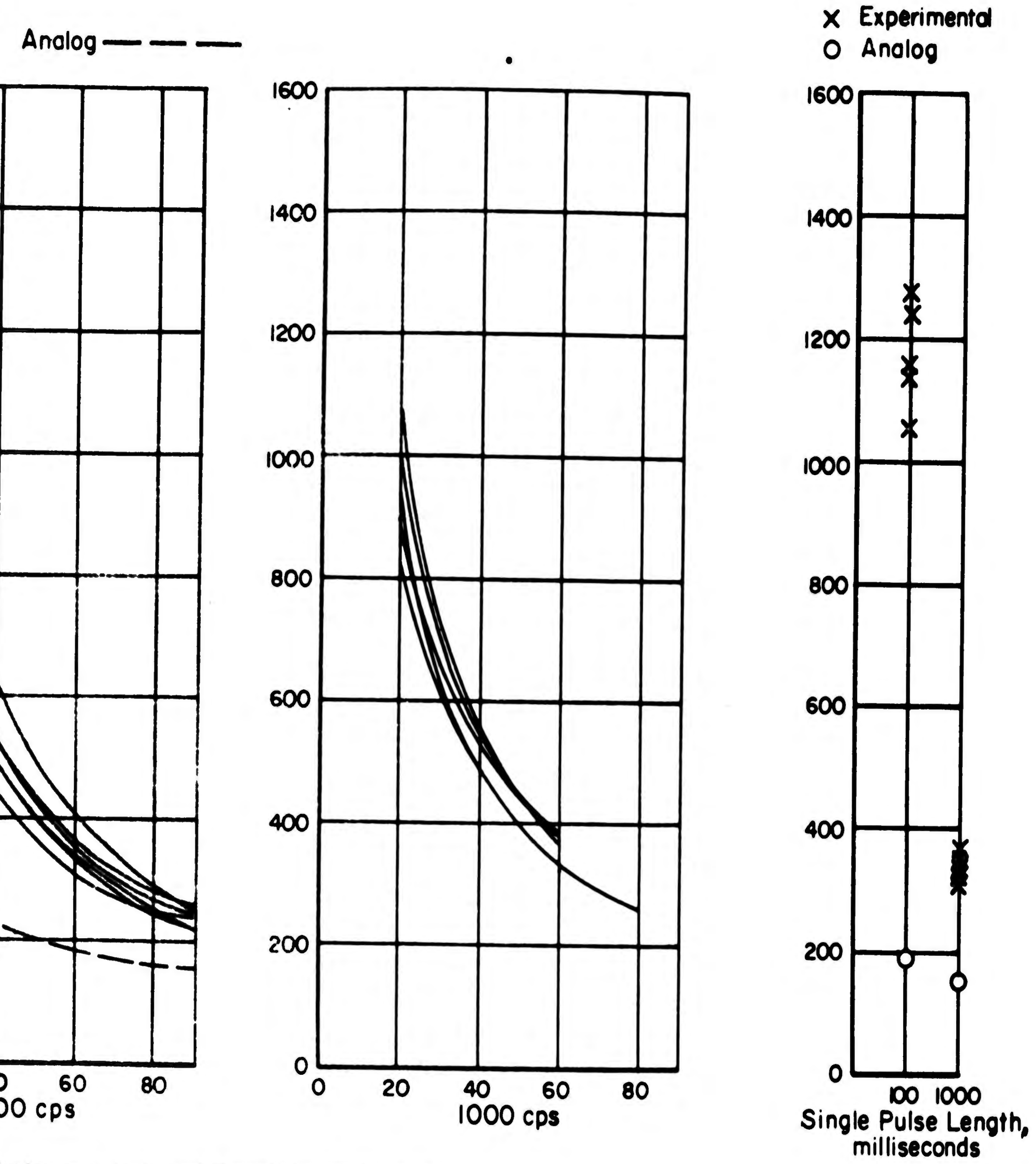


FIGURE 19. ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N335

2



actor, per cent, and Repetition Rate, cps

2N335

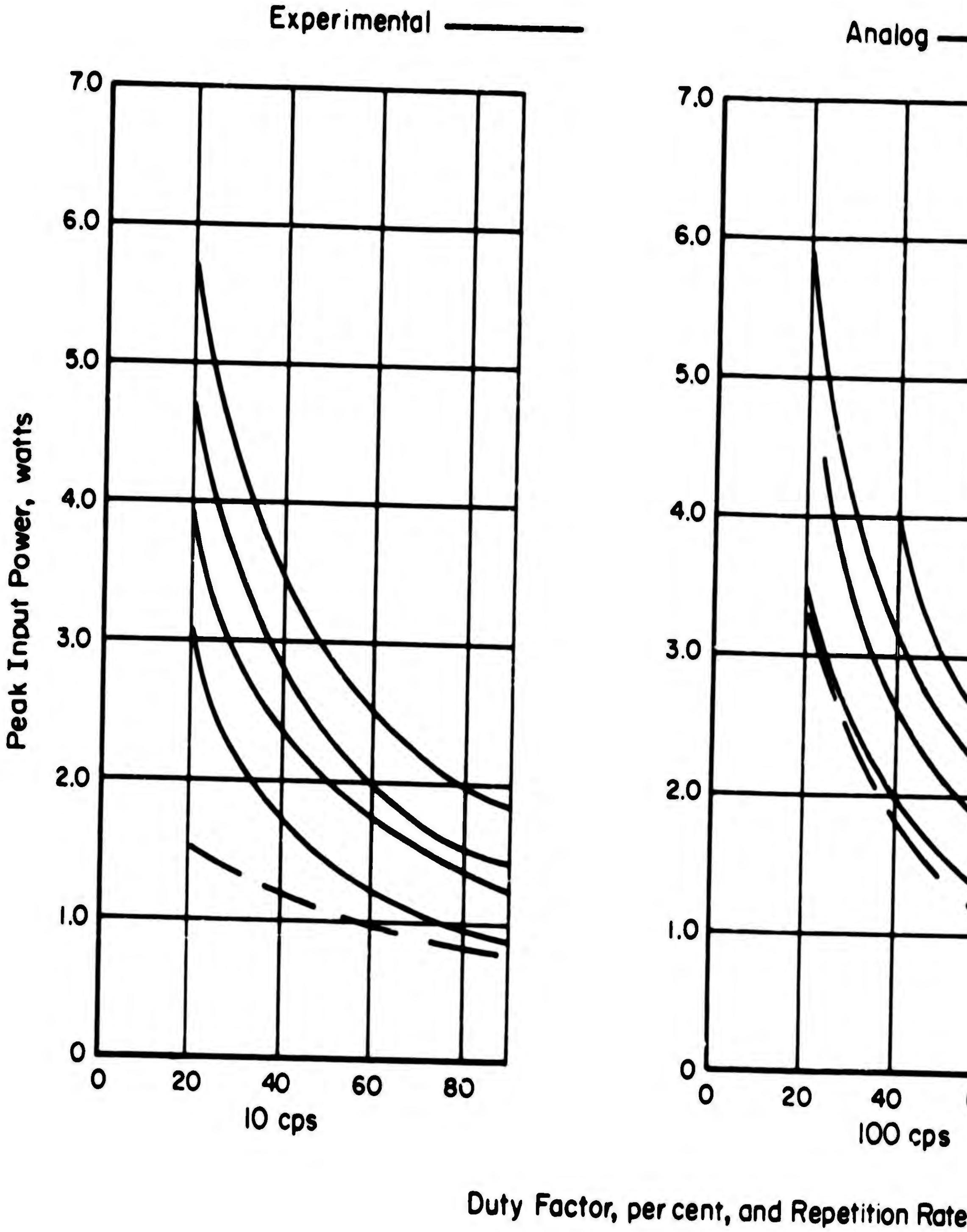
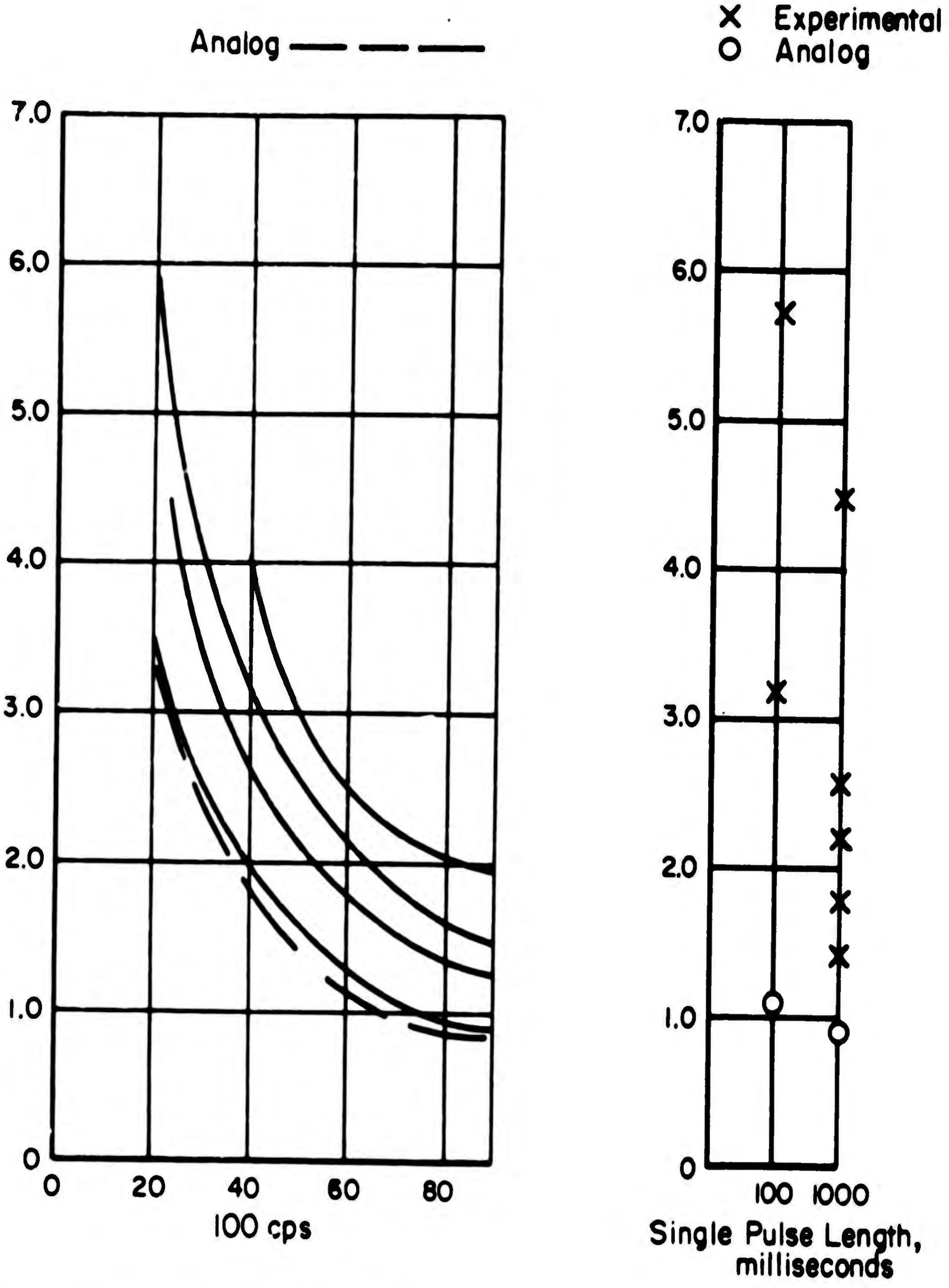


FIGURE 20. ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N341

2



tor, per cent, and Repetition Rate, cps

A-36158

OMPARISON, TYPE 2N341

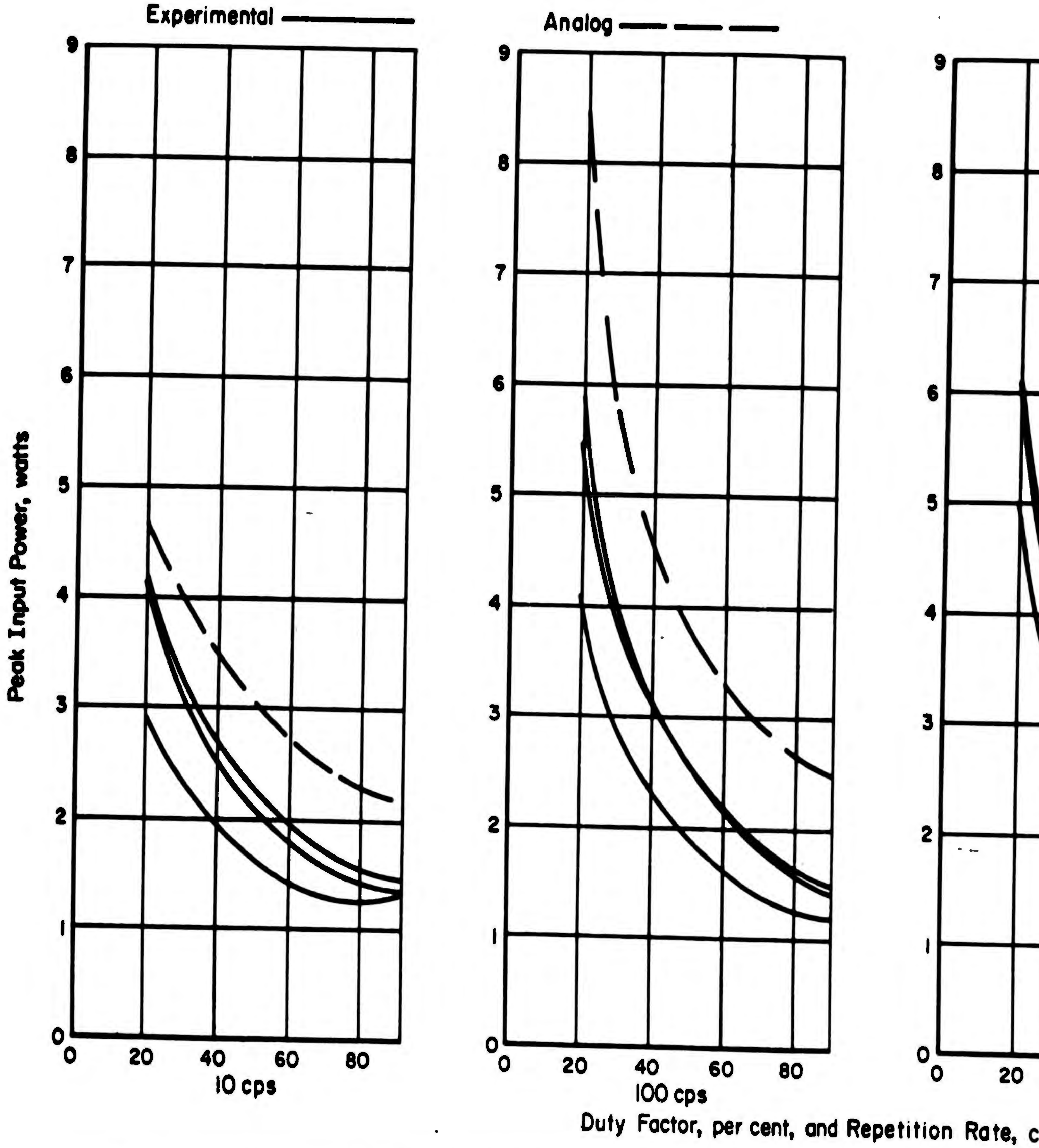
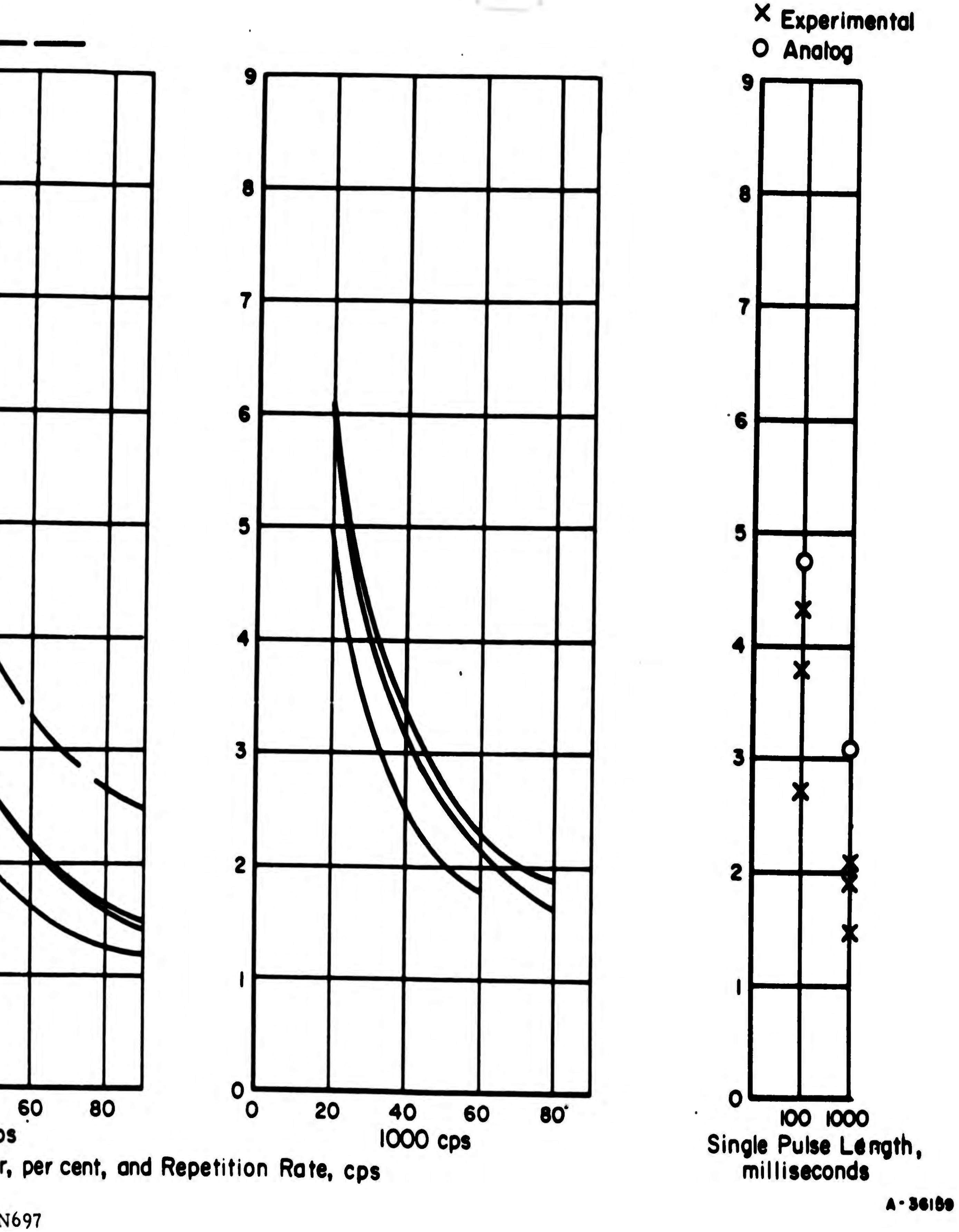


FIGURE 21. ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N697

2


× Experimental
O Analog
9
8
7
6
5
4
3
2
1
0
60
80
ps
0
20
40
60
80
1000 cps
r, per cent, and Repetition Rate, cps
9
8
7
6
5
4
3
2
1
0
100
1000
Single Pulse Length,
milliseconds
A-36159

N697

calibrated oscilloscope. Quantitative measurements made with an oscilloscope are subject to error due to:

(1) Miscalibration

(2) Parallax

(3) Shift of the zero reference.

Particularly bothersome was the shift in the d-c zero reference. This shift seems to be related to the average value of the observed waveform, so that one may obtain a zero reference, apply the signal, and then observe the zero again and find it has shifted. After several seconds, the zero again drops back to where it was before the signal waveform was applied. This effect probably produced errors in the neighborhood of 10 per cent of the quantity being measured.

(3) Lack of Precision

Other errors may have been introduced by possible inaccurate calibration of meters and of the precision resistor R_c. It would seem reasonable to assume that any errors of this type would be considerably smaller than those attributable to the projection of the I_{co} curve and to inaccurate oscilloscope reading.

Measurements seemed to be repeatable to within about ± 10 per cent. The difference between trials may be largely attributed to errors in reading the oscilloscope, as the other factors would tend to cause a constant shift in the readings. An average of several trials was made to obtain each of the recorded values.

Special 2N335 Experiment

An attempt was made to obtain a cooling curve for the 2N335 transistor using a solid-state switching circuit (see Appendix E, Figure E-1), rather than the relay circuit. In this manner, it was possible to obtain much more of the first part of the cooling curve. In this special study the cooling curve of only one sample was obtained, and verification measurements were made on the same sample. The results are shown in Figure 22.

This experiment was not entirely conclusive because considerable delay was still present before I_{co} could be measured. This delay was approximately 1 millisecond as compared with 2 milliseconds for the relay method. The reason for such a high delay was that the General Electric transistor used exhibited a very low I_{co}, much lower than that of the Texas Instrument transistors employed in the earlier measurements. This low I_{co} meant that a high R_b was needed, which lead to a high RC time constant. This effect is explained in more detail in the section of the report concerning the verification experiment, which employs a similar circuit.

Nevertheless, this technique seems to produce fairly close agreement between experimental and analog results, and leads one to be optimistic about the performance of the revised analog technique as outlined in Appendix E. This revised technique should further reduce the delay before the I_{co} decay curves become readable.

An interesting sidelight resulted from this special study. As can be seen by comparing the curves of Figure 22 with those of Figure 19, a great deal of difference exists among the thermal properties of the 2N335 transistors made by different manufacturers. This can probably be attributed to the so-called "fixed-bed mounting" used by General Electric. Although this construction was apparently developed to improve the mechanical reliability of these transistors, it seems also to have superior thermal properties. This brings out the advantages of good thermal design of electronic components. Clearly, improving thermal properties can increase the power-handling ability of otherwise electrically identical transistors.

The difference between the power-handling abilities of transistors from the two manufacturers is especially pronounced in these data because the transistors were mounted in such a way that an almost infinite heat sink was available. Thus, the greater part of the total thermal resistance was in the transistors. Under more realistic conditions, the thermal resistance between the transistor case and ground is considerably higher, and the improvement in power-handling capabilities gained by reducing internal thermal resistance would be less pronounced.

It is also clear that one cannot experimentally determine the power-handling capacity of a transistor type made by one manufacturer and expect it to apply to the same transistor type made by a different manufacturer.

Sources of Error in the Transistor Thermal Analog

Effect of Errors in Determining the Analog Network

The electrical networks used to represent the thermal response of the transistor in the analog are calculated from the transistor-junction cooling curves. The transistor junctions are heated by applying rated power to the collector junction. The power input is removed and the time decay of I_{co} is measured. This I_{co} as a function of time curve is converted to temperature as a function of time. From this temperature decay curve the thermal parameters of the equivalent circuit are computed. The thermal parameters are then converted to electrical parameters.

The equipment used to obtain the junction cooling curves was such that the first 2 milliseconds of the cooling curve was not recorded, and it was necessary to estimate the values of the first portion of the curves. This is probably the largest source of error in the transistor thermal analog.

The effects of this type of error were evaluated to the extent that a complete evaluation obviously would be very complex mathematically and beyond the scope of this project. The value of such a rigorous evaluation is questionable since the effort might be better spent in eliminating the source of the original error.

Other sources of error in the transistor thermal analog are very small by comparison with the error produced as the result of the use of an inaccurate cooling curve. When the experimental technique and equipment used to determine the cooling are

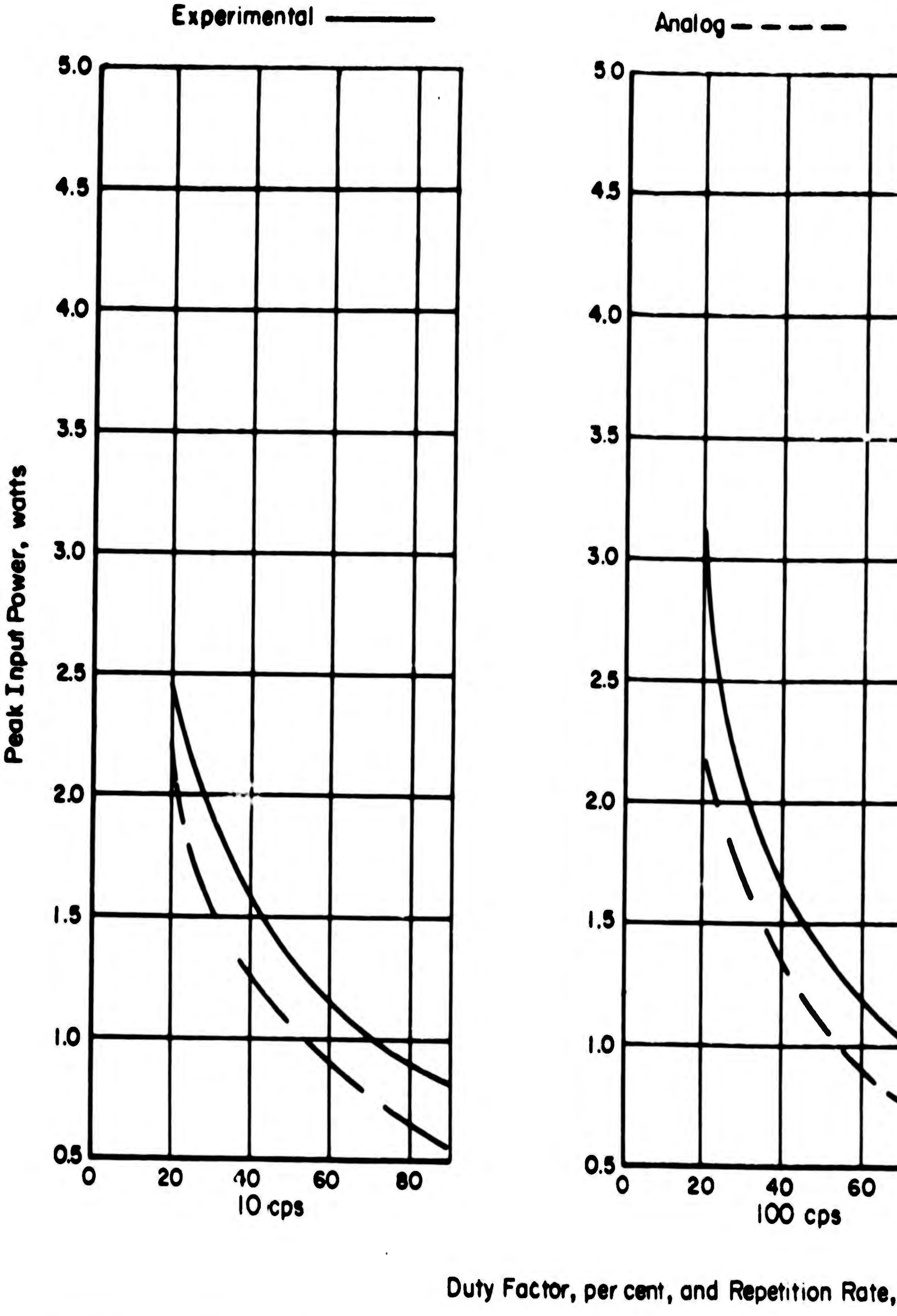
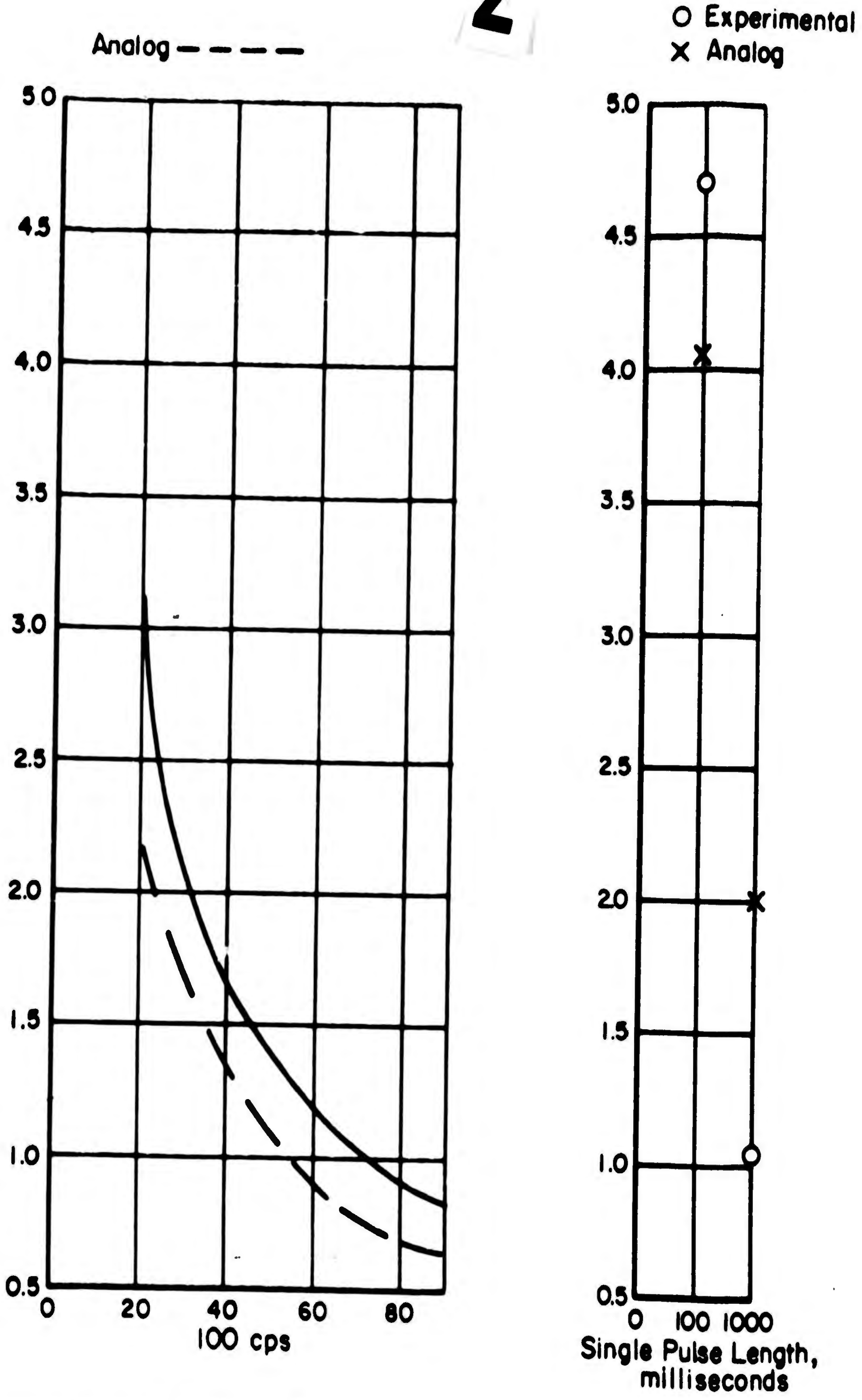


FIGURE 22. SPECIAL-STUDY ANALOG-EXPERIMENTAL COMPARISON, TYPE 2N335

2



tor, per cent, and Repetition Rate, cps

A-36160

ERIMENTAL COMPARISON,

INSTITUTE

improved, it will be necessary to improve the equipment which makes up the driving portion of the transistor thermal analog. These improvements are covered in Appendix E of this report.

Data upon which this report is based may be found in Battelle Laboratory Record Book No. 16628.

HTG:STK/nb

APPENDIX A

THERMAL- AND ELECTRICAL-EQUIVALENT CIRCUIT CONSTANTS

APPENDIX A

THERMAL- AND ELECTRICAL-EQUIVALENT CIRCUIT CONSTANTS

The purpose of this Appendix is to present the thermal and electrical circuit constants for the series string of parallel RC pairs equivalent circuit being used in the transistor thermal analog. The thermal-electrical unit equivalencies used for each transistor type are presented below each table.

TABLE A-1. 2N167 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	458.0	47.86	0.002287	2.186
2	103.1	10.77	0.0001815	0.1735
3	48.0	5.02	0.0000927	0.08862
4	23.85	2.49	0.0000413	0.03948

1°C/w = 104.5 ohms
1°C = 1.288 volts
1 w = 12.31 ma
1 w-sec/°C = 956 μf

TABLE A-2. 2N326 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	2.855	39.74	0.1342	9.634
2	1.250	17.40	0.03680	2.642
3	0.493	6.86	0.02475	1.777

1°C/w = 13.92 K-ohms
1°C = 1.392 volts
1 w = 0.1 ma
1 w-sec/°C = 71.79 μf

TABLE A-3. 2N335 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	373	25.99	0.001394	19.91
2	117	8.15	0.00002620	0.3741
3	516	35.95	0.000001728	0.0247

1°C/w = 69.67 ohms
1°C = 0.3502 volts
1 w = 5.0 ma
1 w-sec/°C = 14280 μf

TABLE A-4. 2N341 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	54.2	22.66	0.03275	78.27
2	23.1	9.66	0.00195	4.661
3	72.2	30.18	0.0002244	0.5363

1°C/w = 418 ohms
1°C = 0.3361 volts
1 w = 0.8 ma
1 w-sec/°C = 2390 μf

TABLE A-5. 2N384 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	240.0	50.16	0.004440	2.122
2	34.30	7.17	0.0007040	0.3365
3	41.70	8.72	0.0000522	0.02495

1°C/w = 209.0 ohms
1°C = 1.395 volts
1 w = 6.667 ma
1 w-sec/°C = 4780 μf

TABLE A-6. 2N502 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	400.0	27.87	0.0001582	2.268
2	68.8	4.79	0.0006057	8.686
3	484.0	33.72	0.000007196	0.1032

1°C/w = 69.97 ohms
1°C = 2.232 volts
1 w = 32.0 ma
1 w-sec/°C = 14340 μf

TABLE A-7. 2N647 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	62.0	25.92	0.02320	55.45
2	21.0	8.78	0.003175	7.588
3	14.0	5.85	0.0007520	1.797
4	2.62	1.10	0.0009050	2.163
5	31.8	13.29	0.0000204	0.04876

Analog operates 10 times faster than real time
1°C/w = 418 ohms
1°C = 3.347 volts
1 w = 8.0 ma
1 w-sec/°C = 0.239 farads

TABLE A-8. 2N697 EQUIVALENT CIRCUIT CONSTANTS

Network	Resistance		Capacitance	
	°C/W	K-Ohms	W-Sec/°C	Microfarads
1	49.35	41.26	0.03420	40.93
2	8.95	7.48	0.003732	4.46
3	20.50	17.14	0.0001844	0.221

1°C/w = 836 ohms
1°C = 0.3348 volts
1 w = 0.4 ma
1 w-sec/°C = 1196 μf

APPENDIX B

TRANSISTOR THERMAL OPERATING CHARACTERISTICS TAKEN FROM THE TRANSISTOR THERMAL ANALOG

LIST OF FIGURES IN APPENDIX B

Transistor Type	Collector Voltage, volts	Ambient Temperature, C	Pulse Period, milliseconds	Wave Shape	Figure Number
2N326	15	65	10	Saw	B-38
2N326	30	65	10	Saw	B-38
2N326	15	25	100	Square	B-39
2N326	30	25	100	Square	B-39
2N326	15	65	100	Square	B-40
2N326	30	65	100	Square	B-41
2N326	15	25	100	Saw	B-42
2N326	30	25	100	Saw	B-42
2N326	15	65	100	Saw	B-43
2N328	30	65	100	Saw	B-43
2N335	Not specified	Not specified	SS	Square	B-44
2N335			SS	Saw	B-45
2N335			10	Square	B-46
2N335			10	Saw	B-47
2N335			100	Square	B-48
2N335			100	Saw	B-49
2N335			1000	Square	B-50
2N335			1000	Saw	B-51
2N341			SS	Square	B-52
2N341			SS	Saw	B-53
2N341			10	Square	B-54
2N341			10	Saw	B-55
2N341			100	Square	B-56
2N341			100	Saw	B-57
2N341			1000	Square	B-58
2N341			1000	Saw	B-59
2N697			SS	Square	B-60
2N697			10	Square	B-61
2N697			100	Square	B-62
2N697			1000	Square	B-63
2N502	<20	25	SS	Square	B-64
2N502	<20	65	SS	Square	B-65
2N502	<20	25	10	Square	B-66
2N502	<20	65	10	Square	B-67
2N502	<20	25	100	Square	B-68
2N502	<20	65	100	Square	B-69
2N502	<20	25	1000	Square	B-70
2N502	<20	65	1000	Square	B-71

(a) Single shot.

(b) 

APPENDIX B

TRANSISTOR THERMAL OPERATING CHARACTERISTICS TAKEN FROM THE TRANSISTOR THERMAL ANALOG

This Appendix presents the thermal operating characteristics as taken from the transistor thermal analog.

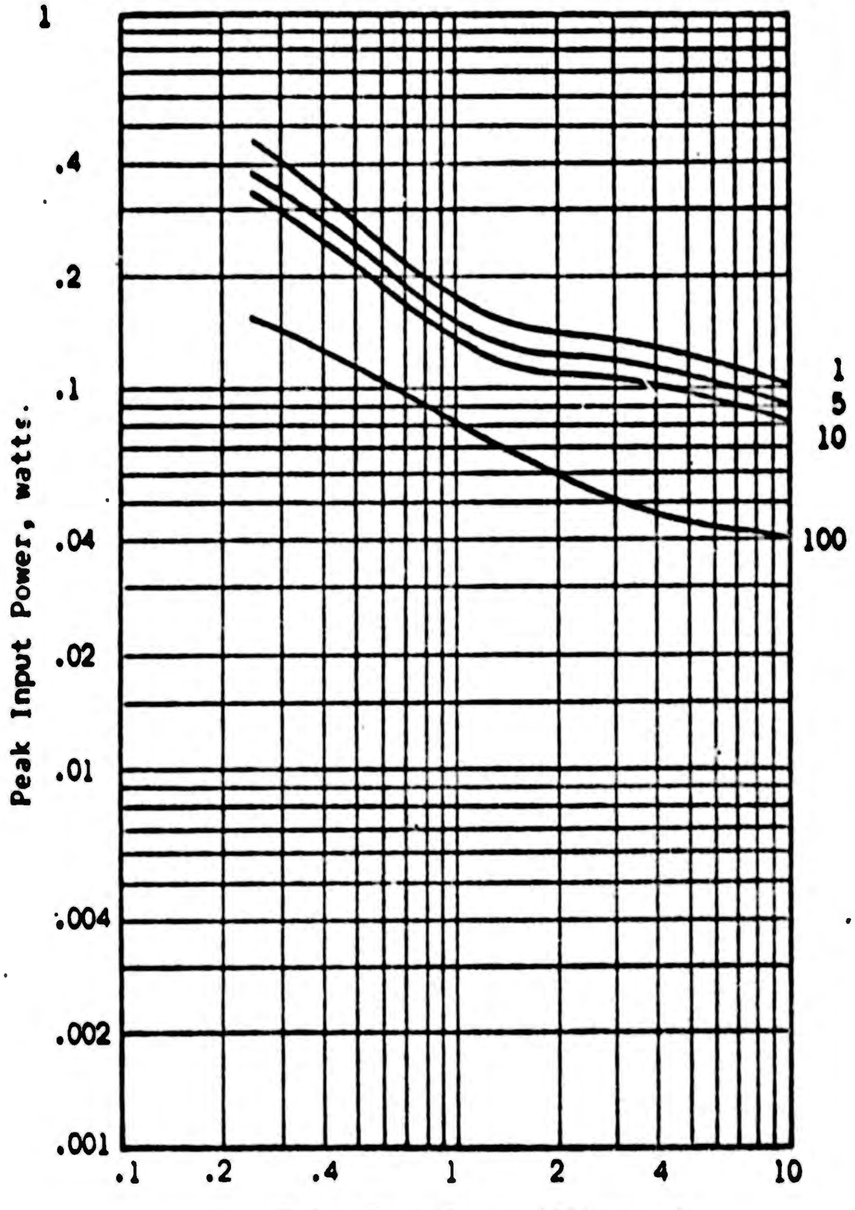


FIGURE B-1A 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

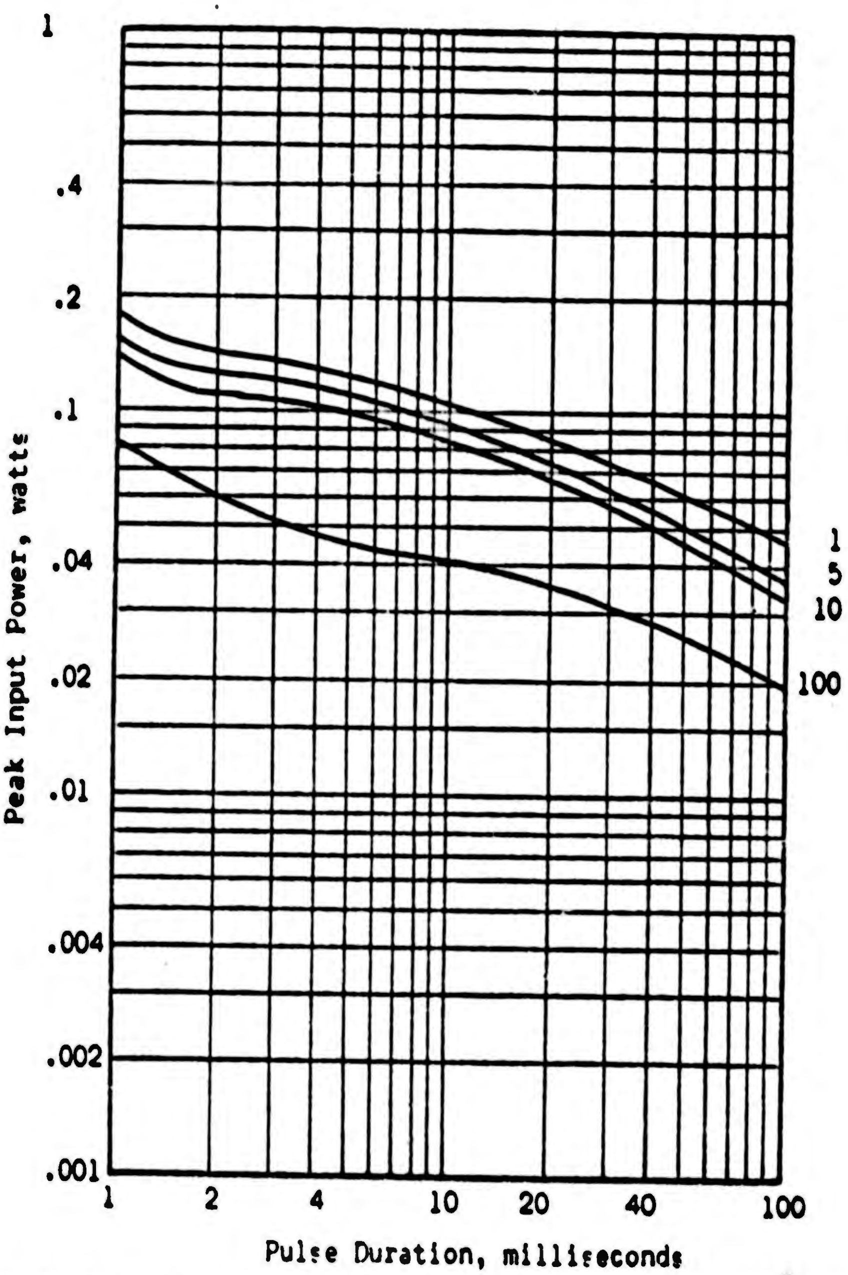


FIGURE B-1B 2N167 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

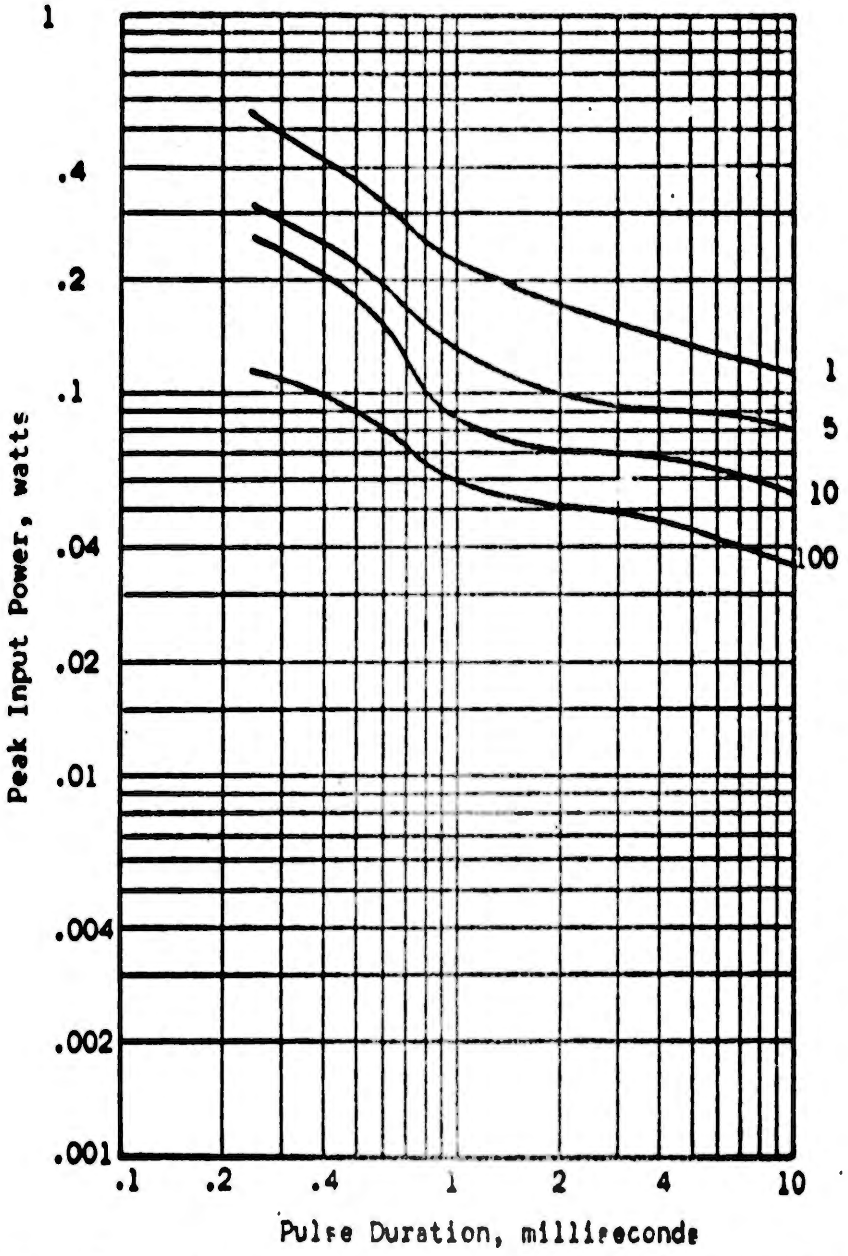


FIGURE B-2A. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

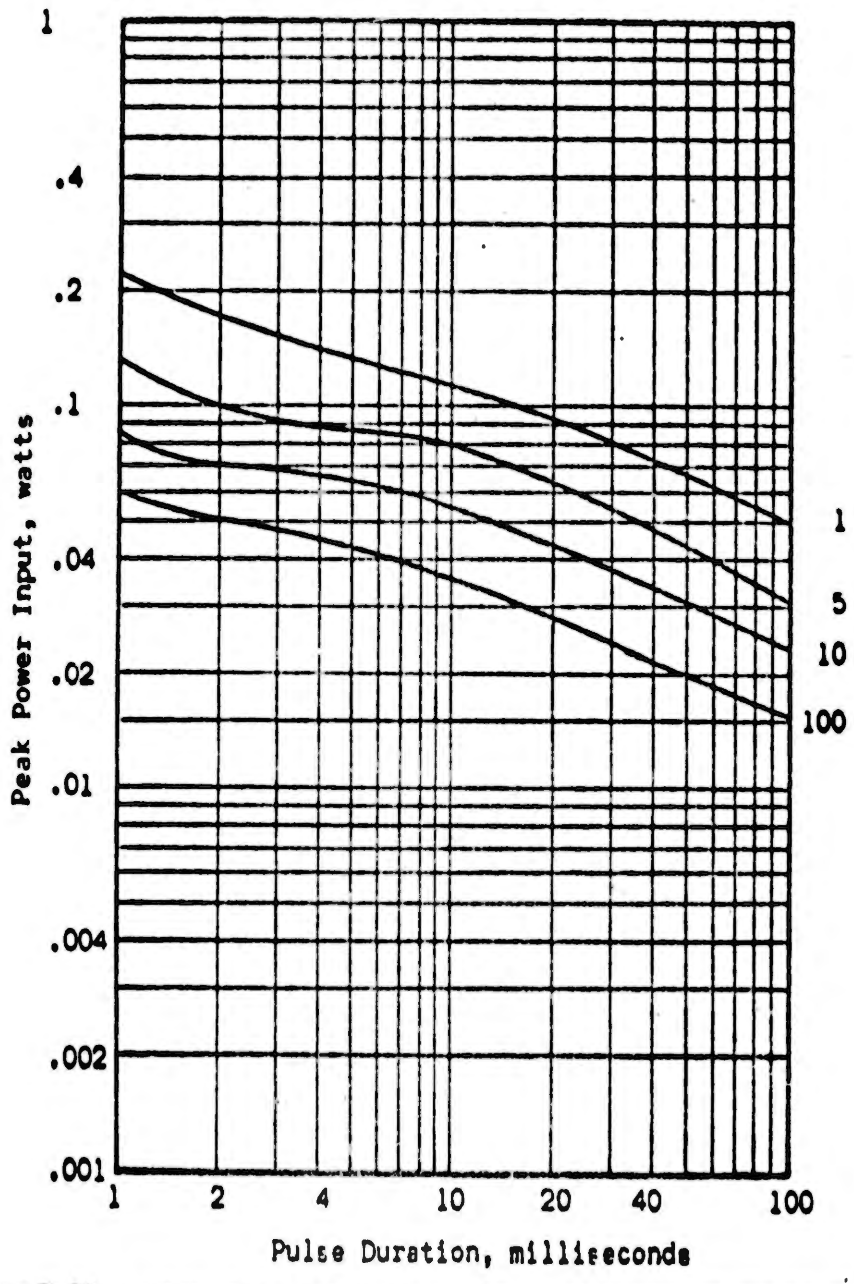


FIGURE B-2B. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

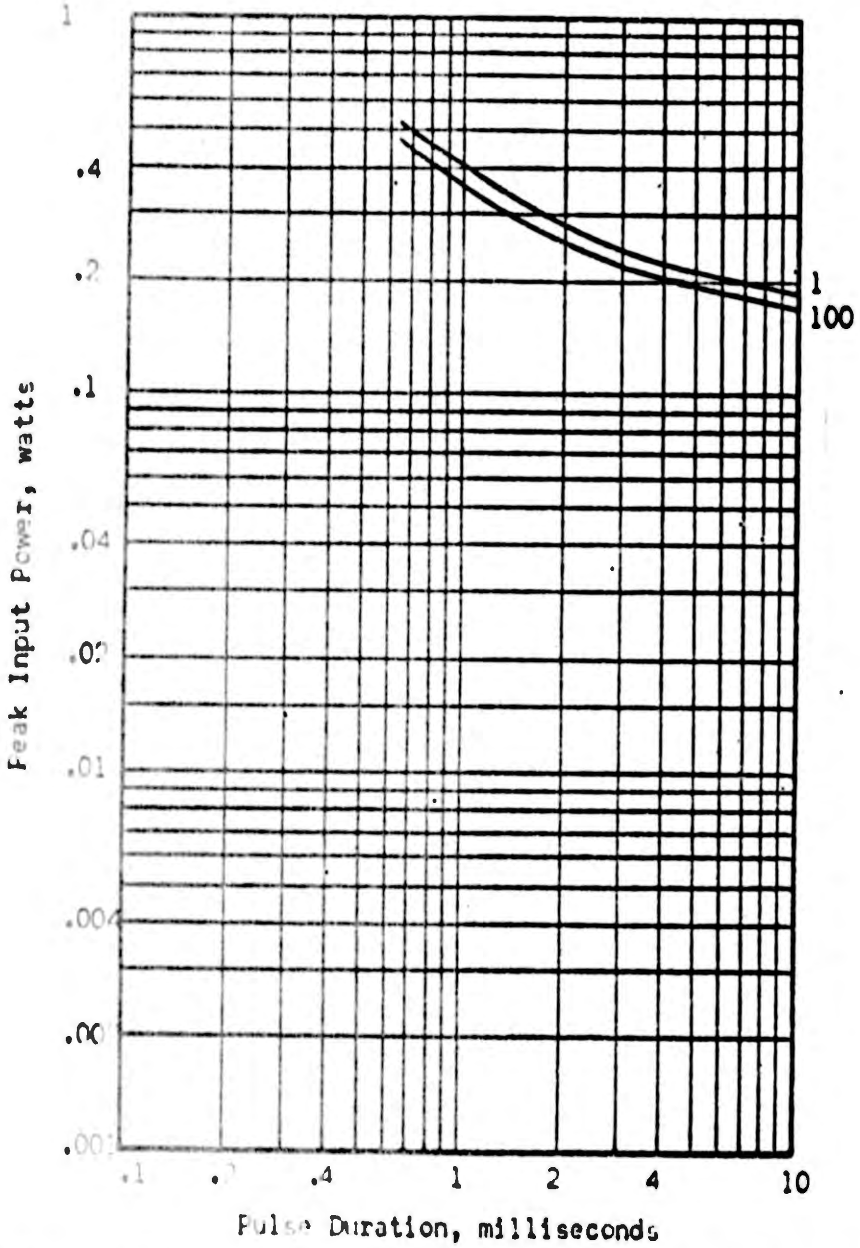


FIGURE B-[illegible]A. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100.

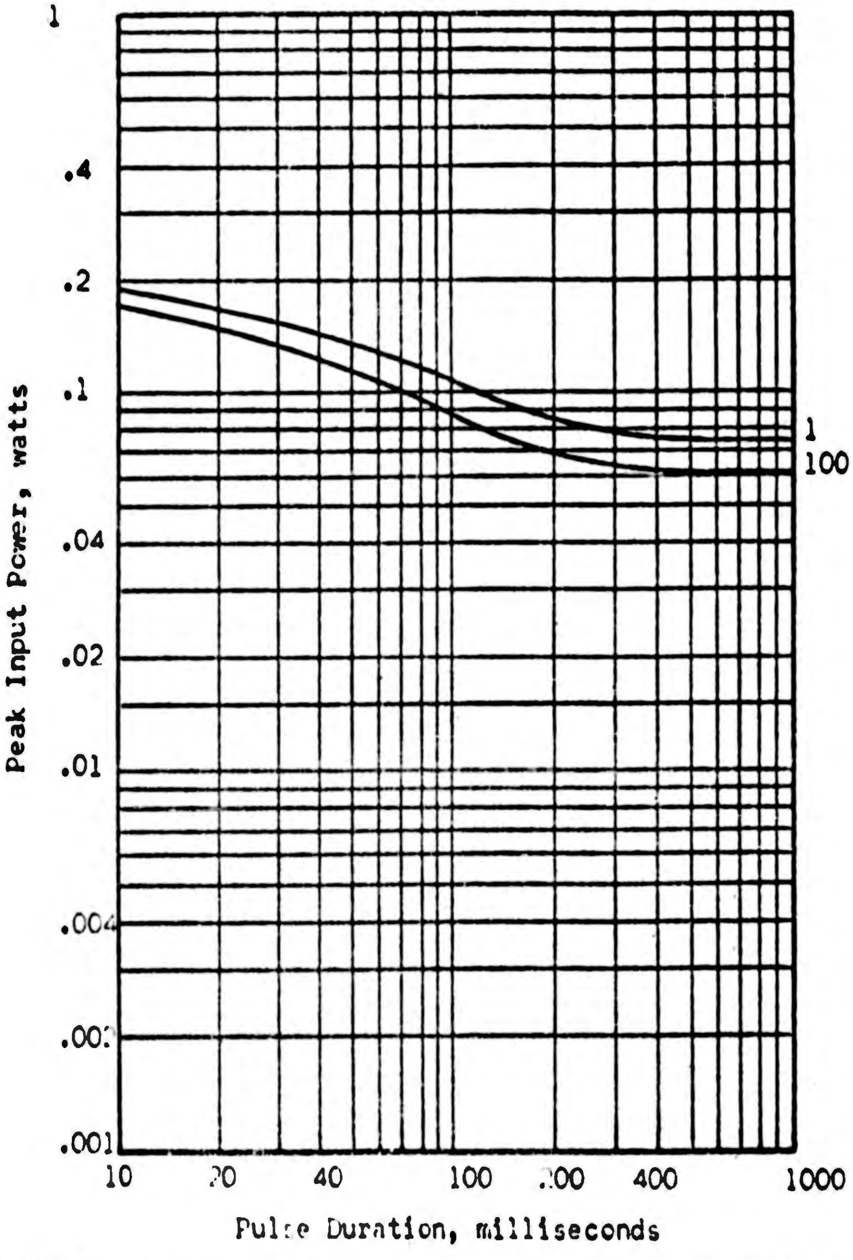


FIGURE B-3B. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

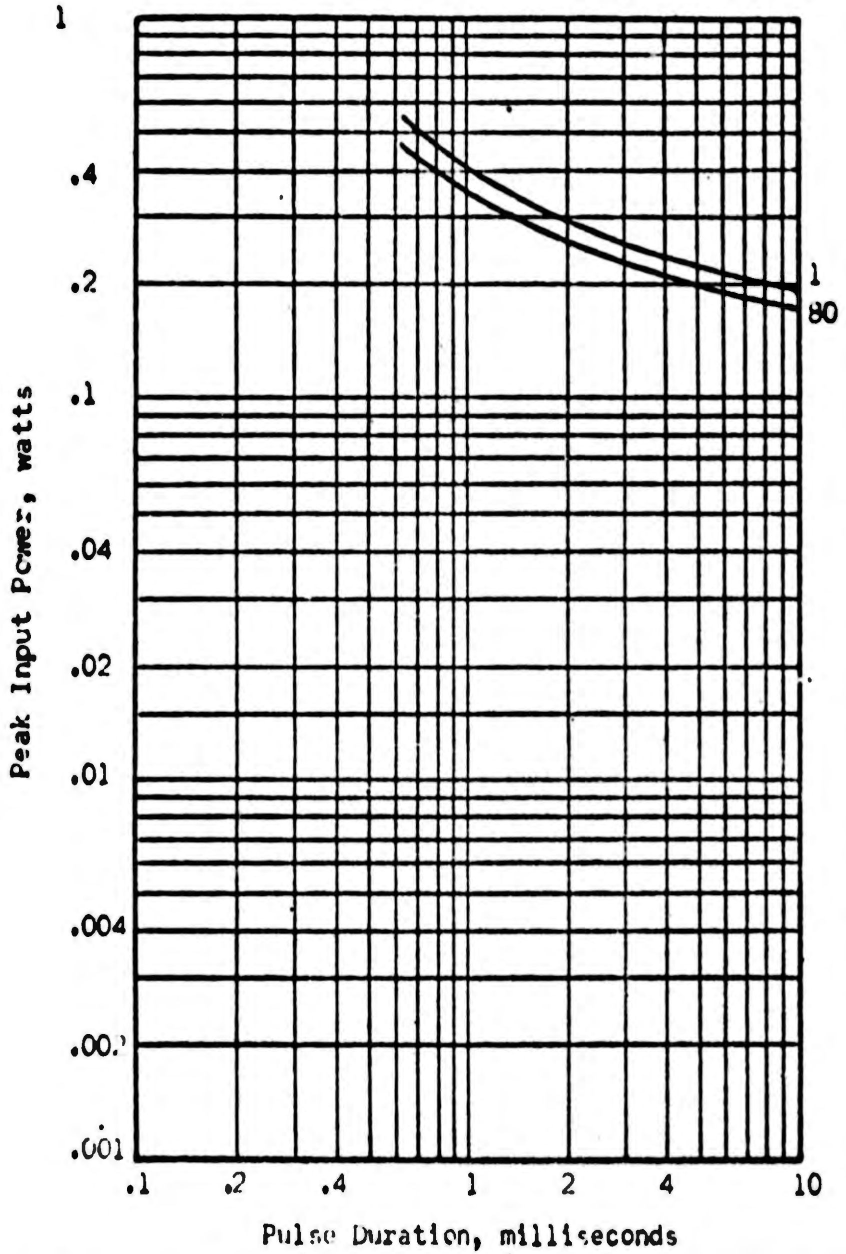


FIGURE B-4A. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal runaway with zero input for S = 82

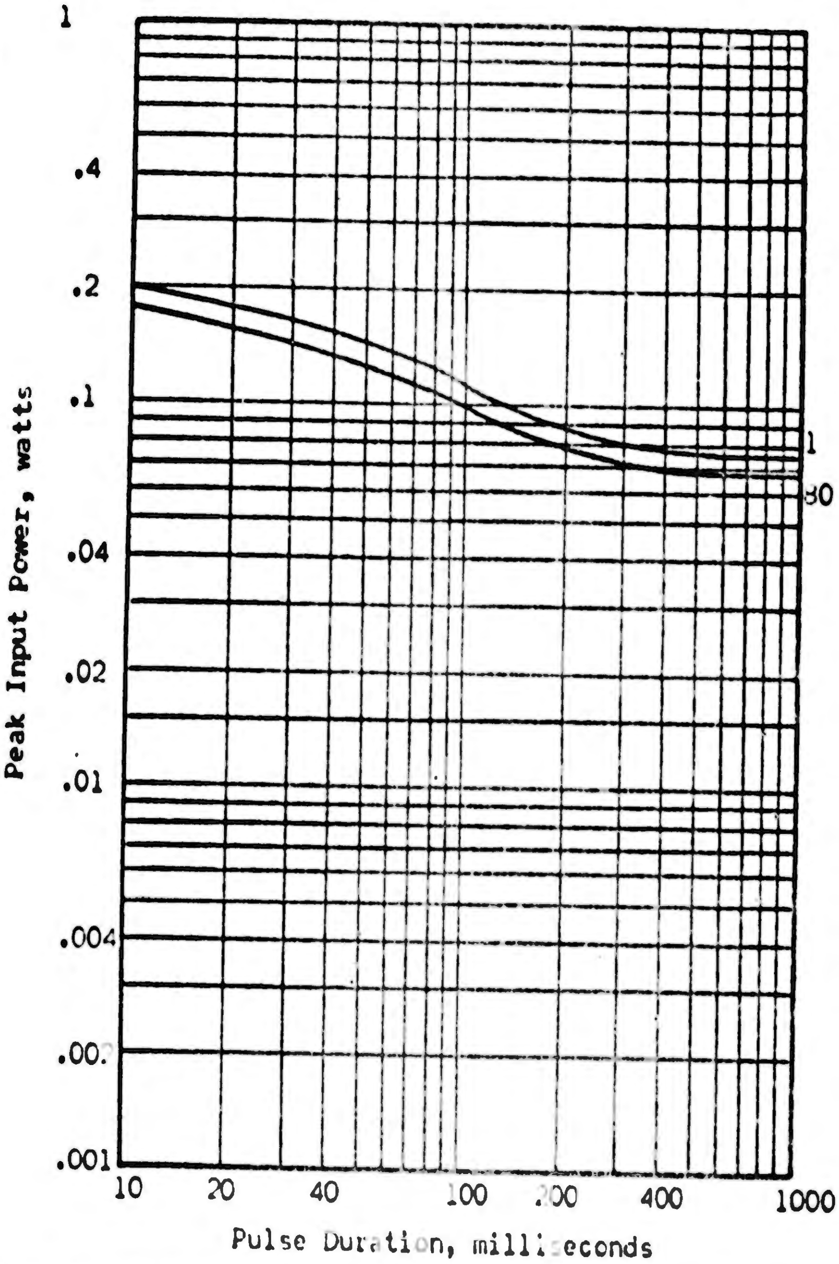


FIGURE B-4B. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal runaway with zero input for S = 80

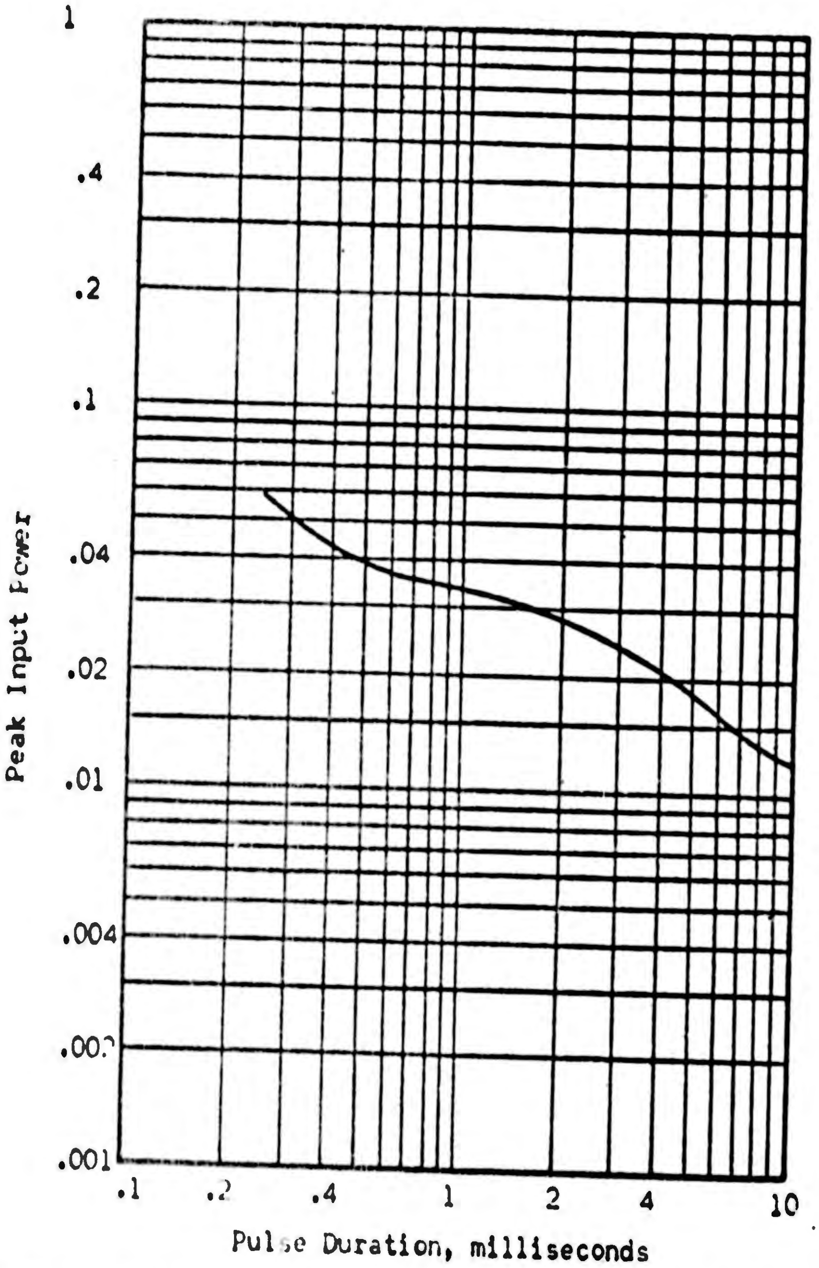


FIGURE B-5A. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C

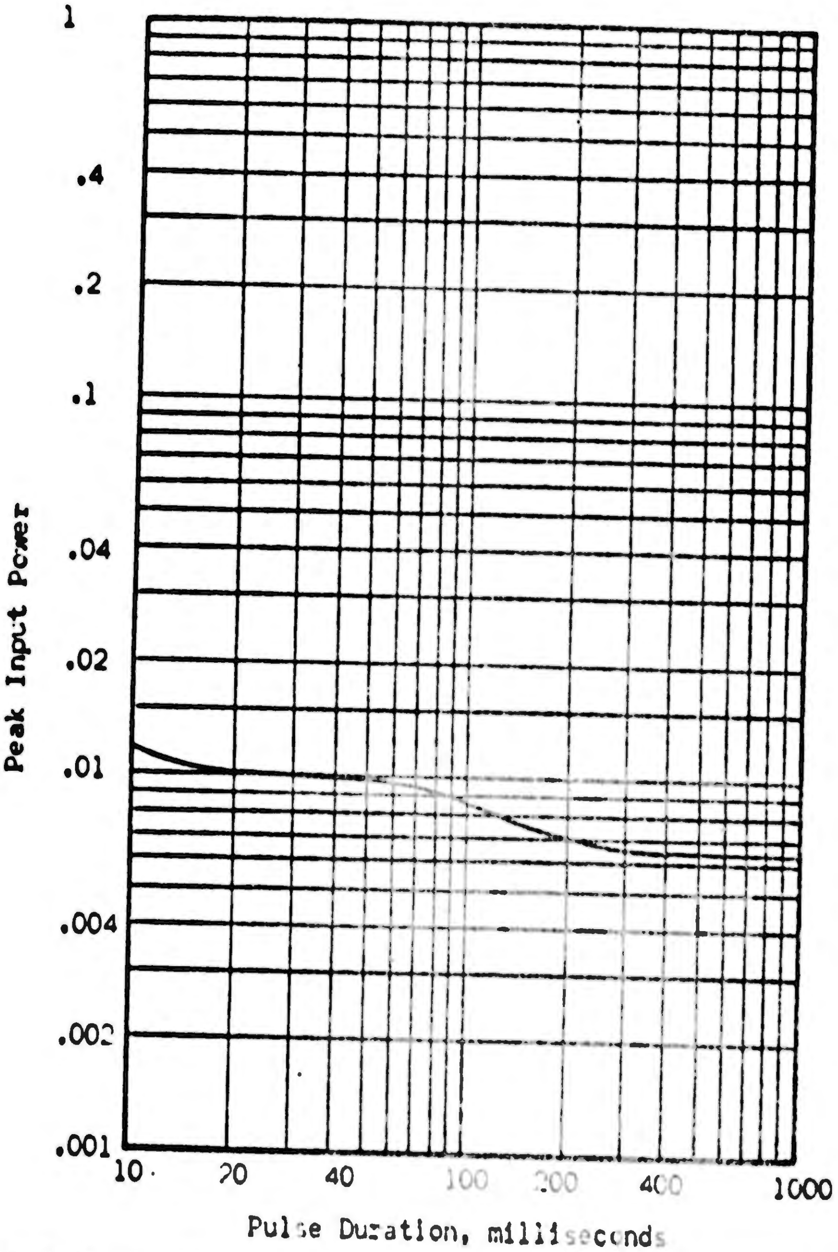


FIGURE B-5B. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C

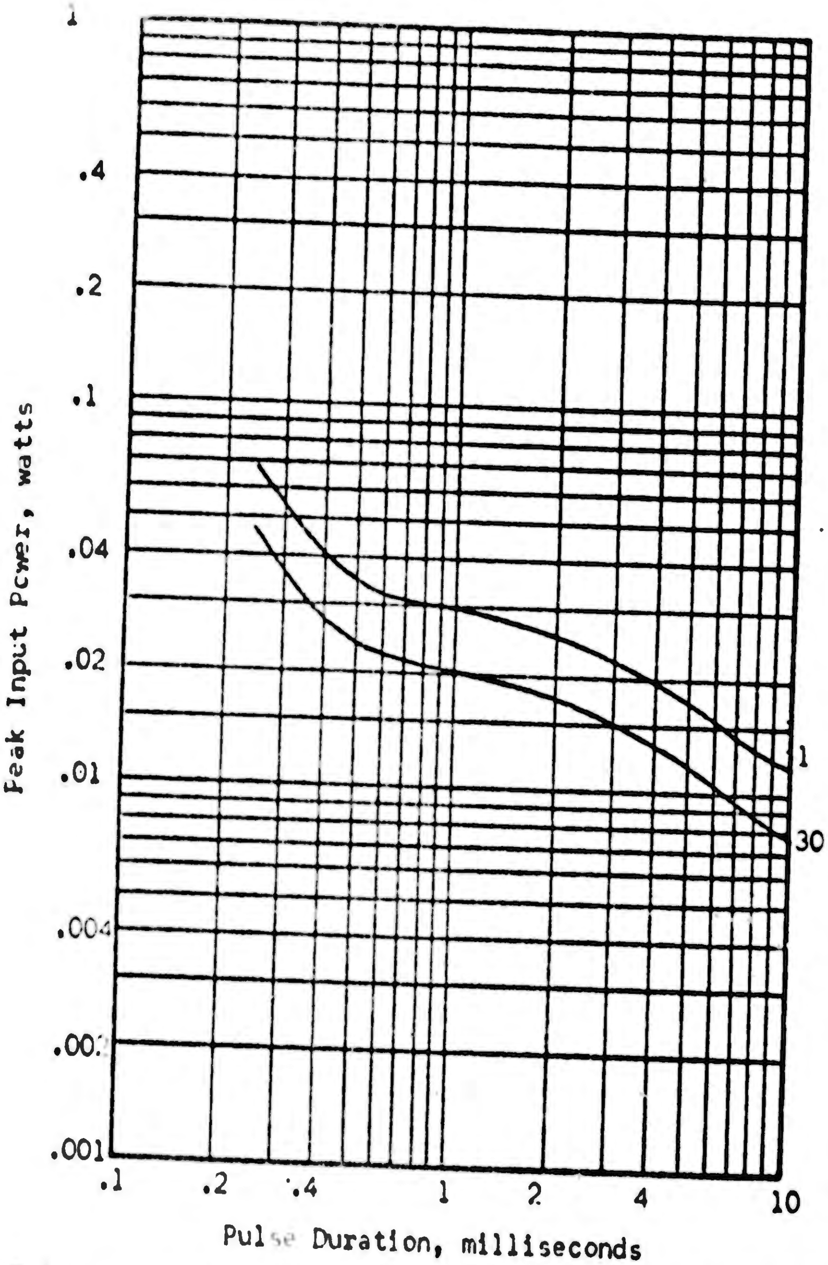


FIGURE B-6A. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 30
Thermal runaway with zero input for S = 50

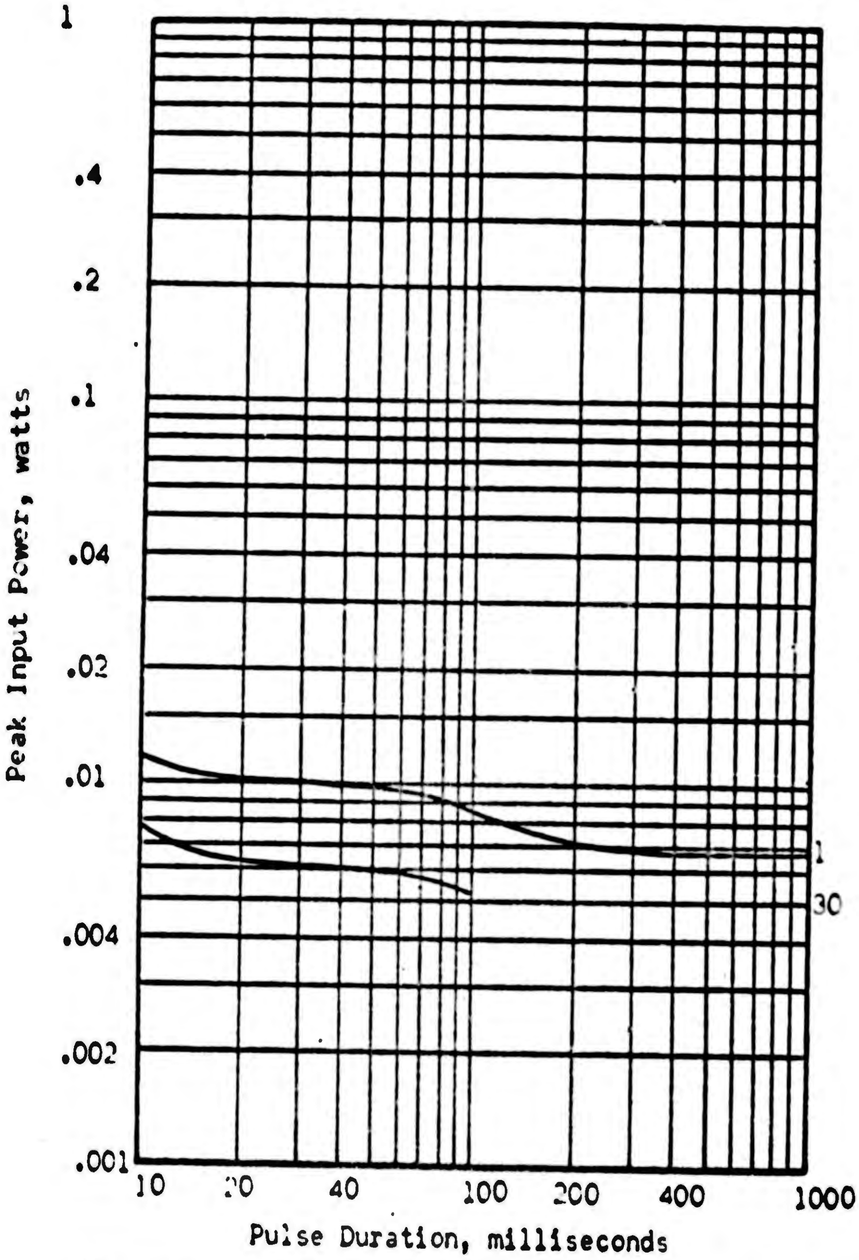


FIGURE B-6B. 2N167 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 30
Thermal runaway with zero input for S = 50

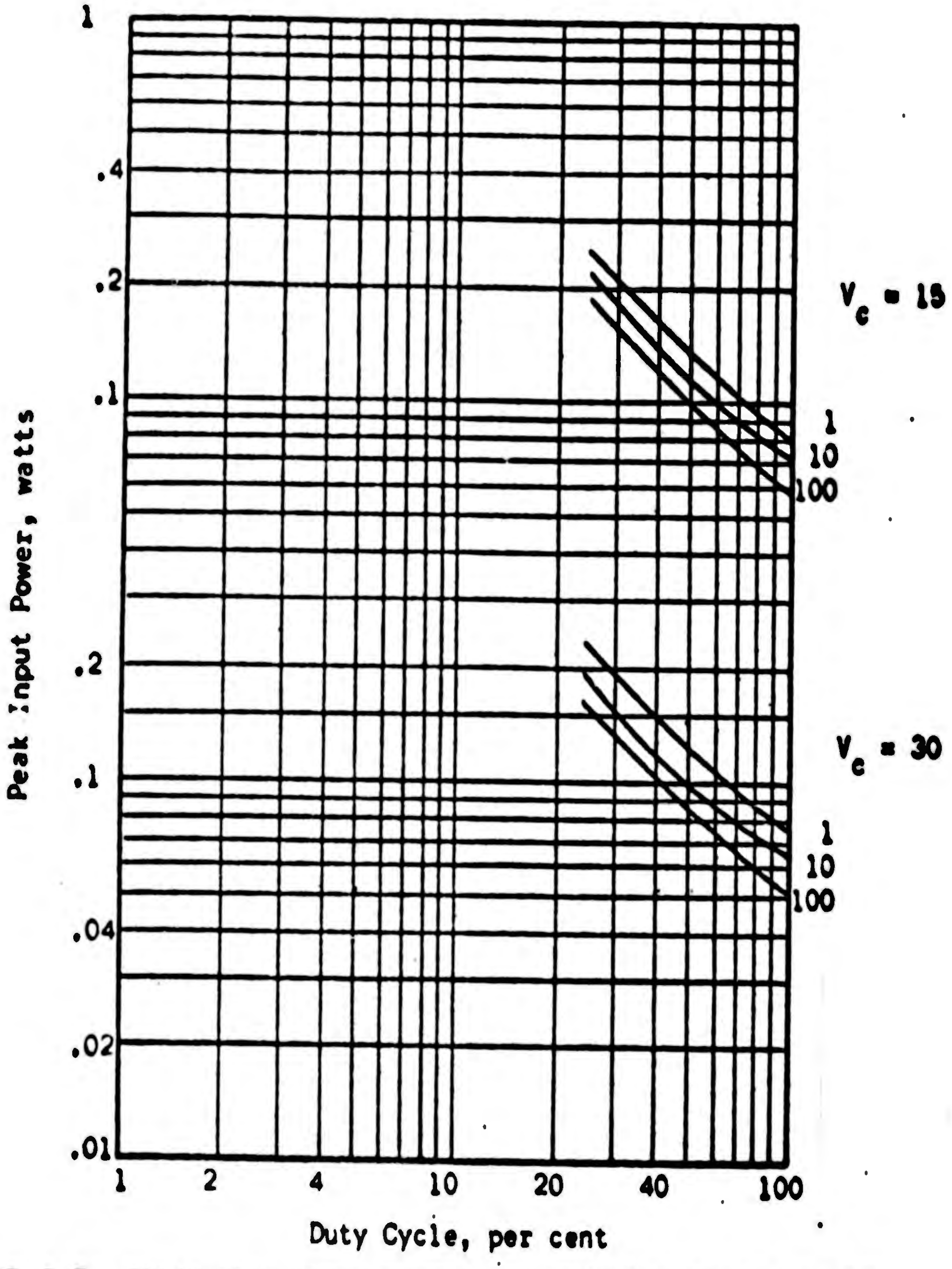


FIGURE B-7. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1 millisecond
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 10, and 100

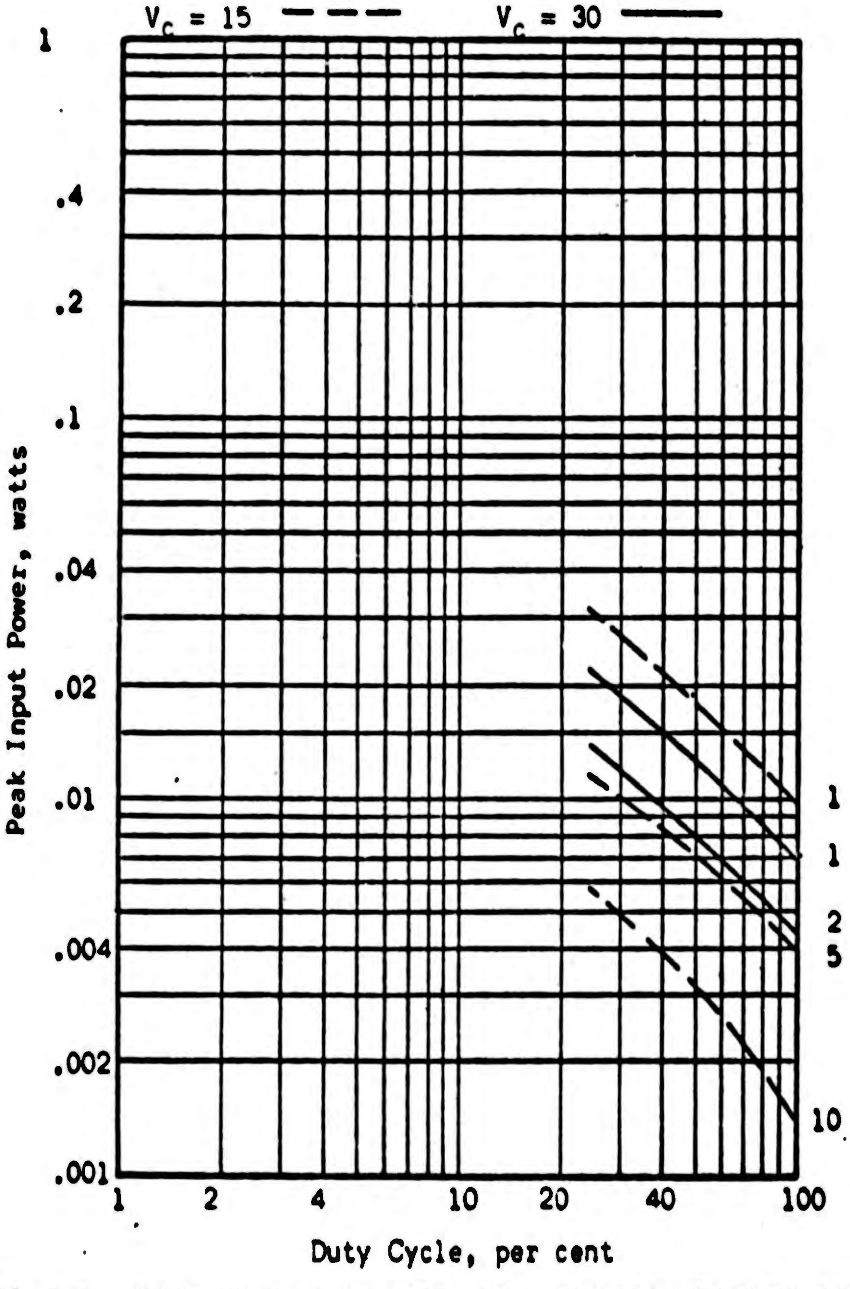


FIGURE B-8. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1 millisecond
Collector voltage = 15 and 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 2, 5, and 10
Zero input peak junction temperature = 85 C for
V_c = 15 and S = 14
V_c = 30 and S = 7

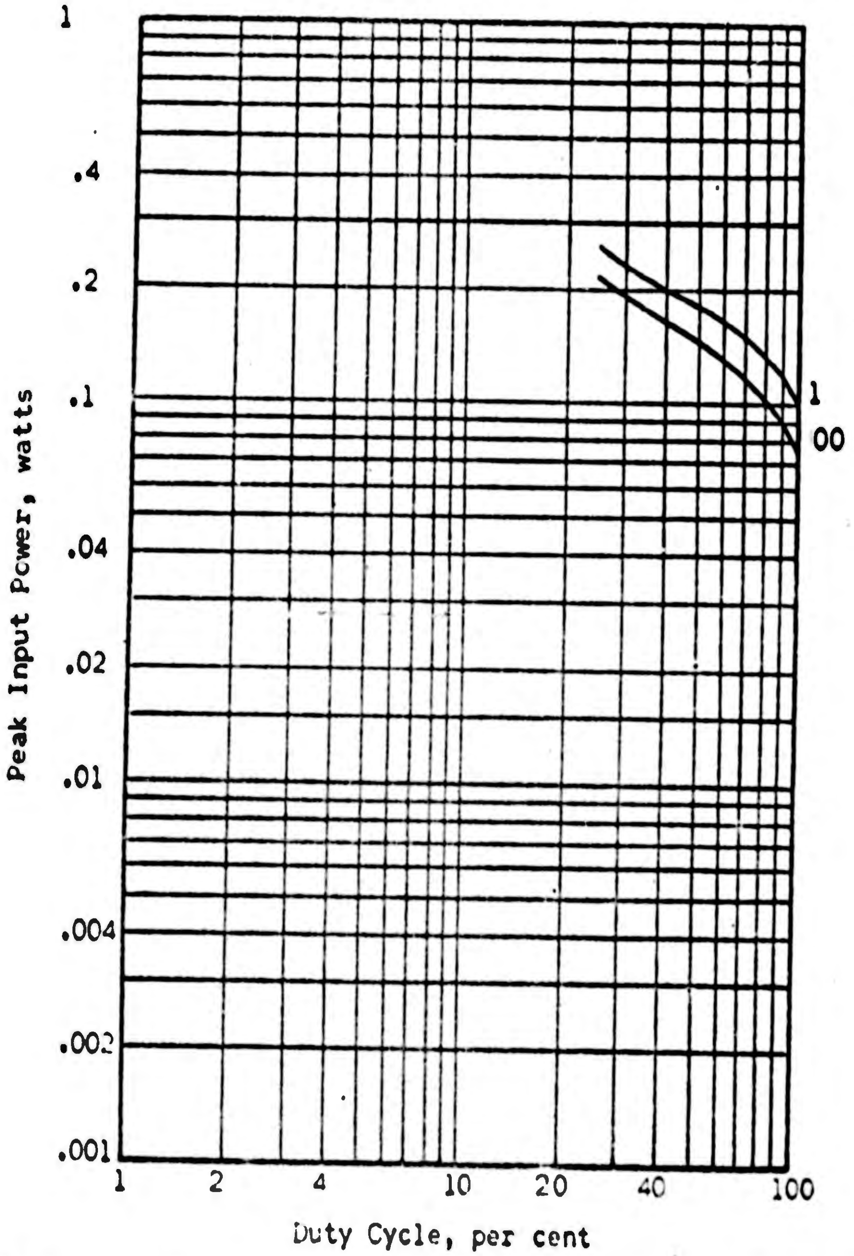


FIGURE B-9. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1 millisecond
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

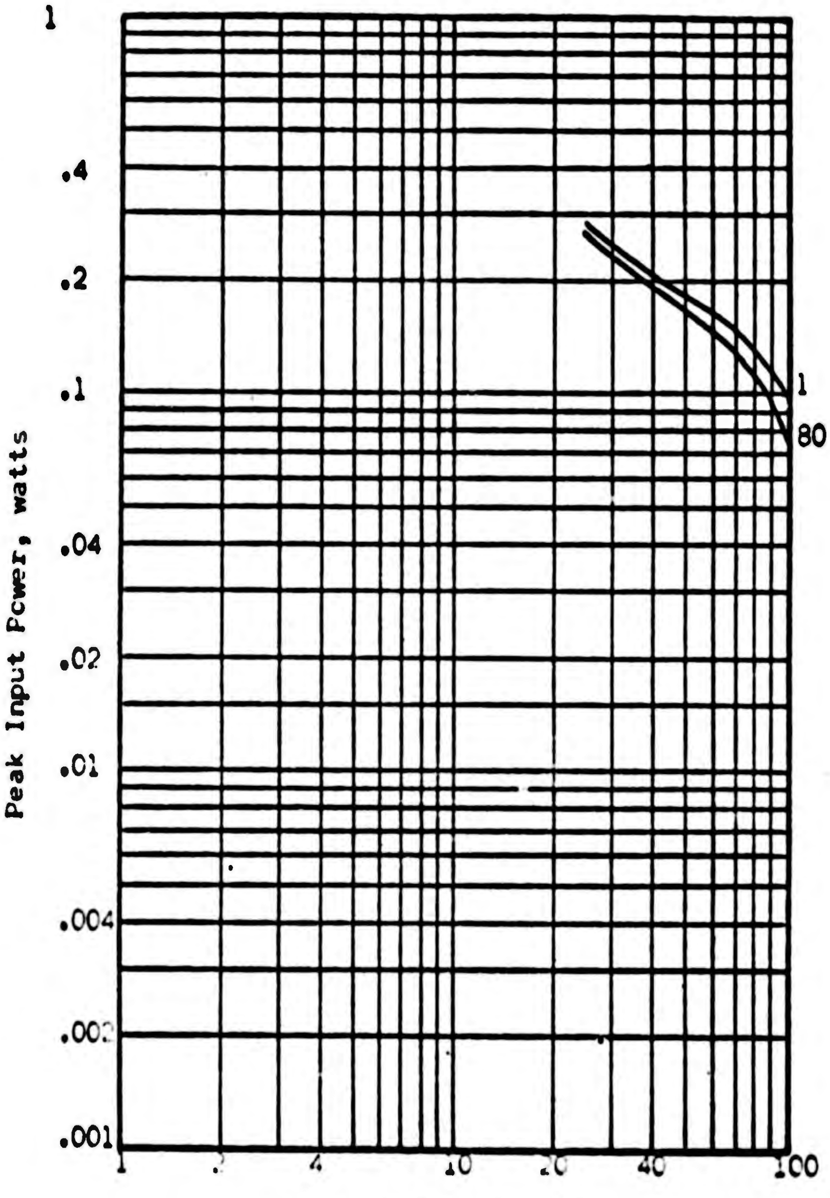


FIGURE B-10. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1 millisecond
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal runaway with zero input for S = 88

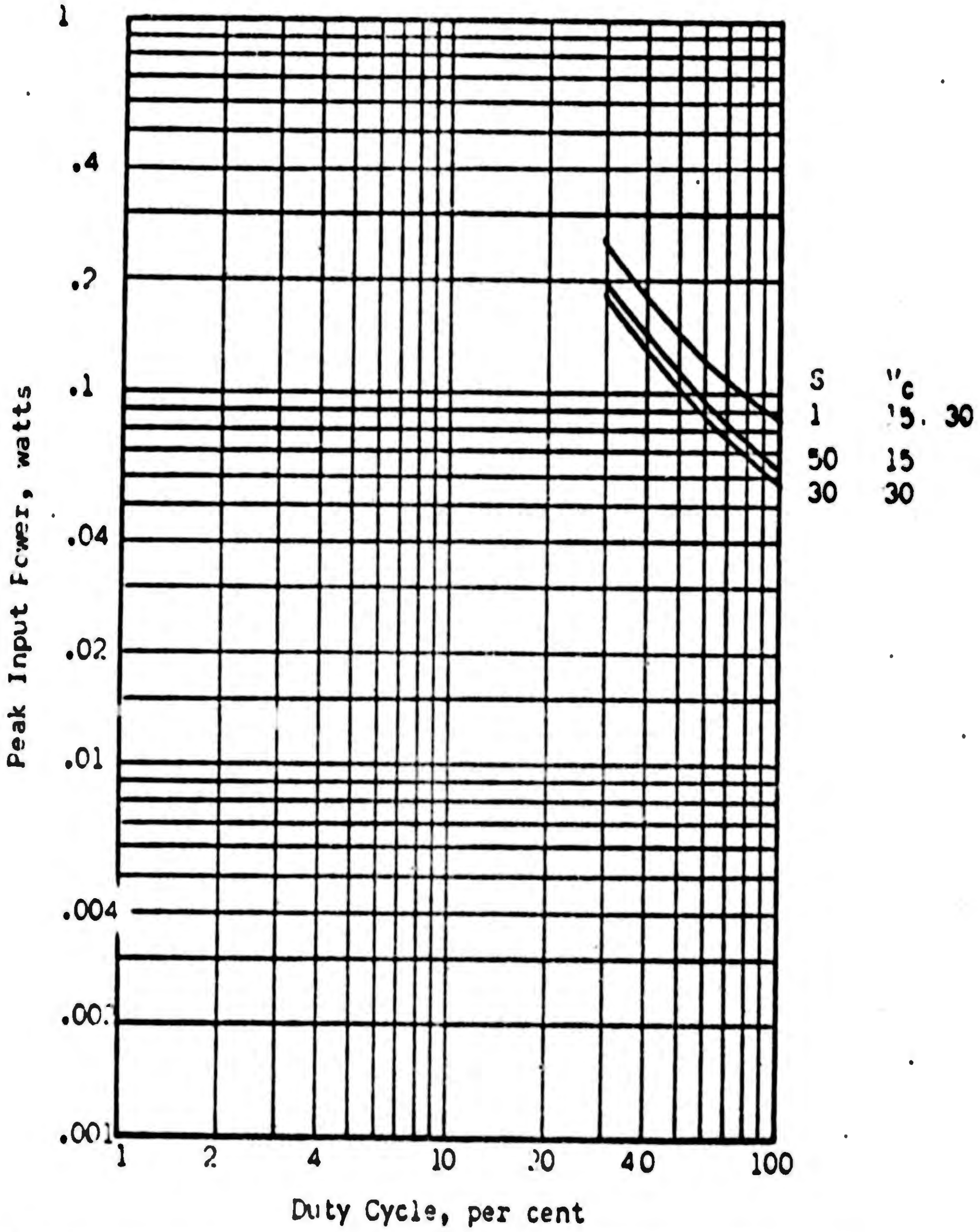


FIGURE B-11. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1 millisecond
Collector voltage = 15, 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 30, and 50

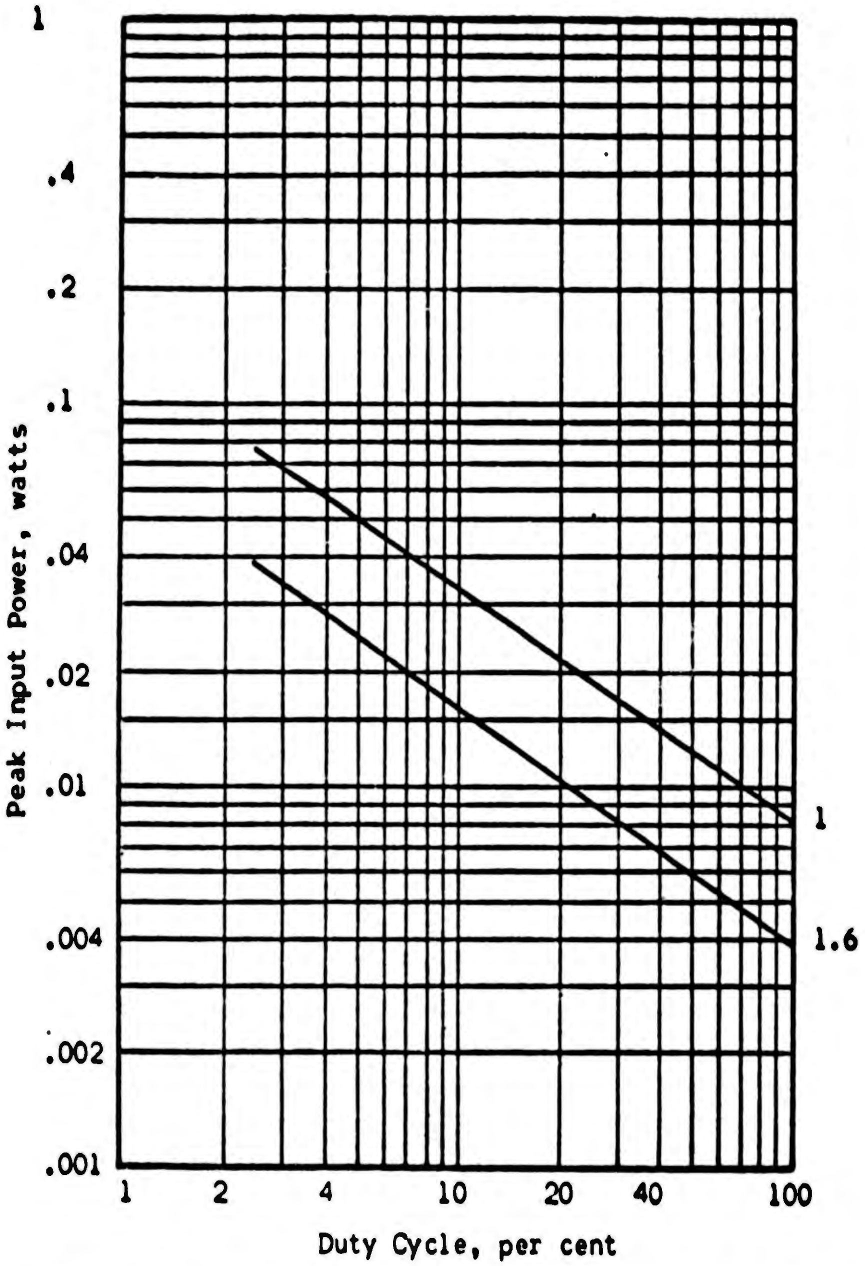


FIGURE B-12. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = 3 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 1.6
Zero input peak junction temperature = 85 C for S = 2.2

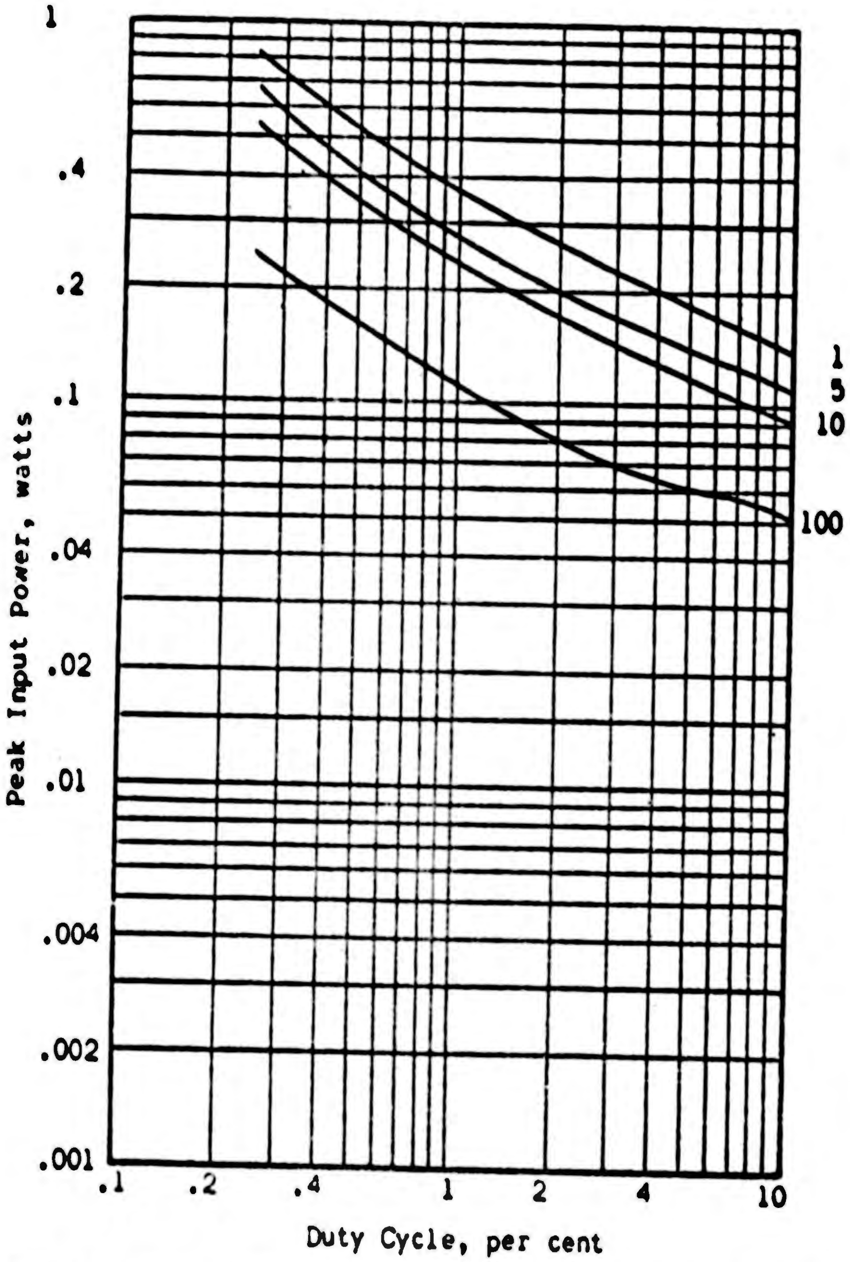


FIGURE B-15A. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

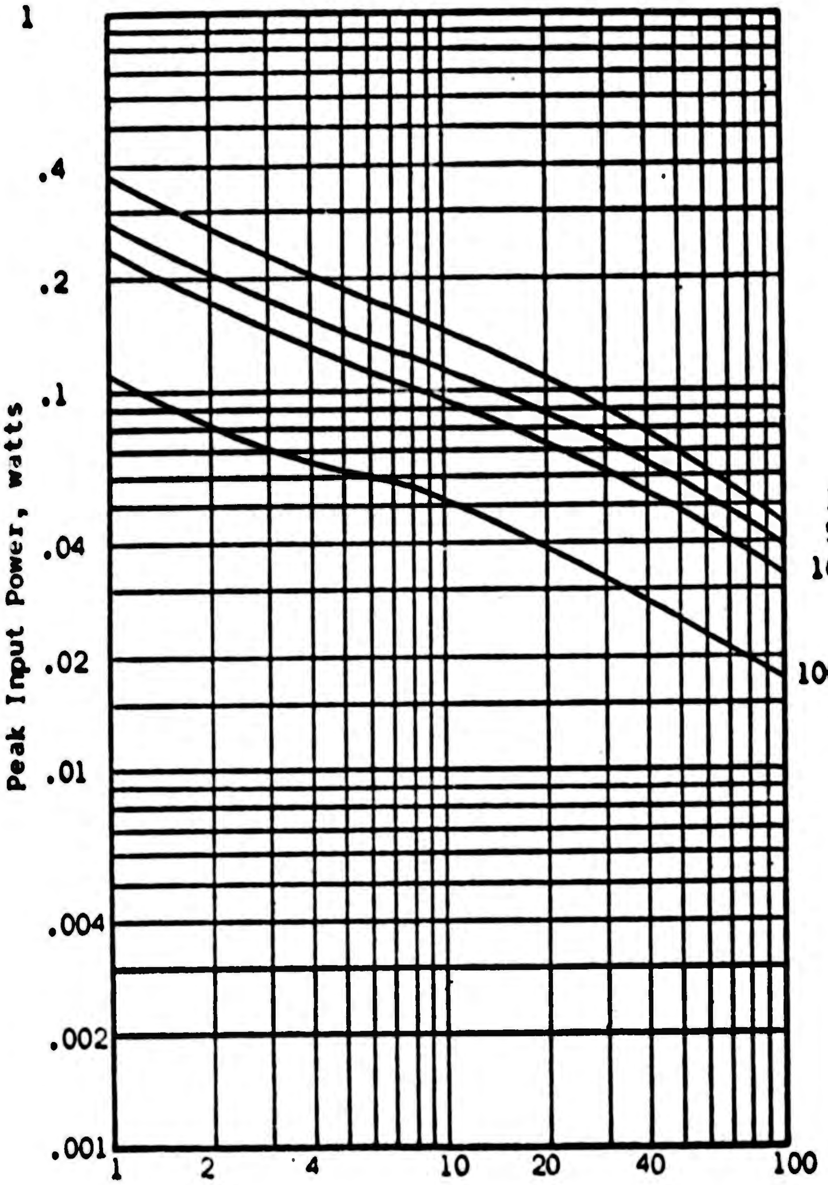


FIGURE B-13B. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

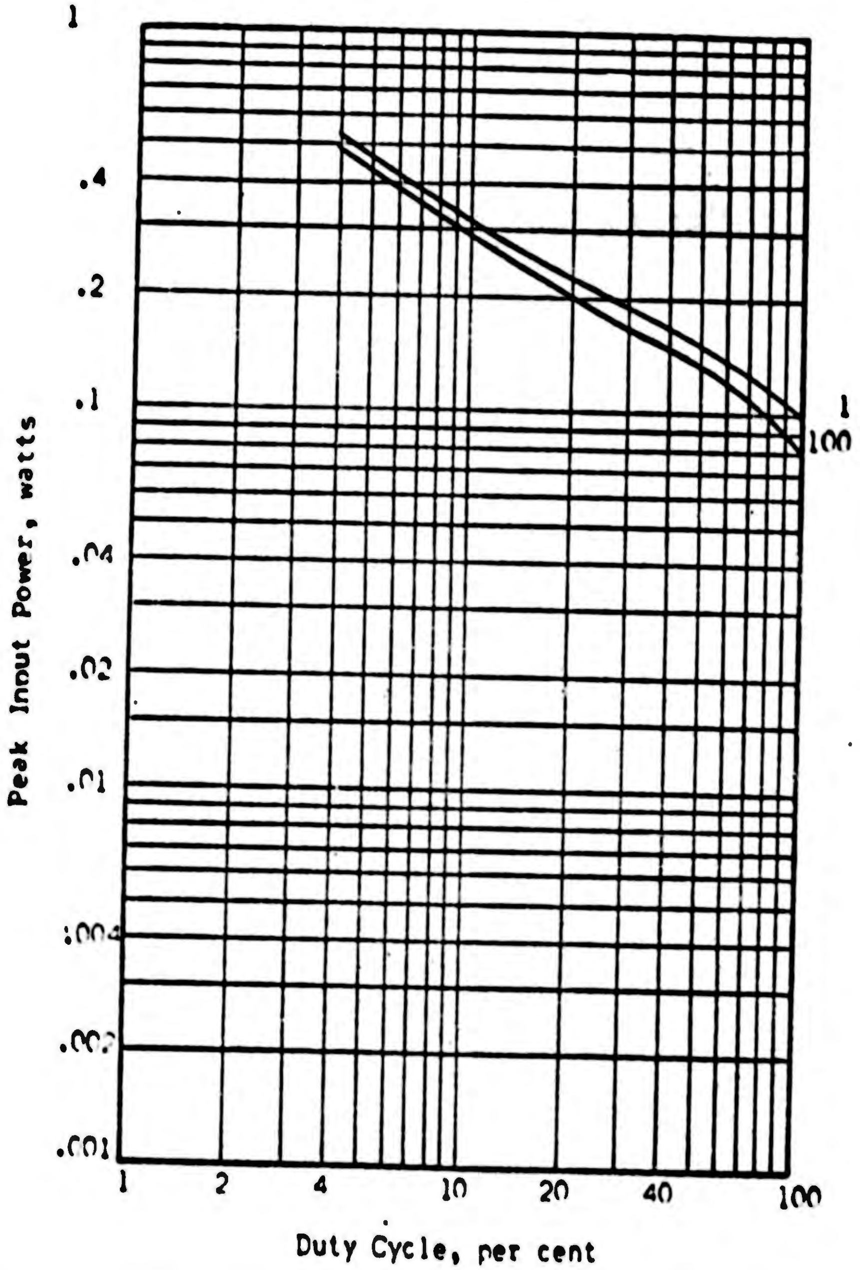


FIGURE B-14. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

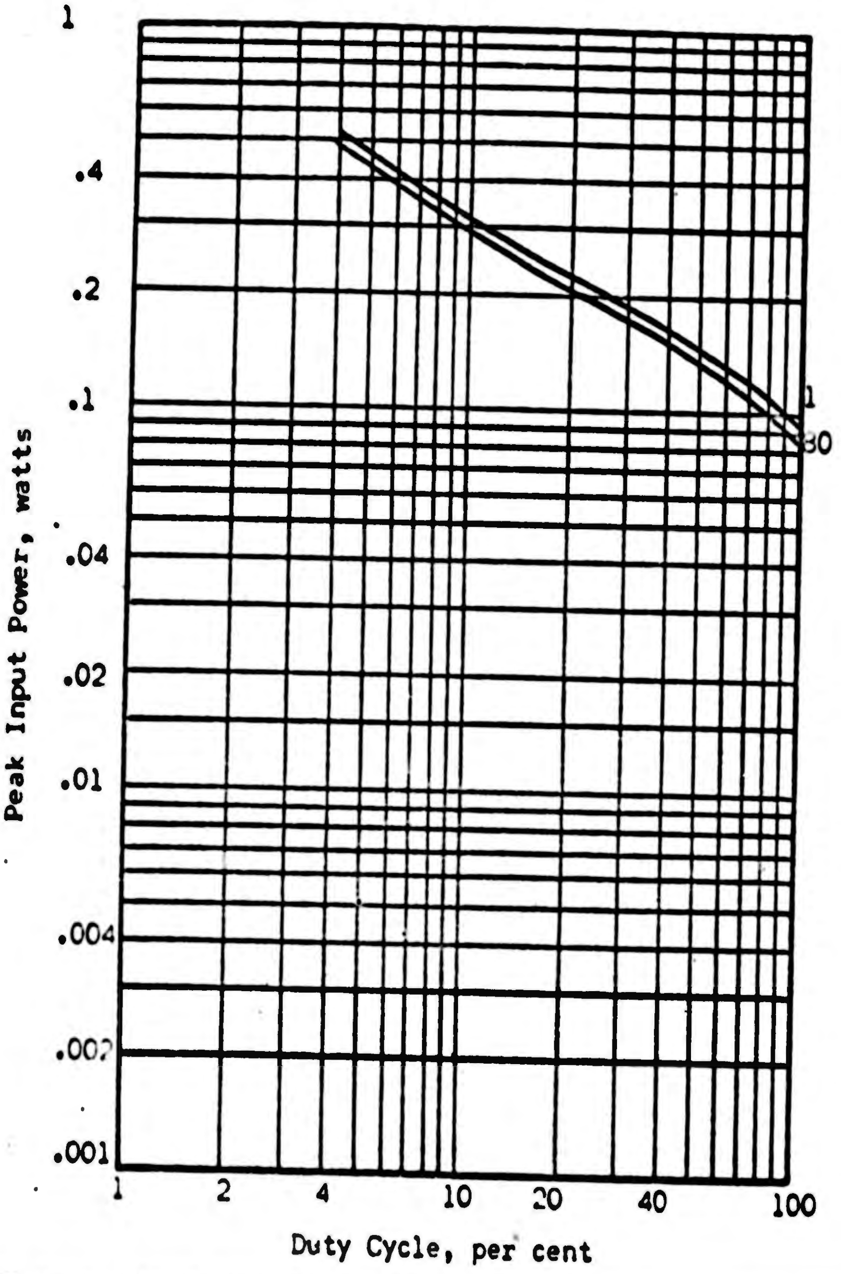


FIGURE B-15. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal Runaway with zero input for S = 88

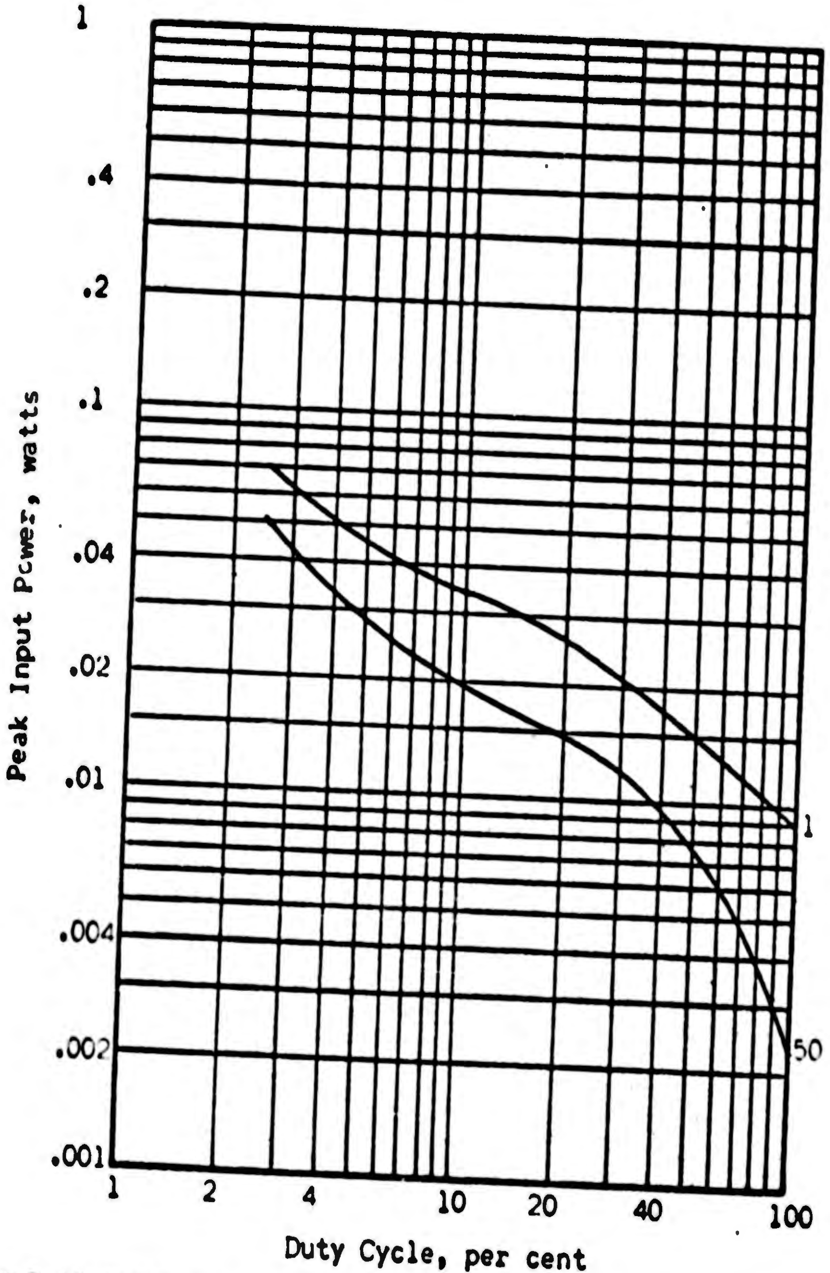


FIGURE B-16. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 50
Thermal runaway with zero input for S = 100

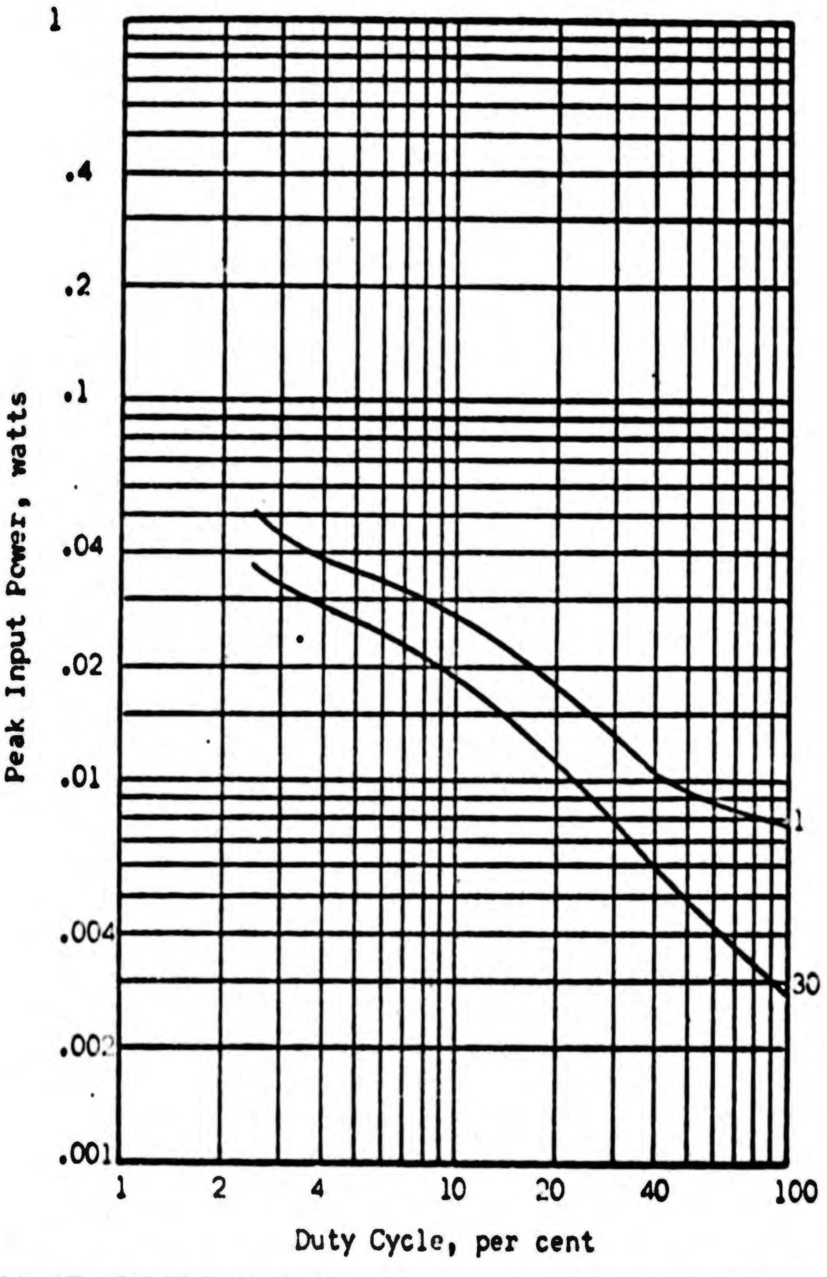


FIGURE B-17. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 30
Thermal runaway with zero input for S = 55

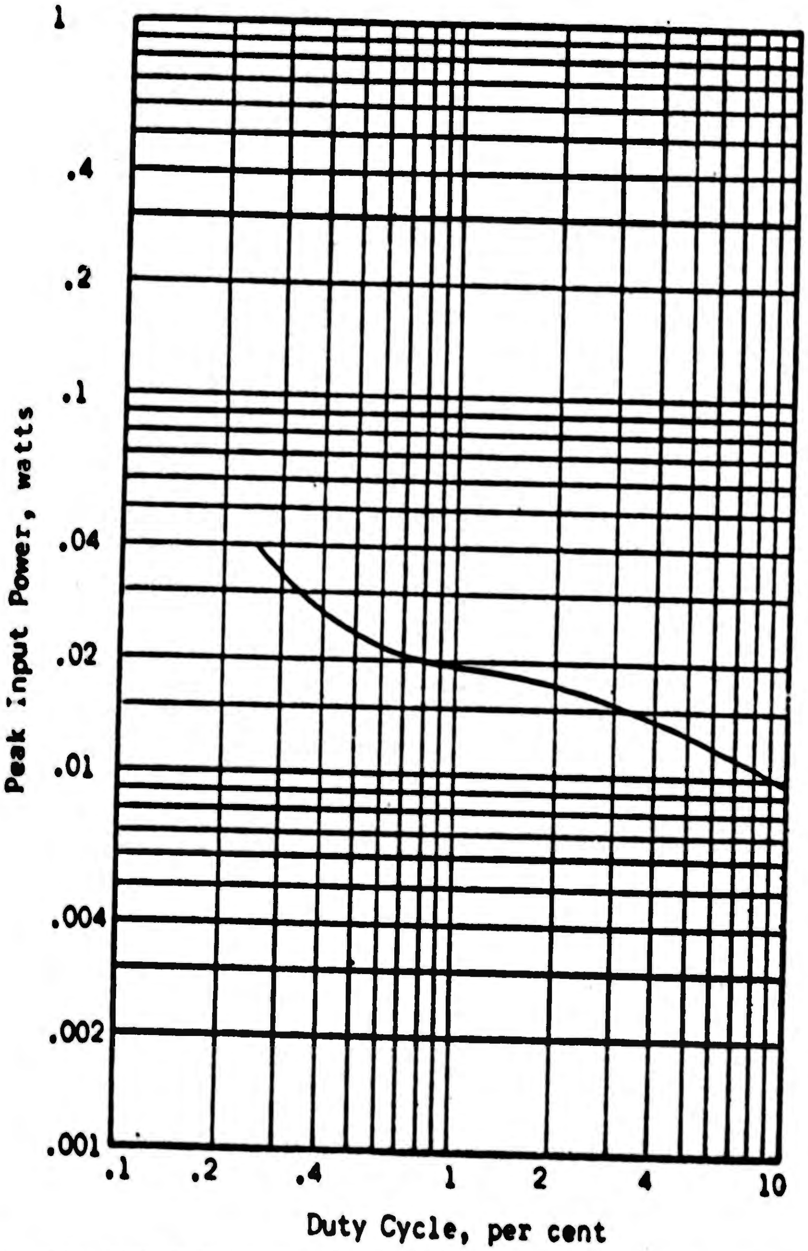


FIGURE B-18A. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 2 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1
Zero input peak junction temperature = 85 C for S = 1.4

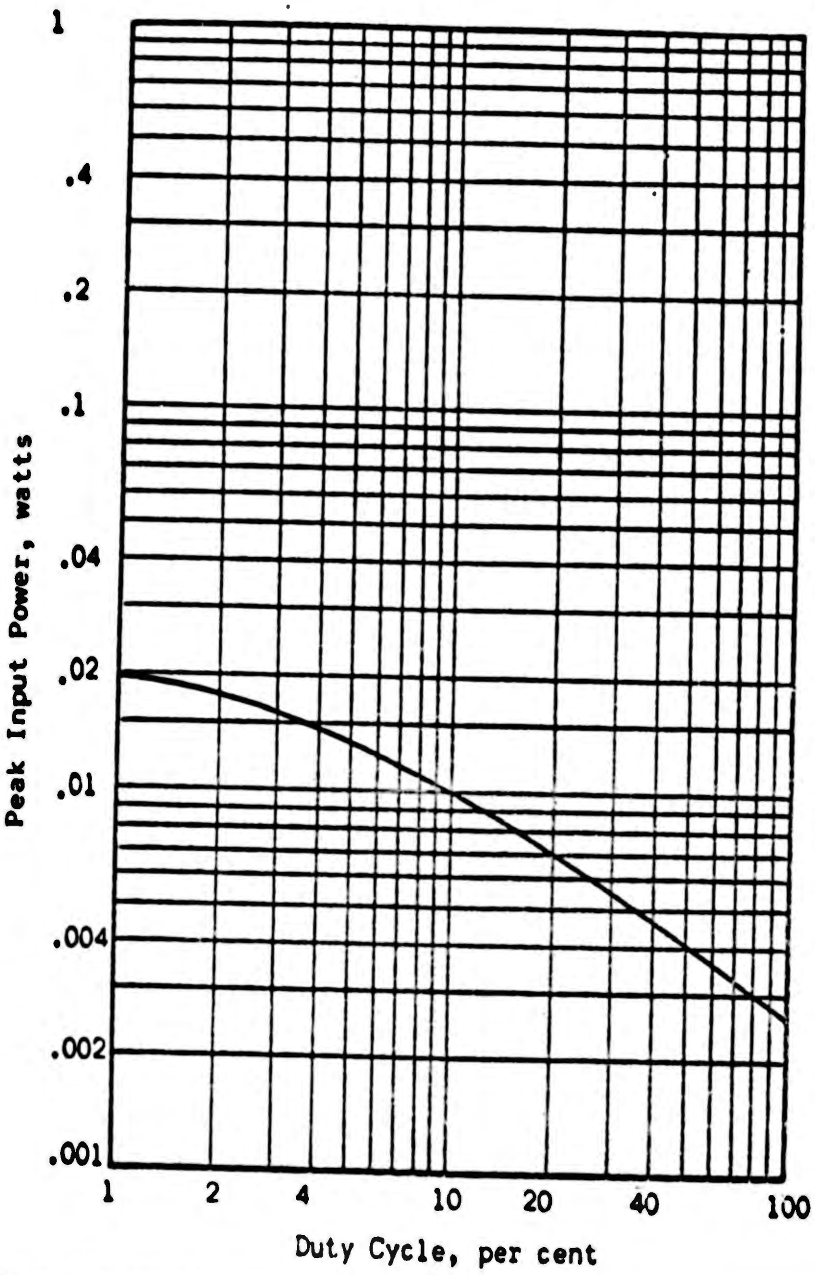
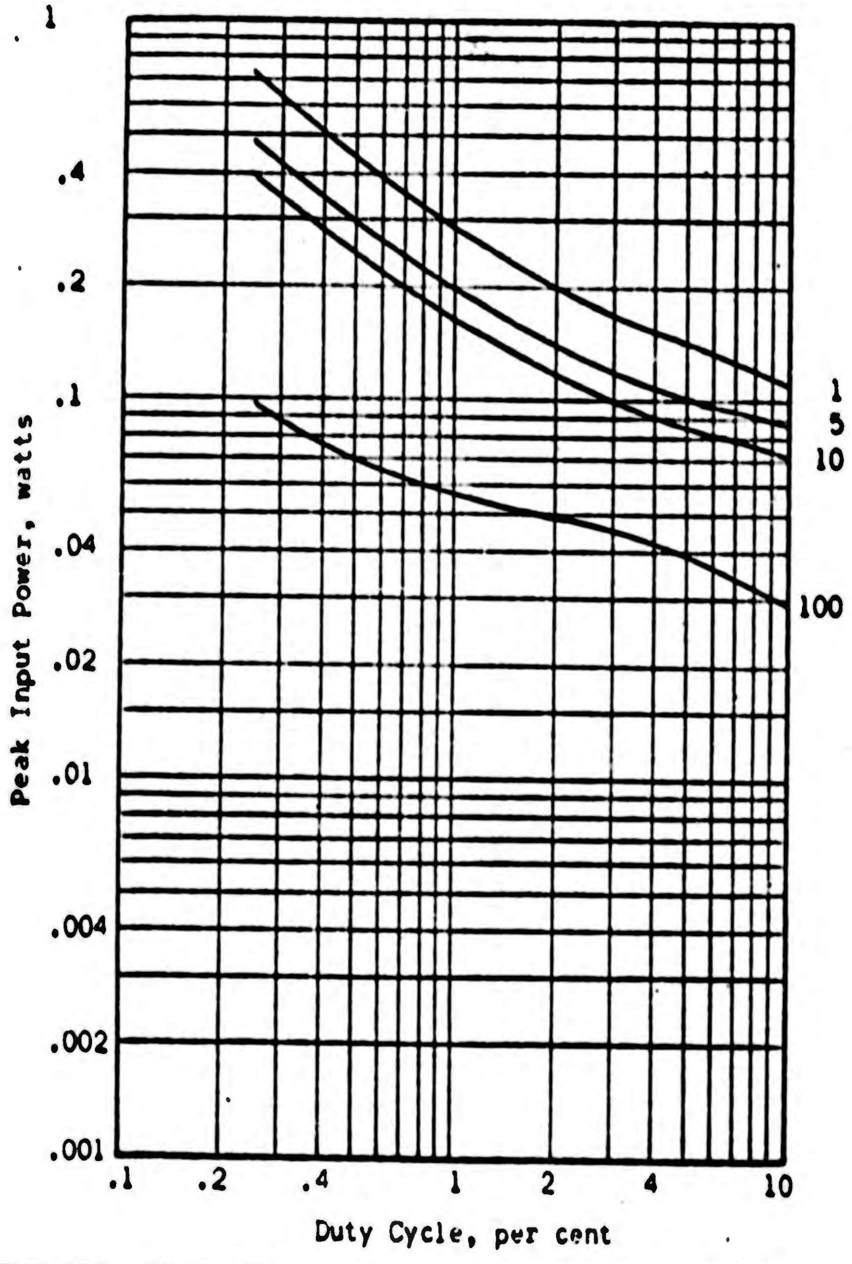


FIGURE B-16B.2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 2 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1
Zero input peak junction temperature = 85 C for S = 1.4



FIGUREB-19A. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

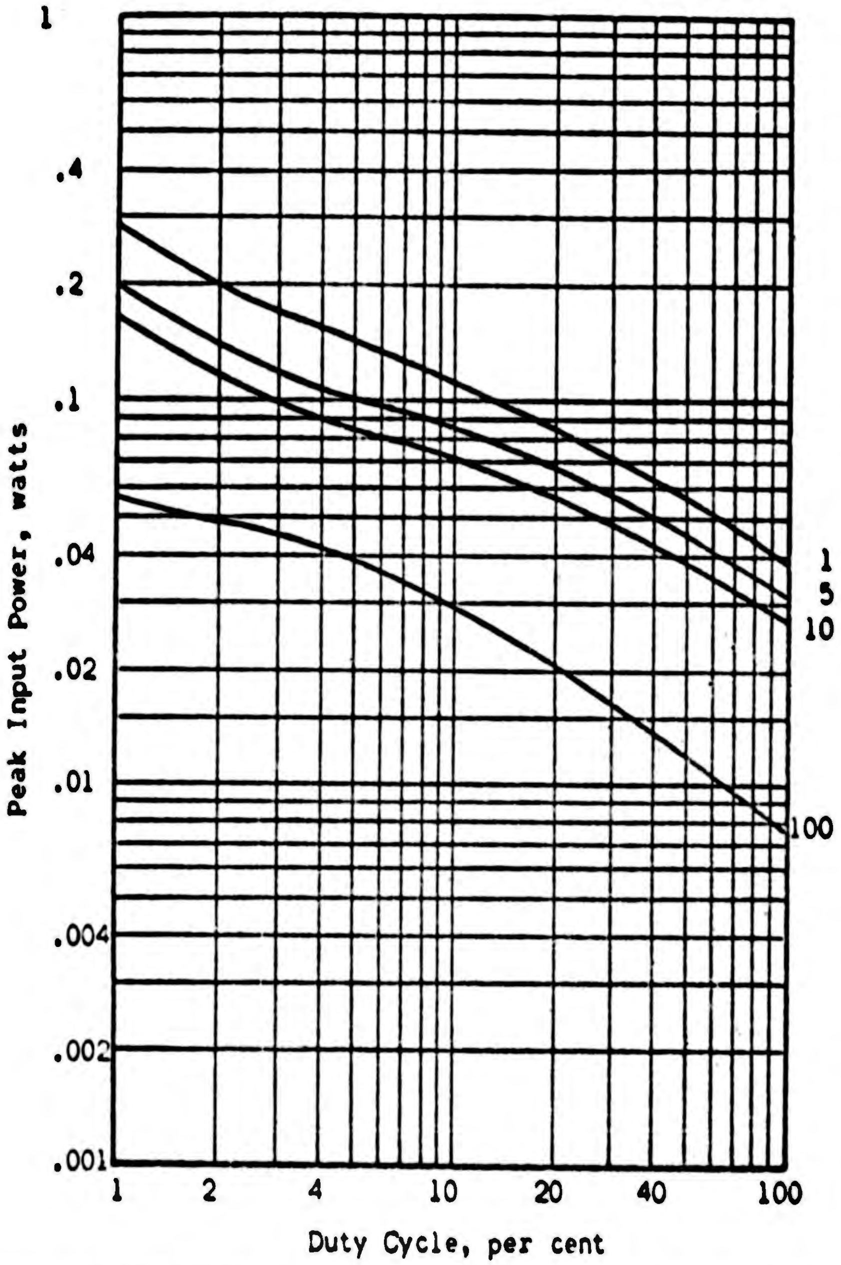


FIGURE B-19B. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak Junction temperature = 85 C
Stability factor = 1, 5, 10, and 100

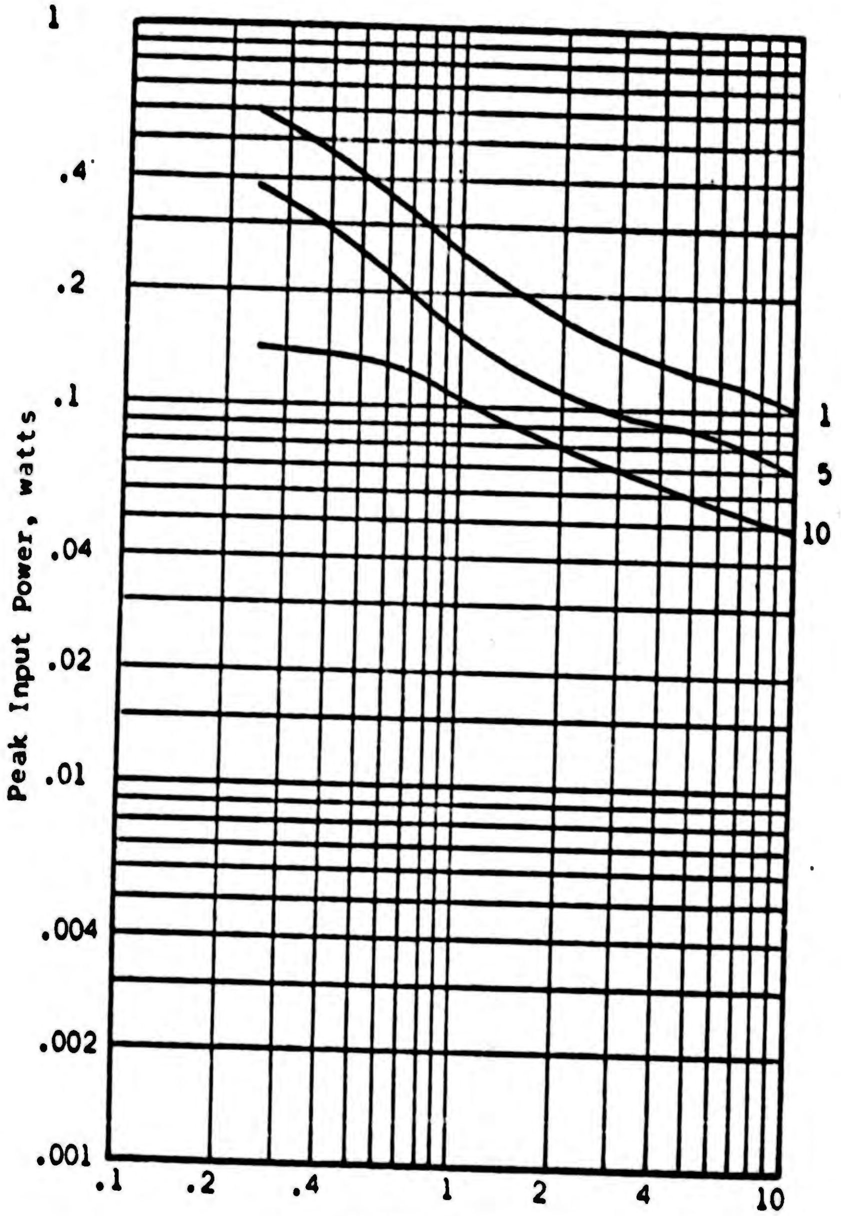


FIGURE B-20A. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1, 5, and 10
Zero input peak junction temperature = 85 C for S = 70

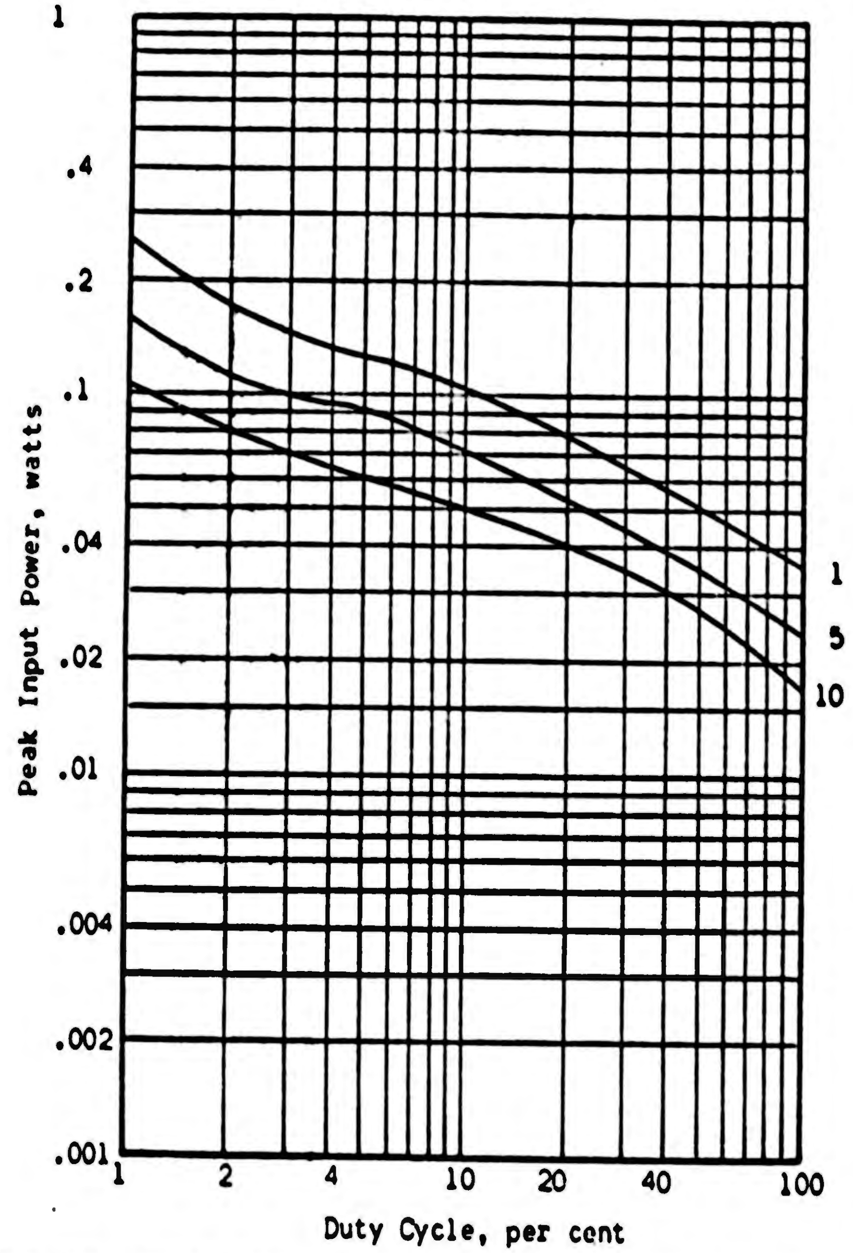


FIGURE B-20B. 2N167 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak Junction temperature = 85 C
Stability factor = 1, 5, and 100
Zero input peak junction temperature = 85 C for S = 70

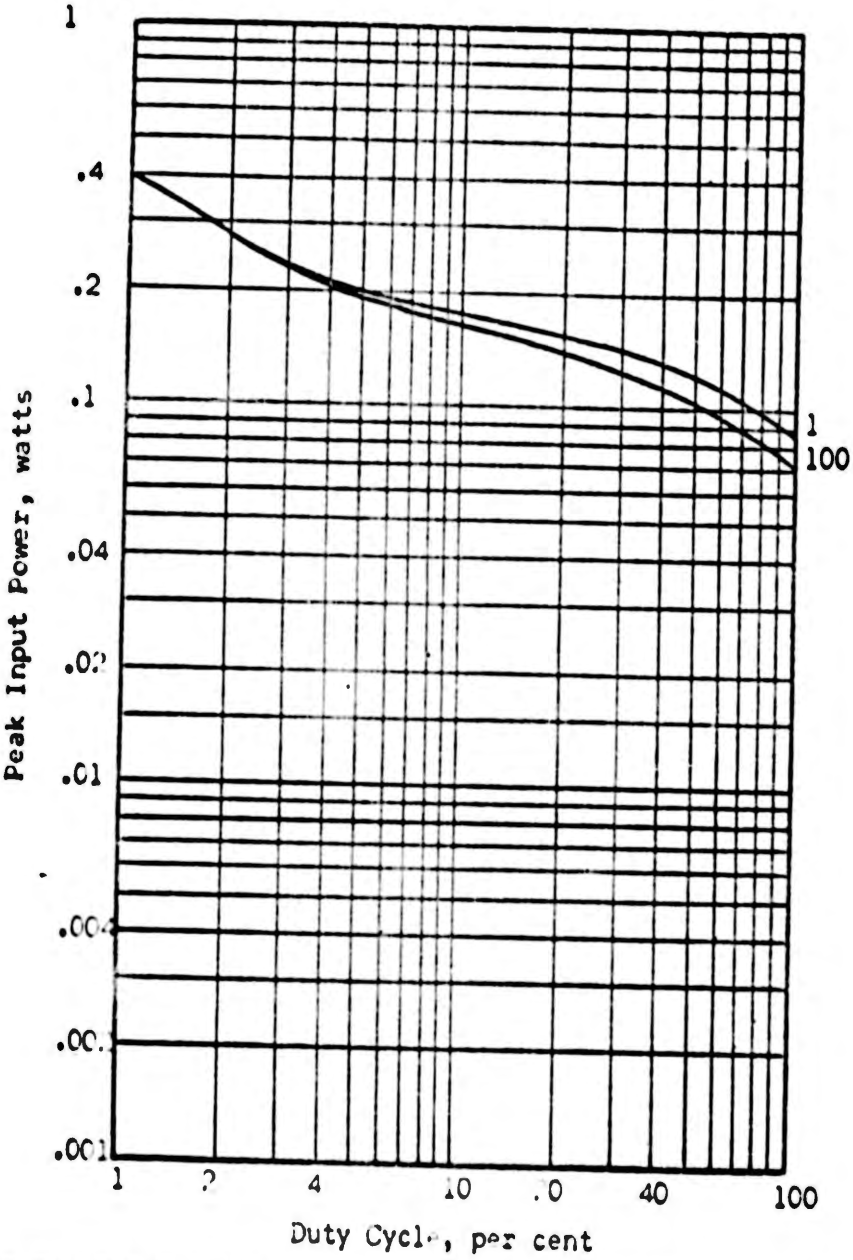


FIGURE B-21A. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

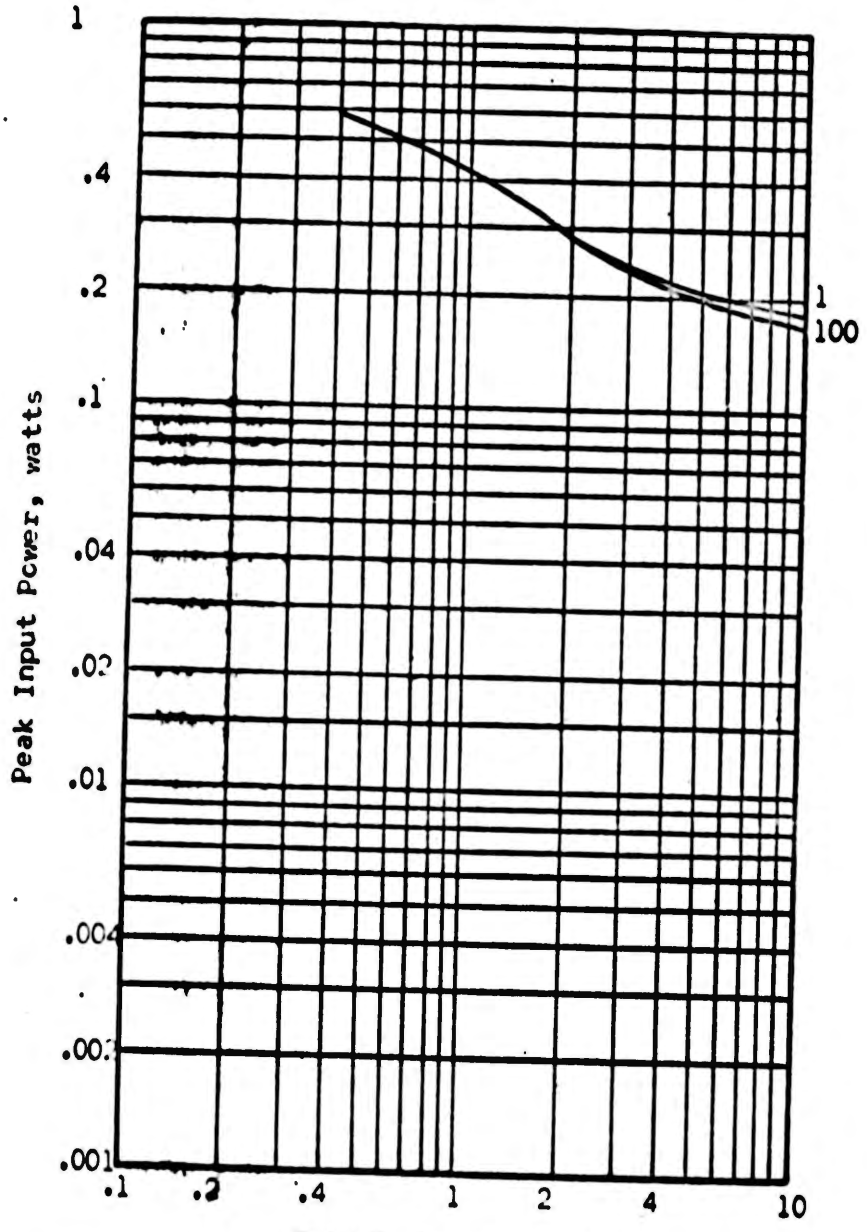


FIGURE B-21B.2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

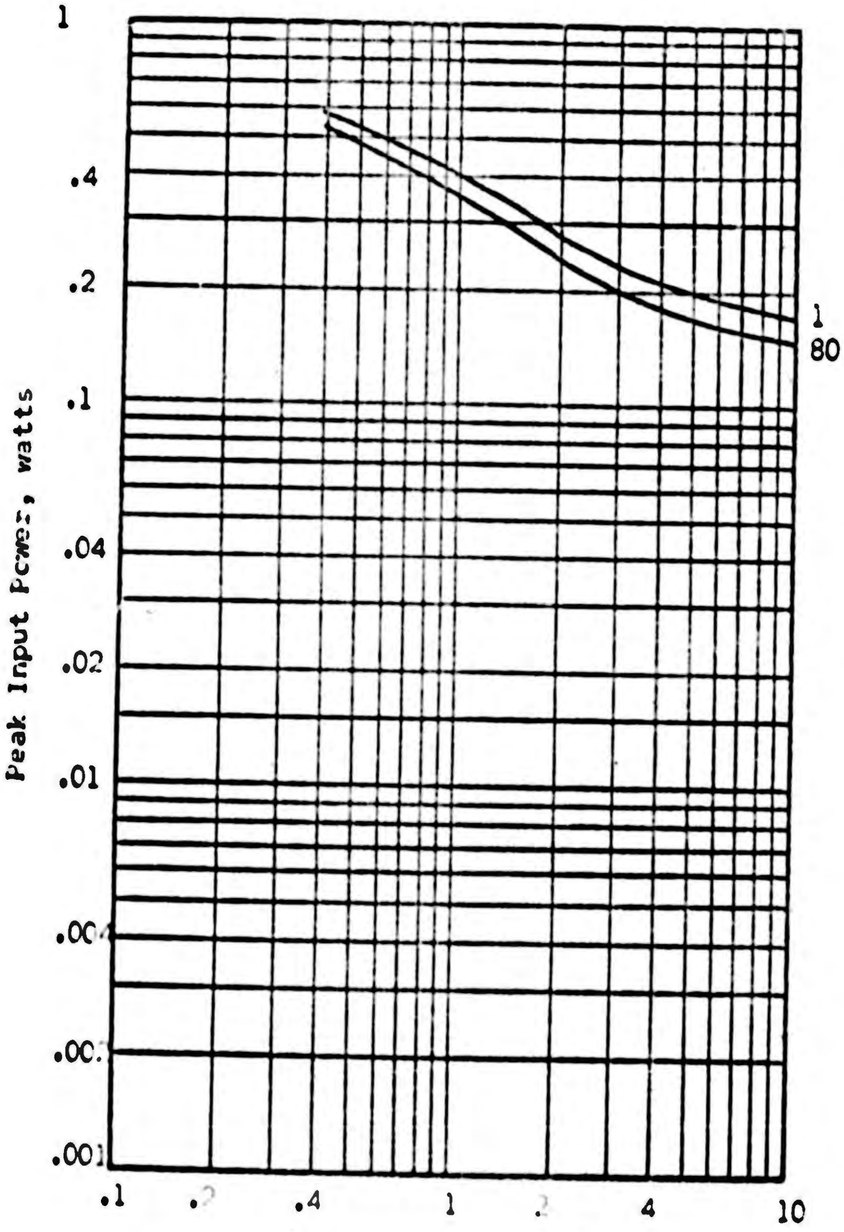


FIGURE B-22A. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal runaway with zero input for S = 91

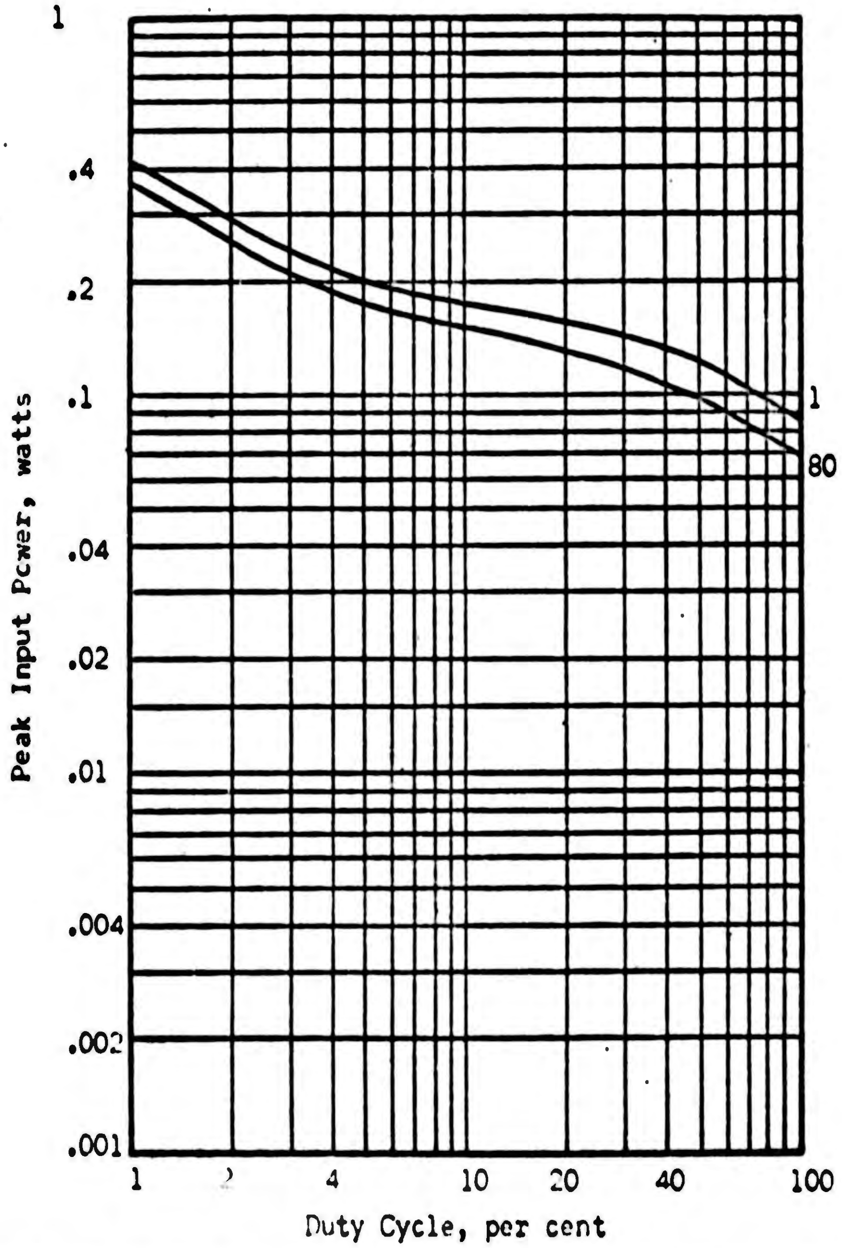


FIGURE B-22B. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 80
Thermal runaway with zero input for S = 91

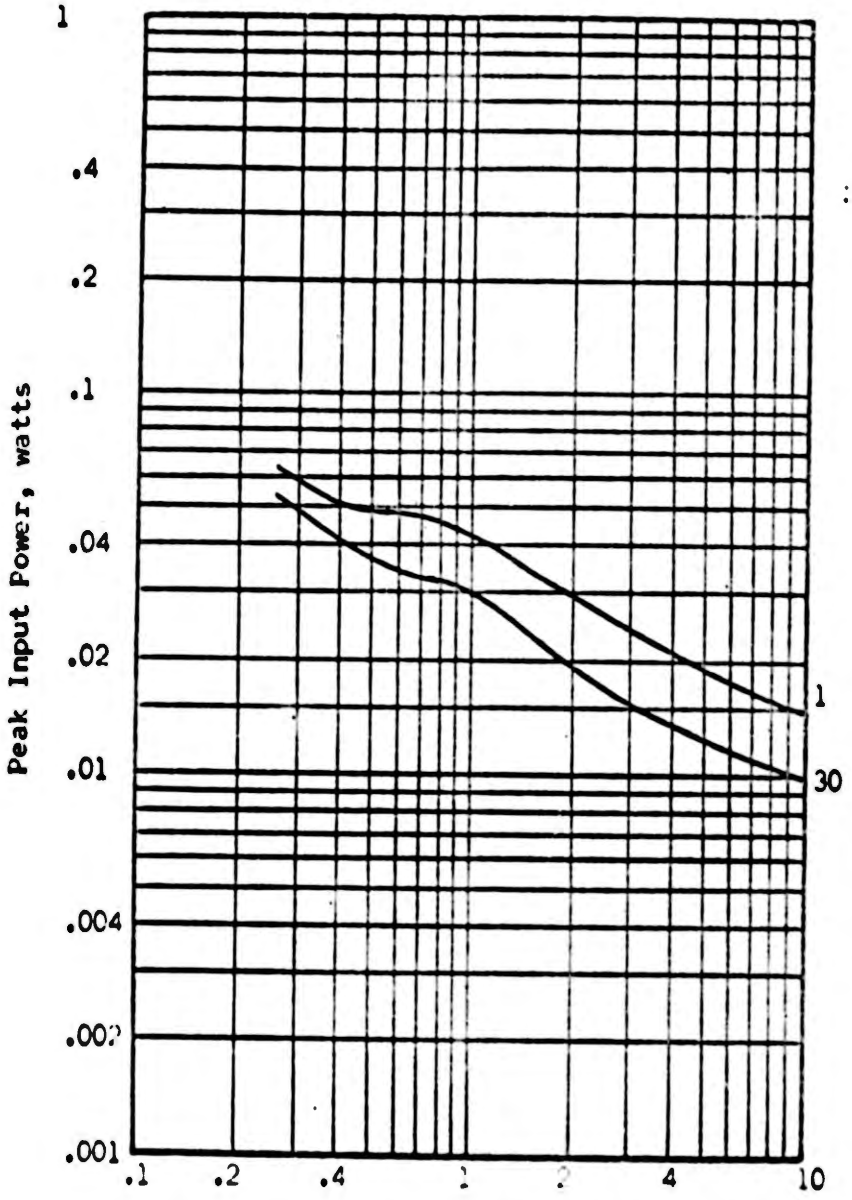


FIGURE B-23A. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition Period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 30
Thermal runaway with zero input for S = 50

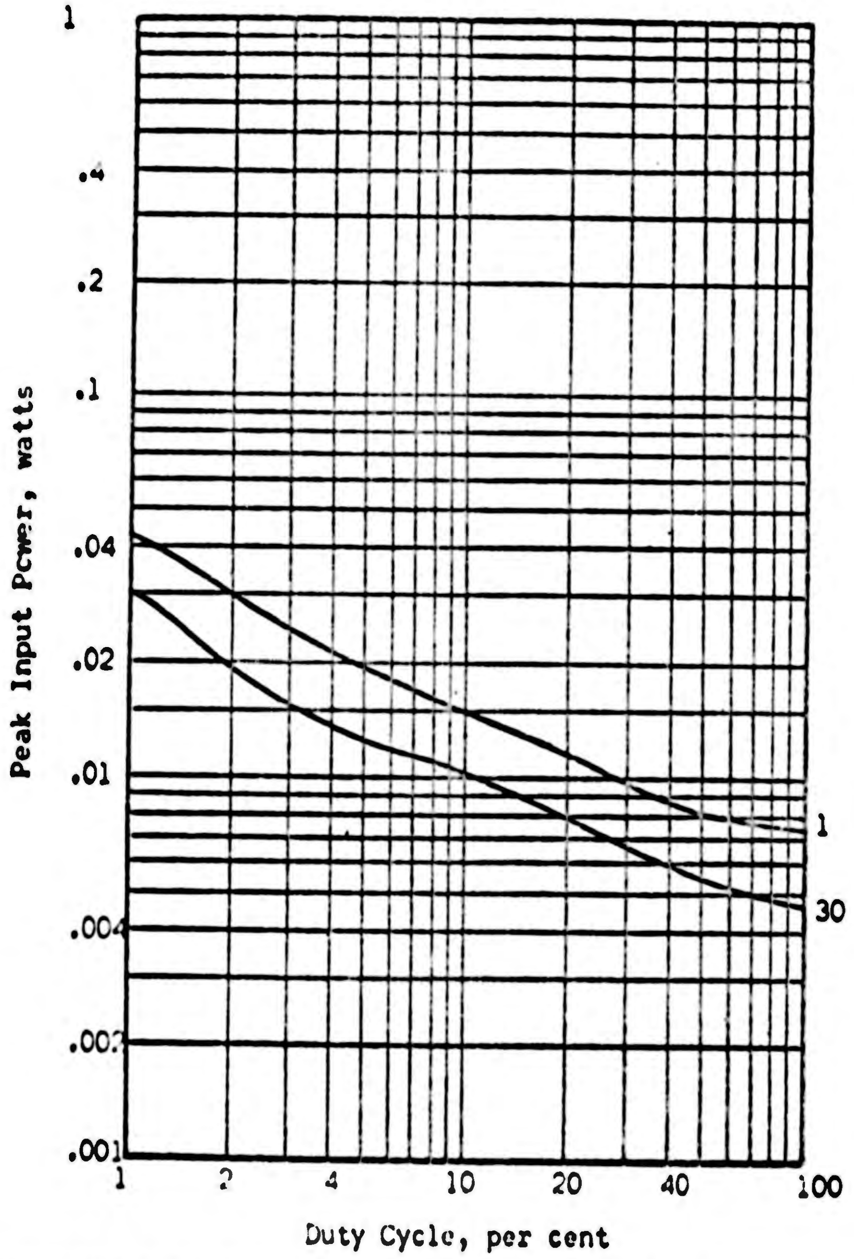


FIGURE B-23B. N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 30
Thermal runaway with zero input for S = 50

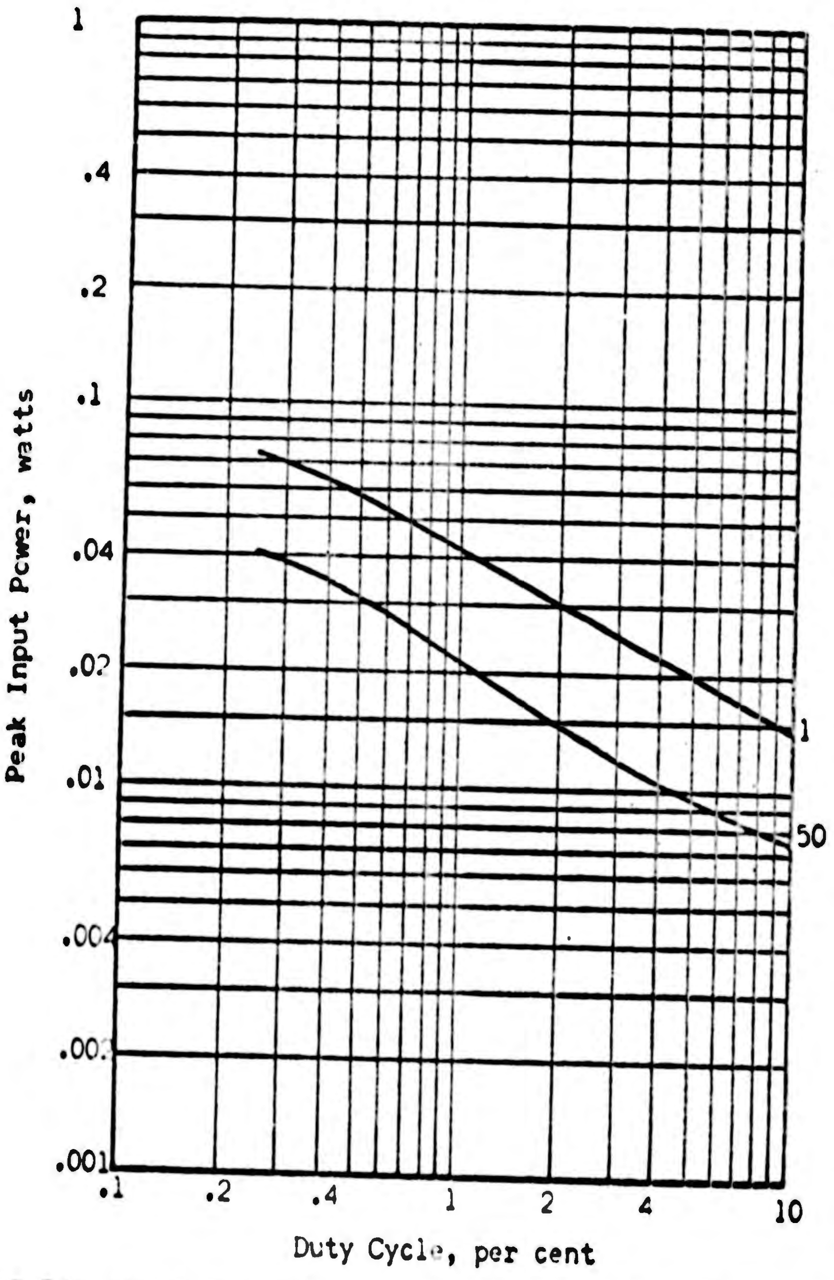


FIGURE B-24A. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 50
Thermal runaway with zero input for S = 100

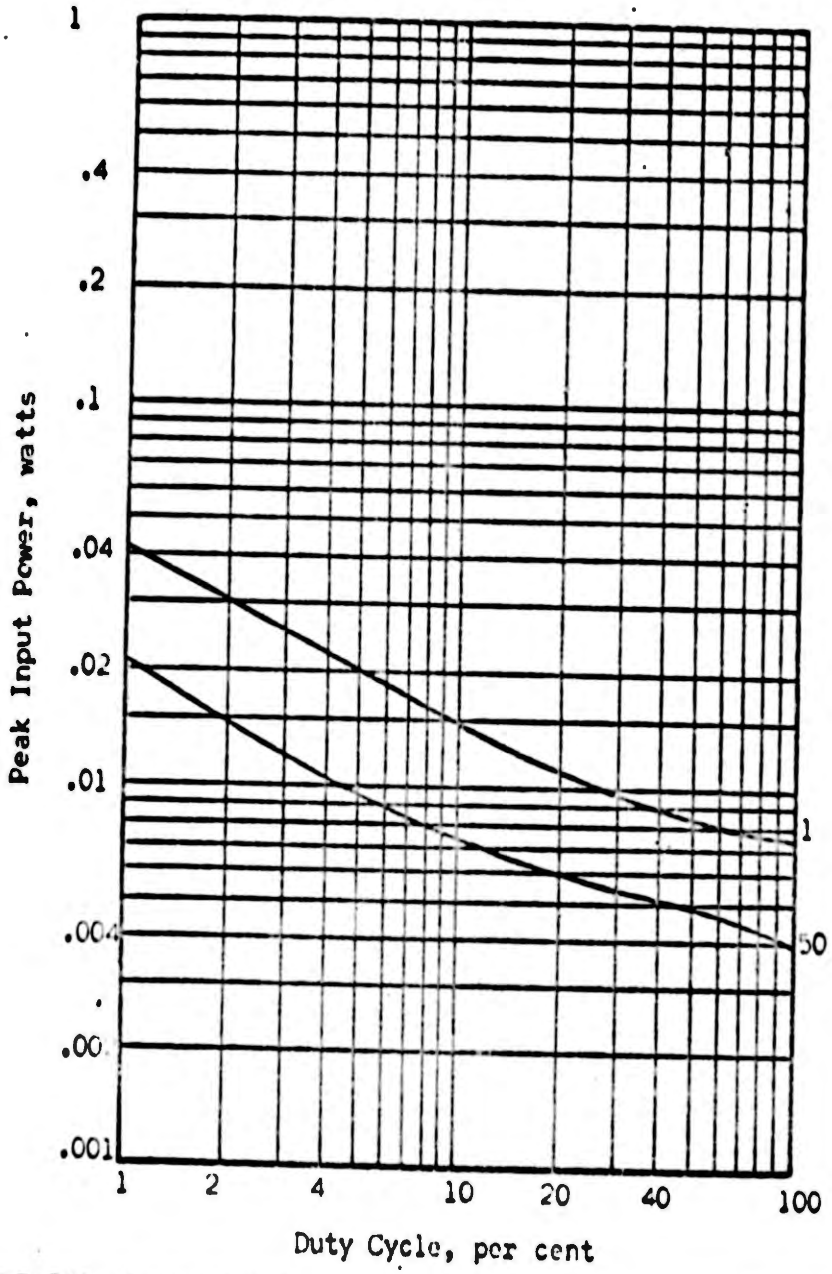


FIGURE B-24B. 2N167 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 50
Thermal runaway with zero input for S = 100

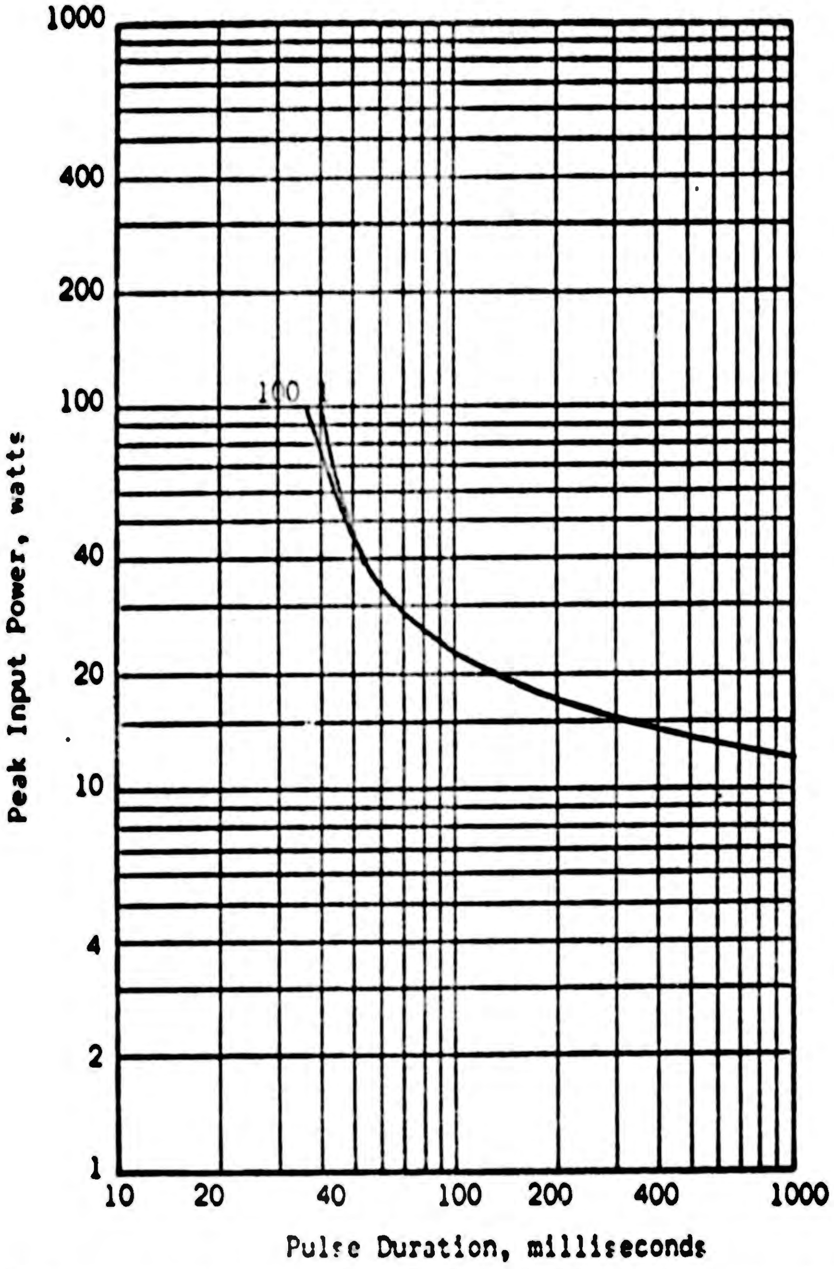


FIGURE B-25. 2N326 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

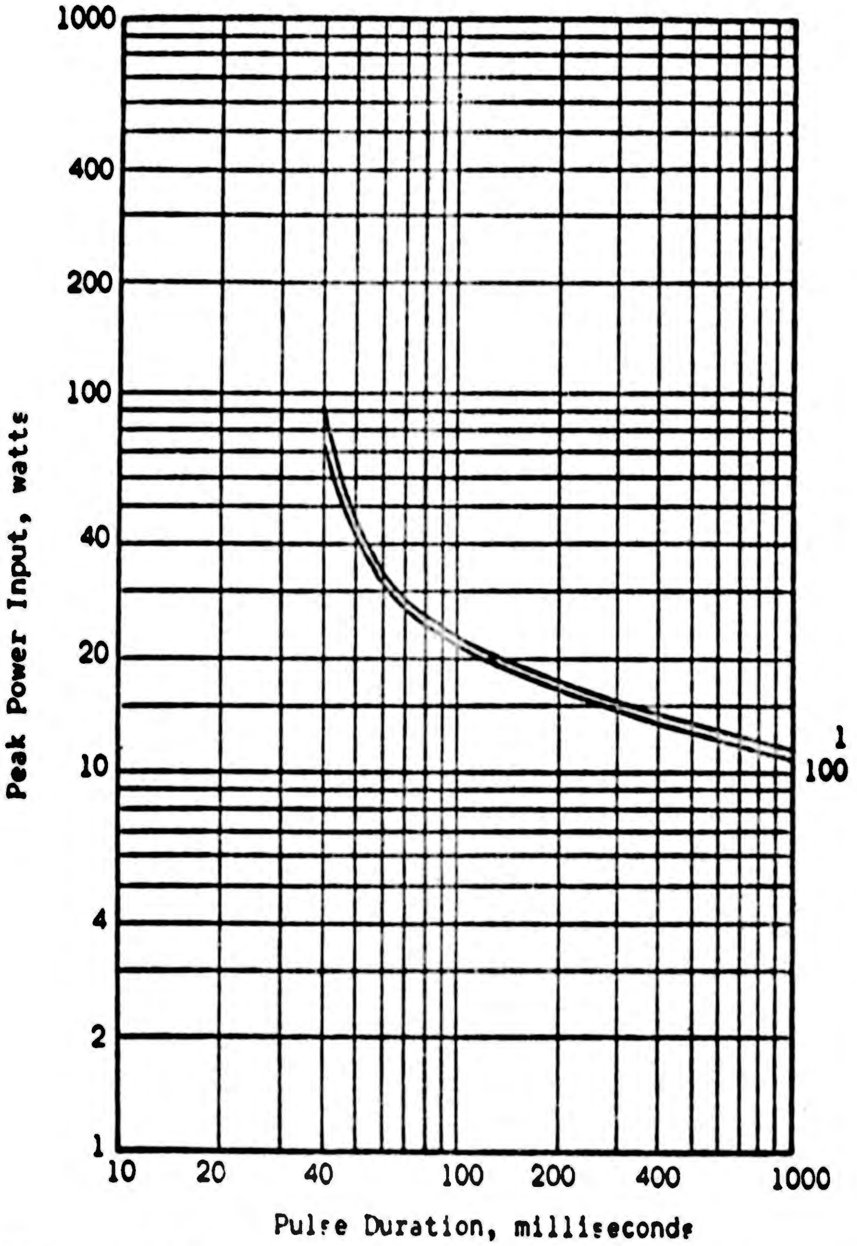


FIGURE B-26. 2N326 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

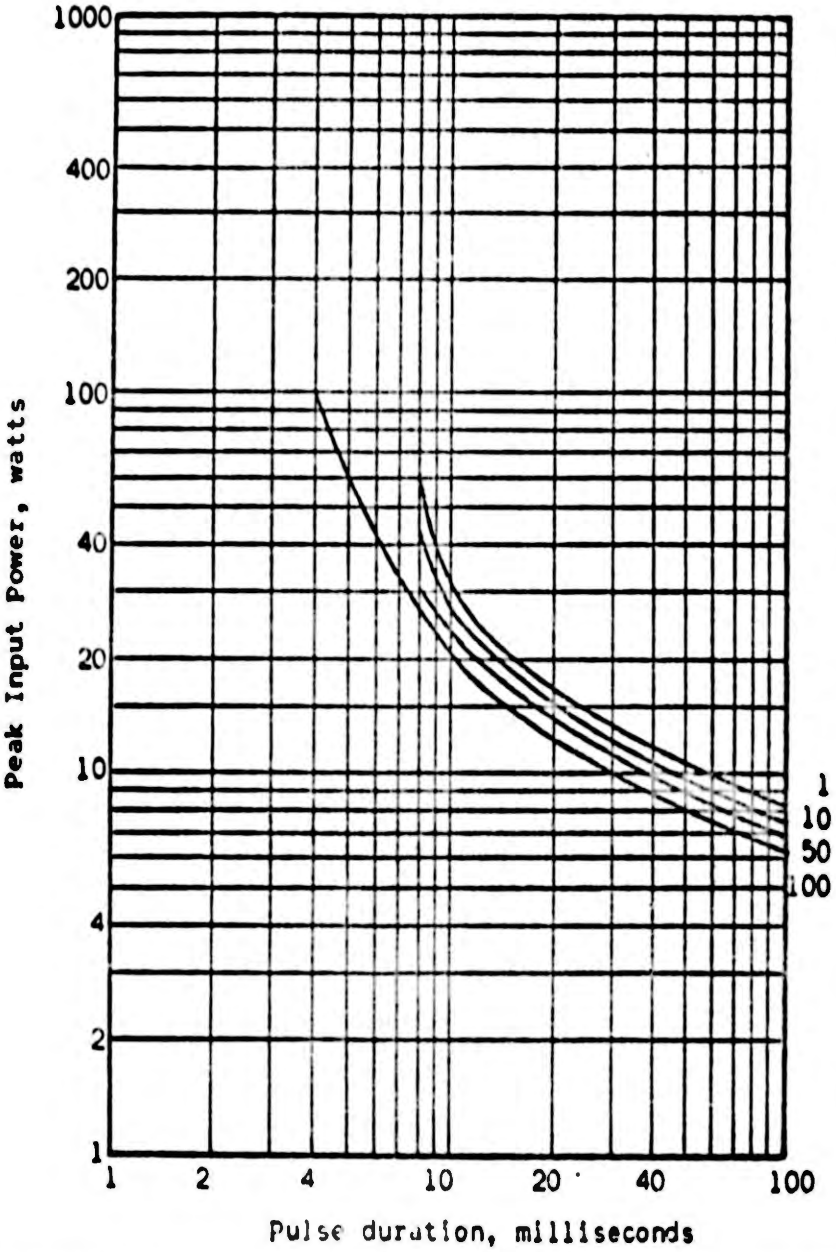


FIGURE B-27A. 2N326 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 10, 50, and 100

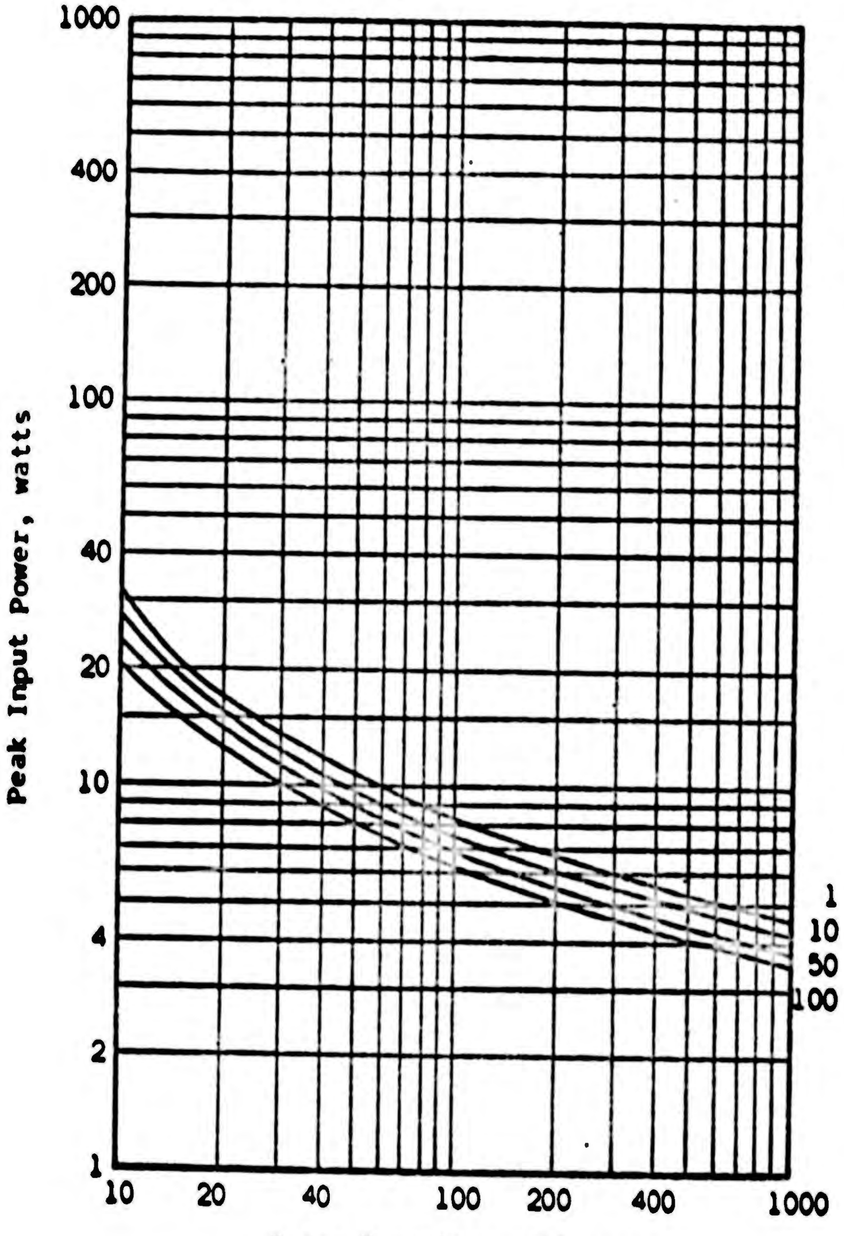


FIGURE B27B. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 10, 50, and 100

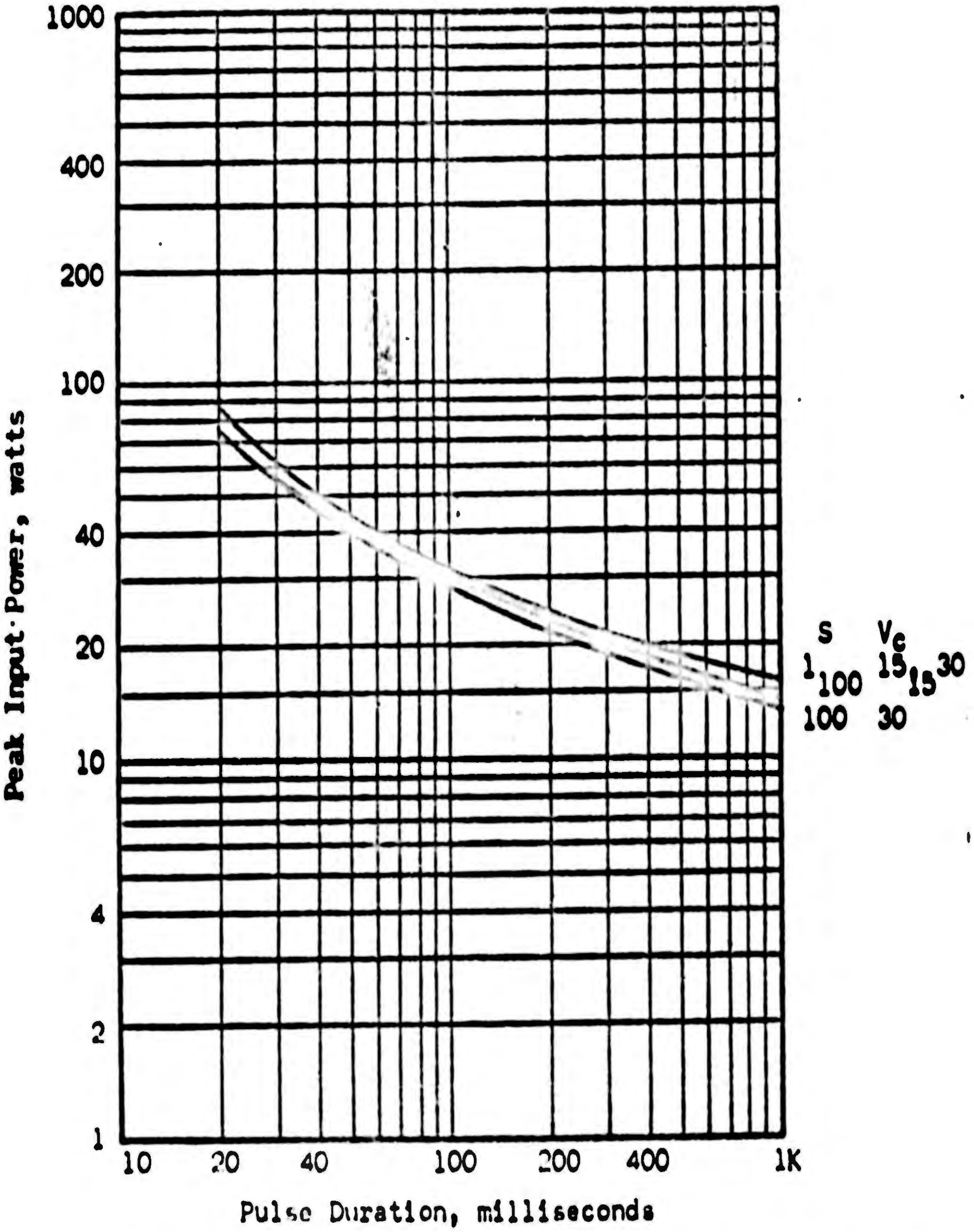


FIGURE B-28A. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

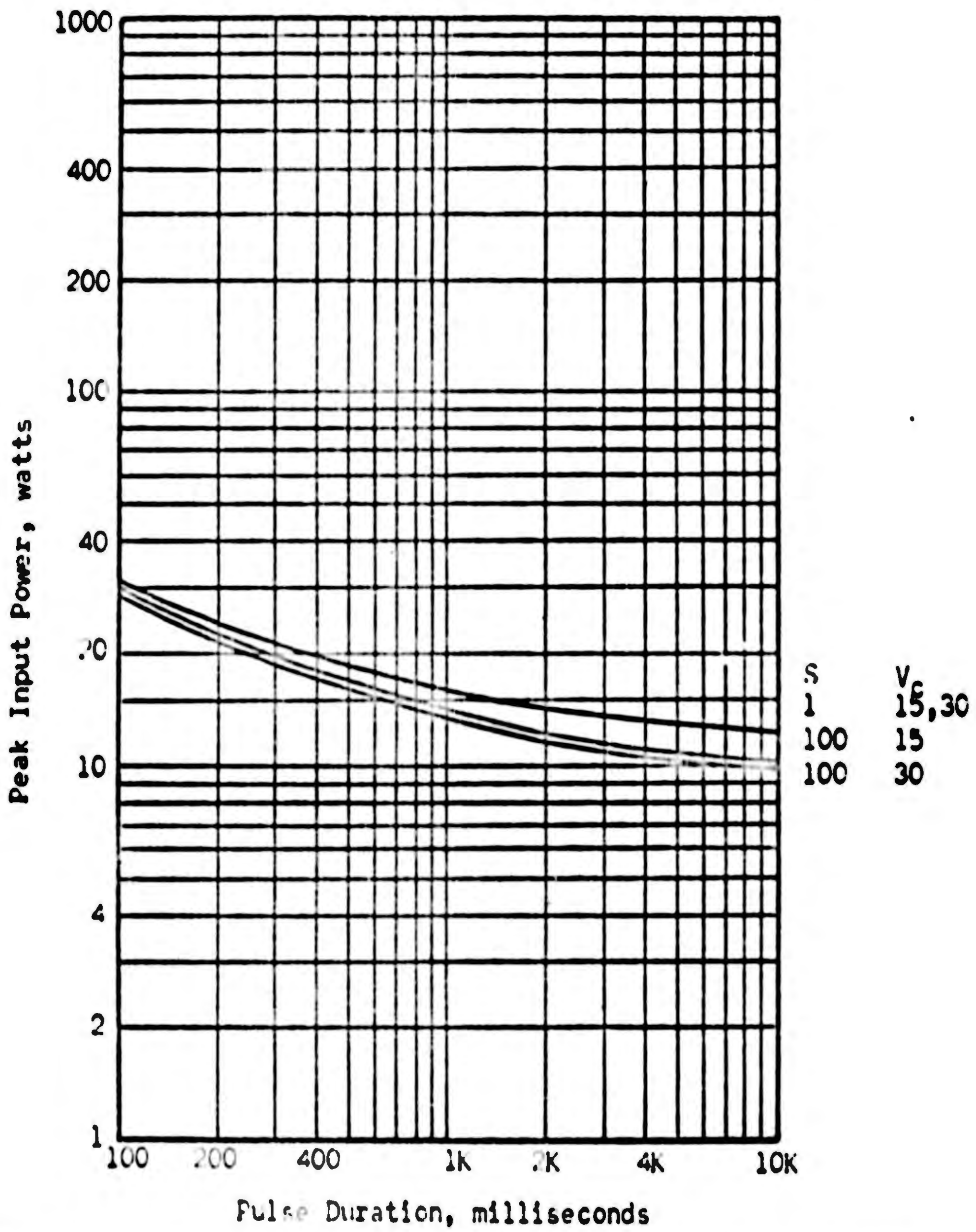


FIGURE B-28B. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

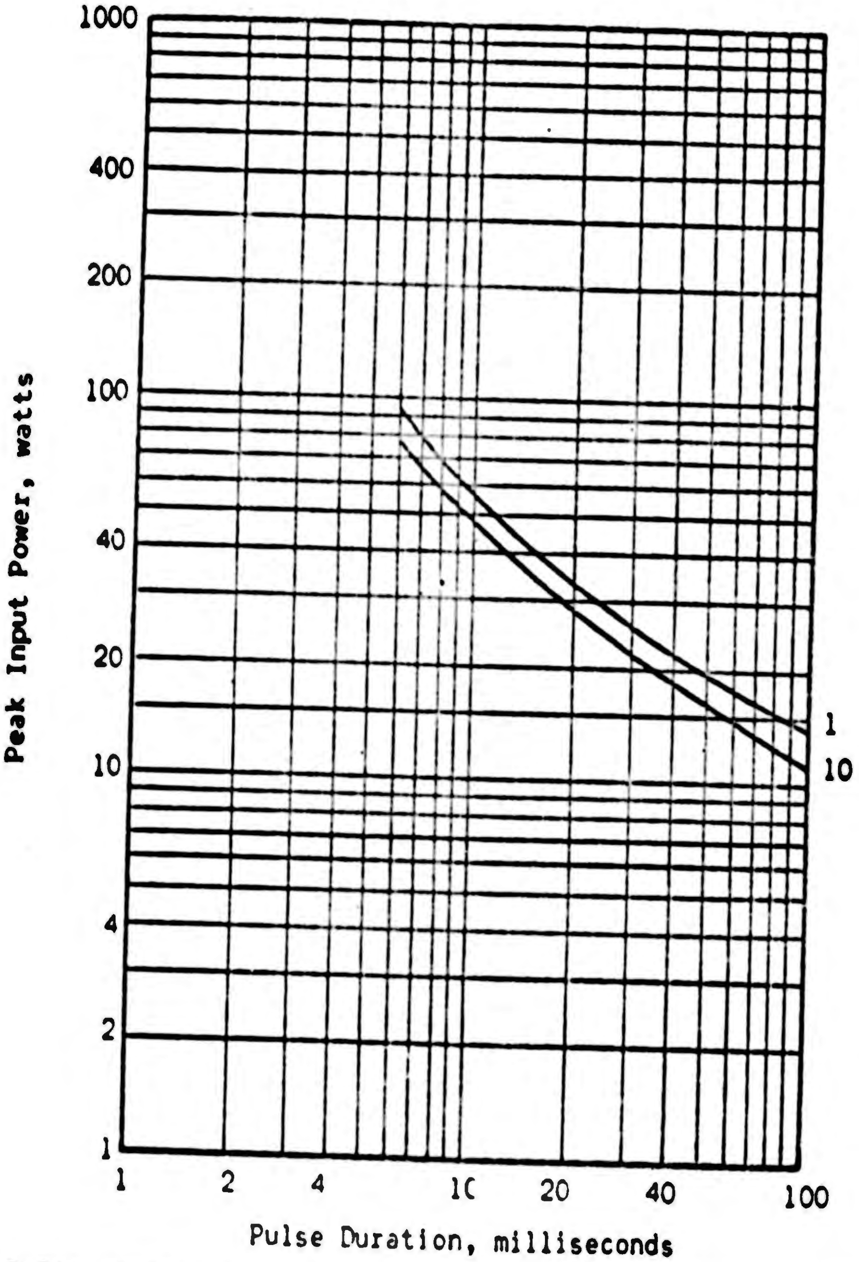


FIGURE B-29A. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse period
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

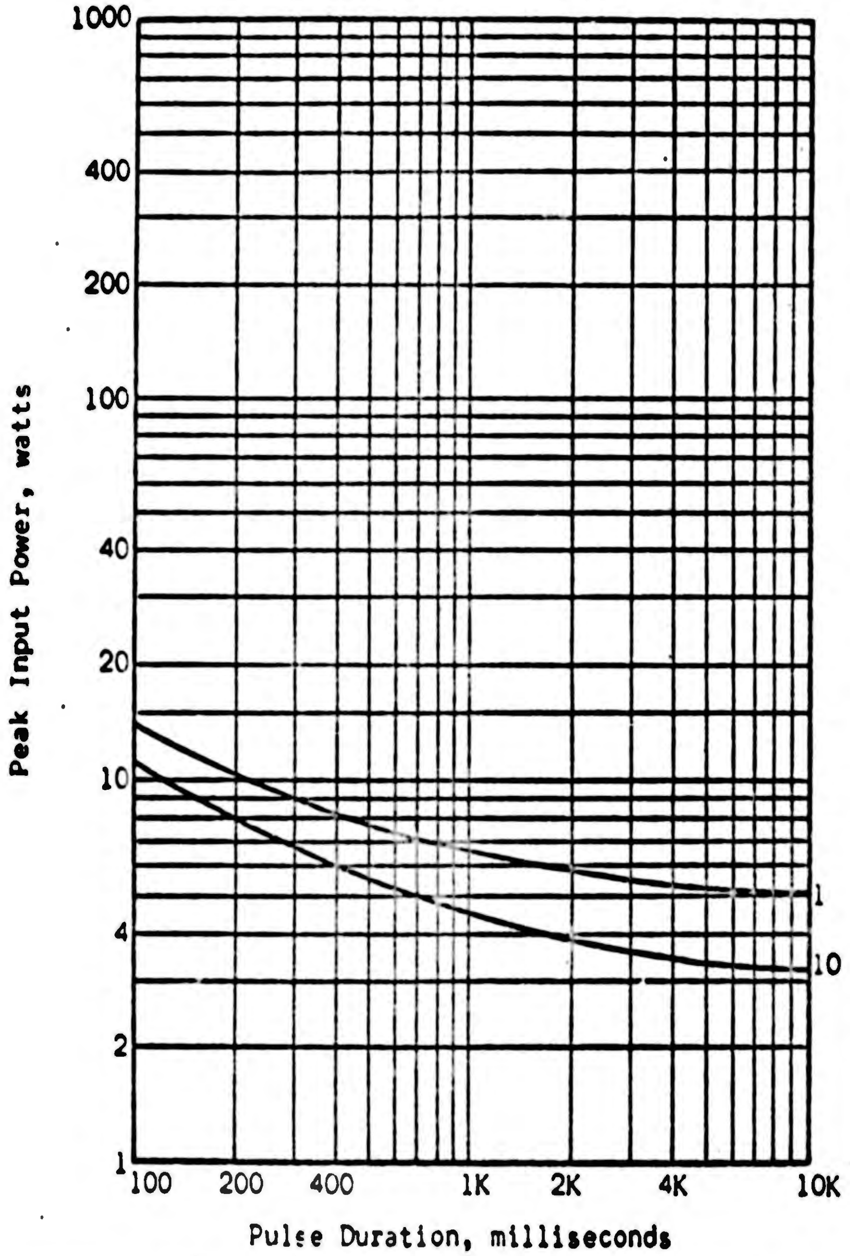


FIGURE B-29B. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse period
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

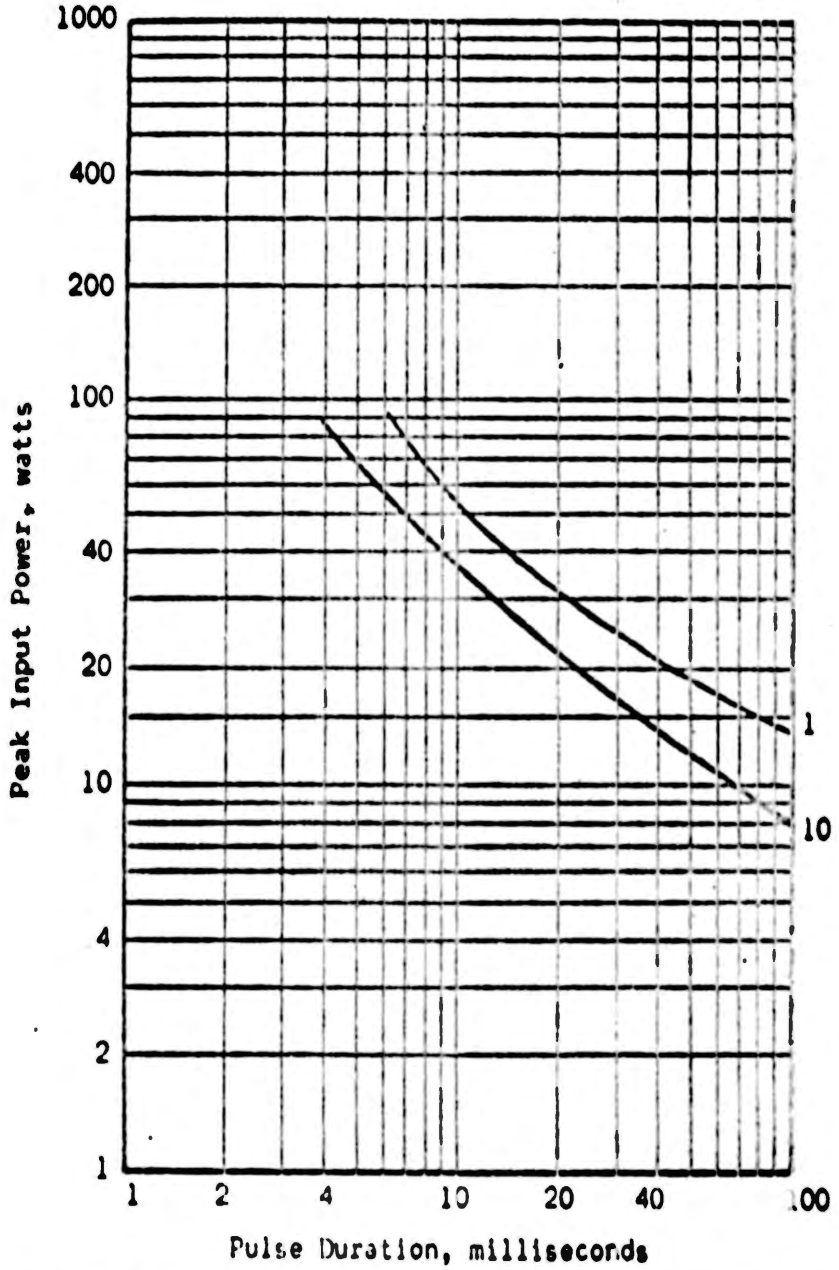


FIGURE B-30A. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse period
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

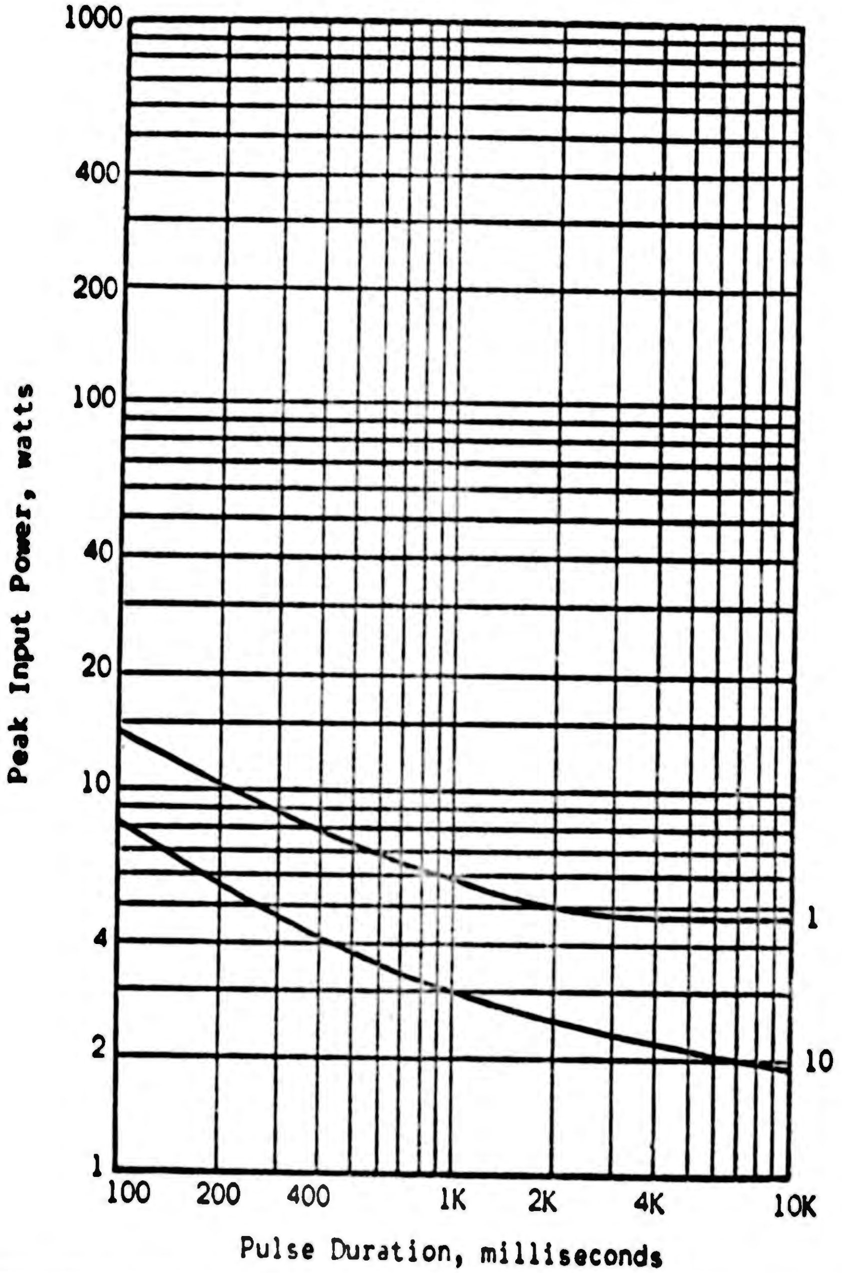


FIGURE B-30B. 2N326 PEAK POWER INPUT AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse period
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

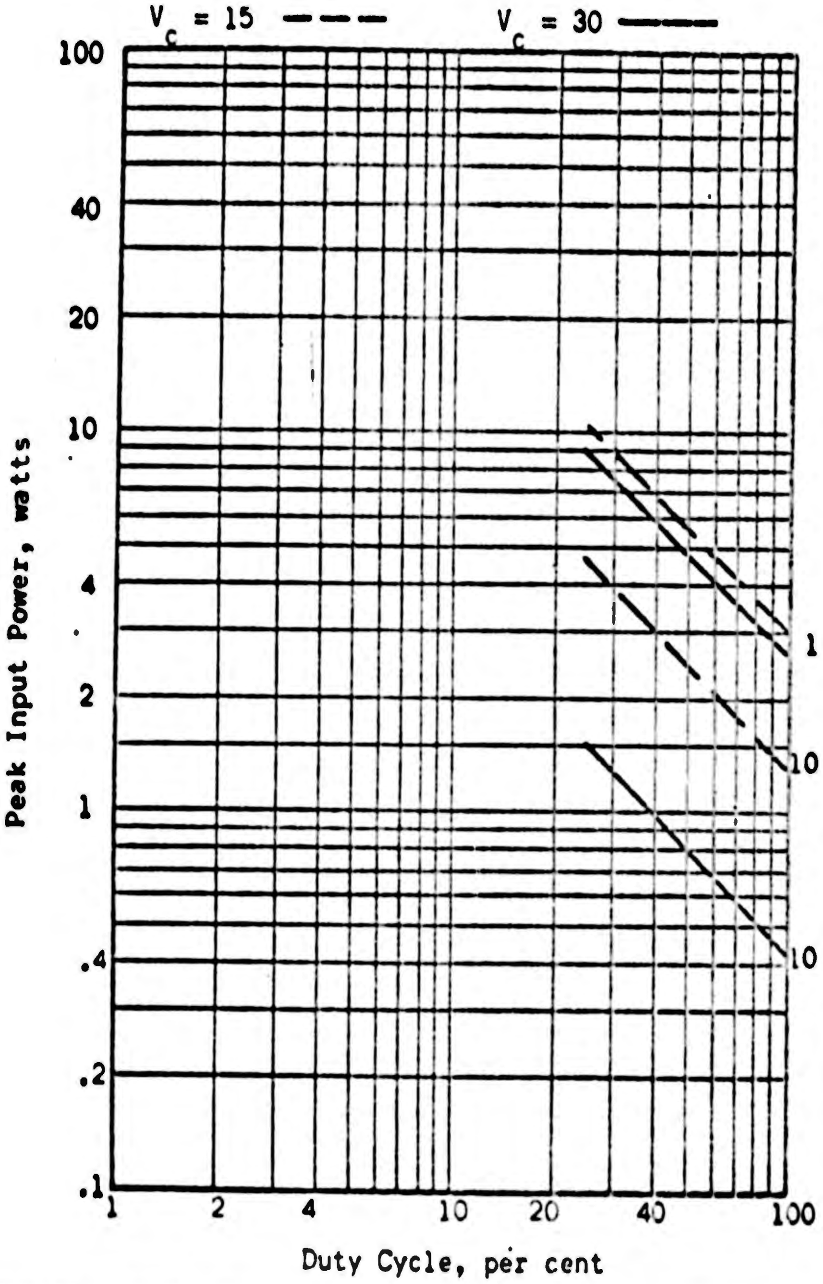


FIGURE B-31. 2N326 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1 millisecond
Collector voltage = 15 and 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10
Zero input peak junction temperature = 85 C for
V_c = 15 and S = 27
V_c = 30 and S = 13

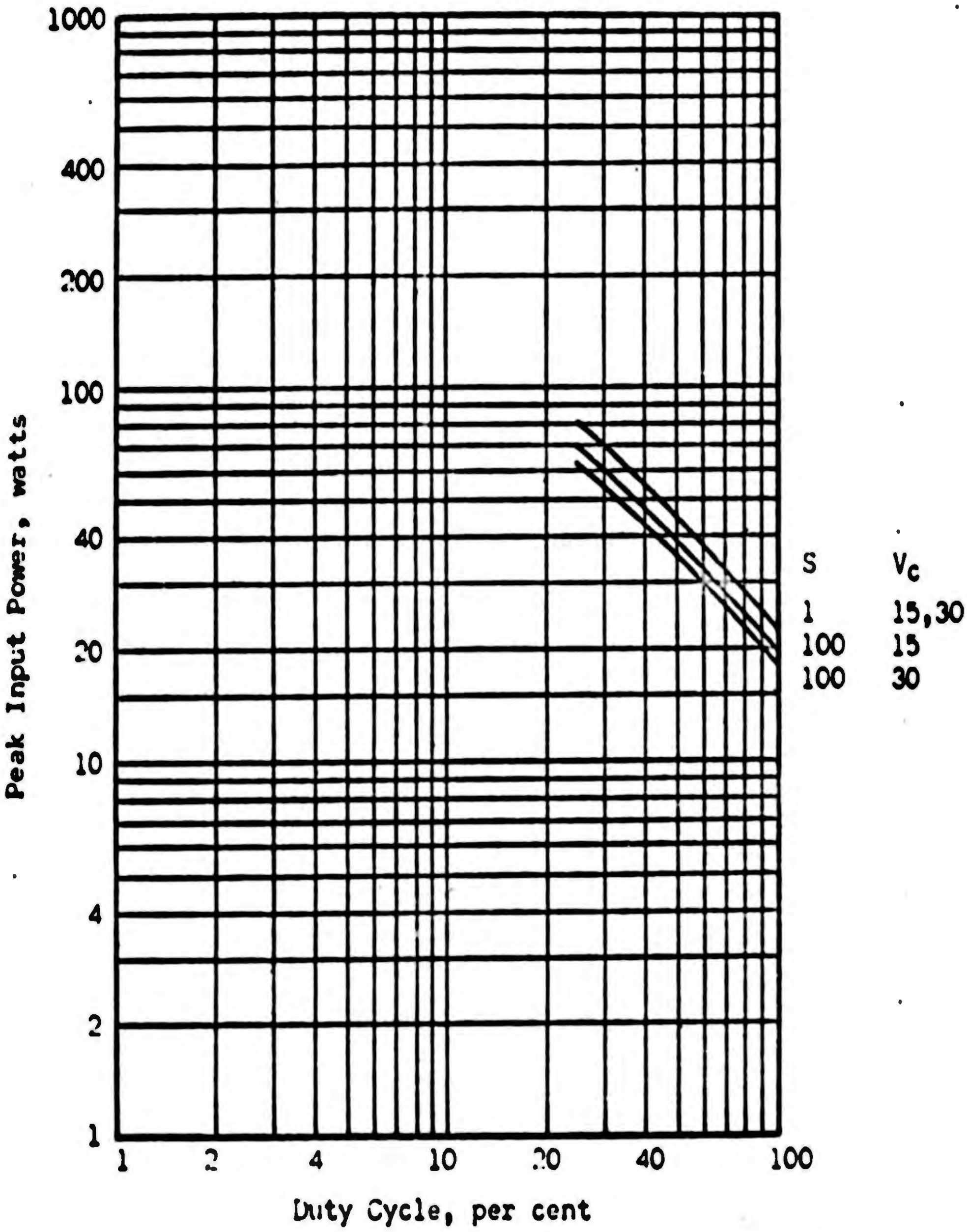


FIGURE B-32. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1 millisecond
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor ≐ 1 and 100

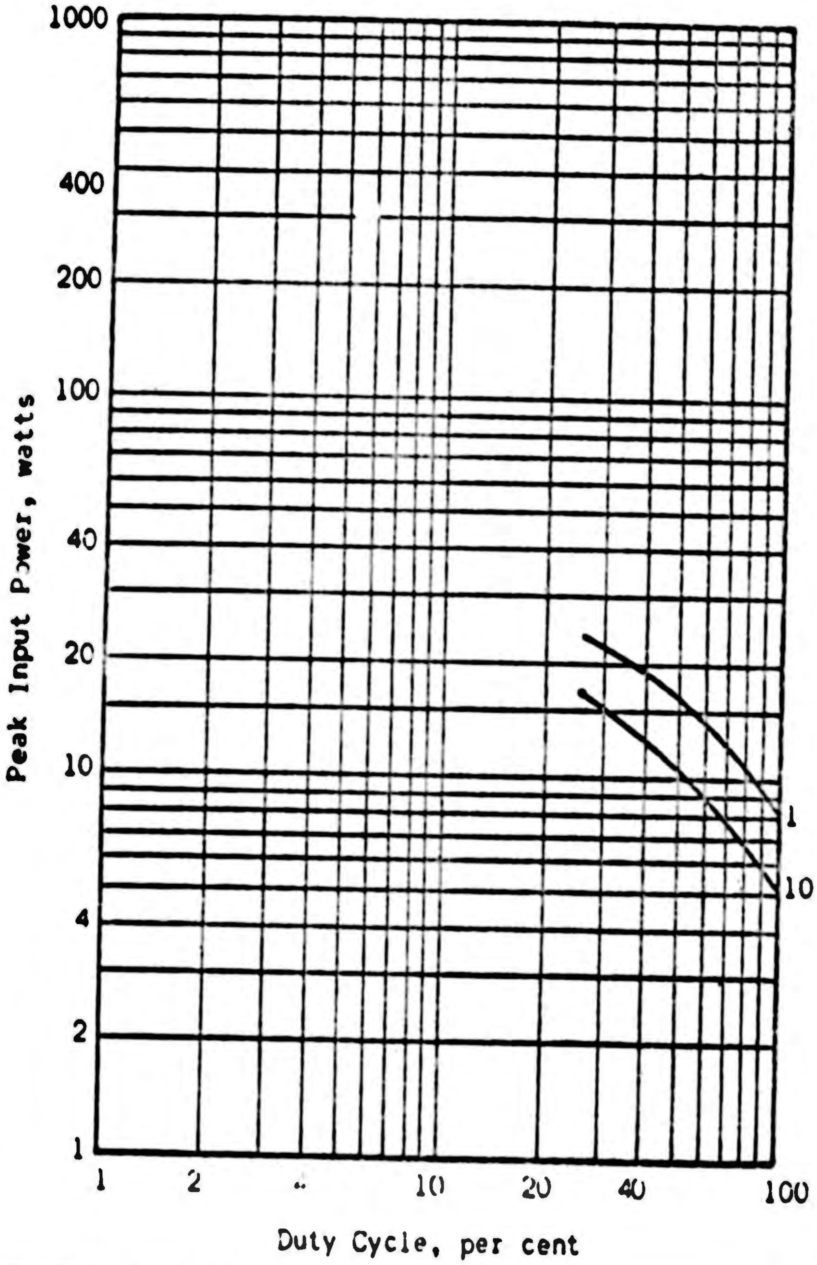


FIGURE B-33. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition rate = 1 millisecond
Collector voltage = 15 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

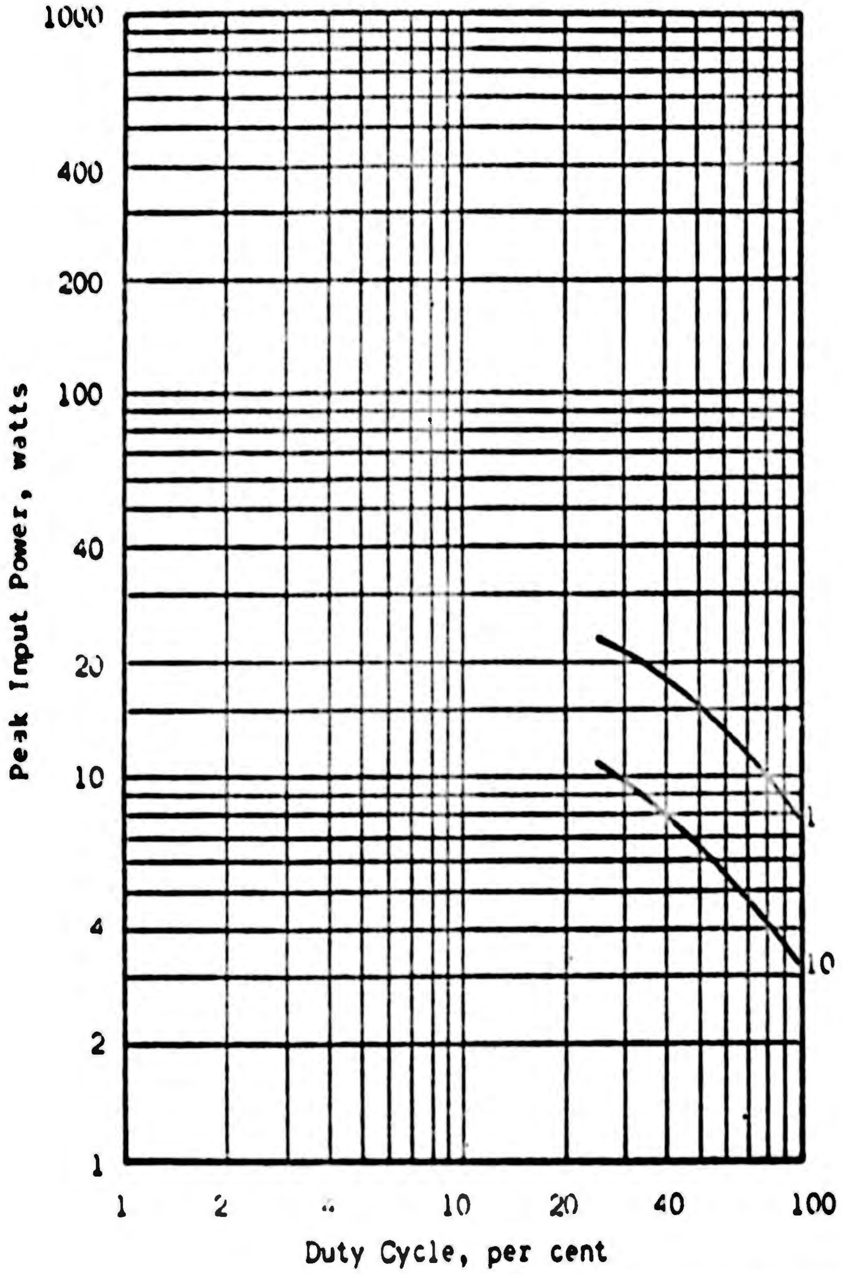


FIGURE B-34. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition rate = 1 millisecond
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 10

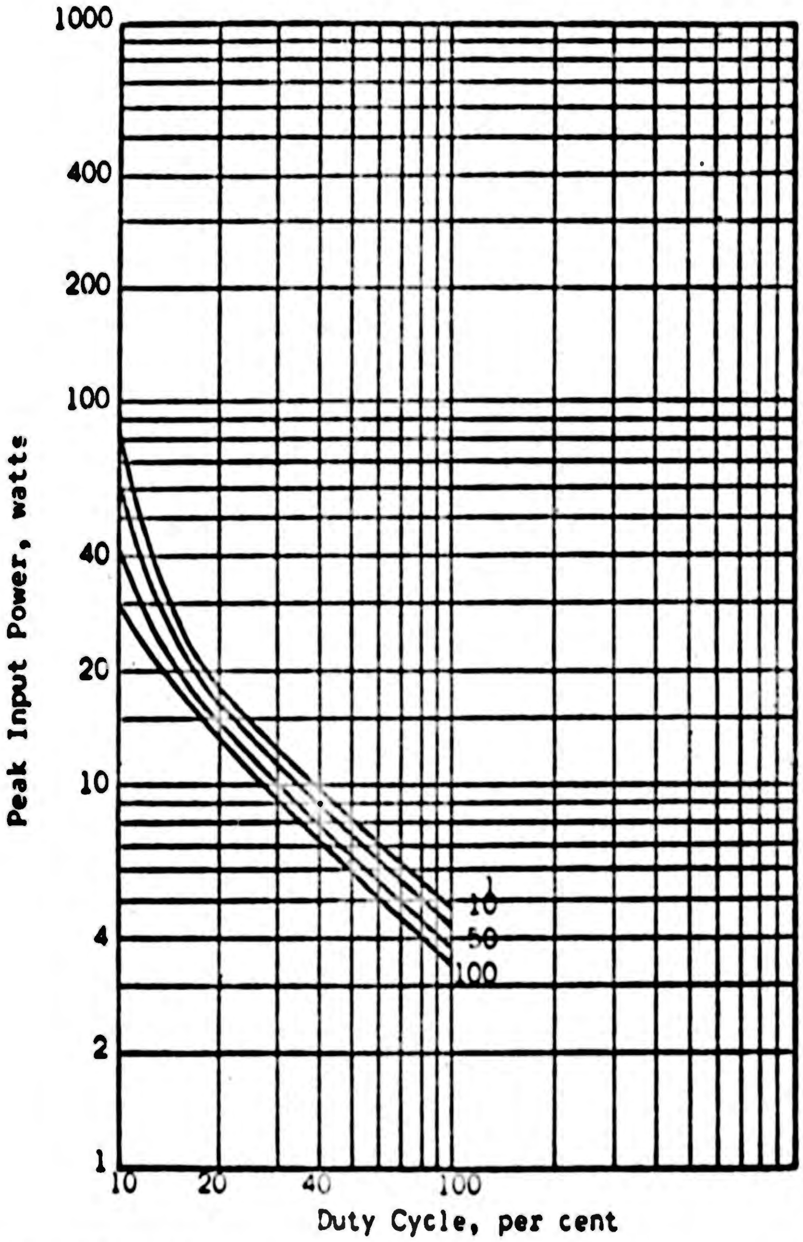


FIGURE B-35. 2N326 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 10, 50, and 100

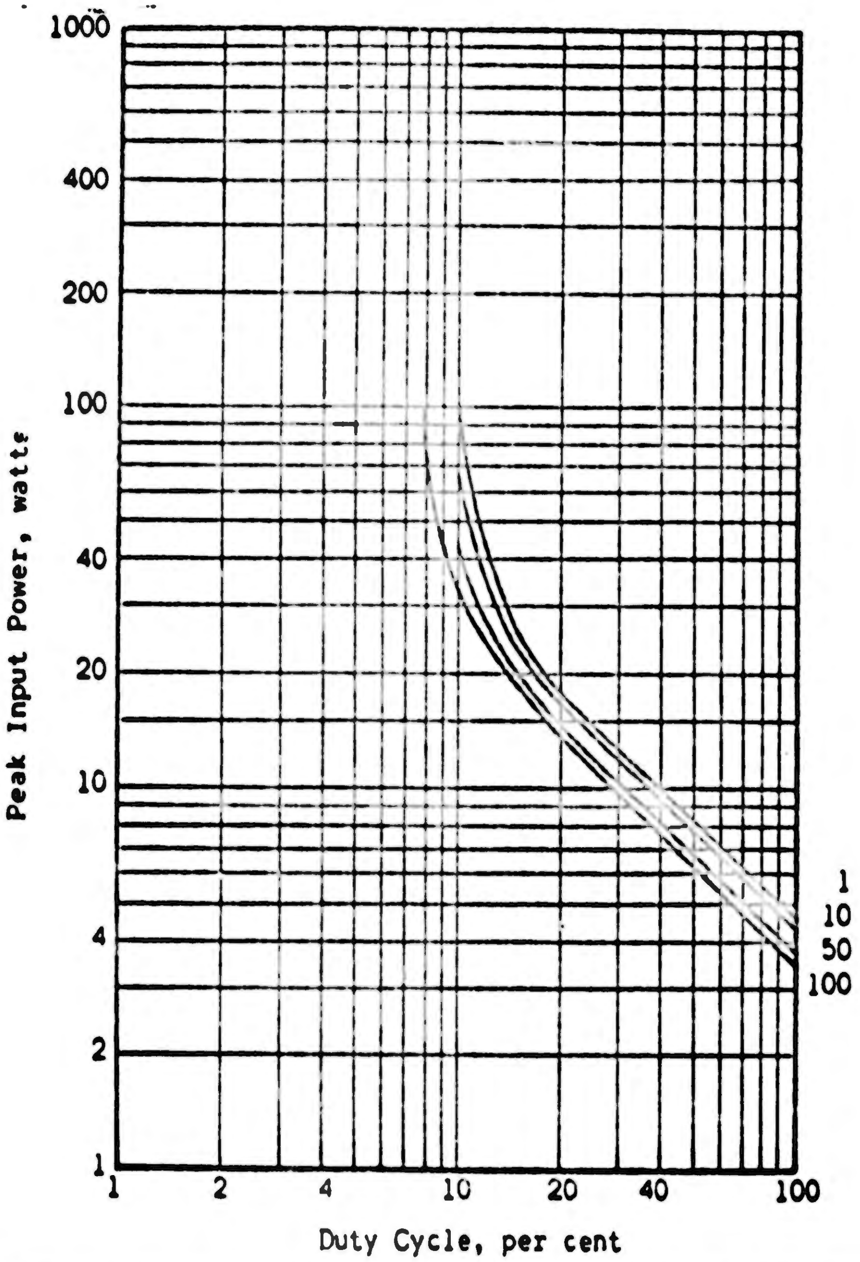


FIGURE B-36. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 10, 50, and 100

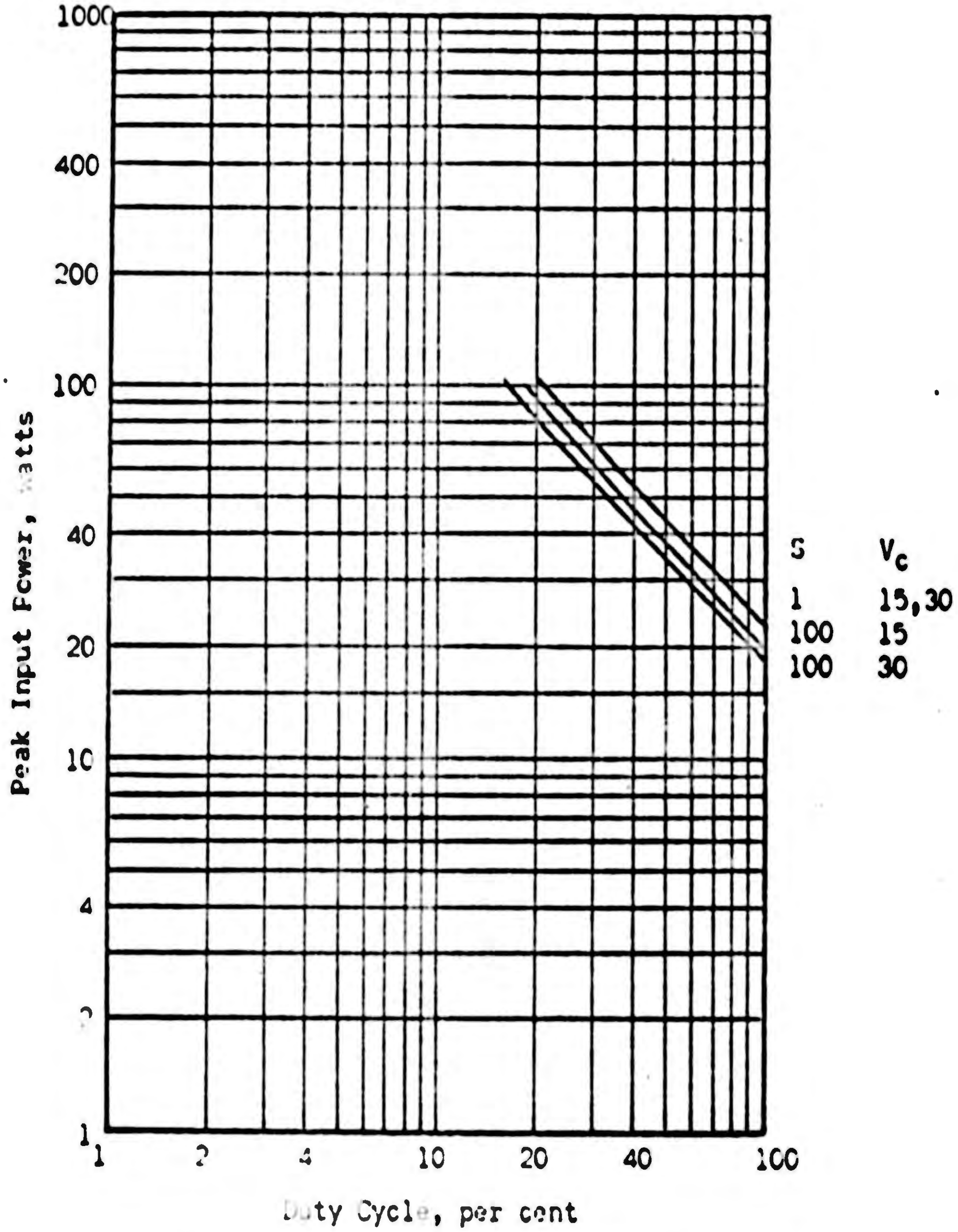


FIGURE B-37. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition Period = 10 milliseconds
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

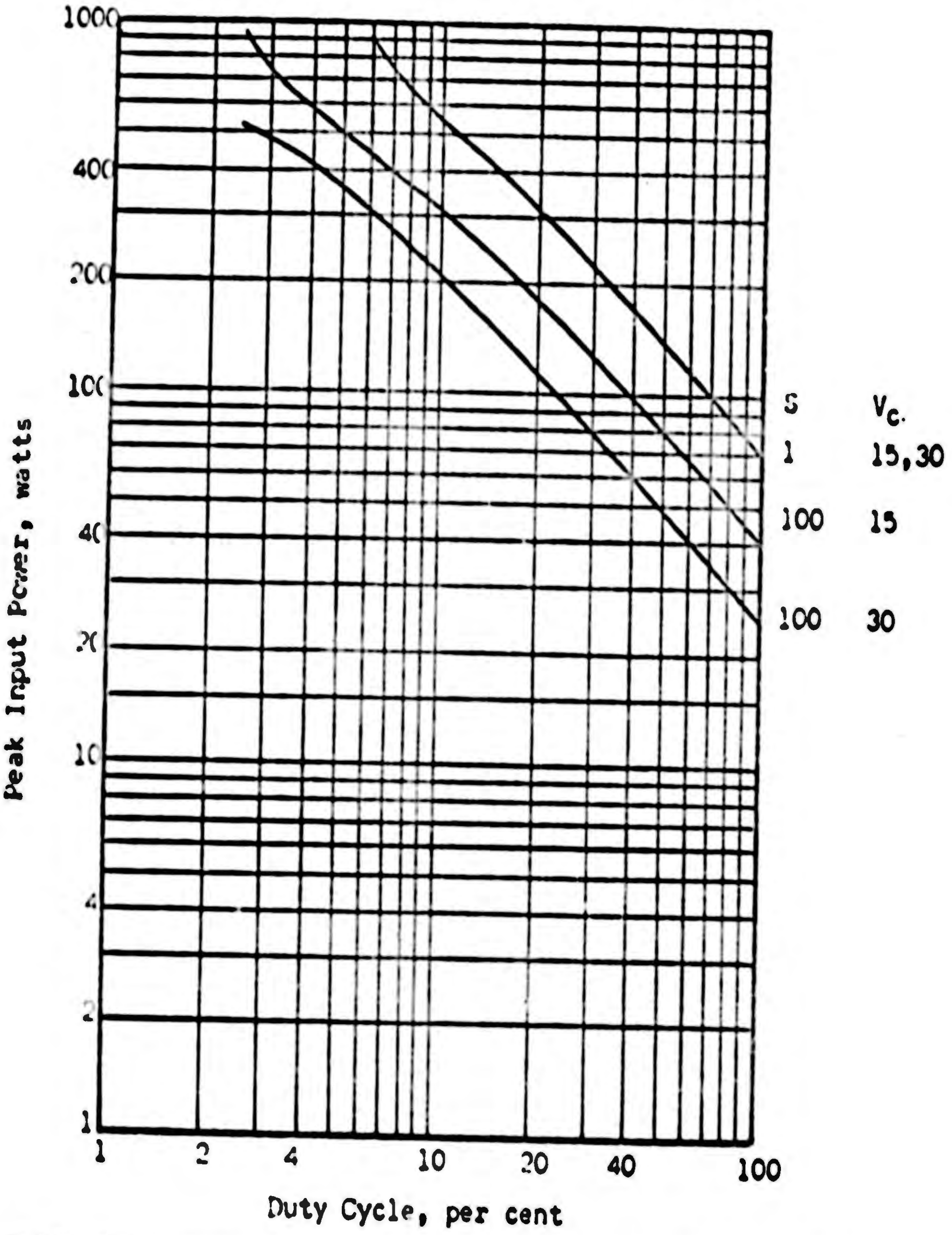


FIGURE B-38. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Collector voltage = 15 and 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

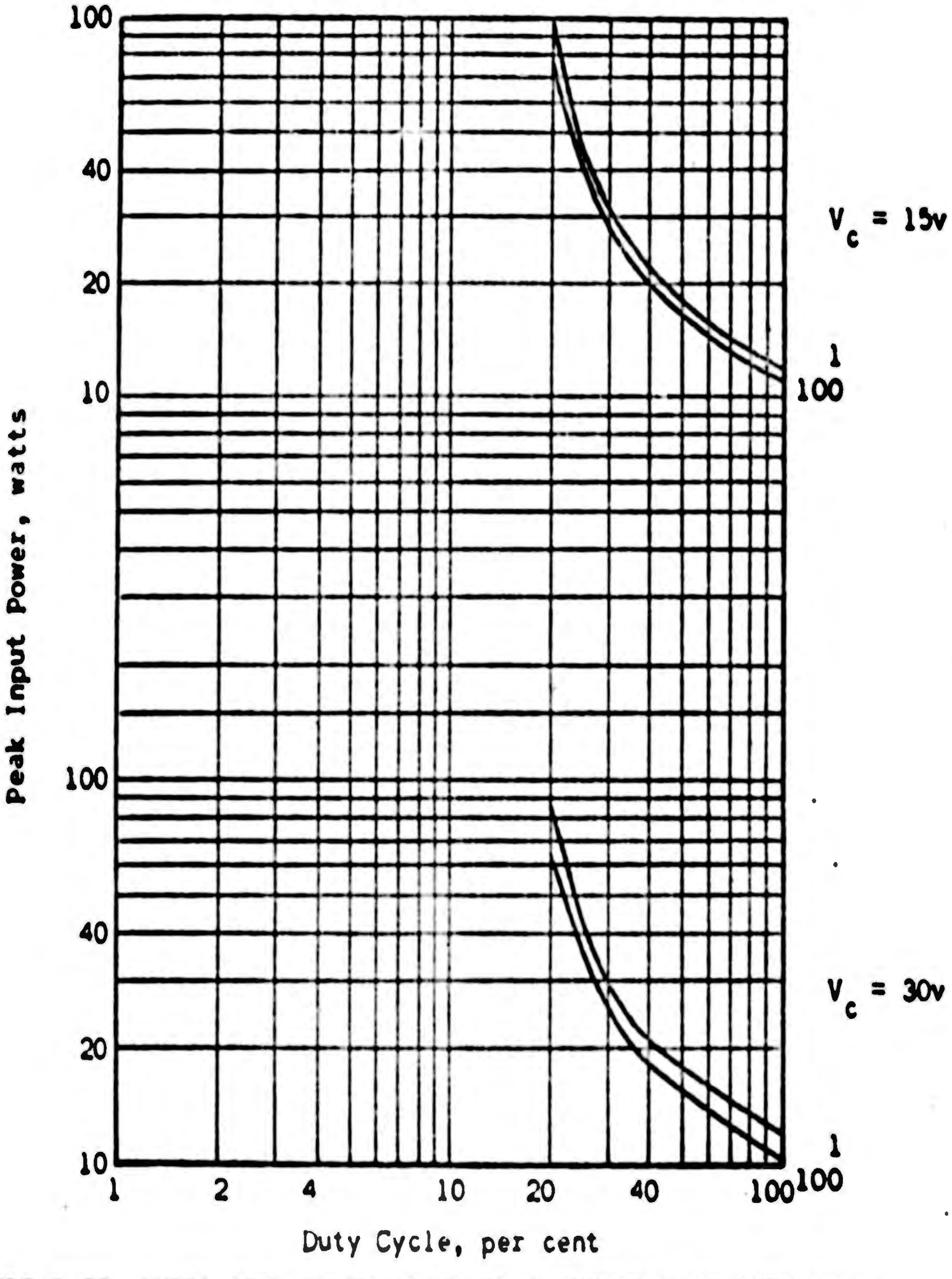


FIGURE B-39. 2N326 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

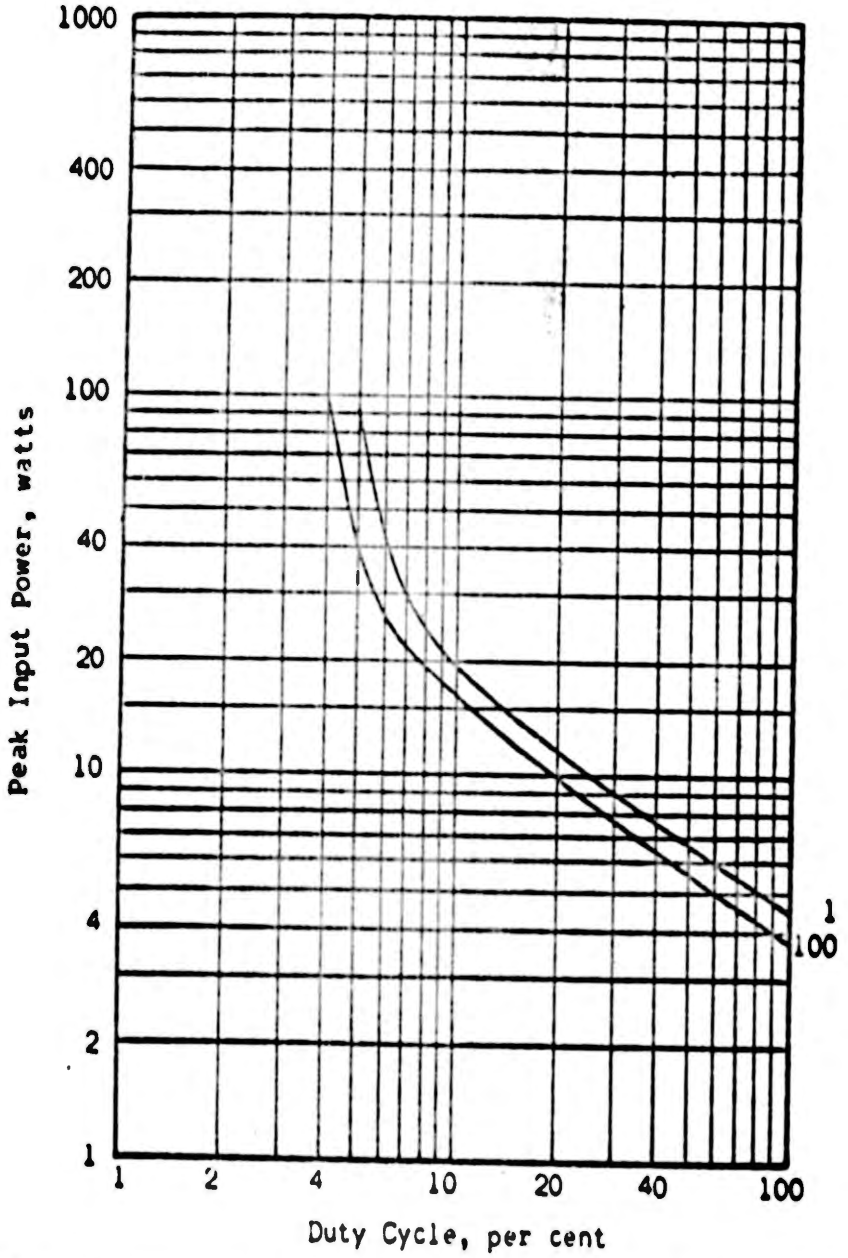


FIGURE B-40. 2N326 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 15 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

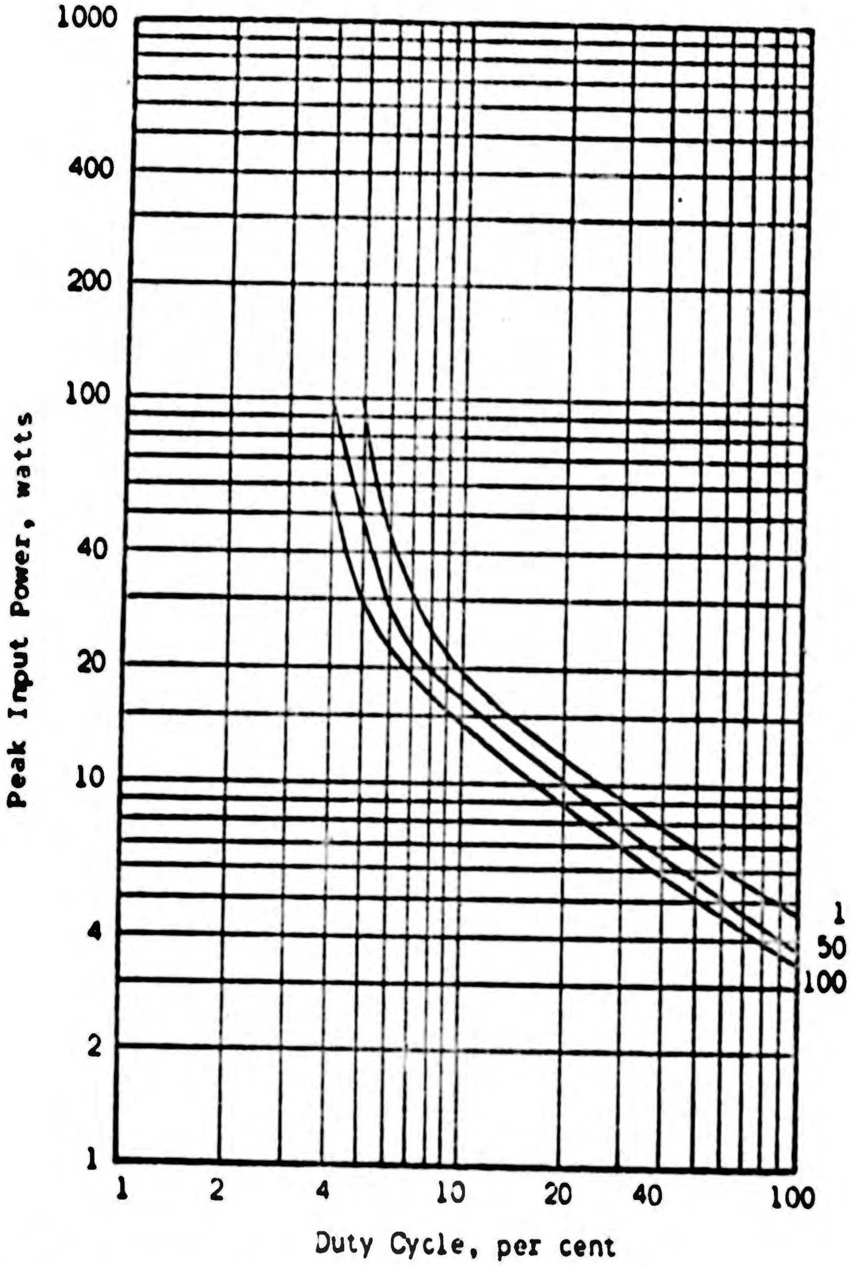


FIGURE B-41. 2N326 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1, 50, and 100

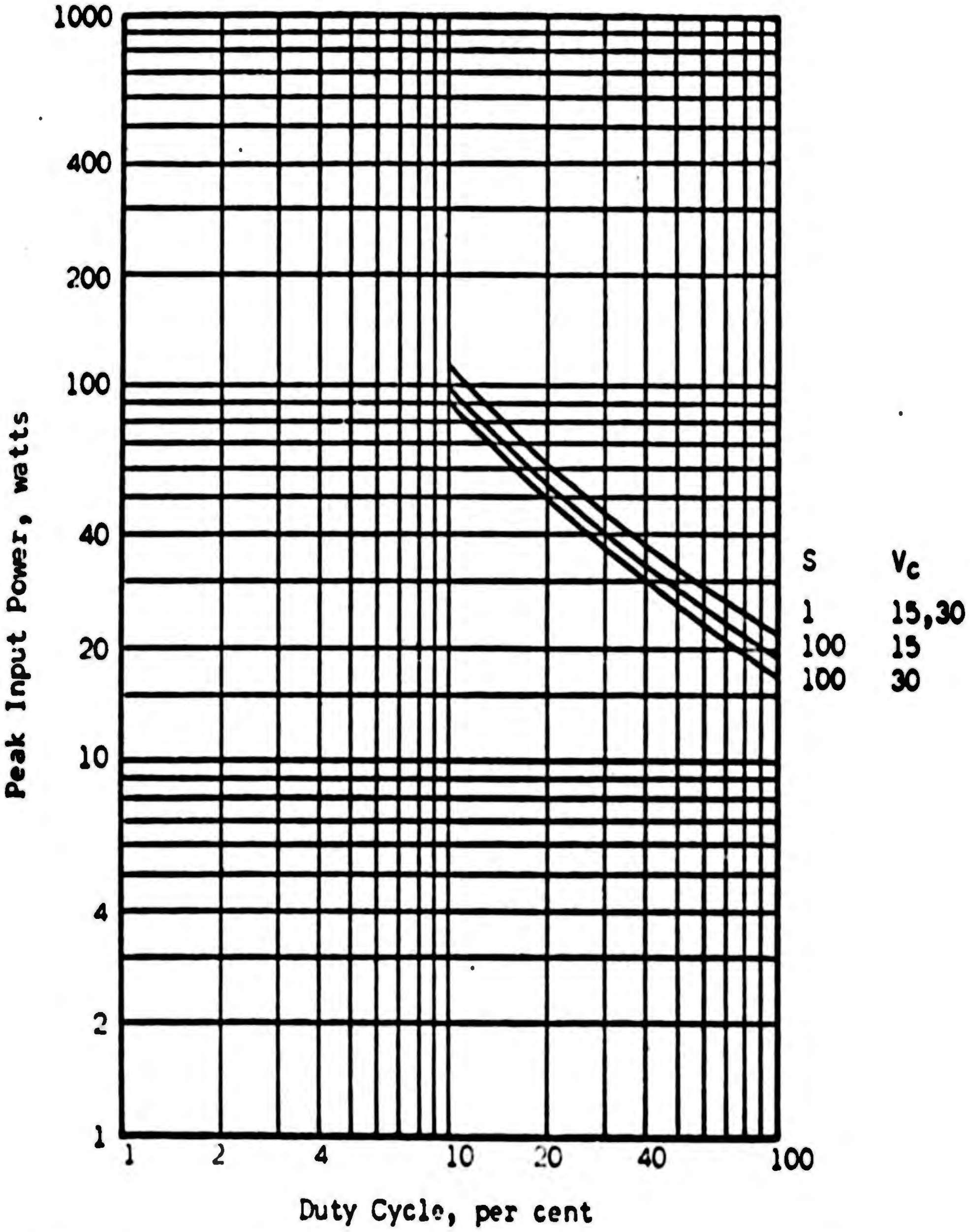


FIGURE B-42. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 and 30 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

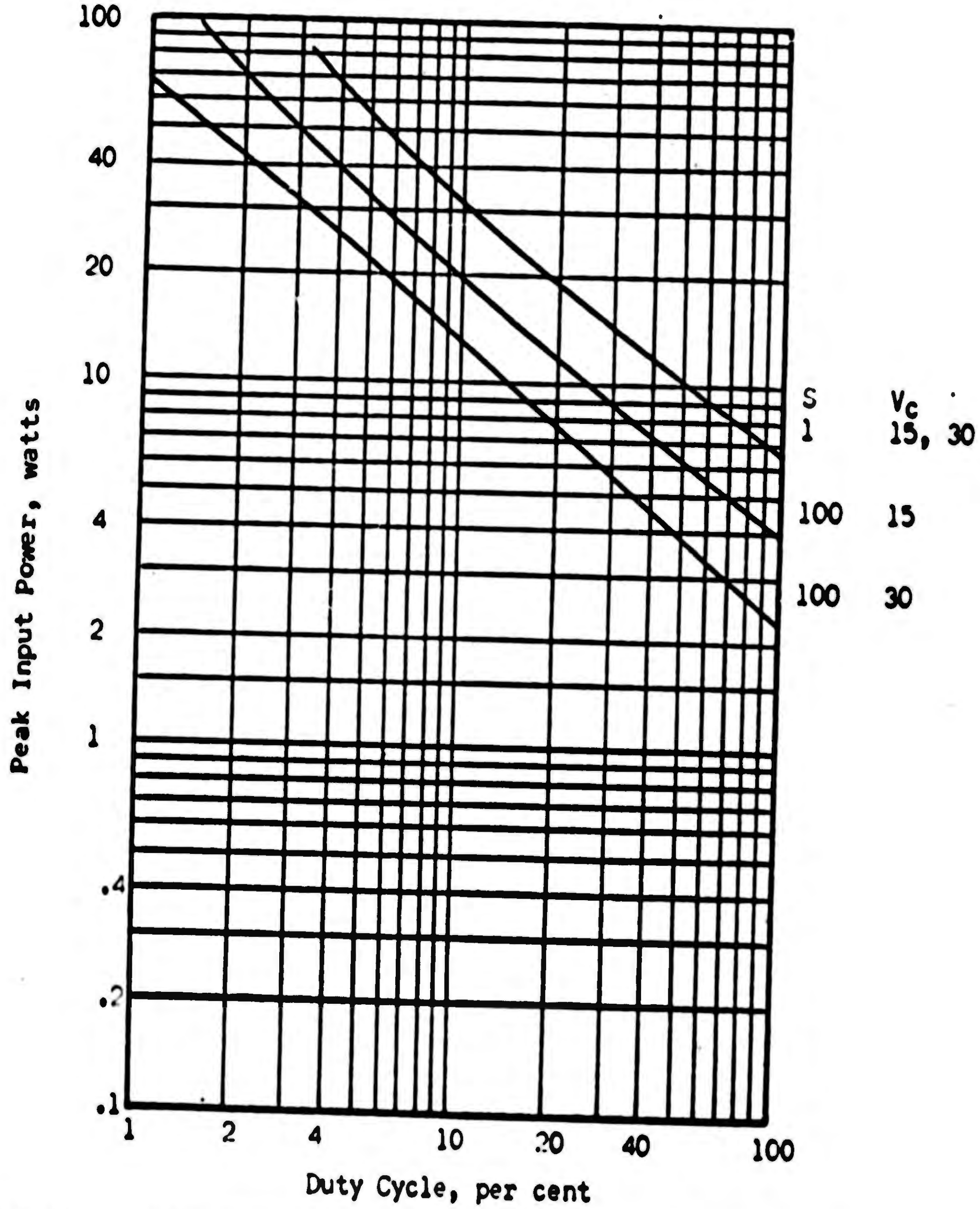


FIGURE B-43. 2N326 PEAK POWER INPUT AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Collector voltage = 15 and 30 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = 1 and 100

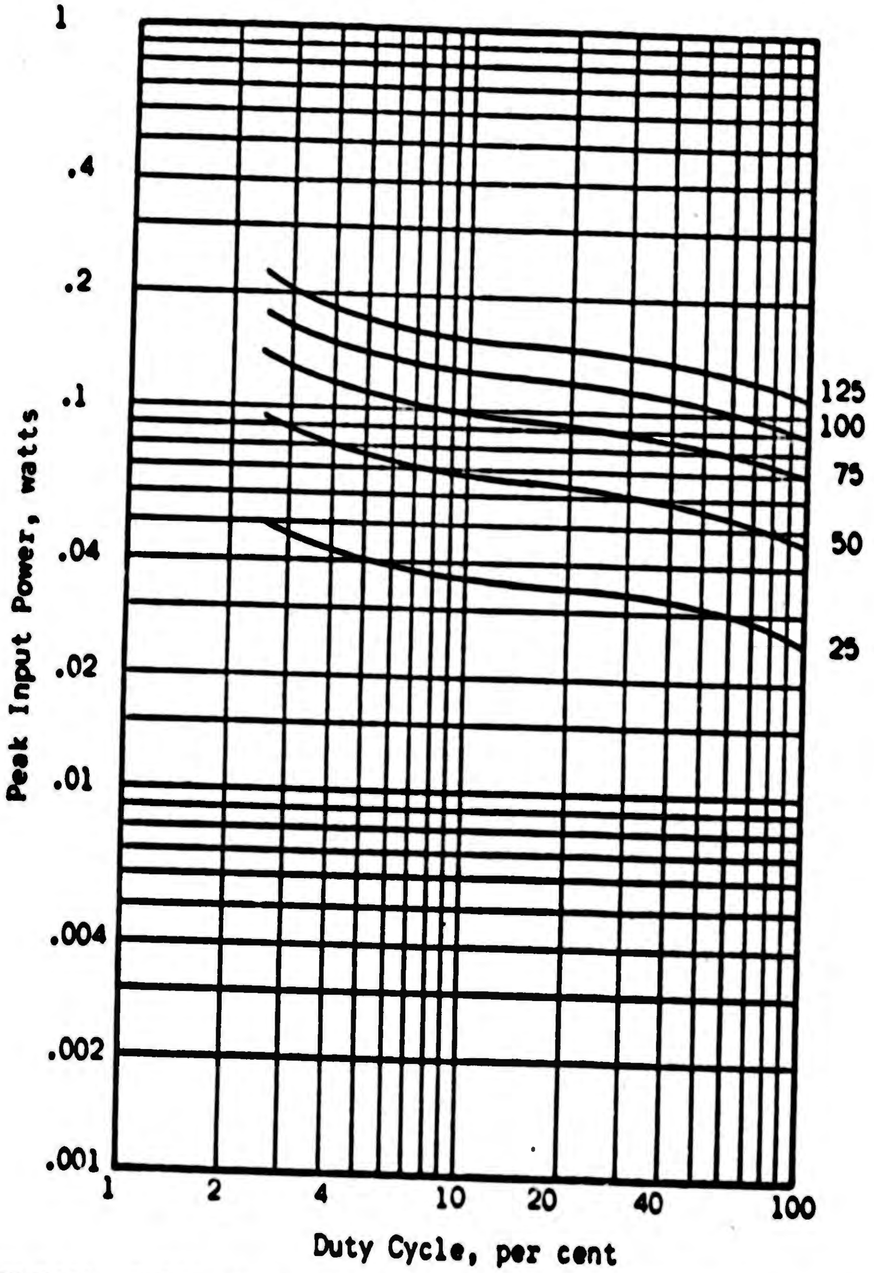


FIGURE B44A. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

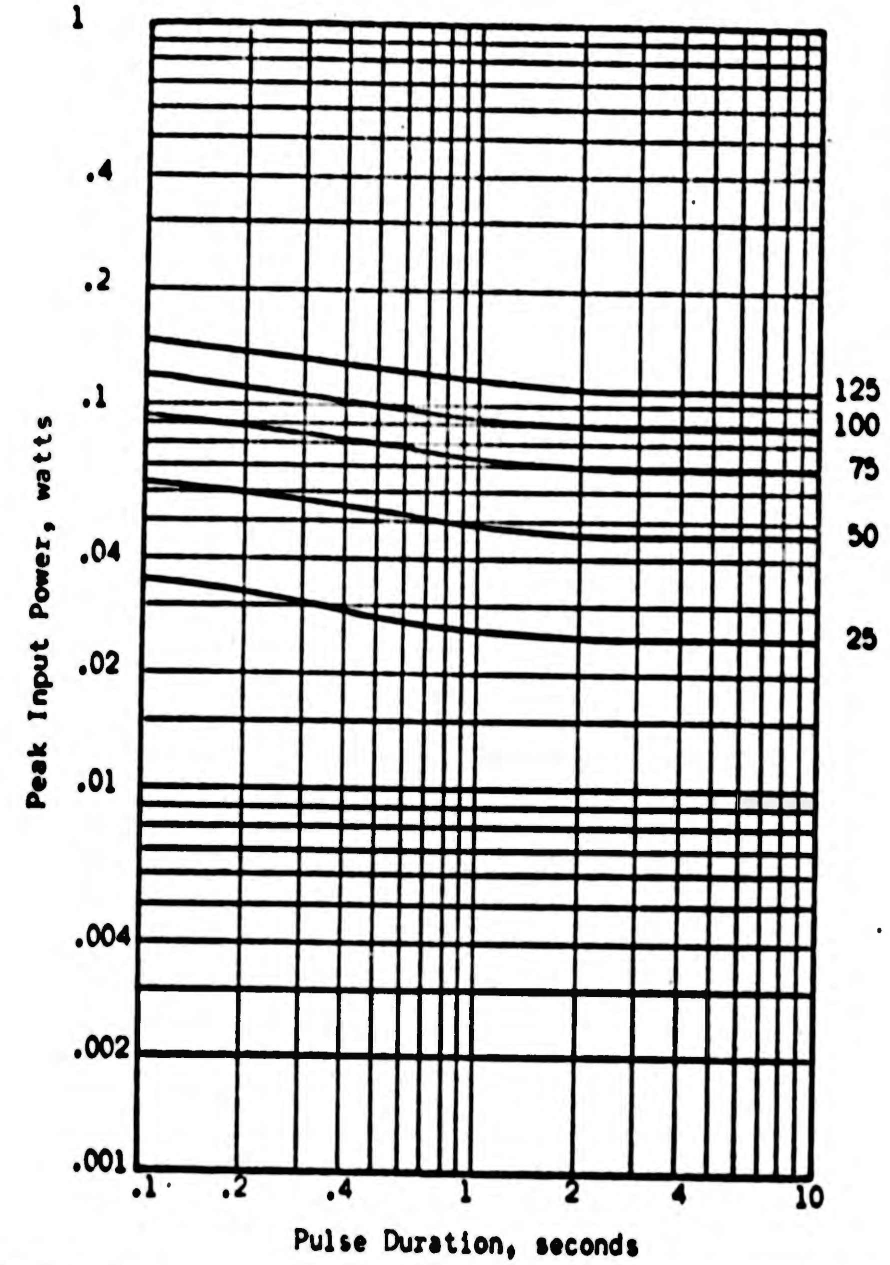


FIGURE B44B. 2N335 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

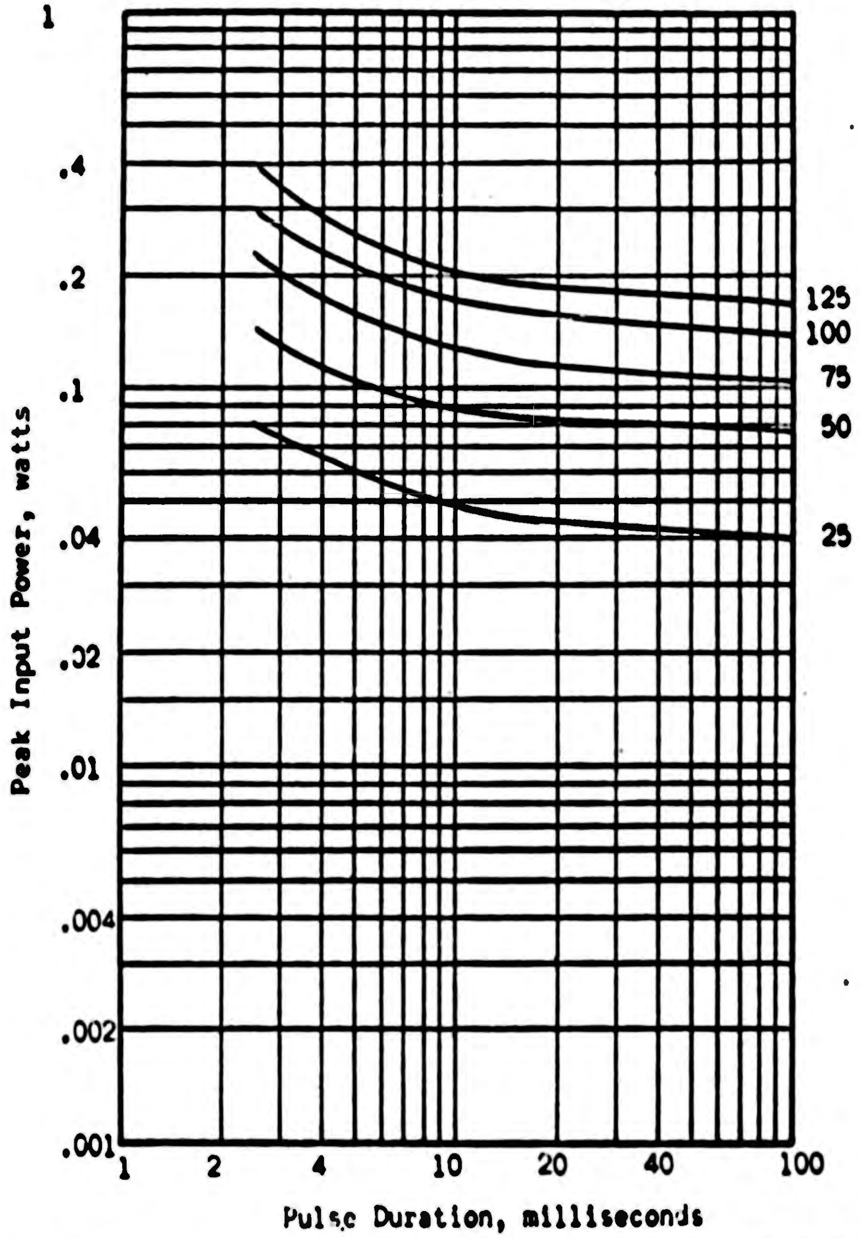


FIGURE B-45A 2N335 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

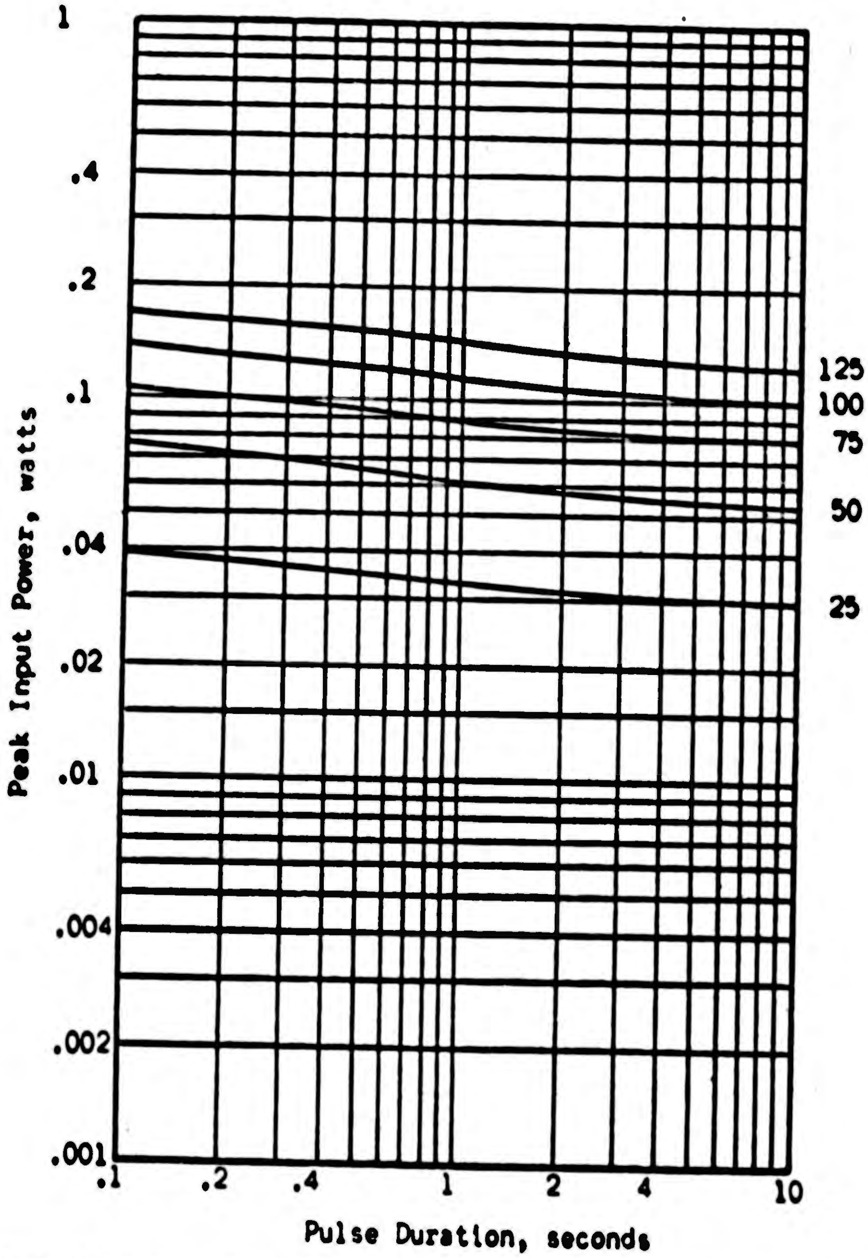


FIGURE B-45B.2N335 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse input
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

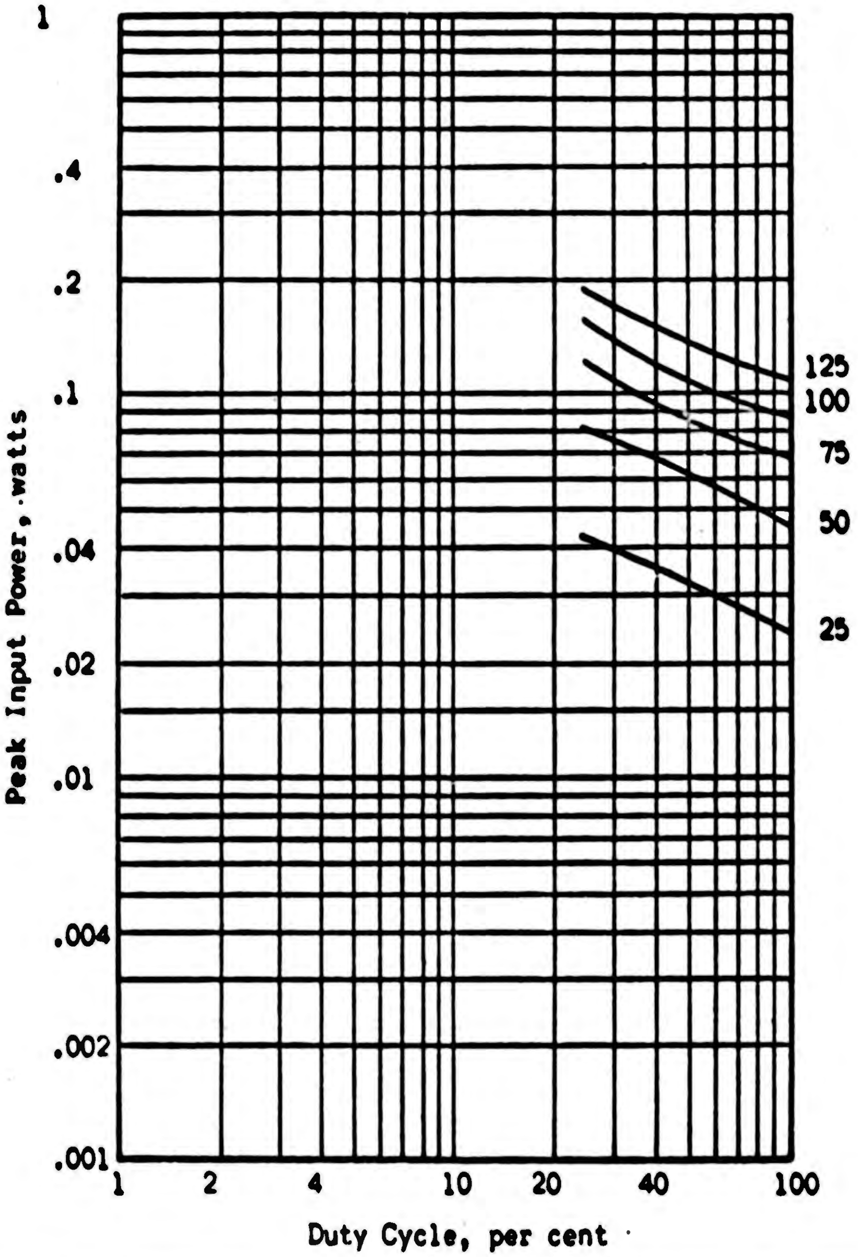


FIGURE B-46. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

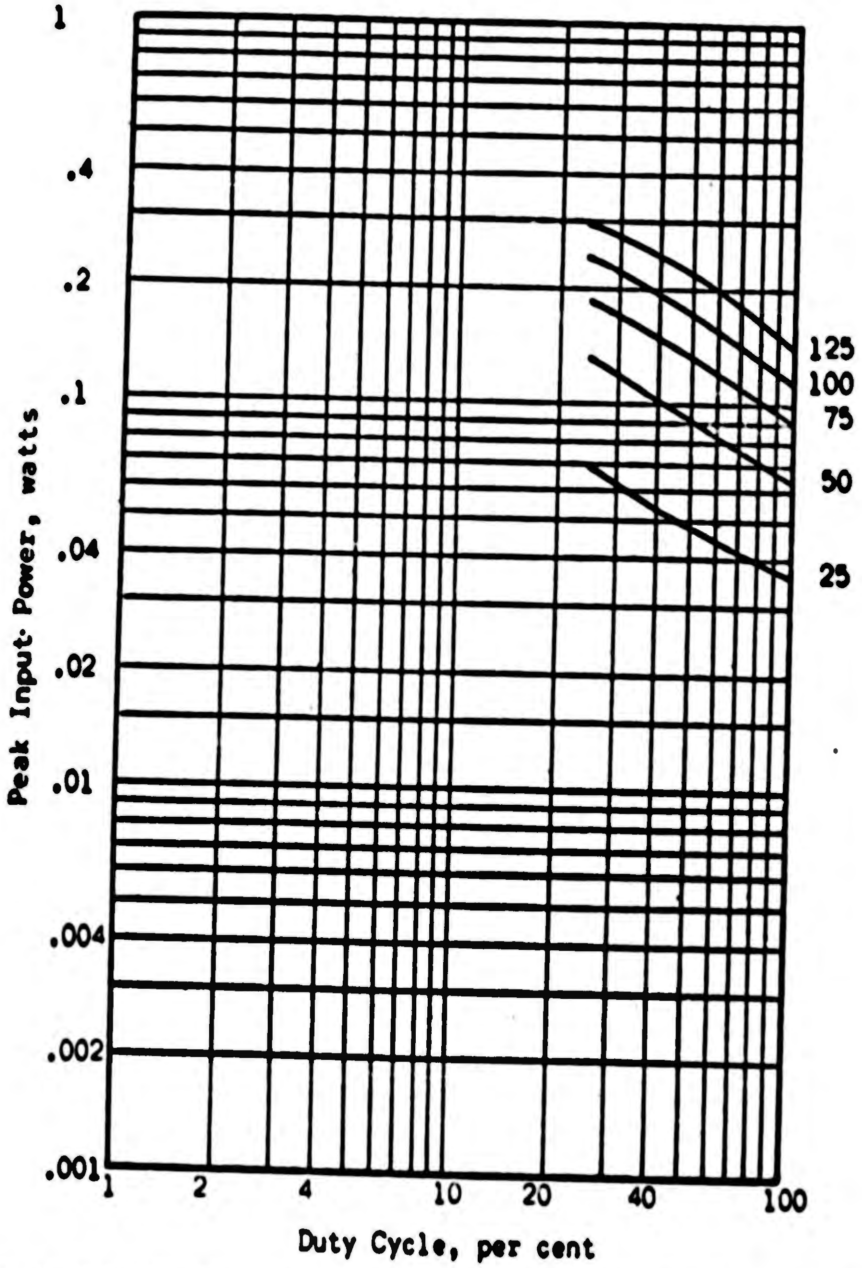


FIGURE B-47. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

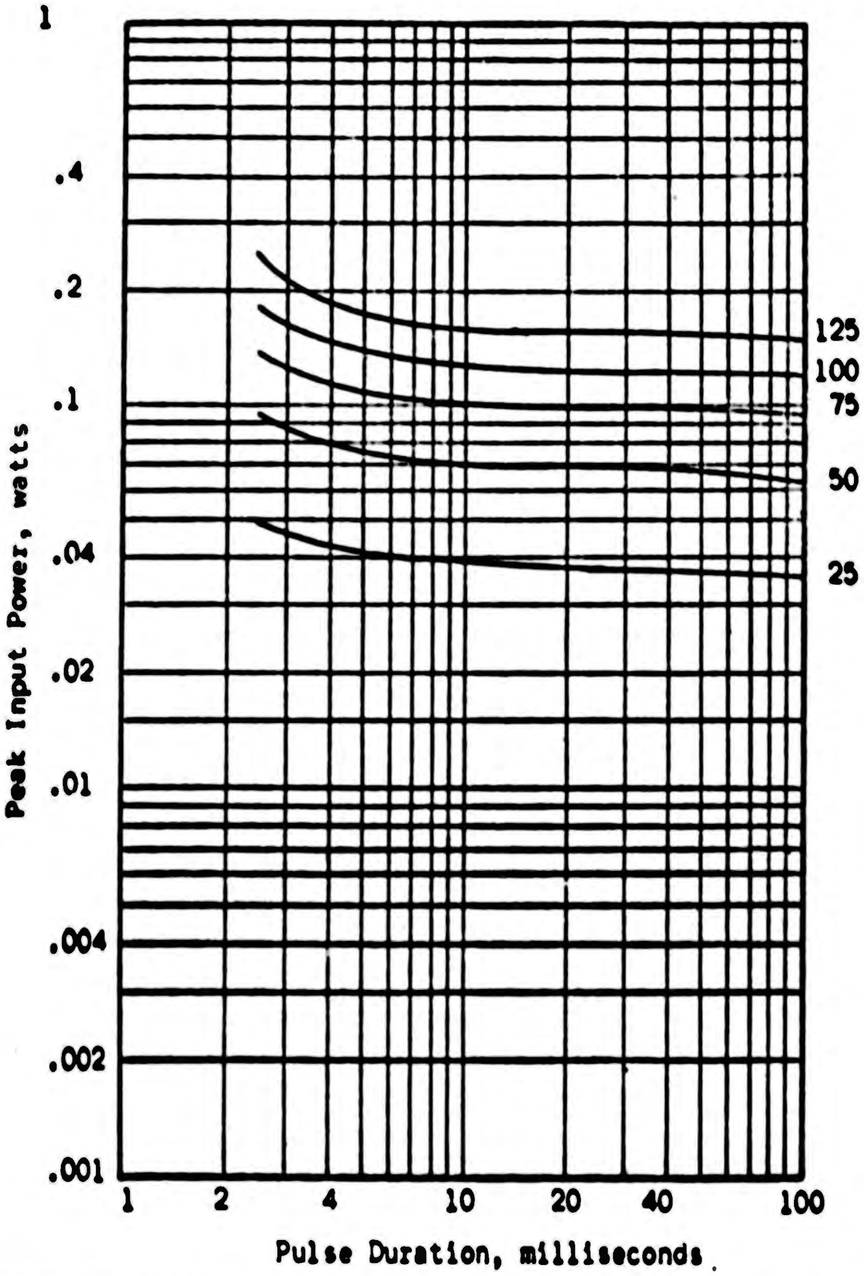


FIGURE B48B. 2N335 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse input
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

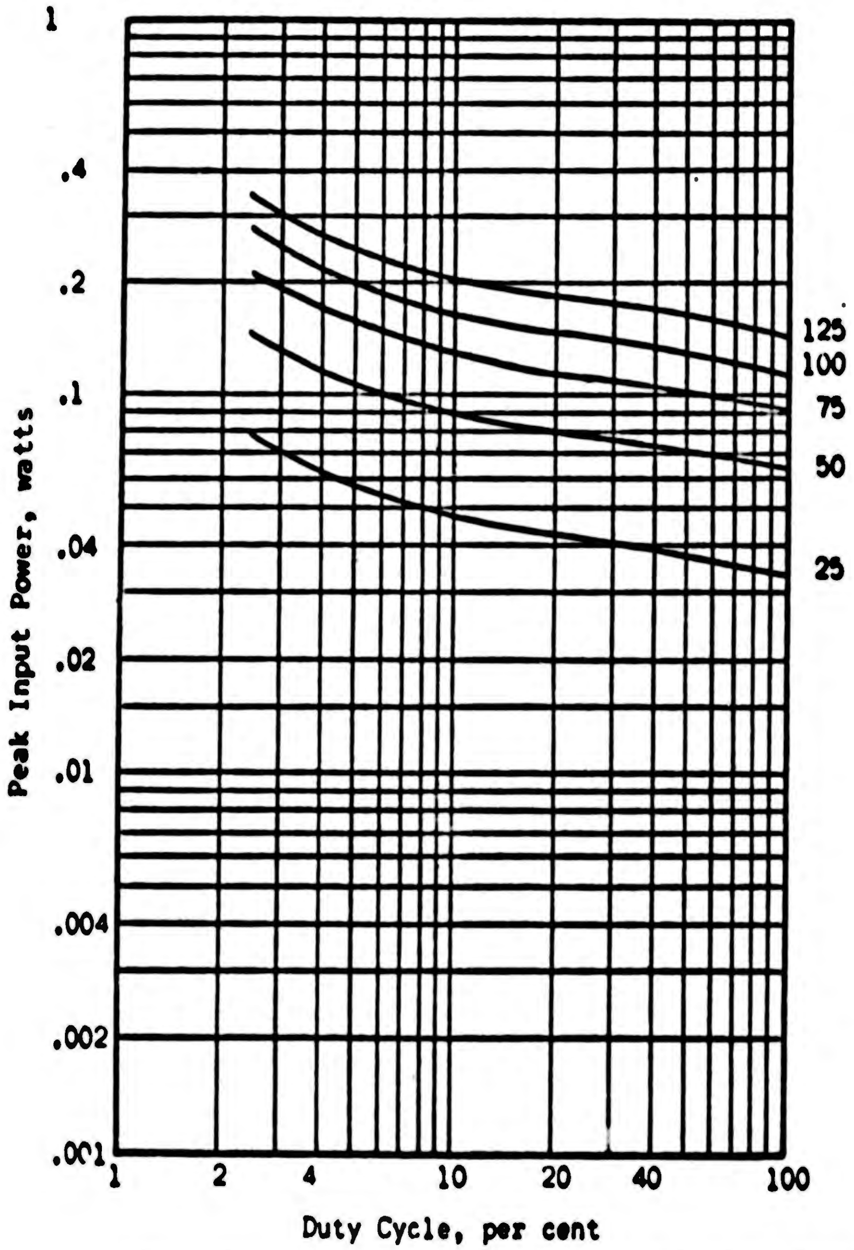


FIGURE B-49. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

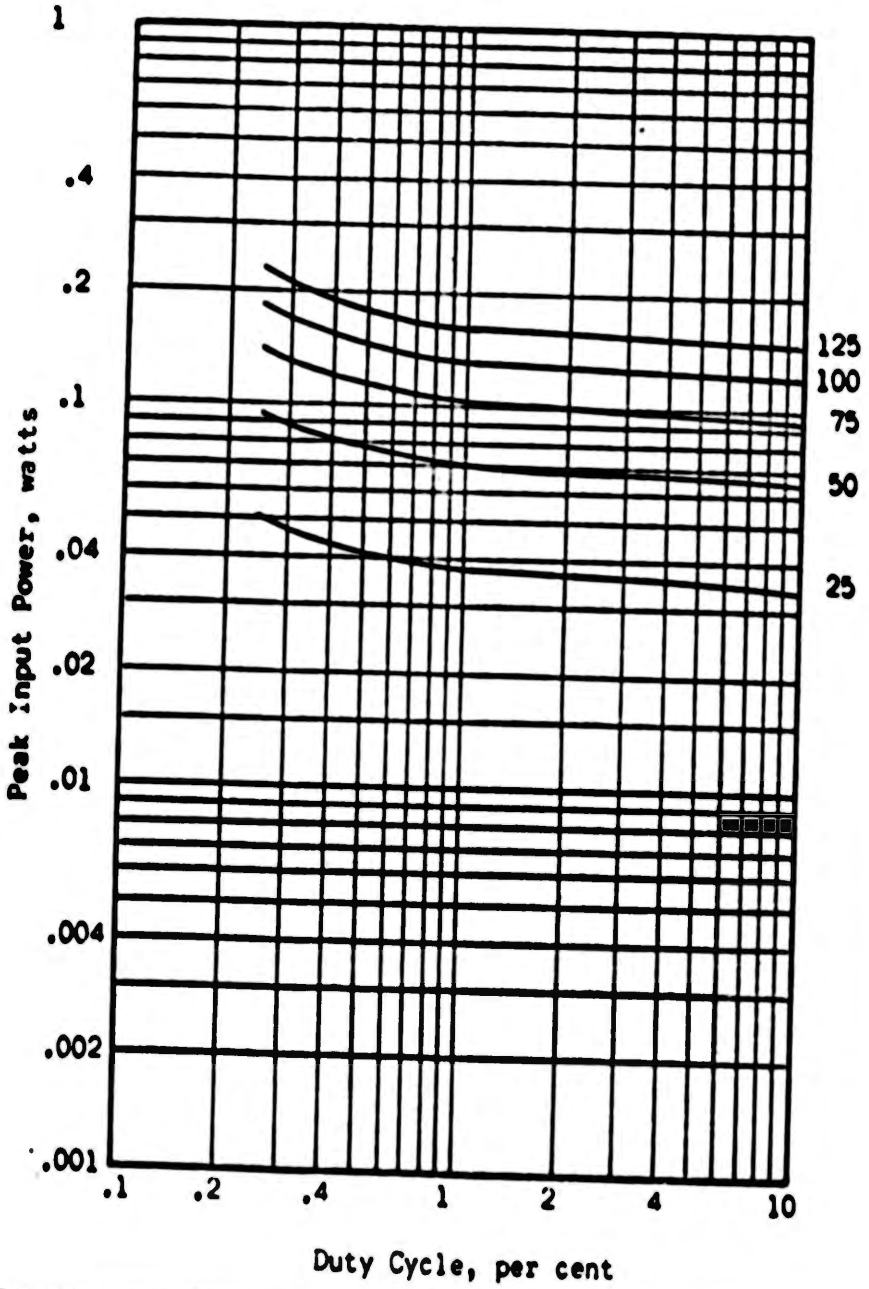


FIGURE B-50A.2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

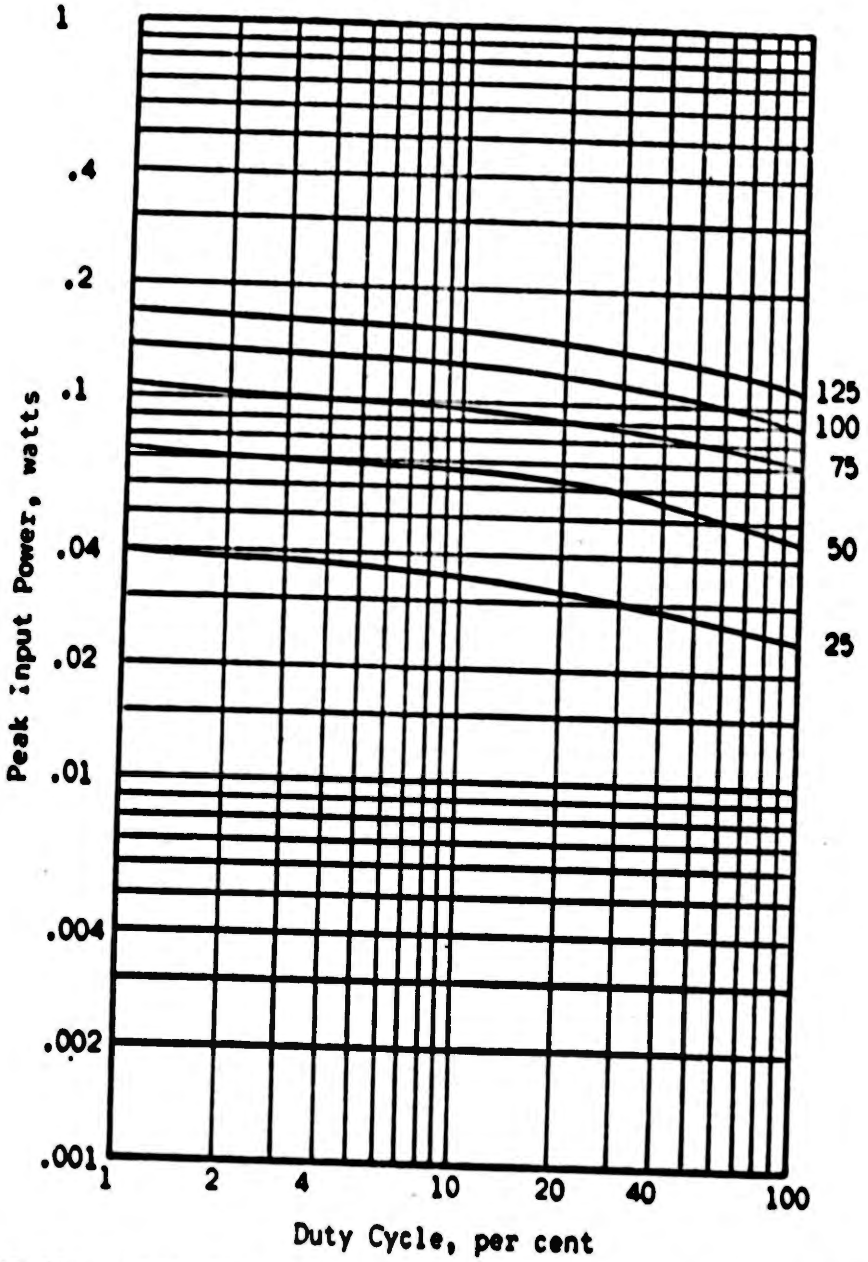


FIGURE B-50B. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

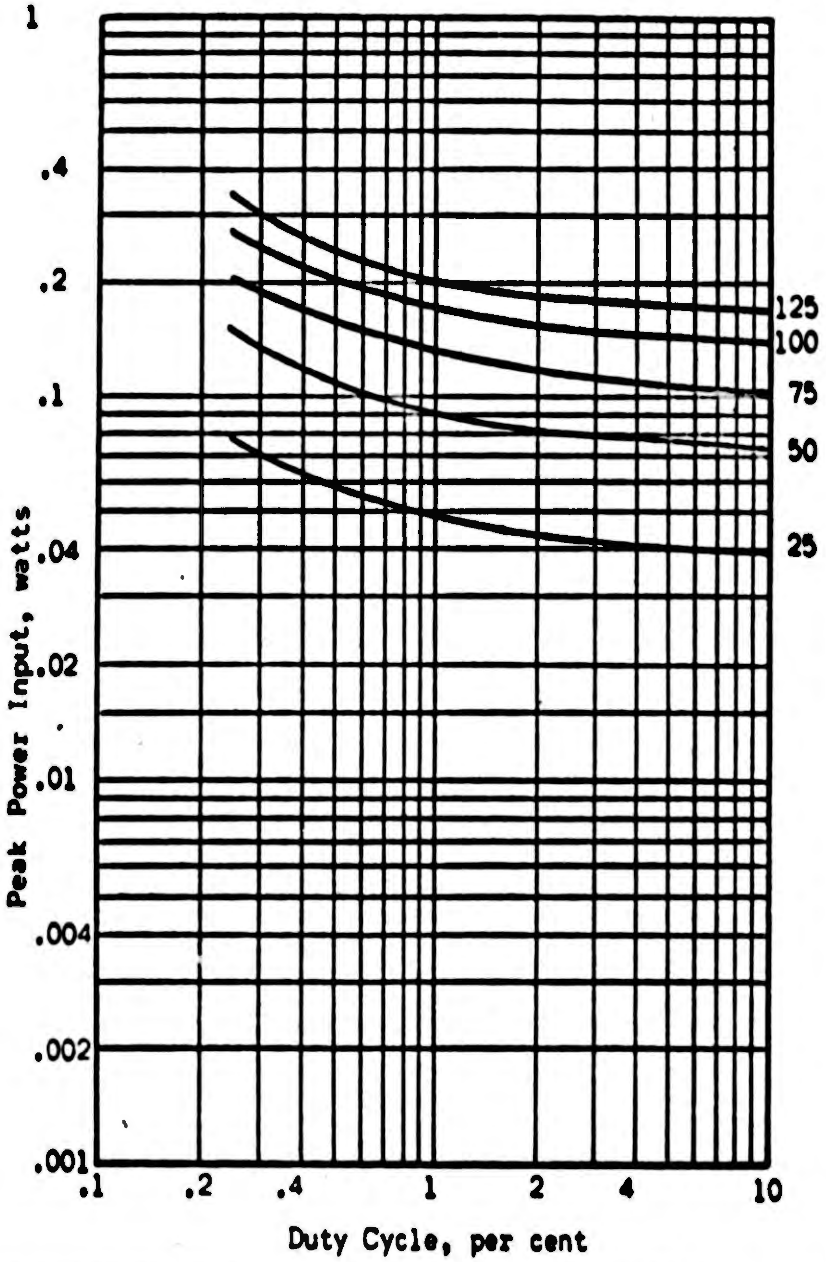


FIGURE B-51A. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

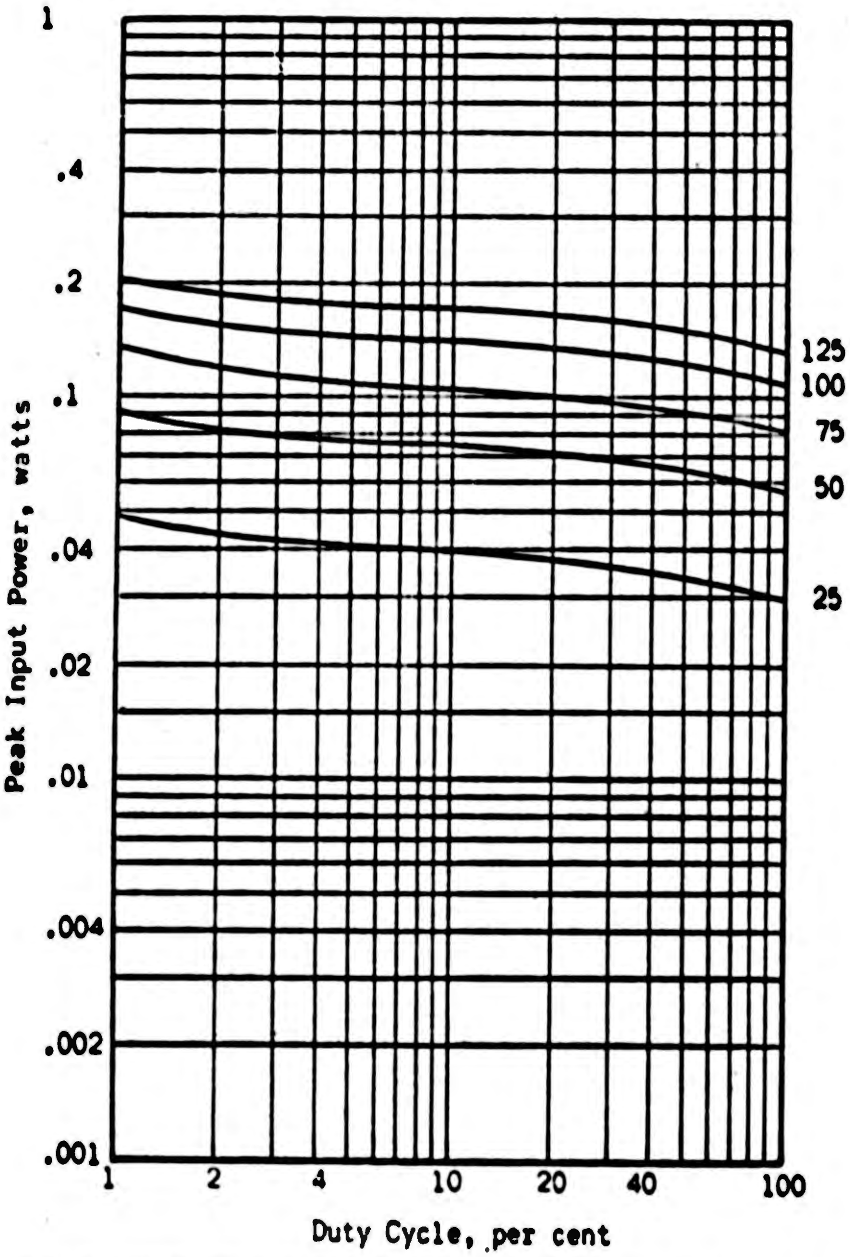


FIGURE B-51B. 2N335 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

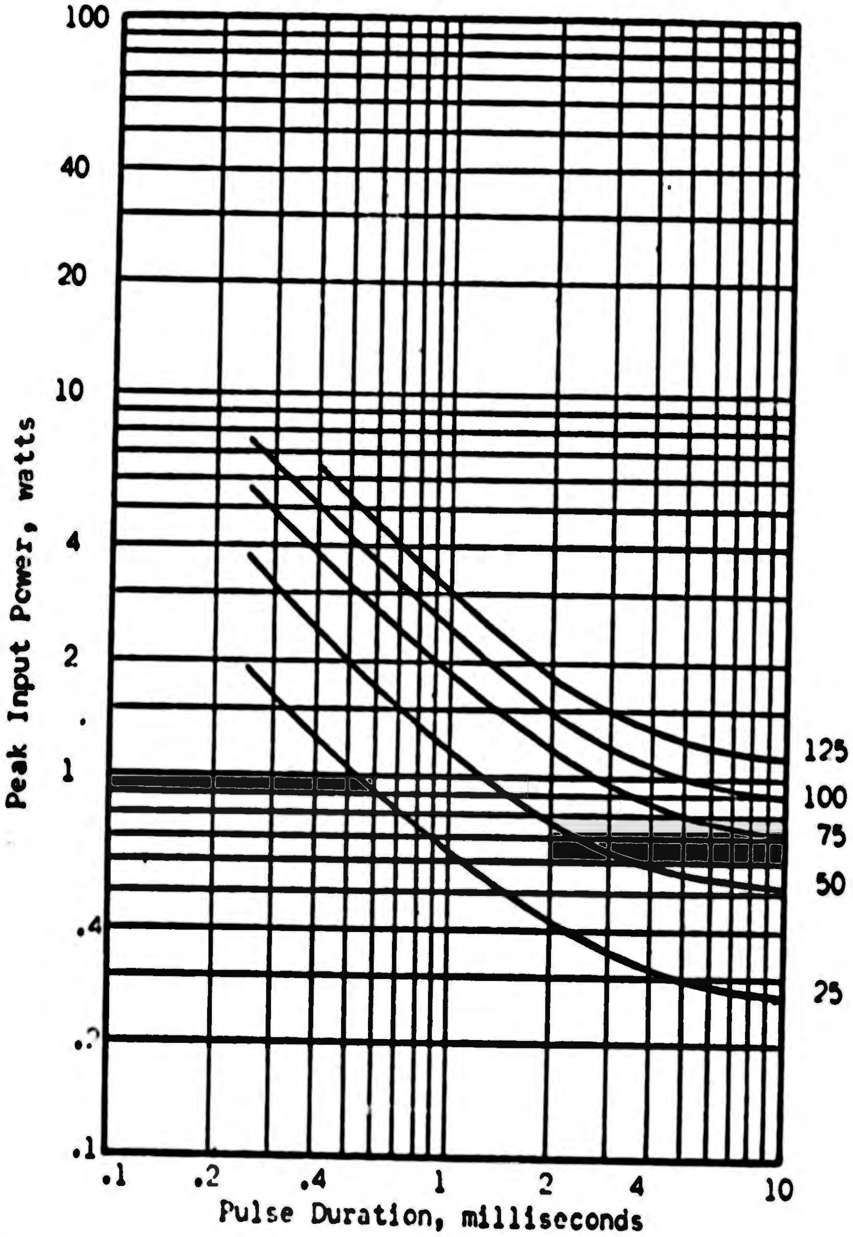


FIGURE B-52A. 2N341 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

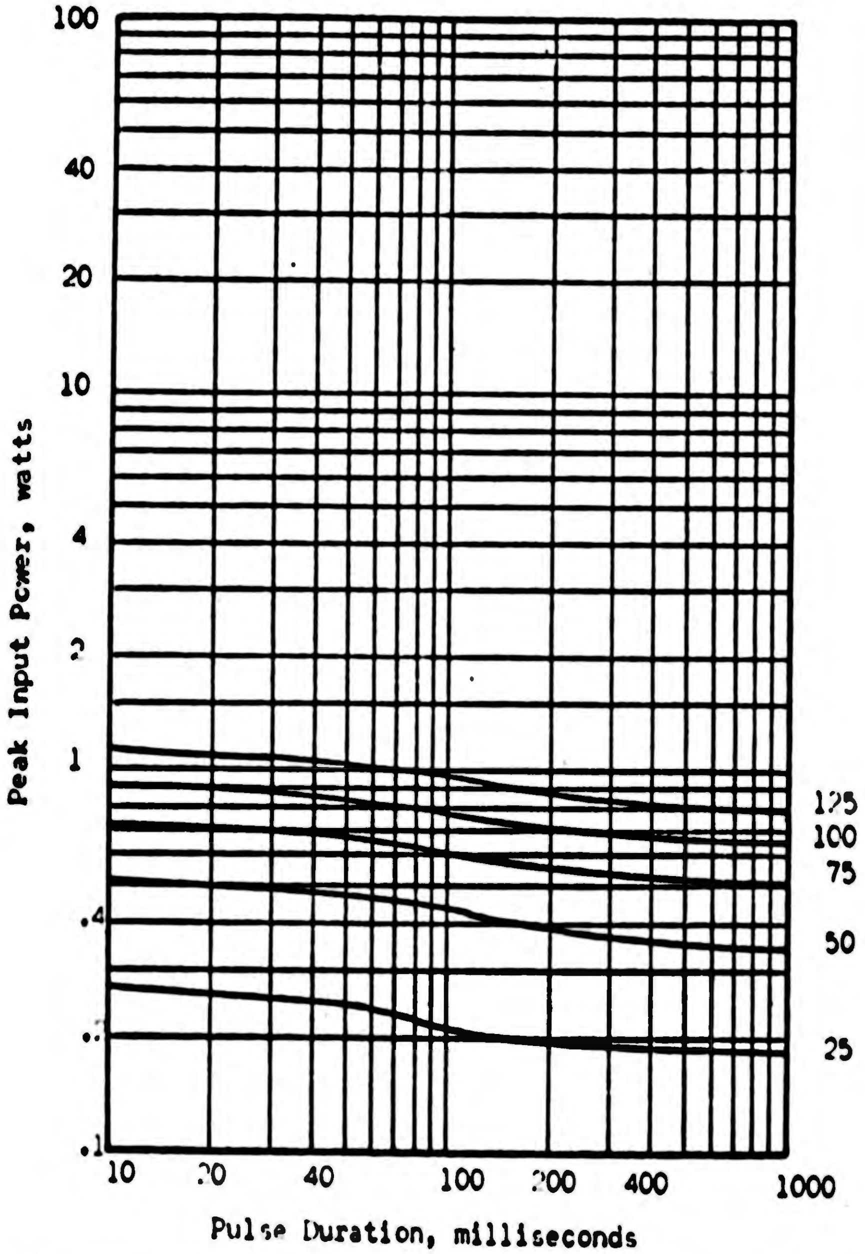


FIGURE B-52B. 2N341 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

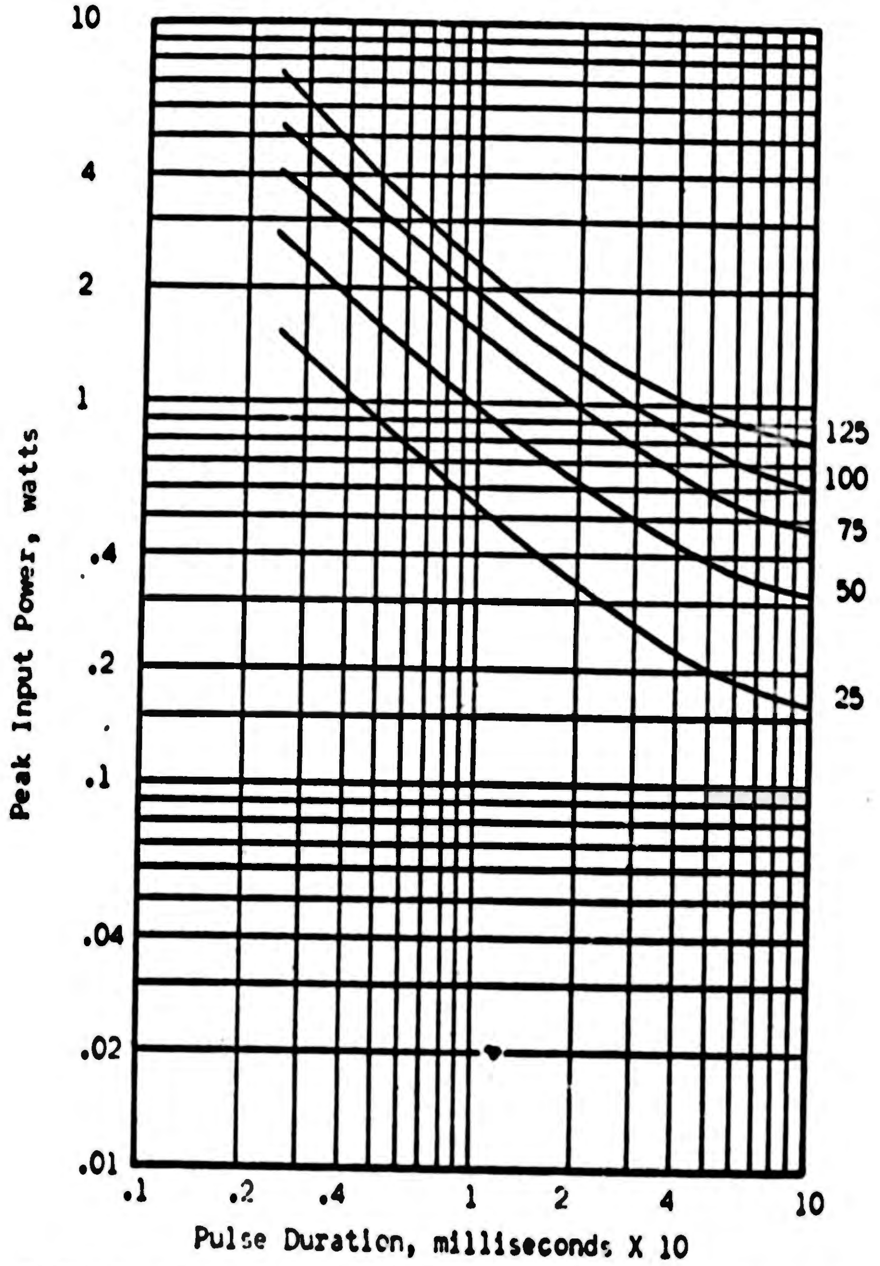


FIGURE B-33A. 2N341 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

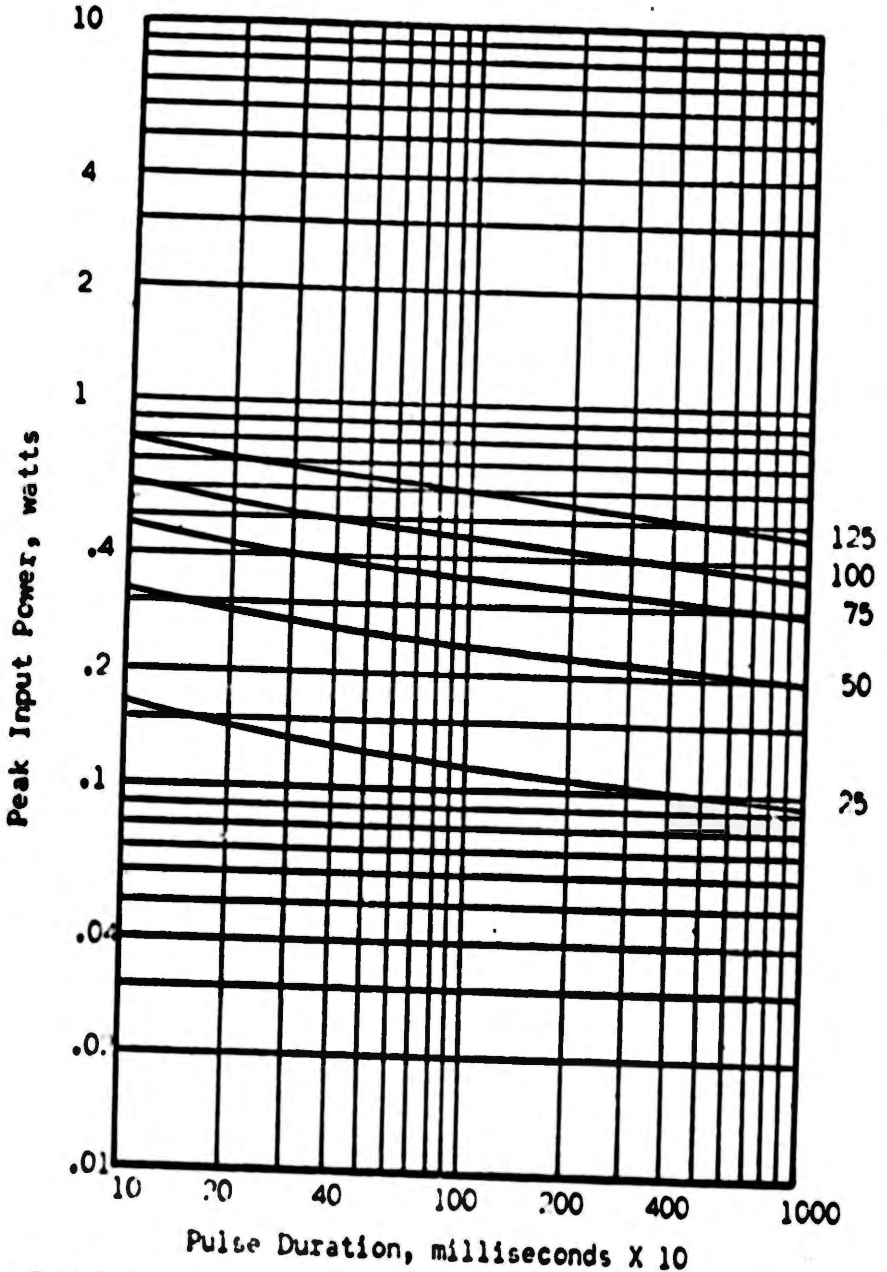


FIGURE B-53 2N341 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

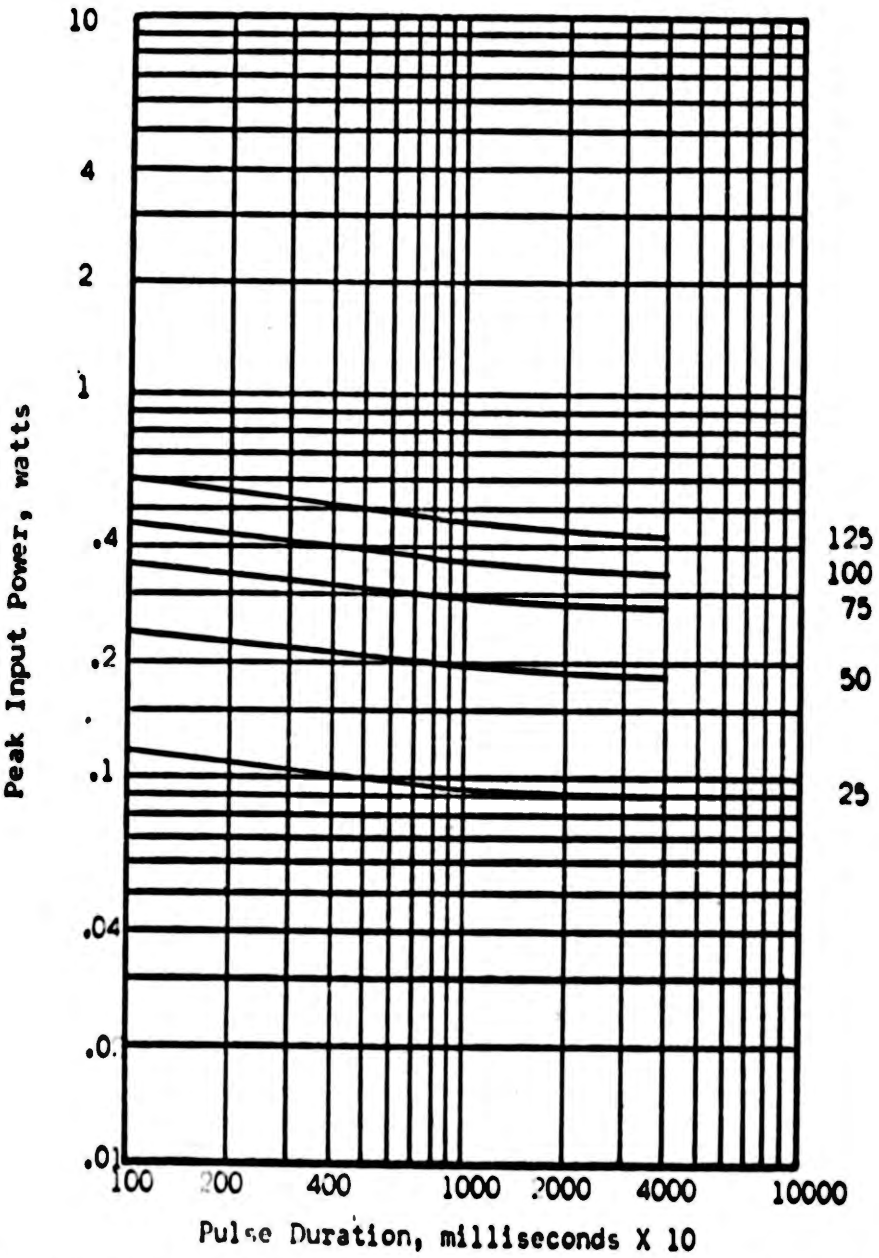


FIGURE B-53C. 2N341 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Saw tooth wave input
Single pulse
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

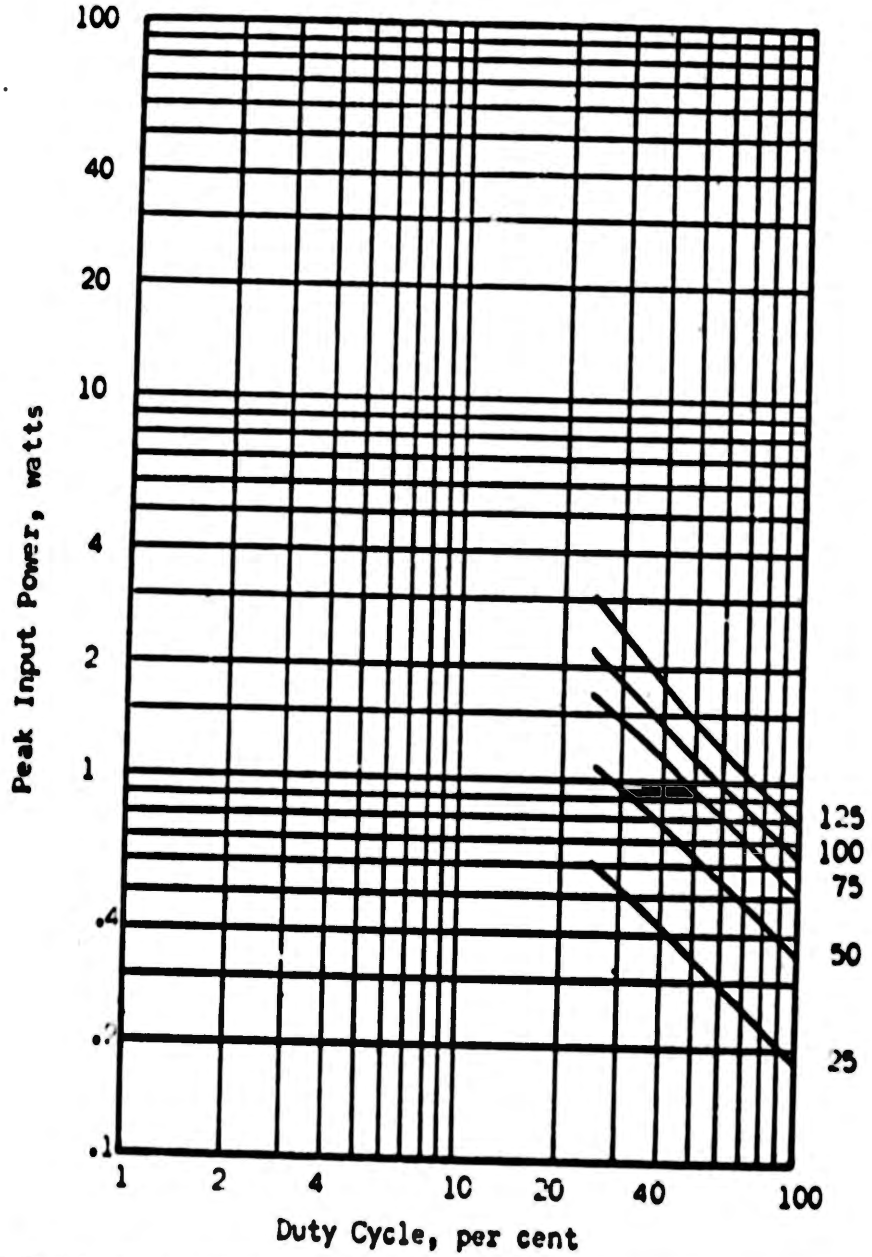


FIGURE B-54. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

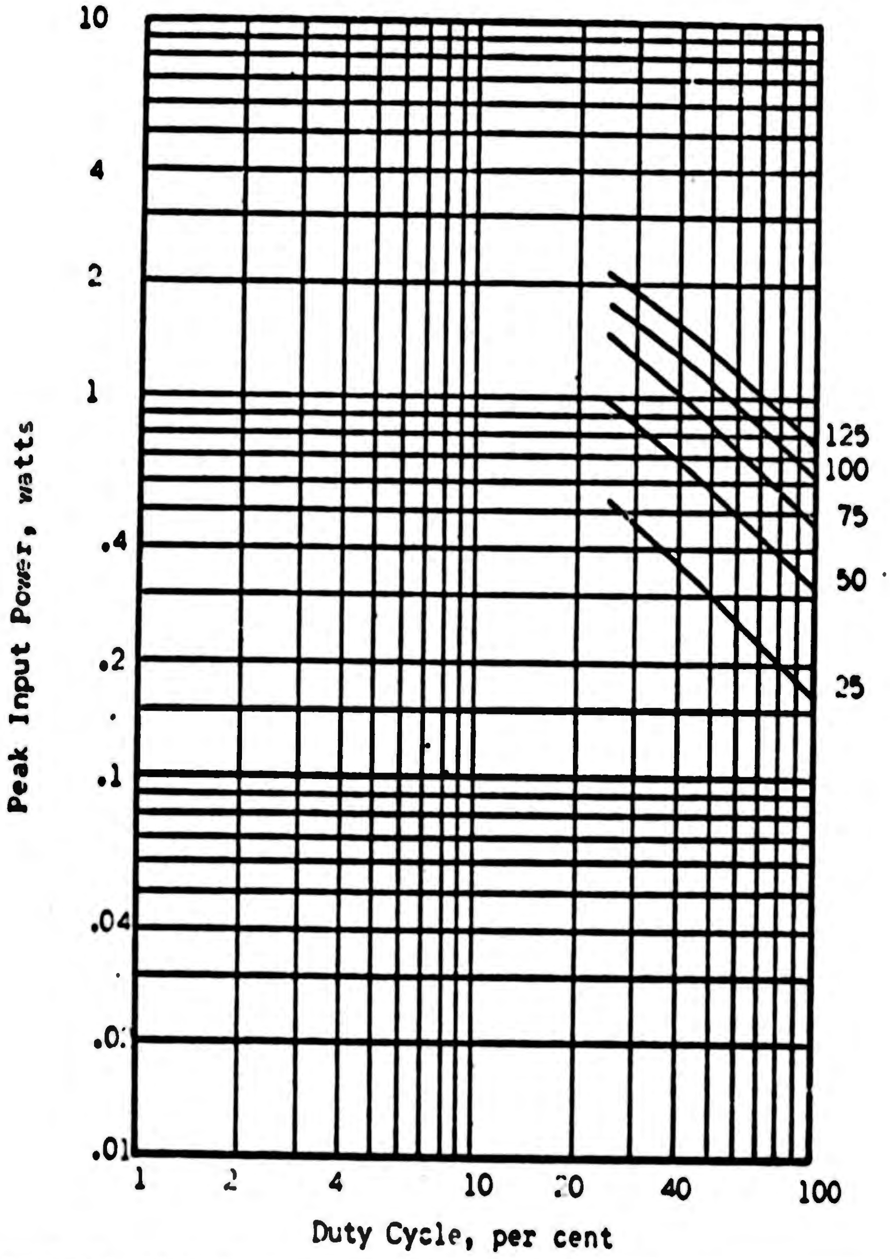


FIGURE B-55. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 10 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

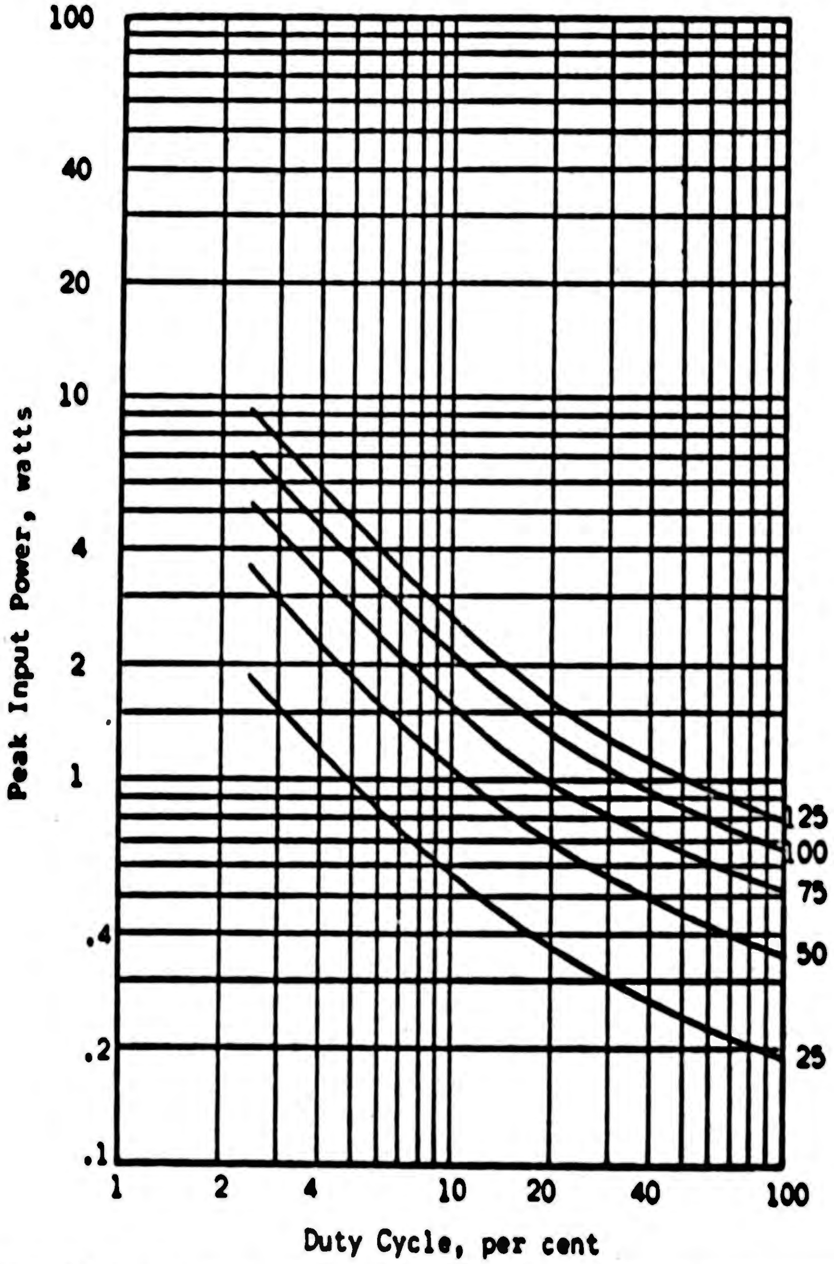


FIGURE B-56.2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

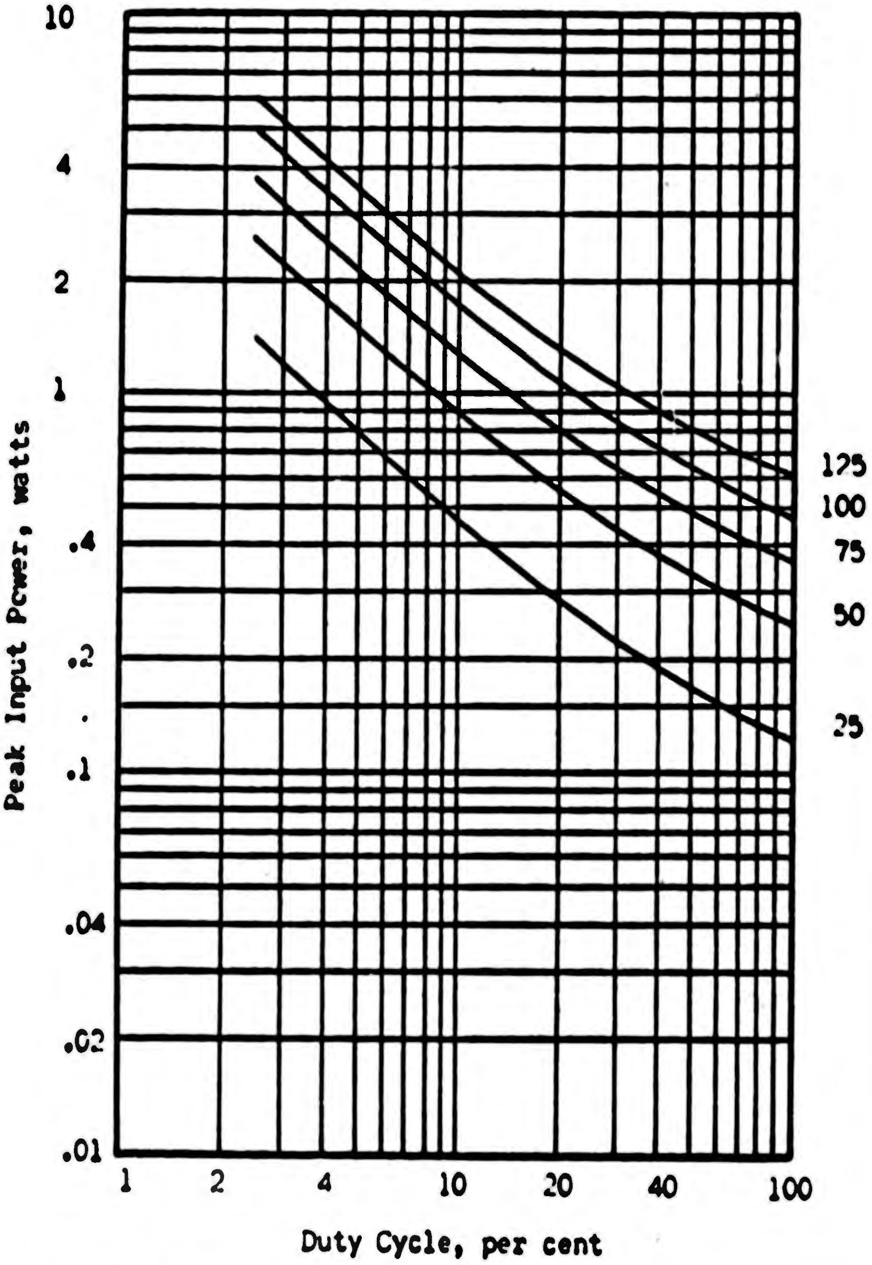


FIGURE B-57. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 100 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

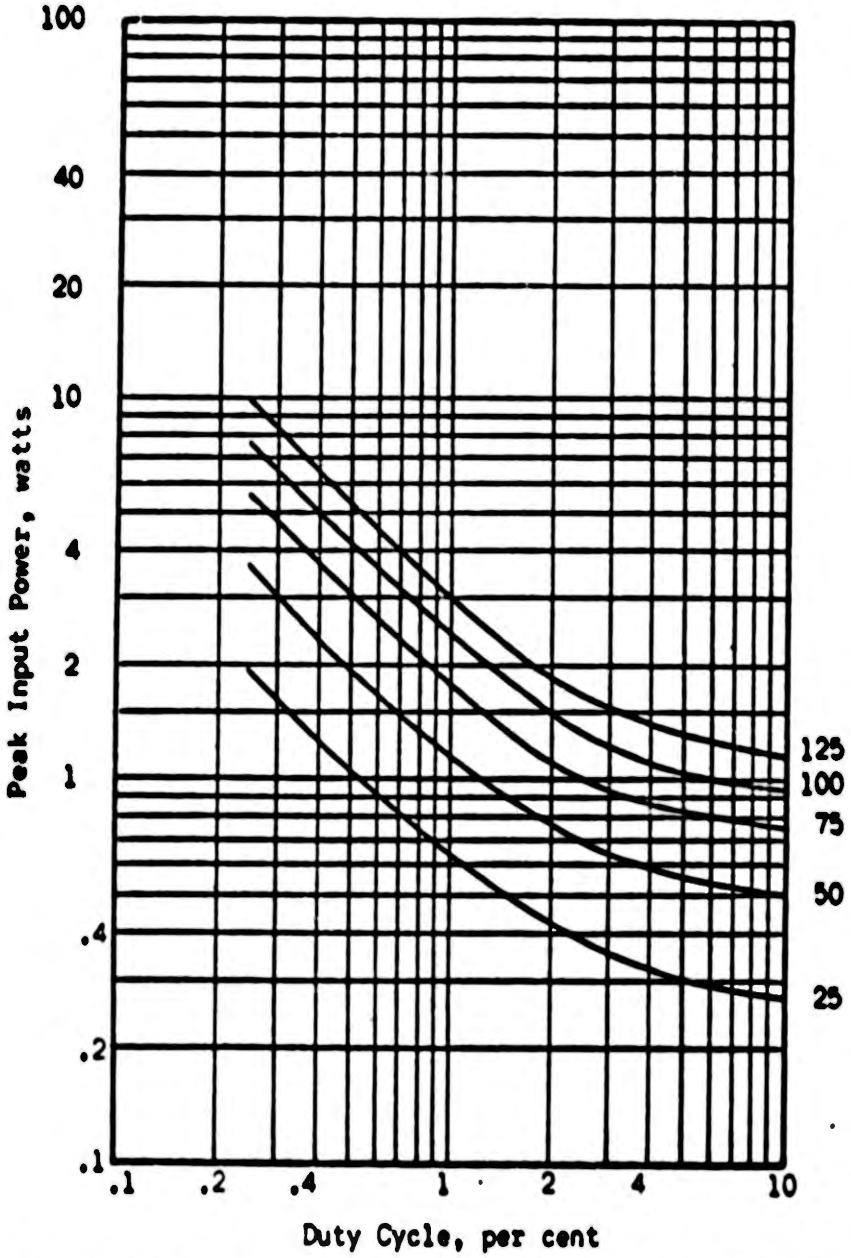


FIGURE B-58A. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125

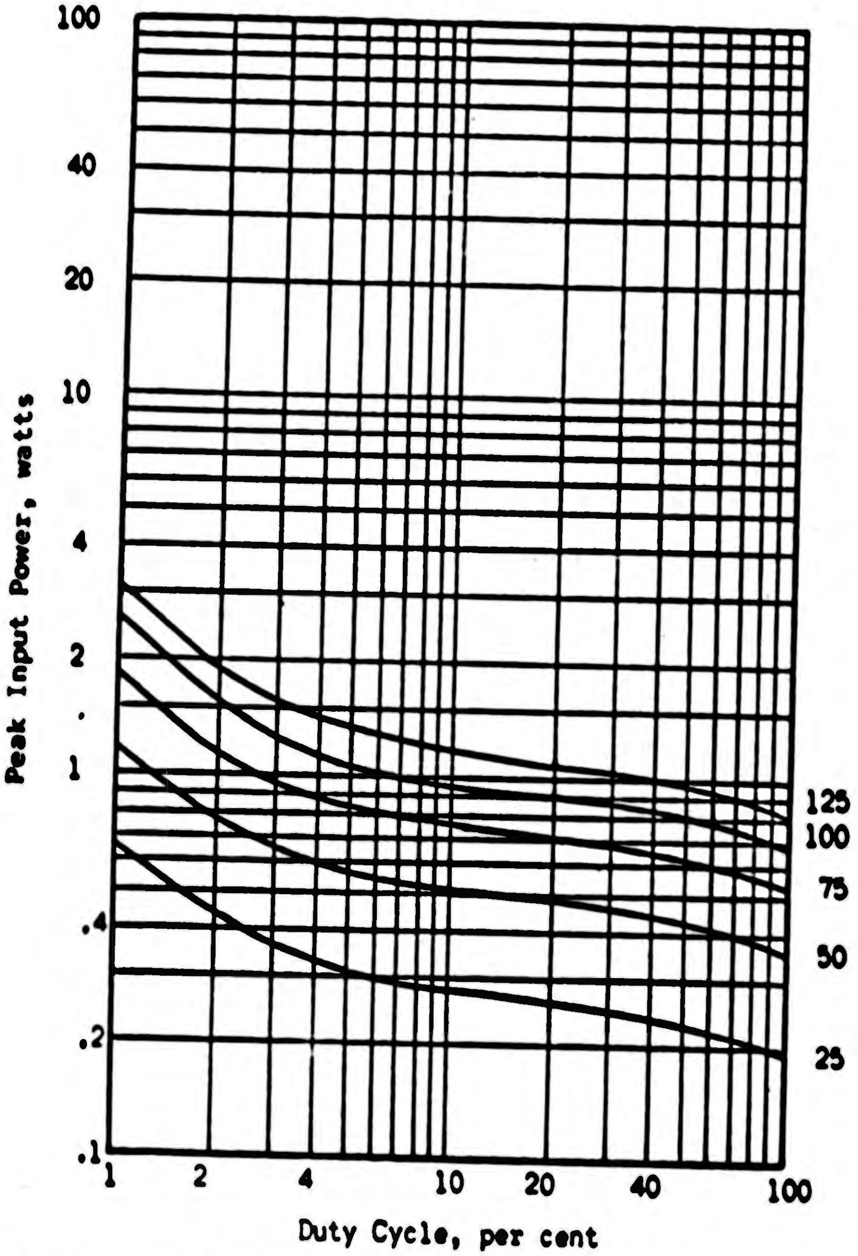


FIGURE B-58B.2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

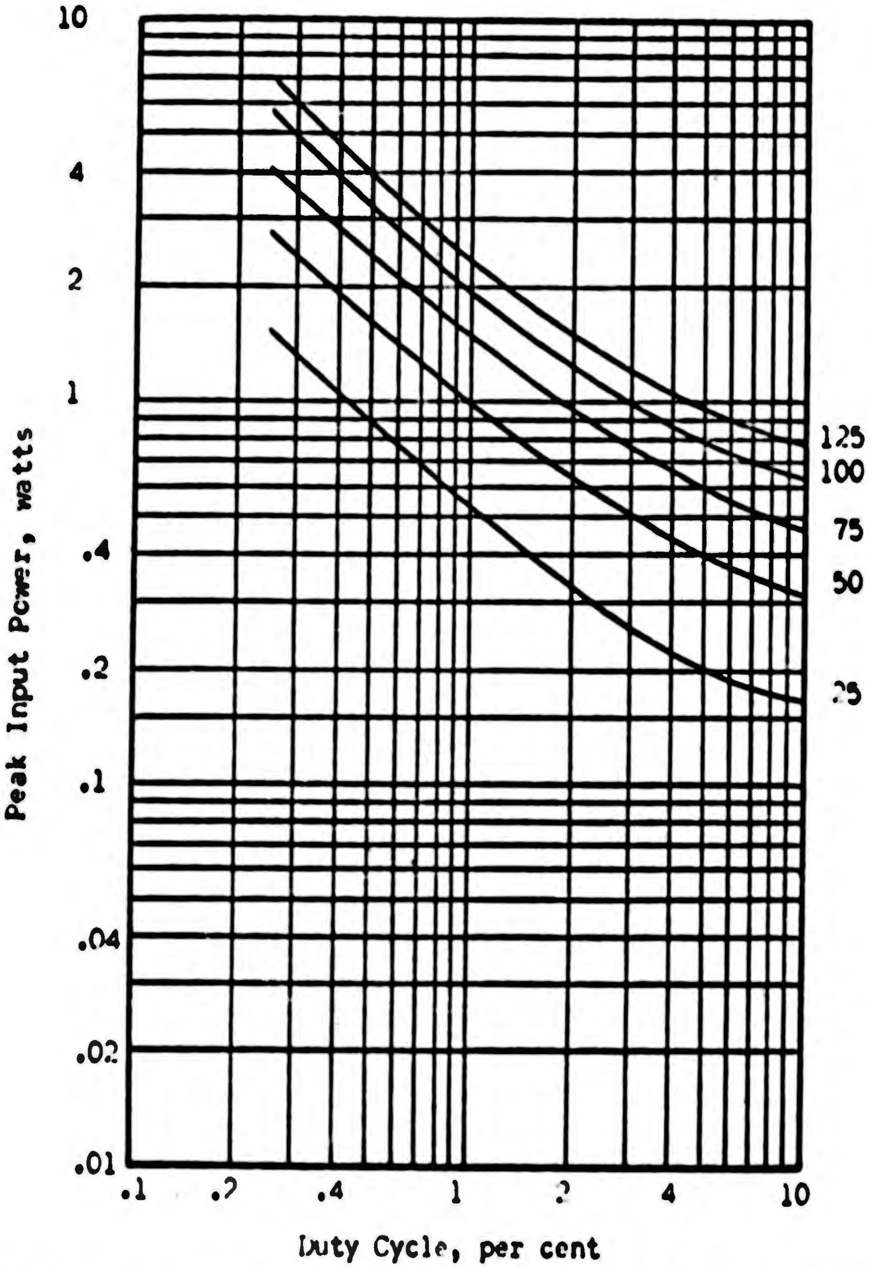


FIGURE B-59A. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

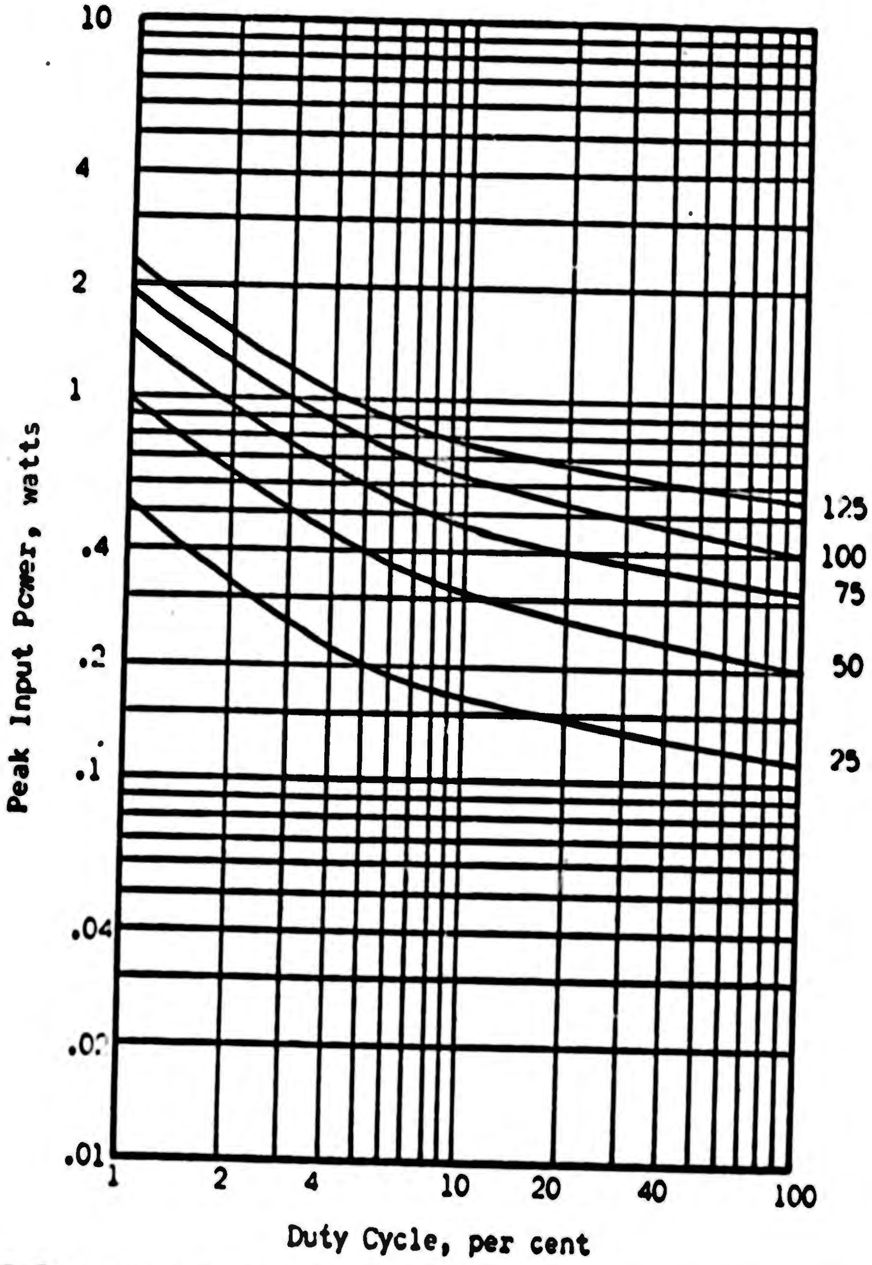


FIGURE B-59B. 2N341 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Saw tooth wave input
Repetition period = 1000 milliseconds
Ambient temperature < 125 C
Stability factor < 100
Temperature rise = 25, 50, 75, 100, and 125 C

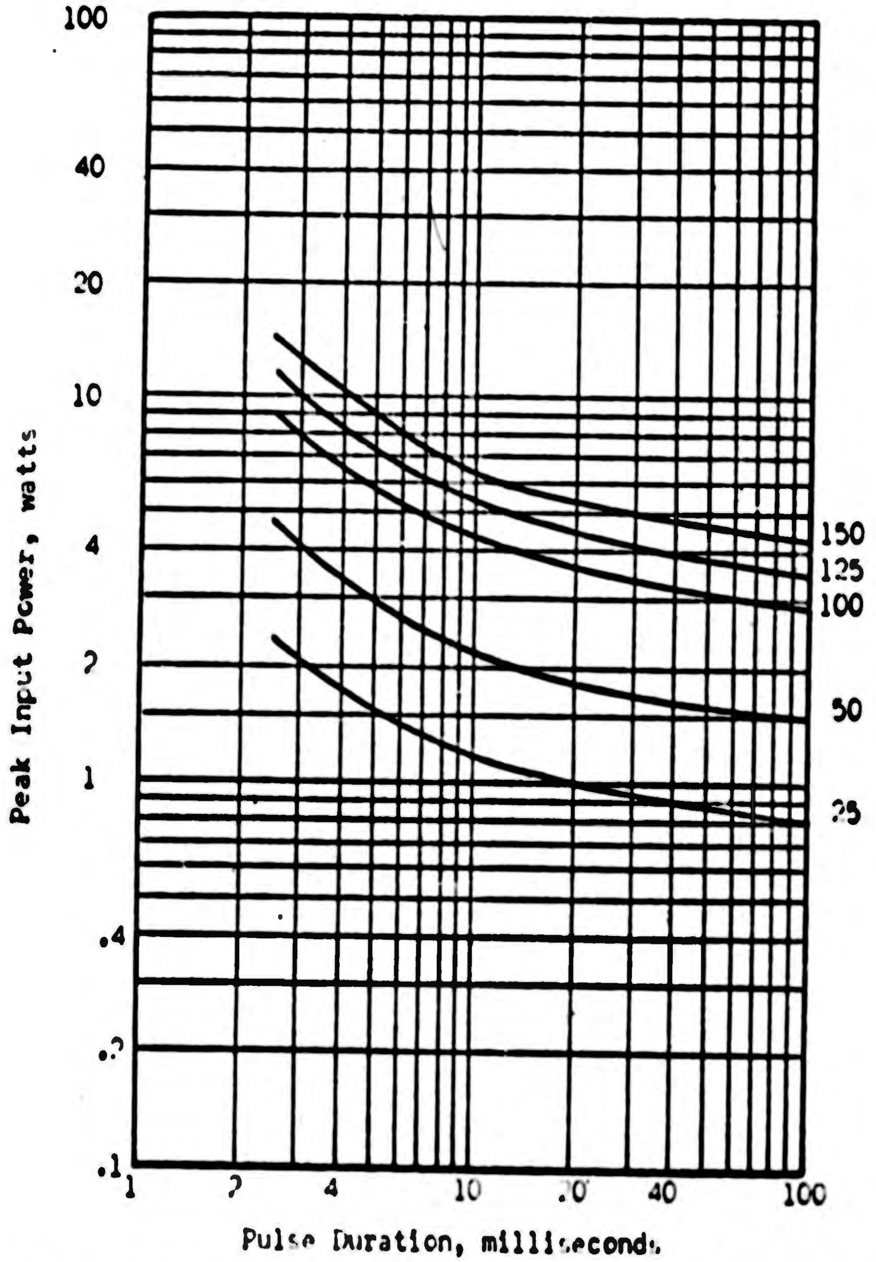


FIGURE B-60A. 2N697 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

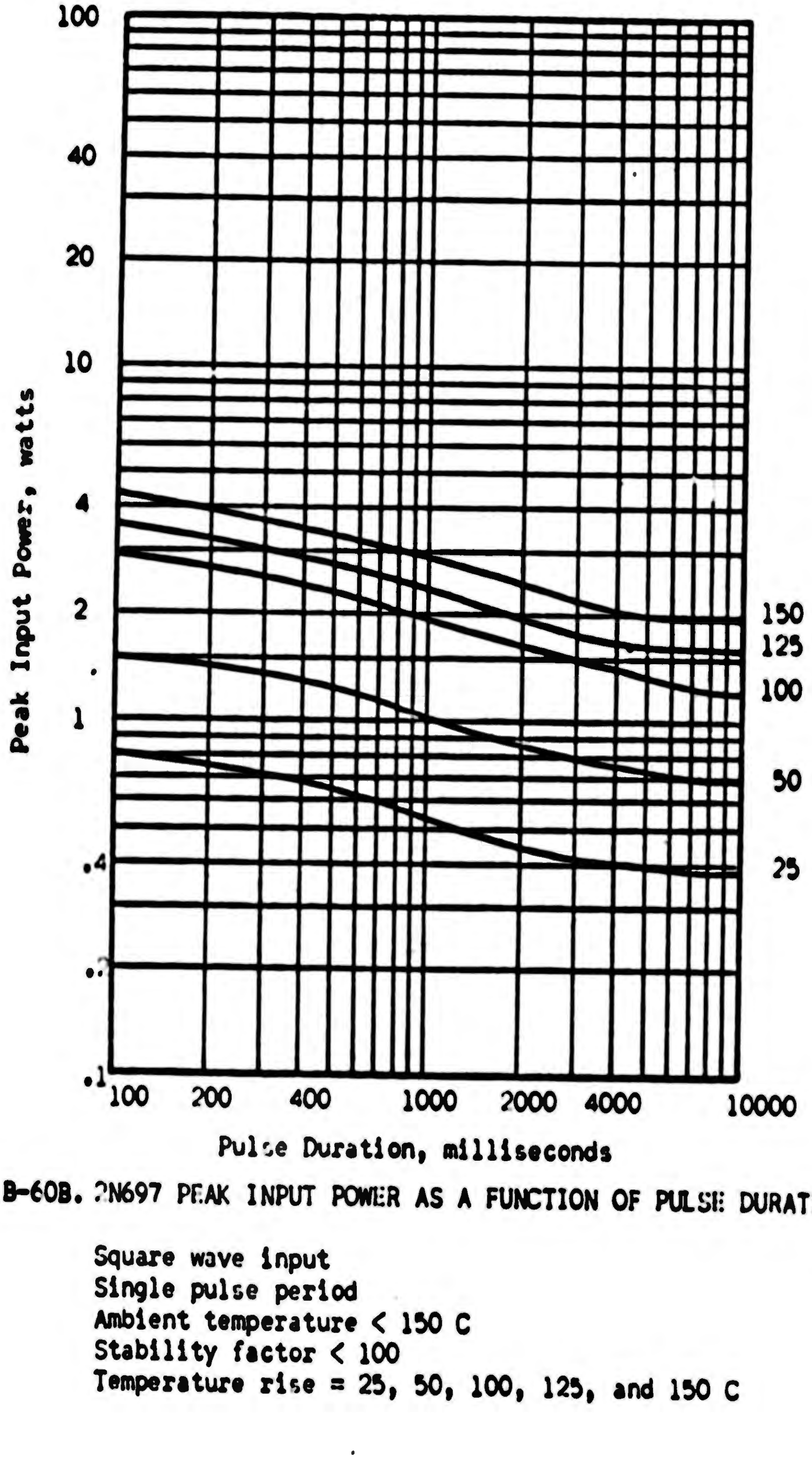


FIGURE B-60B. 2N697 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

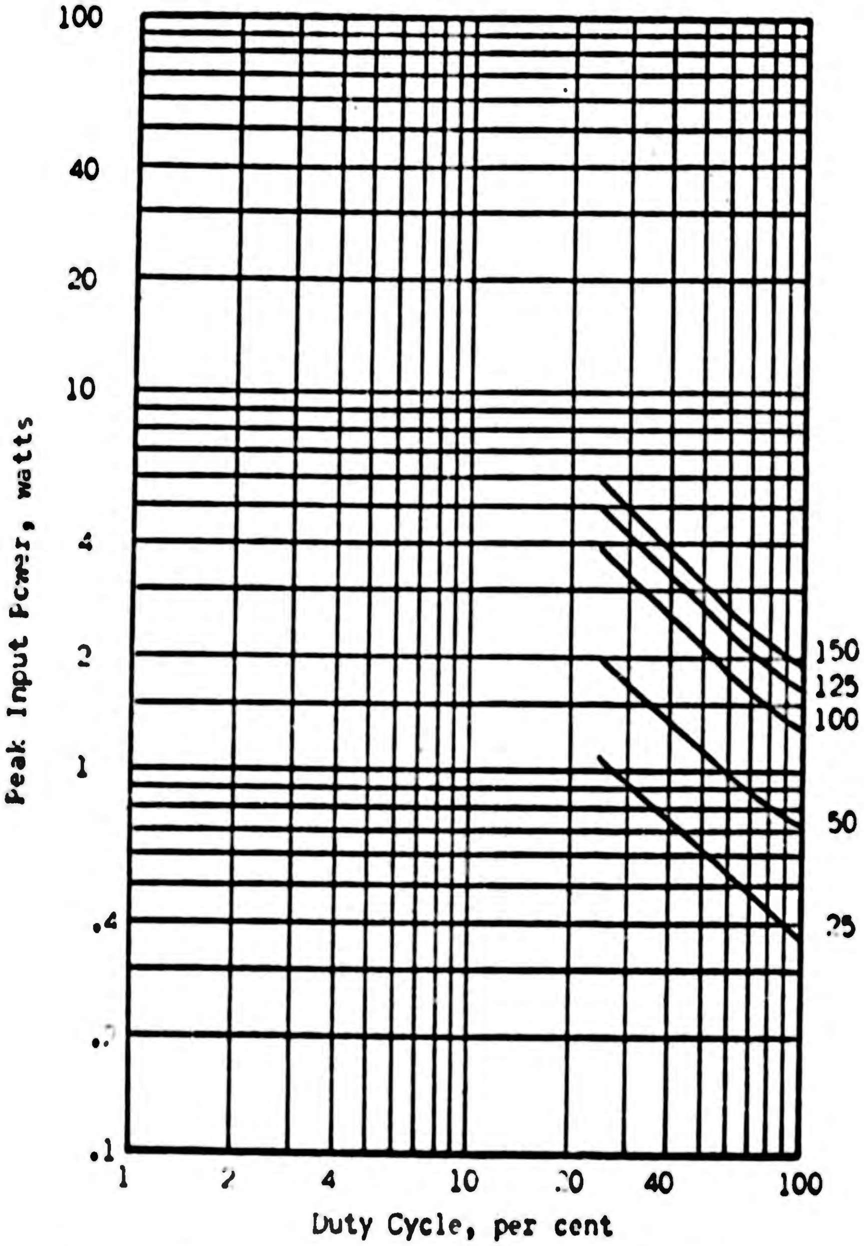


FIGURE B-61. 2N697 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

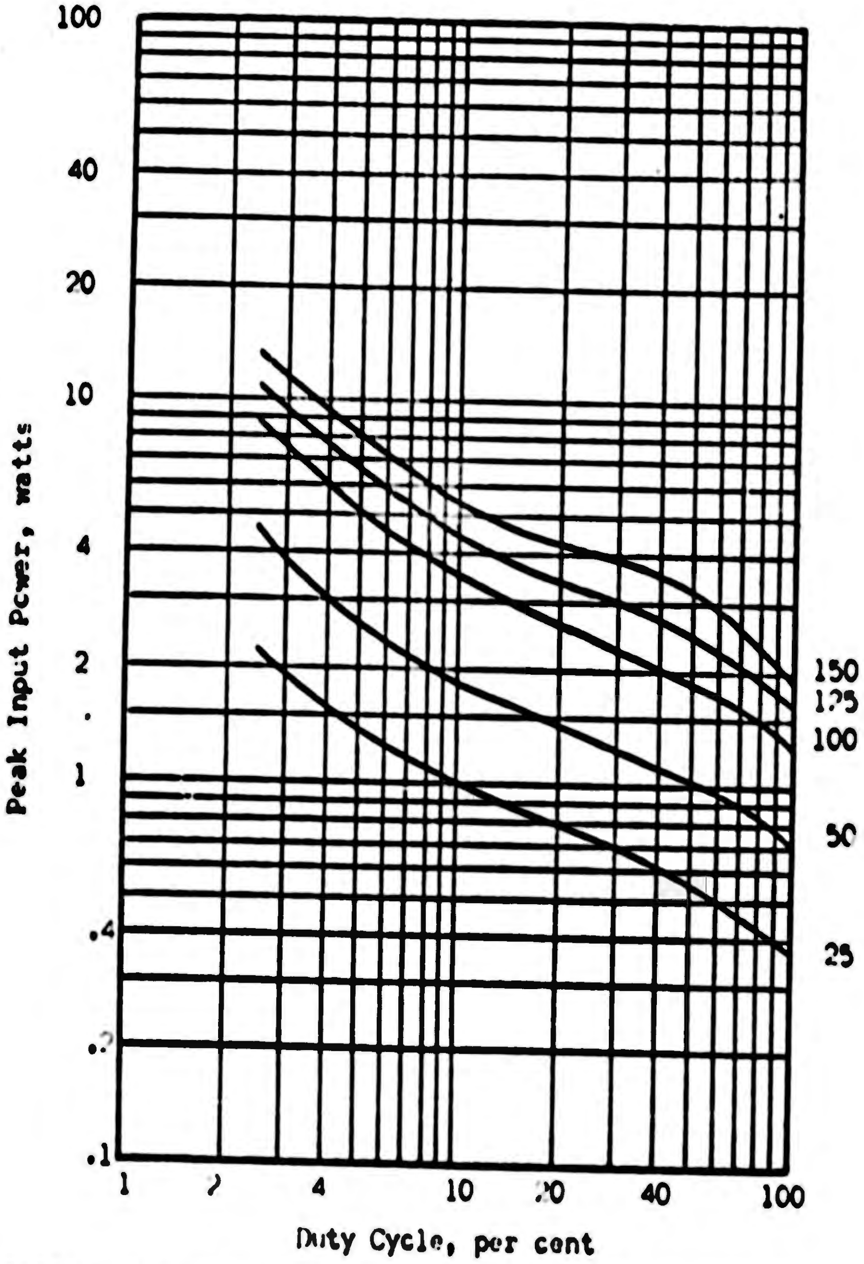


FIGURE B-62. 2N697 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

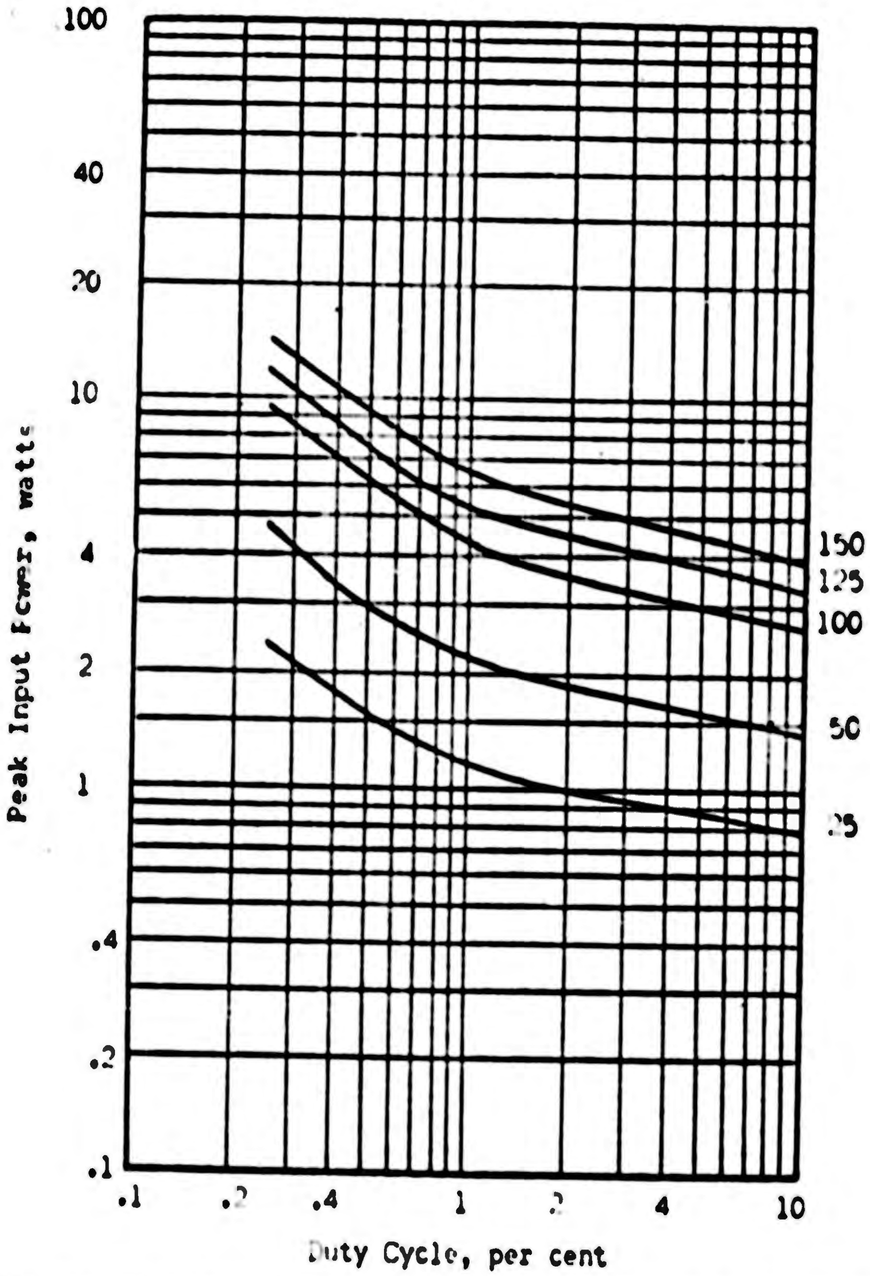


FIGURE B-63A. 2N697 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

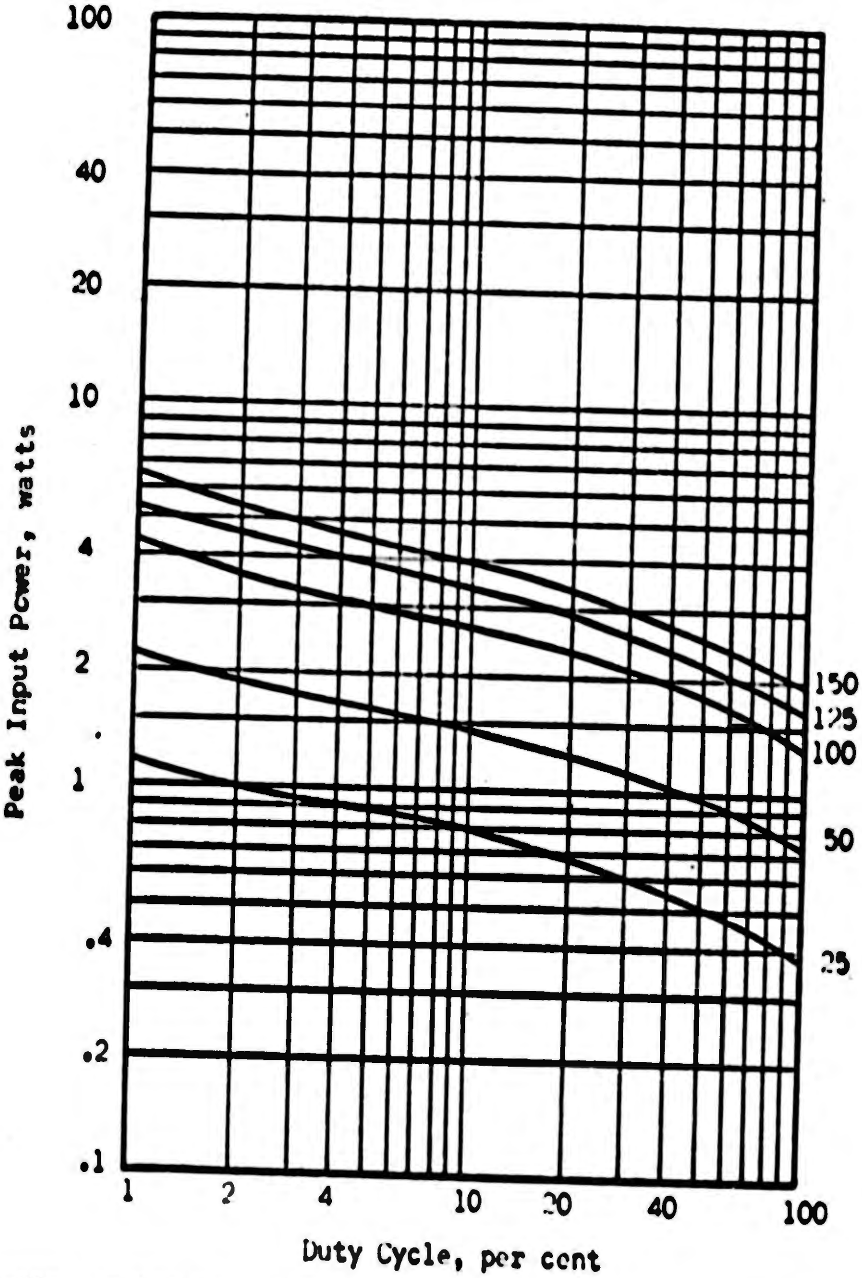


FIGURE B-63B. 2N697 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Ambient temperature < 150 C
Stability factor < 100
Temperature rise = 25, 50, 100, 125, and 150 C

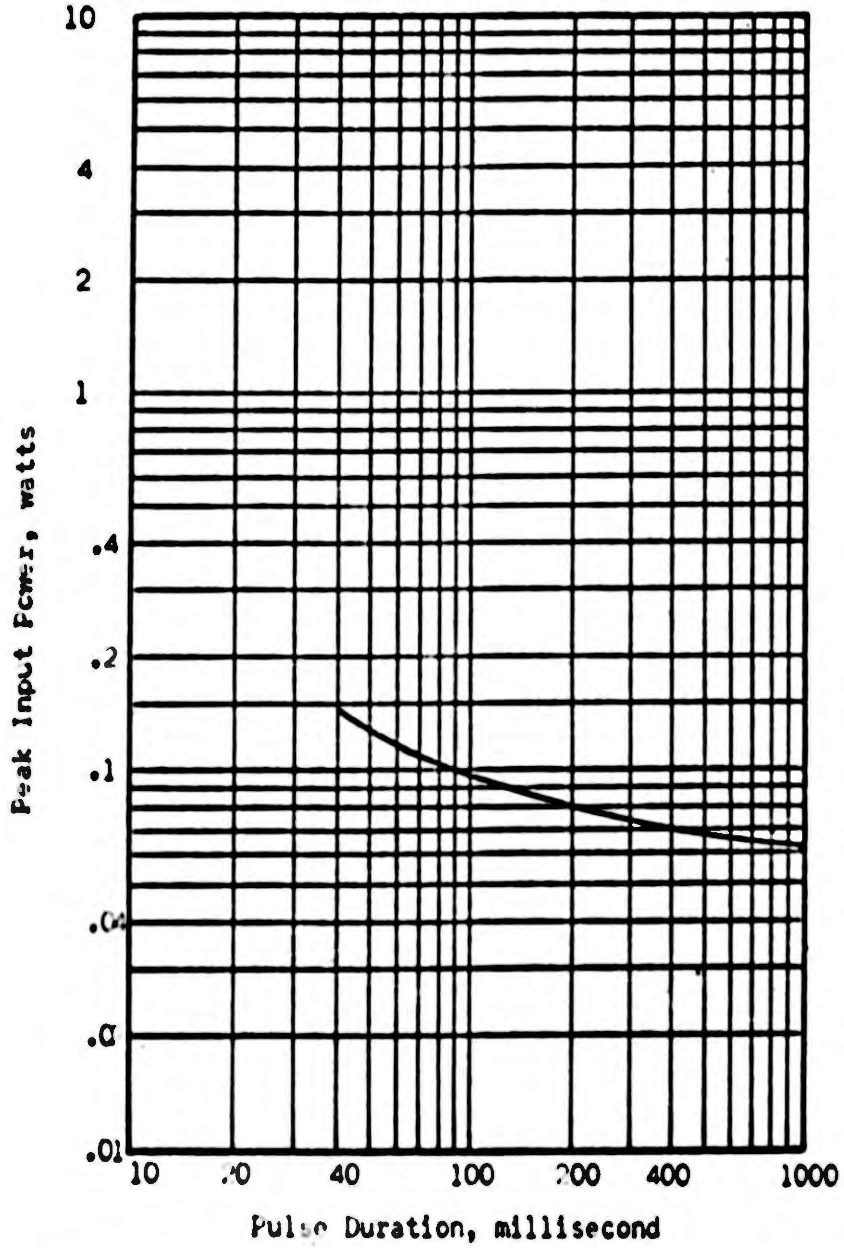


FIGURE B-64A. 2N502 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Collector voltage = < 20 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = < 100

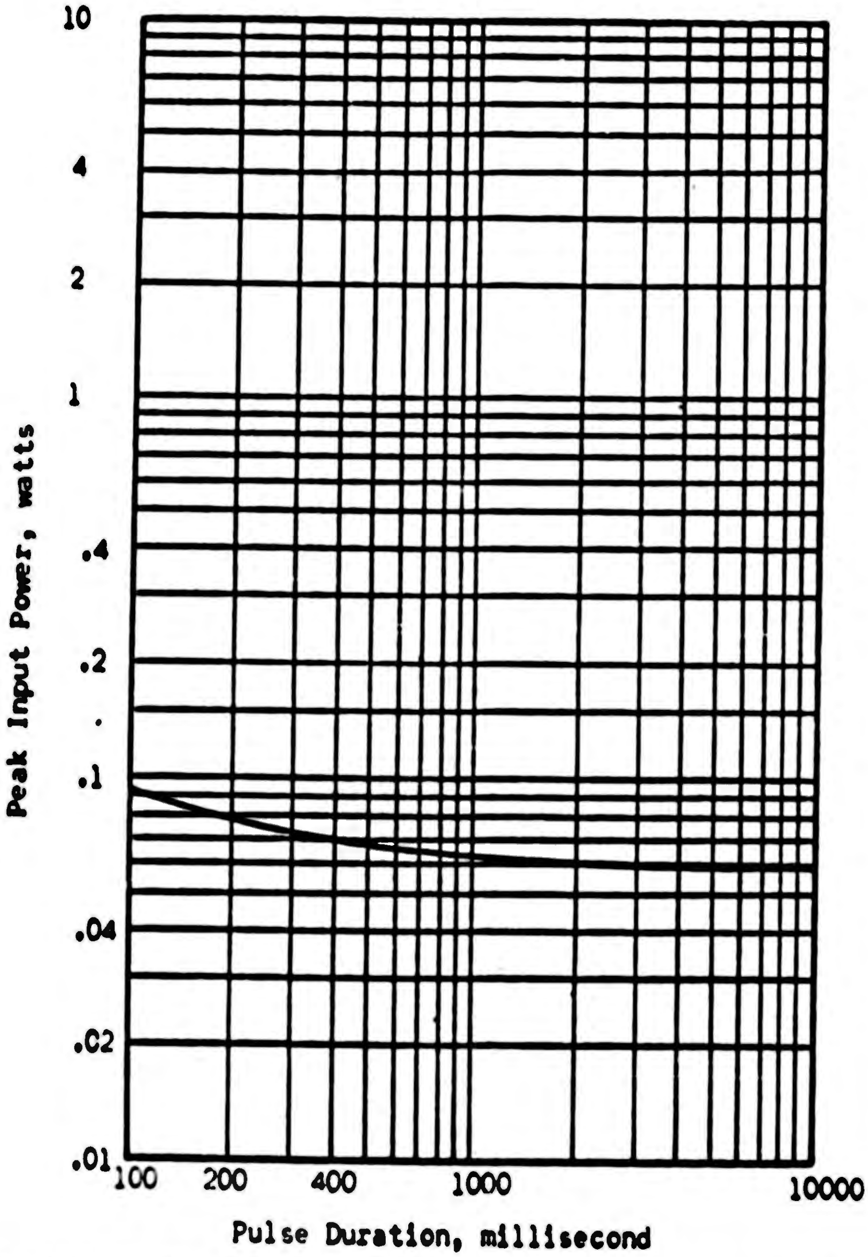


FIGURE B-64B. 2N502 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Collector voltage = < 20 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = < 100

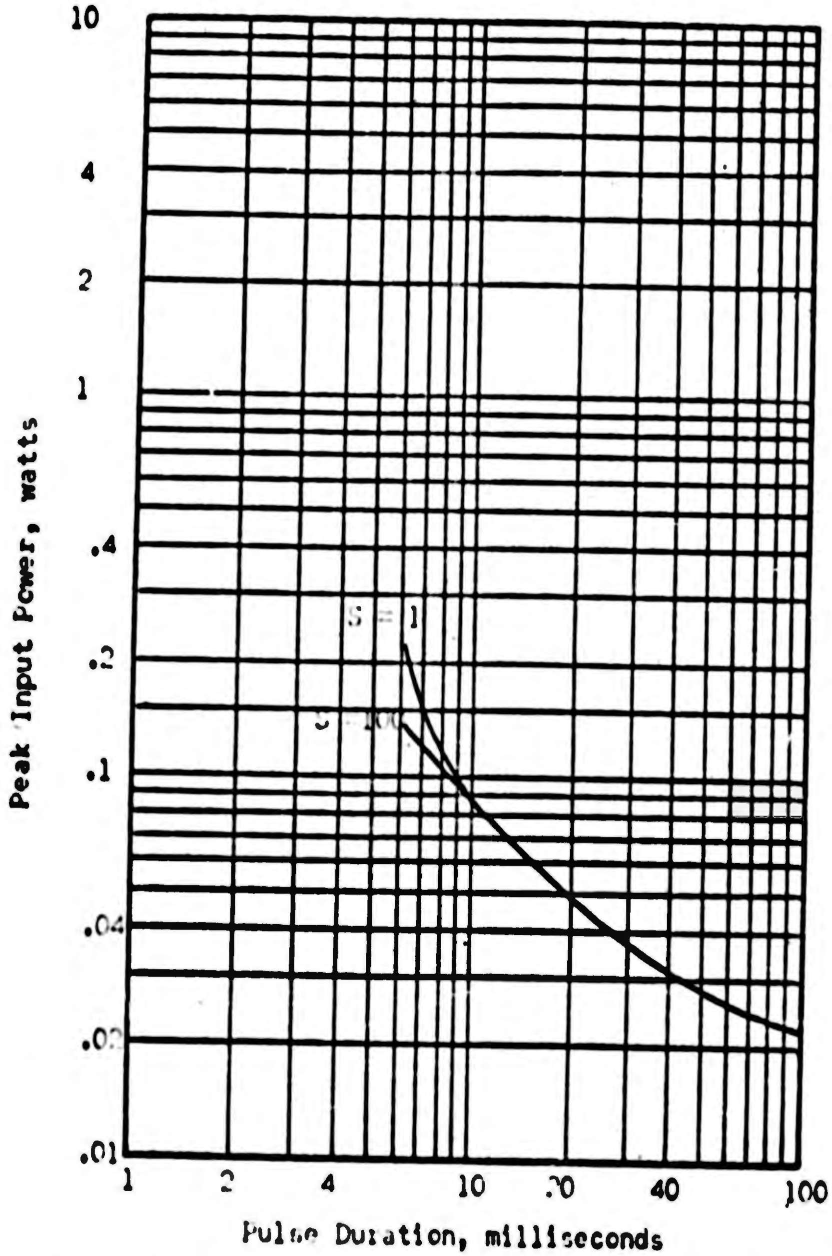


FIGURE B-65A. 2N502 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Collector voltage = 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
S = 100 curve correct for V_c = 20 and 10

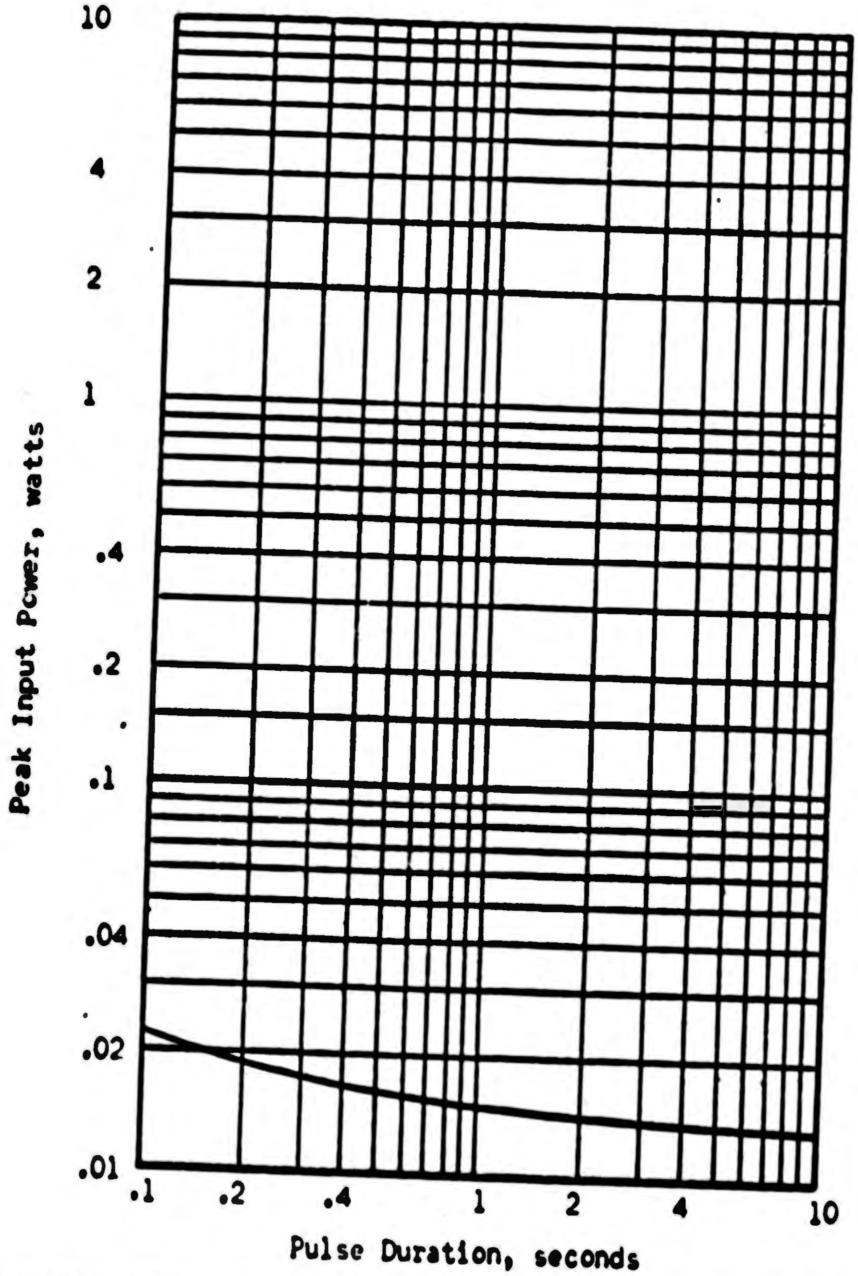


FIGURE B-65B. 2N502 PEAK INPUT POWER AS A FUNCTION OF PULSE DURATION

Square wave input
Single pulse period
Collector voltage = 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
S = 100 curve correct for V_c = 20 and 10

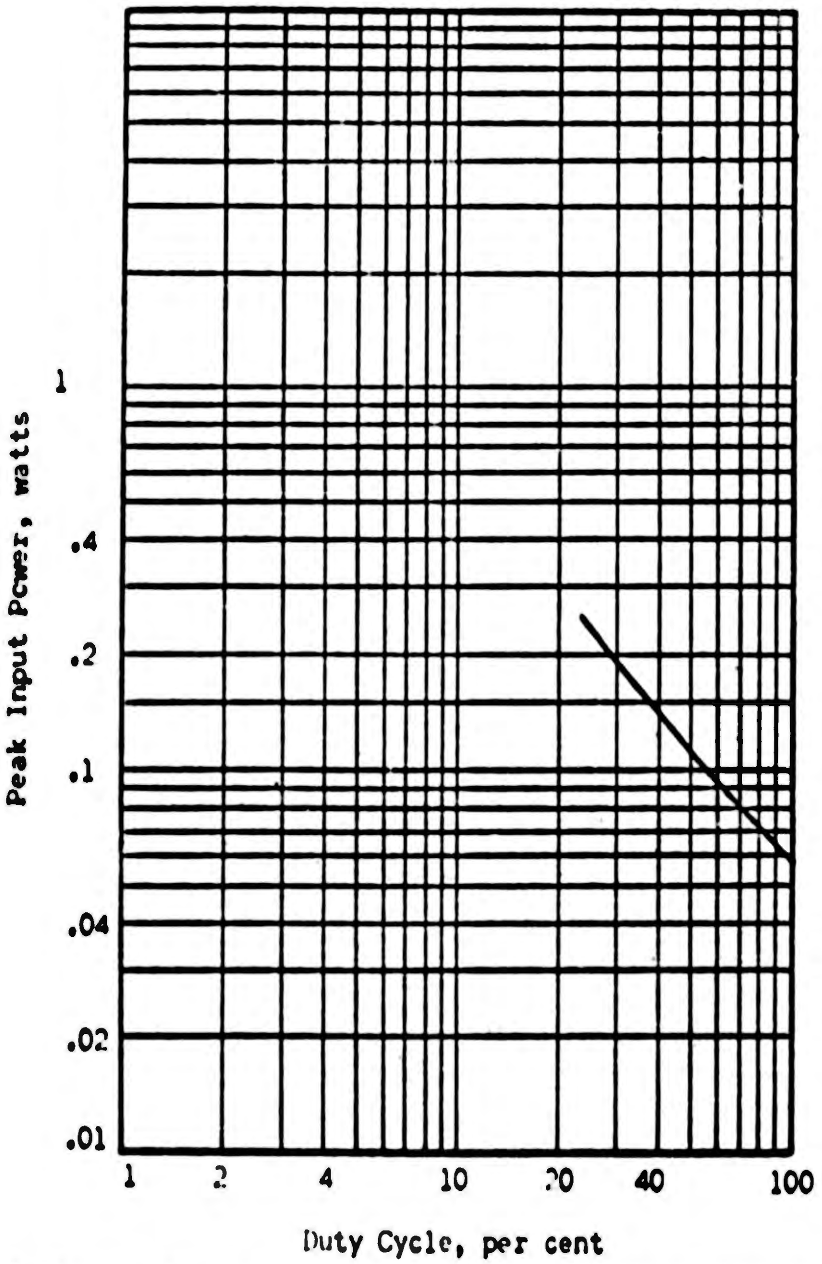


FIGURE B-66. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = < 100

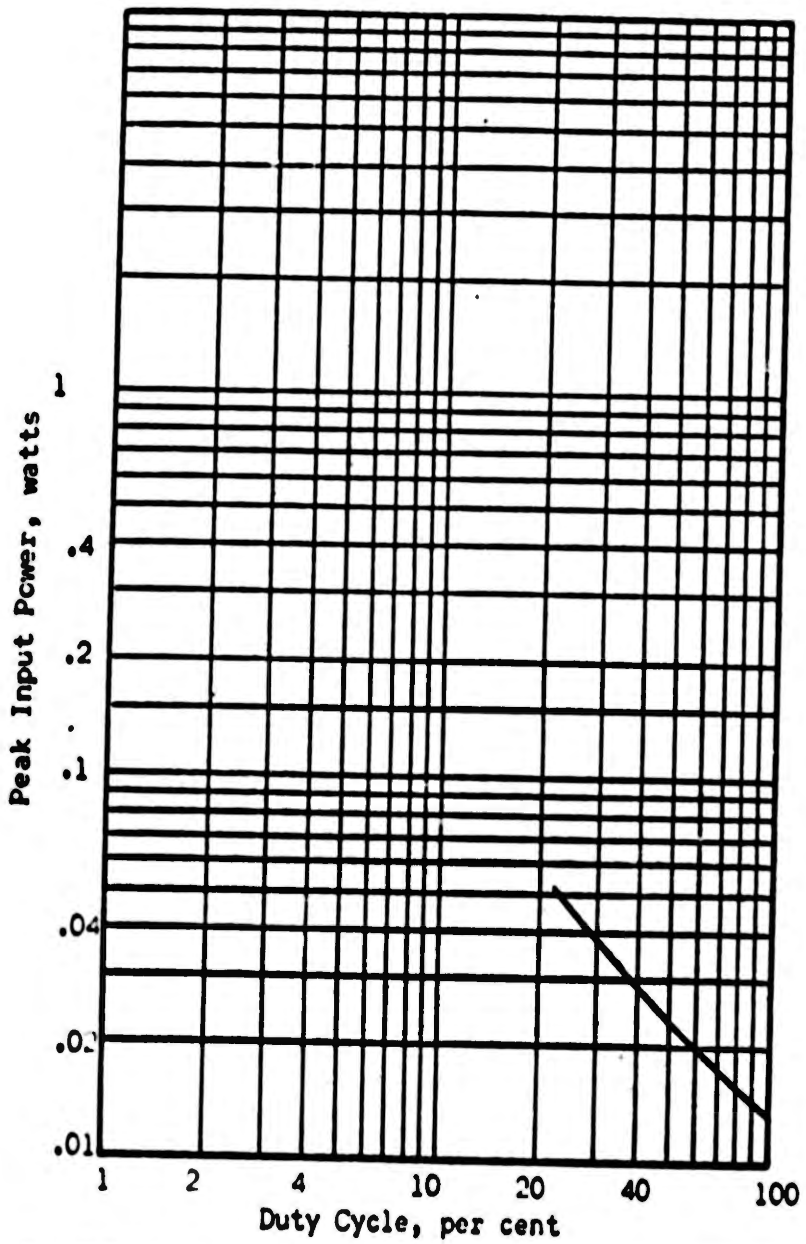


FIGURE B-67. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 10 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = < 100

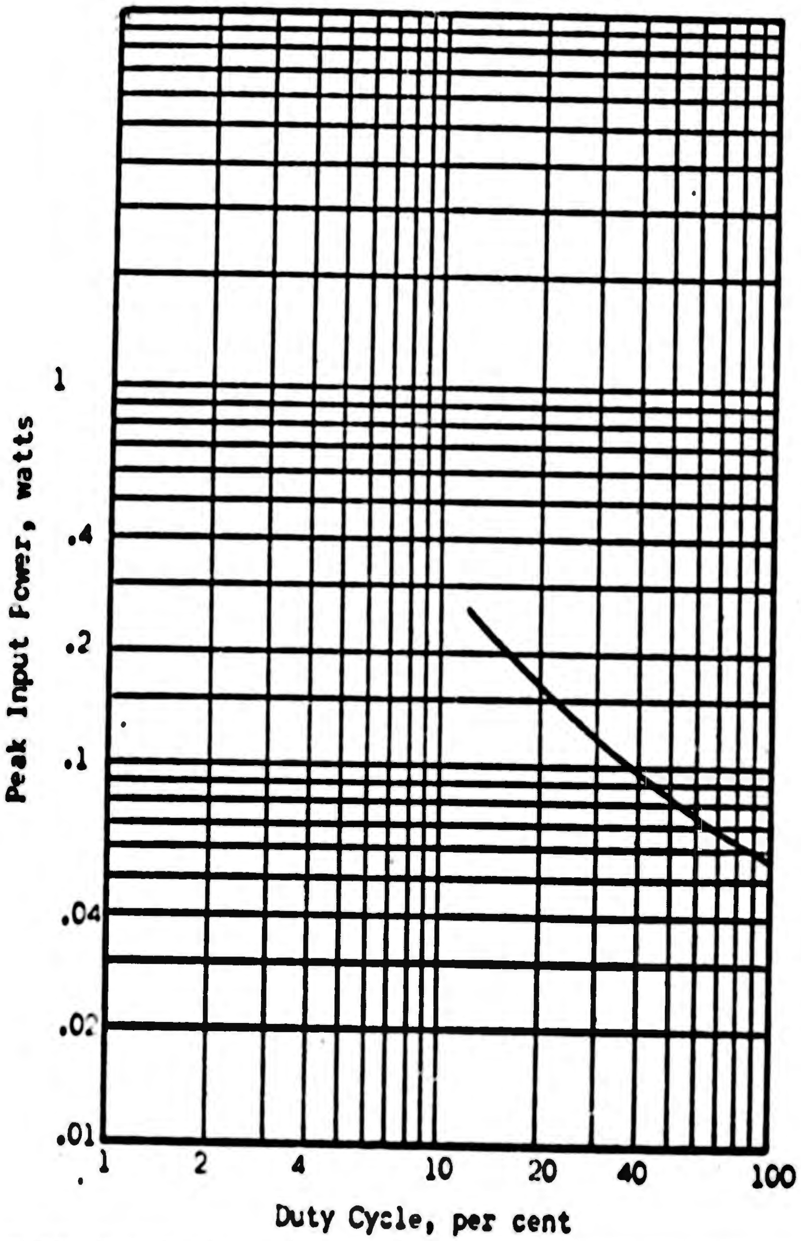


FIGURE B-66. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = < 100

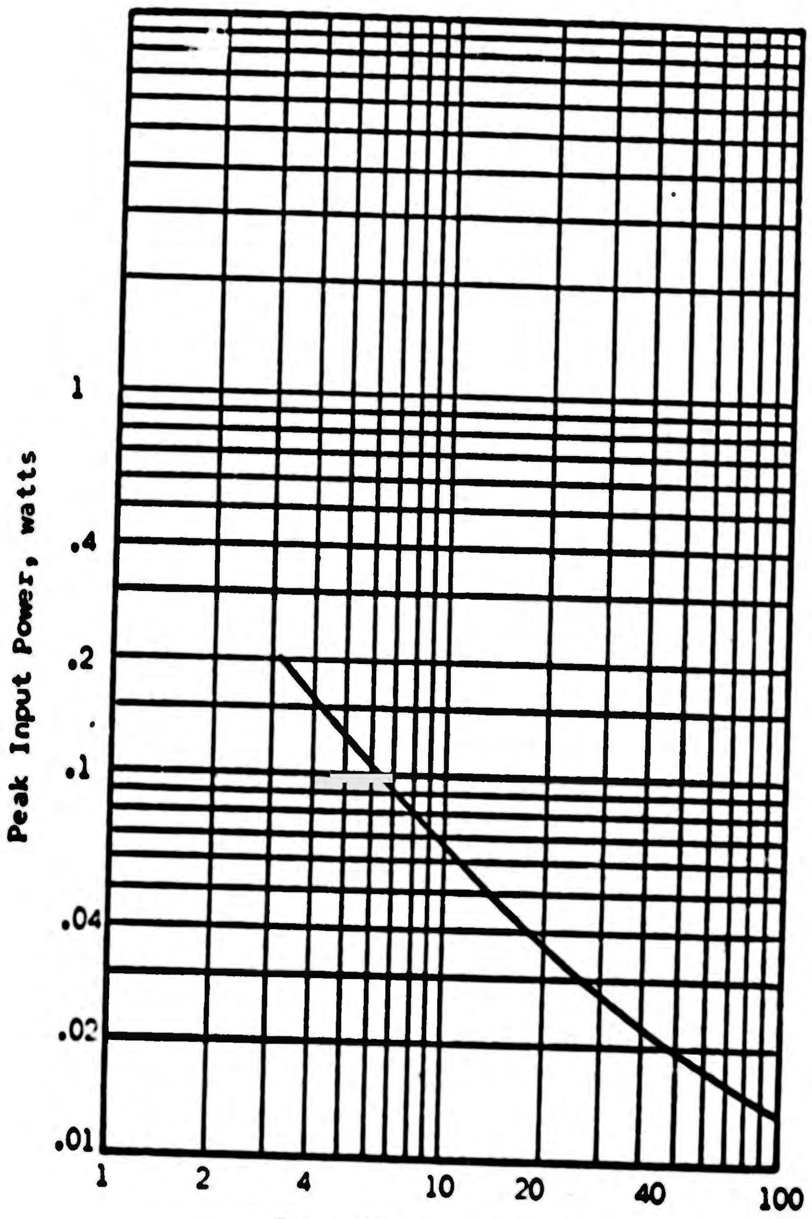


FIGURE B-69. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 100 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = < 100

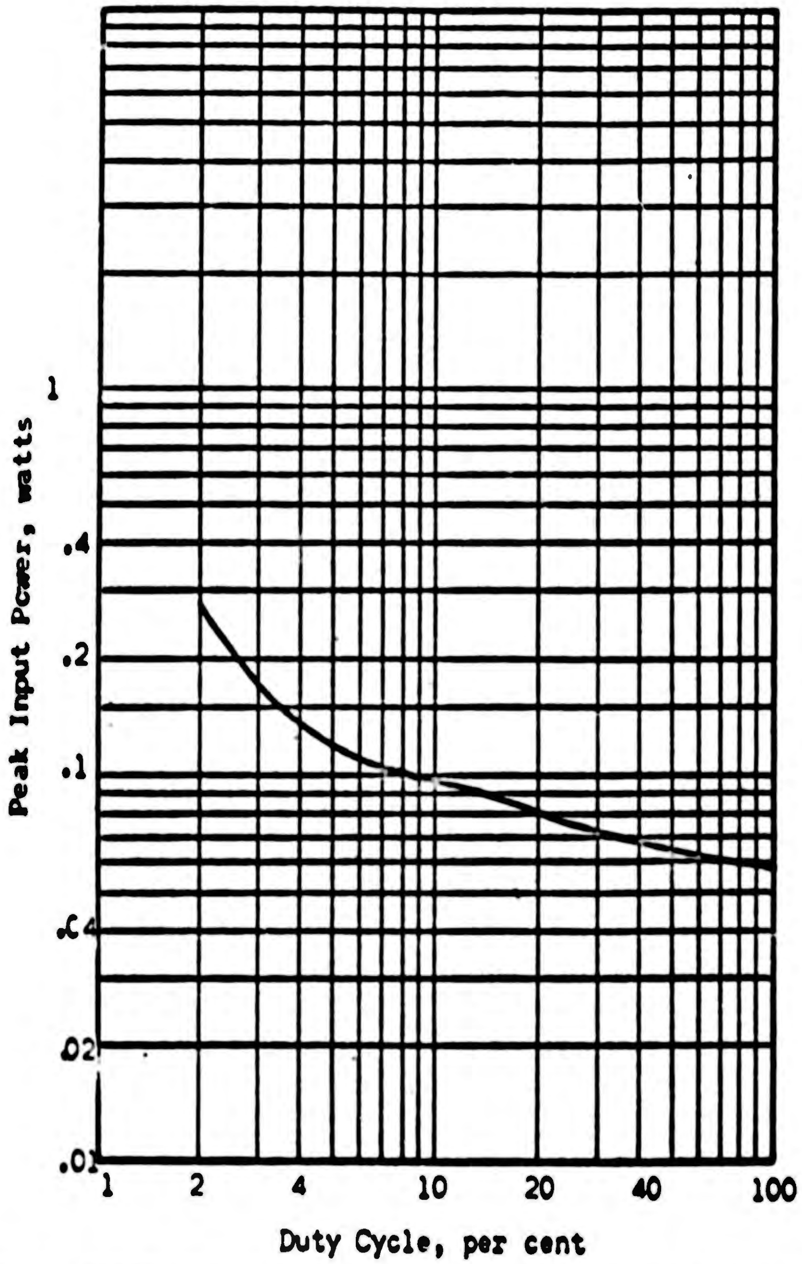


FIGURE B-70. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 25 C
Peak junction temperature = 85 C
Stability factor = < 100

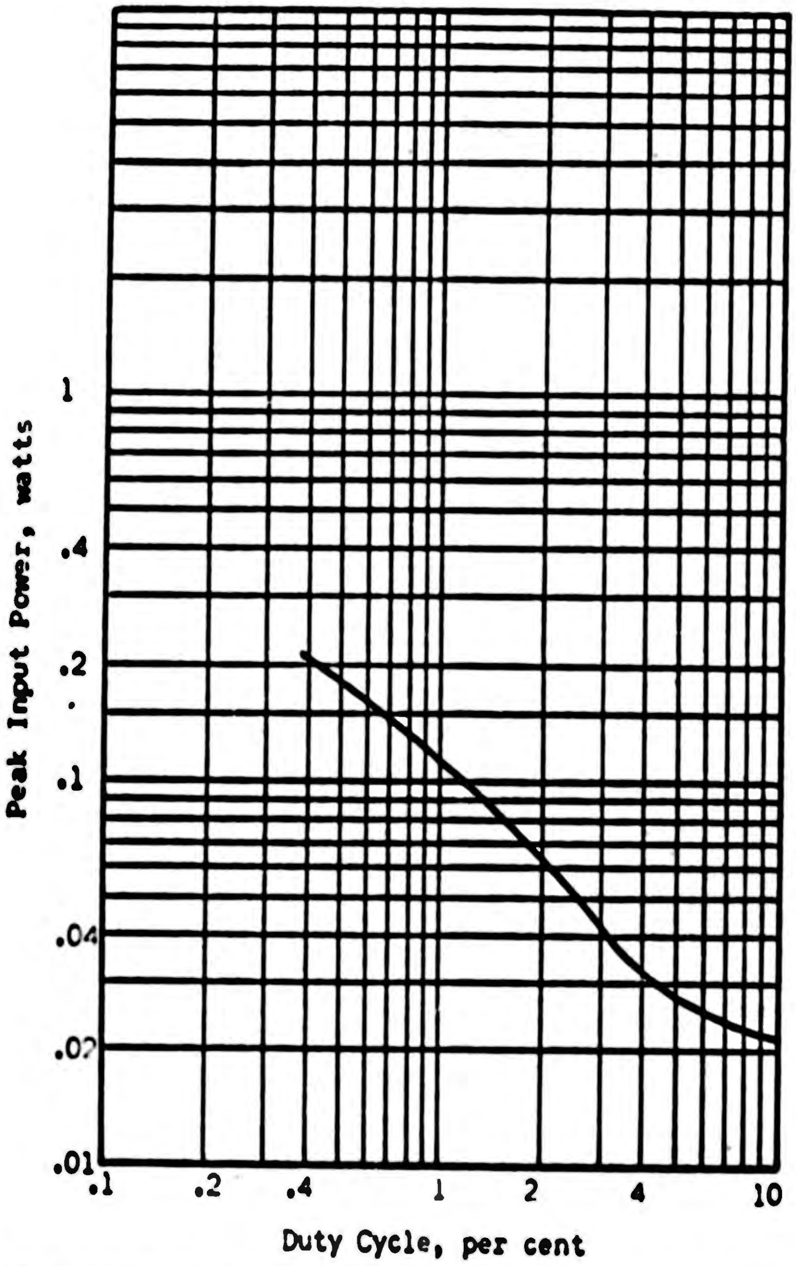


FIGURE B-71A. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = < 100

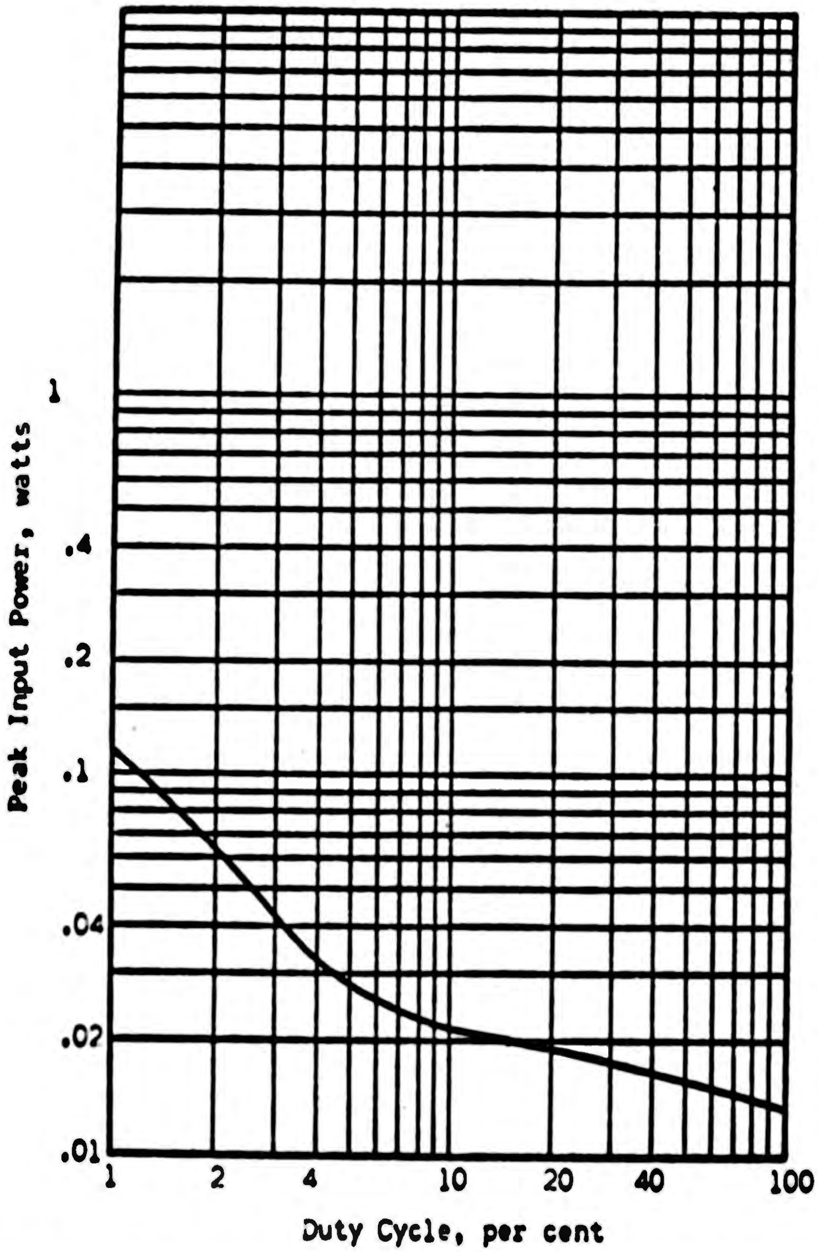


FIGURE B-71B. 2N502 PEAK INPUT POWER AS A FUNCTION OF DUTY CYCLE

Square wave input
Repetition period = 1000 milliseconds
Collector voltage = < 20 volts
Ambient temperature = 65 C
Peak junction temperature = 85 C
Stability factor = < 100

APPENDIX C

DETAILS OF OPERATION OF THE TRANSISTOR THERMAL ANALOG

APPENDIX C

DETAILS OF OPERATION OF THE TRANSISTOR THERMAL ANALOG

The purpose of this Appendix is to present general operating details which should aid in the operation of any transistor thermal analog, and to present operating details for the transistor thermal analog as used during this project.

General Description

Figure 14 (in the body of the report) is a diagram of the transistor thermal analog. The network representing the transistor is shown on the right. This network operates at a potential above ground, and therefore, the network and all connections to it should be shielded from stray electrical pickup.

A 6AU6 vacuum tube was used for the analog developed during this project, but any suitable pentode should be acceptable. The circuit constants of the 6AU6 were adjusted so that the current output of the tube (for a given voltage on the control grid) was constant for a load impedance of low value up to approximately 90,000 ohms. Under these conditions, linear operation occurred in the current range from 1 to 9 milliamperes. Thus, the quiescent current through the analog network was 1 milliampere, and under this condition the voltage drop across the analog network was at a minimum. With a voltage applied to the 6AU6 control grid, the current flow increases and the voltage across the network increases. The zero battery connection is such that a negative voltage appears at the oscilloscope. The negative voltage is equivalent to a positive temperature change.

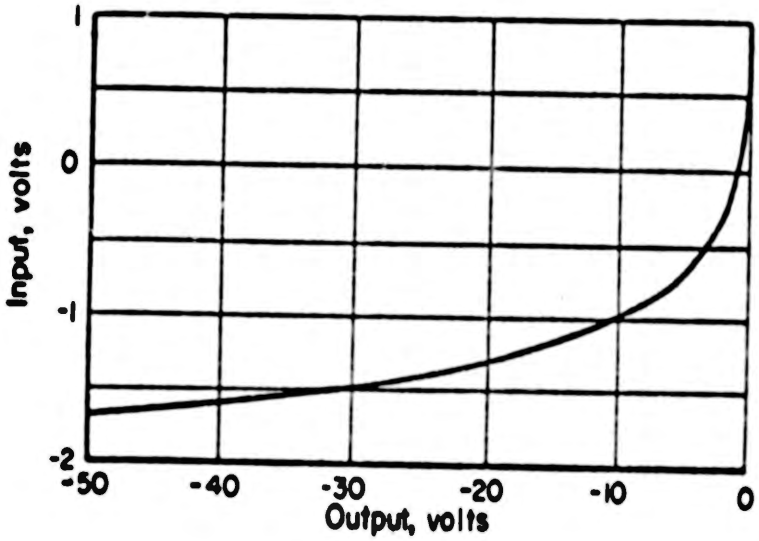
The input to the 6AU6 current source is obtained from two operational amplifiers. The inputs from the signal generator and from the feedback loop are, therefore, 180 degrees out of phase. The input and feedback resistors for the operational amplifiers were constructed in plug-in units to allow for variations from one transistor type to another by changing the gain of the amplifiers.

The equation for the operation of the feedback loop is given at the top of Figure 14 (in the body of this report). It may be seen from this equation that the input to the feedback loop should be zero for a zero temperature difference between the junction of the transistor and ambient temperature. Therefore, the quiescent voltage appearing across the network is balanced out with an adjustable battery. This battery has an output of from 500 to 600 volts and should be adjustable to within 0.1 volt of the desired value. Thus, the voltage, appearing at the input to the attenuator and the input to the oscilloscope, is equivalent to the junction temperature, T_j.

The attenuator in the feedback loop represents "k" in the operation equation. For the transistor types used during this project, it was found that the adjustable portion of the attenuator should represent from 1/4 to 1/3 of the total attenuation. With this ratio the adjustment was sufficiently sensitive to permit easy setting of the proper value of k.

The adder in the feedback loop is a conventional four-input summing circuit with both negative and positive outputs. This permits both positive and negative outputs from the feedback loop to obtain proper phasing for various modes of operation. The three log voltage sources are mercury batteries and ten-turn potentiometers.

The antilog of the adder output is obtained by using an arbitrary-function generator. The arbitrary-function generator is adjusted to produce the input-output function shown in Figure C-1. This adjustment is very critical for values of input voltage greater than zero; if the output of the arbitrary-function generator becomes positive, the 6AU6 is biased to a cutoff condition and the feedback loop causes the 6AU6 to remain in this condition no matter what the input is from the signal generator. Accordingly, a biased diode is used to prevent the arbitrary-function-generator output from becoming positive.



A-36161

FIGURE C-1. ARBITRARY-FUNCTION-GENERATOR INPUT-OUTPUT FUNCTION

A block diagram of the cable connections for the transistor thermal analog is shown in Figure C-2. The connections shown are for a signal generator with a positive output. For a signal generator with a negative output, the signal generator is connected to the feedback-loop input and the feedback loop is connected to the signal-generator input. The input to the arbitrary function is taken from the negative output of the adder. It is thus necessary to readjust the arbitrary-function generator so that the input varies from -1 to +2 volts and the output varies from zero to +50 volts. The biased diode must be reversed.

Operating Procedure

The operating procedure given below should be followed in detail to obtain proper operation of the transistor thermal analog and to prevent damage to the equipment. Variations from this procedure are possible, and in some cases desirable, but variations should not be attempted until some experience is gained with the operation of the transistor thermal analog.

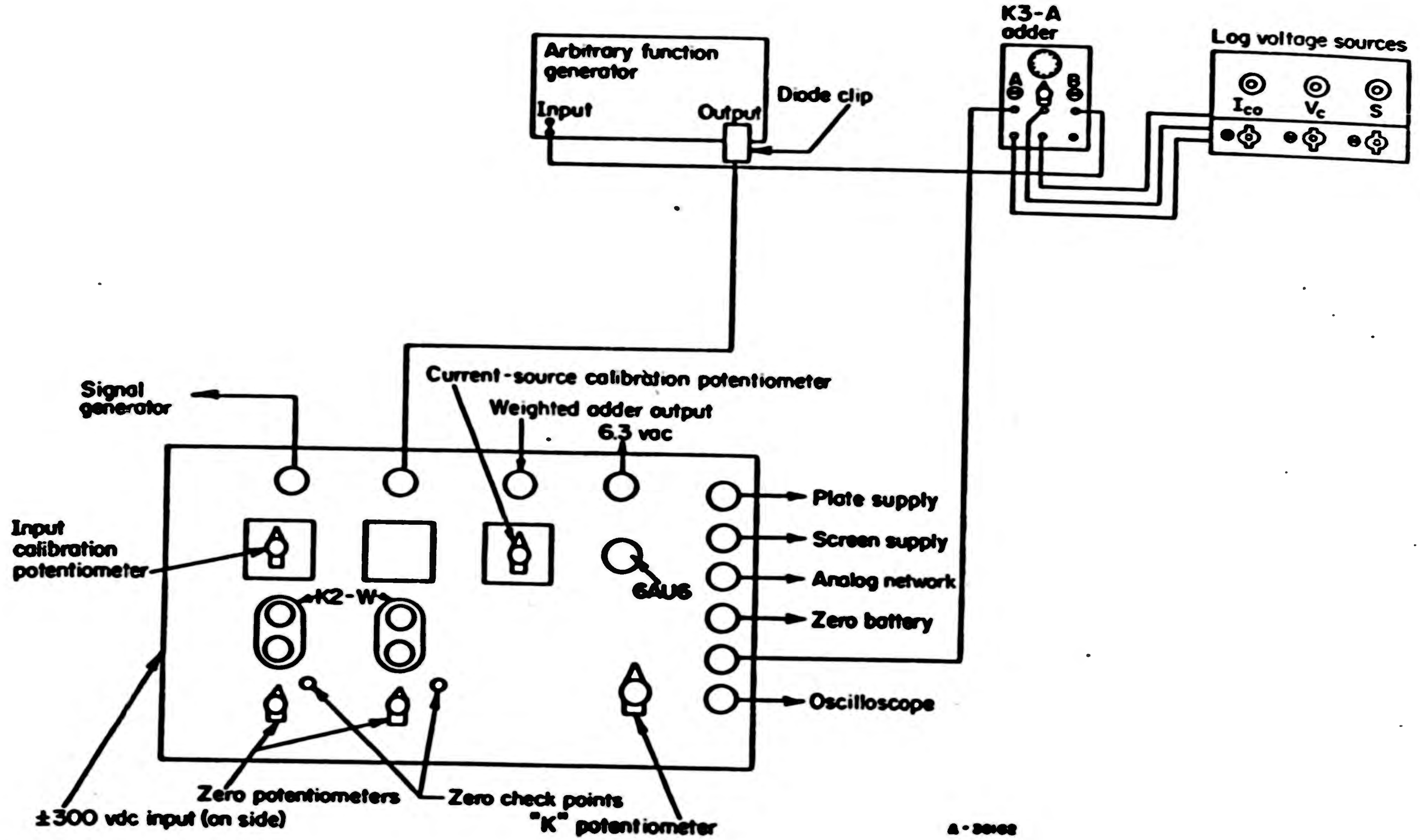


FIGURE C-2. DIAGRAM OF EQUIPMENT CONNECTIONS AND ADJUSTMENT LOCATIONS

Equipment Connections

The various pieces of equipment which make up the transistor thermal analog should be connected together as shown in Figure C-2. Before turning on the equipment, open the connections from the arbitrary-function-generator output, to the input of the arbitrary-function generator, and to the adder from the main chassis. Turn on all of the equipment except the 600-volt plate supply and the 150-volt screen grid supply. Allow at least 30 minutes to warm up.

Zeroing Amplifiers

See the arbitrary-function-generator operating instructions for the zeroing procedure for this piece of equipment. With zero input to the K3-A adder, adjust potentiometer A for zero output at the negative (lower) output jack. Adjust potentiometer B for zero output at the positive output jack. On the main chassis, adjust the K2-W operational amplifier on the left for zero output (using the potentiometer and check point on the left). Repeat this procedure for the righthand K2-W operational amplifier.

Log Voltage-Source Calibration

Set the log I_{co} dial to 85714 and adjust the calibration potentiometer (to the left of the on-off switch) so that the adder output is +6 volts. Set the log V_c dial to 86957 and adjust the calibration potentiometer so that the adder output is -2 volts (log I_{co} turned off). Set the log S dial to 10,000 and adjust the calibration potentiometer so that the adder output is -2 volts.

Zero Battery Adjustment

Turn on the 600-volt plate supply. When the plate supply has had time to warm up, turn on the screen supply. This turn-on sequence is necessary since the 600-volt supply will not regulate properly if turned on under load. Adjust the variable zero battery so that the input to the oscilloscope is zero.

"K" Potentiometer Adjustment

Turn the "k" potentiometer to the full counterclockwise position. Make the connection between the feedback output of the main chassis and the adder input. For the sake of clarity, a 2N697 transistor will be used as an example for the remainder of the procedure. The 2N697 transistor is a 2-watt silicon transistor with a maximum junction temperature of 175°C.

Adjust the log I_{co} voltage source for the value of I_{co} at 170 C (see Appendix D for dial settings). Record the output of the adder. Adjust the log I_{co} source for a value of I_{co} at some lower temperature. For the 2N697 the leakage current is about 1 microampere at 90 C, and this is the minimum setting of I_{co} obtainable from the log voltage source. Apply a d-c voltage to the signal-generator input which will produce a voltage change across the analog network equivalent to a temperature change of 80°C (170 - 90 = 80). Adjust the k potentiometer so that the adder output equals the voltage recorded for the 170 C I_{co} setting.

Feedback-Loop Calibration

Connect the arbitrary-function generator into the circuit. Set the values of log V_c and log S to some convenient values. Compute the value of P_{co} for these settings and determine what current flow in the analog network is equivalent to the power. From this, compute the d-c voltage drop across the network produced by this current flow. Adjust the feedback-loop calibration potentiometer so that this computed voltage appears at the oscilloscope input. Improper choice of value of log V_c and log S may produce thermal runaway. If this happens, choose some smaller value of log S and repeat the above procedure. If thermal runaway does occur, it is necessary to turn off the screen grid voltage momentarily to stop oscillation of the 6AU6 circuit caused by the overload condition and associated nonlinear operation.

Input Calibration

Disconnect the output of the arbitrary-function generator. Adjust the input calibration potentiometer so that the current flowing in the analog network is equivalent to desired power equivalent for the voltage (d-c) input.

Calibration Variations

A little experience with the transistor thermal analog will show that there is considerable latitude in the calibration settings for the same transistor type. For example, a variation in the gain of the feedback input of the weighted adder will result in a variation of the setting of the feedback calibration potentiometer and a variation in the setting of the input calibration potentiometer. It may happen that when the feedback calibration is completed, it might not be possible to get a reasonable calibration of the input voltage from the signal generator. In this case, an adjustable gain for the feedback-loop input to the weighted adder is helpful.

The choice of the voltage input equivalent to a given power input to the transistor is a function of the response of the analog network. If the network has a response curve with a very sharp rise, it will be found that the increase in power with a decrease in duty cycle (to maintain a constant peak temperature rise) is not as great as that required for a network with slower rise times. A change in input wave shape will also affect this characteristic. For a detailed study of any one transistor type, several input-voltage calibrations might be desirable; a calibration for a wide range of power inputs results in poor readability for lower power inputs, and a calibration for small power inputs results in overloading the operational amplifiers (for a gain of 2 in the input calibration amplifier and a gain of 2 for the weighted adder, a 12-volt input signal will produce a 48-volt output signal from the weighted adder, and the maximum voltage range for the operational amplifiers is ±50 volts).

There is no one calibration procedure which is applicable for all transistor types or for different operating ranges of the same transistor type. Experience with the transistor thermal analog will bring increased accuracy of calibration, increased readability of results, and easier operation.

APPENDIX D

EQUIPMENT SPECIFICATIONS

APPENDIX D

EQUIPMENT SPECIFICATIONS

The purpose of this Appendix is the identification of the equipment used in the transistor thermal analog. Purchased equipment will be identified by the manufacturer's name and model number. Constructed equipment will be described by circuit diagrams and operating characteristics.

Adder

The adder used in the feedback loop of the transistor thermal analog is a Philbrick Model K3-A Adding Component. This adder computes the instantaneous sum of up to four voltage inputs and an adjustable constant voltage.

Arbitrary-Function Generator

The arbitrary-function generator used in the feedback loop of the transistor thermal analog is a Philbrick Model FF Arbitrary Function Component. The output is an adjustable function of the input, utilizing an approximation of ten line segments; each with independently adjustable length and slope, and with adjustable rounding between segments.

Signal Generator

The signal generator referred to in this report is a combination of purchased and constructed equipment. This was necessary because the purchased signal generator had no method of varying the amplitude of the output voltage. The purchased signal generator was a Tektronix Type 162 Wave Form Generator. This signal generator was triggered from an external oscillator which determined the repetition frequency of the output pulses. The gate and saw-tooth outputs were used. The gate output produces a 50-volt positive square wave. The duration of this square wave is determined by the setting of the timing circuit of the 162 generator. The saw-tooth output produces a signal which rises to 150 volts, maintains 150 volts for a period of time, and then decreases linearly to zero. The timing circuit of the 162 generator determines the length of time required by the linearly decreasing portion of the output.

An additional piece of equipment was required to vary the amplitude of the output of the 162 generator and also to bias out the +150 volt portion of the saw-tooth wave. This equipment also contains circuits for obtaining half-sine-wave pulses of varying repetition frequency and duty cycle. The schematic for this equipment is shown in Figure D-1.

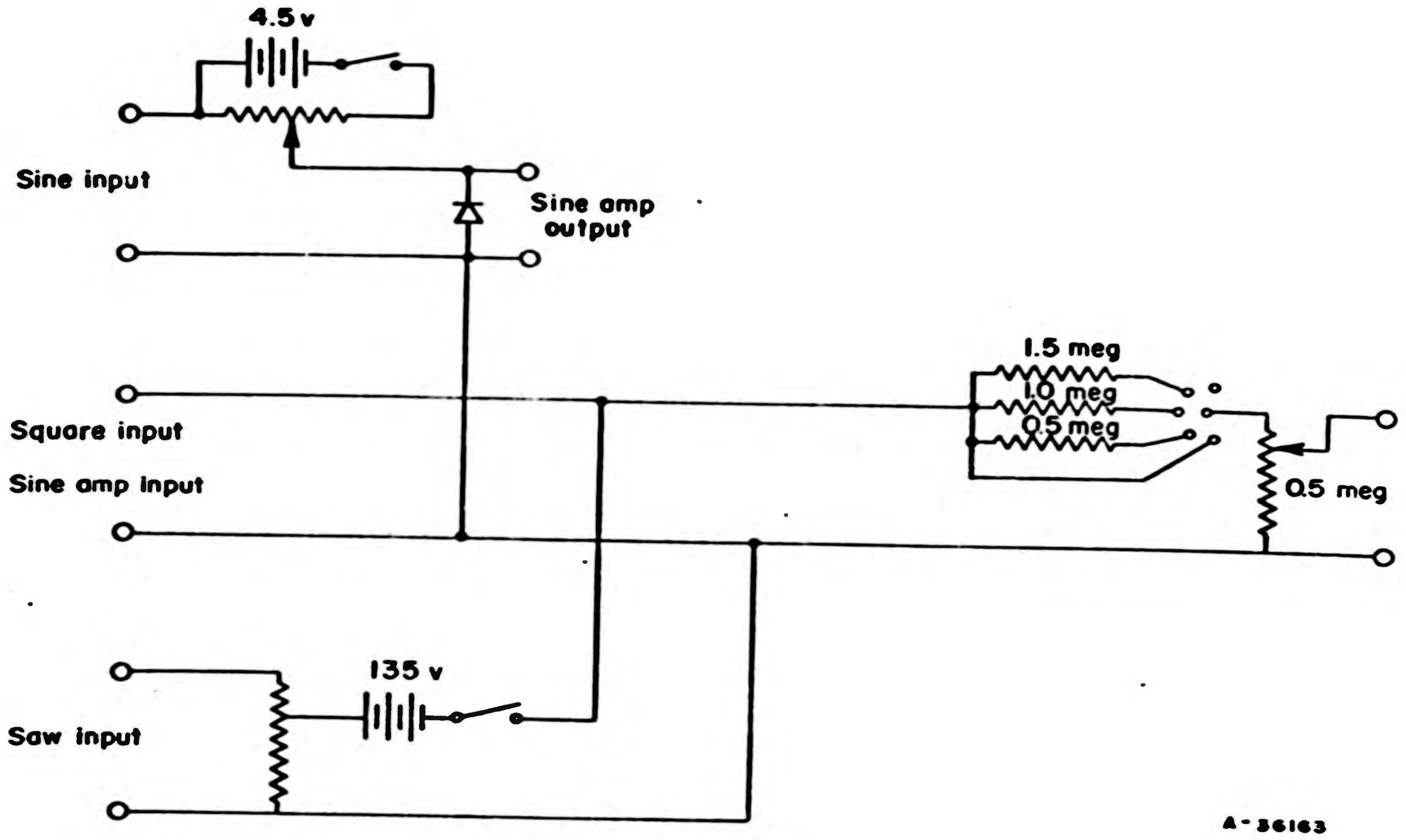


FIGURE D-1. INPUT SIGNAL ATTENUATOR

Weighted Adder and Input Calibration Amplifiers

The weighted adder and input calibration amplifiers are Philbrick K2-W Operation Amplifiers. The circuits used with these amplifiers are shown in Figure D-2. Figure D-2 also shows the electrical connections for the plug-in circuit boxes.

Power Supplies

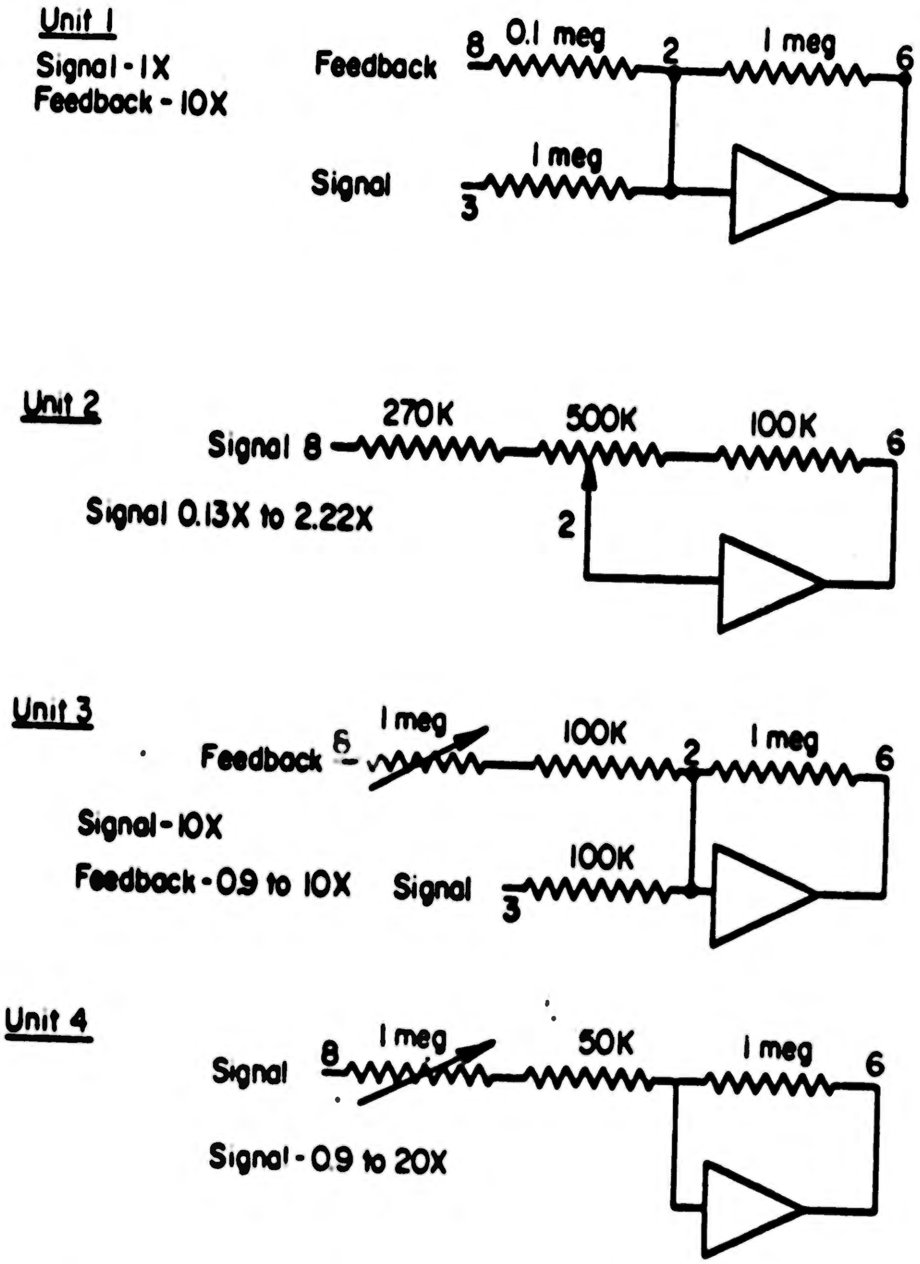
The power supplies for the adder, the arbitrary-function generator, and the operation amplifiers are two Philbrick Model R-100B Power Supplies. The power supply for the signal generator is a Tektronix Type 160A Power Supply. The 600-volt plate supply and the 150-volt screen grid supply are conventional power supplies regulated by VR tubes. It is not considered necessary to supply schematics for these power supplies.

Zero Battery

The zero battery is a tapped battery in series with a voltage divider across a 3-volt battery. This combination provides a continuously adjustable voltage from 500 to 600 volts. This battery floats above ground potential and is shielded from stray pickup.

Log Voltage Sources

The log voltage sources are mercury batteries connected as shown in Figure D-3. The voltage outputs are obtained across ten-turn potentiometers. See Appendix C for the calibration procedure for the log voltage sources. The dial setting equivalent to various values of I_{CO}, V_C, and S are given in Tables D-1, D-2, and D-3.



Note: Numbers refer to plug pin numbers.
Pin 5 ground on all units.

A-36164

FIGURE D-2. TRANSISTOR THERMAL ANALOG PLUG-IN UNITS

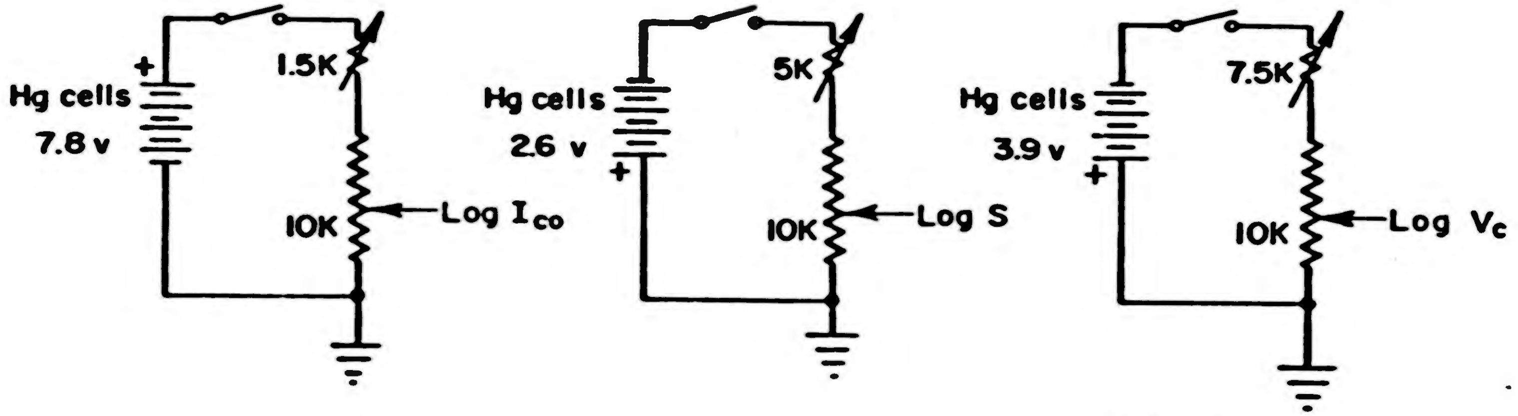


FIGURE D-3. LOG VOLTAGE SOURCES

TABLE D-1. LOG I_{co} VOLTAGE-SOURCE OUTPUT

I_{co}, microamperes	I_{co}, milliamperes	Dial Setting	Output Voltage, volts
1		8571	6.000
2		8141	5.699
3		7890	5.523
4		7711	5.398
5		7573	5.301
6		7460	5.222
7		7364	5.155
8		7281	5.097
9		7208	5.046
10		7143	5.000
15		6891	4.824
20		6713	4.699
25		6574	4.602
30		6461	4.523
35		6366	4.456
40		6283	4.398
45		6210	4.347
50		6144	4.301
60		6031	4.222
70		5936	4.155
80		5853	4.097
90		5780	4.046
100		5714	4.000
200		5284	3.699
300		5033	3.523
400		4854	3.398
500		4716	3.301
600		4603	3.222
700		4507	3.155
800		4424	3.097
900		4351	3.046
1000		4286	3.000
2000		3856	2.699
3000		3604	2.523
4000		3426	2.398
5000		3287	2.301
6000		3174	2.222
7000		3078	2.155
8000		2996	2.097
9000		2923	2.046
10000		2857	2.000
	10	2857	2.000
	20	2427	1.699
	30	2176	1.523
	40	1997	1.398
	50	1859	1.301
	60	1745	1.222
	70	1650	1.155
	80	1567	1.097
	90	1494	1.046
	100	1427	1.000

TABLE D-2. LOG V_c VOLTAGE-SOURCE OUTPUT

V_c, volts	Dial Setting	Output Voltage, volts
1	0000	0.000
2	1309	-0.301
3	2074	-0.477
4	2618	-0.602
5	3039	-0.699
6	3383	-0.778
7	3674	-0.845
8	3926	-0.903
9	4149	-0.954
10	4348	-1.000
12	4692	-1.079
14	4983	-1.146
16	5235	-1.204
18	5458	-1.255
20	5657	-1.301
25	6078	-1.398
30	6422	-1.477
35	6713	-1.544
40	6966	-1.602
50	7387	-1.699
60	7731	-1.778
70	8022	-1.845
80	8274	-1.903
90	8497	-1.954
100	8696	-2.000

TABLE D-3. LOG S VOLTAGE-SOURCE OUTPUT

S	Dial Setting	Output Voltage, volts
1	0000	-0.0000
2	1505	-0.301
3	2386	-0.477
4	3010	-0.602
5	3495	-0.699
6	3891	-0.778
7	4226	-0.845
8	4516	-0.903
9	4771	-0.954
10	5000	-1.000
20	6505	-1.301
30	7386	-1.477
40	8010	-1.602
50	8495	-1.699
60	8891	-1.778
70	9226	-1.845
80	9516	-1.903
90	9771	-1.954
100	10000	-2.000

APPENDIX E

RECOMMENDED CHANGES IN THE EXPERIMENTAL AND ANALOG EQUIPMENT

APPENDIX E

RECOMMENDED CHANGES IN THE EXPERIMENTAL AND ANALOG EQUIPMENT

The purpose of this Appendix is to present recommended changes in the experimental and analog equipment used on this project. These recommended changes are the result of knowledge gained about the thermal operation of transistors and experience gained during the course of the project.

As has been pointed out, one source of uncertainty and error in operation of the analog has been the inability of the relay-operated circuit shown in Figure 11 to obtain the first 2 milliseconds of the cooling curve. This circuit is delayed by the time required for the relays to switch. It is recommended that this circuit be replaced by a circuit employing solid-state switching elements, as shown in Figure E-1. The mechanical switch, S, is used to turn on and off the base drive, and hence, the power input to the transistor. Diode D_1, a high-speed switching diode, permits base current to flow. When switch S is opened, the power pulse is removed, Diode D_1 is reverse biased, and I_{co} can be measured across R_b.

As mentioned in conjunction with the verification experiment, which uses a similar circuit, some delay is introduced by the time constant of R_b and stray shunt capacitance. This can be reduced by using a sensitive preamplifier to enable R_b to be reduced. This preamplifier should be mounted in close physical proximity to R_b, and should have low input capacitance.

The forward voltage drop across D_1 is about 0.5 volt, while the peak value of I_{co} R_b should be less than this to keep the required value of R_b as low as possible. The function of D_2 is to clip the amplified (0.5 X gain) forward voltage drop so as not to overdrive the oscilloscope. The resultant oscilloscope traces can be photographed with several different linear sweep rates to obtain the cooling curve.

The same arrangement of a preamplifier followed by a diode clip shown in Figure E-1 may also be included in the circuit shown in Figure 15. In this manner, the accuracy of any further verification experiments would also be improved through the elimination of the problems encountered in estimating the value of I_{co} during the first millisecond after the power pulse to the transistor is removed. The diode clip should also improve the d-c reference of the oscilloscope, by preventing overdriving.

The above changes in the circuit for obtaining the cooling curve should greatly increase the accuracy of the electrical network used to represent the thermal behavior of the transistor in the transistor thermal analog. This increase in the accuracy of the analog network dictates an increase in the accuracy of the remaining portions of the transistor thermal analog. The changes recommended below for the transistor thermal analog reflect this need for increased accuracy and also result in a piece of equipment which should be more easily set up than the transistor thermal analog developed in this project. The required operating time to obtain given results will also be reduced.

At the time the transistor thermal analog was set up, there was no information available on the ranges of capacitances and resistances required to represent the

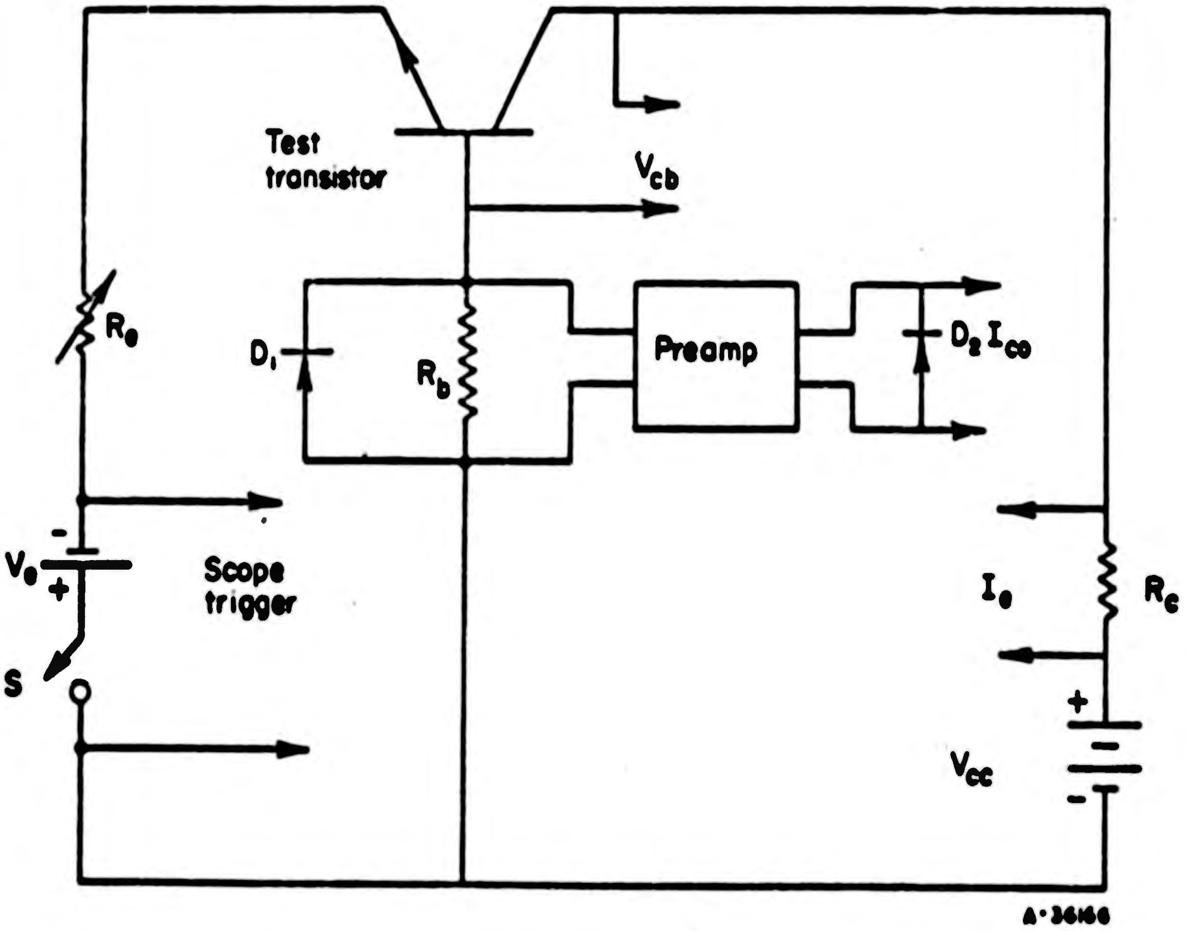


FIGURE E-1. CIRCUIT FOR OBTAINING COOLING CURVE transistor. Accordingly, the individual elements of the series string of RC pairs were made up of plug-in units. These plug-in units were made up of hand-picked ±10 per cent resistors and capacitors (a very time-consuming process). Experience gained during this project makes possible the recommendation of the arrangement of decade units given in Table E-1.

TABLE E-1. RECOMMENDED RANGE OF RESISTANCE AND CAPACITANCE VALUES FOR THE ANALOG NETWORK COMPONENTS

RC Pair Number	Resistance Decades, ohms	Capacitance Decades, microfarads
1 and 2	10K to 60K	1.0 to 9.0
	1K to 9K	0.1 to 0.9
	100 to 900	0.01 to 0.09
	Variable to 100	0.001 to 0.009
3 and 4	10K to 60K	0.1 to 0.9
	1K to 9K	0.01 to 0.09
	100 to 900	0.001 to 0.009
	Variable to 100	0.0001 to 0.0009
		Variable to 100 μμf

Two pairs of terminals should be made available for the addition of a fifth RC pair. These terminals would normally be shorted. Two additional terminals should be available for the insertion of a network to represent chassis or mounting conditions should it be desired to include these in the analog. The addition of a network to represent chassis conditions would have the effect of lowering the required resistance values of the RC pairs and increasing the capacitance values of the RC pairs. The values of capacitance given in Table E-1 need not be changed, since higher capacitance values would be compensated for by changing the real-to-analog time ratio.

It should be remembered that the analog network operates about 500 volts above ground potential, so the analog network decades must be shielded from stray pickup and insulated for operator protection.

One of the most time-consuming portions of the operation of the transistor thermal analog is maintaining the proper adjustment of the zero battery. This battery reduces the quiescent voltage across the analog network to zero to supply the proper input to the feedback loop. The magnitude of this battery is from 500 to 600 volts. Although there is little or no current drawn from the battery, the battery output varies up and down about 1 volt over short periods of time. The value of this voltage must be maintained well within 0.1 volt of the required value. Another requirement of this battery is that it must be very well isolated from ground and stray pickup. Therefore, it is suggested that for any future analogs this battery be replaced by an electronically regulated power supply. Because of the isolation problems, this power supply will of necessity be entirely battery operated. Battery operation is feasible because there is almost no current drain. The electronic regulation could be accomplished with low filament current tubes and an accurate reference diode or VR tube. Inclusion of the regulated power supply should reduce the operation time of the transistor thermal analog by about 50 per cent.

Another time-consuming operation is the switching of the oscilloscope from the output of the analog to the signal input of the analog in order to measure the peak value of the input voltage. This operation could be eliminated through the use of an attenuator system which could be calibrated directly in peak volts; the amplitude of the output of the Tektronix 162 signal generator is unaffected by changes in the duration of the pulses.

The antilog function required by the transistor thermal analog was generated by an arbitrary-function generator. This generator has an input and output voltage range of ±50 volts. The input-voltage range used was -1 to +2 volts or +1 to -2 volts, and the output range was 0 to -50 or 0 to +50 volts. The adjustment of the arbitrary-function generator was critical and had to be checked periodically. Also, because of the narrow range of the input with respect to the wide range of the output, this piece of equipment was subject to short-term drift which hampered the operation of the transistor thermal analog. In addition, the rate of change of slope required by the antilog function was greater than could be accurately reproduced. It is therefore recommended that a piece of equipment be designed to specifically produce the antilog of voltages in the range of -1 to +2. A phase inversion amplifier could be used following the function generator to eliminate the necessity of the plus 1 to minus 2-volt input.

If it is desired to study the effect of pulses of duration down to the order of microseconds, particular attention must be paid to the response time of all of the equipment (purchased and constructed) used in the transistor thermal analog. It is the author's opinion that a frequency response of 50kc should be the lower limit. Obviously, the transistor thermal analog cannot be practically constructed to study some of the high-performance switching transistors presently available. The requirements upon the analog equipment would then become unreasonable.