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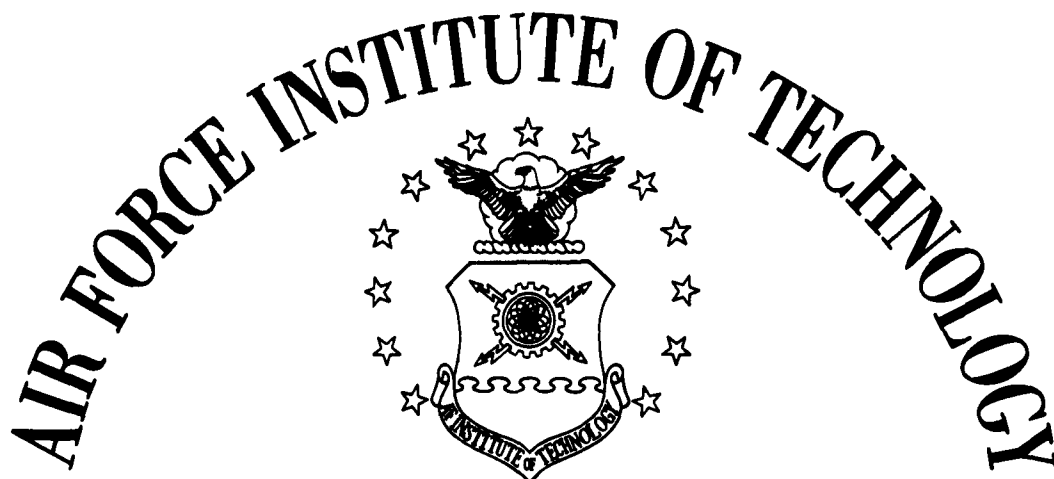
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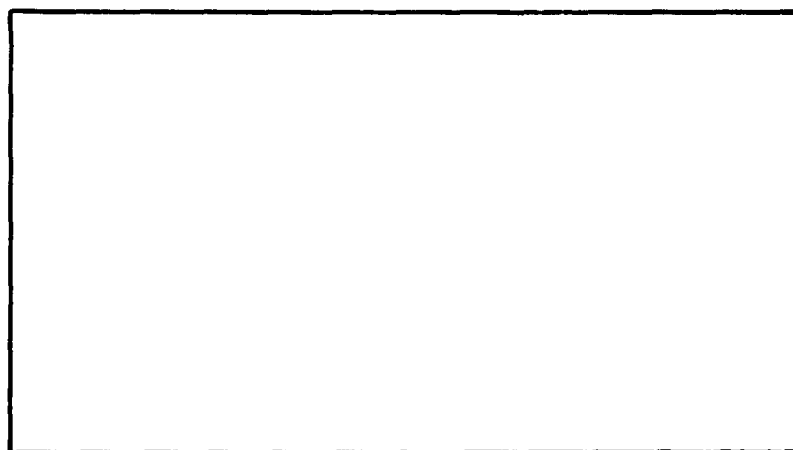
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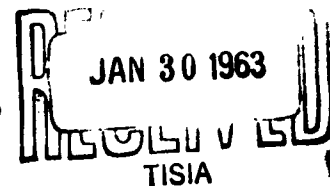


AIR UNIVERSITY
UNITED STATES AIR FORCE



SCHOOL OF ENGINEERING

WRIGHT-PATTERSON AIR FORCE BASE, OHIO



**Presented to the Faculty of the School of Engineering of
the Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the
Master of Science Degree
in Electrical Engineering**

**IMPROVEMENT OF THE IBM 1620 SPS
PROCESSOR
THESIS**

GE/EE/62-5

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Graduate Electronics

12 December 1962

Preface

The selection of this thesis project came as a result of an interest in the growing importance of computer programming in the fields of weapon system development and operations research. When this topic was brought to my attention by Professor C. H. Houpis it seemed like an excellent opportunity to become familiar with the problems involved in the application of computer programming techniques to these fields.

The excellent facilities available at Wright Field made the preparation of this thesis substantially easier. Of particular importance were the 7090 Data Processing System and the auxiliary input/output equipment that were used for numerous assemblies of my computer program. By their willingness to cooperate in the use of their equipment the personnel of the Analysis Branch, ASNCDA contributed immeasurably to this project.

A great deal of thanks goes to Lt. Richard L. Pratt, my faculty advisor, for all his assistance and encouragement in the preparation of this thesis. Only through his guidance was I able to learn in sufficient time the fundamentals of computer programming and analysis that enabled me to conduct an independent research in this area. His suggestions and knowledge of computer programming saved me many hours of lost labor

and effort throughout the thesis investigation.

Special thanks go...to my wife for her patience throughout the past year and a half and for typing this thesis...and to my children for their hours of forgone "playtimes".

And last is a vote of confidence to the AFIT 1620 computer which has been my constant companion (friend and foe) throughout these past five months.

Leland G. Fay

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Abstract

The IBM 1620 SPS Processor Program is examined to determine the possibility of shortening the program and of increasing the capability of the processor. SPS programming and coding techniques used to accomplish these ends are described and illustrated. Program checkout procedures are explained and the modified processor is redesignated the AFIT Version of the 1620 SPS Processor. Operating instructions and a listing of the program are included.

IMPROVEMENT OF THE IBM 1620 SPS PROCESSOR

I. Introduction

The purpose of this thesis project is to improve the IBM 1620 SPS Processor Program. A full appreciation of the problems encountered in this study requires complete familiarity with the IBM 1620 Data Processing System and the IBM 1620/1710 Symbolic Programming System. No attempt will be made to present a detailed breakdown of these systems, but those system aspects central to the problem under investigation will be discussed in context.

The IBM 1620 Data Processing System is a small electronic digital computer system designed for technical and scientific applications. For the purposes of this investigation the configuration of this system will include the IBM 1620 Central Processing Unit, and the IBM 1622 Card Read-Punch Unit which provides the punched card input and output for the processing system.

One of the programming systems designed for the IBM 1620 Data Processing System has been designated the 1620/1710 Symbolic Programming System. The complete system consists of the symbolic language used by the programmer in writing a source program, the library of subroutines and linkage instructions, and the processor

program which translates the symbolic language used by the programmer into the operating machine language of the 1620 (Ref 5:5).

This thesis investigation concerns itself with the modification of the processor program only.

The criteria established for the improvement of the IBM SPS Processor program were that the processor program would (1) occupy less space in core storage, and (2) have an increased performance capability. The adoption of these criteria resolved the thesis study into four major areas of investigation. These were:

1. To shorten the SPS Processor program so that it would occupy less memory storage space without reducing the capability of the processor.
2. To increase the capability of the SPS processor by incorporating the necessary coded routines or modifications into the processor program.
3. To perform a functional and operational checkout of the modified processor program using standard computer procedures.
4. To prepare a compiled list of operating procedures for the modified processor program for use with the 1620 computer facility at the Institute of Technology.

Since the importance of this study rests on the results achieved and the methodology employed, the thesis has been divided into chapters, each reflecting a particular aspect of the methods and techniques employed in this investigation.

Chapter two defines the terms and concepts most frequently used in this report. It includes a functional and operational description of 1620 Data Representation, the Symbolic Programming System and the SPS Processor.

Chapter three describes the basic programming process and associated equipment that was utilized in modifying the IBM 1620 SPS Processor Program.

Chapter four consists of two parts. Part one describes the concepts, methods and coding techniques employed to shorten the IBM SPS Processor Program. Part two outlines the computer programming and coding techniques utilized to increase the capability of the SPS processor.

Chapter five outlines the checkout procedures and techniques that were used to test the modified program.

Chapter six is a summary of the results obtained by employing the methods and techniques outlined in the preceding chapters. This chapter essentially itemizes the major improvements and modifications incorporated into the AFIT Version of the SPS Processor Program.

The appendix contains a compiled set of operating instructions and a detailed description of the AFIT Version of the 1620 SPS Processor Program. A label reference index and a program listing of the AFIT Version of 1620 SPS are also included.

The thesis as outlined above essentially provides a step by step analysis of the procedures, methods, and techniques of computer analysis and programming that led to the improvement of the IBM 1620 SPS Processor Program and resulted in the AFIT Version of 1620 SPS.

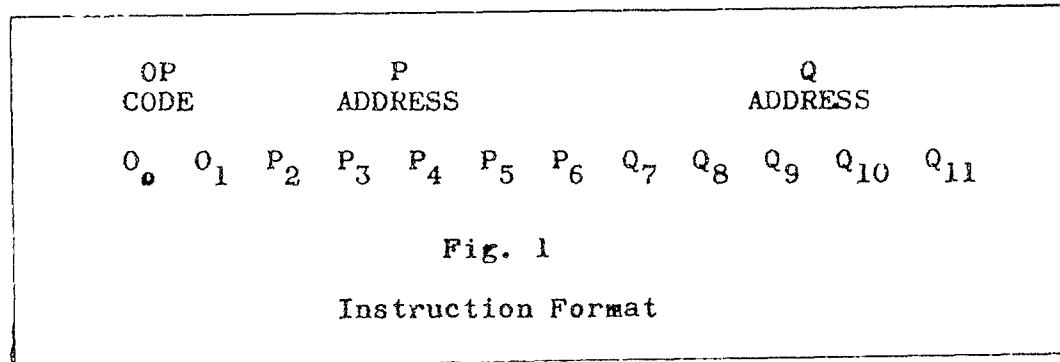
II. Terminology

This chapter is intended to serve as a reference for the terms and concepts utilized throughout the remainder of this thesis report. Those persons thoroughly familiar with the Symbolic Programming System and the 1620 Data Processing System may desire to proceed directly to chapter III.

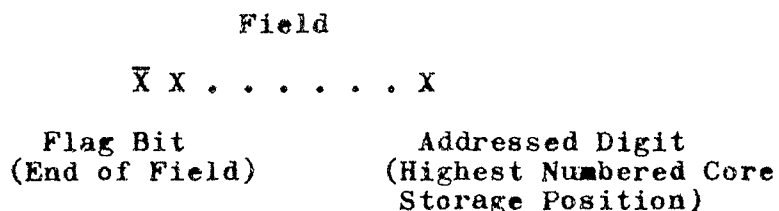
This chapter will discuss three topics - 1620 Data Representation, the Symbolic Programming System, and Processor Operation.

1620 Data Representation

Instruction Format. A 12-digit machine language instruction consisting of a 2-digit operation (OP) code, a 5-digit "P" address and a 5-digit "Q" address is used in the IBM 1620. The core storage format of the instruction is illustrated in Figure 1 (Ref 6:11).



Data Fields. All data can be classified as digits, fields or records, depending on the manner in which they are addressed. Each core storage position is addressable and can store one digit of information. A field consists of a number of consecutively addressed digits that are processed from right to left until terminated by a flag bit.



A record consists of a field or fields of data that are grouped for transmission. Internal records are processed from left to right until terminated by a record mark.

Operation Mode. The IBM 1620 can operate in either the numeric or alphameric mode when reading or writing data; the mode is designated by the input/output instruction. In the alphameric mode two digits of core storage are required to represent a character. Figure 2 shows the digits that are assigned to represent the alphameric characters used in the 1620. Use of the alphameric mode of operation permits program statements to be written in a symbolic language more meaningful and easier to handle than the numerical machine language (Ref 6:7-8).

Two-Digit Representation		Alphameric Character
00	b	
03	.	
04	)	
10	+	
13	\$	
14	*	
20	-	
21	/	
23	'	
24	(	
33	=	
34	@	
41	A	
42	B	
43	C	
44	D	
45	E	
46	F	
47	G	
48	H	
49	I	
50	O	
51	J	
52	K	
53	L	
54	M	
55	N	
56	O	
57	P	
58	Q	
59	R	
62	S	
63	T	
64	U	
65	V	
66	W	
67	X	
68	Y	
69	Z	
70	0	
71	1	
72	2	
73	3	
74	4	
75	5	
76	6	
77	7	
78	8	
79	9	

Minus
0 through 9

Plus or unsigned
0 through 9

Fig. 2

Alphameric Codes

Symbolic Programming System

The Symbolic Programming System is designed to simplify the preparation of programs for the 1620 Data Processing System. The symbolic language is the notation in which the programmer codes the program and is in the form of mnemonic operation codes and a combination of fixed and free format statements. A program written in this manner which is intended for translation into machine language is called a "source" program.

Program Statements. There are three general types of statements, which are based on the type of operation code, that comprise the source program: (1) Area Definition Statements, which correspond to declarative operation codes, are used to define work areas and input/output areas. (2) Instruction Statements, which correspond to imperative op-codes, specify the job the object program is to perform; these are classified as arithmetic, internal data transmission, branch, and program control instructions. (3) Processor Control Statements, which correspond to the control op-codes, provide the programmer with control over portions of the assembly process (Ref 18:1,3).

For convenience a functional listing of 1620 mnemonic operation codes is included in Table 1 on page 9. Table 2 on page 11 lists the unique mnemonic operation codes that are provided in the Symbolic Programming System.

Table I
Mnemonic Operation Codes

1. Area Definitions

Operation Code	Description
DS & DAS & DSS	Define Symbol
DC & DAC & DSC	Define Constant
DSA	Define Symbolic Address
DSB	Define Symbolic Block
DNB	Define Numeric Blank

2. Arithmetic Instructions

Mnemonic Operation Code	Numeric Operation Code	Description
A	21	Add
AM	11	Add Immediate
S	22	Subtract
SM	12	Subtract Immediate
C	24	Compare
CM	14	Compare Immediate
M	23	Multiply
MM	13	Multiply Immediate
LD	28	Load Dividend
LDM	18	Load Dividend Immediate
D	29	Divide
DM	19	Divide Immediate

3. Internal Data Transmission

Mnemonic Operation Code	Numeric Operation Code	Description
TD	25	Transmit Digit
MF	71	Move Flag
TDM	15	Transmit Digit Immediate
TF	26	Transmit Field
TFM	16	Transmit Field Immediate
TR	31	Transmit Record
TNS	72	Transfer Numerical Strip
TNF	73	Transfer Numerical Fill

4. Branch Instructions

B	49	Branch
BNF	44	Branch No Flag
BNR	45	Branch No Record Mark
BD	43	Branch on Digit
BI	46	Branch Indicator
BNI	47	Branch No Indicator
BT	27	Branch and Transmit
BTM	17	Branch and Transmit Immediate
BB	42	Branch Back

5. Program Control Instructions

K	34	Control
SF	32	Set Flag
CF	33	Clear Flag
H	48	Halt
NOP	47	No Operation

6. Processor Control Operation Codes

Operation Code	Description
DORG	Define Origin
HEAD	HEAD
TCD	Transfer Control and Load
TRA	Transfer to Return Address
DEND	Define END

Table II

Unique Mnemonic Operation Codes

1. Unique Input/Output Mnemonic

OP Code		Description
RNTY	Read Numerically	Typewriter
RNCD	Read Numerically	Card Reader
WNTY	Write Numerically	Typewriter
WNCD	Write Numerically	Card Punch
DNTY	Dump Numerically	Typewriter
DNCD	Dump Numerically	Card Punch
RATY	Read Alphamerically	Typewriter
RACD	Read Alphamerically	Card Reader
WATY	Write Alphamerically	Typewriter
WACD	Write Alphamerically	Card Punch

2. Unique Typewriter Control Mnemonic

TBTY	Tabulate	Typewriter
RCTY	Return Carriage	Typewriter
SPTY	Space	Typewriter

3. Unique Branch Indicators

BH	Branch High
BE	Branch Equal
BNN	Branch Not Negative
BP	Branch Positive
BZ	Branch Zero
BV	Branch Overflow
BXV	Branch Exponential Overflow
BA	Branch Any
BNL	Branch Not Low
BC1	Branch Console Switch 1 ON
BC2	Branch Console Switch 2 ON
BC3	Branch Console Switch 3 ON

3. Unique Branch Indicators (cont.)

OP Code	Description
BC4	Branch Console Switch 4 ON
BNH	Branch Not High
BNP	Branch Not Positive
BNE	Branch Not Equal
BNZ	Branch Not Zero
BNV	Branch No Overflow
BNXV	Branch No Exponential Overflow
BNA	Branch Not Any
BL	Branch Low
BN	Branch Negative
BNC1	Branch Console Switch 1 OFF
BNC2	Branch Console Switch 2 OFF
BNC3	Branch Console Switch 3 OFF
BNC4	Branch Console Switch 4 OFF
BLC	Branch Last Card
BNLC	Branch Not Last Card

Statement Format. Each statement except a comment statement may consist of a label field, an operation code field and an operands field.

A Label Field is used to associate a name with a statement to allow a symbolic reference to the statement. Only statements referred to elsewhere in the program need be labeled.

The Operation Code Field contains the actual two-digit numerical operation code or the mnemonic representation of the operation code to be performed.

The Operands Field is used to specify the information that is to be operated upon. The field will contain symbolic or absolute addresses, area sizes, instruction modifiers, or constants.

Asterisks. In order to eliminate the necessity for too many labels, an asterisk (*) is used for addressing relative to the instruction in which the asterisk is contained.

When the asterisk address is used with either area definition or control statements, it references the low order (rightmost) position of the field last defined. For example the statements

```
TFM START,0  
DC 1,@,*
```

produce the instruction 160187600000/ where START equals 01876 (Ref 5:14).

Address Adjustment. Address adjustment, which is permitted with all addresses, actual, symbolic, or asterisk, is used to direct the processor to adjust the addresses of operands arithmetically. This feature reduces the number of symbols necessary for a source program by providing a means to reference a location a given number of positions away from a specific address. For example in the statements

```
TBTY
DC 1,7,*-5
```

the address assigned the constant 7 is 5 digits less than the address of the low order position of the TBTY statement. The assembled instruction appears as 34 0000700108 (Ref 5:15).

Important Instructions. Instructions that are used quite frequently in the examples and illustrations throughout this thesis are defined below.

The Branch (B-49) instruction causes an unconditional branch to the instruction at the P address, which is the next instruction to be executed. The Q part of the instruction is not used.

The Branch and Transmit (BT-27) instruction accomplishes three things: (1) The address of the next instruction in sequence is saved. (2) The instruction at the P address is the next one executed. (3) The data in the field at the Q address is transmitted to the P address minus one and to successively lower core storage positions.

This instruction is used to branch to subroutines.

The Branch Back (BB-42) instruction causes the computer to branch unconditionally to the instruction at the address saved by the Branch and Transmit instruction. This instruction is used to return from a subroutine.

The Transmit Field (TF-26) instruction causes the data field at the Q address to be transmitted to the field at the P address.

The Transmit Record (TR-31) causes the data at the Q address to be transmitted to the P address and successively higher core storage positions until terminated by a record mark (Ref 6:21-27).

A Define Origin (DORG) statement instructs the processor to override its automatic assignment of storage and to begin the assignment of succeeding instructions at the location specified in the operand.

A Define Constant (DC) statement is used to enter numerical constants into the object program, and to assign names to the constants.

A Define Symbol (DS) statement is used to define symbols used in the source program by assigning storage addresses or values to symbolic addresses or labels. It also assigns storage for input, output, or working areas (Ref 5:17-20,37).

Processor Operation

The processor is the 1620 machine language program which performs the function of translation and assembly. The processor takes the source program in symbolic language, converts the mnemonic codes into machine language codes, assigns addresses in core storage to instructions and symbols, and assembles a machine language program known as the "object" program (Ref 18:2). The general operation of the processor in performing these functions is described below.

The processing of a source program is accomplished in two passes. A statement is read, and if the statement is not a comment the operation code field is identified by a search through the operation code table. Each entry of this table contains the mnemonic code and a code digit to indicate the routine which processes this class of instructions. When the correct op code has been identified a branch to the routine that will process that class of instructions is executed.

During pass I, after the statement has been processed by the appropriate routine and the address counter has been adjusted, a branch is made to the label loading routine. In this routine the label is first tested to see if it is blank, and if it is, a branch to process the next statement occurs. If the label is not blank a search is made of the symbol table. If the label is

already present, it is multiply defined, and the statement is treated as if it had a blank label. If the label is not already present, and space is available in the table, the label is placed in the table together with its assigned address.

During pass II the instruction operands are scanned and assembled by a closed subroutine which operates as follows: The operand field is scanned and the characters are collected and examined. If the characters represent a symbol, the symbol table is searched for equivalence, and if the symbol is not found, the symbol is undefined. If the symbol is present, its assigned address is stored and address adjustment, if designated, is performed. After all symbols in the field have been collected and evaluated, a branch back from the routine occurs, and the instruction is then assembled and readied for output (Ref 17:10-15).

III. General Procedure

The purpose of this chapter is to outline the chief steps of the thesis investigation. The chapter will describe the basic computer programming process and the associated equipment that was utilized in modifying the IBM 1620 SPS Processor Program. Photographs and descriptions of this equipment are included in Appendix A.

Analysis of the Processor Program

The first step in the programming process consists of analyzing a listing of the processor program to determine possible areas of modification. This listing can be obtained from the IBM Program Library or can be printed on the IBM 407 accounting machine from the SPS Processor Source deck. For this thesis project the program was analyzed in terms of the two major areas of investigation that were described in chapter I - to determine how the program could be shortened and its capability increased.

Modification of the Processor Program

After completion of the initial analysis the program changes must be converted to coded instructions and incorporated into the processor program. At this point the basic techniques of computer programming and coding which are described in detail in chapter IV are applied. Since many listings of the program will be made during

the course of the programming process, the number of modifications made on any particular listing is a matter of convenience.

Preparation of the Source Deck for a New Listing

The coded instructions that were prepared in step two must now be punched on IBM cards and inserted in the SPS source deck as modifications to the program. After all desired changes and deletions have been made the SPS source deck can be used to obtain a new listing. If further modifications are planned the listing is made on the IBM 407 and the foregoing procedure repeated until all changes have been incorporated.

Program Assembly

When all modifications have been incorporated into the processor source deck the program is assembled on the computer. Due to the number of symbols used in the modified processor program the IBM 1620 could not be used; consequently all assemblies were performed on the IBM 7090 Data Processing System. The input data consisted of the 7090 processor card deck and the modified SPS processor source deck. Since the input to the 7090 is from tape only, off-line card-to-tape conversions were performed on the IBM 1401 Data Processing System.

The output of the 7090 is a listing of the original input data and the assembled machine language instructions, written on another tape for off-line reproduction. Under

control of the IBM 1401, the IBM 1402 Card Read-Punch and the IBM 1403 Printer are used to convert this tape listing to an output object deck and a printed listing.

The complete assembly process using the IBM 7090 is accomplished by the Analysis Branch, ASNCDA.

7090 Listing

The output listing of the 7090 contains the source statements in SPS format and the machine language instructions and storage addresses of the processor program. Error messages, which are identified by five asterisks, are printed out and precede the statement in error. The symbol table and all undefined and multiply defined symbols are printed out at the end of the listing.

If there are an excessive number of errors in the listing the SPS source card deck should be modified and a new assembly made. If there are few errors, corrections can be made by inserting patch cards in the 7090 output object deck.

Program Checkout

The 7090 output object deck is now loaded into the IBM 1620 computer and standard computer techniques utilized to check out the new processor. The checkout procedures* are used in conjunction with the printed listing obtained

*The checkout procedures are described in detail in chapter V.

from the 7090 to trouble-shoot the processor program. As errors in the program are encountered, corrections are made to the listing by rewriting the necessary coded instructions. When a number of corrections have been accumulated, the modifications should be punched on cards, inserted in the SPS processor source deck and the entire programming process repeated to obtain a corrected object deck.

This process is continued until an operational processor program is obtained that incorporates all the desired modifications and changes.

Write Up

As the processor is being tested the operating procedures and techniques that best incorporate the modifications into a workable program are being formulated. When the optimum combination of convenience, flexibility and capability has been obtained, a list of operating instructions and a description of the modifications in the program are compiled into a reference manual for general distribution at the computer facility.

Program Library

In order to maintain the sequence of the coded statements the final processor program is renumbered using the 1620 Sequence Puncher Program. This program assembles a new source deck that contains the statement numbering

sequence designated by the operator. Since the 1620 output card deck is unprinted, the IBM 557 Alphabetic Interpreter must then be used to print the coded statements on the punched cards. The numbered and printed source deck is then used to obtain a final numbered listing from the 7090 for inclusion in the Program Library.

As an optional enclosure a Label Reference Index can be prepared using a 1620 program written by Lt. Pratt. This program assembles an object deck containing a list of all symbols and the card numbers of every location in the program which refers to each symbol. Due to the number of symbols used in the AFIT Version of 1620 SPS additional memory space was required and the School of Logistics 1620 computer facility, which has 40,000 spaces of core storage, was utilized to assemble the program. A printed listing of the Label Reference Index was prepared from the object deck using the IBM 407.

IV. Methodology

This chapter consists of two parts. The first section describes the concepts, methods, and coding techniques that were utilized to shorten the IBM SPS Processor Program. The second part outlines the computer programming and coding techniques that were utilized to increase the capability of the IBM SPS Processor.

Although these two areas of investigation will be described separately in this chapter, they are closely interrelated. The techniques employed in shortening the processor program are equally applicable to the problem of programming and coding computer routines to increase the capability of the processor. Moreover the recoding procedure, which is used extensively as a shortening technique, is also utilized directly to incorporate major changes into the processor without the necessity of adding complete new routines to the program.

Shortening the IBM SPS Processor

As outlined in chapter II, the function of the processor program is to translate the symbolic language used by the programmer in his source program into the operating machine language of the computer. Since the central limitation of the size of a source program is the number of symbols that the computer can accept, there exists a definite trade-off problem between the size of

the symbol table and the length of the processor program. The essential feature of this problem is that the processor program, which only performs the necessary translation procedures, occupies a substantial amount of memory storage space. The significance of the problem is illustrated in Figure 3 on the next page, which indicates that the processor program occupies approximately 17,500 of the 20,000 memory spaces available in the 1620 Data Processing System. If the processor program could be shortened by modification that would not alter the capability of the processor, additional storage space would be available in the symbol table for programming longer and more complicated problems. The remainder of this chapter will examine the programming techniques utilized to modify the processor program.

The programming techniques that were applied to the IBM SPS Processor Program were employed on the basis of the following criterion: "Given a fairly efficient program written in a straightforward manner, it is usually possible to rewrite the program in fewer instructions, but the rewritten program will require increased execution time." In general however, the percentage of decreased space will be considerably larger than the percentage of increased execution time (Ref 4:2).

Since the limitation of memory capacity for the source program symbol table is the most stringent restriction upon

the SPS programmer, the processor program was rewritten to optimize storage space and the penalty of increased execution time, when it occurred, was accepted. In many cases, however, execution time was actually decreased due to better programming.

<u>Program</u>	<u>Storage Addresses</u>
Arithmetic Tables-----	00000 - 00401
Input/Output Areas, Work Storage, Constants-----	00402 - 01779
Processor Program Instructions-----	01780 - 15403
Input/Output Areas, Work Storage Constants-----	15404 - 15844
Operation Code Table (Mnemonics)----	15845 - 17516
Symbol Table-----	17517 - 19999

Fig. 3

Storage Layout of 1620/1710 SPS Processor

Six different techniques were employed in shortening the processor program. These were: (1) Recoding, (2) Optimum use of all portions of an instruction, (3) Redefinition of origin to optimize storage, (4) Optimum use of programmed switches, (5) Looping, and (6) Subroutine formulation (Ref 11:2-6).

The application of these techniques comprised a substantial portion of the thesis investigation; therefore a detailed explanation of the techniques and an illustration of their application to the IBM SPS Processor will be presented in this chapter.

The subroutine and looping techniques accomplished the most significant results in shortening the processor program. The other methods, although less important, were useful coding techniques that were applied to the processor and to the routines formulated using the subroutine and looping methods. In order that the minor techniques will be recognized and appreciated when they appear in the subroutine and looping illustrative examples, they will be discussed first.

Recoding. This technique consists of altering instruction combinations that satisfy the logic of a particular program or routine. It was possible to conserve memory storage by altering the particular logic and/or utilizing different instructions in a different sequence to accomplish the same function.

This technique was applied to the routine in Figure 4 which used the last digit of the op-code field to branch to the correct routine to process an instruction. These routines accomplish the same function in both processors, but the AFIT Processor utilizes 64 fewer spaces in core storage.

IBM PROCESSOR			AFIT VERSION OF 1620 SPS		
OK	TFM	GOODB+6,BTBL	OK	TFM	GOOD1+11,BTBL
	TD	GOCDB+11,ZEPO+30		TD	GOODB+11,ZEPO+30
	A	GOODB+5,GOODB+11	GOODB	MM	*+9,500,810
GOODB	B	,,10		A	GOOD1+11,99
	B	TRA	GOOD1	TF	GOOD2+6
	DORG	*-1	GOOD2	B	
	D	ADC		DORG	*-4
	DORG	*-1		DSA	MACRO
	B	MACRO		DSA	TRA,INST,BI,BNI
	DORG	*-1		DSA	RDW,K
	B	INST	BTBL	DSA	DSDNB,DAS,DC,DAC,
	DORG	*-1		DSA	DSB,DORG,DEND,
	B	BI			HEADER,WORG
	DORG	*-1			
	B	BNI			
	DORG	*-1			
	B	RDW			
	DORG	*-1			
	B	K			
	DORG	*-1			
	B	DSDNB			
	DORG	*-1			
	B	DAS			
	DORG	*-1			
	B	DC			
	DORG	*-1			
	B	DAC			
	DORG	*-1			
	B	DSA			
	DORG	*-1			
	B	DSB			
	DORG	*-1			
	B	DORG			
	DORG	*-1			
	B	DEND			
	DORG	*-1			
	B	HEADER			
	DORG	*-3			

Fig. 4

Recoding

A second aspect of the recoding technique involves the elimination of the asterisk address adjustment feature from the majority of instructions in the processor. This improved the readability of the processor and made modification and coding simpler; however the number of symbols required was substantially increased. The following routine which handles the typed output for the DSA statements illustrates the application of this technique.

<u>IBM SPS PROCESSOR</u>			<u>AFIT VERSION OF THE SPS</u>		
TYPDSA	BNC1	PCON	TYPDSA	BNF	PCON, PRSW
	TFM	*+47, ZEPO		TFM	B45+11, ZEPO
	WATY	CLERER+45	A22	WATY	CLERER+45
	AM	*+23, 5		AM	B45+11, 5
	TF	TYPADD-1	B45	TF	TYPADD-1
	WNTY	TYPADD-5		WNTY	TYPADD-5
	TF	*+35, *-13		TF	B47+11, B45+11
	AM	*+23, 1, 10		AM	B47+11, 1, 10
	BNR	*+20	B47	BNR	B46
	B	PCON		B	PCON
	DORG	*-3		DORG	*-3

Optimum Use of all Portions of an Instruction. The use of declarative statements and address adjustment allows the assignment of constants and work areas within the unused portions of other instructions.

EXAMPLES: (X indicates an unused position)

<u>SPS</u>	<u>UNOPTIMIZED MACHINE LANGUAGE</u> <u>INSTRUCTIONS</u>
HI TBTY	34 XXXXX X01X8
PICKUP DS 5,*-5	
.	
.	
.	
G30 H	48 XXXXX XXXXX
SEVENS DC 7,7070707,*	
.	
.	
.	
BNC4 A4	47 <u>AAAAA</u> X04XX
CNTR DS 2,*	
.	

In the first example the symbol PICKUP is assigned a position within the unused portion of the instruction TBTY. The five digit area occupies the P address of the TBTY instruction.

In the second example the HALT instruction utilizes only 2 of the 12 machine language digits, consequently seven digits of the instruction are used for defining a constant labeled SEVENS. The resulting machine language instruction would be 48 0007070707.

In the third example the symbol CNTR is assigned the location of the last two digits of the preceding instruction. A one-digit constant could be assigned the

Q₇ position of the instruction since this space is also unused.

Maximum use of this technique, particularly in the modifications that were added to the processor, eliminated unnecessary storage requirements.

Redefinition of Origin to Optimize Storage. This technique allows the unused portion of certain instructions to be eliminated in core storage. All instructions in the IBM 1620 are written in a 12-digit machine language format; however, in certain instructions the Q or P address is not used and a zero (00000) address is generated. A DORG statement (Define Origin) can be used to direct the processor to override its sequential assignment of storage and begin the assignment of succeeding instructions at the address specified in the operand of the DORG statement.

The DORG statement can be used to eliminate the unused portion of the Branch and Branch Back instructions.

```
B      START
DORG *-3
.
.
.
BB
DORG *-9
```

The "B" instruction uses only 7 of the 12 digits in the instruction format; consequently the redefinition of

the origin saves four positions of storage.

The BB instruction uses only 2 of the 12 digits; this allows a saving of ten positions.

Although these are the only two commands which allow this type of redefinition, and the IBM SPS Processor has been written utilizing this feature, this technique was applied successfully to all program modifications.

Optimum Use of Programmed Switches. The IBM SPS Processor used an indicator set to 0 or 1 to branch around those instructions that were not to be executed during pass I or II. The switch, which was 0 during the first pass, was set to 1 at the end of this pass to allow execution of the proper instructions for pass II. In the example that follows, during the second pass the Branch on Digit (BD) statement causes a branch around the instruction B LDLBL since at that time the program switch EJS has been set to 1.

EXAMPLE:

```
BD    PRDS, EJS
B     LDLBL
DORG *-3
PRDS BTM LINPRT, DODS
```

It was possible to optimize this programmed switch by using a record mark in place of the 1 and utilizing the Branch No Record Mark instruction:

BNR LDLBL, EJS
PRDS BTM LINPRT, DODS

This modification saves eight spaces, and since this routine was used quite frequently in the processor, a considerable amount of storage space was saved.

Looping. Looping is the ability to repeat an operation. Loops within a computer program enable the computer to return to an earlier part of a program and repeat certain steps with different input data; this allows the computer to perform long repetitious tasks with relatively short simple sets of coded instructions and consequently provides a means to conserve memory storage space.

The open subroutine printed below provides an excellent example of looping. This routine was added to the processor program to clear the area labeled INPUT prior to reading a statement from an input device.

G15	TFM	SET,0,10
	TF	INPUT-2,CLERER+9
	TF	INPUT+10,CLERER+11
	TF	INPUT+18,CLERER+7
	TFM	AA2+6,INPUT+20
AA2	TFM	,,10
	AM	AA2+6,2
	CM	AA2+6,INPUT+140
	BL	AA2
TYPE	DS	2,*
	BB	
	DORG	*-9

The BL (BRANCH LOW) instruction creates a loop back to the instruction labeled AA2 and allows the computer to repeat that sequence of operations immediately following AA2 as often as needed.

This particular technique proved extremely effective and was utilized extensively in modifying the IBM SPS Processor.

Formulation of Subroutines. A program which performs identical functions at various points within the program can be simplified by subroutining. Using this technique a function is coded only once and referenced freely, each reference affecting the program as though the function were coded completely at the place of reference.

A subroutine is a short sequence of coded instructions which performs a specific task. The subroutine is normally executed several times during the course of the main program and is incorporated into the program by a single coded instruction whenever the operation performed by the subroutine is desired. Since the subroutines are only coded once, memory space is conserved.

The processor program was analyzed to determine if additional subroutines could be formulated and considerable shortening was accomplished by the use of this method. In general, however, the original logic and coding had to be changed in order to create tasks that could be performed by identical procedures.

Figure 5 below is an example of two coded routines from the original processor that performed identical functions with different input data and a slightly different logic, and were designed to produce different results.

LBADD	TFM	*+23,SYMTBL	IT	TFM	*+23,SYMTBL
	BD	LBADDS		BD	SEIFIN
	BTM	EVALER,50000		.	
	DC	1,-,*		.	
LBADDS	TF	*+23,LBADD+23	SEIFIN	TF	*+23,IT+23
	TD	*+35		TD	*+35
	TF	LABCOM+11,*-1		TF	*+71,*-1
	TFM	*+47,,10		AM	*+59,,10
	A	*+35,*-1		A	*+47,*-1
	A	LABCOM+11,*+23		C	LABCTR,SEIFIN+47
	CM	COLL-17		BNE	*+36
	BNE	*+36		C	INPUT3
LABCOM	C	COLL-2		BE	ER10
	BE	LABOK		TF	IT+23,*-13
	AM	LABCOM+11,6,10		AM	IT+23,6,10
	TF	LBADD+23,LABCOM+11		B	IT+12
	B	LBADD+12		DORG	*-3
	DORG	*-3			

Fig. 5

Routines Designed to Search the Symbol Table

These two routines were recoded into a single sub-routine which resulted in reducing the length of the processor by approximately 100 spaces of core storage. The routine as it appears in the AFIT Version of 1620 SPS is printed on the next page.

IT	TFM	A63+11,SYMTBL
A63	BD	SEIFIN
D33	B	
	DORG	*-3
SEIFIN	TF	D24+11,A63+11
D24	TD	D25+11
	TF	D26+11,D24+11
D25	AM	D26+11,,10
	A	D26+11,D25+11
D28	D	LABCTR,D25+11
	BNE	D27
D26	C	INPUT3
D29	BE	BB
D27	TF	A63+11,D26+11
	AM	A63+11,6,10
	B	A63
	DORG	*-3

The subroutine technique can be extended to provide an option to branch from a subroutine to any position of a program rather than to the next instruction in sequence.

In this technique a Branch and Transmit Immediate instruction is used to branch to the desired subroutine. The Q address of the BTM instruction contains the address to which the subroutine may branch upon completion.

Example: Assume that an instruction, BTM CKREC, NASS, which is located in another part of the program, causes a branch to the routine CKREC listed on the next page.

CKREC	TF	BR1+6,*-1
	BNR	BR2,INPUT+22
BR1	B	
	DORG	*-3
BR2	CM	INPUT+22,23,10
	BE	BR1
	BB	
	DORG	*-9

As a result of this branch, the Q address NASS will be stored in the CKREC-1 position.

The TF instruction of the subroutine will transmit the address NASS to the branch instruction BR1+6.

The subroutine will perform the designated checks and depending on the results proceed to Branch Back or to Branch to the routine located at NASS.

Several subroutines were formed in this manner and a considerable saving of storage space was realized.

A third type of subroutine, the multiple use subroutine, also proved quite effective. This type of subroutine permits a BTM instruction to branch to various instructions within the routine, to allow execution of only a portion of the subroutine.

An example of this type of subroutine is given on the next page.

Example:

```

TABBY1  TBTY
        TBTY
        TBTY
        TF    G25+6,TABBY1-1
G25      B
        DORG  *-3
G5       AM    ADDR5,5,10
SPAT     WNTY  ADDR5-4
        SPTY
        BB
        DORG  *-9

```

The following Branch and Transmit Immediate instructions were used to branch to this subroutine:

BTM TABBY1,G5 which allows the complete subroutine to be processed.

BTM TABBY1,*+12 which allows the three TBTY instructions to be executed and causes a branch to the instruction immediately following the BTM instruction.

BT SPAT, SPAT-1 which causes only the last portion of the subroutine to be processed.

A total of six subroutines were formed utilizing all of the techniques described in this chapter. This technique produced the greatest reduction in storage space.

Processor Capability

The second major area of investigation was to increase the capability of the SPS processor by incorporating the necessary coded routines or modifications into the

processor program. Suggestions were available from many sources, and ideas from my thesis advisor, reports from the various 1620 Users Group Meetings, and my own computer experience, were all used as a guide in modifying the program. In the final analysis all modifications were based on my own judgement, the only criterion being the desired result - a flexible, useful, processor program with an extended capability.

The problem of increasing the capability of the processor program was essentially the problem of writing a short computer program or routine to perform the function desired. This routine had to define in complete detail what the computer was to do under every conceivable combination of circumstances with all information fed into it.

The number of coded instructions required to perform a particular function varied according to the nature of the task. Since the computer executes instructions one after another, it was necessary to include in the program appropriate instructions to direct the computer to repeat, modify, or skip over certain instructions, depending on the intermediate results or circumstances.

The techniques described under part I of this chapter were equally applicable to the problem of writing computer routines. The subroutining and looping methods, combined with the other techniques of modifying instructions,

permitted a significant reduction in the number of instructions required to perform a specific function.

The general procedure utilized in preparing the routines was: (1) Establishment of the logical program segments to mechanize the operation to be performed, and (2) Arrangement of the coded instructions to satisfy the program logic.

It should be noted that this sequence of operations was repetitive in nature since the peculiarities of the machine logic often necessitated changes in the program logic.

Six new routines were added to the program that resulted in an increased capability for the processor. These routines provided a means to (1) find the size of memory, (2) perform an address check during pass II, (3) include an additional operation code in the program, (4) have the typewriter space over the seam in the paper while listing, (5) reduce the time required to type out a source statement, and (6) eliminate the necessity for a record mark at the end of a statement when utilizing typewriter input.

In addition the recoding procedure, which was used extensively as a shortening technique, was also utilized to increase the capability of the processor. Major changes were incorporated in many routines in the IBM Processor resulting in the addition of eight features to the processor program.

NAST	BNF	G26, PRSW
	TF	LOPOUT, INPUT-2
	C	LOPOUT, CLERER+9
	BNE	G16
	TBTY	
G19	TF	LOPOUT, INPUT+10
	BD	G17, LOPOUT-11
	TBTY	
ORDER	DC	4, 1, *-4
	B	G18
	DORG	*-3
G16	WATY	LOPOUT-8
	B	G19
	DORG	*-3
G17	WATY	LOPOUT-10
G18	TF	LOPOUT, INPUT+18
	WATY	LOPOUT-6
	BNR	B8, INPUT+20
	B	A49
	DORG	*-3

Fig. 7

Routine to Type Out Source Statement

The routine in Figure 7 gives an example of several of the techniques described in part I of this chapter. This routine was included in the AFIT Version of the SPS Processor to allow the typewriter to tabulate (rather than space) to the proper position for type out of a statement if either the page-line field or the label field were blank. The function and logic of this routine is indicated in the flow diagram of Figure 6.

This routine is an excellent example of the trade-off problem of space, execution time and capability. The routine in the original processor accomplished the type out of the statement with fewer coded instructions, but the method of spacing rather than tabulating when blank fields were present was time consuming. To improve the performance of the SPS Processor additional instructions were added which decreased the computer execution time, and resulted in a faster listing due to the increased speed of the typewriter when tabulating. The increased storage requirement imposed by the additional instructions was a trade-off to obtain a reduction in the order of seconds of computer execution time.

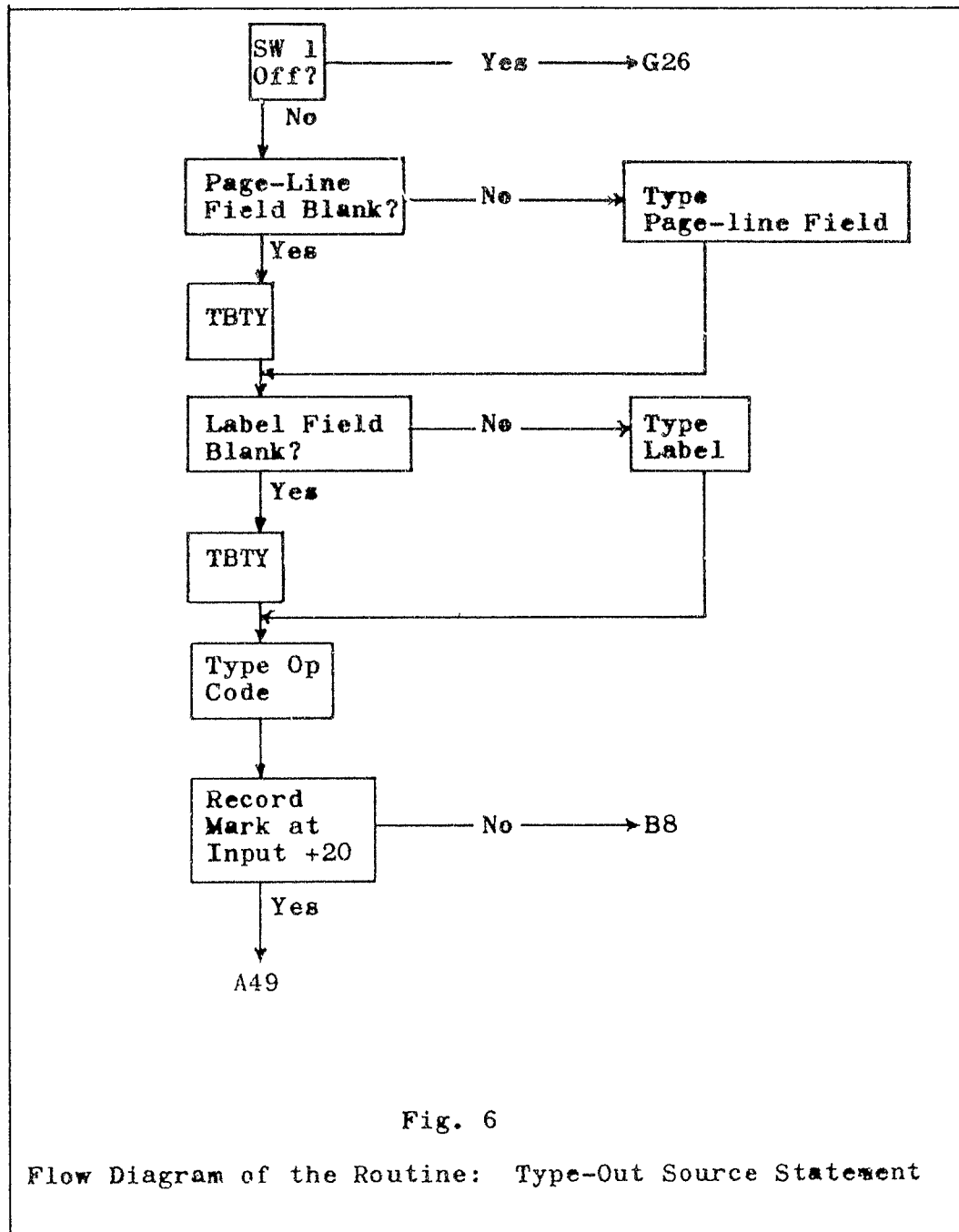


Fig. 6

Flow Diagram of the Routine: Type-Out Source Statement

V. Program Checkout

This chapter will discuss the sixth step of the programming process - checkout of the modified processor program. This step is a major area of investigation, constituting approximately one half of the total time expended on the programming effort, and requiring thorough knowledge of the operating procedures and techniques used to analyze programs in the computer.

An outline of computer operating instructions, equipment, capability, and program testing procedures is included in the IBM Reference Manual A26-4500-2, titled IBM 1620 Data Processing System. No attempt will be made in this chapter to write a definitive study or repetition of this manual; rather, a functional description of those features that proved most valuable to the thesis investigation will be presented. The remainder of this chapter, which is divided into three parts - test requirements, console operation, and debugging techniques - describes these features.

Test Requirements

Adequate checkout of the modified processor program depended on the test of the major individual routines that comprise the processor program. These individual routines were checked out by employing five phases of testing.

(1) Typical flow of the processor, (2) Check of specific routines that handled all instructions containing certain classes of op codes, (3) Error handling procedures, (4) Test of the specific changes and modifications to the processor program, and (5) Final recheck of the complete overall operation of the processor program.

The first phase of testing checked the typical flow of the processor by utilizing a short source program of known configuration to check the input/output routines of the processor. A typical configuration of this short source program is pictured in Figure 8 which shows a listing of the program obtained at the end of phase I.

```

END OF PASS I
01012 *START1 01023 CNTRL
      * INITIALIZATION
          DORG 1000          01000
          RCTY              01000 34 00000 00102
      START1 TFM CNTRL,0    01012 16 01023 00000
      CNTRL DS 5,*         01023 00005
          DEND START1      01012
END OF PASS II

```

Fig. 8
Test Program for Phase I

During Pass I checks were made to determine if (1) statements could be entered from the card reader and the typewriter, (2) error messages would be detected on correct source statements, (3) symbols would be entered into the

symbol table correctly.

During Pass II additional checks were made to determine if (4) the addresses in the statement operands would be evaluated correctly, (5) the type out of the source statements and the assembled instructions was correct, and (6) an uncondensed object deck could be punched.

Major errors were encountered during this phase of the testing and the debugging techniques described later in this chapter were employed extensively. Further checkout of the processor depended on establishing the correct I/O routines in order that all additional errors could be isolated to their respective routines.

Upon completion of phase I testing a check was performed on the specific routines that handled statements according to their class of op-code. The actual coding of the processor simplified this test materially, since only 17 routines process all 116 possible SPS operation codes. These 17 routines are listed in Figure 9 with their respective classes of instructions.

<u>Routine</u>	<u>Instruction</u>
MACRO	All macro-instructions
INST	All arithmetic and internal data transmission, some logic (Branch and Compare) instructions
BI	All Unique Branch Indicator ON MNEMONICS
BNI	All Unique Branch Indicator OFF MNEMONICS
RDW	Input/output instructions
K	Typewriter control instructions
DC	DSC and DC
DSDNB	DS,DSS,DNB
DAS,DAC,DSA,DSB,DORG	One routine for each instruction
DEND,HEADER,MORG,TRA	

Fig. 9

Processor Instruction Routines

All routines were tested by processing the appropriate instruction; where one routine handled multiple instructions one of each type was processed. For example: one arithmetic, one Transmit Field, one Branch, and one Compare instruction were used for testing the routine labeled INST; a DC and a DSC were used to test the DC routine. All statements were processed through the typical flow of the processor using phase I test criteria.

Figure 10 shows the listing obtained from a short program designed to test these instruction routines.

```

*  INITIALIZATION
  DØRG 1000
  START1 TFM CNTR1,1
  CNTR1 DS 5, 1248
  FA START1, CNTR1

  TRA
    AM CNTR1, 1
    ALPHA B START1
    C ALPHA, START1
    BE START1
    BNH START1
    RATY START1
    SPTY
    RCTY
    AREA3 DS 5, *-5
    BLANKS DNB 6
    AREA1 DAS 80
    DELTA DSS 7
    END DC 1,
    NØTE1 DSC 25, NUMBER ØF RECORDS @
    DSA END, ALPHA
    DSB 15, 2
    MØRG 2000
    HEAD X
    END START1

  LØAD SUBRØUTINES

```

01000	16	01248	00000
01000	00005		
01248	00005		
01012	16	02031	01035
01024	49	02000	00000
01031	00001		01000
01038	00005		01248
01042	36	00000	00500
01054	49	00000	00000
01066	11	01248	00001
01078	49	01000	00000
01090	24	01078	01000
01102	46	01000	01200
01114	47	01000	01100
01126	37	01000	00100
01138	34	00000	00101
01150	34	00000	00102
01156	00005		
01167	00006		
01169	00008		
01328	00007		
01335	00001		
01336	00025		
01363	00019		01335
01404	00005		01078
01416	00005		
01424	00015	00002	
02000			
01000			

Fig. 10

Instruction Routine Test Program

The third phase of testing involved checkout of the error handling procedures. Statements containing one of each of the 14 possible errors were processed through the phase I test procedure. Where one error message reflected multiple possible errors, each type of error was processed. The test was designed to check detection of the error, type-out of the proper error message, and proper assembly of the machine language instructions based on the error code. The listing of the program used for checkout of the error handling procedures is shown in figure 11. Errors 9 and 13 were checked separately and are not included in the listing.

The fourth phase of testing was devoted to checkout of the specific modifications incorporated into the program to increase the capability of the processor. Checks were made to determine if they would actually perform the function they were programmed to perform. The specific routines that were checked are summarized in the next chapter under results.

As the routines were being tested the operating procedures that best incorporated the modifications into the processor program were also determined. These procedures became the operating instructions for the modified processor.

Since numerous modifications were added during each phase of testing, a complete recheck of the processor was required during Phase V. All previous test programs

```

*  INITIALIZATION
  DORG 1000
  START1 TFM CNTR1,
  CNTR1 DS 5, 1248
  ENDS TFM START1, CNTR1, 7
  ER 1
  01012 41 00000 00000
  ER 1
  01024 41 00000 00000
  ER 2
  01036 24 00000 01000
  ER 3
  01048 41 00000 00000
  ER 10
  ER 5
  01060 21 01248 00000
  ER 5
  01072 26 00000 02285
  ER 5
  01084 21 00000 01000
  ER 5
  01096 21 00000 01000
  ER 5
  01108 26 00000 02285
  ER 6
  01124 00005 02185
  01136 00005 02186
  01148 00005 01735
  01160 00005 01787
  01172 00005 01935
  01184 00005 01986
  01196 00005 02037
  01208 00005 01060
  01220 00005 01084
  01232 00005 01036
  ER 7
  01684 00050
  ER 8
  01734 00050
  ER 8
  01735 00050
  ER 8
  01787 00050
  ER 8
  01935 00050
  ER 8
  01985 00050
  ER 8
  01986 00050
  ER 8
  02037 00050
  ER 8
  02185 00050
  ER 8
  02186 00050
  ER 8
  02285 00050
  ER 8
  02287 00050
  02386 26 01985 02285
  ER 10
  ER 12
  02398 49 01000 00000ER 14
  02410 49 01000 00000ER 14
  02422 49 01000 00000ER 14
  02434 49 01000 00000ER 14
  02446 49 01000 00000ER 14
  01000

  DSB 15
  DC 52,
  C DSC 52,
  D DAC 52,
  E DNB 52,
  STOP DC 5
  F DSC 2,
  G DAC 4,
  A DC 4, 12345
  B DSC 4, 12345
  SCAN DC 5, 123456
  DAC 5, STOP
  START1 TF STOP.SCAN
  HEAD -
  TIP$ B START1
  TIP* B START1
  TIP- B START1
  TIP, B START1
  123 B START1
  DEND START1
  END OF PASS11

```

Fig. 11

Error Handling Procedure Test Program

* INITIALIZATION		
	DLRG 1000	01000
START1	TFH CNTR1,0	01000 16 01215 00000
	TFH CNTR2,0	01012 16 01263 00000
	TFM A1+6,10000	01024 16 01102 10000
	TFH B1+11,10001	01036 16 01119 10001
	TFH A2+6,10001	01048 16 01318 10001
	TFH B2+11,10001	01060 16 01359 10001
	BLC *+12	01072 46 01084 00000
START2	RACD AREA1	01084 37 01589 00500
A1	TR 10000,AREA1-1	01096 31 10000 01588
B1	BNR AREA2,10001	01108 45 01504 10001
	AM CNTR1,1	01120 11 01215 00001
	AM A1+6,2	01132 11 01102 00002
	TF AREA3,B1+11	01144 26 01198 01119
	AM B1+11,2	01156 11 01119 00002
	BNLC START2	01168 47 01084 00500
	TF AREA4,CNTR1	01180 26 01246 01215
	RCTY	01192 34 00000 00102
AREA3	DS 5,*-5	01198 00005
	DC 1,0,*-4	01199 00001
	CF AREA4-4	01204 33 01242 00000
CNTR1	DS 5,*	01215 00005
	WATY NOTE1	01216 39 01749 00100
	WNTY AREA4-4	01228 38 01242 00100
	RCTY	01240 34 00000 00102
AREA4	DS 5,*-5	01246 00005
	DC 1,0,*-4	01247 00001
	CF AREA3-4	01252 33 01194 00000
CNTR2	DS 5,*	01263 00005
	WATY NOTE2	01264 39 01787 00100
	WNTY AREA3-4	01276 38 01194 00100
	SM B1+11,2	01288 12 01119 00002
	RCTY	01300 34 00000 00102
A2	WATY 10001	01312 39 10001 00100
	RCTY	01324 34 00000 00102
	RCTY	01336 34 00000 00102
B2	BNR AREA5,10001	01348 45 01540 10001
	C B1+11,B2+11	01360 24 01119 01359
	BE END	01372 46 01564 01200
	AM B2+11,2	01384 11 01359 00002
	TF A2+6,B2+11	01396 26 01318 01359
	AM CNTR2,1	01408 11 01263 00001
	TFM CNTR1,0	01420 16 01215 00000
A3	C CNTR2,CNTR1	01432 24 01263 01215
	BNH A2	01444 47 01312 01100
	SPTY	01456 34 00000 00101
	SPTY	01468 34 00000 00101
	AM CNTR1,1	01480 11 01215 00001
	B A3	01492 49 01432 00000
AREA2	AM B1+11,2	01504 11 01119 00002
	AM A1+6,2	01516 11 01102 00002
	B B1	01528 49 01108 00000
AREA5	AM B2+11,2	01540 11 01359 00002
	B B2	01552 49 01348 00000
END	H	01564 48 00000 00000
	B START1	01576 49 01000 00000
AREA1	DAS 80	01589 00020
NOTE1	DAC 13,NUMBER OF RECORDS	01749 00019
NOTE2	DAC 30,ADDRESS OF FINAL RECORD MARK	01787 00030
	QEND START1	01000
END OF PASS11		

Fig. 11a
Phase V Overall Operation Test Program

were rerun and an additional program to test the overall operation of the processor was assembled. A condensed and uncondensed object program were punched and the condensed object deck was used to process data. Figure 11a is a listing of this program.

Console Operation

The operator's console, which is an integral part of the central processing unit, provides for manual and automatic monitoring and control of the system. For monitoring, the console provides small neon light indicators that display the contents of core storage, internal registers, and the machine and program status. The most important of these indicators are described below.

The Operation (OP) Register indicator consists of two lines of five lights each which display the bit configuration of the operation code in the last instruction executed.

The Memory Address Register (MAR) is a bank of five lines of five indicator lights each which can display the bit configuration of the address in any one of the eight MARS registers. The MARS registers are non-addressable intermediate storage positions that control data flow and the addressing of core storage, and through the MAR display bank provide a visual indication of the internal data flow

of the computer. The operation code of an instruction determines the functions to be performed by the registers and designates the particular register to be used. The most frequently displayed registers are: (1) Instruction Address Register 1 (IR-1) - contains the address of the next instruction to be executed, (2) Product Address Register 1 (PR-1) - saves the address of the next instruction in sequence when the Save Key is operated, (3) Instruction Address Register 2 (IR-2) - saves the return address when BT and BTM instructions are executed, (4) Operand Address Register 1 (OR-1) - contains the Q address of the instruction indicated in the OP register after the I - cycle of the instruction, and (5) Operand Address Register 2 (OR-2) - contains the P address of the instruction in the OP register after the I - cycle of the instruction (Ref 6:60,71).

The MARS Display Selector is an eight position rotary switch that permits selection of any of the eight MARS registers for display in MAR.

The High/Positive (H/P) and the Equal/Zero (E/Z) check lights show the condition of their respective internal control gates as a result of the last arithmetic or compare operation.

Control keys are provided for alteration of certain machine functions and for convenient instruction entry. Signal lights are associated with some of the control keys

to indicate which key was last activated.

The Display Mar Key causes the MARS register to which the MARS Display Selector is set to be displayed in the MAR bank of indicating lights.

The Insert Key places the 1620 in automatic mode and activates the typewriter keyboard. This permits numeric instructions to be entered into core storage starting at 00000 and extending to higher numbered positions. The Release Key terminates the typewriter input operation and returns the 1620 to the manual mode.

The Stop/SIE Key stops the computer in the manual mode at the completion of the instruction being executed. Thereafter each depression of the key will cause a single instruction to be executed.

The Instant Stop/SCE Key causes the machine to stop while executing an instruction at the end of the 20-microsecond machine cycle in progress. Further depression of the key will cause the machine to step through single machine cycles.

The Save Key saves the address of the next instruction in sequence by storing the address in PR-1 (Ref 6:51-58).

Since the proper use of these indicators and control keys depends on the mode of operation of the computer a general understanding of this feature of the 1620 is required. The most important points are summarized below:

The 1620 computer can operate in either the automatic

or manual mode. In the manual mode the computer has terminated all operation and is ready to accept operator instructions. When the manual mode is initiated the Manual Light comes on and the program stops running. This occurs after: (1) a Halt instruction, (2) a Stop Key or SIE operation, (3) a Check Stop, (4) an Instant Stop or a SCE operation (automatic light is also on), and (5) depression of the Release Key to end a Read Typewriter instruction or Insert operation.

The manual light is turned off when the Start Key or Insert Key is depressed.

When a program is running the computer is in automatic mode and the automatic light is on. This condition exists during the following conditions: (1) when the Start Key or Insert Key is depressed, (2) when a Read Typewriter instruction is being executed, (3) when single cycling or if the program was stopped in the middle of an instruction by the Instant Stop Key, and (4) when running normally. While the computer is in the automatic mode the Display MAR, Save, Insert or Start operations cannot be executed (Ref 12:16-17).

When the computer is running, the lights on the control panel flicker. If the lights are not flickering the computer is stopped and one of several possible conditions could exist. If the computer stops running without displaying an error indicator, these conditions

would normally be (1) a programmed Halt, indicated by a 48 in the operation register, (2) the program waiting for information to be entered, indicated by a 36 or 37 in the operation register, (3) an illegal input/output device specified. This is indicated by a 38 or 39 in the operation register in combination with digits other than 01 or 05 in the Sense and Branch display indicator, or (4) a record mark at an address specified for output data. If the operation register contains an output code, a record mark (bit configuration C-8-2) displayed in the Memory Data Register would indicate an output instruction (WN for instance) had addressed a record mark. As another possibility, the computer should be checked to see if it is in automatic mode, since the system may actually be running in a very short loop. A programming error that failed to provide the proper conditional branch could cause the machine to hang up in a loop indefinitely (Ref 12:11,15).

Indicator check lights are provided on the console for monitoring the internal and input/output data flow of the computer. These indicators are used to detect parity errors within the computer and can stop computer operation. A description follows:

When the computer stops because of a parity check the Check Stop Light comes on. This condition is caused by (1) Read Check (RD CHK) or Write Check (WR CHK) Light coming on when the I/O switch is set to Stop, (2) Memory Buffer

Register-Even (MBR-E) or Memory Buffer Register-Odd Check Light coming on when the Parity switch is set to Stop, and/or (3) Memory Address Register Storage (MARS) Check Light coming on; this causes an unconditional machine stop regardless of the Parity switch setting. When the Check Stop light is on one or more of these indicators that actually caused the stop is also on. Two other means of stopping computer operation are (4) the Overflow Arithmetic (ARITH CHK) Check light when the Overflow switch is set to Stop, and (5) the Reader No Feed or Punch No Feed Light (Ref 6:51-57). The use of some of these indicators is explained below (Ref 6:51-57).

If the WR CHK light and either the MBR-E or MBR-O light are on, memory has a bad character. If the RD CHK light and either the MBR-E or MBR-O light are on a bad character has been read into memory. When the MARS check light is on, either a digit in MARS has a parity error or there is an illegal 5-digit address present in the register. A MARS check will also occur if two Branch Back instructions occur without a Branch and Transmit instruction intervening.

Debugging Techniques

As indicated in chapter III, program checkout commences when the modified processor object deck, which was assembled on the 7090, is loaded into the IBM 1620 computer. From this point the computer console is used in conjunction

with the printed listing from the 7090 to checkout the program in the computer.

The general checkout technique employed in this investigation utilized standard 1620 operating procedures in conjunction with the light indicators and control keys located on the computer console.

The initial checkout procedure was to allow the modified processor to process a short source program of known configuration, the essential idea being to check the typical flow of the processor program.

Operating errors in the modified processor program were determined by allowing the processor to process the source test program until a Check Stop forced a machine halt or until an incorrect output was obtained. Using this technique the majority of program errors encountered were found to be attributable to two primary problems. First, Transmit Field (TF) and Transmit Record (TR) instructions, because of a canceled flag or record mark in core storage, often erased a portion of the processor program at another location. Second, modification of the processor program for one purpose often had hidden higher order effects on some other process or routine in the program. The remainder of this chapter will discuss the debugging techniques used to analyze the major ramifications of these two problems.

The first of these problems resulted in the frequent

occurrence of the Check Stop and consequently led to the development of a general trouble-shooting procedure to deal with program errors of this nature. Since this procedure is a general trouble-shooting method and applicable to most SPS programs, the procedure is described in detail below so that it may serve as a reference for the inexperienced trouble shooter. It is essentially a compilation of standard console operating procedures that have been modified to meet the requirements of this investigation. The procedure is written from an operational point of view so that the technique of applying the standard console procedures as trouble-shooting aids can be fully appreciated.

Check Stop. When the Check Stop Light comes on the other indicator check lights should be examined to determine the type of check stop that occurred. Depending on switch settings the RD CHK, WR CHK, MBR-E and MBR-O lights should be scanned, and since the check stop is frequently a MARS CHK, the MAR display bank should be observed for content.

Scan the Operation Register. The operation register should be scanned to determine the op code of the last instruction executed. If the op code is invalid the immediate cause of the check stop is known, but the cause of the invalid op code remains to be determined. As indicated earlier the most frequent cause of an invalid

op code was due to a TK or TF instruction that caused data to cancel or replace the original instructions.

Determine Storage Address. The storage address of the last instruction should be determined next. This can be done by setting the MARS Display Selector to IR-1 and pressing RESET and Display MAR. Before pressing RESET the other indicators such as H/P and E/Z should be examined since they will be turned off by the RESET key. Now observe the address appearing in the MAR bank of indicator lights and subtract 12 from this number. The result is the address of the last instruction executed.

Determine Stored Data. The actual data located at the address just computed should be printed out on the typewriter for comparison with the listing. The procedure for printing storage data on the typewriter is as follows: (1) Press Insert, (2) Type 35 XXXXX 00100 where XXXXX is the storage address just determined. This causes data starting at XXXXX to be written numerically on the typewriter until location 19999 is printed or the release key is depressed. Occasionally it is desirable to start the type out at an address preceding the desired information to determine the extent of any erroneous field that may be present, and (3) Depress Release and Stop to execute step (2) (Ref 6:59).

Compare Actual Data and Listing. The data that was printed out on the typewriter should be compared with the

machine language instructions on the listing. If the fields are not identical, the SPS statements on the listing should be analyzed to determine which instruction may have caused the erroneous field to be present at this particular location. If this can not be determined from the listing trouble-shooting will have to continue as described below.

Isolating the Error. The simplest way to isolate the instruction causing the transfer of the incorrect data is to insert a digit with bad parity into the location receiving the incorrect data. When a TF or TR instruction attempts to transfer data into this location and the Parity switch is in the Stop position, the bad character will cause a check stop.

The basic procedure is as follows: (1) When the Check Stop occurs display IR-1 and determine the address of the instruction last executed, (2) Press Insert and enter a bad character (H) into an even numbered storage position located in the instruction just determined, and (3) Reprocess the last statement; when the Check Stop occurs, the address of the TF or TR instruction causing the transfer of incorrect data can be obtained by displaying IR-1 and determining the address of the last instruction executed.

A slower, more time consuming method for isolating an error is simply to process the statement through a

portion of the program before examining the location being altered. In this manner the approximate location of the instruction that is causing the transfer of incorrect data can be isolated.

A useful technique is to use the typewriter Program Alteration and Data Entry procedure to insert a Halt (48) instruction at selected positions in the processor program. Statements can now be processed normally; when the computer stops because of the Halt instruction, the statement can continue to be processed, one instruction at a time, by use of the Stop/SIE Key. The area being altered can now be periodically examined by the following procedure which accomplishes a type out of the stored data and a branch to the next sequential instruction: (1) Depress Stop/SIE, Save, Insert. The address of the next instruction in sequence is saved in PR-1 by depressing the Save Key. (2) Type 35 XXXXX 00100 42. (3) Depress Release and Start. Step 2 is executed and the data in core storage starting at XXXXX is typed out. (4) Depress Release and Start. The type out is halted, a Branch Back (42) to the address saved in PR-1 is executed and processing resumes (Ref 6:59).

Error Correction. When the statement causing the error has been isolated the erroneous data in core storage will have to be corrected. If much of the processor program has been canceled, the processor should be re-loaded into core storage. A few instructions can best be

entered from the typewriter using the Program Alteration and Data Entry procedure: (1) Press Insert. (2) Type: 36 XXXXX00100, (3) Depress Release and Start. The computer executes step 2 which instructs the computer to read numerically data entered from the typewriter into a location starting at XXXXX. (4) Type the correct data and press Release (Ref 6:58). All error corrections should eventually be entered on patch cards if the processor is to be reloaded at a later date. Major modifications will probably require correction of the SPS source deck and another assembly of the processor object deck on the 7090.

Reprocess the Last Statement. The statement which caused the Check Stop light to come on should now be reprocessed. The simplest procedure is to return to the location in the program where the Check Stop occurred. This can be done by pressing Insert, typing 49 YYYYY, where YYYYY stands for the storage address of the last instruction executed, and then depressing Release and Start. If major corrections were made in the processor, however, the test program may have to be completely rerun.

Miscellaneous Techniques. Several debugging techniques that are quite useful, but were not systematically employed in the general trouble-shooting procedure are described below.

The P and Q addresses of an instruction can be

displayed on the MAR indicator bank by: (1) Depressing Stop/SIE key until the instruction that contains the desired address is next. (2) Depressing the Instant Stop/SCE key eight times and then Reset once. (3) Turning the MARS Display Selector to OR-1 and depressing the Display MAR key. The Q address which is in OR-1 is displayed in the MAR bank. (4) Turning the MARS Display Selector to OR-2 and depressing the Display MAR key. The P address which is in OR-2 is displayed in the MAR bank (Ref 6:59). In most cases it was simpler to print the core storage data out on the typewriter using methods previously described.

A technique for determining a branch from a loop routine was helpful in isolating errors in the processor program. The result of compare and arithmetic instructions can be determined by observing the H/P or E/Z indicator lights. If the Stop/SIE key is being used to process a statement one instruction at a time, execution of a conditional branch after the compare or arithmetic instruction can then be anticipated to determine the completion of the loop routine. For example, a Branch Equal instruction after a compare instruction would be executed if the E/Z indicator light came on during the compare instruction.

Another useful technique is the procedure to determine whether a program has branched to a subroutine. Since the IR-2 register is normally blank and is used for the "BB" address, if this register contains a valid address,

the program is probably somewhere between a BT and BB (Ref 12:15). As illustrated in chapter IV, however, some subroutines function without using a BB. In that case, even though the program was not in the subroutine, IR-2 would still contain an address. Consequently IR-1 should be displayed first and if this address proves to be in a subroutine, IR-2 would then tell where the subroutine was entered from.

Let us now examine the second major checkout problem which concerns the higher order effect of modifications. The effects of this problem were primarily reflected in incorrect outputs that were many times removed from a specific modification. The general trouble-shooting procedure just described was extensively employed, but modified for the specific errors being investigated. Many minor errors were encountered, but the modifications that had the most far reaching effects are described below.

Modifications that incorporated the ability to enter a symbol during the second pass presented major trouble-shooting problems. By a series of related instructions, the original modification resulted in an incorrect output for all macro instructions. A detailed step by step analysis of this routine revealed that the operation of a single instruction transferred the wrong information into the area that was to be typed out for the listing of the assembled macro instruction. Further analysis

indicated that an output work area, that had originally been performing a different function for each pass, was now being forced to accept data for both functions during the second pass. A redefinition of the work area corrected this particular problem.

Major trouble-shooting problems also arose due to the alteration of the routines to search the symbol table for equivalence. Incorrect error messages were typed due to the alteration of program logic within the routines that branched to the subroutine searching the symbol table. After extensive trouble-shooting the program logic was modified and the errors were eliminated.

A third major problem arose due to the alteration of the routine that effected a branch to the proper routine for processing each class of instruction. The immediate noticeable effect was the incorrect type out of the assembled instruction during a listing. Investigation revealed that a change of the individual entries in the op code table was required in order to provide op code fields compatible with the modifications in the routine.

VI. Results, Conclusions and Recommendations

The improved IBM 1620 SPS Processor with its reduced memory storage requirements and its increased capability as outlined in this chapter has been designated the AFIT Version of 1620 SPS.

This chapter is a summary of the features and changes that have been incorporated into the AFIT Version of the 1620 SPS Processor. These modifications are the result of the application of the techniques described in chapters III, IV, and V to the IBM 1620 SPS Processor Program. A complete detailed description and operating instructions for the AFIT Version of 1620 SPS are included in the appendix.

Results

Two new macro instructions that were written by Lt. Pratt and added to the IBM 1620 SPS Processor now in use at the Institute of Technology have been incorporated in the AFIT Version of 1620 SPS. These instructions are designated (1) INC - Input Conversion, (2) OUTC - Output Conversion and provide for the conversion of floating point numbers from the internal form to the external form, and vice versa.

The following features which have been incorporated into the AFIT Version of the SPS Processor were outlined

and partially coded by Lt. Pratt. Analysis, modification, and complete checkout of the procedures were performed by the author to consolidate the program and to secure compatible operation of the indicated routines with the AFIT Version of 1620 SPS:

1. A new pseudo-op designated MORG, which allows the programmer to exercise more control over the addresses assigned by the processor, was added to the program.

2. A record mark is not required at the end of a statement when utilizing typewriter input.

3. After 60 lines of typing, a skip over the break in forms will be accomplished by the execution of six carriage returns.

4. The AFIT Version of 1620 SPS will automatically adjust itself to the size of memory; therefore, no modification of the processor card deck is required when additional storage is provided by the IBM 1623 Core Storage Unit.

5. The IBM 870 Document Writing System can be used to make an SPS listing from an SPS object deck. The format is similar to the typewriter listing on the 1620 console. Although this feature had been incorporated into the SPS processor now in use at the Institute of Technology, the procedure was modified and recoded and the ability to preserve the page-line field was incorporated.

6. The error message "adjustment count" has been renumbered to start at one instead of zero if an error occurs before a label has been defined.

The following features are the routines and procedures that were analyzed, coded and checked out by the author for incorporation into the AFIT Version of the 1620 SPS Processor Program:

7. An additional error check has been added and the error 10 message has been redefined to account for this check.

8. An undefined symbolic address, as a result of misspelling or omission, can be defined during pass II and placed in the symbol table. Detailed error correction procedures have been included in the writeup of this feature.

9. The effects of errors on the assembly process with program switch 2 OFF have been altered for error messages 1,3,5 and 11.

10. The symbol table is printed at the end of pass I rather than pass II.

11. With switch 1 ON for a listing on the console typewriter during pass II, if either the page-line field and/or the label field are blank, the typewriter will tabulate rather than space to the proper position for type out of the statement. In addition a space is inserted between the page-line field and the label field during

type out of the listing.

12. When a source deck is being punched during pass I and statements are being entered from the console typewriter, if switch 1 is turned ON to complete entry of the source statements from the card reader, the last entry from the typewriter will be punched in the source deck being prepared.

13. The procedure for the use of switch 4 to punch an object program has been altered.

14. If the processor is halted during either pass for any reason, it is possible to branch to the beginning of pass I by pressing RESET, INSERT, RELEASE, and START.

15. Complete operating procedures and instructions have been included in the writeup of the AFIT Processor.

Conclusions

The AFIT Version of the 1620 SPS Processor Program is a significant improvement of the IBM 1620 SPS Processor. Fifteen additional features have been added and the operating procedures have been altered to provide increased flexibility and convenience. The Processor has been shortened 699 spaces resulting in an extension of the symbol table from 2482 to 3181 memory storage spaces. This constitutes a 28 per cent increase in the size of the symbol table. Complete checkout of the program has been accomplished and detailed operating instructions have been prepared that should allow

this program to be utilized at the Institute of Technology's 1620 computer facility at an early date.

Recommendations

The AFIT Version of the 1620 SPS Processor Program is not compatible with the IBM 1620 subroutine deck. Although it is estimated that only minor modifications are required in the subroutine deck, completion of this work would greatly enhance the value of the AFIT Processor.

The computer facility at the Institute of Technology has recently been modified for several special features including indirect addressing. It may be possible to recode the SPS processor utilizing the indirect addressing feature to save considerable memory storage space and time. This possibility should be investigated and accomplished if feasible.

The final checkout of the processor revealed the presence of three undesirable features. These features can be eliminated by several minor modifications to the processor program. These are discussed below.

Unnecessary typewriter carriage returns and tabulations occur during pass II with switch 1 off in the type out of error messages 6, 7, and 8. The neatness of the listing is not affected by this typewriter operation and the addition of two instructions to the program will eliminate this feature.

During a listing on the console typewriter the storage

addresses of the symbols defined in a DSA (Define Symbolic Address) statement are not consistent with the designated length of the symbols. It is believed that a coding error in the output routine for this class of instructions is responsible for this inconsistency.

In the Load Label routine during pass II, if an EK10 address check is not indicated the label is again loaded into the symbol table. Since the symbol would have already been entered during pass I, this is an unnecessary duplication and computer execution time can be saved by recoding the routine. This modification can be incorporated by altering card number 26585 in order to cause a Branch Equal to D34 rather than G11.

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Appendix A
Facilities and Equipment

Appendix A contains photographs and descriptions of the facilities and equipment that were used in the course of this thesis investigation. Extensive use was made of the 1620 computer facility at the Institute of Technology, and the 7090 computer facility of the Analysis Branch, ASNCDA.



Fig. 13
1620 Data Processing System

The IBM 1620 Data Processing System is a small scientific computer designed for universities and small engineering consultant firms. The AFIT facility houses two units - the IBM 1620 Central Processing unit (which contains the computer, 20,000 positions of core storage, and an I/O typewriter) and the IBM 1622 Card Read-Punch unit which is available for card I/O operations.

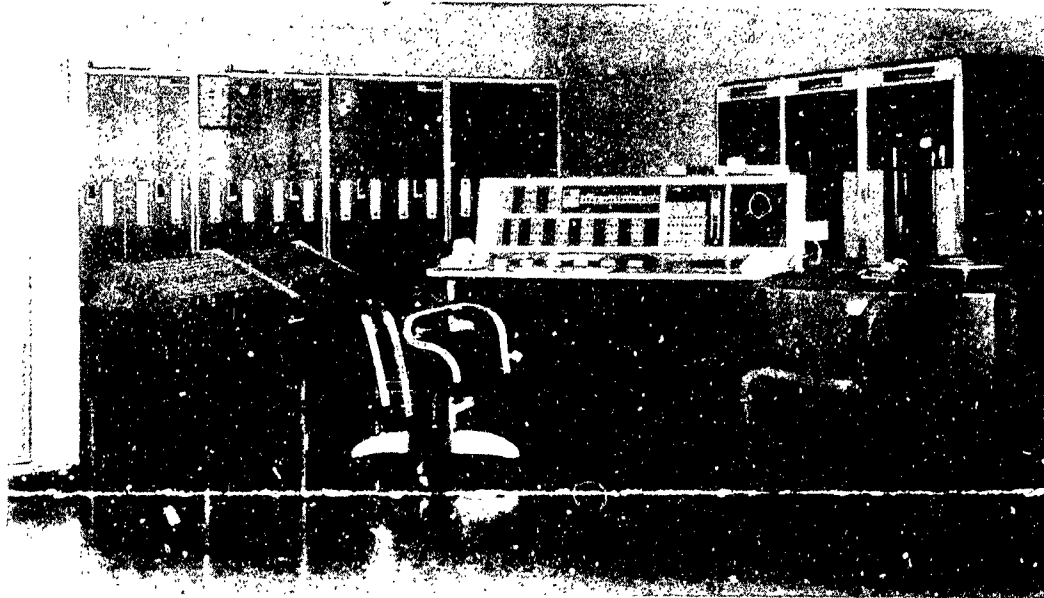


Fig. 14
The IBM 7090 Data Processing System

The IBM 7090 Data Processing System is a large scale high speed scientific data processing system. Input is from tape prepared in an off line card-to-tape prepared operation on the IBM 1401. The 7090 was used to assemble the modified processor program. The output was the SPS source statements and the assembled instructions written on tape to be listed off-line on the IBM 1401.



Fig. 15

The IBM 1401 Data Processing System

The IBM 1401 Data Processing System is used as an auxillary system for the IBM 7090 Data Processing System. This unit receives the tape output of the IBM 7090 and in an off-line operation controls the IBM 1403 Printer and the IBM 1402 Card Read-Punch output media which have respective rated outputs of 600 lines and 250 cards per minute. The 1401 is used to obtain a printed listing of the SPS source statements and their assembled machine language instructions, and a processor object card deck.

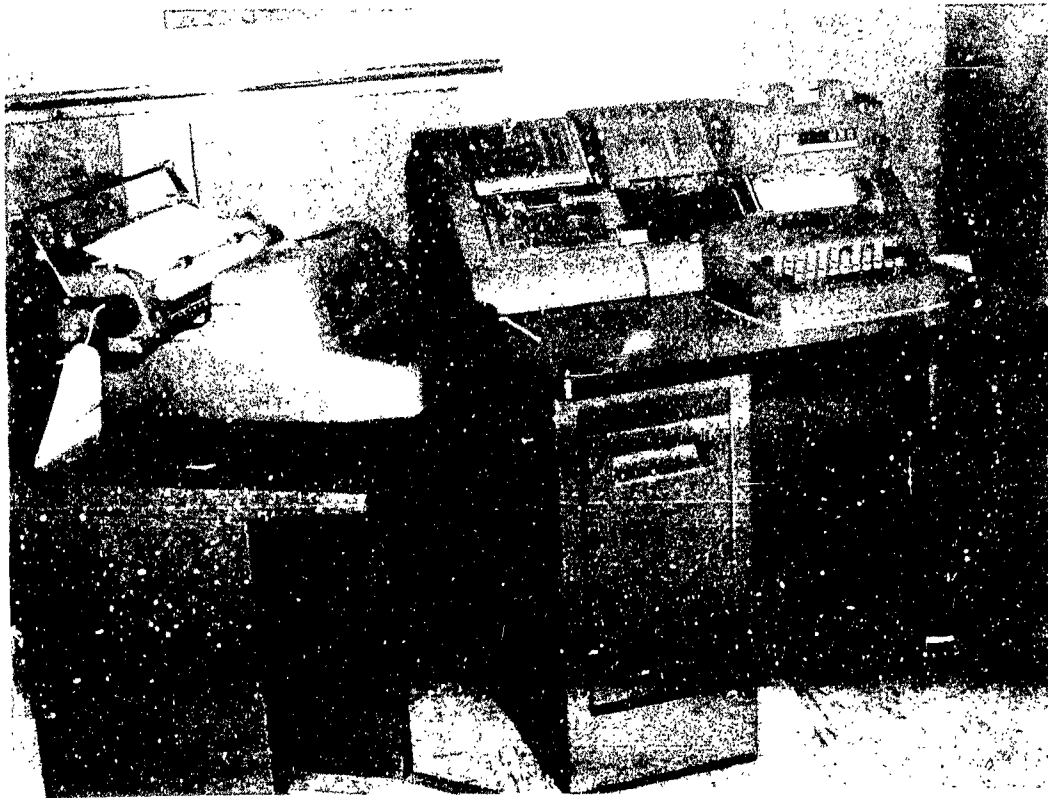


Fig. 16

The IBM 870 Document Writing System

The IBM 870 Document Writing System is a data transfer device. The AFIT facility houses the 836 Control Unit for use as a card punch, and one 866 Non-Transmitting Typewriter for use as an output listing station.

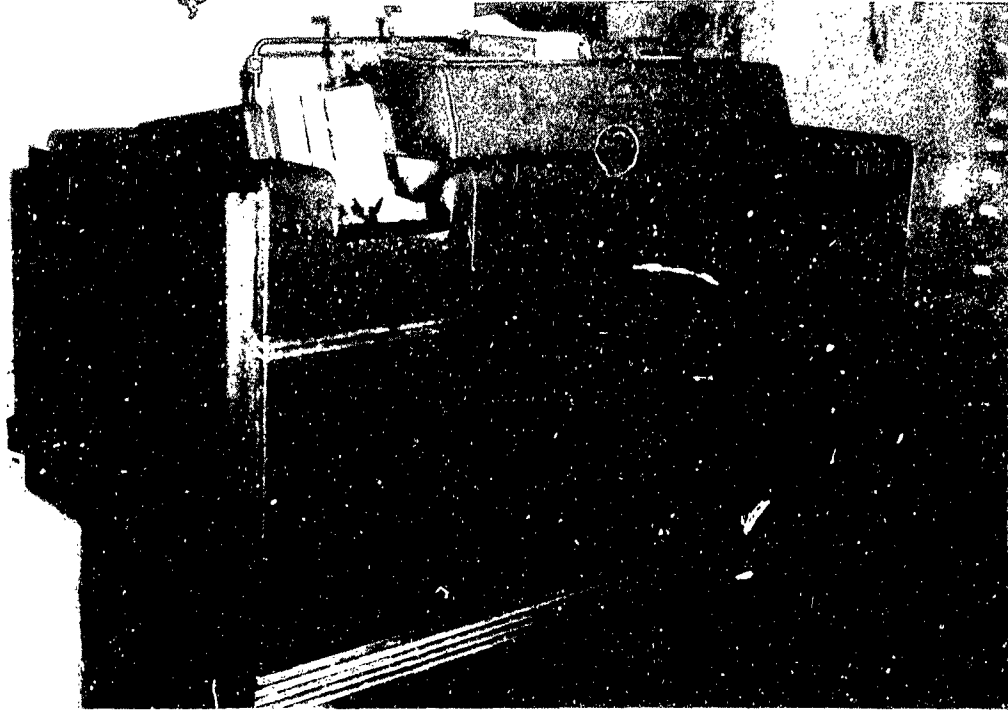


Fig. 17

The IBM 407 Accounting Machine

The IBM 407 Accounting Machine prepares printed listings from IBM cards. The 407 prints 18,000 characters a minute and reads IBM cards at the rate of 150 per minute. This unit is used to obtain a listing of the processor program in standard SPS format.

Appendix B

AFIT VERSION OF 1620 SPS

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AFIT VERSION OF 1620 SPS

I. Introduction

This writeup is intended to serve as a reference text for the AFIT Version of the IBM 1620 Symbolic Programming System. It is assumed that the reader is familiar with the data handling methods and the functions of instructions in the 1620 Data Processing System. This information is available in the IBM Reference Manuals, 1620 Data Processing System, form A26-4500-2, and the IBM 1620/1710 Symbolic Programming System, form C26-500.

II. Description of the Program

The AFIT Version of 1620 SPS is an improvement of the IBM 1620 Symbolic Programming System. A detailed description of the specific modifications is included in the body supplement; for convenience the principal improvements are summarized below.

1. The size of the symbol table has been increased from 2482 to 3181 spaces of core storage. This constitutes a 28 per cent increase in the size of the symbol table.

2. An SPS object deck can now be listed on the IBM 870 in a format similar to the typewriter output listing of the 1620 console.

3. Symbolic labels on all statements can be defined and placed in the symbol table during pass II as well as Pass I.

4. The effects of errors on the assembly process with program switch 2 off have been altered for error messages 1,3,5, and 11.

5. Two new macro instructions designated (1) INC-Input Conversion, and (2) OUTC - Output Conversion have been added to provide for conversion of floating point numbers from both the internal form to the external form and the reverse.

6. A new pseudo-op designated MORG, which allows the programmer to exercise more control over the addresses assigned by the processor, has been added to the program.

7. Typewriter input, output, and correction procedures have been altered to provide increased convenience and flexibility.

8. All operation codes that were exclusively for use with the 1710 or for paper tape input/output have been eliminated from the program. Most non-unique input/output instructions have also been omitted.

III. Program Configuration

This program has been written for the IBM 1620 Data Processing System with 20,000 digits of core storage and for use exclusively with the 1622 card reader punch. The program automatically adjusts to the size of core storage and is compatible with the 1623 Core Storage Unit.

This program utilizes no special features but is

compatible with a computer which has these special features.

The program as of this writing is not compatible with the IBM 1620 subroutine deck. It is anticipated, however, that only minor modifications in the subroutine deck will eliminate this discrepancy.

IV. Operation of the Processor

The AFIT Version of the 1620 SPS card processor is a two pass program. The input for both passes is provided by a source program written in the symbolic language of the SPS.

The two major changes to the basic functions of the IBM SPS processor during pass I and II are: (1) The symbol table will be printed at the end of pass I rather than pass II, and (2) Symbolic labels can now be placed in the symbol table during pass II. The functions of pass I and II are described below.

During pass I the processor (1) checks mnemonic operation codes for validity, (2) prepares a table of symbolic labels and their assigned addresses for use during the second pass, (3) assigns storage positions in memory to constants, instructions, and work areas, (4) performs error checks on the source statements and produces error messages, and (5) prints the symbol table, if desired (Ref 5:79).

During pass II the processor (1) processes the operation codes by converting the mnemonic codes to their 1620 machine language equivalents, (2) Processes statement operands according to the type of operation code. Looks up assigned storage addresses and their symbolic operands in the symbol table that was prepared during pass I. Performs address adjustment, when required, to complete the operands. Examines the flag indicator operand and sets flags in the assembled instruction, (3) processes corrected or newly defined symbolic labels and places them in the symbol table, (4) types error messages for those statements that are unable to be assembled properly, and (5) prepares the assembled output (Ref 5:79).

The operation of the processor is described below:

Pass I input for the processor may be from cards or the console typewriter. The card deck can be used for both passes, but since only card input is allowed for pass II, typewriter input to pass I requires that a source program card deck be punched as an output to pass I to serve as an input to pass II.

Error messages are typed out for both passes. The typewriter output for pass II may consist of the object program with error messages, or error messages only, as determined by the switch settings indicated in Figure 12.

The output of pass II is an object program card deck in either condensed or uncondensed form (see Figure 12 for switch settings). The condensed object deck contains

machine language instructions only, with up to five instructions per card. The uncondensed deck contains both symbolic cards and machine language cards for each statement. Both the condensed and uncondensed card decks contain the loader and arithmetic tables.

After an uncondensed object deck is obtained from pass II a condensed deck may be punched immediately by processing the source cards a third time (see operating instructions). If the third pass is omitted a condensed deck can be obtained from an uncondensed deck by use of the Condenser Program (Ref 5:82-83).

V. Operating Procedures

A. Changes to the Operating Procedures. There are four major changes to the operating procedures for the IBM 1620 SPS. These are:

1. A record mark is not required at the end of a statement when utilizing typewriter input.
2. With switch 1 ON for a listing on the console typewriter during pass II, if either the page-line field and/or the label field are blank, the typewriter will tabulate rather than space to the proper position for type-out of the statement. A space is inserted between the page-line field and the label field during type-out of the listing.
3. After 60 lines of typing, a skip over the

break in the forms will be accomplished by the execution of six carriage returns.

4. The procedure for the use of switch 4 to punch an object program has been altered.

B. Operating Instructions.

1. Clear Memory (this should be done whenever there may be digits in memory with bad parity).

- a. Set all check switches to PROGRAM.
- b. Depress INSTANT STOP and RESET.
- c. Depress INSERT.
- d. Type 16 00010 00000.
(12 digits, no spaces or punctuation)
- e. Depress RELEASE and START (or the R/S key).
- f. After the MAR lights have cycled through memory at least once, depress INSTANT STOP.
- g. Depress RESET.

2. Load the SPS Processor Program.

- a. If the computer is not in manual mode, press INSTANT STOP and RESET.
- b. Set the OVERFLOW switch to PROGRAM, all other check switches to STOP.
- c. Clear the card reader by removing any cards in the hopper and pressing READER STOP and NON-PROCESS RUNOUT. Then remove all cards from the stacker.
- d. Put the Processor deck in the reader hopper.
- e. Depress LOAD.
- f. When the reader stops on the last two cards, depress READER START.
- g. Remove the cards from the read stacker, check for the last card, and put the deck away.

3. Set the program switches as indicated in Figure 12 (Ref 14:8-9).

4. Typewriter Operation. During pass II, with program switch 1 ON, the typewriter types each statement alphanumerically starting at the left margin. After the last character is typed the typewriter tabulates to the place where typing of the storage address and the assembled machine language instruction should begin. Statements are typed in the format entered except that there is a space between the page-line field and the label, and before and after the operation code field. If either the page-line and/or the label field are missing the typewriter will tabulate to the proper position to continue type-out of the statement (Ref 5:91).

The typewriter will type 60 lines of output and then execute six carriage returns to skip over the seam in the paper.

To set up the typewriter, the operator must:

- a. Set right and left hand margins.
- b. Set tab stops 6, 13, and 56 spaces from the left margin. (Note: positions 6 and 13 are fixed. Position 56 may be varied to locate a position a few spaces to the left of the longest statement).
- c. Set paper in the typewriter three lines (three single space carriage returns) below the top of the page.

5. If typewriter input is to be used, the card punch must be readied to punch a source program card deck

as an output for pass I.

- a. Clear the punch by lifting the cards from the hopper and pressing NON-PROCESS RUNOUT.
- b. Discard any cards that are in the stacker.
- c. Load sufficient blank cards into the hopper.
- d. Depress PUNCH START (Ref 14:9).

6. Processing the Source Program

PASS I. After the processor is loaded the program halts. Processing starts when the first statement of the source program is read into the computer and START is depressed.

Typewriter Input:

- a. Type statement.
- b. Depress RELEASE and START keys.
- c. Repeat steps a and b until all statements are entered.

Card Input:

- a. Place source program card deck in the read hopper and depress READER START.
- b. Depress START. Processing proceeds according to the setting of the program switches.
- c. When the reader stops, depress READER START to read the last two cards.

The message "END OF PASS I" is typed out at the end of pass I and the symbol table is printed. The operator may suppress the symbol table type-out by turning program switch 4 ON while the message "END OF PASS I" is being typed. The program halts after type-out of the symbol table (or when switch 4 is turned ON) to allow preparation

for pass II as described below.

PASS II. The source program card deck used in pass I (or the one punched during pass I if typewriter input was used) is used as the input to pass II.

Card Input Only:

- a. Put the source deck in the read hopper and depress READER START.
- b. Set program switches for pass II (see Figure 12). Switch 4 must be ON to punch an object deck.
- c. If an object program is to be punched, ready the punch as outlined in item 5 and depress PUNCH START.
- d. Depress START to begin processing.

After pass II is completed the message "LOAD SUBROUTINES" is typed out if subroutines are required by the source programs. If the subroutines are not required the message "END OF PASS II" is typed and the program halts (Ref 5:92).

Loading the Card Subroutines:

- a. Place the subroutine card deck in the read hopper and depress READER START.
- b. Depress START.

If the subroutine deck being loaded is variable length, the message "ENTER MANTISSA LENGTH" is typed and the program halts. The operator must enter the 2-digit mantissa length (which may range from 02 to 45; a mantissa length of 08 does not have to be entered) from the console typewriter. Processing is resumed by depressing RELEASE and START. The programmer must insure that the number

(length of mantissa) is correct, but program switch four may be used to correct an erroneous entry. (see Figure 12)

Only those subroutines needed by the source program are punched out as part of the object program. After the subroutines are processed the message "END OF PASS II" is typed out and the program is completed (Ref 5:92-92).

7. When the message "END OF PASS II" is typed out, the object deck, if one was being punched, is also complete. The object deck can be removed from the punch by the following procedure:

- a. Lift the blank cards from the punch hopper.
- b. Depress the NON-PROCESS RUNOUT key for a few seconds,
- c. Remove the deck from the stacker and discard the two blank cards at the end (Ref 14:9).

8. Assembling Other Programs. Upon completion of pass II, a condensed object program deck can be obtained by:

- a. Turning program switch 3 ON. (Other switches are set according to Figure 12).
- b. Placing the source cards in the read hopper and depressing READER START and PUNCH START.
- c. Depressing START (Ref 5:93).

VI. Error Handling Procedures

A. Changes to the Error Handling Procedures. The

following is a list of the significant differences concerning error message and correction techniques between IBM 1620 SPS and the AFIT Version of 1620 SPS.

1. An additional error check has been added and the error 10 message has been redefined to account for this check.
2. The error message "adjustment count" has been renumbered to start at one instead of zero, if an error occurs before a label has been defined.
3. An undefined symbolic address, as a result of misspelling or omission, can be defined during pass II and placed in the symbol table.
4. The effects of errors on the assembly process with program switch 2 off have been altered for error messages 1,3,5, and 11.

B. Error Messages. The error message codes that may be typed out on the typewriter during pass I and/or II are identical with error messages of the IBM 1620 SPS except for the modification of error message 10 described below.

ER10

- a. A duplicate label is defined (defined more than once) - Pass I and Pass II.
- b. Incorrect address - Pass II. The address in core storage as assigned in the symbol table during Pass I differs from the address present in the address counter when the statement was processed during Pass II.

As a result of this modification if a card is lost from or misplaced in the source deck between pass I and pass II, an address check comparison will cause type-out of error message code 10 during pass II. During pass II this check is made only when switch 2 is OFF. A multiply defined label that is not corrected between pass I and pass II will cause an error indication during pass II.

In the AFIT Version of 1620 SPS Error Messages have the following form:

LABEL		ADJUSTMENT COUNT	ERROR CODE
XXXXXX	+	XXXX	ERn

Where Label refers to the last defined label and the "adjustment count" refers to the number of statements between that label and the statement in error. If an error occurs before any label has been defined (for instance on the first instruction) the LABEL field is blank and the number in the "adjustment count" is typed out. This number is one on the first instruction (rather than zero as in the IBM 1620 SPS) and goes up by one for each statement processed.

C. Error Correction. Error correction procedures are similar to the IBM 1620 SPS, but there are two significant changes which increase the flexibility of the processor. The first change, which is described below, is the ability to define a symbol during pass II.

The SPS processor places symbols in the symbol table during pass I. However, if through a typographical error or omission a symbol is still undefined at the end of pass I, the processor will accept a definition of the symbol during pass II.

During the second pass, the addresses of the instruction operands are evaluated. If the address is symbolic the symbol table is searched for equivalence, and if the symbol is not found it is undefined and an error message (ER 5) is typed.

With program switch 2 ON, the processor stops after typing the error message so that the undefined symbol can be entered into the symbol table. The procedure to define a symbol at this time is described below:

1. To define a symbol during pass II it is necessary to determine the address of the statement from which a label has been omitted. If this statement has been processed and listed on the typewriter, the address of the unlabeled statement can be read directly from the storage address of the assembled instruction.

If the unlabeled statement has not been listed, the symbol table listing and the program source statements prepared on the SPS coding sheets provide a means to determine the address of the unprocessed statement.

In this case the procedure is to examine the coding sheets to determine the number of intervening instructions

between the nearest defined label and the unlabeled instruction. The address of the unlabeled instruction can be designated by using address adjustment with the symbolic label of the nearest instruction, or by adjusting the storage address of the nearest label as determined from the symbol table listing.

If the undefined symbol had been misspelled rather than omitted the address of the unlabeled instruction does not have to be determined. The procedure for defining symbols under both of these circumstances is explained in the next step.

2. If the undefined label was omitted from an instruction, type the following statement: LABEL DS, XXXXX, where label is the undefined symbol and XXXXX stands for the address, symbolic or actual, of the statement from which the label has been omitted.

If the undefined symbol had been misspelled rather than omitted, the following technique can be utilized: Assume, for example, that many references are made to the symbol FABLE, but the defining statement lists the symbol as FABEL. This can be corrected by typing the statement FABLE DS, FABEL. This will cause the processor to define the symbol FABLE to have the same address as FABEL and to enter this symbol into the symbol table (Ref 1:4-5).

A similar procedure can be utilized to define the labels of declarative statements at areas following the last assigned storage space in the symbol table. Determination of the last assigned address can be made by examining the symbol table listing (which was typed at the end of pass I) to secure the address of the last defined label.

3. Remove the remainder of the source deck from the reader hopper and depress NON-PROCESS RUNOUT.

4. Insert the unprocessed cards and the statement for which the error message was printed in front of the unprocessed portion of the source deck and place in the reader hopper. Depress READER START.

5. If no object deck is being punched (switch 4 OFF) depress RELEASE and START.

6. If an object deck is being punched (switch 4 ON).

- a. Depress RELEASE.
- b. Turn switch 4 OFF.
- c. Depress STOP/SIE once.
- d. Turn switch 4 ON.
- e. Depress START.

7. The symbol with its defining address will be placed in the symbol table, the statement that contained the undefined symbol and the remainder of the source deck will be processed.

The second change concerns the effect of errors on the assembly process. With program switch 2 OFF, the processor does not stop for an error correction, but the errors affect the assembly process. The changes to the IBM 1620 SPS processor are described below:

ER 1 - A NOP instruction, 410000000000, is assembled. If the record mark is in the op code field the label, if non blank, is placed in the symbol table. If the record mark is in the label field the label is treated as a blank.

ER 3 - A NOP instruction, 410000000000, is assembled. The label field, if non blank, is placed in the symbol table.

ER 5, ER 11 - Only the symbol in error is assembled as a 00000 (zero) address; the remainder of the operand is evaluated and assembled for output.

VII. Modifying the Processor for Additional Storage

The AFIT Version of 1620 SPS automatically adjusts itself to the size of memory; therefore, no modification of the processor card deck is required when additional storage is provided by the IBM 1623 Core Storage Unit.

VIII. SPS Listing on the IBM 870

The IBM 870 can be used to make an SPS listing from an SPS object deck. The format is similar to the type-writer listing on the 1620 console except for the following exceptions: (1) a flagged zero is typed as

a +, (2) the flagged digits 1-9 are typed as J-R, respectively, and (3) the first digit of the page-line field is not typed.

To facilitate operation of the IBM 870 for this purpose the object deck card format has been altered in the AFIT Version of 1620 SPS. The page-line field on object deck cards punched by the AFIT processor has been changed to provide: (1) The number "6" in the first column of a source statement card, (2) The number "9" in the first column of a numeric instruction card.

In order to save the first digit of the page-line field (located in the first column of a card) for a listing on the IBM 407 the page-line field has been further altered as follows: (1) The first digit of the page-line field on the source statement has been placed as the second digit in the page-line field on the numeric card, and (2) The second digit on the source statement card (which is identical on the numeric instruction card) is preserved in position. Since the IBM 407 control panel can be wired to replace the digits in their proper position in the page-line field an unaltered listing can be obtained.

The operating instructions for preparing an SPS listing

from an SPS object deck on the IBM 870 are as follows:

1. Clear all cards from the machine.
2. Insert the SPS drum card and lower the star wheels.
3. Make sure the "SPS list control panel" is in the machine.
4. Turn the Auto Feed switch ON.
5. Insert the deck to be listed in the hopper.
6. Make sure blank paper is in the typewriter, and the carriage is in its leftmost position.
7. Press the FEED key twice.
8. The listing will begin. To stop before it is finished, use the same procedure as for other types of listing. After the DEND statement and its associated address have been typed out, the listing should be stopped and the rest of the cards removed. If these cards are allowed to list, most of them will simply pass through the machine without listing, but some of them may cause erroneous listings. In addition, this takes extra time (Ref 16:2-3).

IX. Control Operations

A new pseudo-op designated MORG has been added to the AFIT processor. Through this operation the programmer is able to exercise more control over addresses assigned by the processor.

This pseudo-op instructs the processor to define the origin to be the next larger multiple of the given operand. An example is given below:

```
          DORG  4140
          BB
          MORG  100
X         DS    5
```

The MORG pseudo-op defines the origin to be 4200 and causes the next sequential instruction to be loaded in this position. In this case the symbol X would be assigned the address 4204 (Ref 13:1).

X. Macro-Operations

Two new macro-operations that were written by Lt. Pratt and added to the IBM 1620 SPS processor in use at the Institute of Technology have been incorporated in the AFIT Version of the SPS processor. These are used for conversion of floating point numbers from the internal form to the external form, and vice versa. The two macro-operations are called by using the names (1) INC - INput Conversion, and (2) OUTC - OUTput Conversion. These names appear in column 12, just as with other macro-operations (Ref 15:1).

XI. Miscellaneous

Additional Features. The following features which

were not present in the IBM 1620 SPS have been added to the AFIT processor.

When a source deck is being punched during pass I and statements are being entered from the console typewriter, if switch 1 is turned on to complete entry of the source statements from the card reader, the last entry from the typewriter will be punched in the source deck.

Extensive labeling has been accomplished. Use of the address adjustment procedure was reduced, thus increasing the number of symbols in the program. This was done to improve the readability of the processor program and as an aid to modification and recoding.

Operation of Program Switches. The operation of the program for the AFIT Version of 1620 SPS is outlined in Figure 12 on page 97. The two major changes are (1) Switch 4 has to be ON to punch an object program, and (2) with switch 2 on the procedure for correction of statements containing error messages has been altered.

SWITCH	PASS I		PASS II	
	ON	OFF	ON	OFF
1	Card Reader Input.	Typewriter Input.	Input statement and the assembled machine language instruction are typed out.	Listing is not typed.
2	After an error message is typed the computer stops so that a corrected statement can be entered at the typewriter.	After an error message is typed, the error is adjusted by the processor and processing continues.	Same as pass I. To continue processing after corrected statement has been entered; With SW 4 ON: press RELEASE, turn SW 4 OFF, press STOP/SIE once, turn SW 4 ON, press START. With SW 4 OFF: press RELEASE and START.	Same as pass I.
3		Switch must be off when assembling a program.	Condensed object program.	Uncondensed object program.
4	To correct a typing error made while entering a statement: Turn ON, Depress RELEASE and START. Turn OFF, and re-enter entire statement at typewriter.	Switch should be off when assembling a program.	Object program is punched. (Same as pass I for correction of typing errors).	No object program is punched (used to pre-edit a source program).

Fig. 12

Operation of Program Switches

Flow Diagram Changes. The principal changes to the flow diagrams for the IBM SPS Processor are in (1) the input routines, (2) the routine to load labels into the symbol table, and (3) the DEND/TCD routine. In addition, since the symbol table can now be entered during pass II, all routines proceed to the Load Label routine rather than to pass II as indicated on the IBM SPS processor flow diagrams. Consequently except for the flow diagrams in Figures 18, 19, and 20, if the symbol PASS II is changed to read LOAD LABEL on all IBM SPS processor flow diagrams, the diagram will be compatible with the AFIT Version of 1620 SPS.

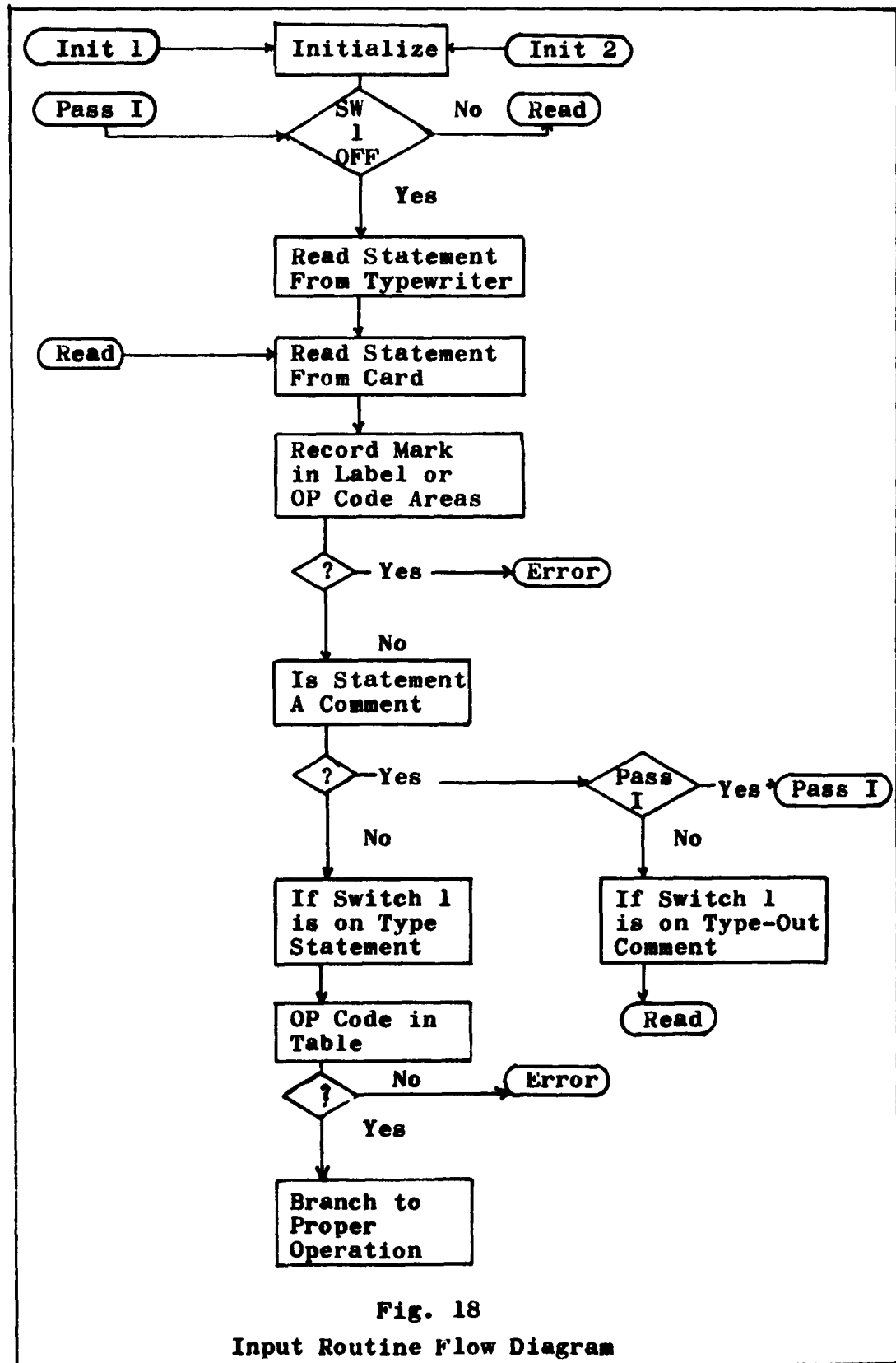


Fig. 18

Input Routine Flow Diagram

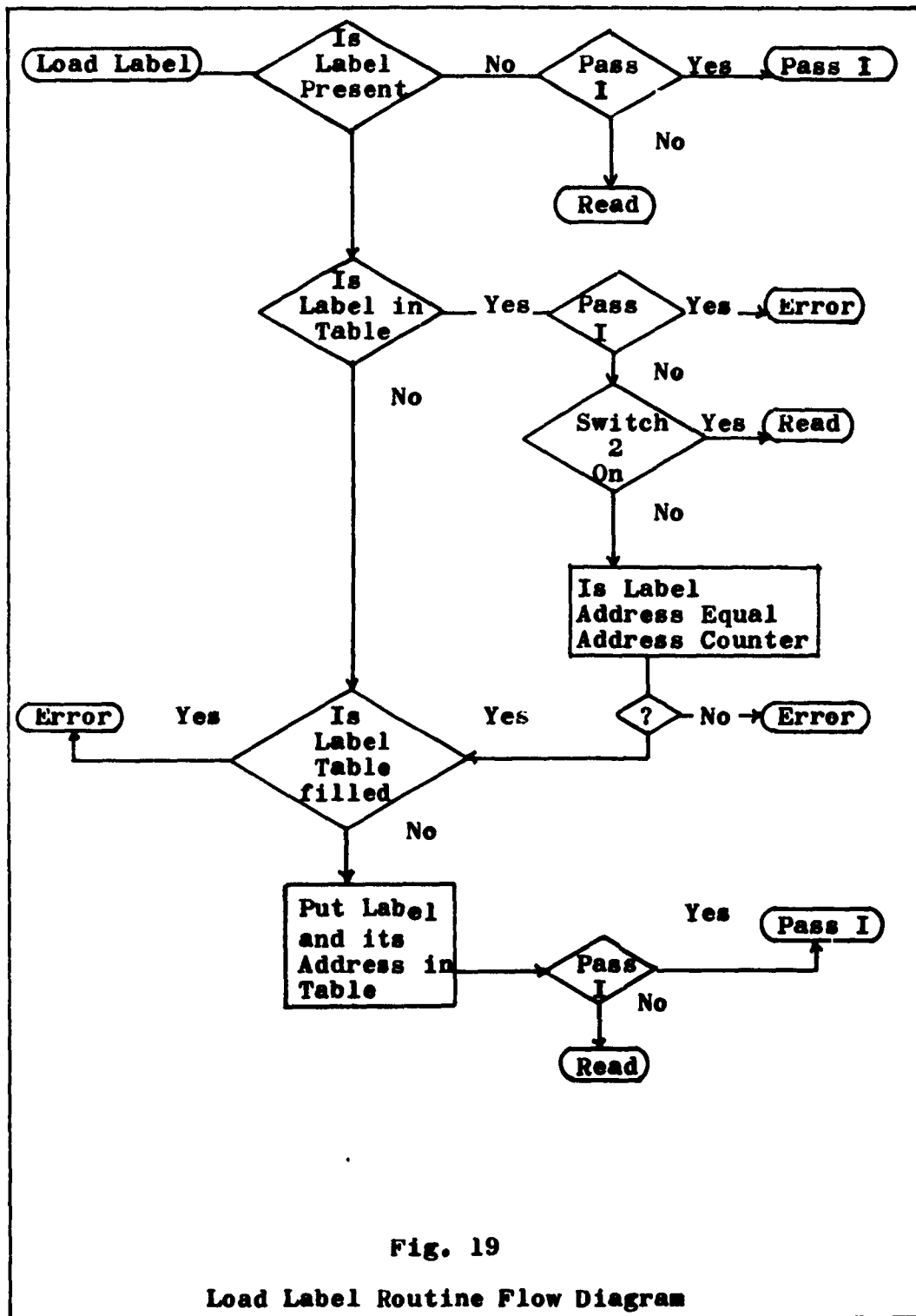


Fig. 19

Load Label Routine Flow Diagram

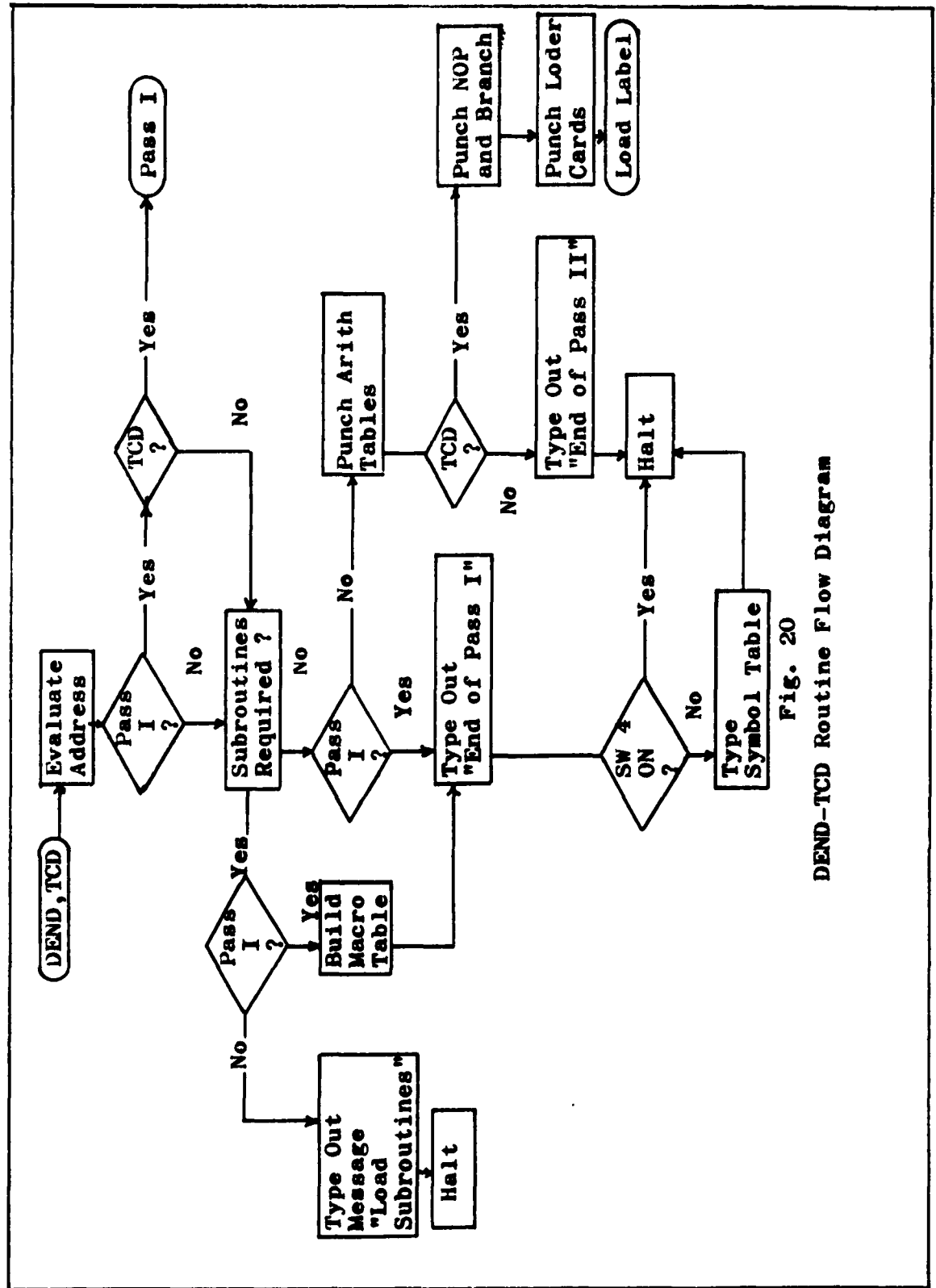


Fig. 20
DEND-TCD Routine Flow Diagram

Appendix C

Label Reference Index

Appendix C contains a printed listing of the Label Reference Index object program that was assembled at the School of Logistics 1620 computer facility using the IBM 1623 Storage Unit. The printed listing was prepared from the object program using the IBM 407.

The Label Reference Index is a list of all symbols in the processor program and of all card numbers in the program which refer to each symbol.

10055*	SPS PROCESSOR FOR AFIT VERSION 1620 CARD 170, DATED 11/17/62
27435	A 13125
11835	AA1 11885
12215	AA2 12205 12225 12235 12245
28905	AA3 28895 28915 28925 28935
20555	ARLE 20385 20405 20495
11445	ADORS 13605 14225 14275 14345 15595 16935 17265 17635 17645 17655
	17795 17825 17835 18705 18715 18725 18745 19285 19295 19735
	19925 19985 20005 20765 20775 20835 21005 21245 21275 21275
	21285 21735 21815 21915 22025 22085 22115 22265 22375 22405
	22435 22545 22575 22615 22695 22715 22915 22925 23055 23455
	23465 23475 24385 25025 25075 25105 25235 25615 25715 25755
	25805 26365 26725 26735
25705	AERB
10155	AJUST 19715
13125	ALFOP 13055
10455	ALPHA 13635 14225 14835 14845 14875 14955 15075 15215
14225	AORS 13665 14195 14235
22155	ASTINE 22035
14995	ASTER 13825
22445	A1 22415 22505
15945	A10 16125
14035	A11 13755 14165 14485
13725	A12 14265 15035 15105 15135
13875	A13 14115
14025	A14 14495
14785	A15 14825
16645	A16 16335
16515	A17 16475 23005
16365	A18 16735
16305	A19 16765
11815	A2 11785 11795 11805 11835
17945	A21 17815 17815
19105	A22 18225
18515	A23 18385
18565	A24 18635
18555	A25 19005
18745	A26 19145 19185
19605	A27 19575 19685
19675	A28 19785
20635	A29 20645 20875
11795	A3 11845
21575	A32 21525
21945	A33 21975
24445	A34 21955

22075	A35	22155
22375	A36	22465
12425	A37	25985 26765
23105	A38	22875 22895
12355	A4	12385 15535
23555	A41	23095 23165
23875	A42	
23235	A43	23515 23535
23255	A44	23525
24085	A45	24015 24075 24095
24155	A46	24055
24025	A47	24065 24135
23175	A48	24175
12985	A49	12955
16825	A5	12525 12545 12545 12545 23575 23575 23595 23705 23705
		23805 23805
24745	A50	24575
24695	A51	24585
24835	A52	24795
25115	A53	25085 25255 25295
25565	A54	25335
25525	A55	25565
25655	A56	25465 25605
25625	A57	25485
25715	A58	25655
25755	A59	25675 25705
13215	A6	12115 13015
26095	A60	26035 26045
26035	A61	26075
26215	A62	26145 26165
15285	A63	15275 15315 15405 15415 15425 26615 26645
16215	A64	16175 26435 26485 26525
15515	A7	13225 15555 16225 24465 25445
24735	A70	24545
15965	A8	22705
15955	A9	16015 16235
20485	BAKR	20435
16875	BB	15395 16815 16825 17895 17905 17945 19365 19415 22985
14365	BRACK	14355
23885	BETA	13625 14255 14875 14965
19525	RI	13515
26375	9IT	26265
17575	SEKVR	17515 17525 17535 17595
27055	BLNKS	12705 16605 16995 17255 17275 17775 18305 18495 23645
11405	RLSND	17625

19535	BNI	13515	
17145	BRNH	17085	17095
27265	BRSQ	23555	23565
21135	BR1	21115	21165
21155	BR2	21125	
13535	BTBL	13435	
11685	B1	11665	11675 11695
13145	B10	13125	13135
16115	B12	16055	
13965	B13	13885	
14185	B14	14155	
14235	B15	14185	
14345	B16	14285	
14425	B17	14385	
14455	B18	14405	
14655	B19	14595	
11675	B2	11705	
14685	B20	14655	14665 14675
14825	B21	14815	
14945	B22	14895	
15645	B23	15615	
15615	B24	15675	
15755	B25	15735	
15795	B26	15745	
15855	B27	15835	
15875	B28	15865	
16465	B29	16435	16445 16455
11875	B3	11825	
16495	B30	16465	
16595	B31	16535	
16695	B32	16555	
16665	B33	16705	16725
15215	B38	15195	15205
17305	B39	17295	
12455	B4	12415	
17415	B40	17395	
17555	B41	17545	17565 17575 17585
17605	B42	17595	
18125	B45	18095	18115 18145
18195	B46	18165	
18165	B47	18145	18155
18955	B48	18925	
19665	B49	19655	
19715	B50	19705	
19725	B51	19715	

19885	A52	19845
19975	A53	19945
20065	A54	20025
20245	A55	20105
20175	A56	20165
20325	A57	20295
20355	A58	20325
20425	A59	20395
12695	A6	12675
20295	A60	20465
20535	A61	20505
20565	A62	20555
20705	A65	20685 20695
20875	A66	20855 20865 20895
20865	A67	20885
20915	A68	20895 20905
21325	A71	21295
21355	A72	21325
21415	A73	21385
21445	A74	21415
21465	A75	21425
21495	A76	21485
21555	A77	21535 21545
21605	A78	21585 21595
21645	A79	21615 21625 21635 21655
12975	A8	12945
21635	A80	21665
21975	A81	21925
22335	A84	22275
22685	A85	22665
23045	A87	22965
23035	A88	22945
23065	A89	23045
22985	A891	17805 17805 23065 23065
12005	A9	12035
23665	A90	23655
23685	A91	23675
23725	A92	23715
23355	A93	23305
23365	A94	23355 23375
23455	A95	23445
23505	A96	23485
24115	A99	24095 24105
20455	CHAR	20605
25165	CHECK	24985

15385	D26	15195	15335	15345	15355	15405	26545
15405	D27	15375					
15465	D28						
15495	D29						
24515	D3	24415					
26545	D30	26405					
26565	D32	26545	26555				
15295	D33	15175	26375				
26745	D34	26575					
24635	D4	24605					
24825	D5	24805					
24875	D6	24855	24865	24895			
24905	D7	24895					
24955	D8	24915					
24985	D9	24955					
17135	EJS	11545	11645	12105	12425	12455	12605
		19845	21765	22135	22205	22445	22685
		24485	25115	25335	25465	25765	25915
							26405
16345	EMPTY	16625					
24425	ERCON	21265	21305	21335	21395	21455	22325
25415	ERDSA	25595					24405
11115	ERLAB	11555	15765	26745			24595
12045	ER1						24755
26415	ER10	26605					24885
14305	ER11						
16145	ER12	16085					
16195	ER13	16035					
26465	ER14	26185	26245				
13195	ER3						
13925	ER5	14735	15175				
26505	ER9	26635					
15555	FV1	15495					
27395	FINAL	11695	15825	17715	26615	28805	28815
21775	F1	21035	21705				
21815	F2	21705					
21765	F3	21805					
26705	F9	25965					
14565	GET	14205	15005				
14195	GET1	14075					
25725	GOAH9	25175					
13455	GOOD8	13095	13355	13445	17055	25705	25775
13475	GOOD1	13435	13465				
13485	GOOD2	13475					
26895	GO10	22915	22955	23035	23785	23795	
22655	G1	22585					

28805	G10	28755	
26615	G11	26375	26585
12305	G13	11725	
21065	G14	21055	
12165	G15	12365	12585 12585
12885	G16	12805	
12915	G17	12835	
12925	G18	12865	
12825	G19	12895	
11895	G20	11795	11855
17255	G22		
12075	G23	12065	
13345	G24	13305	
19265	G25	19255	
13015	G26	12775	12985
23315	G30	23295	
14545	G4	15225	
19285	G5	18205	19025 19035 19165 19175
28735	G8	28775	28785 28805
28775	G9	28745	
26115	HED	11565	13645 14455 14575 14685 15925 16095 16165 26365
12995	H1	12465	
11545	INIT1	23905	28955
11555	INIT2	23335	23895
26865	INRQM	11575	11995 15525 15775 26755
10335	INPUT	11785	11835 11955 11975 12015 12135 12175 12185 12195 12205
		12235	12375 12595 12685 12785 12825 12925 12945 12975 13055
		13075	13085 13155 13295 13785 13815 13845 13865 14035 14035
		14055	14105 14135 14155 14185 15615 15645 15665 15665 15945
		16005	16045 16065 16095 16115 16115 17205 17215 17225 17385
		17425	17475 17915 18275 19055 19455 20105 20285 20285 20295
		20325	20355 20375 20395 20425 20455 20455 20485 20505 20535
		20555	21045 21125 21155 21225 21295 21325 21355 21575 21605
		21895	21925 22035 22335 24325 24355 24415 24445 24565 24595
		24605	24695 24705 24725 24725 24735 24985 25165 25165 25185
		25185	25525 25555 25565 25635 25955 26015 26745 28865
		28875	28885 28895 28925
27165	INSND	18695	
19515	INST	13105	13515
10215	ISTAT	11715	20685 24115 24005 24045
15275	IT	15185	15185 26385 26385
10205	JSTRL		
19705	JUST	13235	13735 19835 19835 20625 20625 21715 21715 21975 21975
19555	K	25885	25885
		13525	

15075	TFADD	15055			
14355	TOBB	15605	15625	15655	
16385	TR	16365	16375	16395	16615
25885	TRA	13515			
11225	TRAC	25905			
20285	TRANS	20335	20575		
25615	TRDSA	25315	25385	25405	25545 25575 25585 25685
24725	TRREC	24615	24645		
26125	TSPEC	26005	26215	26235	26245
12255	TYPE	16345	16645		
24195	WRMS	19075	23965		
28385	XDAS	21225			
28685	XDEN0	13175			
28445	XDNB	17425			
28365	XDS	21895	24325		
28425	XDSA	18275	19055		
28435	XDSB	17385			
28375	XDS5	24355			
10105	ZEPO	13075	13085	13145	13155 13345 13445 18095 18585 18625
		18635	18765	18775	18785 18875 18885 18895 18905 18925 18955
		18975	18995	18995	19105 19105 19605 19615 19615 19625
		19655	19675	19775	19825 19895 19905 19905 19925
		19935	19985	19995	20165 20195 20215 20445 20565 20595 20635
		20645	20695	20805	20815 20825 20835 20845 20915 20925 20935
		22275	22395	22855	22945 23095 23255 23275 23485 23495 23505
		23815	24315	24365	24515 24525 24705 24715 24715 24745 24775
		24805	24815	24825	24835 24855 24905 24925 24955 24965 25125
		25615	25905		
10265	ADPCOW	11585	11985	13245	15075 15515 19705 19725 19735 19855 19885
		20005	20015	21725	21745 21755 22075 22115 22125 22375 22385
		22525	22535	22565	22575 22615 22655 22675 23985 24475 25025
		25035	25045	25655	25665 25675 25685 25695 25725 25895
14055	BCMSPC	13715			
27285	BRLQAN	24265			
16625	BRRDBB	16515	16665		
12665	CASTER				
24565	CCOMER	24735			
21375	CHVALD	21355	21365	21475	21485 21535 21585
10295	CLFRER	11555	11685	11925	11935 11945 12175 12185 12195 12795 13605
		14275	14885	17485	17495 17505 18105 19825 23255 24515 24875
		25955	28865	28875	28885
16295	CMPCON	18455	18525	18605	
16755	CMPINS	18915			
11435	CMPOUT	16355	16385	16405	16425 16525 16555 16565 16575 16585 16605
		16615			

13005	PICKUP	20845	24155
22885	PUNCH1		
25155	PRDCSA		
16525	PUNCHY	16575	
14265	RETURN	13675	14065
19105	SECINS	18965	18985
15315	SEIFIN	15285	
23325	SEVENS	17965	
22565	SHFLA	22535	22545
21455	STCHAR	21465	21675
19225	SURENT	23985	24115 24125 24155
28695	SYMTBL	11665	15275 23225 28705
19195	TABBY1	13385	15585 18205 19035 19175 19255 24505 25485 26605
27215	TARCON	23605	
26785	TALCRD	23585	
14615	TBLEND		
24845	TESTAD	16415	16695
10185	THINGS	13685	13725
26885	TISTAT	11715	23115
14725	TRNUM8	14565	
14795	TRNUM1	14755	14765 14775 14815
18315	TYPADD	18125	18135
18085	TYPDSA	19085	25845
20005	TYPINS	19955	
15825	WRPRND	15865	18455 18525 18605 18915
20595	ZERONE	20515	20545
28985			

Appendix D

Program Listing

Appendix D contains the final printed listing of the AFIT Version of 1620 SPS. This program was assembled on the IBM 7090 and printed in an off-line operation on the IBM 1401.

10365	DC	2.0	00817	2
	-0			
10375	DC	2.0	00819	2
	-0			
10385	DC	2.0	00821	2
	-0			
10395	DC	2.0	00823	2
	-0			
10405	DC	2.0	00825	2
	-0			
10415	DC	2.0	00827	2
	-0			
10425	DC	2.0	00829	2
	-0			
10435	DC	2.0	00831	2
	-0			
10445	DC	2.0	00833	2
	-0			
10455	DC	2.0	00835	2
	-0			
10465	DC	2.0	00837	2
	-0			
10475	DC	2.0	00839	2
	-0			
10485	DC	2.0	00841	2
	-0			
10495	DC	2.0	00843	2
	-0			
10505	DC	2.0	00845	2
	-0			
10515	DC	2.0	00847	2
	-0			
10525	DC	2.0	00849	2
	-0			
10535	DC	2.0	00851	2
	-0			
10545	DC	2.0	00853	2
	-0			
10555	DC	2.0	00855	2
	-0			
10565	DC	2.0	00857	2
	-0			
10575	DC	2.0	00859	2
	-0			
10585	DC	2.0	00861	2
	-0			
10595	DC	2.0	00863	2
	-0			
10605	DC	2.0	00865	2
	-0			
10615	DC	2.0	00867	2
	-0			
10625	DC	2.0	00869	2
	-0			
10635	DC	2.0	00871	2
	-0			

10645	DC 2.0	00873	2
10655	DC 2.0	00875	2
10665	DC 2.0	00877	2
10675	DC 2.0	00879	2
10685	DC 2.0	00881	2
10695	DC 2.0	00883	2
10705	DC 2.0	00885	2
10715	DC 2.0	00887	2
10725	DC 2.0	00889	2
10735	DC 2.0	00891	2
10745	DC 2.0	00893	2
10755	DC 2.0	00895	2
10765	DC 2.0	00897	2
10775	DC 2.0	00899	2
10785	DC 2.0	00901	2
10795	DC 2.0	00903	2
10805	DC 2.0	00905	2
10815	DC 2.0	00907	2
10825	DC 2.0	00909	2
10835	DC 2.0	00911	2
10845	DC 2.0	00913	2
10855	DC 2.0	00915	2
10865	DC 2.0	00917	2
10875	DC 2.0	00919	2
10885	DC 2.0	00921	2
10895	DC 2.0	00923	2
10905	DC 2.0	00925	2
10915	DC 2.0	00927	2

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10925	DC 2,0	00929	2
	-0		
10935	DC 2,0	00931	2
	-0		
10945	DC 2,0	00933	2
	-0		
10955	DC 2,0	00935	2
	-0		
10965	DC 2,0	00937	2
	-0		
10975	DC 2,0	00939	2
	-0		
10985	DC 2,0	00941	2
	-0		
10995	DC 2,0	00943	2
	-0		
11005	DC 2,0	00945	2
	-0		
11015	DC 2,0	00947	2
	-0		
11025	INPUT2 DS 12	00959	12
11035	DS 152	01111	152
11045	ADCRS DS 11	01122	11
11055	DC 1,0	01123	1
	-0		
11065	RMRK DS 3	01126	3
11075	DC 1,0	01127	1
	-0		
11085	LINK TFM 11,23,27		
11095	8	01128	16
11105	DC 1,0	01140	49
	-0	01152	-0011 -0023
11115	ERLAB DAS 6		
11125	DAC 2,0	01155	2 X 6
	-0	01167	2 X 2
11135	MESS1 DAC 15,END OF PASSIT	01171	15 X 2
	-0		
11145	MESS2 DAC 17,LOAD SUBROUTINES	01201	17 X 2
	-0		
11155	LDOUT DS 12	01245	12
11165	DC 4,0	01249	4
	-00		
11175	LAB DS 12	01261	12
11185	DC 1,0	01262	1
	-0		
11195	ELNGTH DC 2,75	01264	2
	-0		
11205	DC 2,70	01266	2
	-0		
11215	DC 2,0	01268	2
	-0		
11225	TRAC DC 26,36000000050049000000000000	01294	26
	-360000000500490000000000		
11235	LODER1 RNC D 72	01296	36
11245	RNC D 201	01308	36
11255	BNF 12,276	01320	44
			00012 00276

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11265	TF	59,274	01332	26	00059	00274
11275	TF	11	01344	25	00011	00000
11285	TF	90,269	01356	26	00090	00269
11295	DNB	3	01370		3	
11305	DC	1,0	01371		1	
11315	DC	4,0	01375		4	
11325	LOCER2	IF 95,264	01376	26	00095	00264
11335	TF	1200	01388	31	00000	00200
11345	TF	114,274	01400	26	00114	00274
11355	TU	11	01412	25	00000	00011
11365	H	12	01424	49	00012	00000
11375	DNR	15	01450		15	
11385	DC	1,0	01451		1	
11395	DC	4,0	01455		4	
11405	BLSNC	-00	01457		12	2
11415	DAC	12,-7J0000J0000	01483		4	
11425	DC	4,50	01485		5	2
11435	CMPOUT	DS 1	01494		1	
11445	DNR	50	01544		50	
11455	DNR	29	01573		29	
11465	INPUT3	DS 12	01585		12	
11475	ENTABL	DSB 7,30	01592		7	30
11485	RECNR	DC 1,0	01796		1	
11495	INITI	TDM LJS				
11505	INIT2	TF ERLAB+10,CLERER+11				
11515	INIT2	TF MED+10				
11525	INIT2	TF INKRM,0				
11535	INIT2	TF ADDCOM+401				
11545	INIT2	TF ORDER,9999,8				
11555	INIT2	TF KCNI,60,10				
11565	INIT2	TF ERLAB+10,CLERER+11				
11575	INIT2	TF MED+10				
11585	INIT2	TF INKRM,0				
11595	INIT2	TF ADDCOM+401				
11605	INIT2	TF ORDER,9999,8				
11615	INIT2	TF KCNI,60,10				
11625	INIT2	TF ERLAB+10,CLERER+11				
11635	INIT2	TF MED+10				
11645	INIT2	TF INKRM,0				
11655	INIT2	TF ADDCOM+401				
11665	INIT2	TF ORDER,9999,8				
11675	INIT2	TF KCNI,60,10				
11685	INIT2	TF ERLAB+10,CLERER+11				
11695	INIT2	TF MED+10				
11705	INIT2	TF INKRM,0				
11715	INIT2	TF ADDCOM+401				
11725	INIT2	TF ORDER,9999,8				
11735	INIT2	TF KCNI,60,10				

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```

11745 *
11755 *
11765 *
11775 *
11785 RSCAN
11795 A3
11805 A3
11815 A2
11825 A1
11835 AA1
11845 A3
11855 B
11865 B3
11875 B3
11885 AA1
11895 G20
11905

11915 *
11925
11935
11945
11955
11965 *
11975
11985
11995
12005 B9
12015
12025
12035 RLOP
12045 ER1
12055

12065
12075 G23
12085
12095

12105
12115
12125
12135 RMFL
12145
12155
12165 G15
12175
12185
12195
12205
12215 AA2
12225
12235
12245
12255 TYPE
12265

TFM A2+11,INPUT+140
TF G20+6,A2+11
SM A2+11,2
TF TEMP
BMR B3,TEMP
CM A2+11,INPUT+20
BH A3
B G20
DORG *-3
CM TLMp+.10
BE AA1
TFM
DC 2,*,*

-1 CLEAR AREA FOR PUNCHING OUT SOURCE STATEMENT
TR INPUT2-1,CLERER
TR INPUT2+52,CLERER
TF INPUT2+148,CLERER+46
TK INPUT2-11,INPUT-11
-1 CHECK FOR RECORD MARK IN LABEL OR OPCODE FIELD
TFM RLOP+11,INPUT-2
TF PLACE,ADDCOM
AM INRM,1,10
AM RLOP+11,2,10
CM RLOP+11,INPUT+20
BE RMFL
BMR B9
TFM EVALER-1,10000
DC 1,*,*

TF G23+6,RLOP+11
TDM 0
TDM SET,
DC 1,*,*

BC NAST,EJS
B A6
DORG *-3
CM INPUT,14,10
BB 0
DORG *-9
TFM SET,0,10
TF INPUT-2,CLERER+9
TF INPUT+10,CLERER+11
TF INPUT+18,CLERER+7
TFM AA2+6,INPUT+20
TFM 1,10
AM AA2+6,2
CM AA2+6,INPUT+140
BL AA2
DS 2,*
BB

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12275 DCRG *-9
12285 BC READ,PRSW
12295 MACD INPUT-10
12305 BT KCTV,KCTY-1
12315 ME READ,PRSW
12325 *
12335 * READ STATEMENT FROM TYPEWRITER
12345 *
12355 A4
12365 BT G15,G15-1
12375 NATY INPUT-10
12385 BC4 A4
12395 DS 2,*
12405 BT MSCAN,SCAN-1
12415 BNF B4
12425 BC READ,EJS
12435 B PASSI
12445 DORG *-3
12455 BNR UP,LJS
12465 b H1
12475 DCRG *-3
12485 *
12495 * PUNCH LOADER
12505 *
12515 PLDR
12525 TR INPUT2,LODER1
12535 BT A5,A5-1
12545 TR INPUT2,LODER2
12555 HT A5,A5-1
12565 * READ STATEMENT FROM CARD
12575 *
12585 BT G15,G15-1
12595 RACC INPUT-10
12605 BNR STAR,EJS
12615 BT KCTV,KCTY-1
12625 HT RSCAN,SCAN-1
12635 *
12645 * CHECK FOR COMMENT STATEMENT
12655 *
12665 BNE NASI
12675 BNF B6,PRSW
12685 NATY INPUT-10
12695 HTM LINC,*12,7
12705 TF INPUT2*10,BLNKS-64
12715 BT PCHCRD,PCHCRD-1
12725 B READ
12735 DORG *-3
12745 *
12755 * TYPE OUT SOURCE STATEMENT
12765 *
12775 NAST
12785 BNF G26,PRSW
12795 TF LOPOUT,INPUT-2
12805 C LOPOUT,CLENER+9
12815 BNE G16
12825 TRTY
12835 TF LOPOUT,INPUT+10
12845 *
12855 G19

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12835	RD	G17,LOPDT-11
12845	TRTY	
12855	ORDER	DC 4,1,0-4
		-001
12865	B	G18
12875	DURG	0-3
12885	G16	WATY LOPDT-8
12895	H	G19
12905	DORG	0-3
12915	G17	WATY LOPDT-10
12925	G18	TF LOPDT,INPUT+16
12935		WATY LOPDT-6
12945	BNR	88,INPUT+20
12955	B	A49
12965	DURG	0-3
12975	B8	WATY INPUT+20
12985	A49	BNF G26,PRSM
12995	H1	TeTY
13005	PICKUP	DS 5,0-5
13015	G26	BC A6,SET
13025	*	
13035	*	SCAN UPCODE TABLE
13045	*	
13055	CP	CM INPUT+12,7C,10
13065		BL ALFUP
13075		TC ZEPD+28,INPUT+12
13085		TD ZEPD+29,INPUT+14
13095		TCM GOODR+11,-2
13105	B	INST
13115	DURG	0-3
13125	ALFNP	TFM H10+11,A-11
13135	H10	AM H10+11,11,10
13145	H10	TF ZEPD+30
13155	COMP	C ZEPD+27,INPUT+16
13165		SE OK
13175		CM COMP-1,XDEND
13185		BL COMP-24
13195	ER3	TFM EVALER-1,3C000
13205		DC 1,,0
13215	A6	RT EPRINT,EPRINT-1
13225	HC2	AT
13235	PT	JUST,JUST-1
13245	AM	ADDCOM,11,10
13255	*	
13265	*	STATEMENT HAD RECORD MARK IN LABEL OR OPCODE FIELD
13275	*	ON THE UPCODE WAS INVALID, HENCE IT IS TREATED AS A NOP
13285	*	
13295	*	
13305		CM KLOP+11,INPUT+16
13315		BL G24,EJS
13325		BM L0L0L
13335		H PASS1
13345	G24	DURG 0-3
13355		TF ZEPD,NUPREC-12
13365		TFM GOODR+11,-2
		MNF LINPR1,PRSM

			PAGE
02846	43	02898	01234
02858	34	00000	00108
02865			4
02870	49	02910	00000
02878			
02878	39	01237	00100
0289C	49	02834	00000
02898			
02898	39	01235	00100
02910	26	01245	00815
02922	39	01239	00100
02934	45	02954	00817
02946	49	02966	00000
02954			
02954	39	00817	00100
02966	44	02990	08664
02978	34	00000	00108
02984			5
02990	43	03166	13313
03002	14	00809	000P0
03014	47	03070	01300
03026	25	00528	00809
03038	25	00529	00811
03050	15	03353	0000K
03062	49	08764	00000
03070	16	03105	J5431
03082	11	03105	000J1
03094	26	00530	00000
03106	24	00527	00815
03118	46	03318	01200
03130	14	03105	J6817
03142	47	03082	01300
03154	16	05105	L0000
03165			1
03166	27	05310	05304
03178	46	05142	00200
0319C	27	08944	08943
03202	11	00725	000J1
03214	14	02233	-0807
03226	43	03238	00587
03238	46	14194	01100
03250	49	02426	00000
03258			
03258	31	00500	00708
03270	15	03353	0000K
03282	44	06342	08664

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13375      BT  MCITY,RCITY-1
13385      BTM  TARRYVL,LINPRT,7
13395      *
13405      *      USING THE LAST DIGIT OF THE CPCODE ENTRY GOODB IS
13415      *      MODIFIED TO BRANCH TO THE CORRECT ENTRY IN BTBL
13425      *
13435      OK  TFM  GOODJ+11,BTBL
13445      ID  GOODR+11,ZERO*30
13455      MM  *+9,500,81C
13465      A  GOODI+11,99
13475      TF  GOOD2+6
13485      GOOD2 8
13495      DORG *--4
13505      DSA  MAC*U

13515      DSA  TRA,INST,BI,BNI

13525      DSA  KDW,K

13535      BTBL  DSA  OSDNB,DAS,DC,DAC,DSA

13545      DSA  CSR,DORG,DEND,HEADER,MORG

13555      *      THE FOLLOWING CLOSED SUBROUTINE EVALUATES
13565      *      THE STATEMENT OPERAND
13575      *
13585      *
13595      NUP
13605      EVALAD TF  ADDMS,CLERER+9
13615      TFM  EVALAD-9,100,9
13625      TF  BETA,ONEZ
13635      TFM  ALPHA,0
13645      SF  HED-2
13655      SF  EVALAD-5
13665      TCM  ADDR$1,1
13675      TDM  RETURN+1,9
13685      TR  COLL-18,THINGS-20
13695      TFM  LABL,1,10
13705      TFM  DOL,1,10

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03294 27 08618 08617
03306 17 08524 -8342

03318 16 03377 -3424
03330 25 03353 00530
03342 13 03351 0-5-0
03354 21 03377 00099
03366 26 03384 00000
03378 49 00000 00000
03385
03389 5 X 1
03389 -9670
03394 5 X 4

03394 J4146
03399 -8764
03404 -8776
03409 -8788
03414 5 X 2

03414 -8800
03419 -8812
03424 5 X 5

03424 J1024
03429 -9974
03434 J2710
03439 J0124
03444 J3614
03449 5 X 5

03449 J0764
03454 J1304
03459 J1444
03464 -5470
03469 J1212

03470 41 00000 00000
03482 26 01122 00741
03494 16 03473 00J00
03506 26 12413 00699
03518 16 00411 -0000
03530 32 14339 00000
03542 32 03477 00000
03554 15 04011 00C01
03566 15 04059 00009
03578 31 00600 00621
03590 16 03825 000-1
03602 16 03823 00C-0

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13715	BNF	RCMSPC,EVALAD-7	03614	44	03874	03475
13725	TR	COLL-18,THINGS-20	03626	31	00600	00621
13735	TFM	LABL,1,10	03638	16	03825	000-1
13745	TFM	DOL,1,10	03650	16	03823	000-0
13755	B	ALL	03662	49	03862	00000
13765	DURG	*-3	03670			
13775		CHECK FOR COMMA				
13785	CM	INPUT+20,23,10	03670	14	00817	000K3
13795	BE	COMMER	03682	46	03886	01200
13805		CHECK FOR ASTERISK				
13815	CM	INPUT+20,14,10	03694	14	00817	000J4
13825	BE	ASTER	03706	46	04686	01200
13835		CHECK FOR DOLLAR SIGN				
13845	CM	INPUT+20,13,10	03718	14	00817	000J3
13855	BE	DOLLAR	03730	46	04150	01200
13865	TDM	LABL	03742	15	03825	00000
13875	CM	COLL-17,7,10	03754	14	00601	000-7
13885	BNE	B13	03766	47	03802	01200
13895		SYMBOL IN OPERAND CONTAINS MORE THAN SIX CHARACTERS.				
13905		NUMBER IN OPERAND HAS MORE THAN FIVE DIGITS OR				
13915		UNDEFINED SYMBOL IN OPERAND				
13925	TCM	SET2,				
13935	DC	1,*,*	03778	15	13312	00000
13945			03789		1	
13955	BTM	EVALER,50000	03790	17	05106	M0000
13965	DC	1,*,*	03801		1	
13975	TF	COLL,INPUT+20	03802	26	00618	00817
13985	CF	COLL-1	03814	33	00617	00000
13995	DS	*	03825		0	
14005	OS	*-2	03823		0	
14015	AM	DOL,1,10	03826	11	03823	000-1
14025	TDM	EVALAD-11	03838	15	03471	00000
14035	TR	COLL-17,10,15	03850	31	00601	00603
14045	TK	INPUT+19,INPUT+21	03862	31	00816	00818
14055		CHECK TO SEE IF OPERAND IS PRESENT				
14065	RCMSPC	DNR COMSPC,INPUT+20	03874	45	03906	00817
14075	COMMER	TCM RETURN+1,1	03886	15	04059	00C01
14085	B	GET1	03898	49	03974	00000
14095	DURG	*-3	03906			
14105		CHECK FOR SPECIAL CHARACTER				
14115	CM	INPUT+20,7C,10	03906	14	00817	00C0P0
14125	BNL	A13	03918	46	03754	01300
14135		CHECK FOR + OR -				
14145	BC	SI,INPUT+20	03930	43	03670	00817
14155		CHECK FOR BLANK				
14165	BD	H14,INPUT+19				
14175	B	ALL	03942	43	03962	00816
14185	TC	H15+11,INPUT+19	03954	49	03862	00000
14195	RC	ADRS,EVALAD-11	03962	25	04033	00816
14205	BT	GET,*,12,7	03974	43	04010	03471
14215	BT	MULT,MULT-1	03986	27	04294	-3998
14225	ADRS	A	03998	27	04600	04599
14235	R15	ADDRS,ALPHA,0	0401C	K1	01122	J0411
14245	TDM	AURS+1,1	04022	15	04611	00001
	TFM	EVALAD-9,100,9	04034	16	03473	00J00

[illegible]

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14785 A15	TR	NUMB-5,NUMB-4	04514	31	00643	00644
14795 TRNUM1	TD	NUMB-1	04526	25	00647	00000
14805	TR	COLL-17,COLL-15	04538	31	00601	00603
14815	TF	B21+11,TRNUM1+11	04550	26	04573	04577
14825 B21	BMR	A15	04562	45	04514	00000
14835	TFM	ALPHA	04574	16	00411	-0000
14845	A	ALPHA,NUMB-1	04586	21	00411	00647
14855	BB	*-0	04598	M2	00000	00000
14865	DORG	*-9	04600			
14875 MULT	M	ALPHA,BETA	04600	23	00411	12413
14885	C	89,CLERER+9	04612	24	00089	00741
14895	BE	B22	04624	46	04648	01200
14905 *						
14915 *						
14925	BTM	EVALER,20000	04636	17	05106	K0000
14935	DC	1,*,*	04647		1	
14945 B22	SF	90	04648	32	00090	00000
14955	TF	ALPHA,99	04660	26	00411	00099
14965	TF	BETA,99	04672	26	12413	00099
14975	BB	*-0	04684	M2	00000	00C00
14985	DORG	*-9	04686			
14995 ASTER	BC	TEST3,EVALAD-11	04686	43	04742	03471
15005	BT	GET,*+12,7	04698	27	04294	-4710
15015	BT	MULT,MULT-1	04710	27	04600	04599
15025	TFM	EVALAD-10,11,10	04722	16	03472	000J1
15035	B	A12	04734	49	03626	00060
15045	DCRG	*-3	04742			
15055 TEST3	BC	TFADD,EVALAD-10	04742	43	04766	03472
15065	BD	SM2,EVALAD-9	04754	43	04810	03473
15075 TFADD	TF	ALPHA,ADDCOM	04766	26	00411	00725
15085	BT	MULT,MULT-1	04778	27	04600	04599
15095	TFM	EVALAD-9,1,10	04790	16	03473	0C0-1
15105	B	A12	04802	49	03626	00000
15115	DORG	*-3	04810			
15125 SW2	TCM	EVALAD-9	04810	15	03473	00000
15135	B	A12	04822	49	03626	00000
15145	DORG	*-3	04830			
15155 LBADD	TF	LABCTR,COLL-17	04830	26	14217	00601
15165	TF	INPUT3,COLL-2	04842	26	01585	00616
15175	TFM	D33*6,FR5,7	04854	16	04952	-3778
15185	BT	IT,IT-1	04866	27	04922	04921
15195 LABOK	TF	B38+11,D26+11	04878	26	04913	05049
15205	AM	B38+11,5,10	04890	11	04913	000-5
15215 B38	TF	ALPHA	04902	26	00411	00000
15225	B	G4	04914	49	04286	00000
15235	DORG	*-3	04922			
15245 *						
15255 *						
15265 *						
15275 IT	TFM	A63+11,SYMTBL	04922	16	04945	J6818
15285 A63	BC	SEIFIN	04934	43	04954	00000
15295 D33	B		04946	49	00000	00000
15305	DORG	*-3	04954			
15315 SEIFIN	TF	C24+11,A63+11	04954	26	04977	04945
15325 D24	TC	D25+11	04966	25	05001	00000

THE SYMBOL TABLE IS SEARCHED FOR EQUIVALENCE

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15335	TF	L26+11,024+11	04978	26	05049	04977
15345	AM	L26+11,10	04990	11	05049	000-0
15355	A	026+11,025+11	05002	21	05049	05001
15365	C	LACR+025+11	05014	24	14217	05001
15375	BNE	L27	05026	47	05062	01200
15385	C	INPUT3	05038	24	01585	00000
15395	BE	RK	05050	46	06334	01200
15405	TF	A63+11,026+11	05062	26	04945	05049
15415	AM	A63+11,0,10	05074	11	04945	000-6
15425	B	A63	05086	49	04934	00000
15435	DURG	*-3	05094	45	59007	00000
15445	BNR	59007				
15455	*					
15465	*	EVALER IS THE ERROR ROUTINE				
15475	*					
15485	EVALER	BT LPRINT,EPRINT-1	05106	27	05310	05309
15495	BC	EVLEJS	05118	43	05174	00587
15505	BNC2	CHKND	05130	47	05222	00200
15515	TF	ADDCOM+PLACE	05142	26	00725	06365
15525	SM	INKRM,1,10	05154	12	15082	000-1
15535	B	A4	05166	49	02474	00000
15545	DORG	*-3	05174			
15555	RC2	AT	05174	46	05142	00200
15565	BNF	CHKND,PRSW	05186	44	05222	08664
15575	BT	RCY,RCY-1	05198	27	08618	08617
15585	BTM	TABBY1,*+12,7	05210	17	08524	-5222
15595	TFM	ADDCS	05222	16	01122	-0000
15605	RC	TUMR,SET2	05234	43	04130	13312
15615	BNR	B23,INPUT+20	05246	45	05266	00817
15625	B	IOBB	05258	49	04130	00000
15635	DURG	*-3	05266			
15645	CM	INPUT+20,23,10	05266	14	00817	000K3
15655	BE	IOBB	05278	46	04130	01200
15665	TR	INPUT+19,INPUT+21	05290	31	00816	00818
15675	B	M24,*2	05302	49	-5246	00000
15685	DORG	*-3	05310			
15695	*					
15705	*	EPRVI PRINTS THE ERROR MESSAGE AND REFERENCE TO				
15715	*	INDICATE THE STATEMENT IN ERROR				
15725	*					
15735	EPRINT	BNF B25,PRSW	05310	44	05334	08664
15745	BL	B26,EJS	05322	43	05382	00587
15755	B25	RCY	05334	34	00000	00102
15765	WATY	ERLAB	05346	39	01155	00100
15775	WNTY	INKRM-3	05358	38	15079	00100
15785	TBTY		05370	34	00000	00108
15795	WATY	EVALFR-11	05382	39	05095	00100
15805	RM		05394	42	00000	00000
15815	DURG	*-3	05402			
15825	WRPRND	C INPUT2+73,FINAL	05402	24	01032	15431
15835	BNE	B27	05414	47	05438	01200
15845	TUM	INPUT2+69,*11	05426	15	01028	0000-
15855	B27	BNC3 PC+CRD	05438	47	06262	00100
15865	TF	B28+6,WRPRND-1	05450	26	05468	05401
15875	R		05462	49	00000	00000
15885	DURG	*-3	05470			

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15895 *
15905 *      HEADER ROUTINE
15915 *
15925   TFM  HED,,10
15935   TCM  HEADER-1
15945   A10  BNR  COMA,INPUT+20
15955   A9   BNR  PASS1-EJS
15965   A8   BTM  LINE,,*12
15975   B    BT  PCHCRD,PCMRD-1
15985   B    READ
15995   DORG *-3
16005   COMA CM  INPUT+20,23,10
16015   BE   A9
16025 *      HEADER OPERAND GREATER THAN ONE CHARACTER
16035   BC   ER13,HEADER-1
16045   CM   INPUT+20,,10
16055   BE   B12
16065   CP   INPUT+20,40,10
16075 *      SPECIAL CHARACTER USED AS HEADER
16085   BL   ER12
16095   TF   HED,INPUT+20
16105   TCM  HEADER-1,1
16115   B12 TR  INPUT+19,INPUT+21
16125   B    A10
16135   DORG *-3
16145   ERI2 TFM  EVALER-1,17200
16155   DC   1,,*
16165   TFM  HED,,10
16175   B    A64
16185   DORG *-3
16195   ERI3 TFM  EVALER-1,17300
16205   DC   1,,*
16215   A64 BT  EPRINT,EPRINT-1
16225   BC2 A7
16235   B    A9
16245   DORG *-3
16255 *
16265 *      THE FOLLOWING ROUTINE PROVIDES A CONDENSED OBJECT DECK IF
16275 *      ONE IS DESIRED
16285 *
16295   CMPCON ILM  CONCD+11,1
16305   A19   TF  TEST,INPUT2+73
16315   S     TEST,INPUT2+68
16325   CM   SIXTY,60,10
16335   BNE   A16
16345   EMPTY TF  TYPE,INPUT2+63
16355   TF  CMPOUT+68,INPUT2+68
16365   A18   TFM  TR+11,INPUT2-1
16375   A     TR+11,INPUT2+63
16385   TR     CMPOUT,0,2
16395   A     TR+6,TEST
16405   TF  CMPOUT+73,INPUT2+73
16415   TF  TESTAD,INPUT2+73
16425   CONCC TCM  CMPOUT+61,1

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16435	TF	B29+11,TR+11	05922	26	05969	05873
16445	A	B29+11,TEST	05934	21	05969	08530
16455	SM	B29+11,1	05946	12	05969	-0001
16465	B29	BNR B30	05958	45	05978	00000
16475	B	A17	05970	49	06002	00000
16485	DORG	B-3	05978			
16495	S	SIXTY,TEST	05978	22	13337	08530
16505	BNZ	BB	05990	47	06334	01200
16515	A17	TDM BRRDBB+1,2	06002	15	06135	00002
16525	PUNCHY	TFM CPMOUT+63,1,10	06014	16	01557	000-1
16535	BNC4	B31	06026	47	06098	00400
16545	AM	ORDER,1	06038	11	02865	-0001
16555	TF	CPMOUT+79,ORDER	06050	26	01573	02865
16565	CF	CPMOUT+76	06062	33	01570	00000
16575	TDM	CPMOUT+75,0,11	06074	15	01569	0000-
16585	WNCD	CPMOUT	06086	38	01494	00400
16595	B31	TFM SIXTY,60	06098	16	13337	-0060
16605	TF	CPMOUT+74,BLKS	06110	26	01568	15268
16615	TFM	TR+6,CPMOUT	06122	16	05868	-1494
16625	BRRDRB	B EMPTY	06134	49	05814	00000
16635	DORG	B-3	06142			
16645	A16	C INPUT2+63,TYPE	06142	24	01022	02423
16655	BE	B32	06154	46	06186	01200
16665	B33	TDM BRRDBB+1,9	06166	15	06135	00009
16675	B	PUNCHY	06178	49	06014	00000
16685	DORG	B-3	06186			
16695	B32	C TLESTAD,INPUT2+68	06186	24	13217	01027
16705	BNE	B33	06198	47	06166	01200
16715	C	SIXTY,TEST	06210	24	13337	08530
16725	BL	B33	06222	47	06166	01300
16735	B	A18	06234	49	05838	00000
16745	DORG	B-3	06242			
16755	CMFINS	TCM COMCD+11,0	06242	15	05921	00000
16765	B	A19+2	06254	49	-5766	00000
16775	DORG	B-3	06262			
16785	*					
16795	*	PCMCRO PUNCHES A CARD NUMERICALLY				
16805	*					
16815	PCMCRO	BC3 BB	06262	46	06334	00300
16825	A5	BNC4 BB	06274	47	06334	00400
16835	AM	ORDER+1	06286	11	02865	-0001
16845	TF	INPUT2+79,ORDER	06298	26	01038	02865
16855	CF	INPUT2+76	06310	33	01035	00000
16865	WNCD	INPUT2	06322	38	00959	00400
16875	BB		06334	42	00000	00000
16885	DORG	B-3	06342			
16895	*					
16905	*	THE ROUTINE WHICH FOLLOWS TAKES CARE OF THE				
16915	*	OUTPUT FOR THE PROCESSOR				
16925	*					
16935	LINPRD	CF ACDS-4	06342	33	01118	00000
16945	CF	LNTH-4	06354	33	00700	00000
16955	PLACE	DS 5*	06365			
16965	CF	TEMPR-4	06366	33	00726	00000
16975	BTM	LINE,*+12	06378	17	06502	-6190
16985	TR	INPUT2+12,LNTH-4	06390	31	00971	00700

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16995 TD INPUT2+17,BLNKS
17005 *
17015 * IF A TYPED LISTING IS TO BE MADE, TYPE ADDRESS
17025 *
17035 BNF PRT1,PRSM
17045 BT SPAT,SPAT-1
17055 PRT1 BNF PRT2,GOODB+11
17065 R DOINST
17075 DORG *-3
17085 PRT2 TF BRNCH+6,LINPRT-1
17095 BNF BRNCH,PRSM
17105 *
17115 * IF A DECLARATIVE, ALSO TYPE LENGTH
17125 *
17135 WNTY LNTH-4
17145 BRNCH B
17155 DORG *-3
17165 *
17175 * PUNCH SOURCE STATEMENT AND PREPARE FOLLOWING CARD
17185 *
17195 LINE BT PCHALF,PCHALF-1
17205 TD INPUT2+4,INPUT-2
17215 TD INPUT2+3,INPUT-4
17225 TD INPUT2+2,INPUT-6
17235 TD INPUT2+1,PCHALF+7
17245 TDM INPUT2+9
17255 G22 TF INPUT2+79,BLNKS
17265 TR INPUT2+5,ADDRS-4
17275 TD INPUT2+10,BLNKS
17285 TF INPUT2+75,9
17295 TF 839+6,LINE-1
17305 B39 B
17315 DORG *-3
17325 GOODSB BNF GOODSB,PRSM
17335 *
17345 * IF DSB TYPE NUMBER OF ELEMENTS
17355 *
17365 SPTY TEMPR-4
17375 WNTY INPUT+18,XDSB-3
17385 DODS C
17395 BNE 840
17405 TR INPUT2+17,TEMPR-4
17415 840 BT PCHCRD,PCHCRD-1
17425 C INPUT+18,XDNB-3
17435 BNE LDLBL
17445 *
17455 * GENERATE OUTPUT CARDS FOR NUMERIC BLANK
17465 *
17475 TF INPUT2-2,INPUT-2
17485 TR INPUT2-1,CLERER
17495 TR INPUT2+52,CLERER
17505 TF INPUT2+112,CLERER+50
17515 TFM BLKVR+11,INPUT2+2
17525 A BLKVR+11,LNTH
17535 A BLKVR+11,LNTH
17545 TFM 841+6,INPUT2+2

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06402 25 00976 15268
06414 44 06438 08664
06426 27 08592 08591
06438 44 06458 03353
06450 49 07956 00000
06458 26 06500 06341
06470 44 06494 08664
06482 38 00700 00100
06494 49 00000 00000
06502
06502 27 07190 07189
06514 25 00963 00795
06526 25 00962 00793
06538 25 00961 00791
06550 25 00960 07197
06562 15 00959 00009
06574 26 01038 15268
06586 31 00964 01118
06598 25 00969 15268
06610 15 01034 00009
06622 26 06640 06501
06634 49 00000 00000
06642 44 06678 08664
06654 34 00000 00101
06666 38 00726 00100
06678 24 00815 16539
06690 47 06714 01200
06702 31 00976 00726
06714 27 06262 06261
06726 24 00815 16550
06738 47 14194 01200
06750 26 00957 00795
06762 31 00958 00732
06774 31 01011 00732
06786 26 01071 00762
06798 16 06881 -0961
06810 21 06881 00704
06822 21 06881 00704
06834 16 06852 -0961

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17555 141 TFM 34,10
17565 AM 841+6,2
17575 CM 841+6
17585 BNE 141
17595 TF 842+6,RLKVR+11
17605 R42 TFM 1,1
17615 DC 1,1
17625 TX INPUT2+113,BLSNO-1
17635 SF ADDR5-4
17645 AM ADDR5,1
17655 TC INPUT2+128,ADDR5-4
17665 TC INPUT2+130,ADDR5-3
17675 TC INPUT2+132,ADDR5-2
17685 TC INPUT2+134,ADDR5-1
17695 TC INPUT2+136,ADDR5
17705 TC 19,ADDR5-4
17715 CM FINAL
17725 BR,E 24
17735 TDM S ADDR5,LNTH
17745 S ADDR5+128,11
17755 TC INPUT2+118,ADDR5-4
17765 TC INPUT2+120,ADDR5-3
17775 TC INPUT2+122,ADDR5-2
17785 TC INPUT2+124,ADDR5-1
17795 TC INPUT2+126,ADDR5
17805 BT 8891,8891-1
17815 B1 A21,A21-1
17825 SM ADDR5,1
17835 A ADDR5,LNTH
17845 B LDLHL,12
17855 DCRG 1-1
17865
17875
17885
17895 PCHALF
17905 BNC4 BB
17915 TO PCHALF+7,INPUT-10
17925 TFM INPUT2-10,76,10
17935 TFM INPUT2+140,70,10
17945 A21 BNC4 BB
17955 AM ORDER,1,10
17965 TF INPUT2+147,SEVENS
17975 TC INPUT2+148,ORDER
17985 TC INPUT2+142,ORDER-3
17995 TC INPUT2+144,ORDER-2
18005 TC INPUT2+146,ORDER-1
18015 MACD INPUT2-10
18025 TFM INPUT2-10,00,10
18035 BB
18045 DCRG 1-1
18055
18065
18075
18085 PCUM,PKSM
18095 TYPDSA BNF PCUM,PKSM

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PCHALF ROUTINE PUNCHES A CARD ALPHABETICALLY

```

BC3 BB
BNC4 BB
TO PCHALF+7,INPUT-10
TFM INPUT2-10,76,10
TFM INPUT2+140,70,10
BNC4 BB
AM ORDER,1,10
TF INPUT2+147,SEVENS
TC INPUT2+148,ORDER
TC INPUT2+142,ORDER-3
TC INPUT2+144,ORDER-2
TC INPUT2+146,ORDER-1
MACD INPUT2-10
TFM INPUT2-10,00,10
BB
DCRG 1-1

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THE FOLLOWING ROUTINE HANDLES THE TYPED OUTPUT FOR DSA

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18065
18075
18085 PCUM,PKSM
18095 TYPDSA BNF PCUM,PKSM

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(6846 16 00000 000L4
06256 11 06852 -0002
06870 14 06852 -0000
06882 47 06846 01200
06894 26 06912 06881
06906 16 00000 000-9
06917 1
06918 31 01072 01456
06930 32 01118 00000
06942 11 01122 -0001
06954 25 01087 01118
06966 25 01089 01119
06978 25 01091 01120
06990 25 01093 01121
07002 25 01095 01122
07014 25 07033 01118
07026 14 15431 -0000
07038 47 07062 01200
07050 15 01087 0600-
07062 22 01122 00704
07074 25 01077 01118
07086 25 01079 01119
07098 25 01061 01120
07110 25 01083 01121
07122 25 01085 01122
07134 27 11592 11591
07146 21 07250 07249
07158 12 01122 -0001
07170 21 01122 00704
07182 49 J4194 00000
07190 46 06334 00300
07202 47 06334 00400
07214 25 07197 00787
07226 16 00949 000P6
07238 16 01099 000P0
07250 47 06334 00400
07262 11 02865 000-1
07274 26 01106 11905
07286 25 01107 02865
07296 25 01101 02862
07310 25 01103 02863
07322 25 01105 02864
07334 39 00949 00400
07346 16 00949 000-0
07358 42 00000 00000
07360
07360 44 07520 08664
07372 16 07419 -0500

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18105 A22 MATY CLERER+45
 18115 AM 345+11,5
 18125 B45 TF TYPADD-1
 18135 WNTY TYPADD-5
 18145 TF 841+11,845+11
 18155 AM 847+11,1,10
 18165 B47 BNR 846
 18175 B PCON
 18185 DORG *-3
 18195 B46 HT RCTV,ACTY-1
 18205 HTM TABBY1,G5,7
 18215 WNTY LNTM-4
 18225 B A22
 18235 DORG *-3
 18245 *
 18255 *
 18265 *
 18275 PCCN C INPUT+18,XDSA-3
 18285 B1 PDSA
 18295 B1 PCHRD,PCMRD-1
 18305 TF INPUT2+74,BLKS
 18315 TR INPUT2+62,CMSND-11
 18325 TFM PCON1+6,OUT+2
 18335 A PCON1+6,INPUT2+73
 18345 S PCON1+6,INPUT2+68
 18355 PCCN1 TC *RECMK
 18365 SM PCON1+6,OUT+2
 18375 CM PCON1+6,51
 18385 BN A23
 18395 TD PCON2+11,OUT+52
 18405 TC OUT+52,RECMK
 18415 TR INPUT2+5,OUT+2
 18425 TF PCON3+11,INPUT2+73
 18435 TF INPUT2+73,INPUT2+68
 18445 AM INPUT2+73,50
 18455 BTM WRPND,CMPCON
 18465 PCON2 TCM OUT+2
 18475 TR OUT+3,OUT+53
 18485 TF INPUT2+68,INPUT2+73
 18495 TF INPUT2+61,BLKS-18
 18505 PCON3 TFM INPUT2+73
 18515 A23 TR INPUT2+5,OUT+2
 18525 BTM WRPND,CMPCON
 18535 B LDL8L
 18545 DORG *-3
 18555 POSA TR INPUT2+62,DSASND-11
 18565 A24 AM INPUT2+73,5
 18575 TF INPUT2+68,5
 18585 TC INPUT2+21,ZEPO+5
 18595 BTM WRPND,CMPCON
 18605 AM INPUT2+9,5
 18615 TR ZEP+1,ZEPO+6
 18625 BNR A24,ZEPO+1
 18635 B LDL8L
 18645 DORG *-3
 18655

PUNCH THE CONSTANT CARDS

07384 39 00777 00100
 07396 11 07419 -0005
 07408 26 08610 00000
 07420 38 08606 00100
 07432 26 07467 07419
 07444 11 07467 CDS-1
 07456 45 07476 00000
 07468 49 07520 00000
 07476
 07476 27 08618 08617
 07488 17 08524 -8580
 07500 38 00700 00100
 07512 49 07384 00000
 07520
 07520 24 00815 16528
 07532 46 07840 01200
 07544 27 06262 06261
 07556 26 01033 15268
 07568 31 01021 15269
 07580 16 07622 -0420
 07592 21 07622 01032
 07604 22 07622 01027
 07616 25 00000 C1796
 07628 12 07622 -0420
 07640 14 07622 -0051
 07652 47 07808 01360
 07664 25 07759 00470
 07676 25 00470 01796
 07688 31 00964 00420
 07700 26 07807 01032
 07712 26 01032 01027
 07724 11 01032 -0050
 07736 17 05402 -5754
 07748 15 00420 00000
 07760 31 00421 00471
 07772 26 01027 01032
 07784 26 01020 15250
 07796 16 01032 -0000
 07808 31 00964 00420
 07820 17 05402 -5754
 07832 49 14194 00000
 07840
 07840 31 01021 15288
 07852 11 01032 -0005
 07864 11 01027 -0005
 07876 26 00980 00505
 07888 25 00981 01796
 07900 17 05402 -5754
 07912 11 00968 -0005
 07924 31 00501 00506
 07936 45 07852 00501
 07948 49 14194 00000
 C7956

AFIT VERSION 1620 SPS

OUTPUT ROUTINE FOR INSTRUCTIONS AND LINKAGES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													
18665 *																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													

AFIT VERSION 1620 SPS

19225 SUBENT DS 5,-*-5
 19235 T8TY 75000
 19245 DC 1,-*-4
 19255 TF G25+6,TABBY1-1
 19265 G25 6
 19275 DORG *-3
 19285 G5 AM ADDKS+5,10
 19295 SPAT WNTY ADDKS-4
 19305 SPTV
 19315 TYPADD DS *-4
 19325 DC 1,-*-4
 19335 BB
 19345 DORG *-9
 19355 RCTY TDM PRSM,0
 19365 BNCL 8B
 19375 TDM PRSM,-1
 19385 RCTY1 RCTY
 19395 PRSM DS 1,-*-1
 19405 SM RCNT,1,10
 19415 BP 8B
 19425 TFM RCNT,6,10
 19435 RC2 RCTY
 19445 RCNT DS 2,-*-4
 19455 SM RCNT,1,10
 19465 BP RC2
 19475 TFM RCNT,61,10
 19485 BB
 19495 DORG *-9
 19505 PRDAS BTM LINPRT,DDDS,8
 19515 INST BTM INSTRN,FLAGGR
 19525 B1 BTM INSTRN,DOBI
 19535 BNI BTM INSTRN,DOBN1
 19545 RDM BTM INSTRN,UORDM
 19555 K BTM INSTRN,DOOK
 19565 DOBI TFM SMDUP+11,46,9
 19575 B A27
 19585 DORG *-3
 19595 DOBN1 TFM SMDUP+11,47,9
 19605 A27 TD ZEPO+9,ZEPO+1
 19615 TD ZEPO+8,ZEPO
 19625 SMCOP TFM ZEPO+1
 19635 B FLAGGR
 19645 DORG *-3
 19655 DORDM TD B49+11,ZEPO
 19665 B49 TFM SMCUP+11,3C,9
 19675 A28 TDM ZEPO
 19685 B A27
 19695 DORG *-3
 19705 JUST TC H50+11,ADDCOM
 19715 B50 TC B51+11,AJUST
 19725 B51 AM ADCCOM
 19735 TFM ADDKS,ADDCOM
 19745 BB
 19755 DORG *-9

PAGE 20

08542 5
 08548 34 75000 00108
 08555 1
 08560 26 08578 08523
 08572 49 00000 00000
 08580
 C8580 11 01122 000-5
 08592 38 01118 00100
 08604 34 00000 00101
 08611 0
 08611 1
 08616 42 00000 00000
 08618
 08618 15 08664 00000
 08630 47 06334 00100
 08642 15 08664 0000J
 08654 34 00000 00102
 08664 1
 08666 12 08709 000-1
 08678 46 06334 01100
 08690 16 08709 000-6
 08702 34 00000 00102
 08709 2
 08714 12 08709 000-1
 08726 46 08702 01100
 08738 16 08709 00001
 08750 42 00000 00000
 08752 17 06342 01678
 08764 17 09030 -9262
 08776 17 09030 -8824
 08788 17 09030 -8844
 08800 17 09030 -8900
 08812 17 09030 -8994
 08824 16 08891 00-46
 08836 49 08856 00000
 08844
 08844 16 08891 00-47
 08856 25 00509 00501
 08868 25 00508 00500
 08880 16 00501 -0000
 08892 49 09262 00000
 08900
 08900 25 08923 00500
 08912 16 08891 00-30
 08924 15 00500 00000
 08936 49 08856 00000
 08944
 08944 25 08967 00725
 08956 25 08979 00599
 08968 11 00725 -0000
 08980 26 01122 00725
 08992 42 00000 00000
 08994

19765 DOK TFM SNOOP+11,34,9
19775 TD ZEPD+11,ZEPD
19785 B AZH
19795 •
19805 • ASSEMBLE INSTRUCTION
19815 •
19825 INSTRN IR ZEPD,CLEVER+41
19835 BT JUST,JUST-1
19845 BC H52,EJS
19855 AM ADDCOM+11,10
19865 B LDHML
19875 DORG *-3
19885 R52 TF TEMP,ADDCOM
19895 TC ZEPD,ZEPD+28
19905 TD ZEPD+1,ZEPD+29
19915 HTM EVALAD,*+12,4
19925 TF ZEPD+6,ADDRS
19935 CF ZEPD+2
19945 BNR H53,INPUT+20
19955 B TYPINS
19965 DORG *-3
19975 B53 BTM EVALAD,*+12,5
19985 TF ZEPD+11,ADDRS
19995 CF ZEPD+7
20005 TYPINS TF ADDR5,ADDCOM
20015 AM ADDCOM+11,10
20025 TF B54+6,INSTRN-1
20035 •
20045 •
20055 •
20065 B54 B
20075 •
20085 •
20095 •
20105 FLAGGR BNR B55,INPUT+20
20115 B SELIM
20125 DORG *-3
20135 •
20145 •
20155 •
20165 SECIM TD R56+9,ZEPD
20175 R56 CM *-9,1,810
20185 BME LINPRT
20195 C *-2,3,ZEPD+1
20205 BE LINPRT,15,10
20215 SF ZEPD+7
20225 B LINPRT
20235 DORG *-3
20245 B55 BTM CKREC,SEEIM
20255 •
20265 •
20275 •
20285 TRANS TM INPUT+19,INPUT+21
20295 B56 BNR B57,INPUT+20
20305 B LINPRT
20315 DORG *-3

BRANCH TO CHECK FOR FLAGS OR INSERT Q MODIFIER

CHECK TO SEE IF THERE IS A FLAG OPERAND

SET FLAG IF IMMEDIATE INSTRUCTION

SCAN FLAG OPERAND

08494 16 08891 00-34
09006 25 00511 00500
09018 49 08924 00000

09036 31 00560 00773
09042 27 08944 08943
09054 43 09086 00587
09066 11 00725 00CJ1
09078 49 14194 00000
09086
09086 26 00406 00725
09098 25 00500 00528
09110 25 00501 00529
09122 17 03A82 09134
09134 26 00506 01122
09146 33 00502 00C0C
09158 45 09178 00817
09170 49 09214 00C00
09178
09178 17 034C2 09190
09190 26 00411 01122
09202 33 00507 00000
09214 26 01122 00725
09226 11 00725 00CJ1
09238 26 09256 00029

09250 49 00000 00000

09262 45 09362 00817
09274 49 09282 00000
09282

09282 25 09303 00500
09294 14 09303 0-0-1
09306 47 06342 01200
09318 24 09341 00501
09330 46 06342 012J5
09342 32 00507 00000
09354 49 06342 00000
09362
09362 17 10066 -9282

09374 31 00816 00818
09386 45 09406 00817
09398 49 06342 00000
09406

AFIT VERSION 1620 SPS

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20325 B57 BC B58,INPUT+19
20335 B TRANS
20345 DORG *-3
20355 B58 CM INPUT+20,23,10
20365 BE LIMPRT
20375 CM INPUT+20,71,10
20385 BNE ABLE
20395 BNR B59,INPUT+22
20405 B ABLE
20415 DORG *-3
20425 B59 CM INPUT+22,70,10
20435 BNE BAKK
20445 SF ZIPO+10
20455 CHAR TR INPUT+19,INPUT+23
20465 B B60
20475 DORG *-3
20485 BAKR CM INPUT+22,71,10
20495 BNE ABLE
20505 BNR B61,INPUT+24
20515 B ZERONE
20525 DORG *-3
20535 B61 CM INPUT+24,70,10
20545 BNE ZERONE
20555 ABLE IC B62+6,INPUT+20
20565 B62 SF ZEP0
20575 B TRANS
20585 DORG *-3
20595 ZERONE SF ZEP0+11,7071,810
20605 B CHAR
20615 DORG *-3
20625 MACRO B1 JUST,JUST-1
20635 A29 SF ZEP0+28
20645 T1 A29+11,ZEP0+29
20655 *
20665 * SET ZERO TO INDICATE SUBROUTINE IS REQUIRED
20675 *
20685 TFM B65+6,1STAT-30
20695 A B65+6,ZEP0+29
20705 B65 TCM
20715 B DSA,,,TO DSA ROUTINE TO COUNT NUMBER OF OPERANDS
20725 DORG *-3
20735 *
20745 * ASSEMBLE LINKAGE
20755 *
20765 MAC1 TF DSASND,ADDRS
20775 TF DSASND-5,ADDRS
20785 AM DSASND,19,10
20795 AM DSASND-5,14,10
20805 TR OUT,ZEP0+1
20815 TR ZEP0,LINK
20825 TR ZEP0+24,OUT
20835 A ZEP0+11,ADDRS
20845 A ZEP0+6,PICKUP
20855 TFM B66+11,ENTABL-7
20865 B67 C
20875 B66 C A29+11

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09406 43 09426 00816
09418 49 09374 00000
09426 14 00817 000K3
09438 46 06342 01200
09450 14 00817 000P1
09462 47 09618 01200
09474 45 09494 00819
09486 49 09618 00000
09494 14 00819 00CP0
09506 47 09550 01200
09518 32 00510 00000
09530 31 00816 00820
09542 49 09386 00C00
09550 14 00819 000P1
09562 47 09618 01200
09574 45 09594 00821
09586 49 09650 00000
09594 14 00821 000P0
09606 47 09650 01200
09618 25 09636 00817
09630 32 00500 00000
09642 49 09374 00000
09650 32 00511 0P0P1
09662 49 09530 00000
09670 27 08944 08943
09682 32 00528 00000
09694 26 09693 00529
09706 16 09736 -0659
09718 21 09736 00529
09730 15 00000 00000
09742 49 13614 00000
09750
09750 26 15299 01122
09762 26 15294 01122
09774 11 15299 00CJ9
09786 11 15294 00UJ4
09798 31 00418 00501
09810 31 00500 01128
09822 31 00524 00418
09834 21 00511 01122
09846 21 00506 02984
09858 16 09893 -1585
09870 11 09893 -0C07
09882 24 09693 00000

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20885 BNE B67
 20895 TF B68+11,M66+11
 20905 SM B68+11,2,10
 20915 R68 TF ZEPH+18
 20925 CF ZEPH+2
 20935 CF ZEPH+14
 20945 B LINPUT
 20955 DORG *-3
 20965 •
 20975 •
 20985 •
 20995 DAS
 21005 TF LNMH,ADDRS
 21015 TF TEMPR,LNTH
 21025 A TEMPR,TEMPR
 21035 TFM F1+6,PRDAS
 21045 BNR DAC3,INPUT+20
 21055 TFM G14+6,MDSINE,7
 21065 G14 B MDSINE
 21075 DORG *-3
 21085 •
 21095 •
 21105 •
 21115 CKREC
 21125 BNR BR2,INPUT+22
 21135 BR1
 21145 DORG *-3
 21155 DW2 CM INPUT+22,23,10
 21165 BE BR1
 21175 BB
 21185 DORG *-9
 21195 •
 21205 •
 21215 •
 21225 DAC
 21235 TF INPUT+18,XDAS-3
 21245 BTM LVALAD,*+12,4
 21255 TF LNMH,ADDRS
 21265 CM LNTH,51
 21275 BNN ERCON
 21285 A ADDRMS,ADDRS
 21295 TF TEMPR,ADDRS
 21305 BNR H71,INPUT+20
 21315 B ERCON
 21315 DORG *-3
 21325 BNR B72,INPUT+22
 21335 B ERCON
 21345 DORG *-3
 21355 B72 TFM CHVALD+11,INPUT+19
 21365 A CHVALD+11,TEMPR
 21375 CHVALD TR OUT+2
 21385 BNR B73,OUT+3
 21395 B ERCON
 21405 DORG *-3
 21415 B73 BNR B74,OUT+5
 21425 B B75
 21435 DORG *-3

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09894 47 09870 01200
 09906 26 09941 09493
 09918 12 09941 000-2
 09930 26 00518 00000
 09942 33 00502 00000
 09954 33 00514 00000
 09966 49 06342 00000
 09974
 09974 17 03M82 09996
 09986 26 00704 01122
 09998 26 00730 00704
 10010 21 00730 00730
 10022 16 10678 -8752
 10034 45 10680 00617
 10046 16 10064 00600
 10058 49 10600 00000
 10066
 10066 26 10096 10065
 10078 45 10098 00819
 10090 49 00000 00000
 10098
 10098 14 00819 000K3
 10110 46 10090 01200
 10122 42 00000 00000
 10124
 10124 26 00815 16484
 10136 17 03M82 00148
 10148 26 00704 01122
 10160 14 00704 -0051
 10172 46 12826 01300
 10184 21 01122 01122
 10196 26 00730 01122
 10208 45 10228 00817
 10220 49 12826 00000
 10228
 10228 45 10248 00819
 10240 49 12826 00000
 10248
 10248 16 10283 -0816
 10260 21 10283 00730
 10272 31 00420 00000
 10284 45 10304 00421
 10296 49 12826 00000
 10304
 10304 45 10324 00423
 10316 49 10348 00000
 10324

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21445 B74	CM	OUT+5,23,10	10324 14	00423	000K3
21455 STCHAR	BNE	ERCON	10336 47	12826	01200
21465 B75	TD	STCHAR+11,OUT+5	10348 25	10347	00423
21475	AM	CHVALD+11,3	10360 11	10283	-0003
21485	TF	B76+6,CHVALD+11	10372 26	10390	10283
21495 B76	TFM	*,10	10384 16	00000	000-0
21505	DC	1,*,*	10395	1	
21515	CM	UUT+3,34,10	10396 14	00421	000L4
21525	BNE	A32	10408 47	10456	01200
21535	TF	B77+6,CHVALD+11	10420 26	10450	10283
21545	SM	B77+6,2,10	10432 12	10450	000-2
21555 B77	TFM	*,10	10444 16	00000	000-0
21565	DC	1,*,*	10455	1	
21575 A32	TR	OUT+2,INPUT+21	10456 31	00420	00818
21585	TF	B78+11,CHVALD+11	10468 26	10503	10283
21595	AM	B78+11,1	10480 11	10503	-0001
21605 B78	TR	INPUT+21	10492 31	00818	00000
21615	TFM	B79+6,OUT+4	10504 16	10546	-0422
21625	A	B79+6,TEMPR	10516 21	10546	00730
21635 B80	SM	B79+6,2,10	10528 12	10546	000-2
21645 B79	CF		10540 33	00000	00000
21655	CM	B79+6,OUT+4	10552 14	10546	-0422
21665	BNE	B80	10564 47	10528	01200
21675	BMR	DAC3,STCHAR+11	10576 45	10680	10347
21685	*	ADDRESS ASSIGNED BY PROCESSOR			
21695	*				
21705	TFM	F1+6,F2	10588 16	10678	J0704
21715 MOSINE	BT	JUST,JUST-1	10600 27	08944	08943
21725	AM	ADDCOM,1	10612 11	00725	-0001
21735	AP	ADDRS,1	10624 11	01122	-0001
21745	A	ADDCOM,TEMPR	10636 21	00725	00740
21755	SM	ADDCOM,2,10	10648 12	00725	000-2
21765 F3	BMR	LDLBL,EJS	10660 45	14194	00567
21775 F1	B		10672 49	00000	00000
21785	DORG	*-3	10680		
21795 DAC3	BTM	CKREC,MOSINE	10680 17	10666	J0600
21805	BTM	EVALAD,F3,5	10692 17	03402	10660
21815 F2	TF	CONSND-5,ADDRS	10704 26	15275	01122
21825	SM	CONSND-5,1	10716 12	15275	-0001
21835	TF	CONSND,CONSND-5	10728 26	15280	15275
21845	A	CONSND,TEMPR	10740 21	15280	00730
21855	BTM	LINPRF,PCON	10752 17	06342	-7520
21865	*	EVALUATE LENGTH OF DSB			
21875	*				
21885	*				
21895 DSB	TF	INPUT+18,XDS-3	10764 26	00815	16462
21905	BTM	EVALAD,*,12,4	10776 17	03M82	10788
21915	TF	LNTH,ADDRS	10788 26	00704	01122
21925	BMR	R83,INPUT+20	10800 45	10832	00817
21935 A33	TFM	EVALER-1,70000	10812 16	05105	P0000
21945	DC	1,*,*	10823	1	
21955	R	A34	10824 49	12838	00000
21965	DORG	*-3	10832		

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PAGE

10632 17 10066 J0812

RTM CKREC,A33
EVALUATE NUMBER OF ELEMENTS OF DSB

10844 17 03442 10856
10856 26 00730 01122
10868 45 10876 00817

ADDRESS ASSIGNED BY PROCESSOR

10880 21 00725 00704
10892 23 00704 01122
10904 32 00095 00000
10916 22 00099 00704
10928 26 01122 00725
10940 21 00725 00099
10952 45 14194 00587
10964 17 06342 -6642
10976 17 10066 J0880

ADDRESS ASSIGNED BY PROGRAMMER

10988 17 01402 11000
11000 45 14194 00587
11012 17 06342 -6642

EVALUATE LENGTH OF DS OR DNB

11024 17 03M82 11036
11036 26 00704 01122
11048 43 11084 00529
11060 14 00704 -0051

BRANCH IF LENGTH OF DNB IS GREATER THAN 50

11072 46 12826 01300
11084 45 11188 00817

ADDRESS ASSIGNED BY PROCESSOR

11096 26 01122 00725
11108 21 00725 00704
11120 43 11152 00528
11132 21 01122 00704
11144 49 11164 00000
11152 11 01122 000-1
11164 45 14194 00587
11176 17 06342 -6678
11188 17 10066 J1096

ADDRESS ASSIGNED BY PROGRAMMER

11200 17 03402 11164
11212 17 03M82 11224
11224 11 00725 -0001

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```

22535 LYNN TF SHEILA+11,ADDCOM
22545 S SHEILA+11,ADDCOM
22555 BP LYNN
22565 SHEILA SM ADDCOM
22575 TF ADDR,ADDCOM
22585 B G1
22595 DORG *-3
22605 DORG BTM EVALAD,*+12,4
22615 TF ADDCOM,ADDCOM
22625 *
22635 *
22645 *
22655 G1 SM ADDCOM,1,10
22665 BNN H85
22675 TFM ADDCOM,99999
22685 885 BNR LDLBL,EJS
22695 CF ADDR-4
22705 BNF A8,PRSW
22715 WNTY ADDR-4
22725 BTM LINE,*+12
22735 BT PCMCRO,PCMCRO-1^
22745 B LDLBL
22755 DORG *-3
22765 *
22775 *
22785 *
22795 DEND BTM EVALAD,*+12,4
22805 TFM MESS1+24,49,10
22815 *
22825 *
22835 *
22845 BC OVER,EJS
22855 BD PASS1,ZEPO+29
22865 BCI A38
22875 WACD INPUT2-10
22885 PNC+11 B A38
22895 DORG *-3
22905 OVER TF GOTU,ADDCOM
22915 CF ADAMS-4
22925 DC 3,G,*
22935 L
22945 BC H88,ZEPO+29
22955 TDM GOTU-17,8
22965 B 887
22975 DORG *-3
22985 BNC3 88
22995 CM SIXTY,60
23005 BNE A17
23015 88
23025 DORG *-9
23035 888 TDM GOTU-17,1
23045 887 BNF 889,PRSW
23055 WNTY ADDR-4
23065 889 BT 8891,8891-1
23075 BTM LINE,*+12

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SET ADDRESS COUNTER TO NEW VALUE

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11236 26 11283 00725
11248 22 11283 01122
11260 46 11248 01100
11272 12 00725 -0000
11284 26 01122 00725
11296 49 11328 00000
11304
11304 17 03M82 11316
11316 26 00725 01122

11328 12 00725 000-1
11340 46 11364 01300
11352 16 00725 R9999
11364 45 14194 00587
11376 33 01118 00000
11388 44 05518 08664
11400 38 01118 00100
11412 17 06502 J1424
11424 27 06262 06261
11436 49 14194 00000
11444

11444 17 03M82 11456
11456 16 01195 000M9

11468 43 11536 00587
11480 43 02426 00529
11492 16 01195 000-0
11504 46 11714 00100
11516 39 00949 00400
11528 49 11714 00000
11536
11536 26 15132 01122
11548 33 01118 00000
11559 3

11560 43 11630 00529
11572 15 15115 00008
11584 49 11642 00000
11592
11592 47 06334 00300
11604 14 13337 -0060
11616 47 06002 01200
11628 42 00000 00000
11630
11630 15 15115 00001
11642 44 11666 08664
11654 38 01118 00100
11666 27 11592 11591
11678 17 06502 J1690

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AFIT VERSION 1620 SPS

PAGE

11690 27 06262 06261
11702 43 12138 00529
11714 27 08618 08617
11726 24 15113 00889

BRANCH IF SUBROUTINES ARE TO BE LOADED

11738 47 12434 01200
11750 43 12138 00587
11762 39 01171 00100
11774 25 00587 01796

PRINT SYMBOL TABLE AND PROCEED TO PASS 11

11786 16 11893 J6817
11798 15 11808 -0005
11810 27 08618 08617
11822 31 00500 06762
11834 16 11973 -0000
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23635 *	TF	INPUT2+79,BLNKS-60	12210	26	01038	15208
23645 PTBL	TF	B90+6,OUT+6	12222	26	12240	00424
23655	TD	,RECMK	12234	25	00000	01796
23665 B90	TF	E91+11,OUT+2	12246	26	12269	00420
23675	TR	INPUT2	12258	31	00959	00000
23685 B91	TDM	INPUT2+75,11	12270	15	01034	0000-
23695	BT	A5,A5-1	12282	27	06274	06273
23705	TF	B92+6,OUT+6	12294	26	12312	00424
23715	TD	,OUT+3	12306	25	00000	00421
23725 B92	TR	OUT,OUT+4	12318	31	00418	00422
23735	BMK	PTBL,OUT+3	12330	45	12210	00421
23745 *						
23755 *						
23765 *						
23775 *						
23785	TR	INPUT2,GOTO-18	12342	31	00959	15114
23795	TR	INPUT2+32,GOTO+14	12354	31	00991	15146
23805	BT	A5,A5-1	12366	27	06274	06273
23815	RC	PLOR,ZEPO+29	12378	43	02586	00529
23825	WATY	MESS1	12390	39	01171	00100
23835 *						
23845 *						
23855 *						
23865 *						
23875 A42	H		12402	48	00000	00000
23885 BETA	DS	10,0	12413		10	
23895	BC3	INIT2	12414	46	01810	00300
23905	B	INIT1	12426	49	01798	00000
23915	DORG	0-3	12434			
23925 *						
23935 *						
23945 *						
23955 *						
23965 MACROS	BC	WRMS,EJS	12434	43	12678	00587
23975	AT	JUST-JUST-1	12446	27	08944	08943
23985	TF	SUBENT,ADDCOM	12458	26	08542	00125
23995 DIN	TFM	CNTR,10	12470	16	02521	000-0
24005	TFM	DJD+11,1STAT-30	12482	16	12565	-0659
24015	TFM	A45+6,ENTABL-7	12494	16	12584	-1585
24025 A47	AM	CNTR,1,10	12506	11	02521	000-1
24035	AM	DJD+11,1,10	12518	11	12565	000-1
24045	CM	DJD+11,1,1STAT	12530	14	12565	-0689
24055	BE	A46	12542	46	12646	01200
24065 DJD	BD	A47	12554	43	12506	00000
24075	AM	A45+6,7,10	12566	11	12584	000-7
24085 A45	TF	,CNTR	12578	26	00000	02521
24095	TF	B99+6,A45+6	12590	26	12620	12584
24105	SM	B99+6,2,10	12602	12	12620	000-2
24115 B99	TF	,SUBENT	12614	26	00000	08542
24125	AM	SUBENT,20,10	12626	11	08542	000K0
24135	B	A47	12638	49	12506	00000
24145	DORG	0-3	12646			
24155 A46	TF	PICKUP,SUBENT	12646	26	02984	08542
24165	TD	NOISE,OUT+3,,STORE NOISY DIGIT	12658	25	14697	00421
24175	B	A48	12670	49	11762	00000
24185	DORG	0-3	12678			

HALT AND PROCEED TO PROCESS PASS1 OF NEW PROGRAM
OR PASS11 OF SAME PROGRAM AGAIN IF SW. 3 IS ON

STORE ADDRESSES OF PICK ROUTINE AND SECONDARY LINKAGES OF
SUBROUTINES USED

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24195 HRMS      WATY MESS2
24205 H
24215 DC 8.5,*
      -000005*
24225 DNB 2,*-6
24235 *
24245 *
24255 *
24265 *
24275 *
24285 *
24295 *
24305 *
24315 DC
24325 *
24335 *
24345 *
24355 D2
24365 D1
24375 *
24385 *
24395 *
24405 *
24415 *
24425 ERCON
24435 *
24445 A34
24455 BT
24465 BC2 A7
24475 TF PLACE,ADDCOM
24485 BMR OP,EJS
24495 BT RCTY1,RCY1-1
24505 BTM TABBY1,OP,7
24515 D3
24525 SF
24535 TCM SFLAG+1,3
24545 B A70
24555 DORG *-3
24565 CCOMER CM INPUT+22,23,10
24575 BE A50
24585 BH A51
24595 BC ERCON,INPUT+22
24605 BC DA,INPUT+21
24615 B TRREC
24625 DORG *-3
24635 D4
24645 B TRREC
24655 DORG *-3
24665 *
24675 *
24685 *
24695 A51
24705 TF SFLAG+11,INPUT+22
24715 TC ZEPO+51,INPUT+22
24725 TRREC TR INPUT+19,INPUT+21

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12678 39 01201 00100
12690 48 00000 00000
12701 8
12695 2
12702 49 15354 00000
12710
12710 43 12742 00528
12722 26 00815 16462
12734 49 12754 00000
12742
12742 26 00815 16473
12754 25 12709 00528
12766 17 03M82 12778
12778 26 00704 01122
12790 14 00704 -0051
12802 46 12826 01300
12814 45 12922 00817
12826 16 05105 00000
12837 1
12838 31 00816 01263
12850 27 05310 05309
12862 46 05142 00200
12874 26 06365 00725
12886 45 03002 00587
12898 27 08654 08653
12910 17 08524 -3002
12922 31 00499 00732
12934 32 00500 00000
12946 15 13135 00003
12958 49 13102 00000
12966
12966 14 00819 00083
12978 46 13114 01200
12990 46 13054 01100
13002 43 12826 00819
13014 43 13034 00818
13026 49 13090 00000
13034
13034 15 13135 00002
13046 49 13090 00000
13054
13054 26 13145 00819
13066 25 00501 00819
13078 31 00500 00501
13090 31 00816 00818

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24735 A70	BNR	CCOMER,INPUT+22	13102	45	12966	00819
24745 A50	BNF	SFLAG,ZEPO	13114	44	13134	00500
24755	W	ERCUM	13126	49	12826	00000
24765	WURG	8-3	13134			00000
24775 SFLAG	SF	ZEPU+50	13134	32	00550	00000
24785	CM	SFLAG+11,34,10	13146	14	13145	000L4
24795	MNE	A52	13158	47	13206	01200
24805	BNF	D5,ZEPO+50	13170	44	13194	00550
24815	SF	ZEPO+49	13182	32	00549	00000
24825 D5	TC	ZEPU+50,RECMK	13194	25	00550	01796
24835 A52	SF	ZEPU	13206	32	00550	00000
24845	TESTAD	D5	13217			5
24855	IFM	D8+6,ZEPO+50	13218	16	13248	-0550
24865	S	D8+6,LNTH	13230	22	13248	00704
24875 D6	C	CLEREN+49	13242	24	00000	00781
24885	BNE	ERCON	13254	47	12826	01200
24895	TF	D7+11,D8+6	13266	26	13289	13248
24905 D7	TR	ZEPU	13278	31	00500	00000
24915	BD	D8,DC-1	13290	43	13314	12709
24925	SF	ZEPU+1	13302	32	00501	00000
24935 SET	DC	1,0,0	13313			1
24945 SET2	DC	1,0,0-1	13312			1
24955 D8	BNR	D9,ZEPO+1	13314	45	13338	00501
24965	CF	ZEPU+1	13326	33	00501	00000
24975 SIXTY	DC	5,60,0	13337			5
24985 D9	BNR	CHECK,INPUT+22	13338	45	13502	00819
24995		ADDRESS ASSIGNED BY PROCESSOR				
25005						
25015						
25025 GOAND	TF	ADDRS,ADDCOM	13350	26	01122	00725
25035	A	ADDCOM,LNTH	13362	21	00725	00704
25045	TF	CONSHD,ADDCOM	13374	26	15280	00725
25055	AM	CONSHD,1,10	13386	11	15280	000-1
25065	BC	DSC,DC-1	13398	43	13430	12709
25075	A	ADDRS,LNTH	13410	21	01122	00704
25085	B	A53	13422	49	13442	00000
25095	DORG	8-3	13430			000-1
25105 DSC	AM	ADDRS,1,10	13430	11	01122	000-1
25115 A53	BNR	LDLBL,EJS	13442	45	14194	00587
25125	TR	OUT+2,ZEPO+1	13454	31	00420	00501
25135	TF	CONSHD-5,CONSHD	13466	26	15275	15280
25145	S	CONSHD-5,LNTH	13478	22	15275	00704
25155 PRDCSA	RTM	LIMPRT,PCOM	13490	17	06342	-7520
25165 CHECK	TR	INPUT+19,INPUT+21	13502	31	00816	00818
25175	RTM	CHKLC,GOAND	13514	17	10066	13350
25185	TR	INPUT+19,INPUT+21	13526	31	00816	00818
25195		ADDRESS ASSIGNED BY PROGRAMMER				
25205						
25215						
25225	RTM	EVALAD,8+12,4	13538	17	03M82	13550
25235	TF	CONSHD,ADDRS	13550	26	15280	01122
25245	WD	G11,DC-1	13562	43	13594	12709
25255	AM	CONSHD,1,10	13574	11	15280	000-1

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25265      0 A53
25275 DORG *-3
25285 D11 A CONSND,LNTH
25295      8 A53
25305 DORG *-3
25315 DSA TFM TRDSA+6,96,10
25325 CF GOEVAL+5
25335 BNR A54,EJS
25345 *
25355 * COLLECT OPERANDS
25365 *
25375 GOEVAL BTM EVALAD,*,12,4
25385 AM TRDSA+6,5,10
25395 CM TRDSA+6,51,10
25405 8L TRDSA
25415 LRDSA TFM EVALER-1,60000
25425 DC 1,*,*
25435 BT EPRINT,EPRINT-1
25445 BC2 A7
25455 TFM TRDSA+5,51,10
25465 BNR A56-EJS
25475 BT RCTY1,RCY1-1
25485 BTM TABBY1,A57,7
25495 *
25505 *
25515 *
25525 A55 CM INPUT+20,23,10
25535 BNE D12
25545 AM TRDSA+6,5,10
25555 D12 TR INPUT+19,INPUT+21
25565 A54 BNR A55,INPUT+20
25575 AM TRDSA+6,5,10
25585 CM TRDSA+6,51,10
25595 BNR ERDSA
25605 B A56
25615 TRDSA TR ZEPO,ADDRS-4
25625 A57 SF GOEVAL+5
25635 BNR GOEVAL,INPUT+20
25645 TFM LNTH,5
25655 A56 TF A58+11,ADDCOM
25665 AM ADDCOM,5,10
25675 TF A59+11,ADDCOM
25685 A ADDCOM,TRDSA+6
25695 SM ADDCOM,1,10
25705 AER8 BNF A59,GOOD8+11
25715 A58 TFM ADDR5
25725 B D13
25735 AM ADDCOM,18,10
25745 DORG *-3
25755 A59 TFM ADDR5
25765 D13 BNR LDLBL,EJS
25775 BNF D14,GOOD8+11
25785 B MAC1
25795 DORG *-3
25805 D14 TF CSASND,ADDR5

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13586 49 13442 00000
13594
13594 21 15280 00704
13606 49 13442 00000
13614
13614 16 13896 000K6
13626 33 13455 00000
13638 45 13830 00587
13650 17 03M82 13662
13662 11 13896 000-5
13674 14 13896 000M1
13686 47 13490 01300
13698 16 05105 00000
13709 1
13710 27 05310 05309
13722 46 05142 00200
13734 16 13895 000M1
13746 45 13938 00587
13758 27 08654 08653
13770 17 08524 J3902
13782 14 00817 000K3
13794 47 13818 01200
13806 11 13896 000-5
13818 31 00816 00818
13830 45 13782 00817
13842 11 13896 000-5
13854 14 13896 000M1
13866 46 13698 01300
13878 49 13938 00000
13890 31 00500 01118
13902 32 13655 00C00
13914 45 13650 00817
13926 16 00704 -0005
13938 26 14021 00725
13950 11 00725 000-5
13962 26 14053 00725
13974 21 00725 13896
13986 12 00725 000-1
13998 44 14042 03353
14010 16 01122 -0000
14022 11 00725 00018
14034 49 14054 00000
14042
14042 16 01122 -0000
14054 45 14194 00587
14066 44 14086 03353
14078 49 09750 00000
14086 26 15299 01122

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25815	SM	DSASND,4	14098	12	15299	-0004
25825	TF	DSASND-5,DSASND	14110	26	15294	15299
25835	SM	DSASND-5,5	14122	12	15294	-0005
25845	BTM	LIMPRT,TYPDSA	14134	17	06342	-7360
25855	*					
25865	*	TRANSFER INSTRUCTION ROUTINE				
25875	*					
25885	TRA	BI JUST-JUST-1	14146	27	08944	08943
25895	AM	ADGLOW,23	14158	11	00725	-0023
25905	TR	ZEPD,TRAC-24	14170	31	00500	01270
25915	BC	LIMPRT,EJS	14182	43	06342	00587
25925	*					
25935	*	ROUTINE TO LOAD LABELS INTO SYMBOL TABLE				
25945	*					
25955	LDLRL	C CLERER+11,INPUT+10	14194	24	00743	00807
25965	RME	F9	14206	47	14226	01200
25975	LABCTR	DS 2,*	14217		2	
25985	B	A37	14218	49	02546	00000
25995	DORG	*-3	14226	15	14353	00001
26005	F9	TCM TSPEC+11,1	14226	15	14353	00001
26015	TF	LAB,INPUT+10	14238	26	01261	00807
26025	TFM	LABCTR,6,10	14250	16	14217	000-6
26035	A61	BD A60,LAB	14262	43	14318	01261
26045	BD	A60,LAB-1	14274	43	14318	01260
26055	SM	LABCTR,1,10	14286	12	14217	000-1
26065	TF	LAB,LAB-2	14298	28	01261	01259
26075	B	A61	14310	49	14262	00000
26085	DORG	*-3	14318	26	01585	01261
26095	A60	TF INPUT3,LAB	14318	26	01585	01261
26105	SP	INPUT3	14330	32	01585	00000
26115	HED	DS 3,*	14341		3	
26125	TSPEC	SF LAB-11	14342	32	01250	00000
26135	CM	LAB-10,3,10	14354	14	01251	000-3
26145	BL	A62	14366	46	14450	01200
26155	CM	LAB-10,21,10	14378	14	01251	000K1
26165	BE	A62	14390	46	14450	01200
26175	CM	LAB-10,33,10	14402	14	01251	000L3
26185	BL	ER14	14414	47	14698	01300
26195	CM	LAB-10,69,10	14426	14	01251	00009
26205	BH	LBLCK	14438	46	14462	01100
26215	A62	TCM TSPEC+11,0	14450	15	14353	00000
26225	LBLOK	TR LAB-11,LAB-9	14462	31	01250	01252
26235	BNR	TSPEC,LAB-11	14474	45	14342	01250
26245	BC	ER14,TSPEC+11	14486	43	14698	14353
26255	CM	LABCTR,6,10	14498	14	14217	000-6
26265	BE	BIT	14510	46	14642	01200
26275	CF	INPUT3	14522	33	01585	00000
26285	AM	LABCTR,1,10	14534	11	14217	000-1
26295	TFM	D17+11,INPUT3	14546	16	14581	-1585
26305	D18	SM D17+11,1,10	14558	12	14581	000-1
26315	D17	BNF D18	14570	44	14558	00000
26325	D19	TF D19+6,D17+11	14582	26	14600	14581
26335	CF		14594	33	00000	00000
26345	TF	D20+6,D19+6	14606	26	14636	14600
26355	SM	D20+6,1,10	14618	12	14636	000-1
26365	D20	TF ,HED	14630	26	00000	14341

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26375	RIT	TFM D33+6,G11	14642	16	04952	J6822
26385	HT	11,11-1	14654	27	04922	04921
26395	*	BC MULTIPLY DEFINED LABEL PASS1 OR INCURRECT ADDRESS PASS11				
26405	BC	D30,EJS	14666	43	14738	00587
26415	EN10	TFM EVALER-1,17000	14678	16	05105	J7C00
26425	*	DC 1,*,*	14689		1	
26435	B	A64	14690	49	05722	00000
26445	QORG	*-3	14698			
26455	NOISE	DS 1,*,*	14697		1	
26465	ERI4	TFM EVALER-1,17400	14698	16	05105	J7400
26475	*	DC 1,*,*	14709		1	
26485	B	A64	14710	49	05722	00000
26495	DORG	*-3	14718			
26505	ER9	TFM EVALER-1,90000	14718	16	05105	R0000
26515	*	DC 1,*,*	14729		1	
26525	B	A64	14730	49	05722	00000
26535	QORG	*-3	14738			
26545	D30	TF D32+11,D26+11	14738	26	14773	05C49
26555	AM	D32+11,5,7	14750	11	14773	-0005
26565	D32	C ADDMS	14762	24	01122	00000
26575	BC2	D34	14774	46	14966	00200
26585	BE	G11	14786	46	14822	01200
26595	BT	RCY1,RCY1-1	14798	27	08654	08653
26605	BTM	TABRY1,ER10,7	14810	17	08524	J4678
26615	G11	C A63+11,FINAL	14822	24	04945	15431
26625	*	LABEL TABLE IS FULL				
26635	B+	ER9	14834	46	14718	01100
26645	TF	D21+6,A63+11	14846	26	14864	04945
26655	TD	,LABCTR	14858	25	00000	14217
26665	A	LABCTR,LABCTR	14870	21	14217	14217
26675	TF	D22+6,D21+6	14882	26	14912	14864
26685	A	D22+6,LABCTR	14894	21	14912	14217
26695	D22	TF INPUT3	14906	26	00000	01585
26705	AM	D22+6,5,10	14918	11	14912	000-5
26715	TF	D23+6,D22+6	14930	26	14960	14912
26725	SF	ADDMS-4	14942	32	01118	00000
26735	D23	TF ,ADDRS	14954	26	00000	01122
26745	D34	TF ERLAB+10,INPUT+10	14966	26	01165	00807
26755	TFM	INRKM	14978	16	15082	-0000
26765	H	A37	14990	49	02546	00000
26775	DORG	*-3	14998			
26785	TBLCRD	RN 100,500	14998	36	00100	00500
26795	RN	172,500	15010	36	00172	00500
26805	RN	244,500	15022	36	00244	00500
26815	RN	316,500	15034	36	00316	00500
26825	RN	,500	15046	36	00000	00500
26835	DM8	15	15072		15	
26845	DC	1,0	15073		1	
26855	DC	4,*,	15077		4	
26865	INRPM	-00,*,	15082		5	
26875	DC	1,*,	15083		1	

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27215	TABCON	DC	4,1007	15329	4	
27225		J007		15333	4	
27235		DC	4,1128	15337	4	
27245		DC	4,2447	15341	4	
27255		K447		15345	4	
27265		DC	4,-3166	15351	6	
27275		L160		15353	2	00500
27285		DC	4,388*	15354	36	00000
27295		L88*		15366	49	00000
27305		DS	6	15373	1	
27315		DNB	2	15408	35	
27325		DNB	35	15410	2	
27335		DC	2,8	15415	5	
27345		DC	5,96	15420	5	
27355		-0096		15421	1	
27365		DC	5,115	15422	1	
27375		-G115		15426	4	
27385		DNB	1	15431	5	
27395		DC	1,0			
27405		-				
27415		DC	4,*			
27425		-00*				
27435		DC	5			
27445		DC	11,-41000000215,,	15442	11	
27455		M100000021N		15453	11	
27465		DC	11,-41540000115,,	15464	11	
27475		M154000011N		15475	11	
27485		DC	11,-46414444015,,	15486	11	
27495		M641444401N		15497	11	
27505		DC	11,-62000000225,,	15508	11	
27515		U200000022N		15519	11	
27525		DC	11,-62540000125,,	15530	11	
27535		DC	11,-66626442025,,	15541	11	
27545		M662644202N		15552	11	
		DC	11,-54000000235,,	15563	11	
		N400000023N				
		DC	11,-54540000135,,			
		N454000013N				
		DC	11,-46546453035,,			
		M654645303N				
		DC	11,-53440000285,,			
		N344000028N				
		DC	11,-53445400185,,			
		N344540018N				
		DC	11,-44000000295,,			
		N400000029N				

OPERATION CODE TABLE

ADD
ADD IMMEDIATE
FLOATING ADD
SUBTRACT
SUBTRACT IMMEDIATE
FLOATING SUBTRACT
MULTIPLY
MULTIPLY IMMEDIATE
FLOATING MULTIPLY
LOAD DIVIDEND
LOAD DIVIDEND IMMEDIATE
DIVIDE

27555	DC 11,-4454000195,,	DIVIDE IMMEDIATE	15574	11
27565	M45400019M	FLOATING DIVIDE	15585	11
27575	M644496509N	COMPARE	15596	11
27585	M30000024N	COMPARE IMMEDIATE	15607	11
27595	M35400014N	TRANSMIT DIGIT	15619	11
27605	DC 11,-63440000255,,	TRANSMIT DIGIT IMMEDIATE	15629	11
27615	DC 11,-63445400155,,	TRANSMIT FIELD	15640	11
27625	DC 11,-63460000265,,	TRANSMIT FIELD IMMEDIATE	15651	11
27635	DC 11,-6346540016N	TRANSMIT FLOATING FIELD	15662	11
27645	DC 11,-63465300065,,	TRANSMIT RECORD	15673	11
27655	DC 11,-63590000315,,	FLOATING SHIFT LEFT	15684	11
27665	M662530005N	FLOATING SHIFT RIGHT	15695	11
27675	M62590008N	TRANSMIT NUMERIC STRIP	15706	11
27685	DC 11,-63556200725,,	TRANSMIT NUMERIC FILL	15717	11
27695	DC 11,-63554600735,,	BRANCH	15728	11
27705	M200000049N	BRANCH NO FLAG	15739	11
27715	DC 11,-42554600445,,	BRANCH NO RECORD MARK	15750	11
27725	M25590045N	BRANCH DIGIT	15761	11
27735	M244000043N	BRANCH AND TRANSMIT	15772	11
27745	DC 11,-42630000275,,	BRANCH AND TRANSMIT IMMEDIATE	15783	11
27755	DC 11,-42635400175,,	BRANCH AND TRANSMIT FLOATING FIELD	15794	11
27765	M263465307N	BRANCH BACK	15805	11
27775	DC 11,-42420000425,,	BRANCH INDICATOR	15816	11
27785	M249000046N	BRANCH NO INDICATOR	15827	11
27795	DC 11,-42554900475,,	CONTROL	15838	11
27805	M200000034N	SET FLAG	15849	11
27815	DC 11,-62460000325,,	CLEAR FLAG	15860	11
27825	M346000033N	MOVE FLAG	15871	11
	DC 11,-54460000715,,			
	N446000071N			

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27835	DC 11,-48000000485,,	HALT	15882	11
27845	M80000048N	NO OPERATION	15893	11
27855	DC 11,-55565700415,,	BRANCH HIGH	15904	11
27865	M556570041N	BRANCH POSITIVE	15915	11
27875	DC 11,-42480000114,,	BRANCH EQUAL	15926	11
27885	M248000011M	BRANCH ZERO	15937	11
27895	DC 11,-42570000114,,	BRANCH OVERFLOW	15948	11
27905	M257000011M	BRANCH EXPONENTIAL OVERFLOW	15959	11
27915	DC 11,-42450000124,,	BRANCH ANY	15970	11
27925	M245000012M	BRANCH NOT LOW	15981	11
27935	DC 11,-42690000124,,	BRANCH NOT NEGATIVE	15992	11
27945	M269000012M	BRANCH CONSOLE SWITCH 1 ON	16003	11
27955	DC 11,-42650000144,,	BRANCH CONSOLE SWITCH 2 ON	16014	11
27965	M265000014M	BRANCH CONSOLE SWITCH 3 ON	16025	11
27975	DC 11,-42676500154,,	BRANCH CONSOLE SWITCH 4 ON	16036	11
27985	M243710001M	FLOATING SHIFT RIGHT SUBROUTINE	16047	11
27995	DC 11,-42437100014,,	BRANCH NOT HIGH	16058	11
28005	M243720002M	BRANCH NOT POSITIVE	16069	11
28015	DC 11,-42437300034,,	BRANCH NOT EQUAL	16080	11
28025	M243730003M	BRANCH NOT ZERO	16091	11
28035	DC 11,-42437400044,,	BRANCH NO OVERFLOW	16102	11
28045	M243740004M	BRANCH NO EXPONENTIAL OVERFLOW	16113	11
28055	DC 11,-46625962147,,	BRANCH NOT ANY	16124	11
28065	M662596214P	BRANCH LOW	16135	11
28075	DC 11,-42554800113,,	BRANCH NEGATIVE	16146	11
28085	M255480011L	BRANCH CONSOLE SWITCH 1 OFF	16157	11
28095	DC 11,-4255471013,,	BRANCH CONSOLE SWITCH 2 OFF	16168	11
28105	M25547101L	BRANCH CONSOLE SWITCH 3 OFF	16179	11
	DC 11,-4255437202L			
	M255437202L			
	DC 11,-42554373033,,			
	M255437303L			

20115	DC 11,-42554374043,,	BRANCH CONSOLE SWITCH 4 OFF	16190	11
20125	M255437404L	READ NUMERIC TYPEWRITER	16201	11
20135	M955636861K	WRITE NUMERIC TYPEWRITER	16212	11
20145	DC 11,-66556368812,,	DUMP NUMERIC TYPEWRITER	16223	11
20155	M455636851K	READ ALPHA TYPEWRITER	16234	11
20165	DC 11,-59416368712,,	WRITE ALPHA TYPEWRITER	16245	11
20175	M41636871K	TABULATE TYPEWRITER	16256	11
20185	DC 11,-63426368811,,	RETURN CARRIAGE TYPEWRITER	16267	11
20195	DC 11,-59436368211,,	SPACE TYPEWRITER	16278	11
20205	M943636821J	FLOATING ADD SUBROUTINE	16289	11
20215	DC 11,-62576368111,,	FLOATING SUBTRACT SUBROUTINE	16300	11
20225	M64100003P	FLOATING MULTIPLY SUBROUTINE	16311	11
20235	DC 11,-66540000047,,	FLOATING DIVIDE SUBROUTINE	16322	11
20245	M65400004P	FIXED DIVIDE SUBROUTINE	16333	11
20255	DC 11,-44496500017,,	FLOATING SQUARE ROOT SUBROUTINE	16344	11
20265	M449650001P	FLOATING COSINE SUBROUTINE	16355	11
20275	DC 11,-46625859067,,	FLOATING SINE SUBROUTINE	16366	11
20285	M662585906P	FLOATING ARCTANGENT SUBROUTINE	16377	11
20295	DC 11,-46416355097,,	FLOATING EXPONENTIAL BASE 10 SUBROUTINE	16388	11
20305	M641635509P	FLOATING NATURAL EXPONENTIAL SUBROUTINE	16399	11
20315	DC 11,-46456763107,,	FLOATING LOG BASE 10 SUBROUTINE	16410	11
20325	M645670011P	FLOATING NATURAL LOG SUBROUTINE	16421	11
20335	DC 11,-46535647127,,	FLOATING SHIFT LEFT SUBROUTINE	16432	11
20345	M653564712P	TRANSMIT FLOATING FIELD SUBROUTINE	16443	11
20355	DC 11,-46625362157,,	BRANCH AND TRANSMIT FLOATING FIELD S	16454	11
20365	DC 11,-42634662177,,	DEFINE SYMBOL	16465	11
20375	M263466217P	DEFINE SPECIAL SYMBOL	16476	11
20385	DC 11,-44620000010,,	DEFINE ALPHA SYMBOL	16487	11
	M462000010			
	DC 11,-44626200110,,			
	M4626200110			
	DC 11,-44416200001,,			
	M4416200001			

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28395	DC 11,4443000C002,,	DEFINE CONSTANT	16498	11
	M443000002			
28405	DC 11,44624300102,,	DEFINE SPECIAL CONSTANT	16509	11
	M4624300102			
28415	DC 11,44414300'03,,	DEFINE ALPHA CONSTANT	16520	11
	M4414300103			
28425 XDSA	DC 11,44624100004,,	DEFINE SYMBOLIC ADDRESS	16531	11
	M4624100004			
28435 XDSB	DC 11,44624200005,,	DEFINE SYMBOLIC BLOCK	16542	11
	M4624200005			
28445 XDNR	DC 11,445542000G,,	DEFINE NUMERIC BLANK	16553	11
	M4554200000	WRITE ALPHA CARD	16564	11
28455	DC 11,-66414344942,,	READ ALPHA CARD	16575	11
	O641434494K			
28465	DC 11,-59414344752,,	DUMP NUMERIC CARD	16586	11
	N941434475K			
28475	DC 11,-44554344542,,	WRITE NUMERIC CARD	16597	11
	M455434454K			
28485	DC 11,-66554344842,,	READ NUMERIC CARD	16608	11
	O655434484K			
28495	DC 11,-59554344652,,	BRANCH LAST CARD	16619	11
	N955434465K			
28505	DC 11,-42534300094,,	BRANCH NOT LAST CARD	16630	11
	M253430009H			
28515	DC 11,-42555343093,,	DEFINE ORIGIN	16641	11
	M25534309L			
28525	DC 11,44565947C06,,	HEAD	16652	11
	M4565947006			
28535	DC 11,48454144008,,	MORG	16663	11
	M8454144008			
28545	DC 11,54565947009,,	TRANSFER TO PROCESS	16674	11
	M4565947009			
28555	DC 11,63434400016,,	TRANSFER TO LOAD	16685	11
	O3434400016			
28565	DC 11,-63594100106,,	INPUT CONVERSION	16696	11
	O3594100100			
28575	DC 11,-49554342187,,	OUTPUT CONVERSION	16707	11
	M955434218P			
28585	DC 11,-50646343007,,	*****DUMMY OP CODE*****	16718	11
	M064634300P			
28595	DC 11,60606060606,,	*****DUMMY OP CODE*****	16729	11
	O0606060606			
28605	DC 11,60606060606,,	*****DUMMY OP CODE*****	16740	11
	O0606060606			
28615	DC 11,60606060606,,	*****DUMMY OP CODE*****	16751	11
	O0606060606			
28625	DC 11,60606060606,,	*****DUMMY OP CODE*****	16762	11
	O0606060606			
28635	DC 11,60606060606,,	*****DUMMY OP CODE*****	16773	11
	O0606060606			
28645	DC 11,60606060606,,	*****DUMMY OP CODE*****	16784	11
	O0606060606			
28655	DC 11,60606060606,,	*****DUMMY OP CODE*****	16795	11
	O0606060606			
28665	DC 11,60606060606,,	*****DUMMY OP CODE*****		
	O0606060606			

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*****DUMMY OP CODE*****

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28675      DC 11,60606060606,,          *****DUMMY OP CODE*****
          00606060606
28685 XEND  DC 11,4455544007,,          DEFINE END
          M4+55544007
28695 SYMTBL DS 1
28705      DORG SYMTBL
28715 *      ROUTINE TO FIND SIZE OF MEMORY
28725 START  TR 19999,REC1,2
28735 G8     BNR G9,0
28745      B G10
28755      DORG *-3
28765 G9     AM G8+3,20,10
28775      B G8
28785      DORG *-3
28795      TF FINAL,G8+6
28805 G10    SM FINAL,20
28815      CF LODER1+76
28825      CF LODER2+76
28835      TR 00000,STRT2
28845 *      ROUTINE TO CLEAR INPUT AREA
28855      TF INPUT-2,CLERER+9
28865      TF INPUT+10,CLERER+11
28875      TF INPUT+18,CLERER+7
28885      TFM AA3+6,INPUT+20
28895 AA3    AM AA3+6,2
28905      CM AA3+6,INPUT+140
28915      BL AA3
28925      DSC 2,*,*-1
28935 REC1   O*
28945 STRT2  B INITI
28955      DC 1,*,*-4
28965      *
28975      DEND START

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16806      11
16817      11
16818      1
16818
16818 15 0000 00000
16830 31 J9999 17036
16842 45 16862 00000
16854 49 16882 00000
16862 11 16833 00000
16874 49 16830 00000
16882 26 15431 16836
16894 12 15431 -0020
16906 33 01372 00000
16918 33 01452 00000
16930 31 00000 17038
16942 26 00795 00741
16954 26 00807 00743
16966 26 00815 00739
16978 16 16996 -0817
16990 16 00000 000-0
17002 11 16996 -0002
17014 14 16996 -0937
17026 47 16990 01300
17036      2
17038 49 01798 00000
17045      1
16818

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ADDCOM	00725	A21	07250	ALFOP	03070	865	09730	CSTAT	11726
BCKSPC	03874	A22	07384	ALPHA	00411	866	09882	D11	13594
BRLOAD	15354	A23	07808	AORS	04010	867	09870	D12	13818
BRDRBR	06134	A24	07852	A	15442	868	09930	D13	14054
CASIER	02694	A25	08372	ASINE	10976	86	02130	D14	14086
CCOMFR	12946	A26	08016	ASTER	04686	871	10228	D17	14570
CHVALD	10272	A27	08856	B10	03094	872	10248	D18	14558
CLERER	00732	A28	08924	B12	03658	873	10304	D19	14594
CMPCON	05754	A29	09682	B13	03802	874	10324	D1	12754
CMPIINS	06242	A2	02010	B14	03962	875	10348	D20	14630
CMPOUT	01494	A32	10456	B15	04022	876	10384	D21	14858
COMMER	03886	A33	10812	B16	04118	877	10444	D22	14906
COMSPC	03906	A34	12838	B17	04182	878	10492	D23	14954
COMSND	15280	A35	10880	B18	04218	879	10540	D24	04966
DOINST	07956	A36	11096	B19	04374	880	10528	D25	04990
DOLLAR	04150	A37	02546	B1	01918	883	10832	D26	05038
DSASND	15299	A38	11714	B20	04410	884	11084	D27	05062
ELNGTH	01284	A3	01986	B21	04562	885	11364	D28	05014
ENTABL	01592	A41	12138	B22	04648	887	11642	D29	05050
EPRINT	05310	A42	12402	B23	05266	888	11630	D2	12742
LRCHAR	04274	A43	11798	B24	05246	889	11592	D30	14738
EVALAD	03482	A44	11822	B25	05334	889	11666	D32	14762
EVALER	05106	A45	12578	B26	05382	88	02954	D33	04966
FLAGGR	09262	A46	12646	B27	05438	890	12234	D34	14966
GOEVAL	13650	A47	12506	B28	05462	891	12258	D3	12922
HEADER	05470	A48	11762	B29	05958	892	12306	D4	13034
INPUT2	00959	A49	02966	B2	01906	893	11914	D5	13194
INPUT3	01585	A4	02474	B30	05978	894	11926	D6	13242
INSTRN	09030	A50	13114	B31	06098	895	12034	D7	13278
LABCTR	14217	A51	13054	B32	06186	896	12094	D8	13314
LINPRY	06342	A52	13206	B33	06166	899	12614	D9	13338
LUDER1	01296	A53	13442	B38	04902	89	02186	DAC3	10680
LUDER2	01376	A54	13830	B39	06634	BAKR	09550	DAC	10124
LDPDUT	01245	A55	13782	B3	02066	BBACK	04142	DAS	09974
MACROS	12434	A56	13938	B40	06714	BB	06334	DC	12710
NOPREC	00720	A57	13902	B41	06846	BETA	12413	DENC	11444
NOFINE	10600	A58	14010	B42	06906	B1	08776	DIN	12470
NOTYPE	08172	A59	14062	B45	07408	B1T	14642	DJD	12554
PCHALF	07190	A5	06274	B46	07476	BLKVR	06870	D0B1	08824
PCHCRD	06262	A60	14318	B47	07456	BLNKS	15268	D0B4J	08844
PICKUP	02984	A61	14262	B48	08252	BLSND	01457	DUDSB	06642
PNCM11	11516	A62	14450	B49	08912	BNI	08788	D0DS	06678
PRDCSA	13490	A63	04934	B4	02566	B1	10090	DOK	08994
PUNCHY	06014	A64	05722	B50	08956	BR2	10098	DOL	03823
RETURN	04058	A6	03166	B51	08968	BRNCH	06494	DOROW	08900
A10	05494	A70	13162	B52	09086	BRSO	15351	DORG	11304
A11	03862	A7	05142	B53	09178	BTBL	03424	DSA	13614
A12	03626	A8	05518	B54	09250	CHAR	09530	DSB	10764
A13	03754	A9	05506	B55	09362	CHECK	13502	OSC	13430
A14	03850	A11	02034	B56	09294	CHKND	05222	DSDNB	11024
A15	04514	A12	02376	B57	09406	CKREC	10066	DSS	11152
A16	06142	A13	16990	B58	09426	CNTR	02521	DJS	00587
A17	06002	ABLE	09618	B59	09494	COLL	00618	EMPTY	05814
A18	05838	ADRS	01122	B60	09386	COMA	05550	ER10	14678
A19	05766	AERB	13998	B61	09594	COMP	03106	ER11	04094
A1	11164	AJUST	00599	B62	09630	CONCD	05910	ER12	05678

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ER13	05710	GET1	03974	MORG	11212	RECMK	01296	TSPEC	14342
ER14	14698	GET	04294	MULT	04600	RLOP	02222	TYPE	02423
ER1	02234	GOAMD	13350	MASS	11188	RMFL	02302	WRMS	12678
ER3	03154	GOOD1	03366	MAST	02774	RMRK	01126	XDAS	16487
ER5	03778	GOOD2	03378	NOISE	00648	RSCAN	01974	XDEND	16817
ER9	14718	GOOD8	03342	NUMB	00648	S1	03670	XDNB	16553
LRCON	12426	GOTU	13132	OK	03318	SEEM	09282	XDSA	16531
ERDSA	13698	H1	02978	ONEZ	00699	SEN	10868	XDSR	16542
ERLAB	01155	MED	14341	OP	03002	SET	13312	XDS	16445
EV1	05174	INIT2	01810	ORDER	02865	SFLAG	13134	XOSS	16416
F1	10672	INIT1	01798	OUT	00418	SIRTY	13137	ZEPU	00500
F2	10704	INCRM	15082	OVER	11536	SNDOP	08880	SEFIN	08416
F3	10660	INPUT	00797	PASS1	02426	SNT	11882	SEVEN5	11905
F9	14226	INSND	15318	PCOM1	07616	SPEC	08592	SHEILA	11272
FINAL	15431	INST	08764	PCOM2	07796	STAR	02522	STCMAR	10316
G10	16882	ISTAT	00689	PCOM3	07796	START	16818	SUBENT	08542
G11	14822	IT	04922	PCON	07520	STR12	17038	SYMBL	16818
G13	02450	JSTNL	00659	PDSA	07840	SW2	04810	TABBY1	08524
G14	10058	JUST	08944	PLACE	06365	SYM1	11962	TBLCON	15329
G15	02316	K	08812	PLDR	02586	SYM2	11986	TBLEND	04353
G16	02878	LABL	03825	PNGH1	02438	TABBY	08548	TESTAD	13217
G17	02898	LABOK	04878	PROAS	08752	IDM	15629	THINGS	00641
G18	02910	LAB	01261	PROSA	11012	TEMP	00730	TISTAT	15113
G19	02834	LBAD0	04830	PRDS	11176	TEST	00406	TRNUMB	04526
G1	11328	LBLOK	14462	PRSM	08664	TFADD	04766	TYPADD	08611
G20	02090	LOHED	14498	PRSYM	11786	TORR	04130	TYPDS	07360
G22	06574	LDLBL	14194	PRTI	06438	TRAC	01294	WRPRNU	05402
G23	02258	LINE	06502	PRT2	06458	TRANS	09374	ZERONE	09650
G24	03258	LNK	01128	PTBL	12210	TRA	14146		
G25	08572	LNTH	00704	RC2	08702	TRDSA	13890		
G26	02990	L	11559	RCMT	08709	TRREC	13090		
G30	11894	LYNN	11248	RCTY1	08654	TR	05862		
G4	04286	MAC1	09750	RCTV	08618				
G5	08580	MACRU	09670	RDM	08000				
G8	16830	MESS1	01171	READ	02634				
G9	16862	MESS2	01201	RECI	17036				

END OF ONE ASSEMBLY.