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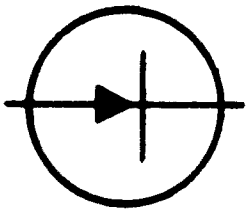

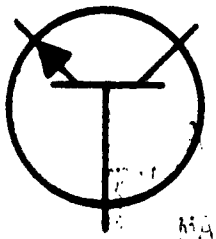

WESTINGHOUSE ELECTRIC CORPORATION
1625 K Street
Washington, D. C.

Second Quarterly Report
covering period 1 October to 31 December, 1962

HIGH CURRENT AND HIGH VOLTAGE SILICON CONTROLLED RECTIFIERS

NObsr-87647 Proj. No. SR-0080301 Task No. 9348

NAVY DEPARTMENT
BUREAU OF SHIPS
ELECTRONICS DIVISION

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ABSTRACT

Silicon material was received, evaluated and processed through the initial phases of device fabrication. Material evaluation indicates that the silicon approximates the required specifications.

Sample fabrication was initiated about one of the device structures prescribed in the preceding report. Diffusion results and evaluations are given.

A modified capsule design for anticipated improved thermal characteristic is discussed. Design features of both approaches are given.

Test fixtures are discussed in view of the extended current rating (500A) compared to conventional devices.

SECTION I

A. PURPOSE

The research and development effort to be conducted under this contract is directed toward the development of a 500 ampere, 500 volt silicon controlled rectifier. Specifications for the device are given in Table I.

TABLE I

Characteristic	Symbol	Condition	Value
Average Forward Current (Min.)	$I_{FB(Av)}$	180 electrical degrees of half sine wave conduction at T_C=80°C.	500A
Peak Surge Current (Min.)	$I_{FM(Surge)}$	A non-recurrent surge 180 electrical degrees of one-half sine wave conduction immediately preceded and followed by $I_{FB(Av)}$ = 500A at T_C=80°C.	10,000A
Peak Forward and Peak Reverse Blocking Voltage (Min.)	PFV - PRV	Over the workable temperature range of the device.	500V
Turn-Off Time (Max.)	t_{off}	Initially 500A into a resistive load with mounting interface surface at 80°C steady state.	30 usec
Turn-On Time (Max.)	t_d & t_r	Turn-on with a square wave current pulse. $I_{FB(Av)}$ may be limited to 50A through a non-inductive load.	10 usec
Rate of Rise of Anode-To-Cathode Voltage (Min.)	dv/dt	Test circuit similar to MIL-S-19500/204, Fig. 11 shall be used.	50V/ usec

Device encapsulation shall be such that it withstands, by itself, normal shipboard environmental conditions. The package shall be designed to remove heat by conduction through a mounting interface surface to a mating surface. The 80°C mounting surface temperature contemplates water cooling of the heat sink to which the device is attached. The device shall not be designed to contain or directly contact liquid or vapor cooling mediums.

In order to attain the contract objectives, a program has been designed about the following phases:

1. Silicon Material - - - - - - - availability and procurement
2. Basic Device Structure - - - - design and optimization
3. Encapsulation - - - - - - - - design and refinement
4. Sample Fabrication - - - - - - experimental & final (in-spec)
5. Device Evaluation - - - - - - equipment design & electrical test
6. Delivery - - - - - - - - - - - devices and reports

B. GENERAL FACTUAL DATA

During this report period, the following personnel contributed to the project effort for the number of man-hours indicated:

L. Garrison - - - - - 24 hours
A. Knopp - - - - - - - 440 hours
R. Kuehn - - - - - - - 401 hours
C. Skooglund - - - - - 15 hours

C. MATERIALS (Silicon)

Crucible grown material has been received from one supplier. Table II is a list of the range of the specifications on the ingots received. Refer to Table II of the preceding report on this contract for a comparison between the proposed and the obtained parameters.

TABLE II

Silicon Evaluation Data

Diameter	1.125 inch
Resistivity	18-31 ohm-cm
Resistivity Gradient (across slice)	1 - 15%
Lifetime	100 - 400 micro sec.
Dislocation Density	0 - 10,000/cm^2
Lineage	None

To date, three crystals have been processed. The characteristics of these crystals as evaluated prior to device fabrication were similar except for the orientation. Crystal 3013 (of Table IV) was 1.5° from (111) plane while 3011 was 1.0° from (111) plane. The majority of the fusion starts processed from crystals Nos. 3013 and 3011 were either short or very low voltage in the forward (V_{BO}) direction. The reverse characteristics exhibited some degree of blocking voltage. On the otherhand, 80% of the units processed from crystal 2995 exhibited reasonably high forward and reverse blocking voltages. The orientation of this crystal was 0.5° from (111) plane. Thus, as anticipated, large area devices are extremely critical of orientation if desired diffusion and alloying results are to be attained. Evaluation of control samples for all three ingots (cf. Table V) indicates good forward and reverse blocking voltages. However, the area of the Au-Sb dots on the control samples is one-tenth of the area used on the actual units. Thus, the specification on the orientation of the crystals has been reduced from 2° to 0.5° from the (111) plane.

As noted previously, evaluation of silicon material sources will be on a continuing basis to insure that the best material available is used for the subject contract.

D. BASIC DEVICE STRUCTURE

The basic device structure utilized in work during the second report period was outlined in the previous contract report as Type 2. Preliminary design studies are considered complete as of this report. Optimization was begun in terms of initiating sample fabrication. Information is not yet available for reporting on this second sub-phase of the "Basic Device Structure" since test of fabricated devices has not been completed. However, preliminary evaluations are given in Section I-F, "Sample Fabrication."

E. ENCAPSULATION

The stud mounted capsule development was continued along the lines described in the first report. As presently envisioned, the cathode terminal will be a cylindrical copper rod to which a standard type cable clamp can be attached. Both the gate and cathode potential terminals will be of the quick connect variety now widely used for low power connections. If for some reason this type of termination is proven not to be satisfactory, modification can readily be made to permit other conventional types of terminations, e.g. welded leads.

An alternate ceramic-metal seal design is also under investigation. The modified seal employs a solid ceramic top with the necessary feedthrough in place of the metal cap on the present design. Such a seal is desirable since it has a minimum number of joints. Moreover, the modification provides a top insulating surface as well as the side insulating surface which, in practice, is less susceptible to contamination from the operating ambients in terms of creepage path. There are a number of details yet to be resolved before a change to this design could be anticipated.

Two major difficulties have already been encountered which have retarded progress on the capsule development phase of the contract. Procurement of satisfactory seals is behind schedule due to unexpected fabrication problems by the suppliers. A few usable seals are available, although their quality is not up to normal Westinghouse standards. Delivery of improved quality seals in larger quantities is expected within the next report period.

Modifying the only available dry-box welding chamber facility to accommodate this device created a difficult design problem since the required size of the capsule approaches the maximum size capability of the equipment. Several alterations of the weld-chamber and adjustments to the welder will permit the necessary assembly and weld operations to be performed. As soon as a sufficient quantity of all parts are available, sample assemblies will be made to evaluate both the capsule design and the fabrication system.

One parameter specified for this device which may become a serious problem in the future is the thermal drop from junction to case. Although extrapolation of capsule size to current ratings for smaller power devices indicates that the present design should be capable of meeting the specified power rating, many factors which are difficult to control and are inherent in fabricating large area devices, may adversely affect the characteristics of the device. For that reason, it has been decided that an alternate design approach - a flat base, clamp mounted capsule - would be undertaken simultaneously with the stud mounted design. One reason for initiating this action is the elimination of the stud to permit the central base area immediately beneath the junction to be utilized as an efficient heat conducting channel to the heat sink. The thermal resistance of the base is decreased in two ways. The effective area of the base is increased, and the effective distance from junction to sink is decreased. A second reason for pursuing the alternate approach is that the low yield strength copper stud can be replaced by several high

strength steel bolts which will provide the increased contact pressure required for a low case-to-sink thermal resistance. Since steel bolts can be used which will not fail through creep at high temperatures, as does copper, this problem can thereby be eliminated.

A general description of the capsule considered as the alternate for the studs mounted design is as follows:

1. The base of the unit is approximately 2.2 inches in diameter.

2. The bottom of the base is flat to provide intimate contact to the heat sink in the central portion of the base.

3. The seal and terminals are essentially the same as described for the stud mounted device.

4. A clamp, rectangular in shape with bolts in each corner, provides the necessary means of mounting the unit to the heat sink.

As was mentioned in an earlier paragraph, devices made with capsules of both designs will be fabricated and tested. Physical and environmental tests will be made in addition to the required electrical tests. The thermal impedance of the device may be a limiting factor; therefore, it will be thoroughly checked for both designs. Since the thermal resistance, case-to-sink, is affected by the contact pressure between the two interfaces, the effect of stud creep will be checked on the stud mounted devices.

Both devices will eventually be tested under shock, vibration, salt spray, high and low temperature storage and thermal cycling conditions. Other tests may also be made to further determine the mechanical capabilities of the designs.

After completion of the testing program, the design which proves to be the most satisfactory will be proposed as the final capsule design.

F. SAMPLE FABRICATION

For convenience of reference in future reports, this phase will be divided into the following subsections:

(1.) Silicon Preparation
(2.) Diffusion
(3.) Alloying
(4.) Surface Treatment
(5.) Encapsulation

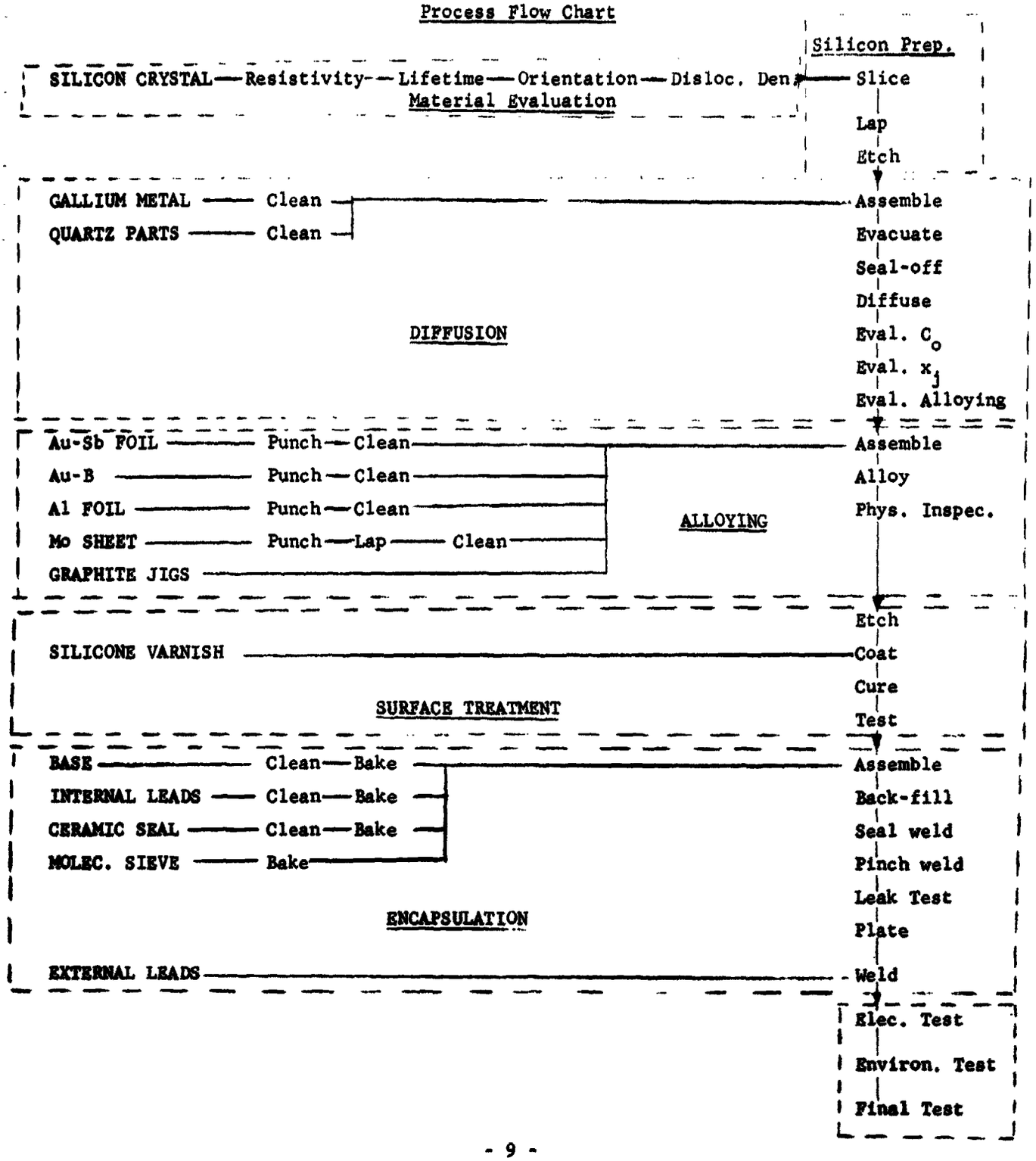
A process flow chart in block diagram form, Figure 1, outlines in more detail the operations included under the five sections given above. Note that Section I-C covers the area of crystal parameter evaluation, and Section I-G covers the area of final test and evaluation.

1. Silicon Preparation

Following acceptance of silicon material for device fabrication as a result of crystal parameter evaluation, the ingots are passed through the operations of slicing, lapping and etching. The first operation reduces the cylindrical ingot to wafers. The wafers are then lapped with alumina on a planetary-type lapping machine which achieves the dual objectives of reducing the wafers to desired thickness and providing plano-parallel surfaces. The latter is very important in subsequent diffusion and alloying operations to insure plane-parallel p-n junction fronts. The final step, etching, serves to both clean the surfaces of contaminants and "damaged" silicon and to provide a suitable surface finish for diffusion and alloying.

FIGURE 1

Process Flow Chart



2. Diffusion

The steps described immediately above are preparatory to the first major fabrication step: diffusion. The diffusion operation is designed to simultaneously establish impurity gradients of p-dopant on both faces of the etched silicon wafer. This is done in sealed quartz ampoules at temperatures of about 1200°C with typically aluminum or gallium serving as the p-dopant material. The precise time-temperature relationship is determined from device design considerations which dictate the diffusion gradient of impurities, the surface concentration (C_o) and the junction depth (x_j).

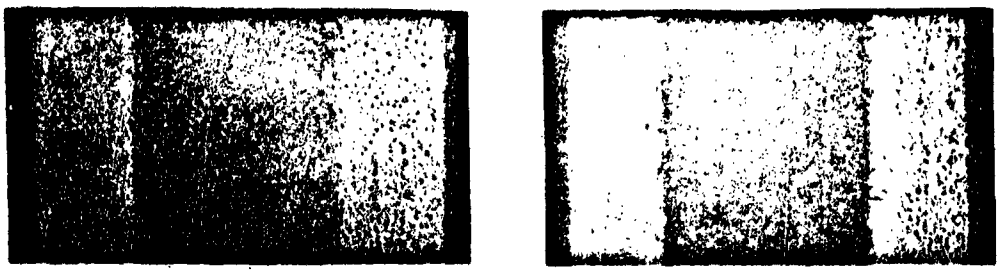
During this period, two diffusion runs have been carried out. The Type 2 design already described in the preceding contract report has been used exclusively. In order to minimize possible diffusion irregularities resulting from either crystal properties or diffusion parameters, the surface concentrations have been held somewhat below 1 x 10^{18} cm^{-3}, the value prescribed by the Type 2 design. Diffusion results are listed in Table III.

TABLE III

Diffusion Evaluation Data

Run #	Slice Thickness (μ)	Diffusant	Junction Depth (μ)	Surface Concentration (cm^{-3})
489/1	180-210	Gallium	50	6.5 x 10^{17}
493/1	180-210	Gallium	52	8 x 10^{17}

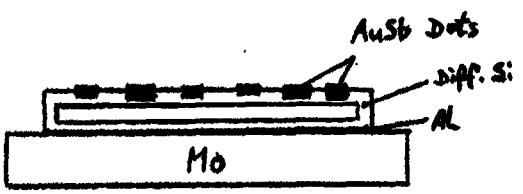
In both cases, the slices were cooled down to temperatures below 450°C, with controlled cooling rates before removal from the diffusion furnace. Figure 2 shows typical p-n-p transition regions as obtained from 90° junction delineation.



Picture No. 1 300X Picture No. 2

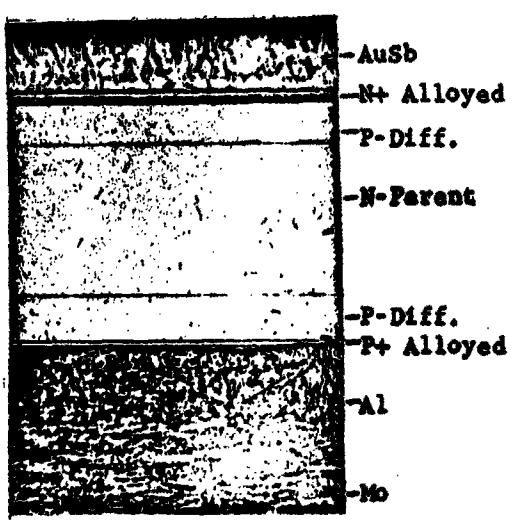
90° Gallium Diffused Junction Delineation

Figure 2



Control Sample Configuration

Figure 3



Cross Section of Alloyed Junction

Figure 4

3. Alloying

The second major fabrication step is that of alloying. This operation is designed to form the cathode p-n junction, ohmic contact to the gate region and ohmic contact to the anode region. Table IV tabulates the component parts comprising the fusion assembly.

TABLE IV

Fusion Assembly Parts

Part	O.D. (cm)	I. D. (cm)	Effective Area (cm^2)	Denotation in Structure
Molybdenum	3.34	------	8.75	Anode
Aluminum	2.86	------	6.15	Anode Emitter
Silicon	2.86	------	6.15	P-N-P Diffused Si
Gold-Antimony	2.54	0.3	5.00	Cathode Emitter
Gold-Boron	0.22	------	0.038	Gate Dot

Deviations from the proposed dimensions listed in Table III of the first contract report resulted from available silicon diameters. In order to maintain full-load current densities comparable with existing devices, the O. D. of the gold-antimony emitter had to be 25 mm.

An evaluation technique used to check the blocking capability and the turn-on characteristics of diffused silicon wafers utilizes special control samples. Nine gold-antimony dots of different thickness are alloyed across the entire area of the silicon wafer as shown in Figure 3 (Page 11).

Table V gives results of both control samples and standard 500A controlled rectifier samples after alloying and surface treatment.

TABLE V

Results of Alloying Runs: Controls and 500A SCR's

Diff. Run	Crystal	Alloy Assembly Structure	AuSb-Th. (u)	Range of Breakover Voltage at 25°C (V)	Range of Breakover Voltage at 130°C (V)	Typical Reverse Voltage at 25°C (V)	Typical Reverse Voltage at 130°C (V)	(1) I_g at 25°C (mA)	(1) V_F/1A/25°C (V)
489/1	3013	Controls	25	850-740	464-496	500(2)	350(2)	-------	----------
			30	640-720	528-640	500(2)	350(2)	-------	----------
			35	608-672	496-608	500(2)	350(2)	-------	----------
493/1	2995	Controls	30	320-780	336-840	1000(3)	1050(3)	------	----------
			35	272-784	208-784	1000(3)	1000(3)	------	----------
			40	100-768	68-480	1000(3)	1000(3)	------	----------
489/1	3013	500A SCR	33	0-800	0-24	900(2)	600(2)	15-60	0.8-0.9
	3011		30	0-704	0-136	900(2)	400(2)	20-100	0.8-1.02
493/1	2995	500A SCR	28	0-924	0-720	500	500	250	0.99-1.38(4)

(1) I_g = Gate Current, D. C.; V_F = Forward Voltage Drop, D. C.

(2) High Leakage Current

(3) Avalanche Breakdown

(4) Not "fired" completely

Several cross-sections were made in order to check the flatness of alloyed fronts. Figure 4 (Page 11) represents a typical alloyed region at 200X magnification. From the evaluation data one may draw the following conclusion:

a. Diffusion Run 489/1 with crystals 3013 and 3011 yields very sensitive switching characteristics and relatively high leakage currents. Shorts in the forward direction may result from crystal properties prior and after diffusion in conjunction with alloying. (Compare data of crystals Nos. 3013, 3011 vs. No. 2995). Diffusion parameters do not vary such that major differences could be expected.

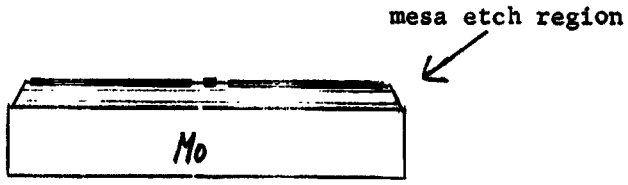
b. Diffusion Run No. 59311 with crystal No. 2995 yields less sensitive switching, though shorts in the forward direction could not be excluded. Reverse leakage currents are reasonable. Forward voltage drops are somewhat higher, probably due to the thinner gold-antimony emitter.

c. Blocking voltages up to 1000V can be applied before punch-through or breakdown occurs and breakover voltages greater than 500V/130°C can be reached by this design.

4. Surface Treatment

a. Control Samples. To evaluate the blocking voltage on the control wafers, the Au-Sb dots are masked with wax (See Fig. 3). The unmasked portion (silicon) is etched until the forward and reverse junctions are isolated. The wax is then removed and the etched portion is coated and cured.

b. Standard 500A SCR'S. The silicon edge extending beyond the cathode junction is rather narrow. Thus, a mesa-type etch is used to isolate the anode and gate regions as shown in Fig. 5. The field at the junction is reduced by shaping the edge at a shallow angle. A standard etch is used on the junction.



Edge Geometry After Isolation of Gate and Anode Regions

FIGURE 5

Electrical data of both the alloyed controls and the regular fused elements have already been presented in paragraph 4. Regular units are checked immediately after etching for the forward and reverse a.c. blocking voltage, the d.c. gate voltage and current, and the forward voltage drop at 1 amp d.c. The tests are conducted at room temperature. If the leakage current is low, the unit is coated and cured. The blocking voltages (a.c. and d.c.) are again checked at room temperature and elevated temperature on the coated device. The unit is then temperature cycled between 25° and 200°C to insure a stable unit.

The control units are checked for the forward and reverse a.c. blocking voltage. These tests are conducted at room temperature and elevated temperature. The purpose of the control wafers is two-fold. First, uniform voltages across the entire device indicate a good diffused slice, and

second, by using various gold thicknesses for the AuSb dots, the proper thickness can be determined for optimum forward blocking voltage, good temperature dependence, and low forward voltage drop.

5. Encapsulation

None of the fused elements have been encapsulated to date.

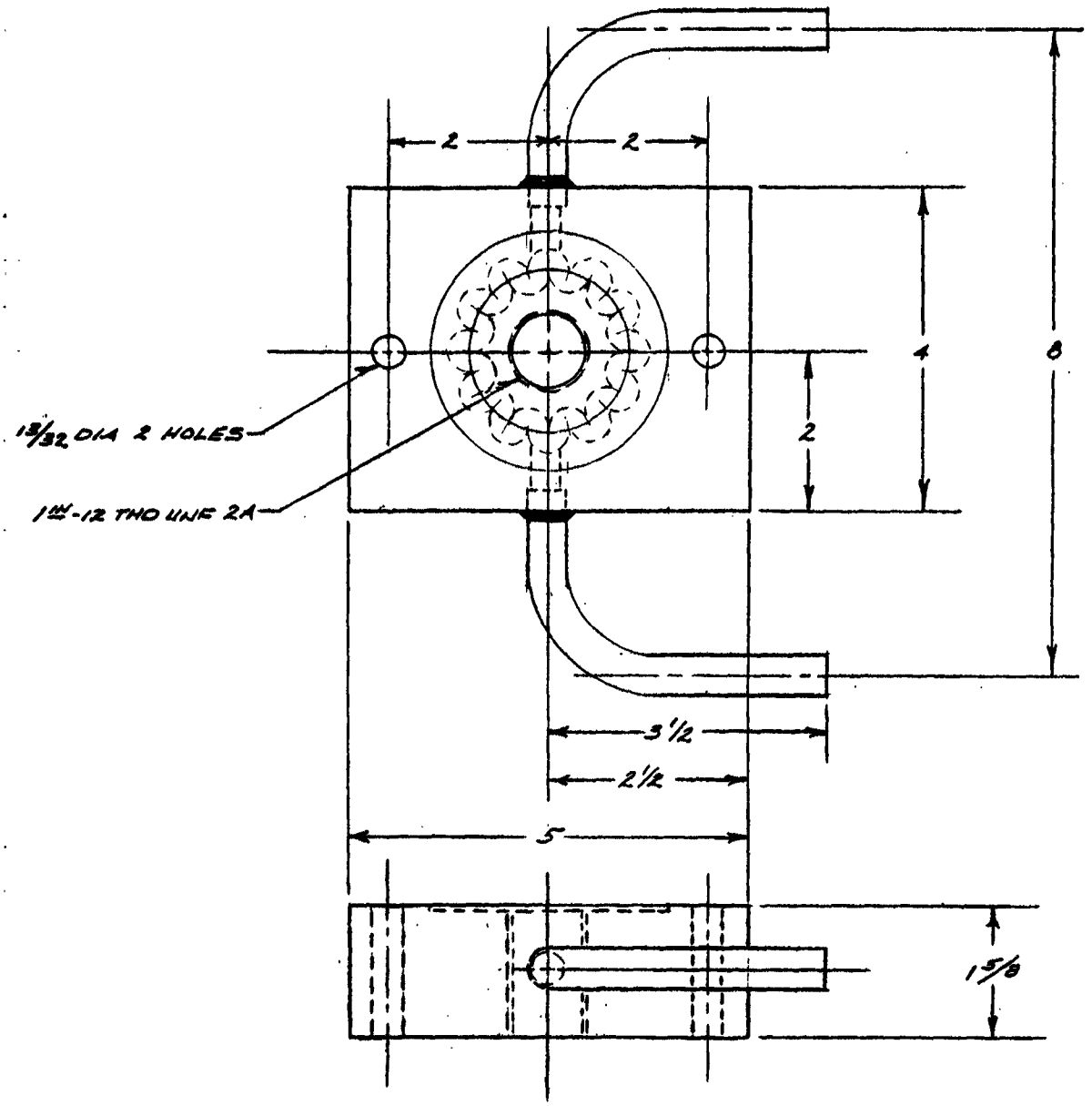
G. DEVICE EVALUATION

Wattage dissipation for the high power device is expected to approach one kilowatt while conducting 500 amperes average half wave current. Efficient heat transfer is required to maintain device operating junction temperature to 125°C. Three series thermal paths must be considered in dissipating heat from the junction; (1) junction-to-case; (2) case-to-sink; and (3) sink-to-cooling medium. The latter two items will be lumped and considered in the following text for test fixture heat sink design.

Based upon the design parameter of 1.8 volt peak forward drop at $300A/cm^2$, the power dissipation was calculated at 750 watts under rated conditions. An efficient dissipator is required to remove this heat.

A number of heat sink designs were considered. The design shown in Figure 6 has been chosen for manufacture and evaluation.

To obtain maximum heat transfer between heat source and cooling medium, turbulent fluid flow is required. It is expected that the rosette water passage pattern shown will produce maximum turbulence of the fluid. The flow passage is divided to assure uniform cooling of the heat sink and consequently, the test device. Following completion of the heat sink, cooling efficiency will be measured and reported.



TEST FIXTURE HEAT SINK DESIGN

FIGURE 6

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H. DELIVERY

It is anticipated that delivery of state-of-art samples will be on schedule.

J. CONCLUSIONS

The procurement of large diameter silicon has been satisfactory to date. However, this area of study must be considered problematical until such time as a consistent supply of quality material, where quality material is defined as that which produces devices to specifications, is assured.

The first sub-phase of both basic device structure and encapsulation are considered complete. Optimization and refinement are underway, and will receive great impetus as the sample fabrication phase progresses.

Sample fabrication was initiated in this report period. However, only preliminary results - as reported in Section I.F - are available. These initial results are considered very satisfactory.

The first sub-phase of device evaluation is also considered complete. Work in this area will continue as prototype units are produced.

SECTION II

A. PROGRAM FOR NEXT INTERVAL

Effort will continue along the lines indicated in this report. Emphasis will shift to fabrication of completed devices such that optimization and refinements in the various study areas can be initiated. The intermediate goal of this work is the fabrication, evaluation and delivery of twenty state-of-art samples as per the contract schedule.

B. PROJECT PERFORMANCE AND SCHEDULE

See Figure 7.

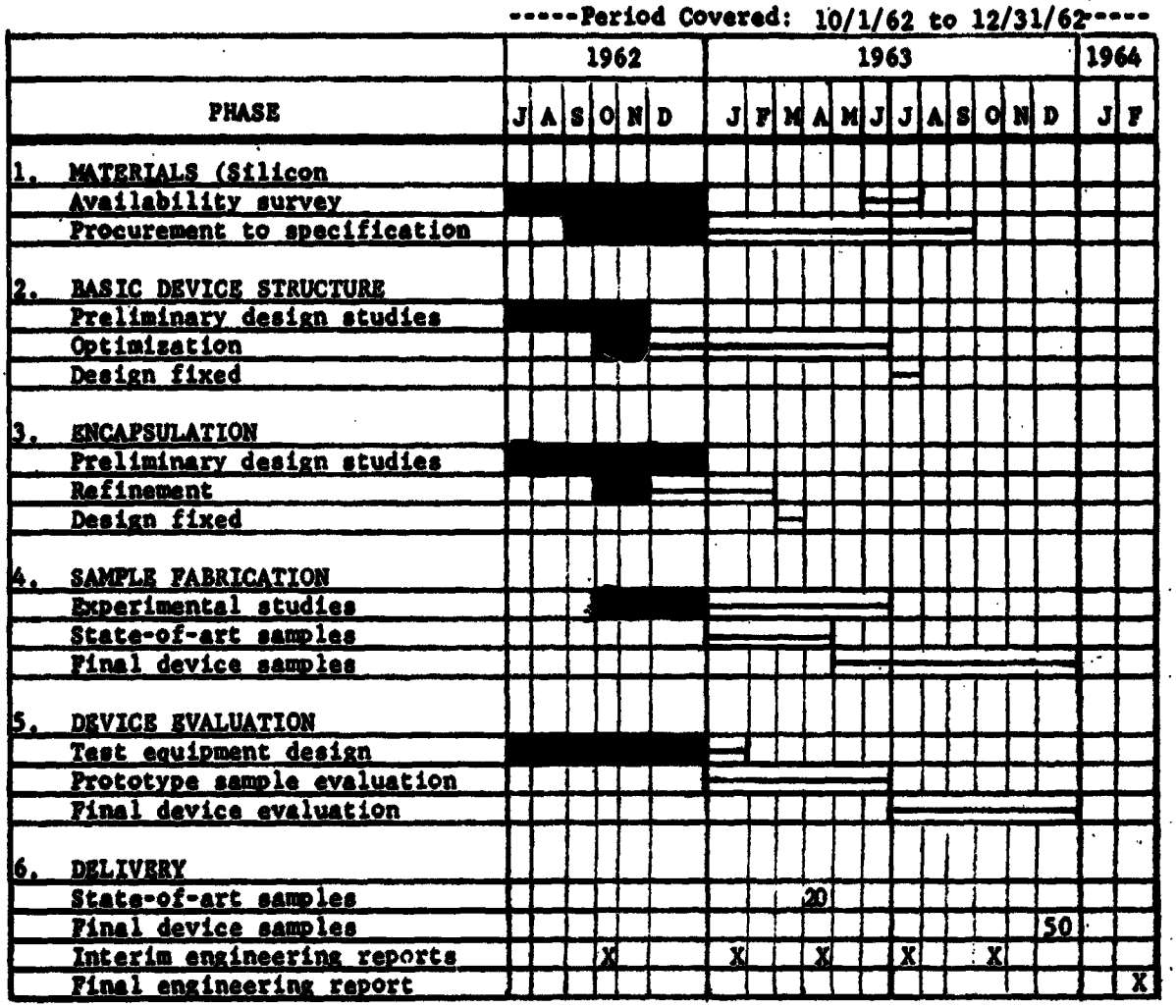
WESTINGHOUSE ELECTRIC CORPORATION

Project Performance and Schedule

Project No. SR-0080301 Task No. 9348

Contract No. NObsr-87647 Date: 31 January, 1963

-----Period Covered: 10/1/62 to 12/31/62----



LEGEND Work Performed Schedule of projected operation

Estimated Completion in Percent of Total Effort Anticipated by Phase

1. Materials ----------40%
2. Basic Device Structure -35%
3. Encapsulation ----------25%
4. Sample Fabrication - 5%
5. Device Evaluation---20%
6. Delivery- - - - - - - 0%

Figure 7