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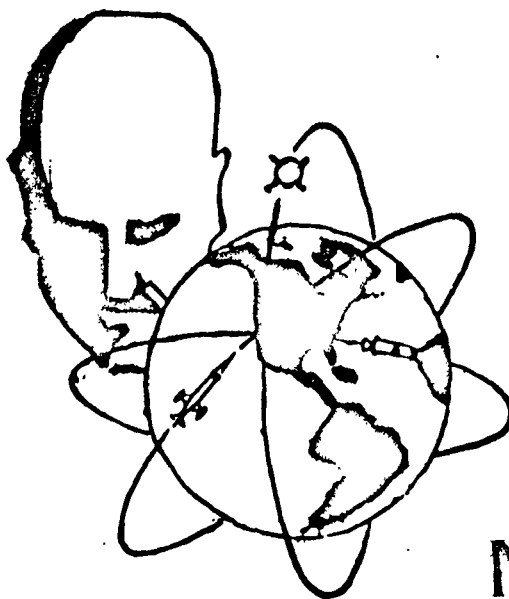
473L DPSS/ICSS INTERFACE DESCRIPTION

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ABSTRACT

This document contains material generated at meetings of the 473L Subsystem Integration Design Group (SIDG). Technical material presented herein does not constitute a specification but represents a generally concurred on description of the interface between the 473L Data Processor (AN/FYQ-11) and the System Integrated Consoles (AN/FYA-2, 3, and 4.).

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473L DPSS/ICSS INTERFACE DESCRIPTION

1.0 INTRODUCTION

The 473L Data Processing Subsystem (DPSS) communicates on a real-time basis with a number of input/output consoles comprising the Integrated Console Subsystem (ICSS). These consoles are of three types designated the AN/FYA-2, AN/FYA-3 and AN/FYA-4 respectively and differing principally in the aggregation of major functional components provided in each.

The AN/FYA-2 console (Type A) contains all major components, these being:

1. Electronic Typewriter/Display (ET)
(includes Control Keyboard)
2. Logic Keyboard Assembly (LKB)
3. Multicolored Display (MC)
4. Hard Copy Device (for MC) (HC)
5. Console Printer (CP)

The AN/FYA-3 Console (Type B) contains only items 1, 2 and 3 of the above. The AN/FYA-4 Console (Type C) contains only items 1 and 5.

The detailed description of these integrated consoles may be found elsewhere.

This document describes the electrical and functional interface between these consoles and the DPSS and establishes their mode of interaction.

The DPSS and the ICSS will be installed in two phases. These are the IOC phase (Interim Operational Capability) and the COC phase (Complete Operational Capability). The IOC phase requires a partial implementation of system equipment configuration and involves the use of only one AN/FYQ-11 data processor and 4 integrated consoles. For the sake of generality, the following description relates to the COC configuration of which the IOC configuration is but a subset. With the exception of the implications of "duplex" switching between two data processors, the larger number of consoles and the references to the Large Panel Displays, the console interface descriptions are equally applicable to the IOC configuration.

1.1 General Description of DPSS/ICSS Interface

In general, the DPSS provides separate and distinct interfaces for communication with each of three major functional areas in the integrated consoles.

- These are:
1. ET, and Control Interface (incl. LKB)
 2. MC Display Interface (incl. Large Panel Displays)
 3. Console Printer Interface

An I/O register directly associated with the computer portion of the Data Processor communicates directly with the ET and CONTROL area of the consoles by high speed data transfer in either direction. This ET and CONTROL interface handles all Integrated Console inputs to the Data Processor and all outputs to the ET Display, Logic Keyboard and the Control Keyboard. (i.e., all communications to the console except M-C display and console printer outputs).

The DPSS communicates with the M-C Displays via an area of the MASS MEMORY unit designated the Mass Memory Buffer Store (MMBS).

The M-C Display interface provides solely an output capability, data being transferred from the DPSS to the M-C displays on a word demand basis.

The DPSS communicates with the Console Printers via an area in the MASS MEMORY unit designated the Mass Memory Console Printer Store (MMCPS). An output capability only is provided, data being transferred from the DPSS to the Console Printer on a character demand basis.

Console inputs to the DPSS functionally related to the M-C Displays or Console Printers are transmitted via the ET and Control interface.

In addition to the above, the DPSS communicates with Large Panel Displays in an output function only and via the M-C Display interface. Separate channels in this interface functionally identical to those provided for M-C Displays provide for DPSS output to future LP displays on a word demand basis. Since the LP displays have not yet been specified, this part of the interface is considered tentative.

The COC configuration of the Data Processing Subsystem will provide 15 ET and Control input/output channels and 11 M-C Display, 15 Console Printer and 8 Large Panel Display output channels. With the exception of the 8 LPD channels, the above channel complement is duplicated in each of the two data processors and any or all consoles may be manually switched to either processor with no degradation of output capability (other than that which may result from increasing the load on a given processor).

Only 4 basic LPD channels are provided in each of the two data processing subsystems. The 4 basic output channels are expanded to 8 by processor controlled switching which permits time sharing of outputs to two Large Panel Displays. Any or all LP displays may be manually switched to either Data Processing subsystem but if more than 4 are switched to one processor, time sharing of affected channels will reduce output rate to the related LP displays.

The ET and Control interface input/output channels are not capable of simultaneous operation. No buffer storage is provided and all consoles communicate directly with the same I/O register on a sequential basis for input and on a program selected basis for output. The same I/O register is used to communicate with the DATACOM interface. Data transfers via this register, however, are of sufficient speed that effective practical simultaneity of operation of the Integrated Consoles is achieved. This is further aided by the essentially "off-line" mode of operation of the Consoles between data transfers.

Data transfers to the M-C and LP displays involve a substantial amount of buffer storage in each MMBS. The MMBS is shared among all connected M-C and LP displays, but each output channel contains recirculating storage for two blocks of data. Consequently, outputs via these channels can proceed simultaneously with only minor interactions during channel accesses to the MMBS or data processor accessing of the MMBS.

Data transfer to the Console Printer is via separate buffer storage in the MMCPs allocated to each Console Printer output channel. Outputs via each channel can proceed independently and simultaneously with only minor interactions.

In the COC configurations, all consoles and Large Panel displays interface with the DPSS through manual duplex switching which permits assignment of each console or LPD to either Central Processor. Any or all of the consoles or LPDs may be simultaneously and independently assigned to either processor or they may be distributed between the two processors in any manner desired to meet operational requirements.

The manual switching is accomplished independently for each interface area so that the ET and Control, M-C display and Console Printer portions of each console may be individually assigned to either processor subsystem. Ordinarily, all components of a console would be assigned to the same processor, however failure of a Mass Memory unit may require placing all M-C displays and Console Printers on the remaining Mass Memory unit while the ET and Control portions remain distributed between two processors. Switches for 10 M-C and 32 Console's are electrically ganged.

The Central Processor program may test the status of the manual duplex switching to determine which interface channels on either processor are actively connected to consoles or LP displays.

The manual switching does not provide the capability to switch devices from one channel to another in the same processor subsystem nor to any arbitrary channel on the alternate processor subsystem. Switching only occurs between a given channel and its alternate. Change of channel assignments beyond this requires relocation of device connectors.

A general outline of the DPSS/ICSS interface including the tentative duplex manual switching is shown in Figure 1 (a).

Figure 1 (b) shows the Large Panel Display interface as it is defined at this time. Although this interface is tentative and cannot be confirmed until the Large Panel Display subsystem is specified and defined in detail, it is expected that little change will occur in the portion described herein.

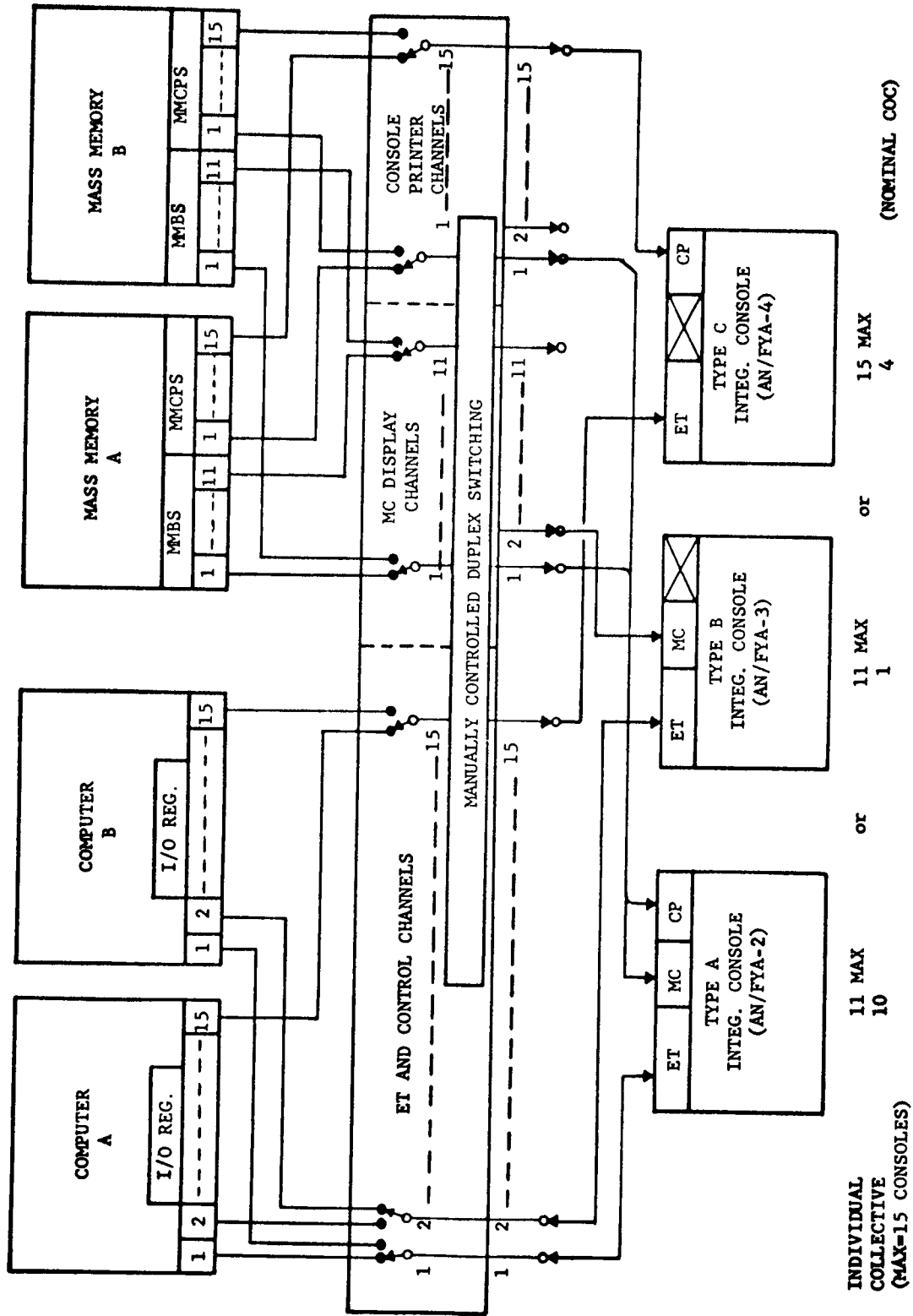
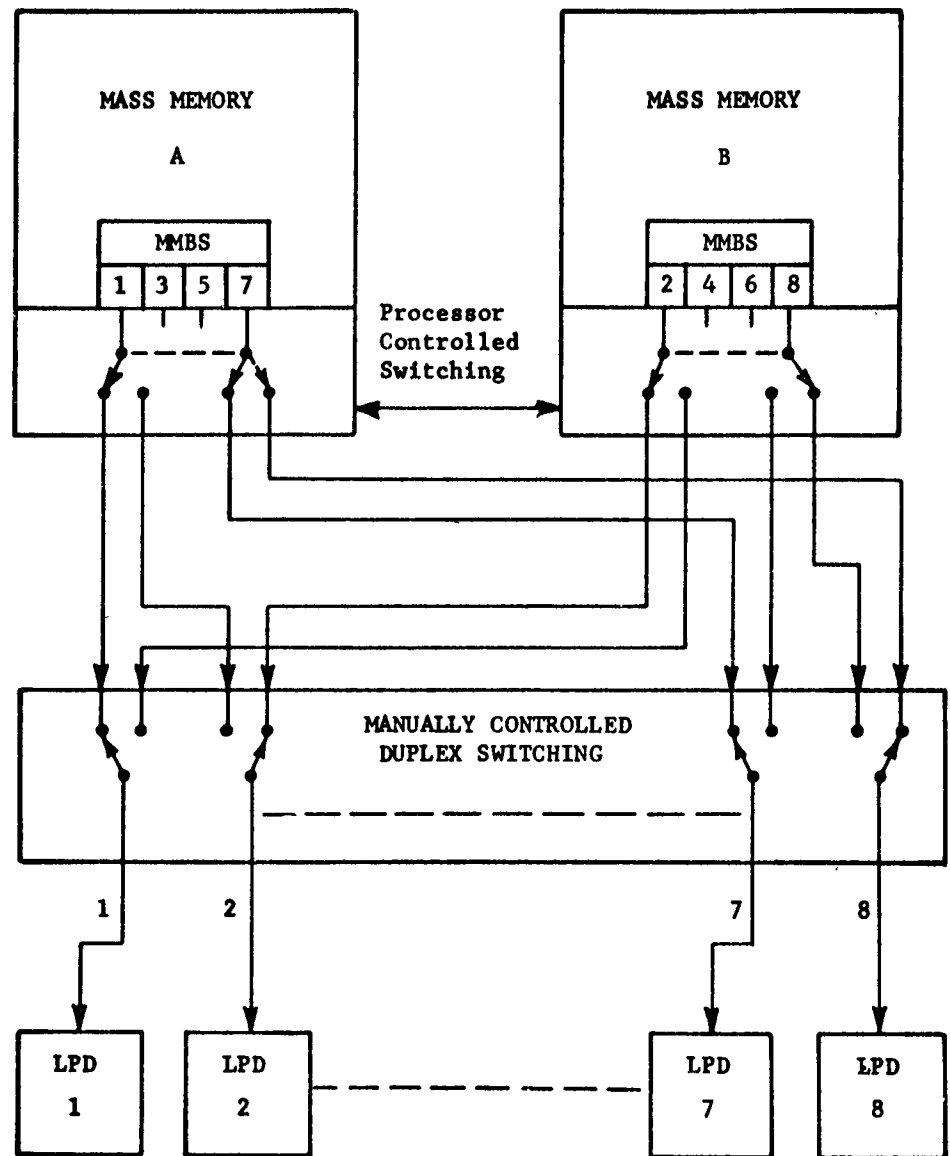


Fig. 1a DPSS/ICSS INTERFACE (SCHEMATIC ONLY)



LPD's 1 & 2 are shown switched to individual channels
 LPD's 7 & 8 are shown switched to time share channel 7
 of MMA

NOTE: Neutral OFF position may also exist on all manually
 controlled switches

Fig. 1b DPSS/LPD INTERFACE (SCHEMATIC ONLY)

2.0 ET AND CONTROL FUNCTION INTERFACE

The ET and Control Function Interface is illustrated grossly in Figure 2.

ET and control messages are carried in a two-way transmission function over an individual set of lines for each ICSS. These lines communicate directly with a special input-output register connected with the processor core memory, which is also used for Digital Data Link transmission.

"Input to Processor" requests (Message Available signals from the ICSS's) are scanned, with all the Digital Data Links being considered every time an ICSS is considered, to produce a processor "Input" interrupt. The processor, programmatically, determines the source of input, allocates space in core memory and initiates the input operation proper. The processor continues its program execution and may test for completion of the input process. At the end of the message transfer, the processor will receive an "I/O Interface Not Busy" interrupt.

Outputs to the ICSS and Digital Data Links are initiated by processor program execution. Outputs are from core memory through the input-output register used for input and proceed independent of program execution. Outputs are sent by address directly to the receiving device without operator intervention but responsive to the "Device Available" signal which indicates console status. A console, when not in the INPUT mode, is always ready to accept an output control message and an output to the ET display usually occurs in response to an input control message request coupled intrinsically with readiness of the ET to receive the output message.

When output to the ET Display occurs in response to a control message request other than those originating in the Logic Keyboard, activation of the request control key clears the ET Display so that it is ready to receive the requested message. When the output to the ET Display occurs in response to a Logic Keyboard operation or without operator request, the ET Display is cleared by the console on receipt of the Message header and prior to transmission of the rest of the message. In the latter instances, transmission of the body of the output message is delayed by the receiving device for approximately 16 milliseconds while the ET Display is cleared.

The 3155 computer program can precede the transmission of an output message by a test of the state of the duplex switching.

The actual output process is initiated by executing an output instruction defining the destination device (with the field selection characters) and the (indexed) memory location of the first word to be transmitted. During transmission, this instruction is held in a special input-output instruction register, so the computer can proceed with its program. Core memory accesses are made by interrupt at logic level.

The output process begins with a signal on the Output Priority Line to the selected device. The device must answer on the Device/Message Available line, or the transmission aborts. Transmission begins when the first data bit is on the Output Data line and the Input/Output Operation line goes ON. Device clock pulses gate successive bits of the message.

The output operation terminates when the device signals Output Operation Complete in response to receipt of an EOM character.

If the computer detects bad parity in a word it is about to transmit, it removes the Input-Output Operation signal, aborts the transmission and causes an error interrupt in the program. This condition is noted in the device and any retransmission is made under program control.

If the receiving device detects bad parity in a character, it removes the Device/Message Available signal, not having sent an Output Operation Complete signal. This condition aborts the transmission and causes a second type of error interrupt in the program. The processor program may attempt to retransmit the aborted ET message. If errors persist, the program may retransmit the ET message with a special header. This header is recognized by the receiving device which then accepts the entire message regardless of parity errors and without sending error signals back to the processor or aborting transmission. The resulting ET Display, in this instance, will show special flashing symbols in place of characters on which bad parity is detected.

If an output instruction selects a device that does not respond with a Device Available signal, a third type of error interrupt occurs. As duplex switching status is separately program testable, this error condition presumably indicates an inoperative device.

The same lines used for output carry input messages. The input process is signified by an absence of a signal on the Output Priority line.

The input process begins with a device originated signal on the Device/Message Available line. A scanner selects one of the devices asking to input and causes a program interrupt. Transmission begins when the computer executes an input instruction which sends a signal to the selected device on its Input-Output Operation line. The device responds by sending Data and Device Clock. Core memory accesses are made by interrupt at logic level. The input instruction carries the (indexed) memory location where the input message is to start.

The input operation terminates when the computer detects an EOM character and signals Input Operation Complete.

If the computer detects bad parity in a word it is receiving, it removes the signal on the Input-Output Operation line without sending Input Operation Complete. No more characters will be received, and an error interrupt occurs in the program. The device notes failure of reception and the message retransmission, if desired, is performed by the console operator.

The device may recognize that it has bad parity in a character it is sending and abort the transmission by removing the Device/Message Available signal. This is noted in the computer and an error interrupt occurs in the program.

If the device fails to send its clock in response to the Input-Output Operation, a hang-up occurs in the interface. The hang-up is ended by a timer which frees the interface to respond to other inputs and outputs and generates a "Hang-up Error" interrupt.

Any error interrupts to the program in the computer may be selectively ignored, under program control.

2.1 Data Transmission Rate

Data is transmitted between the Data Processor I/O register and the ET and control portion of the integrated console at a rate of 720±15% kilobits/sec. Data is transmitted in a "Non-Return to Zero" (NRZ) signal mode to or from the console and is timed by a console originated clock signal establishing the actual rate of transfer. The maximum data transfer rate acceptable by the Data Processor is 1.1 megabits/sec.

2.2 Message Formats

The two types of messages transferred in the ET and control function interface are ET Display Messages and Control Messages. Data transmission formats are in general governed by the Data Processor 56 bit word format which is alphanumeric and contains 8 characters each comprised of 6 bits plus parity. Data is transmitted to and from the processor, in this interface, serially by bit on a character basis. Each word is transmitted with the least significant bit of the most significant character first in the sequence (i.e., Bit 1, Character 7; Bit 2, Character 7;..... Bit 7, Character 7; Bit 1, Character 6; Bit 2, Character 6;..... Bit 7, Character 6;..... Bit 1, Character 0; Bit 2, Character 0, etc.) Normally, the format of every message transferred in this interface is headed by a control character, which identifies the nature of the message, and is terminated by an "EOM" character.

2.2.1 ET Message Formats

ET messages from the Data Processor to the console are destined for display on the ET display surface and would normally not exceed 2370 characters including the message header and the "end of message" (EOM) character (i.e., one ET display page). The length of an ET message is arbitrary up to this value. In any event, the console terminates the transmission on receipt of EOM or the 2369th character, whichever occurs first.

ET messages transmitted from the console to the Data Processor cannot exceed 2370 characters including the message header and the EOM character because of limit in page size. The actual length of ET messages transmitted by the console is arbitrary up to this number.

2.2.1.1 Data Processor to Console

The message format applicable to ET message transmissions from the Data Processor to the console is shown in Figure 3. The control character heading the format has two states applicable to ET message transmissions. These designate ET Type 1 and ET Type 2 messages. ET1 messages are subject to interrupt on parity error detection. ET2 messages are transmitted to the ET display in entirety regardless of parity errors occurring during transmission. In the latter case, parity errors are nevertheless detected and indicated to the console operator.

The control character heading the ET message occurs only in the Character 7 position of the first word of the message. Subsequent words may be fully packed with alphanumeric symbol data. The EOM character terminating the message may occur in any character position of the appropriate word in the sequence. The first displayed character in the message is that appearing in the Character 6 position of the first word of the message. Subsequent characters follow in sequence according to the Data Transmission sequence described in Paragraph 2.2.

In an ET message the only control character used other than the header and EOM characters is the "Lower Case" code which may occur anywhere in the ET message and causes the ET to perform the "carriage return/line feed" function. No symbol is displayed on the ET corresponding to this character code.

2.2.1.2 Console to Data Processor

The message format applicable to ET message transmissions from the console to the Data Processor is shown in Figure 3. The first character transmitted in any ET message is a control character identifying the message as an ET message and in some instances indicating to the processor the operation to be performed on the input data. Bit positions 5 and 6 of the control character are used to indicate to the processor which of the three display pages available to the ET Display is being transmitted. The first line of the ET Display (64 characters) is reserved for further instruction to the processor regarding the disposition of the following portion of the message. This line is used for such things as routing address, storage address, etc. Consequently, the format of a complete ET input message header consists of a control character followed by 64 characters in which direction to the processor is given. This is followed by the body of the ET message and terminated by the EOM character. The total ET input message, including header and EOM, cannot exceed 2370 characters. The EOM character can occur anywhere in the ET message following the control character.

The control character code is not responsive to control by the alphanumeric keyboard on the console nor is it displayed on the CRT. The control character for a given message is in general set up by console pushbutton action. Consequently, a direct relationship exists between the character codes utilized and corresponding pushbuttons on the Integrated Console. The utilization and significance of the control character codes available are shown in Figure 3.

2.2.2 Control Message Formats

All control messages transferred between the DPSS and the Integrated Console are headed by a control character identifying the message as a control message. The control character may also contain other information relative to the control function to be performed.

2.2.2.1 Data Processor to Console

The message format applicable to control messages transmitted from the Data Processor to the console is shown in Figure 4(a). These messages consist of two 56 bit words and are terminated by an EOM character at the end of the second word. The control character heading the control message designates whether a CM Type 1 (CM1) or CM Type 2 (CM2) message is being transmitted. Parity error in a CM1 message does not indicate error to the console operator but requests retransmission of the message by the processor. If a parity error occurs in a CM2 message, transmission is aborted, all control indicators*on the receiving console are not changed, and an appropriate error indicator is lit on the Integrated Console. ("Message Waiting" counters on the console remain at existing count) (* Logic keyboard indicators will be cleared to OFF.)

With the exception of the characters transmitted controlling the logic keyboard indicators, all characters have "Zero" in bit positions 4, 5, and 6. Logic keyboard control characters always have a "one" in bit position 6. Bits in positions other than those fixed above (except parity) may have any simultaneous values so that a single control message can simultaneously establish several control or indicator conditions. (Obviously some combinations are contradictory and would not normally occur) The location and significance of control message codes are shown in Figure 4(a).

2.2.2.2 Console to Data Processor

The message format applicable to transmission of control messages from the console to the Data Processor is shown in Figure 4(b). These control messages are initiated by console pushbuttons and consist of four characters only. The first character (Ch. 7) uniquely identifies the message as a control message by means of the values 1111 or 1001 in bit positions 1, 2, 3, and 4 respectively. Bits 5 and 6 of the control character designate the ET display page being viewed at the time of transmission of the control message.

Character 4 of the control message is always an EOM character signifying the end of transmission.

Characters 5 and 6 have different meanings depending on whether the control message is originated by the Logic Keyboard or by a control pushbutton. In the former case, character 6 indicates which overlay is in place on the Logic Keyboard while character 5 indicates which Logic Key was depressed. In the latter instance, character 6 is

always "ZERO" and character 5 indicates which control pushbutton was activated. The codes assigned for character position and their significance are shown in Figure 4(b).

2.3 Transmission Modes

2.3.1 Data and Control Lines

The following signal lines are used for transmission of control and ET messages to and from the console. Several lines are dual purpose carrying different signals depending on whether the console is in the "Input Mode" or in the "Output Mode." "Input Mode" is defined as the condition wherein the console is transmitting data to the Data Processor. The "Output Mode" exists when the Data Processor is transmitting data to the console.

Line	Input Mode		Output Mode	
	Function	Signal Source	Function	Signal Source
1	Input Operation	Data Proc.	Output Operation	Data Proc.
2	Input Op. Complete	Data Proc.	Output Data	Data Proc.
3	Output Priority	Data Proc.	Output Priority	Data Proc.
4	Device Clock	Console	Device Clock	Console
5	Input Data	Console	Output Op. Complete	Console
6	Message Available	Console	Device Available	Console

The functions of each of these lines are outlined below.

Line 1 - Input/Output Operation (I/O OP)

When in Input Mode this line will go true in response to a "Message Available" signal from the console when the Data Processor is ready to receive the message to be transmitted. Under these conditions, the "True" state of this line indicates that an Input Operation is in progress. The I/O OP line goes false if a parity error is detected by the processor in the incoming message.

When in output mode, this line goes true in response to a "Device Available" signal transmitted by the console on receipt of a Data Processor request to output a message (Output Priority). The true state of the I/O OP line under these conditions indicates that an output operation is in progress. This line will go false if a parity error is detected by the processor in the output message.

Line 2 - Input Operation Complete/Output Data (IOC or OD)

In Input Mode, this line goes true when the Data Processor successfully receives an EOM character signifying the end of the input transmission.

In Output Mode, this line carries the data transmitted by the processor to the console.

Line 3 - Output Priority (OP)

In Input Mode this line remains false indicating that the console is in the Input Mode.

In Output Mode this line is set true by the processor to indicate to the console the start of Output Message sequence.

Line 4 - Device Clock

In both Input and Output Modes this line carries console generated clock signals used to synchronize transfers of data to and from the console.

Line 5 - Input Data/Output Operation Complete (ID or OOC)

In Input Mode this line carries data transmitted by the console to the Data Processor.

In Output Mode this line is set true by the console on successful receipt of the EOM character (or on receipt of 2369 characters) signifying completion of the transmission. The line will remain false if a parity error in the transmitted message is detected at the console. (Except when an ET2 message is transmitted)

Line 6 - Message Available/Device Available (M/D A)

In Input Mode this line is set true by the console to indicate that a message is ready for transmission to the Data Processor. Provided the OP line is false, the true state of this line causes an "input interrupt" and places the console in the input mode.

In the Output Mode this line goes true in response to receipt of an Output Priority (OP) signal, signifying that the console is operating and ready to receive an output message. This line will go false if a parity error in the transmitted message is detected at the console. This line

is interlocked with other console originated signal lines to ensure that no console error or failure will tie up the I/O interface of the central processor. The false state of this line signifies functional disconnection of the console of "Device Not Available."

2.3.2 Normal Output Operation (DP to IC)

The relative timing of signals and data relevant to an output transmission is shown in Figure 5(a).

An output operation is initiated by the Data Processor by causing the Output Priority Line (OP) to go true. In response to this action the Device Available line must be set true by the console within 6μ seconds. If the Device Available line does not go true after 2μ seconds and before 6μ seconds after the OP line goes true, or is true before OP goes true, a "Hang-up Error" interrupt of the Data Processor will occur causing the console to be functionally disconnected for that operation.

The Output Operation line will go true, signifying commencement of output transmission, in response to the console originated Device Available signal at $8+2\mu$ seconds after the Output Priority line goes true. The first data bit is present on the Output Data line at the time that the Output OP line goes true. The console then supplies clock pulses on the Device Clock line controlling output of data.

Upon receipt of the EOM character signifying the end of the transmission, the console switches the Output Operation Complete line (OOC) to the true state for one bit period. In response to the true state of the OOC line the processor returns the Output OP and Output Priority lines to the false state. Clock pulses are supplied by the console until the Output Operation line goes false. The Device Available line will be set false by the console at the end of an output operation, coincident with the return of OOC to the false state.

The sequential states of the various control signals during an output operation are summarized in Table 1 below.

Call	Response	Transmit	End OP	Receive Error	Send Error	Device Inoperative
OP $\rightarrow$ 1	M/D A $\rightarrow$ 1	OP=1 M/D A=1 OOC=0 I/O $\rightarrow$ 1	OOC $\rightarrow$ 1 (EOM or full page)	M/D A $\rightarrow$ 0 I/O OP=1 OOC=0	I/O OP $\rightarrow$ 0 OP $\rightarrow$ 0	Hang-up error if: No M/D A $\rightarrow$ 1 or OP $\rightarrow$ 1 Attempted when M/D A $\rightarrow$ 1

TABLE 1

The ET Display cursor is normally positioned over the EOM character after completion of a data transfer from the processor. If a full page transfer is made (2369 characters including header) the cursor is automatically positioned in the first position of the second line of the ET Display.

2.3.3 Normal Input Operation (IC to DP)

The relative timing of control signals and data relevant to an input operation is shown in Figure 5(b).

An input operation is possible only when the Output Priority line is false. Under these conditions the input operation is initiated by the console setting the Message Available line (M/D A) true as a response to operator action.

In response to a true level on the Message Available line, the processor sets the Input Operation line true under program control. Clock pulses and data are then sent to the processor by the console on the Device Clock and Input Data lines.

Upon receipt of the EOM character signifying the end of transmission, the processor sets the Input Operation Complete line (IOC) true. The console must respond to a true level on the IOC line by returning the Message Available line to the false state.

The processor then returns the Input Operation line to the false state on receipt of EOM signifying completion of the input operation. The Device continues to send clock pulses until the IOC line is set false by the processor.

The normal sequence of control signals occurring in an input operation is summarized in Table 2 below.

Call	Response	Termination	Receive Error	Send Error	Device Inoperative
M/D A→1 OP=0	I/O OP→1 M/D A=1 IOC=0 OP=0	IOC→1 OP=0 (on receipt of EOM)	I/O OP→0 IOC=0 OP=0	M/D A→0 IOC=0 I/O OP=1 OP=0	No M/D A→1 on call

TABLE 2

2.4 Error Considerations

In general, three types of malfunction can occur in the DPSS/ICSS interface causing errors in operation. These are errors in the data being transmitted, errors in control line levels or sequence of operation and operator procedure errors. Reliance is placed on parity checking and in some instances code legality checks to discover errors in data transmission and initiate appropriate action. Parity is checked both at the console and at the Data Processor M Register on all message transmissions and error conditions indicated to the operator. Control line errors are detected or prevented by functional or direct interlocking where feasible particularly if such errors cause unwarranted serious degradation of the system. In the latter case, if a console is the source of the error condition, special devices are used to ensure that total interface hang-up does not occur.

Operator procedure errors, where not inhibited by console interlocks are in general detected by the processor program and indicated to the operator via the procedure error indicator and if appropriate by an ET display or console printer message.

Two of the control lines are used to signify error conditions detected at the processor and at the console. The Input/Output Operation line (I/O OP) is used to signal the console that an error condition is detected at the processor while the Message/Device Available line (M/D A) is used to signal the processor regarding error conditions detected at the console. In both instances, the false state of these lines when they would normally be expected to be true signifies an error condition and halts or prevents the operation in progress. In either case, a data processor interrupt occurs allowing the program and/or the console operator to take appropriate remedial action.

2.4.1 Error in Output Operation (DP to IC)

An output operation will consist of either an ET message transmission or a control message transmission. In either case parity is checked at the Data Processor M Register prior to entry of data into the I/O word register. Parity errors, if they occur, are detected at the end of the word and cause the processor to set the I/O OP line false. A false level on the I/O OP line in conjunction with the false state of the OOC line and the true state of the M/D A line indicates a Data Processor detected parity error. Transmission of the message is stopped and the console disconnected, by virtue of the I/O OP line going false, and an "M Register Parity Error" interrupt occurs.

Parity checking of both ET and control messages also occurs at the console. In addition the console performs legality checks on the first character (control character) of each incoming message. In event of a console detected error the console will cause the M/D A line to go false and continue to send clock pulses until the Input/Output Operation line (I/O OP) goes false. The processor will set the I/O OP and the Output Priority lines false within 5μ seconds after the M/D A line goes false, generate a "Data Parity Error" interrupt, and disconnect the console.

In the normal sequence of operations, detection by the console of the EOM character terminating a message, or receipt of 2369 characters causes the console to set the M/D A line to false state terminating transmission and freeing the processor I/O interface to service other devices. Failure by the console to detect EOM will cause transmission to continue until the 2369th "character" is received. If this condition fails to terminate transmission, a timer in the Data Processor will automatically terminate the operation. Any ET or Control message output not terminated normally or by a detected error will be terminated by the processor in 45-85* milliseconds, disconnecting the Console from this interface. The output operation is thereby terminated and an "I/O Hang-up Error" interrupt generated. (Adjustable by manufacturer)

All parity errors are indicated to the operator. If a parity or illegal code error is detected in the first character of an output message the console cannot determine what type of message is being received. The processor will attempt to retransmit the message in which the error was detected. After the third unsuccessful attempt, the message is aborted and an indicator on the console lit signifying the inoperative state of that console or output channel.

2.4.1.1 ET Message Error Operations

ET messages are normally transmitted to the console with an ET1 control character. Parity or other errors detected in the ET1 message are indicated to the processor as described above and cause cessation of transmission and disconnection of the console. Under program control, the processor may retransmit the message with an ET1 control character. If errors occur the second time, the processor may elect to retransmit the message with an ET2 control character. This control character causes the console to accept the message regardless of parity errors (except in 1st character) and display the message. Under these conditions, characters on which parity errors are detected are displayed as a special blinking symbol (■).

2.4.1.2 Control Message Error Operations

Control messages are normally transmitted to the console with a CM1 control character header. If a parity error is detected on a CM1 control message, transmission is halted as above and the control message is ignored. Under program control the CM1 message may be retransmitted by the processor. On a third attempt, the Processor may change the control character to a CM2 header. The console detects this header, ignores the input message if a parity error is detected and indicates an error condition to the operator. Control indicators remain unchanged. Further remedial action may be taken by the processor.

2.4.1.3 Control Line Error Operations

Control lines active during an output operation may fail in either the false or the true state at either the transmitting or receiving end. Console clock pulses may fail preventing transfer of

data out of the Processor I/O register. Since unilateral failure of the console clock can cause serious degradation of I/O interface this line where feasible, is interlocked with the Message/Device Available line at the console so that failure of clock signals will cause the M/D A line to go false effectively disconnecting the console. A summary of the effects of control line error on an output operation is given below. It is assumed that only one control line will fail at a time. When a timed disconnect occurs, this means that the output operation is terminated by the processor, the console is disconnected from the I/O interface and an "I/O Hang-up Error" interrupt is generated.

Line 1 - Input/Output Operation

Error 1

I/O OP Locked False

Result

Timed disconnect occurs.

Error 2

I/O OP Locked True

Result

Not absolutely determined. Either a normal transmission or a timed disconnect will occur.

Line 2 - Output Data Line

Locked in False or True state

Result

This will cause a first character parity or illegal code error at the console causing disconnection of console and a processor interrupt.

Line 3 - Output Priority (OP)

Error 1

OP Locked False

Result

Fails to signal output operation to console. Absence of M/D A→1 response from console signifies "Device Inoperative" causing "Hang-up Error" interrupt.

Error 2

OP Locked True

Result

Timed disconnect occurs

Line 4 - Device ClockError

Failure of clock signals

Result

This condition is interlocked with M/D A line causing a false condition of this line and appropriate disconnect and processor interrupt actions. Timed disconnect occurs if error is not disconnected by other means.

Line 5 - Output Operation Complete (OOC)Error 1

OOC Locked False

Result

Similar to failure to receive EOM or detect end of page. Timed disconnect occurs.

Error 2

OOC Locked True

Result

Processor sends only one character and ceases transmission. Programming implications not determined.

Line 6 - Message/Device Available (M/D A)Error 1

M/D A Locked False

Result

Signifies Device Inoperative to Processor. A "Hang-up Error" interrupt occurs if the processor attempts to output. If this occurs during an output operation, a "console detected error" is indicated causing an attempt at retransmission and consequent "Hang-up Error" interrupt.

Error 2

M/D A Locked True

Result

If this condition exists prior to an output operation, the console is locked in the input mode and a "Hang-up Error" interrupt occurs on attempt to output.

If this occurs during an output operation, a timed disconnect will occur.

2.4.2 Error in Input Operation (IC to DP)

An input operation will consist of either an ET message or a control message transmission from the console to the Data Processor. Parity is checked both at the console and at the Data Processor. The response to error conditions is identical for both ET and control messages.

Parity errors on an input message are detected by the Data Processor at the end of a word on transfer of this word from the I/O register to the DP "M Register". A detected parity error will cause the processor to set the Input Operation line to the false state without sending Input Operation Complete, terminate the input operation and generate an "I/O M Register Error" interrupt. The console will recognize this early termination as a Data Processor detected parity error, switch the M/D A line to the false state and notify the operator that a transmission error has occurred.

Parity errors in an input message detected at the console cause the console generated M/D A line to go false terminating the input operation. Indication of input transmission error is given to the operator and to the program as a "Data Parity Error" interrupt. (The computer recognizes the early termination as an error)

The console is not disconnected immediately on the occurrence of an error interrupt. The program, however, can examine the Input Scanner to determine which console is causing the error, disconnect that console and allow the scanner to proceed to the next device.

The stepping circuits of the scanner are inhibited by the presence of an error condition setting any of the detailed error flip-flops associated with the processor I/O interface. The scanner will continue to select the last device used for input until either the "Ignore Error" flip-flop is set or the detailed error flip-flop is reset by the computer program.

If the input operation does not terminate normally or by a detected error it will be terminated by the processor in 45 to 85 milliseconds, generating an "I/O Hang-up Error" interrupt. Program response to the interrupt can cause the Input scanner to step to the next device, disconnecting the affected console.

Procedure errors in input operations, where not inhibited by functional or electrical interlocks at the console, are detected by the computer program and the console operator notified by a special indicator, and at the discretion of the program, by an ET Display or console printer message.

In general, errors occurring in transmission of ET or control messages terminate the input operation and notify the console operator that an error condition exists. Retransmission of the message is achieved by the operator if desired by repeating the input operation that failed. Persistent failure to achieve a successful input transmission indicates console or DP interface failure requiring maintenance.

2.4.2.1 Control Line Errors

The control lines relevant to an input operation may fail in either a false or a true state at either the console or the Data Processor. Where necessary to prevent I/O interface hang-up, the controlling levels are functionally or electrically interlocked. A summary of the effects of control line failures on an input operation is given below.

Line 1 - Input/Output Operation (I/O OP)

Error 1

I/O OP Locked in False State

Result

Timed disconnect occurs

Error 2

I/O OP Locked True

Result

Not fully determined

Line 2 - Input Operation Complete (IOC)

Error 1

IOC Locked False

Result

This condition causes action similar to "Computer Detected Error" at the console causing the M/D A line to go false. Transmission is terminated normally and error condition indicated to the operator.

Error 2

IOC Locked True

Result

This will cause early termination of the input operation and causes a processor detected "Data Parity Error" interrupt.

Line 3 - Output Priority (OP)Error 1

OP Locked False

Result

No significant effect on input operation unless true at processor end. If true at processor end, a "Hang-up Error" interrupt will occur if an Output operation is attempted.

Error 2

OP Locked True

Result

Inhibits input operation. No hang-up of I/O interface will occur.

Line 4 - Device ClockError

Locked True or False

Result

A timed disconnect will occur generating a "Hang-up Error" interrupt.

Line 5 - Input DataError

Locked True or False

Result

Because of normal NRZ operation of this line, false condition will transmit all zeros. Parity error detection will halt transmission and signal console operator. If locked true, all ones will be transmitted and a timed disconnect will occur freeing the interface.

Line 6 - Message/Device Available (M/D A)Error 1

M/D A Locked in False State

Result

No input operation can be initiated. Console is in the "Device Inoperative" state.

Error 2

M/D A Locked in True State

Result

The console will be in continuous input mode because of priority of Input mode over Output mode. A timed disconnect will occur generating a "Hang-up Error" interrupt.

2.5 Summary of Console Key Functions Providing Inputs to the Data Processor Via the ET and Control Interface

The following console keys transmit control messages or control characters plus ET messages from the console to the Data Processor. The functions to be performed by these keys will be fully described in technical memoranda pertaining to the design of the integrated console. A number of spare keys and spare codes will exist on the console to accommodate a reasonable number of additions.

2.5.1 The following keys generate and insert a unique control character in the ET message header and initiate transmission of the combined ET message to the processor. Subsequent action is initiated and carried out by the DPSS program. The control character includes designation of the ET display page being viewed at the time of transmission.

<u>Name</u>	<u>Function</u>
1. ENTER	Enter ET page
2. LINE PRINTER	Enter ET page and print entire related message on line printer.
3. CONSOLE PRINTER	Enter ET page and print displayed page on console printer.
4. NEXT PAGE	Enter ET page, clear ET display and display next page in sequence.
5. PREVIOUS PAGE	Enter ET page, clear ET display and display previous page in sequence.
6. STORE MESSAGE	Enter ET page and store total related message in location designated in header.
7. ROUTE MESSAGE (TENTATIVE)	Enter ET page and route related message to destination indicated in header.

2.5.2 The following keys generate and insert unique codes for the control character and the third character of a control message, and initiate transfer of a four character control message to the processor. The second and fourth characters of these control messages are "ZERO" and EOM respectively. The control character includes designation of the ET Display page being viewed at the time of transmission.

Name	Function
1. HARD COPY	Initiate M-C display hard copy cycle and notify processor for security logging.
2. PRIORITY/MESSAGE ACCEPT	Clear ET Display and request display of next priority or ET message in queue.
3. ERROR/REPLY ACCEPT	Clear ET Display and request display of next message in "Retrieval" and "Procedure Error" queue.
4. MESSAGE ACCEPT (M-C DISPLAY)	Request display of next M-C display in queue.
5. FORMAT INDEX	Clear ET Display and request display of index of formats.
6. CANCEL OPERATION	Request processor to cancel all operations initiated by this console.

2.5.3 The following keys generate unique codes for the control character and the third character of a control message. The second character in these control messages is a unique code determined by the designator of the overlay in position on the logic keyboard. The fourth character of all control messages is EOM. The control character includes designation of the ET Display page being viewed at the time of transmission.

Name	Function
Start (Overlay)	Start sequence of operations identified by the overlay descriptor; light initial options.
Logic Pushbuttons	Perform operation associated with particular overlay key and overlay descriptor indicated.

Code assignments for the above functions and their location in the appropriate message formats are shown in the message format diagram.

2.6 Summary of Console Indicators Activated by Outputs from the Data Processor Via the ET and Control Interface

2.6.1 The following console indicators are activated by control messages from the Data Processor.

Name	Function
1. PRIORITY/MESSAGE COUNTER	Indicates number of priority and routed messages waiting in queue for transmission to console.
2. "PRIORITY/MESSAGE ACCEPT" P. B. Indicator	Indicates "Priority" messages waiting if top half of dual indicator is flashing red. Indicates non-priority routed messages waiting if only white portion of indicator lit.
3. "ERROR/REPLY ACCEPT" P. B. Indicator	Indicates that "Query" reply or "Procedure Error" message is ready for transmission to console. Dual indicator shows red for "Procedure Error" message, white for "Reply" message.
4. "MESSAGE ACCEPT" P. B. Indicator (M-C)	Indicates that a message is ready for transmission to the console M-C Display.
5. "KEYBOARD ACTIVATE" P. B. Indicator	Indicates OFF, ENABLED and ACTIVE state of ET Keyboard. May be switched between ENABLED state (green) and ACTIVE state (white) by Data Processor Control message as well as by operator action.
6. "START"	Indicates initial condition of Logic Key operation or option to restart under control of processor or operator.
7. LOGIC KEYS	Indicate permissible options in Logic Keyboard overlay sequence

All control pushbuttons, logic keys and local function keys with the exception of power switches, error indicator P. B.'s and miscellaneous test or adjustment controls are disabled during transmission of a message from the console to the DPSS and, if the transmission is successful, remain disabled until the DPSS sends an appropriate enabling control message. These control keys and pushbuttons are also disabled during transmission of messages from the DPSS to the console and when the console is in the "STANDBY" condition.

2.6.2 The following ET indicators are activated by control line conditions in the ET and control portion of the console interface or by internal console action related to data transfers.

<u>Name</u>	<u>Function</u>
OUT OF ORDER	Indicates detected error in transmission from processor to console
RE-ENTER	Indicates detected error in transmission from console to processor

The names assigned for the above keys and indicators are subject to change although the functions are as indicated.

2.7 Character Codes and Symbol Set

(See Appendix A)

2.8 Physical and Electrical Interface

The electrical characteristics of the signals in the ET and Control interface are as follows:

- A logical "True" level (1) is represented by 8.5 ± 2.5 Volts
- A logical "False" level (0) is represented by 0 ± 1.0 Volts
- Rise and fall times on all signals will be between 0.1 and 0.3 microseconds.

The input impedance presented to a line by the receiving device shall be 75 ohms $\pm$ 10% for either logical level. The driving or output impedance is not specified; provision should be made to add a 75 ohm resistor if it is required for termination purposes.

75 ohm coaxial cable with a capacity no greater than 23 picofarads/foot will be used for all data and control lines between the console and the processor. Cable lengths have not yet been determined.

Detailed electrical and physical characteristics are to be determined and specified in the detailed subsystem interface specification.

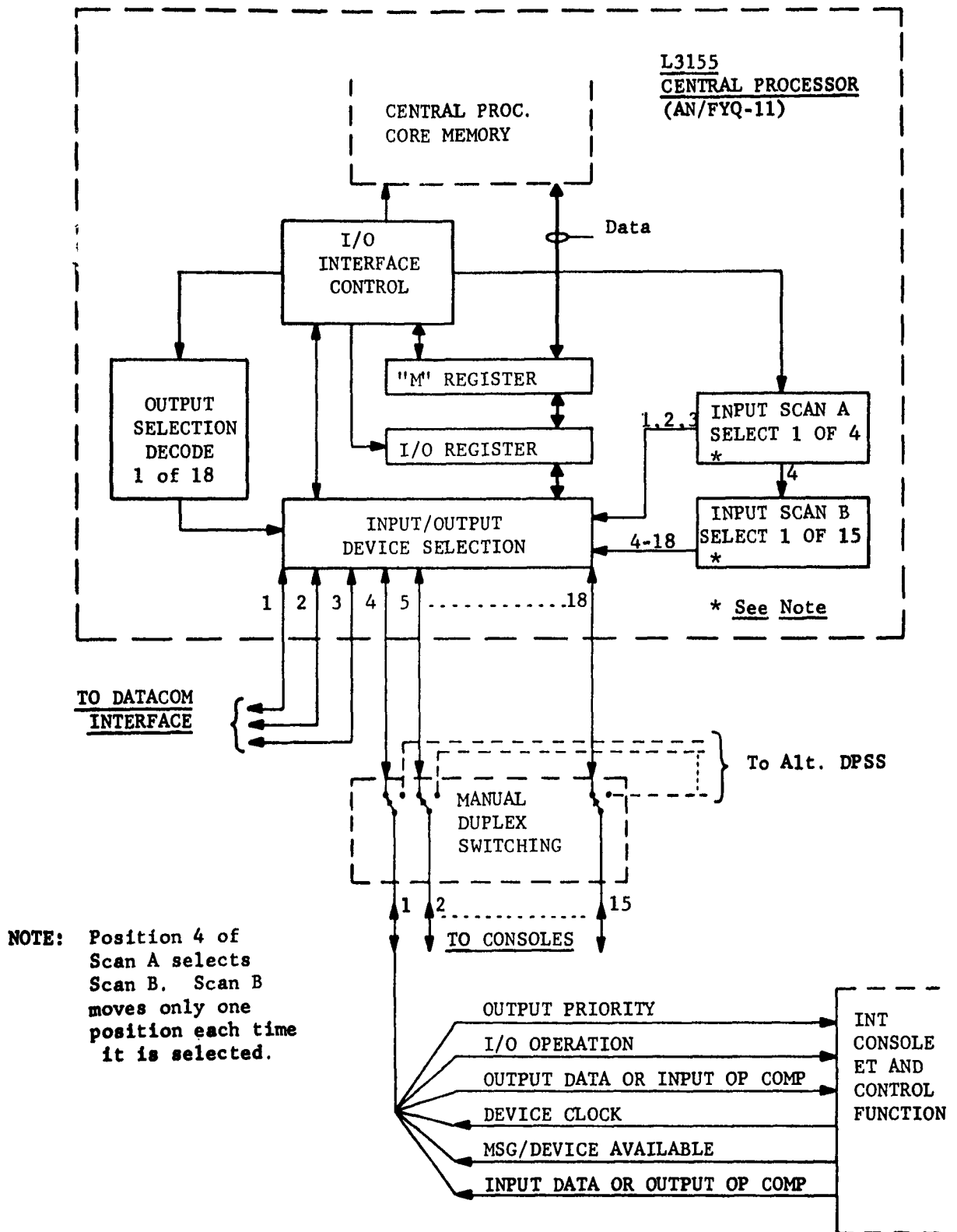
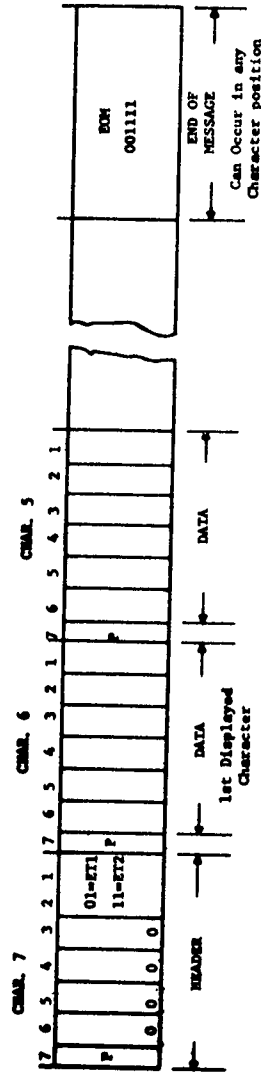
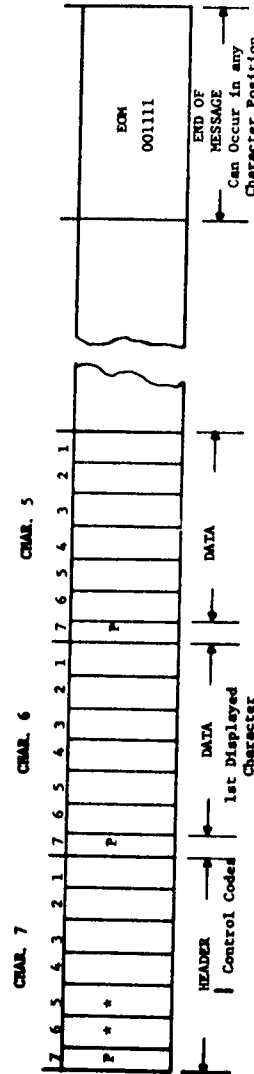


Fig. 2 ET AND CONTROL INPUT/OUTPUT INTERFACE



ET TO ET MESSAGE



ET TO ET MESSAGE

Data is transmitted serially with least significant bit of most significant character first. (i.e., Bit 1, Ch. 7) Each subsequent character is transmitted least significant bit first.

* Bits 5 and 6 of Char. 7 indicate which ET Display page is selected at time of transmission

Bit
6 1 5
0 1 = Display 1
1 0 = Display 2
1 1 = Display 3

CONTROL CODES

0000 ENTER
0001 LINE PRINTER
0010 CONSOLE PRINTER
0011 NEXT PAGE
0100 PREVIOUS PAGE
0101 STORE MSG
0110 SPARE
0111 SPARE
1000 SPARE
(1001 1st Control Msg.)
(1111 P.B. Control Msg.)

Fig. 3

DATA FORMATS - ET/ETSS INTERFACE

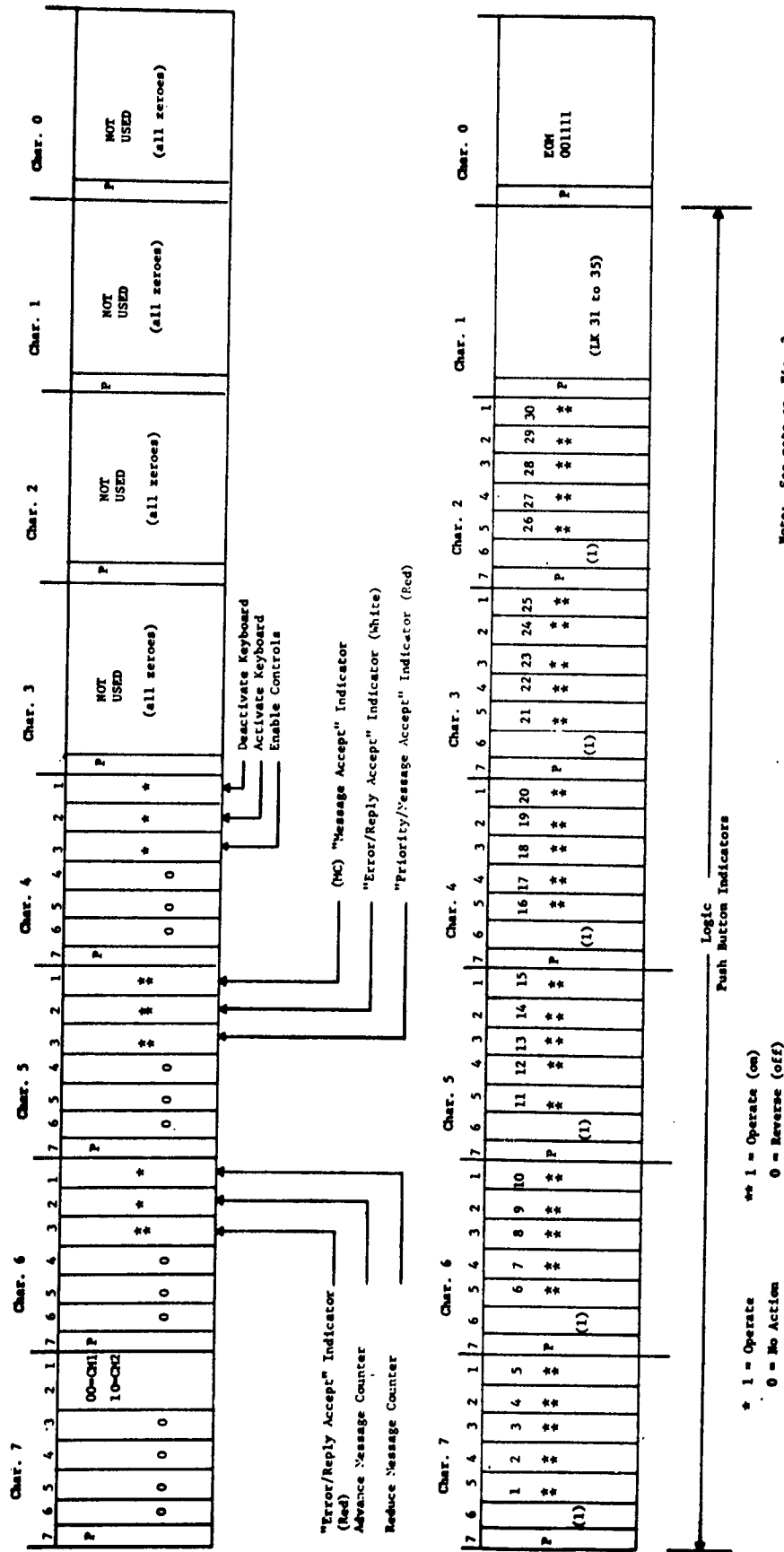
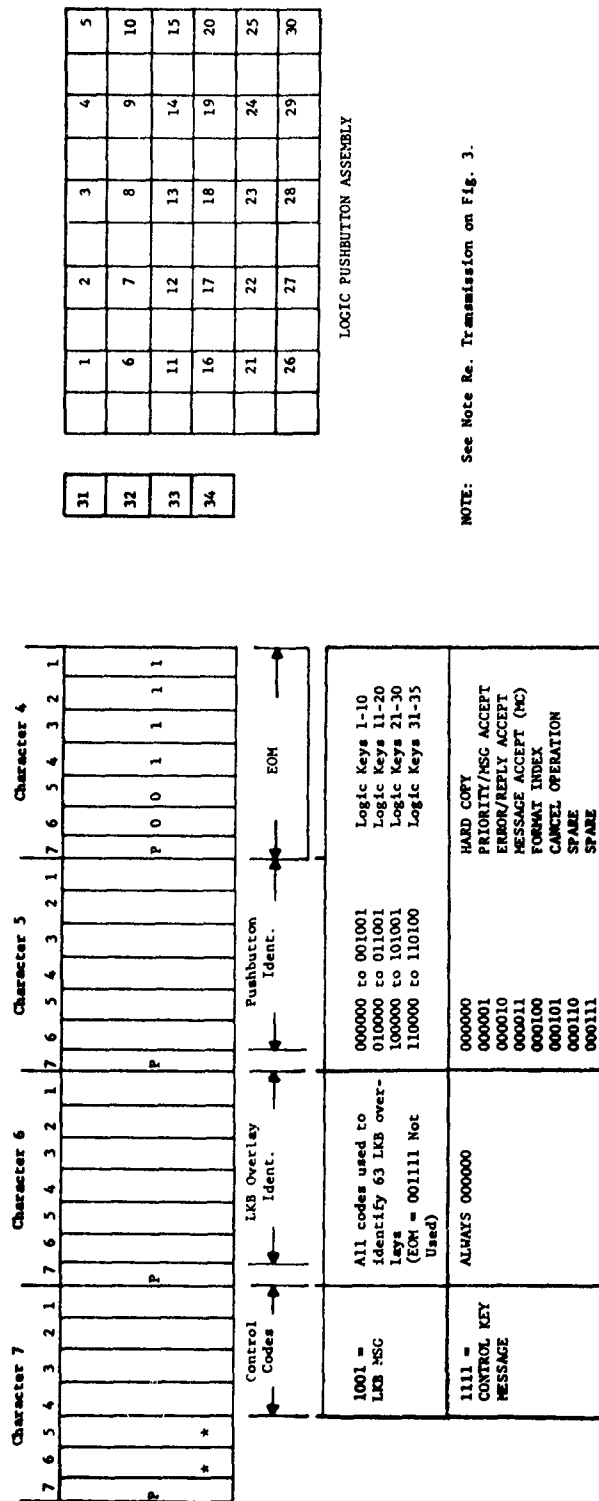


Fig. 4a CONTROL MESSAGE FORMAT DP TO IC



NOTE: See Note Re. Transmission on Fig. 3.

Fig. 4b

CONTROL MESSAGE FORMAT IC TO DP

bits 5 and 6 of Char. 7 indicate which ET DISPLAY page is selected at the time of transmission. See Fig. 3

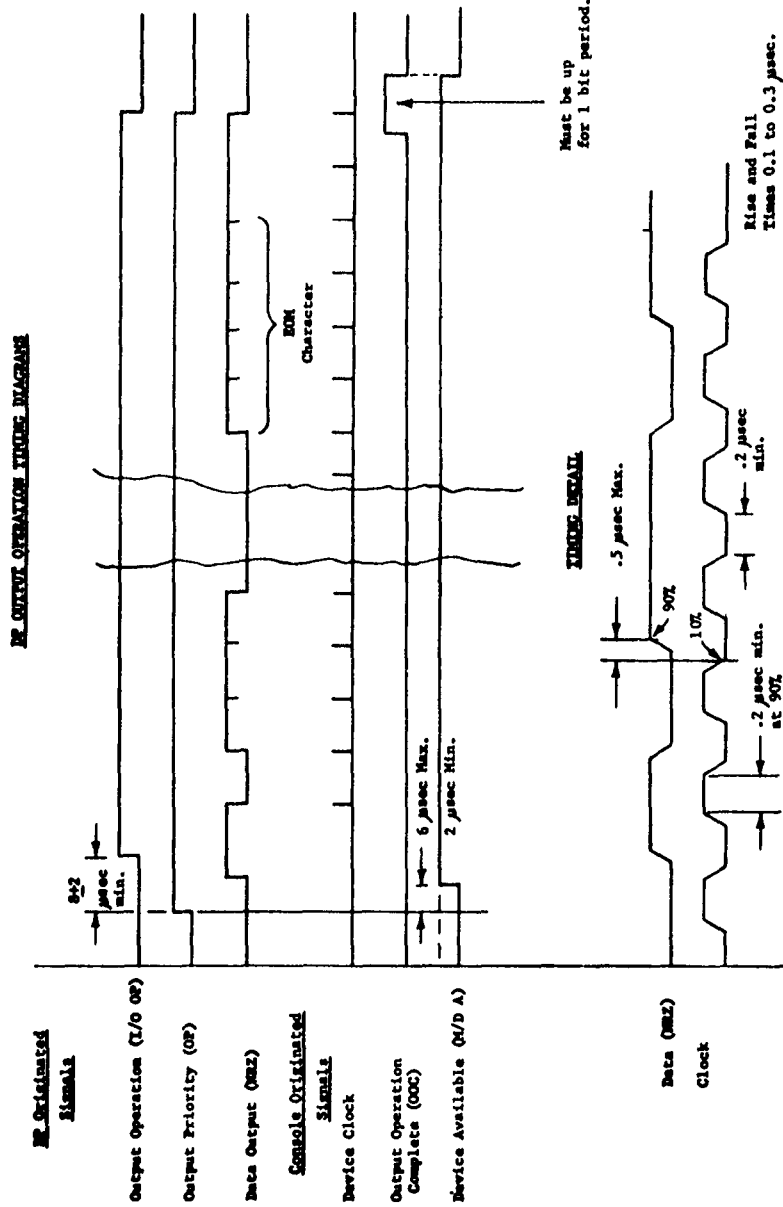


Fig. 3a
TIMING DIAGRAMS
DATA PROCESSOR OUTPUT OPERATION TO RT AND CONTROL

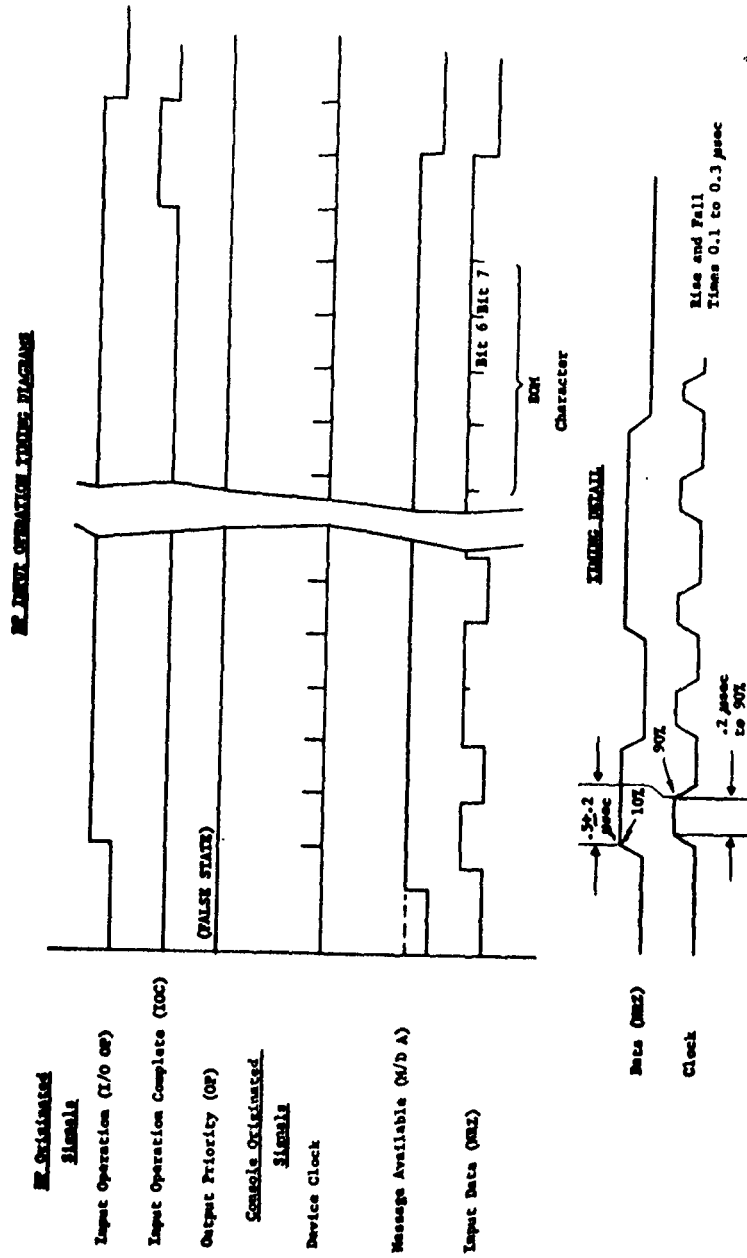


Fig. 5b
TIMING DIAGRAMS
DATA PROCESSOR INPUT OPERATION FROM INTEGRATED CONSOLE

3.0 MULTI-COLORED DISPLAY INTERFACE (TENTATIVE LARGE PANEL DISPLAY INTERFACE)

Display messages for all M-C and Large Panel displays are output via a portion of the Mass Memory disk file designated as the Mass Memory Buffer Store (MMBS). This MMBS has a capacity of 16,000 words which is shared among fifteen output channels. Eleven of these output channels are assigned for M-C displays while four are reserved for Large Panel Display outputs. Display messages, or portions thereof, sent to the MMBS have destination addresses identifying the appropriate output channels and these messages are automatically routed to the displays connected to these channels at display demand rates. Each output channel contains a circulating register capable of holding two 16-word blocks of a display message and, except during block accesses from the MMBS, providing simultaneous output to all displays.

An outline of the M-C (and LP) display interface is shown in Figure 6.

The MMBS is loaded by the processor under program control by a File Command which initiates the display message output operation. Processor loading of the MMBS is by 16-word block units. Output of data from the MMBS to the circulating registers in the output channels is also by 16-word block units. Outputs to each M-C Display is by word demand from the associated circulating register containing two 16-word blocks of the display message. Transmission of display messages from all output channels can proceed simultaneously and independently except for block accesses to the MMBS which may interfere with one another or may be interfered with by processor loading of the MMBS.

Transmission of a display message to a particular M-C display will continue, subject to word demand signals from the M-C display, until the MMBS is depleted of blocks with the corresponding destination address. This may or may not be the end of the complete display message since the processor may transfer a very long display message into the MMBS in several sections to avoid occupying an excessive amount of the available MMBS storage capacity to service only one display device.

The processor is notified by a special interrupt when the MMBS is depleted of blocks for a particular display. Then, and only then, can additional blocks for that display be entered by the processor into the MMBS.

The end of a display message transmission to a particular M-C display is signified by the occurrence of an EOM character. It is a program requirement that the EOM character, when it occurs, coincide with the depletion of blocks in the MMBS for the associated display. Otherwise, an error condition will occur causing an interrupt to be generated.

3.1 Data Transmission Rate

M-C display data transmission from the MMBS output channel to the display console is by word demand at a maximum rate of approximately 180 words per second. Data transmission in this interface is one way only, no messages from the M-C Display being transmitted to the processor via this route. Control messages for the M-C display are routed through the ET and Control interface.

In most instances the Mass Memory Buffer will supply a word to the M-C Display within a maximum of 5.6 milliseconds after receipt of a word demand signal from the console. Words are transmitted bit serially at a rate of $356 \pm 10\%$ kilobits/sec. as determined by the MMBS clock. The least significant bit of the most significant character is transmitted first as in the ET and control interface.

Each character is processed by the M-C display device in approximately 1 millisecond. Vectors require a maximum of 10 milliseconds. If a character or vector is to be displayed in a color different from that of the preceding transmitted symbol, an additional 100 milliseconds is required by the device in order to effect the color changes.

3.2 M-C Message Formats

M-C messages from the DPSS to the console are of arbitrary length and are terminated by an EOM character. When the EOM character is received by the console, the transmission is terminated and the M-C display image is processed.

The message formats applicable to M-C message transmissions are shown in Figure 7.

Three types of word formats are used in the M-C message, Reference Slide Selection Words, M-C Character Words, and M-C Line Coordinate Words. Each type of word is headed by a control character identifying the word and determining the color of the printed character or line. The remainder of the word identifies the reference slide or contains coordinate and character information.

In order to display a line it is necessary to send two words in sequence to the console, one designating the initial coordinate, the second designating the final coordinate. Color designation is repeated in both control characters. If two different colors are designated, the second color only is recognized and implemented by the M-C display.

The reference slide selection word contains the selected slide number in characters 0, 1 and 2. The first bit of character 2 has numerical weight 256; the 4th bit of character 1 has numerical weight 128, etc. If more than one slide selection command occurs in a message, only the first such command will be honored by the console.

The character designation word contains the designated alpha-numeric character in character 6. X and Y coordinates of the character display position are contained in characters 5, 4, and 3 and characters 2, 1, 0, respectively. X and Y position information is in binary form with bit values as indicated in Figure 7.

Line coordinates are sent in character positions identical to those described above for character coordinates and are also designated in binary form.

3.3 Transmission Mode

The following signal lines are used in transferring information to the M-C display:

- a. "Word Transfer Order" - MMBS originated signal transmitted concurrent with data and clock signals.
- b. "Clock" - MMBS originated clock signal transmitted concurrent with data.
- c. "Data" - MMBS originated data signals. These signals are transmitted in "Non-return to Zero" (NRZ) mode.
- d. "Word Demand" - Console originated signal requesting a word from the MMBS.

3.3.2 Normal Output Operation

Timing diagrams showing the interrelationship of control, clock and data signals for normal output operation are given in Figure 8.

Message transfer to an MC display begins with a File Command. This File Command contains the destination code which chooses an output channel and hence the display to which it is connected. The File Command initiates transfer of a designated number of blocks from core memory into the Mass Memory Buffer Store. The Load Point Register counts in sequence through the block addresses on the disk during transfer and so controls where in the MMBS the blocks are put. An Unload Point Register keeps note of the oldest block not yet transmitted to a display. This cannot be passed by the Load Point Register and loss of information by overwriting is thereby prevented. Should the Load Point Register catch up to the Unload Point Register, a program interrupt occurs.

Concurrent with transfer of data to the MMBS, the first two blocks of the display message are loaded into the designated output channel circulating register. This loading, as well as processor loading of MMBS with the display message, is conditioned by a logical "ONE" (true state) on the WORD DEMAND line from the related M-C display device.

Loading of the designated output channel takes approximately 5.6 milliseconds. After the output channel is loaded and after an access delay of approximately 0.3 milliseconds, the WORD TRANSFER ORDER line is set true and the first word of the display message is transmitted bit serially to the M-C display over the related DATA line. Concurrent with transmission of the data, exactly 56 MMBS originated clock pulses are transmitted to the M-C display over the related CLOCK line. When the full word has been transmitted, the WORD TRANSFER ORDER line is set false.

Successful reception of the transmitted word is acknowledged by the console by setting the WORD DEMAND line false within 4.5 milliseconds after the WORD TRANSFER ORDER line goes false. The WORD DEMAND line must remain false a minimum of 10 microseconds. Transmission of the next word ensues when the WORD DEMAND line is again set true by the console signifying readiness to receive the next word, provided the circulating line has brought the next word into position. If the WORD DEMAND line is set true within 4.5 milliseconds after the end of the previous word transmission, the next word will be transmitted 5.6 milliseconds after the end of the previous word transmission. If a longer delay is encountered in setting the WORD DEMAND line true, transmission of the next word will ensue in corresponding multiples of 5.6 milliseconds after the end of transmission of the previous word. The true state of the WORD TRANSFER ORDER line causing transmission occurs on concurrence of a true state on the WORD DEMAND LINE and proper positioning of data in the output circulating register. Transmission of successive words occurs as above until a full 16-word block is transmitted.

After the first block in the output channel circulating register has been transmitted, transmission of the second block proceeds immediately and simultaneous with output channel accesses to the MMBS to mark the transmitted block obsolete and to transfer the third block of the message to the circulating register. Transmission of the remaining blocks of the message in the MMBS proceeds smoothly in this manner until the MMBS is depleted of blocks for that output channel except for occasional possible interference in accessing the MMBS caused by loading of the MMBS by the processor or by accesses by other output channels.

When the last word of the last block in the MMBS for any output channel has been sent, the related M-C display will acknowledge receipt as above. The output channel will access this block in the MMBS, mark it obsolete and cease transmitting. As soon as the Processor-Mass Memory interconnection allows a "Display" interrupt is generated signifying depletion of the MMBS or data blocks for that channel.

If the last word transmitted was not an EOM, the MC display will request further transmission by setting the WORD DEMAND line true as above. This will allow the processor program to load a continuation of the display message into the MMBS and further transmission ensues as above.

If the last word transmitted is an EOM, the M-C will keep the WORD DEMAND line false until it is ready to receive subsequent messages.

Whenever a message transmission is completed, either successfully or through an abort resulting from error condition, a program interrupt occurs notifying the processor that the transfer is terminated. At this time, the program can determine which output channel (and, hence, which display device) was involved and whether or not the transmission was successful.

Since M-C or LP display messages are of arbitrary length and the 16,000 words of the MMBS are shared among all MC and LP displays it may not be possible to insert a full M-C or LP display message in the MMBS at one time. If this occurs, as many blocks of the message are transferred from the processor to the MMBS as there is space available (subject to programming or other procedures or constraints). When the available space is filled, the message transfer is interrupted until all of the blocks of data in the MMBS for that display have been transmitted. The processor may then again access the MMBS under program control and transfer more of the message. During this access and transfer from the processor to the MMBS, output from the affected channel to the display is halted and resumed only when the rest of the message or the maximum number of blocks available for that display in the MMBS have been filled.

The Processor can test the status of each output channel to determine whether it is transmitting or not, whether the non-transmitting state resulted from a successful transmission of all blocks available in the MMBS for a particular channel or from an abort condition and whether an operative display device is present on a given output channel as indicated by the true state of the related WORD DEMAND line. The processor can then determine in response to interrupt which channels are ready for loading, which have completed message transmission and which have aborted or are not available through inoperative condition of the channel or the connected device.

3.4 Error Considerations

3.4.1 Data Transfer Errors

Parity is checked at the MC display for each word transmitted. If a parity error is detected by the M-C display, receipt of the word is not acknowledged and the WORD DEMAND line is held true for at least 4.5 milliseconds after the WORD TRANSFER ORDER line is set false. The output channel will respond to this error indication by retransmitting the incorrectly received word, approximately 5.6 milliseconds after the end of the previous transmission. If this transmission is received correctly, normal transmission of subsequent words ensues. If, however, a parity error is again detected on the retransmitted word, a third attempt at transmission is made as above. If an error is detected in the third transmission attempt, the M-C display will

signal detection of the error as above by holding the WORD DEMAND LINE true. The WORD TRANSFER ORDER line will go true again within 5.6 milliseconds and will remain true for the normal duration of word transmission though data will not be transmitted. This will signify to the console that the MC display message is aborted. The MMBS at this time will stop sending the display message, mark all blocks of the message remaining in the MMBS obsolete and signal the program with a "Display" interrupt that the transmission is terminated and an error has occurred in transmission to that particular console. The fact that transmission has failed due to three successive parity errors on a given word is indicated to the console operator by means of an "M-C ERROR" indicator. The M-C display device will at this time abort the portion of the message already processed and ready itself to receive the next M-C display message.

If the WORD DEMAND line, after acknowledging a successful word transmission, fails to demand the next word within 3.0 ± 1 seconds after acknowledgment of the previous word due to turn-off of the device before complete transmission, erroneous interpretation of a character as EOM or for any other reason, the transmission will be aborted as above. The timer causing this abort is located in the MMBS portion of the interface and an individual timer is provided for each of the 15 output channels.

3.4.2 Control Line Errors

Any of the control, clock or data lines may fail in either the false or the true states. A general system requirement exists to ensure that no persistent malfunction of a particular M-C or LP display or its corresponding MMBS output channel will cause serious degradation of outputs capability to other M-C or LP displays. Such degradation could occur if a substantial portion of the MMBS was occupied by a particular display message which is neither transmitted nor aborted due to undetected malfunction of the related output channel or display device. The effect would be to reduce the space available in the MMBS for all other display messages and adversely affect service time for all other M-C and LP displays.

In general, timing devices or functional interlocking of clock, signal and control lines are used where feasible to minimize system degradation on single output channel or display device malfunctions.

A summary of the effects of data, clock, and control lines follows. The assumption is made that only one failure will occur at a time in a given display device interface.

Line 1 - WORD TRANSFER ORDER

If the WORD TRANSFER ORDER line fails in either the false or the true state, the display device will not acknowledge receipt of the transmitted word and the sequence described for repeated parity errors will occur ultimately causing abort of the message.

Line 2 - CLOCK

Same effect as failure of WORD TRANSFER ORDER line results for CLOCK failure in false or true state.

Line 3 - DATA

If the DATA line fails in the false state, all zeroes will be transmitted causing parity error detection and abort of transmission after third unsuccessful transmission try.

If the DATA line fails in the true state, all ones will be transmitted and transmission will continue until the entire message is sent unless the display device recognizes this condition and causes an abort via control of the WORD DEMAND line. It is expected that bit number 6 of Character 5 of each M-C (or LP) display word will be always designated as zero and checked by the display device to ensure that the DATA line is not failed in the true state. Detection of "ONE'S" in all three bit positions will cause the device to initiate "abort" procedures.

Line 4 - WORD DEMAND

If the WORD DEMAND line fails in the true state, the effect will be the same as for repeated parity errors and the message will abort on the third transmission try.

If the WORD DEMAND line is failed in the false state prior to transfer of a display message to the MMBS, the transfer will not take place since Processor test of output channel status will indicate no operative display device present for that channel.

If WORD DEMAND fails false after the MMBS has been loaded and before the first word is transmitted. the related display message will abort.

If WORD DEMAND fails false after acknowledging successful transmission of one or more words, it will fail to demand the next word and the transmission will abort within 3.0 ± 1 seconds after the end of the acknowledged word transmission.

3.5 Character Codes and Symbol Set

See Appendix A.

3.6 Physical and Electrical Interface

The electrical characteristics of the signals in the M-C display interface are as follows:

- A Logical "True" Level (1) is represented by -8.5 ± 2.5 Volts.
- A Logical "False" Level (0) is represented by 0 ± 1.0 Volts.
- Rise and Fall times on signals from the MMBS to the MC Display will be between 0.1 and 0.3 microseconds.

- Rise and Fall times on signals from the M-C display to the MMBS will be between 0.1 and 3.0 microseconds.

The input impedance presented to a line by the receiving device will be 75 ohms $\pm$ 10% for either logical level. The driving or output impedance is not specified. However, provision will be made to add a 75 ohm resistor at the Line Driver if it is required for termination purposes.

75 ohm coaxial cable with capacity no greater than 20 picofarads per foot will be used for all data and control lines between the console and the MMBS. Cable lengths have not yet been determined.

Detailed electrical and physical characteristics are to be provided in the interface specification.

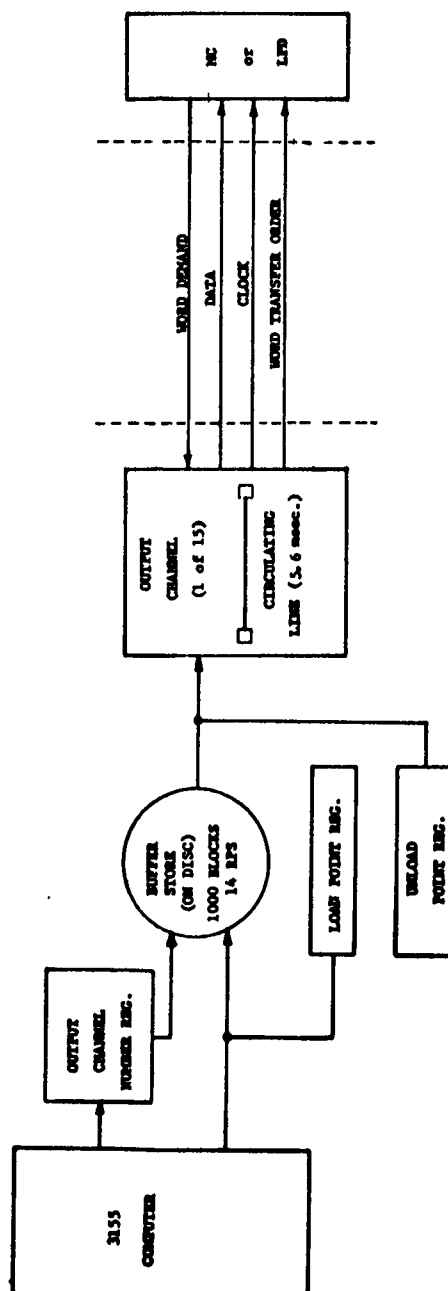
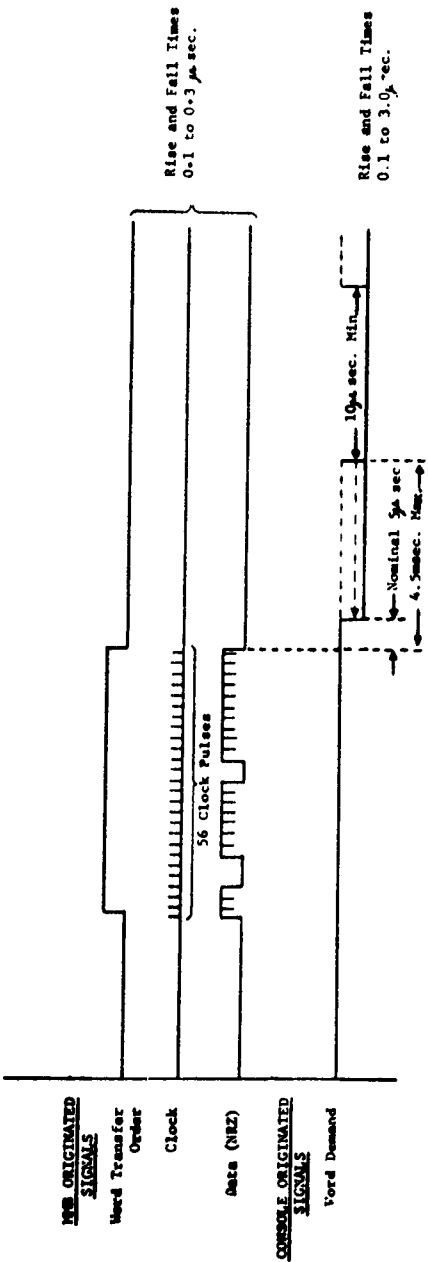
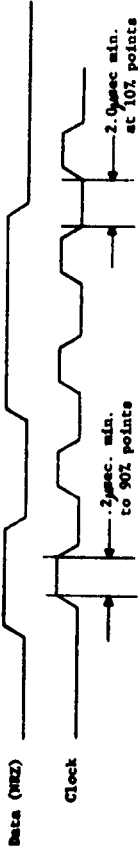


Fig. 6
MC (and LFD)
OUTPUT INTERFACE



TIMING DETAIL



Center of Clocks Must be Concurrent With the Center of the Data to Within 0.5µ sec.

Fig. 8
TIMING DIAGRAMS
DATA PROCESSOR OUTPUT OPERATION TO M-C DISPLAY

4.0 HARD COPY ASSEMBLY INTERFACE

No data or control transmission exists between the DPSS and the M-C display hard copy assembly. Request for a hard copy reproduction of the M-C display is initiated through depression of the "Hard Copy" control key. This key generates and transmits a 4 character control message to the Data Processor via the ET and Control Interface notifying the processor, for logging purposes, that a copy of the M-C display is being made.

Once this control message has been successfully transmitted, the M-C display reproduction cycle is initiated locally at the console.

Controls internal to the console insure that no change occurs to the M-C display for which a reproduction is requested until critical portions of the reproduction cycle are completed or until the request is aborted as a result of failure to successfully transmit the Hard Copy control message to the Data Processor.

5.0 CONSOLE PRINTER INTERFACE

Transmission of messages to a Console Printer (CP) may be initiated independently by the Data Processor or in response to a control message request received by the Processor via the ET and Control interface. In all instances, however, CP messages are output by the Data Processor via the Mass Memory Console Printer Store (MMCPs).

The MMCPs is an integral part of the Mass Memory unit and contains 15 regions of disk storage each with a nominal capacity of 1024 characters. Actual storage capacity of each region is 1110 characters. Transfer of data from the Processor to the MMCPs, however, is by block where each block contains 1024 characters.

Each MMCPs region is uniquely associated with one of 15 Console Printer output channels. All 15 CP output channels are capable of independent simultaneous output. Output channel accesses to the MMCPs are by character, each channel holding one character at a time until it is accepted by the associated console printer.

Data Processor loading of the MMCPs is initiated by a File Command containing the address of the region to be loaded and hence the Console Printer with which it is associated. The program may precede the transmission with a test of the system duplex switching to ensure that a console printer is switched to the addressed channel.

Once a full or partial message block is loaded into the MMCPs and a character is available in the relevant output channel, transmission will proceed subject to character demand by the associated Console Printer. Transmission continues on a character-by-character basis until the MMCPs region is depleted of characters or an EOM character is detected signifying end of message. In either case the processor is notified of the termination of transmission by a "Display" interrupt occurring at the end of whatever file operation was in process and coincident with the "End of File Operation" program interrupt. The program at this time can determine by test which console printer channels are no longer transmitting and consequently which MMCPs regions are ready to be reloaded with a subsequent block (or, partial block) of the output message or with the first block of a new message.

If the processor attempts to output data to an MMCPs region still involved in transmission or to which an "unavailable" console printer is connected, the data will not be transferred and a "Display" interrupt will occur. (The "unavailable" condition of the Console Printer is signified by a false state of the associated "Character Demand" line at the time of the attempted output operation).

The program may test at any time to determine the transmitting/non-transmitting status of each Console Printer output channel. "Unavailable" status however, as defined above, cannot be determined meaningfully by test prior to attempted output since determination of this state requires

program interpretation of receipt of a "Display" interrupt in response to the output attempt together with the "non-transmitting" status of the relevant output channel as determined by test.

5.1 Data Transmission Rate

Data is transmitted from the CP Buffer to the Console by character demand. Each character is represented by levels on seven parallel lines (6 bits + parity) and transmitted sequentially in response to Character Demand signals transmitted by the Console Printer. The nominal rate of demand is 14 characters per second.

5.2 Message Format

With the exception of insertion of "Line Advance/Carriage Return" and EOM codes in appropriate places in the printer message, no particular format restrictions exist. If the "Line Advance/Carriage Return" codes are omitted, the printer will automatically perform this function at the end of each printer line. Messages may be of any arbitrary length subject only to programmed limitations which may arise as a consequence of the relatively slow rate of output via the console printer.

5.3 Transmission Mode

5.3.1 Data and Control Lines

Transmission from the Mass Memory Buffer to the console printer is effected through utilization of the following signal and control lines.

Lines 1 to 7 - Data Lines

Six lines carry levels identifying the character transmitted. The seventh line level indicates odd parity for the character.

Line 8 - CHARACTER AVAILABLE

This line is set true by the MMCPs whenever a character exists on the Data Lines.

Line 9 - CHARACTER DEMAND

This line is set true by the console printer to indicate readiness to receive the next character. The line will be false while the printer is printing the last received character or if the Console Printer is off or in "Not Available" condition.

5.3.2 Normal Output Operation

The MMCPs region associated with a particular Console Printer output channel is loaded with the first block (or partial block) of an output message under program control and subject to the availability

of that channel for transmission. Data transfer from the Processor to the MMCPs is initiated by a File Command specifying the region to be loaded. Data transferred in one operation is limited to one block = 1024 characters. When this data transfer to the MMCPs is completed, the processor is signaled by means of a "File Not Busy" interrupt.

After the MMCPs region is loaded and when the first character is present on the output channel data lines, the "Character Available" line level is set true. The related Console Printer "Character Demand" line will normally be true at this time and the Console Printer will sense the available character and commence the print cycle.

As soon as the Console Printer has adequately sensed the transmitted character, it will set the Character Demand line false for at least 4 microseconds. The Character Demand line will be returned to the true state as soon as the Console Printer is ready to accept the next character of the message.

When the Character Demand line is set false as above, the output channel will set the Character Available line false within 4 microseconds and begin access of the MMCPs to obtain the next character. This access may take from 4 microseconds to 70 milliseconds depending on the position of the related MMCPs region on the storage disk relative to the readout position.

Once the next character has been accessed and is present on the output data lines, the Character Available line is again set true. Transmission will ensue immediately if the Character Demand line is true at that time or will occur when the Character Demand line becomes true.

Transmission will continue as above on a character-by-character basis until all 1024 characters in the MMCPs region are transmitted or until an EOM character is detected. Either condition will cause transmission to be halted and cause a "Display" interrupt to be generated at the end of whatever File operation was in progress and coincident with the "End of File Operation" interrupt.

The processor may, at this time, test the status of all Console Printer output channels and, if allowed, commence transfer of additional blocks of data into appropriate MMCPs regions.

5.4 Error Consideration

5.4.1 Data Transfer Errors

The "transmitting" or "non-transmitting" status of each Console Printer output channel is indicated to the Processor by program test of a Display Status word. The program would ordinarily precede an attempt to load a particular region of the MMCPs with a test to ensure that the related output channel is in the "non-transmitting" state. If, however, an attempt is made to load MMCPs region where channel is in "Transmitting" status, a "Display" interrupt is generated and the loading attempt is blocked.

"Unavailable" status of the Console Printer channel is indicated to the MMCPs by a "false" level on the Character Demand line but does not directly affect the Display status word. An attempt by the processor to load an "unavailable" region of the MMCPs will cause a "Display" interrupt. Occurrence of the Display interrupt in conjunction with "non-transmitting" status of the output channel may be interpreted by the program as "unavailable" status.

The Console Printer checks parity on each incoming character. Detection of a parity error does not affect the transmission but causes a special symbol (■) to be printed in place of the character received in error. Detection of a parity error also causes a "PRINTER ERROR" indicator on the Console Printer to be lit and remain lit until manually reset. Parity error detection and indication is strictly a local function of the Console Printer, no information concerning detected parity errors being fed back to the Data Processor or the MMCPs output channel.

5.4.2 Control and Data Line Failures

Any of the Control or Data lines may fail in either the false or true state. Since failures affecting a particular Console Printer output channel will not significantly affect outputs to other channels no serious degradation of the system will result. Consequently, no elaborate interlocks or automatic disconnects are required.

5.4.2.1 Data Line Failures

Failure of any one of the Data lines, including the Parity line, in either false or true state will result in multiple parity error printouts and garbled copy easily identified by the console operator as a faulty condition and indicating the need for maintenance.

5.4.2.2 Control Line Failures

Character Demand Line - If a Character Demand line fails in the true state, either before or during transmission, data transfer from the Processor to the MMCPs will take place without interrupt (at least for the first block transferred) but only one character will be transmitted to the Console Printer and transmission will cease. The affected channel will remain in the "transmitting" state. Program testing of the Display Status word prior to subsequent output attempts will indicate "transmitting" status of this channel and the output attempt may be deferred. No explicit indication of this fault condition is given to the Processor or to the Console Operator.

Failure of a Character Demand line in the false state will, if it occurs prior to an attempt by the processor to output a message, indicate "unavailable" status of the affected output channel to the processor by means of a "Display" interrupt occurring when an attempt is made to load the affected region of the MMCPs.

Since "unavailable" status may be a normal state, no explicit indication of "fault" condition is given to the Processor or to the Console operator.

If a Character Demand line fails false after the related MMCPs has been loaded, transmission to the console printer will cease. The affected output channel will remain in the "transmitting" state. Program test of the Display status word prior to a subsequent output attempt will indicate "transmitting" status of this channel and cause further loading of the MMCPs region to be deferred.

No explicit indication of this fault condition is given to either the console operator or the Data Processor.

Character Available Line Failure

Failure of the Character Available line is either the false or true state will exhibit transmission of data from the MMCPs to the Console Printer but will not directly affect transfer of data from the Processor to the MMCPs. After the related MMCPs region is loaded, however, it will remain in the "transmitting" state. Program test of the Display status word will indicate "transmitting" status for the affected channel and the attempt to load the MMCPs region may be deferred.

No explicit indication of this fault condition is given either to the Processor or to the Console Printer operator.

5.5 Character Codes and Symbol Set

See Appendix A.

Two of the assigned codes are interpreted by the printer as instructions for mechanism action other than printing. These are:

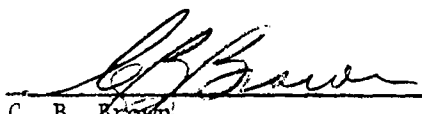
(a) EOM- prints EOM symbol, causes paper to be advanced to permit operator viewing of the received message and left justifies the printer "carriage".

(b) Lower Case Code - Advances paper one line and returns carriage to left hand margin.

5.6 Physical and Electrical Characteristics

Cable type, input and output impedances, True and False levels and Rise times are as described for the M-C interface.

Detailed electrical and physical characteristics are included in the detailed interface specifications.


C. B. Brown

CBB:vanl

Attachments: Appendix A, Appendix B, Appendix C
Distribution List

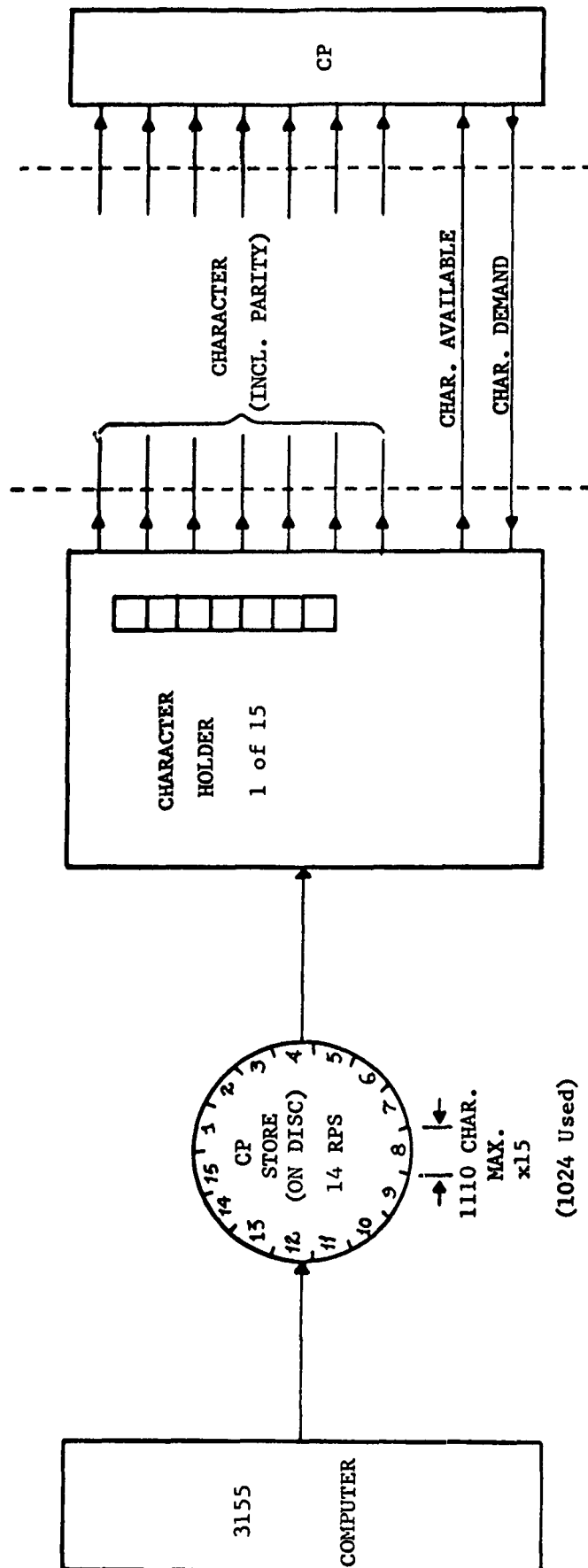


Fig. 9
CP OUTPUT
INTERFACE

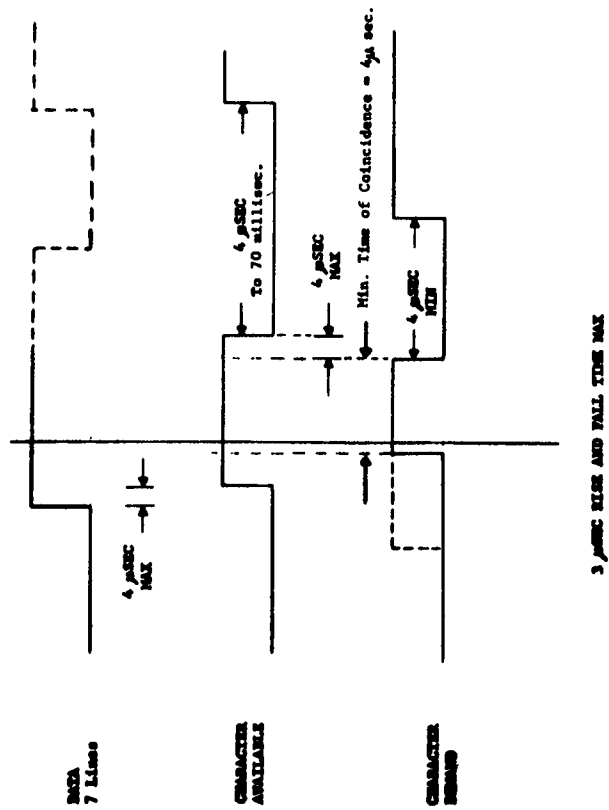


Fig. 10
SIGNAL CHARACTERISTICS
DATA PROCESSOR TO CONSOLE PRINTER

APPENDIX A

473L EQUIPMENT CHARACTER SET

Appendix A

473L EQUIPMENT CHARACTER SET

The following is an updated list of symbols to be used in the 473L System. The Console Printer and the ET Display have an extra symbol, not shown in the list, that will not have an associated code but will be generated and displayed when a parity error is detected on an incoming message. This symbol (■) will be printed instead of the erroneous character received by the Console Printer and will be presented as a flashing symbol in place of erroneous character received by the ET Display.

473L EQUIPMENT CHARACTER SET

L-3055 Code 7 65 4321	Line Printer & Typewriter Characters	(1) Field Data Characters	Integrated Con- sole Characters (Includes ET, CP, MC)	(3) Card Reader/ Punch Row(s)
1 11 0000	(Blank)	(Space)	(Blank)	(Blank)
0 11 0001	A	A	A	12-1
0 11 0010	B	B	B	12-2
1 11 0011	C	C	C	12-3
0 11 0100	D	D	D	12-4
1 11 0101	E	E	E	12-5
1 11 0110	F	F	F	12-6
0 10 0111	G	G	G	12-7
0 11 1000	H	H	H	12-8
1 11 1001	I	I	I	12-9
1 11 1010	)	)	)	12-8-4
0 11 1011	. (Period)	.	.	12-8-3
1 11 1100	(2) □	BELL	□	11-8-2
0 11 1101	(2) (Underline)	OWD	(Underline)	12-8-6
0 11 1110	(2) ≠	!	≠	11-8-5
1 11 1111	(2) ?	?	?	12-8-7
0 10 0000	: (Colon)	:	:	12-8-5
1 10 0001	J	J	J	11-1
1 10 0010	K	K	K	11-2
0 10 0011	L	L	L	11-3

L-3055 Code 7 65 4321			Line Printer & Typewriter Characters	(1) Field Data Characters	Integrated Con- sole Characters (Includes ET, CP, MC)	(3) Card Reader/ Punch Row(s)
1	10	0100	M	M	M	11-4
0	10	0101	N	N	N	11-5
0	10	0110	O	O	O	11-6
1	10	0111	P	P	P	11-7
1	10	1000	Q	Q	Q	11-8
0	10	1001	R	R	R	11-9
0	10	1010	(Minus)	(Minus)	(Minus)	11
1	10	1011	*	*	*	11-8-4
0	10	1100	(2) ^ (Up)	(Upper Case)	^	11-8-7
1	10	1101	(2) \$	\$	\$	11-8-3
1	10	1110	(2) (Down)	(Lower Case)	See note 4	12-8-2
0	10	1111	(2) ♦	&	♦	0-8-5
0	01	0000	+	"(Quote)	+	12
1	01	0001	/	/	/	0-1
1	01	0010	S	S	S	0-2
0	01	0011	T	T	T	0-3
1	01	0100	U	U	U	0-4
0	01	0101	V	V	V	0-5
0	01	0110	W	W	W	0-6
1	01	0111	X	X	X	0-7
1	01	1000	Y	Y	Y	0-8
0	01	1001	Z	Z	Z	0-9
0	01	1010	(	(	(	0-8-4
1	01	1011	(Comma)	(Comma)	(Comma)	0-8-3
0	01	1100	(2) #	#	#	0-8-2
1	01	1101	(2) ° (Degree)	° (Degree)	° (Degree)	6-8
1	01	1110	(2) ;	;	;	11-8-6
0	01	1111	(2) [	(line Feed)	[	0-8-7
1	00	0000	0	0	0	0
0	00	0001	1	1	1	1
0	00	0010	2	2	2	2
1	00	0011	3	3	3	3
0	00	0100	4	4	4	4
1	00	0101	5	5	5	5
1	00	0110	6	6	6	6
0	00	0111	7	7	7	7

L-3055 Code	Line Printer & Typewriter Characters	(1) Field Data Characters	Integrated Con- sole Characters (Includes ET, CP, MC)	(3) Card Reader/ Punch
7 65 4321				
0 00 1000	8	8	8	8
1 00 1001	9	9	9	9
1 00 1010	=	%	=	8-3
0 00 1011	(Apostrophe)	(Apostrophe)	(Apostrophe)	8-4
1 00 1100	(2)>	>	>	8-2
0 00 1101	(2)<	>	<	8-5
0 00 1110	(2)]	(Carriage Return)	]	0-8-6
1 00 1111	(2)(EOM)	(Master Space)	EOM	8-7

- NOTES: (1) As translated by the L-119 Buffer Processor
- (2) Low speed print characters (Line Printer)
- (3) This code is compatible with IBM 026 Type-H print set
- (4) This code when received by the ET or CP will cause the cursor or writing mechanism to space down one line and over to the extreme left. When received by the MC, the solid box is generated (■).

APPENDIX B

LIBRASCOPE SPECIFICATION

L190 000 832

Preliminary specification of L3155 Central
Processor Input/Output Interface with the
ET and Control portions of the ICSS (and
with the L119 Buffer Processors.)

1.0 SCOPE

- 1.1 The Central Processor Input-Output Interface provides the path for information transfer between the L-3155 Central Processor and the L-119 Buffer-Processor and the ET portion of the ICSS. The interface characteristics, both functional and electrical requirements, are defined by this specification.

2.0 LANGUAGE AND WORD

- 2.1 An L-3155 Central Processor character consists of six data bits and one odd parity bit. The code used in the L-3155 is given in Appendix A.
- 2.2 Eight characters constitute one word.
- 2.3 An input message is defined as any sequence of characters transmitted from the external device to the L-3155 Central Processor bit serially over the input data line. A character will be transmitted least-significant bit first in sequence through the most-significant of the six data bits. Every seventh bit will be the odd parity bit for the six preceding data bits.
- 2.4 An output message is defined as any sequence of characters transmitted from the L-3155 Central Processor to the external device bit serially over the output data line. A character will be transmitted least-significant bit first in sequence through the most-significant of the six data bits. Every seventh bit transmitted will be the odd parity bit for the six preceding data bits.
- 2.5 Messages, both input and output, will be transported in decreasing order of character significance. A partial-word portion of a message will occupy the most-significant register positions.

3.0 SIGNAL LEVELS AND IMPEDANCE

- 3.1 Signals to External Device.
- 3.1.1 A "true" level (logical one) on the signal lines to the external devices shall be represented by $-8.5V \pm 2.5V$.
- 3.1.2 A "false" level (logical zero) on the signal lines to the external devices shall be represented by $0V \pm 1V$.
- 3.1.3 The signals to the external devices shall be transmitted over 75 ohm coaxial line such as Amphenol 21-597.

CODE IDENT NO.	SIZE		
36090	A	L190 000 832	
SCALE			SHEET 2

- 3.1.4 The input impedance of the external device for any signal line, measured at the device terminals, shall be 75 ohms $\pm$ 10%, to signal ground, for either the true or false levels. This specified impedance shall include any required line termination.
- 3.1.5 The rise and fall times measured between the 10% and 90% points shall be between 0.1 and 0.3 microseconds after transmission through two hundred feet of properly terminated coaxial line.
- 3.2 Signals from External Device.
- 3.2.1 A "true" level (logical one) on the signal lines from the external device shall be represented by -8.5V $\pm$ 2.5V.
- 3.2.2 A "false" level (logical zero) on the signal lines from the external device shall be represented by 0V $\pm$ 1.0V.
- 3.2.3 The signals from the external devices will be transmitted over 75 ohm coaxial line such as Amphenol 21-597.
- 3.2.4 The input impedance at the Central Processor to any signal from the external device will be 75 ohms $\pm$ 10% to signal ground for either the true or the false levels.
- 3.2.5 The rise and fall times measured between the 10% and 90% points shall be between 0.1 and 0.3 microseconds after transmission through two hundred feet of properly terminated coaxial line.
- 3.2.6 Clock pulses will have a minimum duration of 0.2 microseconds as measured between the 90% amplitude points and a minimum separation of 0.2 microseconds as measured between the 10% amplitude points. Concurrent input data bits will be sampled at the trailing edges of the clock pulses and must be 90% established 0.5 $\pm$ 0.2 microseconds before the 10% amplitude point of the false transition of the clock signal. Output data bits will be 90% established 0.5 $\pm$ 0.2 microseconds after the 10% amplitude point of the false transition of the clock signal. The time specifications refer to the L-3155 Central Processor connectors and do not include cable delays.
- 3.3 Transfer Rates.
- 3.3.1 Transfer rate, both input and output, for the L-119, as established by the L-119 clock will be 760,000 $\pm$ 10% bits per second.
- 3.3.2 Transfer rate, both input and output, for the ET portion of the ICSS, as established by the ET clock will be 720,000 $\pm$ 10% bits per second.

CODE IDENT NO.	SIZE	L190 000 832
36090	A	
SCALE		SHEET 3

4.0 INTERFERENCE LIMITS

4.1 Any External Device which interfaces with the L-3155 Central Processor shall meet the interference limits as specified in MIL-I-26600.

5.0 SIGNALS AND DESIGNATIONS - L-119 BUFFER-PROCESSOR AND L-3155 CENTRAL COMPUTER COMMUNICATION

5.1 Signals Required for L-119 Output Operation from L-3155 Central Processor.

5.1.1 Signals from the L-3155 Central Processor to the L-119.

i = Addressed Device

Opl(i) Output Operation ($3 \leq i \leq 5$)

Opo2(i) Output Data ($3 \leq i \leq 5$)

5.1.2 Signals from the L-119 to the L-3155 Central Processor.

Cppl(i) Device Clock ($3 \leq i \leq 5$)

Cpp2(i) Operation Complete ($3 \leq i \leq 5$)

Cpp3(i) Device Available ($3 \leq i \leq 5$)

Cppl(i) Parity Error ($3 \leq i \leq 5$)

5.2 Signals Required for L-119 Input Operation to L-3155 Central Processor.

5.2.1 Signals from the L-3155 Central Processor to the L-119.

j = Addressed Device

Pcol(j) Input Operation ($0 \leq j \leq 2$)

Pcc2(j) Computer Operation Completed ($0 \leq j \leq 2$)

5.2.2 Signals from the L-119 to the L-3155 Central Processor.

Popl(j) Message Available ($0 \leq j \leq 2$)

Pop3(j) Device Clock ($0 \leq j \leq 2$)

Pop4(j) Input Data ($0 \leq j \leq 2$)

CODE IDENT NO.	SIZE		
36090	A	L190 000 832	
SCALE		SHEET	4

5.3 The indices i and j above refer to a specific L-119 connector position on the L-3155 Central Processor console.

6.0 SIGNALS AND DESIGNATIONS - ET PORTION OF THE ICSS AND L-3155 CENTRAL COMPUTER COMMUNICATION

6.1 Signals required for ET Input-Output Operation between the L-3155 Central Processor and ET Portion of the ICSS.

6.1.1 There are six lines providing communications between the ET portion of the ICSS and the L-3155 Central Processor.

6.2 Signal Descriptions.

6.2.1 During output operations, which are specified by a true condition of the Output Priority signal line, designated Cpc3(k), the lines have the following meanings, respectively:

6.2.1.1 Signals from L-3155 to ET:

Cpc3(k)	Output Priority	$(0 \leq k \leq 14)$
Cpc4(k)	Output Data	$(0 \leq k \leq 14)$
Cpc5(k)	Output Operation	$(0 \leq k \leq 14)$

6.2.1.2 Signals from ET to L-3155:

Cpp5(k)	Device Clock	$(0 \leq k \leq 14)$
Cpp6(k)	Output Operation Complete	$(0 \leq k \leq 14)$
Cpp7(k)	Device Available	$(0 \leq k \leq 14)$

6.2.2 During input operations, which are designated by a false condition of the Output Priority (Cpc3) line, the wires have the following designations:

6.2.2.1 Signals from L-3155 to ET:

Cpc3(k)	Output Priority	$(0 \leq k \leq 14)$
Cpc4(k)	Input Operation Complete	$(0 \leq k \leq 14)$
Cpc5(k)	Input Operation	$(0 \leq k \leq 14)$

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SCALE		SHEET	5

6.2.2.2 Signals from ET to L-3155:

Cpp5(k)	Device Clock	($0 \leq k \leq 14$)
Cpp6(k)	Input Data	($0 \leq k \leq 14$)
Cpp7(k)	Message Available	($0 \leq k \leq 14$)

6.3 The index k above refers to a specific input-output device connector position on the L-3155 Central Processor console.

7.0 SYSTEM OPERATION - OUTPUT TO THE L-119 BUFFER-PROCESSOR FROM THE L-3155 CENTRAL PROCESSOR

7.1 External Device Addressing.

7.1.1 The preparedness of the L-119 to receive an output message from the L-3155 Central Computer will be ascertained by program testing the appropriate "Device Available" (Cpp3) line and the status of duplexing switching.

7.1.2 The output instruction will select the L-119 and connect its set of signal lines enumerated in section 5.0 to the Central Processor-Buffer Processor Interface.

7.2 Message Transfer from L-3155 Central Processor to L-119.

7.2.1 The "Device Available" (Cpp3) line will remain true throughout the transmission period until the Central Processor returns the "Output Operation" (Cppl) line to the false state. A test instruction during the transmission period will find any output L-119 unavailable.

7.2.2 Data will be transferred to the selected L-119 bit serially over the "Output Data" (Cpo2) line. The first bit transmitted will be the least-significant bit of the most-significant character of the output message.

7.2.3 The true state of the "Output Operation" (Cppl) line will indicate to the external device that a meaningful bit is present on the "Output Data" line. The "Output Operation" line will assume its true state after the first data bit has been established on the "Output Data" line.

7.2.4 When the L-119 is ready to receive the output message, it will send a series of clock pulses to the L-3155 Central Processor on the "Device Clock" (Cppl) line. The L-3155 will use the trailing edges of the clock pulses received from the L-119 to make the subsequent bits of the message available to the L-119.

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SCALE			SHEET 6

- 7.2.5 The L-119 will check the parity of each character as it is received. Parity of each character shall also be checked at the computer prior to transmission.
- 7.3 Output Operation Termination.
- 7.3.1 An end-of-message character transmitted from the Central Processor and recognized by the L-119 will be used to terminate the output operation. The end-of-message character will be the "end-of-message" character specified in the L-3155 Code listed in Appendix A.
- 7.3.1.1 The output operation will also be terminated by the character code for '?' (question mark) as listed in Appendix A, which can be interpreted also as End-of-Block, more block(s) following.
- 7.3.2 After the L-119 recognizes the end-of-message or end-of-block character and has verified parity, it will place a logical one on the "Operation Complete" (Cpp2) line and continue sending clock pulses on the "Device Clock" line.
- 7.3.3 After a logical one is placed on the "Operation Complete" line, the Central Processor will place a logical zero on the Output Operation line.
- 7.3.4 After a logical zero is placed on the "Output Operation" line, the L-119 will place a logical zero on the "Device Available" line, cease transmitting clocks on the "Device Clock" line and place a logical zero on the "Operation Complete" line.
- 7.3.5 When the L-3155 Central Processor places a logical zero on the "Output Operation" line, it will also disconnect the selected external device from the Central Processor-Buffer Processor Interface and generate an "I-O Interface Not Busy" interrupt.
- 7.3.6 The termination control signals will operate in synchronism with the L-119 clock.
- 7.4 Error Considerations.
- 7.4.1 If a parity error is detected by the L-119, it will place a logical one on the "Parity Error" (Cpp4) line and maintain this signal level and continue sending clock pulses on the "Device Clock" line until a logical zero is placed on the "Output Operation" line. The logical one on the "Device Available" line will be maintained by the L-119. "Data Parity Error" interrupt is generated by these conditions.
- 7.4.2 If the L-3155 Central Processor detects an error, it will disconnect the selected L-119 from the Central Processor-Buffer Processor Interface by placing a logical zero on the "Output Operation" line. The

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logical one on the "Device Available" line will be maintained by the L-119. "I-O M Register Error" or "I-O Operand Address Error" interrupt is generated by these conditions.

7.4.3 If the output operation has not terminated normally, as described in 7.3, or by detected error, as described in 7.4.1 and 7.4.2, it will be terminated in $7.0 \pm 10\%$ milliseconds, disconnecting the L-119 and causing an "I-O Hang-up Error" interrupt.

7.4.4 If a logical zero is placed on the "Output Operation" line while a logical zero is on the "Operation Complete" line, the L-119 will ignore all bits received during the interrupted output operation.

8.0 SYSTEM OPERATION - INPUT TO L-3155 CENTRAL COMPUTER FROM THE L-119 BUFFER-PROCESSOR

8.1 External Device Addressing.

8.1.1 The L-3155 Central Processor will contain two interlocked electronic stepping circuits that will cycle and sample the state of the "Message Available" (Pcp1) or (Pcp3) lines of each external device position. Three external device positions will be uniquely available for L-119 Buffer-Processors. One of the two electronic stepping circuits will sample the L-119 "Message Available" lines at computer clock rate. For every cycle through the L-119 positions, the second stepping circuit will advance to the next available ET position, i.e., during every fourth consecutive computer clock period, all L-119 Buffer-Processors and one ET will be sampled for message availability. If a stepping circuit finds that an external device has a message available (logical one level on the "Message Available" line), it will select that position and generate a program interrupt. The program will be able to distinguish between a L-119 message and an ET message by the type of interrupt.

8.1.2 The program can determine the identity of the device having the message available, and cause an input operation from that device by an input instruction.

8.1.3 The input instruction will directly connect the set of signal lines enumerated in section 5.2 or 6.2 of the selected external device to the Central Processor-Buffer Processor Interface.

8.2 Message Transfer from L-119 to L-3155 Central Processor.

8.2.1 The "Message Available" (Pcp1) line will remain true throughout the transmission period until the Central Processor returns the "Input Operation" (Pcp1) line to the false state. However, a test instruction during the transmission period will not find a message available.

CODE IDENT NO.	SIZE		
36090	A	L 190 000 832	
SCALE			SHEET 8

- 8.2.2 Data will be transferred from the selected L-119 bit serially over the "Input Data" (Pop4) line. The first bit transmitted will be the least-significant bit of the most-significant character of the input message.
- 8.2.3 The true state of the "Input Operation" line shall indicate to the L-119 that the L-3155 Central Processor is ready to receive data.
- 8.2.4 When the L-119 is ready to transmit the message, it will send a series of clock pulses to the L-3155 Central Processor on the "Device Clock" (Pop3) line. The computer will use the trailing edges of the clock pulses received from the L-119 to strobe the bits on the "Input Data" line and check parity on each character received.
- 8.3 Input Operation Termination.
- 8.3.1 An end-of-message or end-of-block character transmitted from the L-119 and recognized by the L-3155 Central Processor will be used to terminate the input operation.
- 8.3.1.1 The end-of-message character specified will designate an end-of-message without following blocks.
- 8.3.1.2 The end-of-block character designated by the code representing a question mark will specify blocks following.
- 8.3.2 After the L-3155 Central Processor recognizes either end-of-block or end-of-message character and has verified parity, it will place a logical one on the "Computer Operation Complete" (Poc2) line.
- 8.3.3 After a logical one is placed on the "Computer Operation Complete" line, the L-119 will place a logical zero on the "Message Available" line.
- 8.3.4 The Central Processor will respond to the logical zero on the "Message Available" line by placing logical zeros on the "Input Operation" and "Computer Operation Complete" lines. The logical zero on the "Input Operation" line will disconnect the external device from the Central Processor-Buffer Processor Interface, and generate an "I-C Interface Not Busy" interrupt.
- 8.3.5 The termination control signals will operate in synchronism with the L-119 clock.
- 8.4 Error Considerations.
- 8.4.1 If the L-3155 Central Processor detects an error, it will disconnect the selected L-119 from the Central Processor-Buffer Processor Interface by placing a logical zero on the "Input Operation" line. The

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SCALE		SHEET 9

logical one on the "Message Available" line will be maintained by the L-119. "I-O M Register Error" or "I-O Operand Address Error" interrupt is generated.

8.4.2 If a logical zero is placed on the "Input Operation" line while a logical zero is on the "Computer Operation Complete" line, the L-119 will retain all portions of the message transmitted and it will be prepared to retransmit.

8.4.3 If the input operation has not terminated normally, as described in 8.3, or by detected error, as described in 8.4.1 and 8.4.2, it will be terminated in $7.0 \pm 10\%$ milliseconds, generating an "I-O Hang-up Error" interrupt. Program response to the interrupt can cause the stepping circuit to step, disconnecting the L-119.

8.4.4 The "Stepping Circuits" will be inhibited by the presence of an error condition as specified by any of the detailed error flip-flops associated with the Processor Interface. The Stepping Circuit will continue to select the last device used for 'Input' until either the Ignore Error flip-flop is set, or the detailed error flip-flop is reset.

9.0 SYSTEM OPERATION - OUTPUT TO ET PORTION OF THE ICSS FROM THE L-3155 CENTRAL PROCESSOR

9.1 External Device Addressing.

9.1.1 The preparedness of the external ET device to receive an output message from the L-3155 Central Computer will be ascertained by program testing the appropriate status indicator of the duplexing switching.

9.1.2 The output instruction will directly connect the set of signal lines enumerated in section 6.2 of the selected ET to the Central Processor Input-Output Interface.

9.2 Message Transfer from the L-3155 Central Processor to External Device.

9.2.1 An output operation is initiated by the "Output Priority" (Cpc3) line going true.

9.2.2 In response to this action, the "Device Available" (Cpp7) line must come true within 5.0 microseconds. The "Device Available" line will remain true throughout the transmission period, until the Central Processor returns the "Output Operation" (Cpc5) line to the false state.

9.2.3 Data will be transferred to the selected ET bit serially over the

CODE IDENT NO.	SIZE		
36090	A	L190 000 832	
SCALE			SHEET 10

"Output Data" (Cpch) line. The first bit transmitted will be the least-significant bit of the most-significant character of the output message.

- 9.2.4 The true state of the "Output Operation" (Cpo5) line shall indicate to the ET that meaningful data is present on the "Output Data" (Cpch) line. The "Output Operation" line will assume its true state after the first data bit has been established on the Output Data line but no sooner than 10 microseconds after the "Output Priority" line goes true.
- 9.2.5 When the ET is ready to receive the output message, it will send a series of clock pulses to the L-3155 Central Processor on the "Device Clock" (Cpp5) line. The L-3155 will use the trailing edges of the clock pulses received from the ET to make the subsequent bits of the message available to the ET.
- 9.2.6 The ET shall check the parity of each character as it is received. Parity of each word shall also be checked at the computer prior to transmission.
- 9.3 Output Operation Termination.
- 9.3.1 An end-of-message character transmitted from the Central Processor and recognized by the ET will be used to terminate the output operation. The end-of-message character will be the end-of-message character specified in the L-3155 code as listed in Appendix A.
- 9.3.2 After the ET recognizes the end-of-message character and has verified parity, it will place a logical one on the "Output Operation Complete" (Cpp6) line and continue sending clock pulses on the "Device Clock" (Cpp5) line.
- 9.3.3 After a logical one is placed on the "Output Operation Complete" line, the Central Processor will place logical zeros on the "Output Priority" and "Output Operation" lines.
- 9.3.4 After a logical zero is placed on the "Output Operation" (Cpo5) line, the ET will place a logical zero on the "Device Available" (Cpp7) line, cease transmitting clocks on the "Device Clock" line, and place a logical zero on the "Output Operation Complete" (Cpp6) line.
- 9.3.5 When the L-3155 Central Processor places logical zeros on the "Output Operation" line and the "Output Priority" line, it will also disconnect the selected ET from the Central Processor Input-Output Interface and generate an "I-O Interface Not Busy" interrupt.

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- 9.3.6 The termination control signals will operate in synchronism with the ET clock.
- 9.4 Error Considerations.
- 9.4.1 If a parity error is detected by the ET, it will place a logical zero on the "Device Available" (Cpp7) line without placing a logical one on the "Output Operation Complete" line and continue sending clock pulses on the "Device Clock" line until logical zeros are placed on the "Output Operation" and "Output Priority" signal lines. "Data Parity Error" interrupt is generated by these conditions.
- 9.4.2 If the L-3155 Central Processor detects an error, it will disconnect the selected ET from the Central Processor Input-Output Interface by placing logical zeros on the "Output Operation" and "Output Priority" signal lines without placing a logical one on the "Output Operation Complete" line. When the ET detects a logical zero on the "Output Operation" line, it will stop sending clock pulses and place a logical zero on the "Device Available" line. "I-O M Register Error" or "I-O Operand Address Error" interrupt is generated by these conditions.
- 9.4.3 If "Device Available" does not come true after 1 usec and before 5 microseconds after "Output Priority" goes true, or is true before "Output Priority" goes true, this will lead to an "I-O Hang-up Error" interrupt of the L-3155 Central Processor and cause the ET to be disconnected.
- 9.4.4 If the output operation has not terminated normally, as described in 9.3, or by detected error, as described in 9.4.1 and 9.4.2, it will be terminated in $35 \pm 10\%$ milliseconds, disconnecting the ET and causing an "I-O Hang-up Error" interrupt.

10.0 SYSTEM OPERATION - INPUT FROM THE ET PORTION OF THE ICSS TO THE L-3155 CENTRAL COMPUTER

10.1 External Device Addressing.

- 10.1.1 The L-3155 Central Processor will contain two interlocked electronic stepping circuits that will cycle and sample the state of the "Message Available" (Pcp1) or (Pcp3) lines of each external device position. Three external device positions will be uniquely available for L-119 Buffer-Processors. One of the two electronic stepping circuits will sample the L-119 "Message Available" lines at computer clock rate. For every cycle through the L-119 positions, the second stepping circuit will advance to the next available ET position,

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i.e., during every fourth consecutive computer clock periods, all L-119 Buffer-Processors and one ET device will be sampled for message availability. If a stepping circuit finds that an external device has a message available (logical one level on the "Message Available" line), it will select that position and generate a program interrupt. The program will be able to distinguish between a L-119 message and an ET message by the type of interrupt.

- 10.1.2 The program can determine the identity of the device having the message available and cause an input operation from that device by an input instruction.
- 10.1.3 The input instruction will directly connect the set of signal lines enumerated in section 6.2 of the selected ET to the Central Processor Input-Output Interface.
- 10.2 Message Transfer from the ET to the L-3155.
 - 10.2.1 During an input operation, the "Output Priority" (Cpc3) line will remain false.
 - 10.2.2 The "Message Available" (Cpp7) line will remain true throughout the transmission period, until the Central Processor returns the "Input Operation" (Cpp5) line to the false state.
 - 10.2.3 Data will be transferred from the selected ET bit serially over the "Input Data" (Cpp6) line. The first bit transmitted will be the least-significant bit of the most-significant character of the input message.
 - 10.2.4 The true state of the "Input Operation" (Cpc5) line shall indicate to the ET that the L-3155 Central Processor is ready to receive data.
 - 10.2.5 When the ET is ready to transmit the input message, it will send a series of clock pulses to the L-3155 Central Processor on the "Device Clock" (Cpp5) line. The L-3155 will use the trailing edges of the clock pulses received from the ET to strobe the bits on the "Input Data" line and check parity on each word received.
- 10.3 Input Operation Termination.
 - 10.3.1 An end-of-message character transmitted from the ET and recognized by the L-3155 Central Processor will be used to terminate the input operation. The end-of-message character will be the end-of-message character specified in the L-3155 code as listed in Appendix A.
 - 10.3.2 When the L-3155 Central Processor recognizes the end-of-message character and has verified the parity, it will place a logical one

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on the "Input Operation Complete" (Cp4) line.

- 10.3.3 When a logical one is placed on the "Input Operation Complete" (Cp4) line, the external device will place a logical zero on the "Message Available" (Cp7) line.
- 10.3.4 The L-3155 Central Processor will respond to the logical zero on the "Message Available" line by placing a logical zero on the "Input Operation" line. It will also disconnect the selected external device from the Central Processor Input-Output Interface and generate an "I-O Interface Not Busy" interrupt.
- 10.3.5 The termination control signals will operate in synchronism with the ET clock.
- 10.4 Error Considerations.
- 10.4.1 If a parity error is detected by the ET, it will place a logical zero on the "Message Available" (Cp7) line without placing a logical one on the "Input Operation Complete" line and continue sending clock pulses on the "Device Clock" line until a logical zero is placed on the "Input Operation" (Cp5) line. "Data Parity Error" interrupt is generated by these conditions.
- 10.4.2 If the L-3155 Central Processor detects an error, it will disconnect the selected ET from the Central Processor Input-Output Interface by placing a logical zero on the "Input Operation" line. The ET will stop sending clock pulses and prepare to retransmit. "I-O M Register Parity Error" interrupt is generated by these conditions.
- 10.4.3 If the input operation has not terminated normally, as described in 10.3, or by detected error, as described in 10.4.1 and 10.4.2, it will be terminated in $35 \pm 10\%$ milliseconds, generating an "I-O Hang-up Error" interrupt. Program response to the interrupt can cause the stepping circuit to step, disconnecting the ET.
- 10.4.4 The "Stepping Circuits" will be inhibited by the presence of an error condition as specified by any of the detailed error flip-flops associated with the Processor Interface. The Stepping Circuit will continue to select the last device used for 'Input' until either the Ignore Error flip-flop is set, or the detailed error flip-flop is reset.

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SCALE			SHEET 14

APPENDIX C

LIBRASCOPE SPECIFICATION

L190 000 833

Preliminary Specifications of the MASS
MEMORY output interface with the MC Dis-
play and Console Printer portions of the
ICSS (and LP displays.)

PRELIMINARY

1.0 SCOPE

- 1.1 The Mass Memory Output Interface provides for information transfer between the L-3155 Central Processor and the MC and CP portions of the ICSS. Any device satisfying the MC requirements (such as a Large Panel Display) can be connected to this interface.

2.0 LANGUAGE AND WORD

- 2.1 An L-3155 Central Processor character consists of six data bits and one odd parity bit. The code used in the L-3155 is given in Appendix A.
- 2.2 Eight characters constitute one word.
- 2.3 Sixteen words constitute one block.
- 2.4 Information transfers from the L-3155 Central Processor to the Mass Memory (for subsequent transmission to the ICSS) shall be in units of blocks.
- 2.5 An output message from the Mass Memory to the MC is defined as a sequence of words transmitted bit serially over the MC data line. A word is transmitted most-significant character first. Each character is transmitted least-significant bit first. Every seventh bit transmitted will be the odd parity bit for the six preceding data bits.
- 2.6 An output message from the Mass Memory to the CP is defined as a sequence of characters transmitted seven-bit parallel over the CP character lines. The seventh bit is the odd parity bit for the other six bits.

3.0 SIGNAL LEVELS AND IMPEDANCE

- 3.1 Signals to MC and CP.
- 3.1.1 A "true" level (logical one) on the signal lines to the external devices shall be represented by $-8.5V \pm 2.5V$.
- 3.1.2 A "false" level (logical zero) on the signal lines to the external devices shall be represented by $0V \pm 1V$.
- 3.1.3 The signals to the external devices shall be transmitted over 75 ohm coaxial line such as Amphenol 21-597.

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SCALE		SHEET

- 3.1.4 The input impedance of the external device for any input signal line shall be 75 ohms $\pm$ 10% for either the true or false levels. This specified impedance shall include any required line termination.
- 3.1.5 The rise and fall times measured between the 10% and 90% points shall be between 0.1 and 0.3 microseconds after transmission through two hundred feet of properly terminated coaxial line.
- 3.2 Signals from MC and CP.
- 3.2.1 A "true" level (logical one) on the signal lines from the external devices shall be represented by -8.5V $\pm$ 2.5V.
- 3.2.2 A "false" level (logical zero) on the signal lines from the external devices shall be represented by 0V $\pm$ 1.0V.
- 3.2.3 The signals from the external devices will be transmitted over 75 ohm coaxial line such as Amphenol 21-597.
- 3.2.4 The input impedance to any signal from the external device will be 75 ohms $\pm$ 10% for either the true or the false levels.
- 3.2.5 The rise and fall times measured between the 10% and 90% points shall be between 0.1 and 3.0 microseconds after transmission through two hundred feet of properly terminated coaxial line.
- 3.3 Transfer Rates.
- 3.3.1 Transfer rate from the Mass Memory to the MC shall be at 356,000 $\pm$ 10% bits per second, controlled by the Mass Memory clock. The transfer will initiate at a maximum of 5.6 milliseconds, in most cases, in response to a demand by the MC.
- 3.3.2 Transfer rate from the Mass Memory to the CP shall be 14 $\pm$ 5% characters per second maximum, as determined by demand by the CP.
- 4.0 INTERFERENCE LIMITS
- 4.1 Any External Device which interfaces with the L-3455 Mass Memory shall meet the interference limits as specified in MIL-I-26600.

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5.0 SIGNALS REQUIRED FOR OUTPUT OPERATION FROM MASS MEMORY TO MC

5.1 Signals from Mass Memory to MC.

i = Addressed Device

5.1.1	F1MC(i)	Word Transfer Order	$0 \leq i \leq 14$
5.1.2	F2MC(i)	Data	$0 \leq i \leq 14$
5.1.3	F3MC(i)	Clock	$0 \leq i \leq 14$
5.2	Signals from the MC to Mass Memory.		
5.2.1	MCF(i)	Word Demand	$0 \leq i \leq 14$

6.0 SIGNALS REQUIRED FOR OUTPUT OPERATION FROM MASS MEMORY TO CP

6.1 Signals from Mass Memory to CP.

j = Addressed Device

6.1.1	F0CP(j)	Character Available	$0 \leq j \leq 14$
6.1.2	F(k)CP(j)	Data $1 \leq k \leq 6$	$0 \leq j \leq 14$
6.1.3	F7CP(j)	Parity	$0 \leq j \leq 14$
6.2	Signals from CP to Mass Memory.		
6.2.1	CPF(j)	Character Demand	$0 \leq j \leq 14$

7.0 SYSTEM OPERATION - OUTPUT TO MC

7.1 Transfer from Central Processor to Mass Memory Buffer Store (MMBS).

7.1.1 The preparedness of the MC to receive an output message may be in part ascertained by program testing of the status of the duplexing switching.

7.1.2 The selection of a specific output channel, and thereby the MC to which it is connected, shall be by specific characters in the File Command that initiates transfer of a program designated number of blocks from the Central Processor to MMBS.

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- 7.1.3 Mass Memory Buffer Store (MMBS) will consist of 1000 blocks of storage within the File Console, numbered sequentially and filled sequentially and cyclically by the Central Processor. The sequential filling is handled automatically, and is not under program control.
- 7.1.4 As with other File Commands, the Central Processor program is signaled by a "File Not Busy" interrupt when message transfer to MMBS ends.
- 7.1.5 Error Considerations.
- 7.1.5.1 When message transfer to the MMBS cannot take place without overwriting a non-transmitted block, the message transfer ends. The program can detect incomplete transfer by a specific test in response to interrupt, and determine the appropriate manner in which to resume message transfer.
- 7.1.5.2 When a message transfer is programmed to the MMBS addressed to an output channel engaged in transmission to an MC or to which there is not connected an MC ready to receive a transmission, the message transfer to MMBS will not take place and a "Display" interrupt will be generated. The program can detect failure of the message transfer by a specific test in response to the interrupt. This test is further described in section 7.2.9.5.
- 7.2 Message Transfer from Mass Memory Buffer Store (MMBS) to MC.
- 7.2.1 Concurrent with the transfer to MMBS, the first two blocks (or the only block) of the message are loaded into the selected output channel circulating line. This loading, as well as the transfer to MMBS, is conditioned by a logical one on the "Word Demand" line.
- 7.2.2 After the selected output channel is loaded (taking approximately 5.6 milliseconds), and after a delay of approximately 0.3 milliseconds for the first word to appear, the first word is transmitted to the MC bit serially over the Data line, as described in section 2.5.
- 7.2.3 A logical one on the Word Transfer Order line shall indicate to the MC that meaningful data is present on the Data line. A logical zero will be placed on the "Word Transfer Order" line at the end of the last (56th) bit of the data.
- 7.2.4 Clock pulses will be present on the Clock line concurrent with the center of the data bits. The clock pulses shall be in the logical one state a minimum of 0.2 microseconds as measured at the 90%

CODE IDENT NO.	SIZE	
36090	A	L190 000 833
SCALE		SHEET 5

amplitude points. The clock pulses shall be in the logical zero state a minimum of 2.0 microseconds as measured at the 10% amplitude points. The center of the clock pulses shall be concurrent with the center of the data within 0.5 microseconds.

- 7.2.5 Successful transmission of the word will be acknowledged by the MC by placing a logical zero on the Word Demand line within 4.5 milliseconds after a logical zero is placed on the Word Transfer Order line. The logical zero must remain on the Word Demand line a minimum of 10 microseconds.
- 7.2.6 After acknowledgement, a logical one placed on the Word Demand line will indicate readiness of the MC to receive the next word. If acknowledgement is made as in section 7.2.5, and a logical one placed on Word Demand within 4.5 milliseconds after the end of a word transmission, the next word will be transmitted 5.6 milliseconds after the end of a word transmission. A longer delay in placing a logical one on Word Demand will cause transmission of the next word in a corresponding multiple of 5.6 milliseconds after the end of a word transmission.
- 7.2.7 After the first block in the output channel has been transmitted, transmission of words from the second block ensues without hesitation, while the output channel accesses MMBS to mark the first block obsolete and to pick up the third block of the message and ready it for transmission. Transmission of the remaining blocks proceeds smoothly in this manner except for occasional possible interference by loading of MMBS by the Central Processor or by accesses by other output channels.
- 7.2.8 Termination of Transmission.
- 7.2.8.1 When the last word of the last block in MMBS for any channel has been transmitted, the MC will acknowledge as in section 7.2.5. The output channel will access and mark obsolete this block in MMBS, and enter a non-transmitting state. As soon as the Central Processor-Mass Memory interconnection allows, a "Display" interrupt will be generated.
- 7.2.8.1.1 If the last word of a transmission is not an EOM, the MC will request further transmission as in section 7.2.6, which will allow the program to load a continuation of the output display image as in section 7.1.
- 7.2.8.1.2 If the last word of a transmission is an EOM, the MC will continue to place a logical zero on the Word Demand line until such time as it can accept resumption of transmission.

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- 7.2.8.2 The Central Processor can test the status of all the output channels as to transmitting, or non-transmitting, and thus determine, in response to interrupt, which channel is ready for loading.
- 7.2.9 Error Considerations.
- 7.2.9.1 Parity Errors in Transmission.
- 7.2.9.1.1 If a parity error is detected by the MC, there will be no acknowledgement as in section 7.2.5, and the MC will continue to place a logical one on the Word Demand line for at least 4.5 milliseconds after a logical zero is placed on the Word Transfer Order line.
- 7.2.9.1.2 The Output Channel will respond to the error indication in section 7.2.9.1.1 by retransmitting the word as described in sections 2.5, 7.2.3 and 7.2.4. Retransmission will begin in approximately 5.6 milliseconds after the previous transmission.
- 7.2.9.1.3 Successful retransmission will be acknowledged as described in section 7.2.5 and the normal transfer sequence will resume.
- 7.2.9.1.4 If a parity error is detected in the first retransmission, the conditions in sections 7.2.9.1.1, 7.2.9.1.2 and 7.2.9.1.3 will again apply, providing a second retransmission.
- 7.2.9.1.5 If a parity error is detected in the second retransmission, the conditions in section 7.2.9.1.1 shall apply. Approximately 5.6 milliseconds after the second retransmission, a logical one will be placed on the Word Transfer Order line for the normal duration of a Word Transmission. When a logical zero is again placed on the Word Transfer Order line, the transfer to the MC will be considered to have aborted.
- 7.2.9.2 Signal Failures.
- 7.2.9.2.1 If the Word Demand line fails so that a logical one is continuously presented to the Output Channel, the sequence described in 7.2.9.1 will take place, as though there were repeated parity errors, and the message transmission will abort.
- 7.2.9.2.2 If the Word Demand line presents a logical zero between MMBS loading as described in section 7.2.1 and first word transmission as described in section 7.2.2, the message transmission will abort.
- 7.2.9.2.3 If the Word Demand line, after acknowledging a successful transmission, as described in section 7.2.5, fails to demand the next word as described in section 7.2.6 within a timed interval after the end of the acknowledged transmission, the transmission will abort. The timed interval will be 3.0 ± 1.0 seconds.

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- 7.2.9.2.4 Should there be a failure of the Word Transfer Order line or the Clock line, the MC will not acknowledge transmission and the sequence described in 7.2.9.1 will take place, as though there were repeated parity errors and the message transmission will abort.
- 7.2.9.2.5 If the Data line fails, it will either send logical zeros, recognized as bad parity, or logical ones in which case message transfer is not halted, unless the MC recognizes this condition and induces an abort.
- 7.2.9.3 When message transfer to an MC is aborted resulting from conditions described in sections 7.2.9.1 and 7.2.9.2, the Output Channel will cease responding to signals on the Word Demand line, and will cease transmitting words. It will find and mark obsolete all remaining blocks of the message in MMES, and then enter a "non-transmitting, error" state. As soon as the Central Processor-Mass Memory interconnection allows, a "Display" interrupt will be generated.
- 7.2.9.4 The Central Processor test of Output Channel status, described in section 7.2.8.2, will indicate additionally for each channel whether the non-transmitting state resulted from a successful transmission or from an abort condition.
- 7.2.9.5 The Central Processor test of Output Channel status, described in sections 7.2.8.2 and 7.2.9.4, will indicate additionally for each channel whether an operative MC is present as indicated by a logical one on the Word Demand line.

8.0 SYSTEM OPERATION - OUTPUT TO CP

- 8.1 Transfer from Central Processor to the Mass Memory Console Printer Store (MMCPs).
- 8.1.1 The preparedness of the CP to receive an output message may be in part ascertained by program testing of the status of the duplexing switching.
- 8.1.2 The selection of a specific output channel, and thereby the device to which it is connected, shall be by a specific file address in the File Command that initiates transfer of the message to Mass Memory Console Printer Store.
- 8.1.3 The Mass Memory Console Printer Store (MMCPs) will consist of 15 regions of storage, each region capable of holding up to 1110 characters. Each region will operate in conjunction with a specific one of the 15 Console Printer Output Channels.
- 8.1.4 As with other File Commands, the Central Processor program is

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signaled by a "File Not Busy" interrupt when message transfer to MMCPs ends.

8.1.5 Error Considerations.

8.1.5.1 When a message transfer is programmed to the MMCPs addressed to an output channel engaged in transmission to a CP, the message transfer to MMCPs will not take place and a "Display" interrupt will be generated. The program can detect failure of the message transfer by a specific test in response to the interrupt. This test is further described in section 8.2.6.

8.2 Message Transfer from Mass Memory Console Printer Store (MMCPs) to CP.

8.2.1 Subsequent to MMCPs loading, and after access time, the Character Available line will go true indicating presence of the first valid character of the message on the Data lines and on the Parity line.

8.2.2 The Character Demand line may be on or may come on in response to a signal on the Character Available line.

8.2.3 When the Character Demand line goes false, the Character Available line will go false within 4 usec. and access to the next character will begin. This access will last between 4 usec. and 70 milliseconds.

8.2.4 After the next character is accessed, the message transfer will continue as described in 8.2.1.

8.2.5 When the end of the message loaded into MMCPs is reached, or when an EOM character is detected, message transmission will cease and a "Display" interrupt will be generated.

8.2.6 The Central Processor can test the status of all output channels as to transmitting/unavailable or not transmitting, and thus determine, after interrupt, which channel is ready for loading. Unavailable status shall be indicated by a logical zero on the "Character Demand" line after the output channel has finished transmitting.

8.3 Error Considerations.

8.3.1 No provision is made to detect erroneous parity in the MMCPs during transmission, nor is provision made to signal the MMCPs of parity error detected in the CP.

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