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NRL Report 5866

# A DIODE DIGITAL-TO-ANALOG CONVERSION TECHNIQUE

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## ABSTRACT

The transformation of information which is in digital form to an analogous form involving electrical potentials or currents is called digital-to-analog conversion. The transformation is approximate since errors are introduced during conversion. Various techniques have been developed to minimize these errors; the most popular ones are the weighted resistor method and the ladder arrangement.

The weighted resistor can be used as the input to a summing amplifier, and the voltage input errors to the weighted resistor can be reduced through the use of a balanced-current diode switching circuit. Experimental results derived from an investigation of the characteristics of the diode switching circuit showed a maximum switching error of $\pm 6 \times 10^{-3}$ volts. The calculated value for the worst case of relative output error for the converter is 0.065 percent when the switch is used as the input to the weighted resistor. Actual measurements performed on the output of the 11-bit input converter gave a maximum relative error of only 0.027 percent. The digital-to-analog conversion speed amounted to 20 microseconds for the case considered.

The advantages of the diode switch as an auxiliary to the weighted resistor method are simplicity of design, guaranteed linearity of error, low relative output errors, and, in conjunction with the summing amplifier, the ability to control large changes of voltage while supplying relatively large output currents.


## PROBLEM STATUS

This is an interim report. Work on this problem is continuing.

## AUTHORIZATION

NRL Problem R06-06
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# A DIODE DIGITAL-TO-ANALOG CONVERSION TECHNIQUE

## INTRODUCTION

Digital-to-analog conversion is an approximate relationship between a digital input and an electrical potential or current as output. Whereas the digital input is precise by nature, the electrical analog can only be an approximation of the input since conversion introduces errors. These errors are associated with deviation from a true position and position linearity. Various techniques have been developed to minimize conversion errors. Among the most popular techniques are the weighted resistor method and the ladder arrangement. Although the errors in the weighted resistor method tend to be greater than in the ladder arrangement, the weighted resistor method has the advantage of simplicity of design and can be used as the input to a summing amplifier, which in turn has the capability of controlling large changes in voltage and supplying relatively large amounts of current. This report will describe a technique employing diode switches and precision resistors as the input to a summing amplifier in order to provide a realistic short- and long-term relative output error and a guaranteed linearity of at least 0.065 percent.

## DIODE SWITCHING CIRCUIT

Figure 1 is a schematic of a switching circuit employing diodes that can be used in conversion circuits. $R_1$ sets the total current at the junction of the diodes $D_2$ and $D_3$. The size of $R_x$ is such that the parallel combination of $R_{sum}$ and $R_x$ produces a current through $D_3$ equal to that in $D_2$. Switch sw1 can be any device which, when closed, connects the $D_2$-$D_3$ diode junction to a voltage $-V_2$ that will back-bias diodes $D_2$ and $D_3$. Diode $D_1$ is used to prevent the back-bias voltage on diode $D_3$ from exceeding approximately one volt. In the physical circuit, diodes $D_2$ and $D_3$ are held in close proximity to keep surrounding temperature differences to a minimum. These diodes therefore should be placed apart from any heat sources.

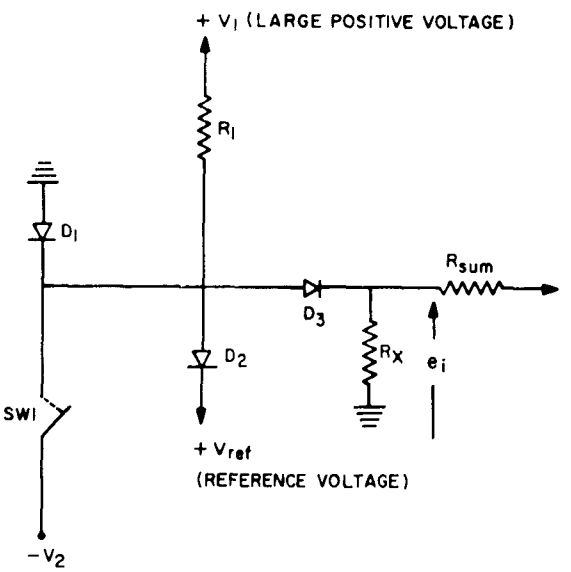



Fig. 1 - Diode switching circuit

In general when switch sw1 is open, $e_i$ equals the reference voltage $V_{ref}$. When sw1 is closed, diodes $D_2$ and $D_3$ are back-biased, and $e_i$ will equal approximately zero. Therefore, the degree to which the reference voltage $V_{ref}$ can be reproduced at the output of $D_3$ (diodes $D_2$ and $D_3$ conducting) and the degree to which ground reference can be maintained at the output of diode $D_3$ (diodes $D_2$ and $D_3$ back-biased) are the major factors contributing to the switching error. By adjusting the current through diodes $D_2$ and $D_3$, $e_i$ can be made equal to the reference voltage $V_{ref}$, but the characteristics of the circuit must be such that short- and long-term drifts remain within prescribed limits. The so-called "ideal diode" could accomplish this, but, in the practical sense, a diode with low drift characteristics, operating on that part of the volt-ampere characteristic curve which provides a small change in voltage for large changes in current, and with reasonable dissipation levels could approximate the ideal condition.

## DIODE SELECTION

To meet the conditions of low drift characteristics and reasonable dissipation levels, possible diode pairs $D_2$ and $D_3$ were matched on a curve tracer. Those pairs were selected which had characteristic curves which, in addition to maximizing $di/dv$ in the operating region, had voltage-drop differences of less than 5 millivolts. This task was accomplished with very little difficulty. There are, however, sufficient differences between diode curves so that a selection of diode pairs with only a 1-millivolt difference would have been very tedious.

Tests were run on a cross section of both germanium and silicon diodes to determine what type of diode best fit these requirements. Selected for testing were diode types 1N92, 1N137, 1N138, 1N198, 1N251, 1N270, 1N351, 1N627, and 1N629. Table 1 is a tabulation of diode characteristics for the above diodes as given by the Electronic Industries Directory. Figure 2 is the test setup used to determine their drift characteristics. For testing purposes, a reference voltage of +50 volts was selected. The reason for selecting a large reference voltage will be discussed later in this report.

Table 1
Diode Characteristics as Given by the Electronic Industries Directory

| Diode | Reverse | | | Forward | |
|---|---|---|---|---|---|
| | $E_p$(volts) | $I_{max}$($\mu$a) | at V(volts) | $I_{min}$(ma) | at V(volts) |
| 1N137A* | 36 | 0.03 | 20 | 3 | 1.0 |
| 1N138* | 18 | 0.01 | 10 | 5 | 1.0 |
| 1N198† | 75 | 10.0 | 10 (at 25°C) | 4 | 1.0 |
| 1N251† | 200 | 0.1 | 10 | 5 | 1.0 |
| 1N270 | 20 | 75.0 | 10 (at 25°C) | 200 | 1.0 |
| 1N351* | 120 | 0.03 | 100 | 20 | 1.0 |
| 1N627* | 84 | 30.0 | 75 | 4 | 1.5 |
| 1N629* | 200 | 100.0 | 75 | 4 | 1.5 |

*Silicon diode.
†Germanium diode.

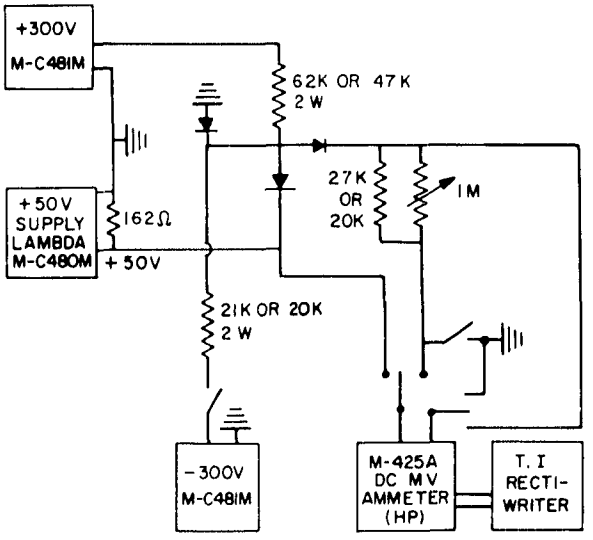



Fig. 2 - Diode drift and leakage current test apparatus

The initial tests on diode drift were conducted with a one-hour sampling period at an ambient temperature of 25°C. Table 2 shows the results of these tests. A measurement of leakage current versus back-bias voltage was also made at 25°C. The test arrangement and the results are shown in Figs. 3 and 4, respectively. The experimental arrangement in Fig. 3 was used only for this test. Diodes 1N92, 1N198, and 1N270 were subsequently eliminated from further testing due to their relatively high degree of leakage current or drift (Fig. 4).

Table 2
Diode Drift for a One-Hour Sampling Period at an Ambient Temperature of 25°C

| Diode | 1N137A | 1N138 | 1N198 | 1N251 | 1N270 | 1N351 | 1N627 | 1N629 |
|---|---|---|---|---|---|---|---|---|
| Peak-to-peak drift (mv) | 2.0 | 2.3 | 3.7 | 2.3 | 2.4 | 2.0 | 3.2 | 2.6 |
| | (these values are for the worst cases of drift) | | | | | | | |

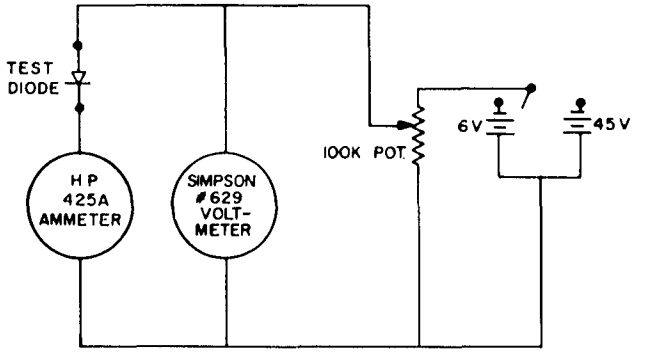



Fig. 3 - Leakage current vs back-bias voltage test setup

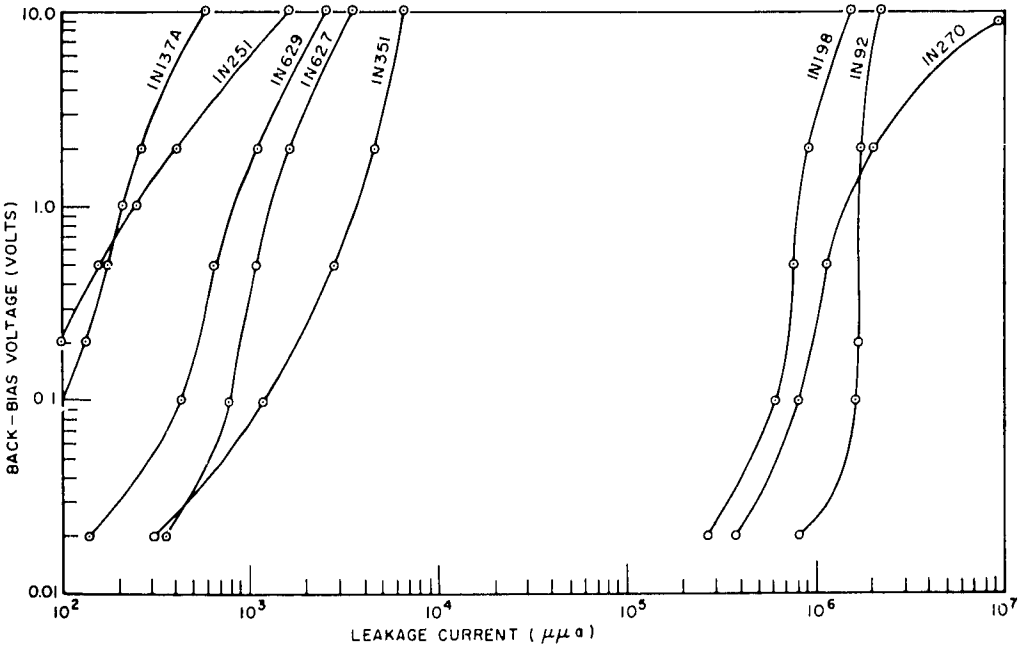



Fig. 4 - Leakage current vs back-bias voltage at 25°C

The second phase of testing consisted of diode drift and leakage current measurements made while varying the ambient temperature from -20°C to +60°C during the sampling period (Table 3). For this test, duplicate diode circuits were used, one having an operating current of 2 milliamperes, and the other, 4 milliamperes. Two operating currents were selected in order that the effects at two operating points could be observed; however, no significant difference was observed from the recorded data. This was probably due to the placement of the operating points well above the bend in the diode characteristic curve. (In all the tests the voltage difference between the reference voltage $V_{ref}$ and the diode $D_3$ output voltage was initially set to zero by the trimming resistor $R_x$ (Fig. 1).) The results of the drift and the leakage current tests are shown in Tables 3 and 4. It should be noted in Table 4 that the back-biased voltage was different for the two circuits even though the same type of diode was used as a clamp. This was attributed to differences in the clamping currents as well as differences in the diode characteristic curves. Due to these differences, the increase of leakage current for the 80-degree temperature change was used as a measure of the particular diode. The tests indicated that diodes 1N137 and 1N351 displayed the best compromise between drift and leakage current. Diode 1N351 was selected finally over diode 1N137 since in the intended application the back-bias voltage would have exceeded the maximum allowed for diode 1N137. The maximum peak-to-peak drift for the 1N351 was $6 \times 10^{-3}$ volts. The maximum leakage current was $0.11 \times 10^{-6}$ amperes. The leakage current would produce a voltage error at the summing resistor input which can be calculated from Ohm's law $V = IR$, where R is the parallel combination of the summing resistor and $R_x$, the current trimming resistor, which approximately equals $13 \times 10^3$ ohms. Substituting this value of R we obtain

$$V = 0.11 \times 10^{-6} \times 13 \times 10^3 = 1.43 \times 10^{-3} \text{ volts.}$$

Since this is much less than the switching error of $6 \times 10^{-3}$ volts, it can be neglected in the worst case of relative output error calculation.

Table 3
Diode Drift for a Temperature Change from -20°C to +60°C

| Diode | 1N137 | 1N251 | 1N629 | 1N351 | | |
|---|---|---|---|---|---|---|
| | | | | Run 1 | Run 2 | Run 3 |
| Peak-to-peak drift (mv) | 4.0 | 7.6 | 7.6 | 6.0 | 4.0 | 4.0 |
| | (these values are for the worst case of drift) | | | | | |

Table 4
Diode Leakage Current and Back-Bias Voltage at +25°C and +60°C for the Worst Case

| Diode | 1N137 | 1N251 | 1N351 | 1N629 |
|---|---|---|---|---|
| Leakage current at 25°C (mμa) | 40 | 13 | 40 | 40 |
| Bias voltage at 25°C (mv) | 700 | 1100 | 700 | 1000 |
| Leakage current at +60°C (mμa) | 170 | 150 | 110 | 320 |
| Bias voltage at +60°C (mv) | 1100 | 1070 | 680 | 1000 |
| Increase of leakage current for $\Delta\Gamma$ (mμa) | 130 | 137 | 60 | 280 |

## DIGITAL-TO-ANALOG CONVERTER

### Error Analysis

To show that the diode switching circuit could be used in a practical digital-to-analog conversion circuit, a converter consisting of an 11-bit input, in 1224 code, to a Philbrick operational amplifier was constructed. A large reference voltage of +40 volts was selected since, from the general equation for the operation of the summing amplifier where the gain for practical purposes is infinite (see Eq. (1) below), the error in the output voltage would vary proportionally to the errors in the voltage input to the summing resistors:

$$e_o = -R_f \sum_{i=1}^{n} \frac{e_i}{R_i}, \tag{1}$$

where $R_f$ is the feedback impedance, $R_i$ refers to the individual summing impedances, $e_o$ is the output voltage, and $e_i$ is the input voltage to the individual summing resistors. Therefore, since the absolute error at input remains constant, the relative output precision for a large reference voltage would be greater. This results in less stringent tolerances being placed on the components involved.

Figures 5-7 show the assembly and detail drawings of the digital-to-analog converter for circuit No. 1. In this circuit there is an additional uncertainty contributed by the precision of the summing resistors in addition to (a) the error in switching the reference voltage to the summing resistor input, and (b) the ground reference error. From the relationship expressed by Eq. (1), the worst case full-output percent error can be determined by taking the total differential

$$de_o = -R_f \sum_{i=1}^{n} \frac{de_i}{R_i} - \sum_{i=1}^{n} \left( e_i \frac{dR_f}{R_i} \right) + R_f \sum_{i=1}^{n} \frac{dR_i}{R_i^2} e_i . \tag{2}$$

The second term represents the change in output voltage which would result if the feedback resistor changed values. This is a linear relationship and the term can be neglected for short-term conversion work, or if the selected resistor is very stable. The resistor used was a Daven No. 1307 precision resistor with a temperature coefficient of ±20 parts per million per degree centigrade, which would allow a temperature change of 1.25°C for an error contribution of less than a millivolt. This is a conservatively low condition for most operating environments and the second term can therefore be neglected. Rearranging, we obtain

$$de_o = -\sum_{i=1}^{n} \frac{R_f}{R_i} de_i + \sum_{i=1}^{n} \left( \frac{R_f}{R_i} \right) \left( \frac{dR_i}{R_i} \right) e_i , \tag{3}$$

where $de_i$ is the absolute error in the input voltage to each summing resistor, which from experimental results for the worst case of the acceptable 1N351 diode equals $6 \times 10^{-3}$ volts, $e_i$ is the reference voltage (+40 volts, nominally), $dR_i/R_i$ is the tolerance of each of the summing resistors, and

$$\sum_{i=1}^{n} \frac{R_f}{R_i}$$

is the summing ratio, where for $dR_i/R_i$ equal to 0.1 percent for the least significant bit ($i = 1$) and 0.05 percent for $i = 2$ to $i = 11$ this summing ratio becomes 1.995 and 0.0025, respectively; the other component values are $R_f = 20$ kilohms and, for $i = 1$ to $i = 11$, $R_i = 20, 40, 100, 200, 200$, and 400 kilohms and 1, 2, 2, 4, and 8 megohms, respectively. These summing ratios result in

$$de_o = -1.9975\, de_i - \left( 1.995 \frac{dR_i}{R_i} + 0.0025 \frac{dR_i}{R_i} \right) e_i .$$

Substituting the other values and changing signs to calculate the worst-case error we obtain

$$de_o = 12 \times 10^{-3} \text{ volts} + 39.9 \times 10^{-3} \text{ volts} + 0.1 \times 10^{-3} \text{ volts} = 52 \times 10^{-3} \text{ volts}.$$

Evaluating Eq. (1), using the applicable values listed for Eq. (3), we get $e_o = -(1.9975 \times 40)$ volts or -79.9 volts. Therefore, the full-output, worst-case percent error becomes

$$\frac{de_o}{e_o} = \frac{52 \times 10^{-3} \text{ volts}}{79.9 \text{ volts}} \times 100 \text{ percent} = \pm 0.065 \text{ percent error}.$$

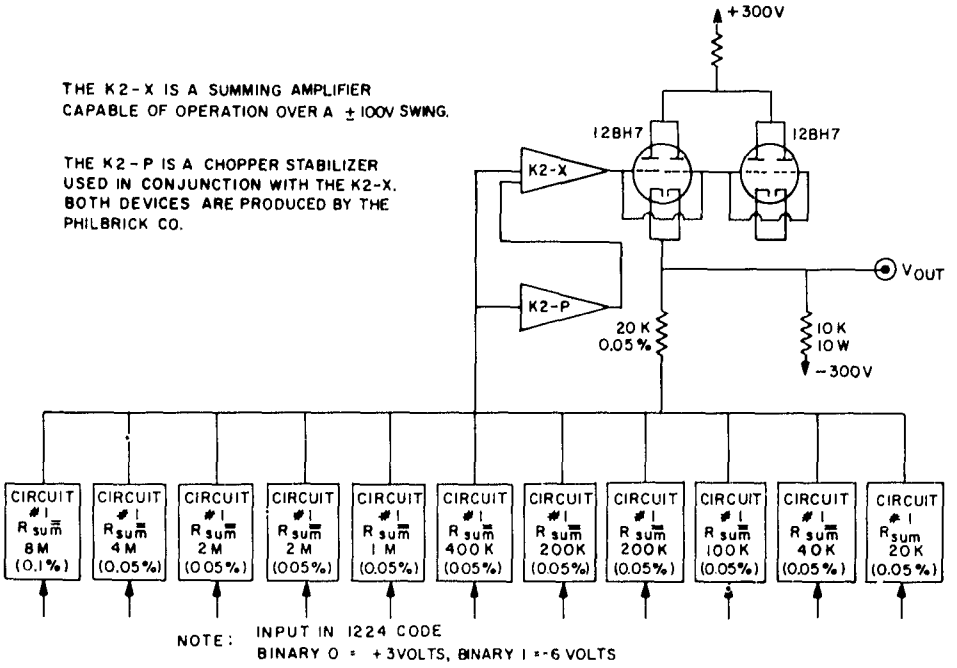
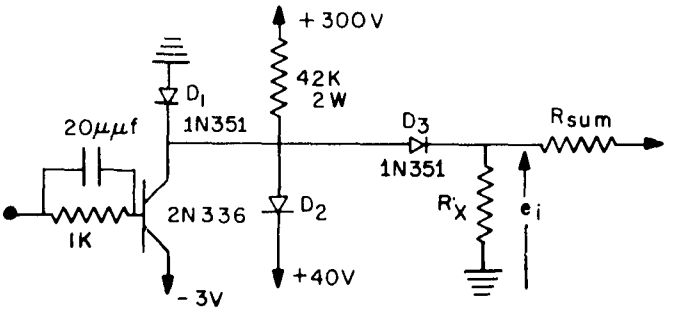



Fig. 5 - Digital-to-analog converter assembly drawing and 11-bit input of circuit No. 1




Voltage Reference

| Fraction of Circuit Contribution | $e_o$(volts) | $I_o$(ma) | $R_x$(× $10^3$ ohms) | $R_{sum}$ | Precision (%) |
|---|---|---|---|---|---|
| 1/400 | 0.1 | 0.005 | 13.0 | 8M | 0.1 |
| 1/200 | 0.2 | 0.01 | 13.0 | 4M | 0.05 |
| 1/100 | 0.4 | 0.02 | 13.0 | 2M | 0.05 |
| 1/100 | 0.4 | 0.02 | 13.0 | 2M | 0.05 |
| 1/50 | 0.8 | 0.04 | 13.0 | 1M | 0.05 |
| 1/20 | 2.0 | 0.1 | 13.0 | 400K | 0.05 |
| 1/10 | 4.0 | 0.2 | 14.0 | 200K | 0.05 |
| 1/10 | 4.0 | 0.2 | 14.0 | 200K | 0.05 |
| 1/5 | 8.0 | 0.4 | 15.0 | 100K | 0.05 |
| 1/2 | 20.0 | 1.0 | 19.3 | 40K | 0.05 |
| 1 | 40.0 | 2.0 | 43.0 | 20K | 0.05 |

Note: For the higher order bits it is required that $R_x$ be trimmed to satisfy the equality $V_{ref} = e_i$.

Fig. 6 - Schematic of circuit No. 1 and tabulated values of $R_{sum}$ circuit contributions

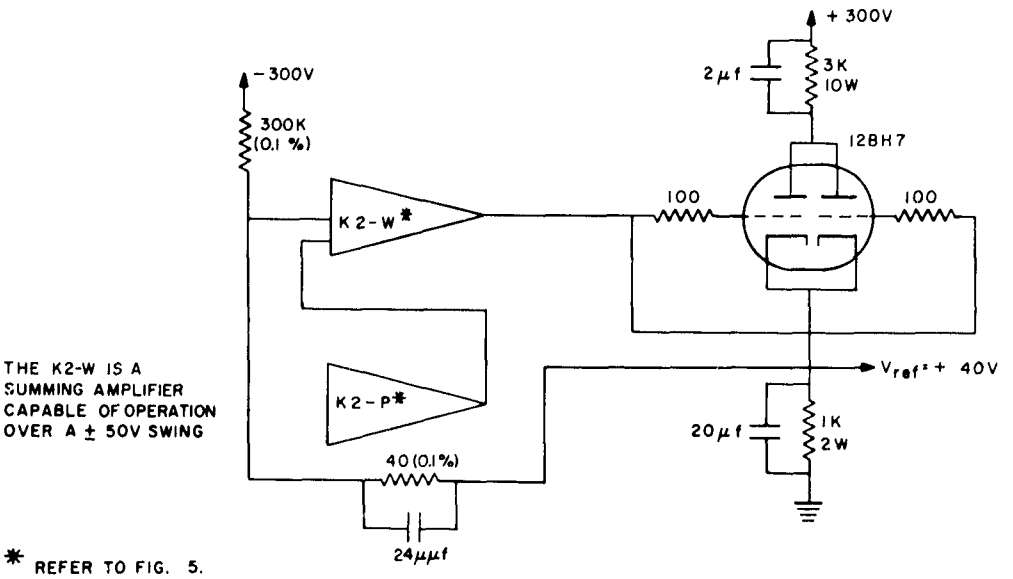



Fig. 7 - Voltage reference power supply for circuit No. 1

Experimental Results

This value was checked experimentally by measuring the output error for various bit configurations. The measurements were made using a Kintel 302 dc-voltage standard which has the inherent ability to measure voltage inputs to a millivolt, using the null method, with an accuracy of 0.01 percent. Figure 8 shows the experimental setup. The procedure used was to measure the output of each bit individually, then to measure progressively the contribution of all the bits. The five least significant bits were not measured individually since the Kintel 302 does not measure voltages less than 1 volt. The percent error was then calculated from the equation

$$\text{Percent Error} = \left( \frac{\text{Measured Output} - \sum_i \frac{R_f e_i}{R_i} + \text{Measurement Error}}{\text{Full Output}} \right) \times 100.$$

The measurement error is measured in terms of millivolts. The term

$$\sum_i \frac{R_f e_i}{R_i}$$

is the output for all the bit contributions where each $e_i$ is measured at the same time that the output reading is taken. The tabulated measurements and results are shown in Table 5. As shown, the worst-case error occurred near full output and amounted to 0.027 percent. This is less than the maximum theoretical error, as might be expected, if the input error contribution was random in nature instead of worst-case additive or subtractive.

A test was also conducted on the drift characteristics of the digital-to-analog-converter full output. Figure 9 shows the experimental setup. The sampling period was 24 hours. The drift over this period amounted to $6 \times 10^{-3}$ volts peak to peak. This agrees with the advertized drift for the summing amplifier of ±8 millivolts. Also Table 5 can be used to

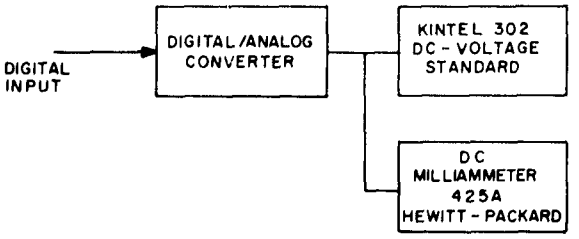



Fig. 8 - Output-error test setup

Table 5
Measurements of the Output Error

| $V_{ref}$ (volts) | $-V_{300}$ (volts) | $E_{out}$ (mv) for $e_i = 0$ | $e_o$ (nominal volts) | $\sum \frac{R_f}{R_i}$ | $\sum \frac{R_f e_i}{R_i}$ for $e_i = V_{ref}$ | Measured $e_o$ (mv) | $e_o - \sum \frac{R_f e_i}{R_i}$ (mv) | ±Instrument Error (mv) | Total Output Error | Percent Output Error |
|---|---|---|---|---|---|---|---|---|---|---|
| 39.984 | 300.021 | -3.5 | 0 | 0.0 | 0.0 | -3.5 | -3.5 | - | - | - |
| 39.984 | | -3.1 | 2 | 0.05 | 1.999 | 2.001 | +3.0 | 0.2 | 3.2 | .004 |
| 39.983 | 300.034 | -2.9 | 4 | 0.1 | 3.998 | 4.001 | +3.0 | 0.4 | 3.4 | .004 |
| 39.983 | | -2.9 | 4 | 0.1 | 3.998 | 3.998 | 0.0 | 0.4 | 0.4 | .0005 |
| 39.984 | 300.050 | -2.85 | 8 | 0.2 | 7.997 | 7.998 | +1.0 | 0.8 | 1.8 | .002 |
| 39.984 | | -2.85 | 20 | 0.5 | 19.992 | 19.992 | 0.0 | 2.0 | 2.0 | .003 |
| 39.985 | | -2.80 | 40 | 1.0 | 39.985 | 39.994 | +9.0 | 4.0 | 13.0 | .016 |
| 39.986 | 300.065 | -2.75 | 60 | 1.5 | 59.979 | 59.989 | +10.0 | 6.0 | 16.0 | .020 |
| 39.986 | | -2.70 | 68 | 1.7 | 67.976 | 67.985 | +9.0 | 6.8 | 15.8 | .019 |
| 39.986 | | -2.65 | 72 | 1.8 | 71.975 | 71.982 | +7.0 | 7.2 | 14.2 | .018 |
| 39.985 | 300.078 | -2.65 | 76 | 1.9 | 75.972 | 75.981 | +9.0 | 7.6 | 16.6 | .021 |
| 39.985 | | -2.60 | 78 | 1.95 | 77.971 | 77.978 | +7.0 | 7.8 | 14.8 | .018 |
| 39.985 | | -2.55 | 78.8 | 1.97 | 78.770 | 78.779 | +9.0 | 7.9 | 16.9 | .021 |
| 39.985 | 300.075 | -2.50 | 79.2 | 1.98 | 79.170 | 79.184 | +14.0 | 7.9 | 21.9 | .027* |
| 39.985 | | -2.50 | 79.6 | 1.99 | 79.570 | 79.579 | +9.0 | 8.0 | 17.0 | .021 |
| 39.985 | | -2.50 | 79.8 | 1.995 | 79.770 | 79.782 | +12.0 | 8.0 | 20.0 | .025 |
| 39.986 | 300.083 | -2.50 | 79.9 | 1.9975 | 79.872 | 79.881 | +9.0 | 8.0 | 17.0 | .021 |

*This measured value is called the worst-case output error. When calculated using Eq. (1) and the values applicable to Eq. (3), the worst-case value is ±0.065 percent.

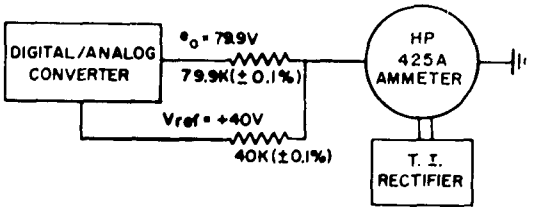



Fig. 9 - Full-output-drift test setup

calculate the voltage reference ($V_{ref}$) drift versus the -300 volt input to the voltage reference summing amplifier (Fig. 7). The voltage reference drifted 3 millivolts for a voltage input drift of 62 millivolts.

### Speed of Operation

The critical area limiting speed of operation was found to be the settling time required for a step change to reach its average measured value. Experimental results indicated that at least 20 microseconds were needed for a step change to reach its average measured value.

## CONCLUSIONS

Experimental results derived from an investigation of the characteristics of a diode switching circuit showed a maximum switching error of $\pm 6 \times 10^{-3}$ volts. Incorporation of this switch as input to a weighted resistor, 11-bit, digital-to-analog converter resulted in a calculated worst-case relative output error of 0.065 percent. Experimental measurements performed on the output of the converter resulted in a maximum relative output error of only 0.027 percent. The digital-to-analog conversion speed was limited by the time required for a step change to settle, which in this case amounted to 20 microseconds. The advantages of this design are its simplicity, guaranteed linearity, low relative output errors, and ability to control large changes of voltage while supplying relatively large output currents.

## ACKNOWLEDGMENT

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The weighted resistor can be used as the input to a summing amplifier, and the voltage input errors to

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2. Switching circuits - Errors
3. Switching circuits - Design

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The advantages of the diode switch as an auxiliary to the weighted resistor method are simplicity of design, guaranteed linearity of error, low relative output errors, and, in conjunction with the summing amplifier, the ability to control large changes of voltage while supplying relatively large output currents.

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