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SECOND QUARTERLY PROGRESS REPORT  
FOR  
MATERIAL PROCESSING AND PHENOMENA INVESTIGATION  
OF  
FUNCTIONAL ELECTRONIC BLOCKS  
CONTRACT AF 33(657)-9196

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1 December 1962 through 28 February 1963

Texas Instruments Incorporated  
13500 North Central Expressway  
Dallas 22, Texas

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**SUMMARY**

Work has proceeded as follows:

**Task I**

1. GaAs epitaxial deposition on GaAs in an open system is routine. The technology of SiO<sub>2</sub> masking against deposition is under control.
2. Diffusions from SiO<sub>2</sub> films into GaAs have produced very flat junctions.

**Task II**

1. GaAs epitaxial depositions in a closed system are semi-routine.
2. A study of high resistivity mechanisms, voltage breakdown across thin layers, and maximum component packing density has started.

**Task III**

1. Materials preparation of single crystal CdS, both pure and doped, is routine.
2. Ohmic and some diodic contacts to CdS have been developed.
3. Technology for etching, shaping, diffusion, etc. is becoming routine.

Task IV

1. Epitaxial depositions of GaAsP by phosphorus diffusion and by vapor deposition have become routine. Phosphorus diffusion gives material varying from GaP to GaAs. Vapor deposition has covered the range GaAs to GaAs<sub>0.6</sub>P<sub>0.4</sub>.

2. Light-producing diodes have been made from GaAs<sub>0.6</sub>P<sub>0.4</sub> ( $\lambda = 6700 \text{ \AA}$ ) and GaAs<sub>0.9</sub>P<sub>0.1</sub> ( $\lambda = 8200 \text{ \AA}$ ). These are forward-biased injection EL diodes.



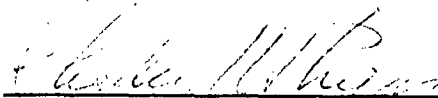
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I. WORK STATEMENT OF THE CONTRACT

Research efforts are as follows:

1. Use of high resistivity GaAs as a substrate for functional electronic blocks.
2. Investigation of problems associated with three dimensional arrays.
3. Investigation of phenomena (particularly photon-induced actions) in II-VI compounds as amenable to further functional electronic block designs.
4. Investigation of GaP and GaAsP epitaxial growth with various doping agents for electroluminescent devices.

## II. DESCRIPTION OF TASKS

### A. Task I - High Resistivity GaAs Substrates

In this quarter, we have concentrated on

1. Epitaxial deposition of GaAs on GaAs,
2. Masking and diffusion techniques applicable to FEB's,
3. To a lesser extent, silicon epitaxial films.

The proposed objectives for Task I are more than 50% complete. No difficulty is expected to prevent successful completion of the task.

#### Silicon Epitaxial Films

The problems expected in depositing epitaxial silicon on GaAs are

1. The dissociation pressure of GaAs is appreciable at the temperature necessary for good silicon deposits.
2. The halides present during the usual deposition of silicon would act as a corrosive agent on the GaAs.

We decided to deposit silicon by an electron beam evaporation process. The cleanliness and control of the system are great advantages over the halide system. We felt it worthwhile to attempt to deposit a thin layer of silicon which would seal the surface of the GaAs substrate. Further deposition might then be made at a higher temperature without GaAs dissociation.

The equipment and special apparatus were constructed and assembled during this quarter. All preliminary tests have been completed, and we have made a number of depositions of silicon on glass substrates. During the next quarter, depositions will be made on GaAs substrates.

Because of the success of our GaAs operations, we have tried to deposit GaAs on silicon. If the GaAs layer is deposited high resistivity, it can act as the substrate in a functional electronic block application. The silicon would then be considered the active layer. This approach avoids the difficulties described above for silicon deposition and allows one to

choose directly the physical properties of the active layer. Our attempts, using the apparatus described below, have been unsuccessful so far. We believe a surface layer of  $\text{SiO}_2$  is preventing deposition.

### GaAs Epitaxial Films on GaAs

We have developed a routine method of producing epitaxial films of GaAs on GaAs, using a flow system. We have the technology of masking selectively against deposition to produce an epitaxial array. The epitaxial deposition does not affect the high resistivity properties of the substrate.

The apparatus is shown in Fig. 1. All our runs to date have used GaAs as feed material. The hemispherical cross section in the deposition area permits deposition on one side only. Cooling air or some other heat sink can be used to control deposition at the substrate only, though we have not found that necessary.

The substrate is prepared from a (111) slice of GaAs. Our chemical polish ( $\text{H}_2\text{SO}_4 - \text{H}_2\text{O}_2$ ) gives a preferential polish on the B, or arsenic, face; most of our depositions have been made on that face. During a typical run, the seed is chemically etched at  $750^\circ\text{C}$  in the  $\text{H}_2 - \text{AsCl}_3$  stream for a few minutes. Then the source temperature is brought up to  $900^\circ\text{C}$ , and deposition proceeds at about  $2\mu/\text{hr}$ . The entrant gas stream is about 0.7 mm  $\text{AsCl}_3$  pressure in one atmosphere total pressure. Under these conditions, a very uniform epitaxial deposit is produced.

We have tried to evaluate precisely the thickness of the deposit by either gold plating or electrical probing. When the substrate was high resistivity and the deposit low resistivity n-type, gold could usually be plated on the deposit from an alkaline gold cyanide solution. Some samples were angle-lapped and probed electrically to determine where the high resistivity - low resistivity boundary was. These two techniques did not completely satisfy us, since there is a remote possibility that the boundary might migrate during deposition and no longer represent the place where

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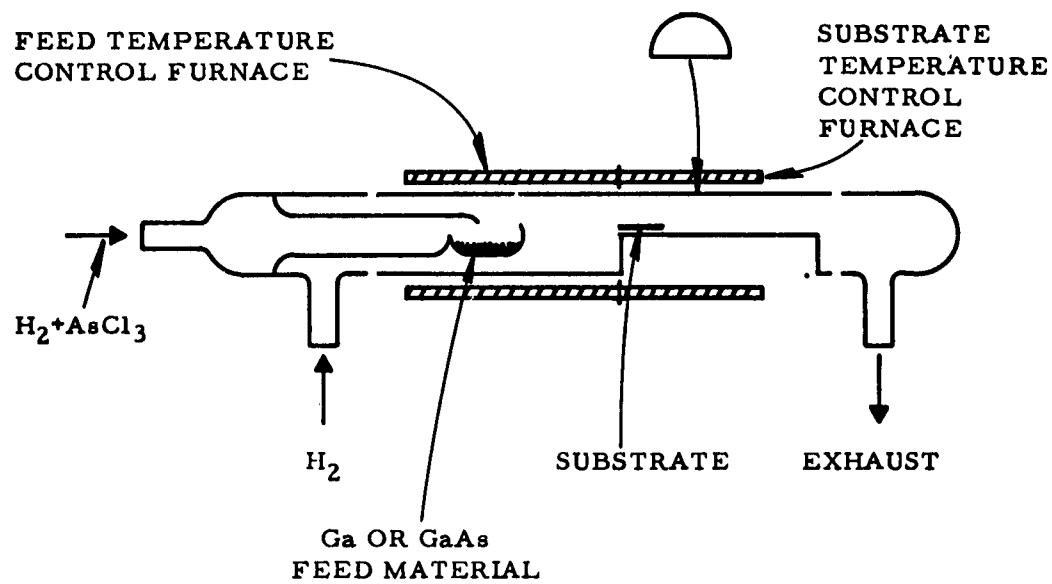


Fig. 1 Apparatus for epitaxial deposition of GaAs.

This difficulty has been solved by using  $\text{SiO}_2$  as a mask against deposition. Our first attempts consisted of a stripe pattern of  $\text{SiO}_2$  on the surface of the polished GaAs. After deposition, which occurred only on the areas free of  $\text{SiO}_2$ , the sample was angle-lapped and gold-plated. It was possible to correlate the three methods, electrical probing, gold plating and visual examination. No boundary movement could be detected to  $< 0.1\mu$ .

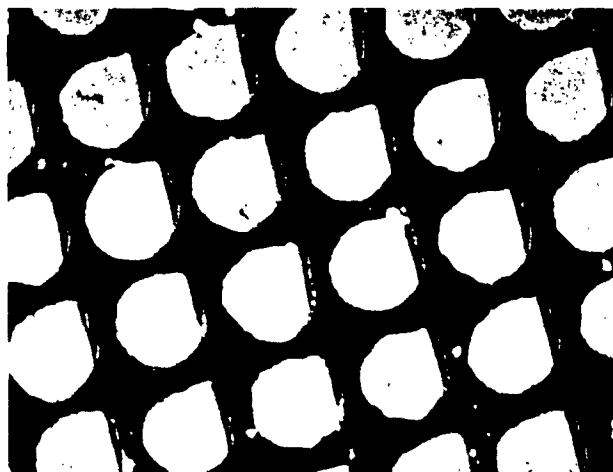
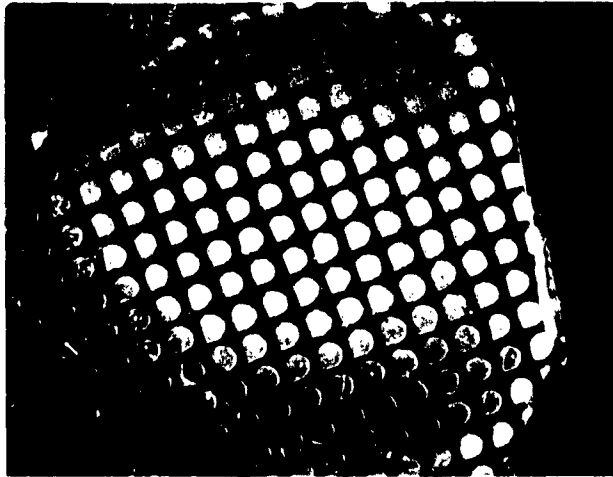
These experiments have led us to try depositing arrays of epitaxial GaAs. Figure 2 shows such a deposit. Each spot of GaAs is single crystalline; each shows facets precisely lined up with all other deposits. We feel that we have the deposition and masking technology under good control.

The attempts to deposit on the A, or gallium, face have not been successful; the deposits are polycrystalline. The faces have been mechanically polished in past experiments. We will try the chemical method in the next quarter. One deposition was made using a (100) substrate. The rate was twice as fast as seen for (111) deposition. We plan to continue to investigate other crystal orientations.

#### Evaporated Passive Elements, Masking and Diffusion

During this quarter we completed the work required to show feasibility of passive elements on GaAs substrates. We have developed a masking and diffusion technology which will prove satisfactory for making active circuit elements and diffused passive circuit elements.

In the First Quarterly Report we described the resistors and capacitors prepared by vacuum deposition of metals and dielectrics. In general, the techniques are standard with any changes which might be dictated by use of GaAs as the substrate. In this quarter we made a series of runs to prepare capacitors and analyzed them for uniformity.



**Fig. 2 GaAs Epitaxially Deposited Array.**

The capacitors were made by alternate  $\text{SiO}_x$  and Al evaporation at  $200^\circ\text{C}$  on chemically polished GaAs (111) slices. We chose arbitrary thicknesses of  $3000 \text{ \AA}$  for the Al and  $5000 \text{ \AA}$  for the  $\text{SiO}_x$ . A base layer of  $\text{SiO}_2$   $4000 \text{ \AA}$  thick was sputtered on the GaAs. For 15 functional units, the capacitance was  $10.15 \pm 0.10$  nanofarads/cm<sup>2</sup>. This passive element technology is available when needed to fabricate functional electronic blocks.

The lack of a good diffusion system for GaAs has seriously hampered the development of suitable devices. This lack has been particularly detrimental to development of sophisticated devices where we require close control on concentrations of impurities and device dimensions. GaAs starts chemical dissociation at about  $650^\circ\text{C}$ , so the usual method for diffusion has been to seal diffusant and GaAs in a small volume ampoule. The small volume limits the amount of dissociation, but diffusion control and chemical purity are problems. Some diffusions have been made through a  $\text{SiO}_2$  film deposited on the GaAs. Better control of both diffusion and purity is possible. We have found that diffusion of a dopant from a  $\text{SiO}_2$  film on GaAs gives excellent control of the diffusion and chemical purity and also produces junctions which are extremely flat.

All our experiments have used zinc as the dopant. In general, a  $\text{SiO}_2$  plus zinc film is deposited on a chemically polished GaAs substrate. The films analyze 2 to 3 times as much zinc as  $\text{SiO}_2$  and are roughly  $7000 \text{ \AA}$  thick. (It is possible, of course, to predeposit a  $\text{SiO}_2$  film and cut windows by standard techniques to select the spots where the zinc diffusion will occur.) Diffusions are made in a forming gas or hydrogen atmosphere at  $900^\circ\text{C}$ .

A large number of runs have been made for purely mechanical reasons, that is, to check the deposition rate and the chemical analysis, and to evaluate and optimize all factors with respect to the diffusions. Angle lapping at  $1^\circ$  and electrolytic staining with 10% KOH solution has been used to study the planarity of the junctions. Visual microscopic examination indicates that the junctions are far superior to those prepared by previous diffusion methods.

Table I shows the data available thus far on these diffusions. Because the sheet resistivities remain relatively constant with depth, the diffusion acts as a limited source type. The one- and three-hour diffusions appear to give the same junction depth. These data will be rechecked. Some of the material from Run 11 was used to make GaAs lasers. Another sample of the same bulk material was diffused with zinc by the method used in our previous work. (This laser evaluation of our material and technology was done under Contract # AF 33(657)-9824.) We found that material from our newer diffusion method gave lasers with threshold currents as much as a factor of 10 lower than the previous material. It is generally accepted that laser action depends upon planarity of the junction. These data indicate we have achieved a significant advance in making junctions.

Much of the work discussed above is preliminary and has not yet been applied to the epitaxial material. Further studies and applications will be made in the next quarter.

#### B. Task II - Three Dimensional Arrays

This task requires production of epitaxial high resistivity GaAs layers which can be used to insulate circuit elements from each other vertically while allowing the vertical production of additional epitaxial layers. We have emphasized a closed tube epitaxial deposition which we think will give the closer control necessary to get precisely doped high resistivity layers. The system has produced good epitaxial deposits and we are ready to try doping to high resistivity. We are also studying the mechanisms responsible for high resistivity to:

1. Optimize the material for this and other tasks;
2. Identify the processes which cause breakdown between adjacent circuit elements separated by thin films of high resistivity GaAs;
3. Determine the maximum packing density for functional electronic blocks limited by these voltage breakdowns.

Table I

Diffusion Data for Zn-SiO<sub>2</sub> Films at 900°C

<u>Run</u>	<u>Time (hrs)</u>	<u>Atmosphere</u>	<u>Sheet Resistance (<math>\Omega</math>/square)</u>	<u>Junction Depth (microns)</u>
1	3	Forming Gas	0.1	3 - 4
2	3	Forming Gas	--	3.8
3	1	Hydrogen	50	5.0
4	1	Hydrogen	62	3.8
5	1	Hydrogen	50	5.0
6	1	Hydrogen	62	3.8
7	3	Hydrogen	--	3.4
8	3	Hydrogen	--	3.2
9	2 <sup>(a)</sup>	Hydrogen	60	5.0
10	24	Hydrogen	61	7.3 <sup>(b)</sup>
11	32	Hydrogen	56	8.9
12	32	Hydrogen	55	8.8

(a) Slow-cooled 900°C → 400°C in 2-1/2 hours.

(b) Part of this run used to make GaAs laser.

### Epitaxial Deposition of High Resistivity GaAs

Haisty, Mehal and Stratton<sup>1</sup> have proposed a mechanism using zinc plus oxygen to achieve high resistivity GaAs. The flow system for epitaxial deposition described under Task I cannot give the control necessary to dope with both zinc and oxygen. Therefore, we have adopted a closed system, similar to one described by Holonyak,<sup>2</sup> for our work.

The bomb tubes are 10 cm x 1 cm diameter quartz containing a GaAs seed, 0.5g GaAs, 0.05g arsenic and a sealed ampule of AsCl<sub>3</sub>. After the bomb is evacuated to  $5 \times 10^{-5}$  mm and sealed, the AsCl<sub>3</sub> ampule is broken to release the AsCl<sub>3</sub>. The seeds are n-type GaAs slices, either (111) mechanically polished (alumina) or ( $\bar{1}\bar{1}\bar{1}$ ) chemically polished. The GaAs source is held at 900°C, and a run lasts from 2 to 6 hours. The data on runs to date are summarized in Table II. The successful deposits on the (111) face show some unevenness because of a thermal gradient, but the deposit is single and thick enough to evaluate. These results satisfy the first part of this task and we are ready to try the doping experiments necessary to get the high resistivity.

### High Resistivity GaAs Technology

The entire subject of high resistivity GaAs is complicated by the many ways the material can be produced. Zinc plus oxygen doping, copper doping, arsenic vacancies, and other methods have been suggested for its preparation. In many cases, high resistivity GaAs appears spontaneously while attempts are being made to prepare high purity GaAs. High resistivity material prepared at different times will show wide variations

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<sup>1</sup> R. W. Haisty, E. W. Mehal and R. Stratton, J. Chem. Phys. Solids **23**, 829 (1962).

<sup>2</sup> N. Holonyak, Jr., D. C. Jillson and S. F. Bevacqua, "Metallurgy of Semiconductor Materials," J. B. Schroeder, Editor, (Interscience Publishers, New York, 1962), p. 52.

Table II

GaAs Deposition - Closed System

<u>Run</u>	<u>AsCl<sub>3</sub> (mg)</u>	<u>Seed Temp. (°C)</u>	<u>Reaction Time (hrs)</u>	<u>Orientation</u>	<u>Remarks</u>
116A	65	700	4	(TTT)	Poly
116B	65	725	4	(TTT)	No deposit
116C	55	650	4	(TTT)	No deposit
116D	35	750	4	(TTT)	Poly
118A	55	775	2	(TTT)	No deposit
118B	55	775	4	(TTT)	Poly
118C	55	775	6	(TTT)	No deposit
119A	50	775	2	(111)	Single
119B	50	775	2	(111)	Single

in properties such as resistivity and voltage breakdown in thin layers. The variations are not readily identifiable with specific chemical impurities.

Texas Instruments has a wide range of samples of high resistivity material, many prepared before the present contract. We have measured the thermally stimulated currents in some of these samples and plan also to make photo-Hall measurements when the apparatus becomes available. Our objective is to identify the various physical phenomena with specific impurities.

Thermally stimulated current measurements can identify the energy level and concentration of deep-lying impurities. A sample is cooled to liquid nitrogen temperature and saturated with white light to produce carriers and fill the deep levels. The light is removed and the dark current is measured as a function of temperature. The temperature identifies the energy level, and the area under the current vs temperature curve gives the concentration at that level. The system is similar to that described by Bube.<sup>3</sup>

Several samples of high resistivity GaAs have been examined. The results so far indicate;

1. Zinc plus oxygen high resistivity material had levels at 0.2 eV, 0.4 eV (strongest), 0.5 eV and 0.56 eV above the valence band edge. Resistivity vs temperature indicated a level at 0.76 eV.
2. Iron diffusion gave levels at 0.09 eV and 0.42 eV by resistivity vs temperature, and 0.15 eV and 0.42 eV by thermally stimulated current.
3. Further work has not shown whether iron produces the 0.42 eV level or removes a deep acceptor to reveal this level. The problem is complicated by the random changes in type and charge concentration which result from the annealing of the samples after diffusion.

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<sup>3</sup> R. H. Bube, J. Appl. Phys. 31, 315 (1960).

These results are preliminary and will require continuing effort to yield satisfactory conclusions. For example, a fairly high resistivity GaAs can be obtained now by iron diffusion, but a much higher resistivity can be obtained by doping to produce the 0.76 eV level.

#### Breakdown in High Resistivity Layers

Measurements have been started on thin GaAs slices to see if the voltage at which the current suddenly increases by several orders of magnitude varies as the square of the thickness. This is the "traps-filled-limit" voltage of Lampert.<sup>4</sup> Indium-tin dots are alloyed on a thin slice, the dark current-voltage curve is plotted, and the sample is lapped to a thinner dimension; new dots are alloyed, and the process is repeated. Only one sample has been measured thus far.

<u>Thickness</u>	<u>Breakdown Voltage</u>
1150 microns	450 (limit of voltage supply)
670 microns	200
460 microns	150

These results show the voltage is not changing as the square of the thickness and appears to be about  $3000 \text{ V cm}^{-1}$ . Other workers<sup>5</sup> have reported values as low as  $200 \text{ V cm}^{-1}$ .

An expanded discussion of this important problem and its implications for layered structures appears in Appendix A.

#### C. Task III - II-VI Photo Effect Devices

During this quarter we have emphasized primarily the materials and technology aspects under this task. We have made excellent progress in the

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<sup>4</sup> M. A. Lampert, Phys. Rev. **103**, 1648 (1956).

<sup>5</sup> J. W. Allen and R. J. Cherry, Nature **476**, 297 (1961).

material available and the materials handling processes. It has become apparent that the materials problems, and particularly the contact problems, are limiting the application of devices.

#### Materials and General Technology

We are now routinely preparing high quality CdS, both pure and copper-doped at various levels. The continuing success of our project depended on control of the material to be used. We have described our processes and the material characteristics in more detail in Appendix B. These methods will be usable for other II-VI compounds, as well.

The general objective of this task was to prepare circuit elements and electronic functions in CdS. The high resistivity available was to isolate the circuit elements and the photo-response of the material was to activate the various circuit functions. The copper-doped CdS crystals now available have resistivity of  $10^{12}$  ohm cm and show a change of more than  $10^8$  in conductivity when illuminated with white (incandescent) light.

With large single crystals of CdS available we have developed etches for cleaning the surface and polishing. Surface treatment of CdS has been of little general interest or importance in the past; consequently, we developed many of the treatments without the aid of precedents. We are using a shallow indium diffusion to reduce the surface resistivity and increase the light sensitivity. This technique will allow us to establish current-carrying paths in the surface of high resistivity CdS, copper-doped crystals. Current paths can be defined either indium deposition and diffusion through a mask or masking and etching the surface after diffusion.

One of the most pressing problem areas is that of contacts, particularly diodic and blocking contacts. Using indium, either evaporated or evaporated and diffused, as ohmic contacts has proved satisfactory. The contacts are non-rectifying and low resistance for either pure CdS or CdS:Cu.

- Diodic contacts of tellurium which exhibit good rectification ratios have been made on pure CdS. Both evaporated and diffused contacts have been

tested; the latter are suitable and are more rugged. However, since we have been using the high resistivity CdS:Cu, no attempt to prepare a good diodic contact has succeeded. In addition, the blocking contacts, used in the gate of the field effect transistor and in the capacitor, have shown large leakage currents. Further improvement of the devices depends upon better contacts for the particular operation desired. To a large extent, we have used device fabrication to evaluate the progress of our contact studies.

#### Photo Variable Devices

A number of capacitors have been constructed. Figure 3 shows the device construction and evaluation. The capacitance change is much less than expected and shows an unexpected change with frequency. However, use of our newer material has increased the capacitance change to a factor of two, compared to a few percent change reported in the previous quarterly report. With the single crystal boules which we are now producing, the actual device preparation is greatly simplified.

No great improvements have been made in the field effect transistor. Figure 4 shows the configuration and evaluation of a recent sample used to test the gate contact. As indicated in the First Quarterly Report, the preparation of diodes and resistors is under satisfactory control.

The circuits in which these elements will be used are being considered. We have plans to build a photodiode bridge circuit using CdS:Cu as a substrate and either photomasking or selective diffusion to form the circuit elements. It has become apparent that some invariant circuit elements will be needed; we expect to start work on these in the next quarter.

#### D. Task IV - GaAsP and GaP for Epitaxial Devices

As described in the previous quarterly report, we have started preparation of the materials along these lines:



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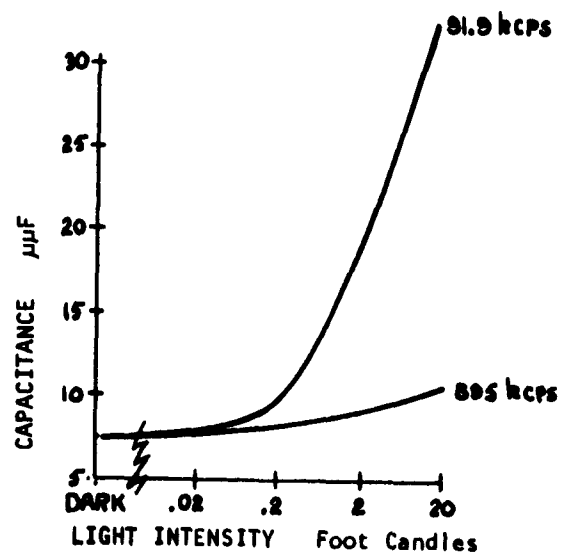
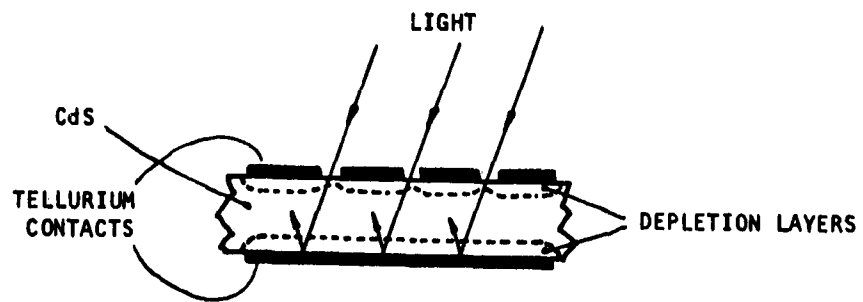
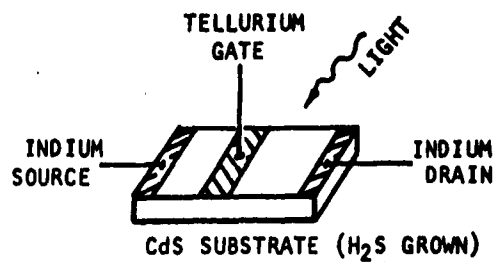
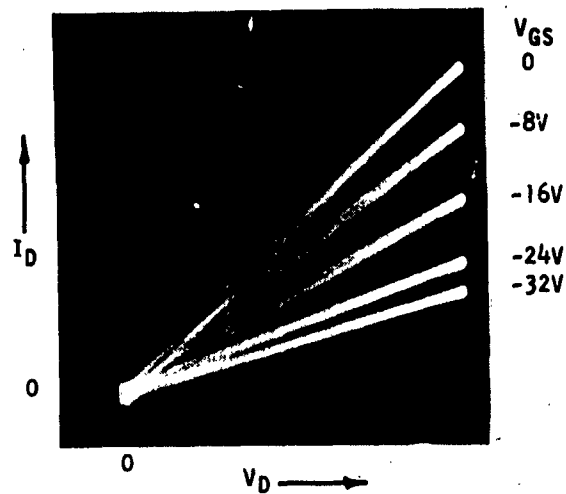


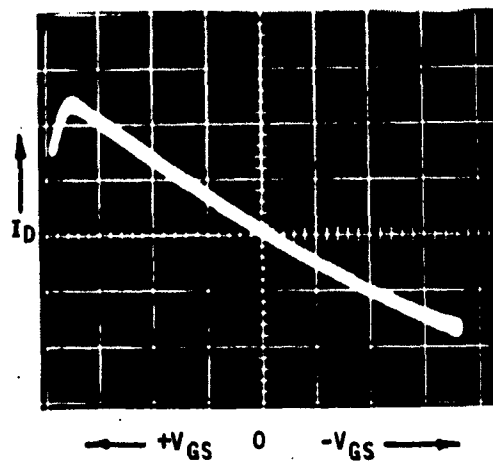
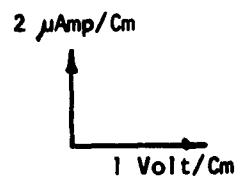
Fig. 3 Photocapacitor, Showing Construction and Variation of Capacitance with Light Intensity and Frequency of Operation.



CdS PHOTO FIELD EFFECT TRANSISTOR



DYNAMIC DRAIN RESISTANCE



TRANSCONDUCTANCE

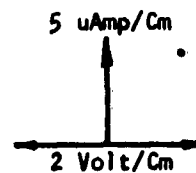


Fig. 4 Field Effect Transistor Showing Construction and Electrical Evaluation

1. Diffusion of phosphorus into GaAs,
2. Vapor deposition of GaAsP or GaP.

The preparation of bulk GaP or GaAsP with a high percentage of phosphorus is difficult because of the high temperatures and high vapor pressure of phosphorus required for equilibrium. We feel that suitable GaP or GaAsP for various devices can be made by epitaxial vapor deposition or diffusion as described below. These two methods are relatively simple with respect to equipment and technology, and the former allows good control of the final product.

During the past quarter we produced GaAsP layers up to 25 microns thick by phosphorus diffusion. The composition varies from GaP on the surface to GaAs in the bulk of the substrate. We have deposited epitaxial  $\text{GaAs}_x\text{P}_{(1-x)}$  layers on GaAs substrates by vapor deposition with  $x$  varying from 1.0 to 0.6. We have prepared injection electroluminescent devices which produced wavelengths as short as 6700 Å. We expect to extend our composition to pure GaP in the next quarter. This task of the contract is on schedule, and no difficulties are foreseen in completing contract obligations.

#### Phosphorus Diffusion

The problems with oxygen described in the previous quarterly report have been overcome in producing GaAsP layers on GaAs. We used high purity phosphorus, 99.999%, which had been prepared under conditions to exclude oxygen. All bomb loading operations were performed in an oxygen-free dry box. Preparing GaAsP layers is now a routine operation.

We have extended the diffusion conditions up to 1000°C for 65 hours. An estimated phosphorus pressure of 25 atmospheres is in the bomb tube in a normal run. Under these conditions, the GaAsP layer is 25 $\mu$  thick and is n-type. The substrate is tellurium-doped (111) GaAs at  $10^{17} \text{ cm}^{-3}$ ; its bulk properties do not change during the diffusion experiments.

Initial runs were air-quenched, i.e., rapidly cooled. X-ray examination of the deposit showed a strong indication of a (220) deposit or layer on the (111) GaAs substrate. Alloyed diodes have been made in these quenched layers and often show a high breakdown in both forward and reverse directions. (The diodes were prepared by alloying a gold-zinc wire to the deposit; ohmic contact was made to the GaAs bulk. An occasional diode shows a low forward voltage drop, though higher than the usual GaAs diode because of the greater band gap of the GaAsP.) This high forward drop could have resulted from a material discontinuity. Figure 5 shows a layer grading from pure GaP on the surface to pure GaAs in the bulk. A definite discontinuity can be seen. Slow cooling the diffusion tubes after the run relieved the problem somewhat but did not solve it. It is difficult to understand the process leading to an apparent discontinuity when the gradation of composition is so gradual.

X-ray analysis of the deposits has been our primary tool in evaluating our work. We have found evidence for all compositions of the ternary compound in the diffused layer. Further analysis has indicated a relatively linear gradation of phosphorus, from 100% on the surface to 0% at the discontinuity in the bulk. Its exact interpretation has not yet been determined.

A number of attempts have been made to form a junction by diffusing zinc into the layer. In general, a layer of  $\text{SiO}_2$  about 4000 Å thick was put on the GaAsP layer and zinc diffused through at 600°C for 1-2 hours. (This is our old zinc diffusion method; we have not yet tried the  $\text{SiO}_2$  plus zinc film method.) In all cases, the zinc diffused completely through the GaAsP, as though it had a surface concentration too high by a factor of 100. Irregularities on the surface of the GaAsP layer after the diffusion caused this behavior. The surfaces of the slices appear vigorously etched. The  $\text{SiO}_2$  film then deposited could not be very homogeneous and probably contained pin-holes through which the zinc diffused rapidly. We tried lapping the GaAsP layer before depositing the  $\text{SiO}_2$  film for the zinc diffusion. The zinc now behaves properly, giving an apparent surface concentration of  $10^{17} \text{ cm}^{-3}$ . We expect, of course, to apply our new zinc diffusion technology to this system.

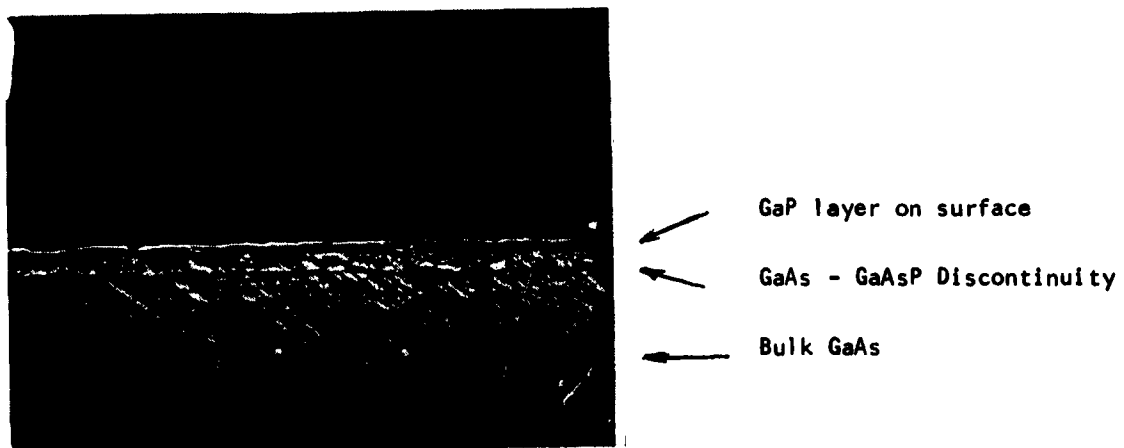


Fig. 5 Diffused GaAsP Layer on Bulk GaAs. The Layer is Approximately 18 Microns Thick.

### Epitaxial Vapor Deposition

The epitaxial deposition of GaAsP on GaAs substrates has become a routine operation. We have covered the range of compositions from GaAs to  $\text{GaAs}_{0.6}\text{P}_{0.4}$  with the apparatus described in the First Quarterly Report. We have broadened the capabilities of the apparatus as follows:

1.  $\text{AsCl}_3$  and/or  $\text{PCl}_3$  can be used as the halide species.
2. Either Ga or GaAs can be used as the source material for deposition.

With these changes we have deposited all compositions of GaAsP, but the deposits have not been epitaxial above 40% phosphorus. We have not attempted to prepare GaP for use as a source material for further epitaxial depositions since our present apparatus seems to satisfy all requirements. In the past quarter we have satisfied most of the material requirements under the contract and can now emphasize device requirements.

The GaAsP deposition takes place at  $750^\circ\text{-}850^\circ\text{C}$  with a source temperature of  $860^\circ\text{-}1000^\circ\text{C}$ . The gas stream contains the  $\text{AsCl}_3\text{-PCl}_3$  ratio needed for the deposition desired in the particular experiment. The seed is pre-etched with pure hydrogen at deposition temperature and is then etched with the halide stream. Seeds have been (111) slices of n-type GaAs, and we prefer to deposit on the A or  $(\bar{1}\bar{1}\bar{1})$  face. The deposit is n-type.

To evaluate our first runs, for expediency we made alloyed diodes in the deposit, using zinc to give the alloy. Light was produced in the junction area when the diode was reverse-biased. Breakdown voltage was about 6 volts. Light appeared as a myriad of microscopic spots around the junction area. Forward bias with currents to 100 mA did not produce light. As more material became available, we tried a zinc diffusion into the GaAsP layer.\*

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\* Much of the work described for the EL diodes was possible through the assistance of personnel working on Contract AF 33(657)-9824.

Simple ohmic contacts were made to the p-type GaAsP layer and to the n-type bulk GaAs. The diodes, biased in a forward direction at about 100 mA, gave visible red light at room temperature. Figure 6 shows the emission of the diode. The light is much brighter at lower temperatures. A major peak at about 6700 Å represents the recombination process approximately across the band gap. Figure 7 gives the emission vs wavelength. The transition at 8750 Å is approximately that seen for GaAs diodes, and that at 12,700 Å is also very often seen in GaAs diodes. The exact origin of these energy transitions is not clear.

The main transition at 6700 Å represents a band gap of 1.8 eV or a composition of GaAs<sub>0.6</sub>P<sub>0.4</sub>. X-ray analysis of the material agrees with this value. Other compositions have been prepared, and we have made diodes from GaAs<sub>0.9</sub>P<sub>0.1</sub> which emit light at about 8200 Å. It appears possible to prepare material with all intermediate compositions and prepare light bulbs which emit anywhere in the region 8700 Å (GaAs) to 6700 Å.

We have prepared one deposit thick enough for direct electrical evaluation. The composition was GaAs<sub>0.85</sub>P<sub>0.15</sub> and the substrate was lapped away. At room temperature, the material was n-type and had  $1.4 \times 10^{17}$  carriers/cm<sup>3</sup> and mobility of 1200 cm<sup>2</sup>/volt sec. These figures represent low to medium purity and point out the necessity for considerable improvement in chemical purity in the deposition system.

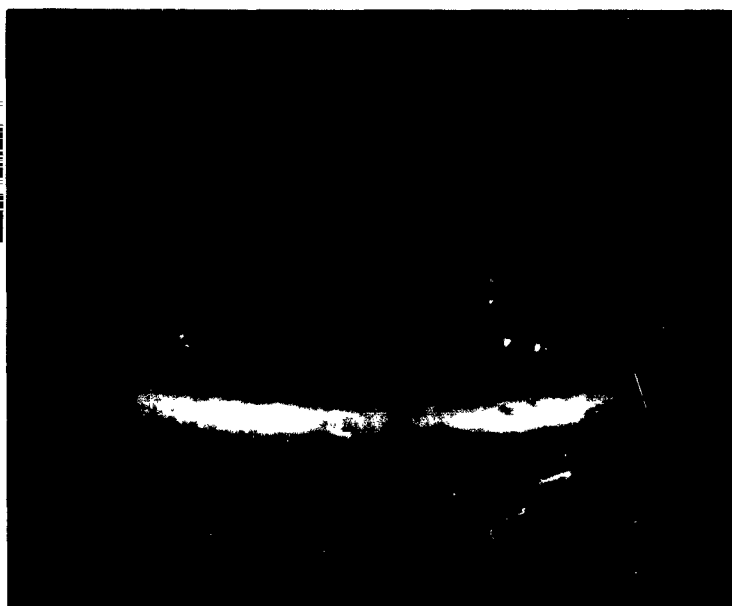
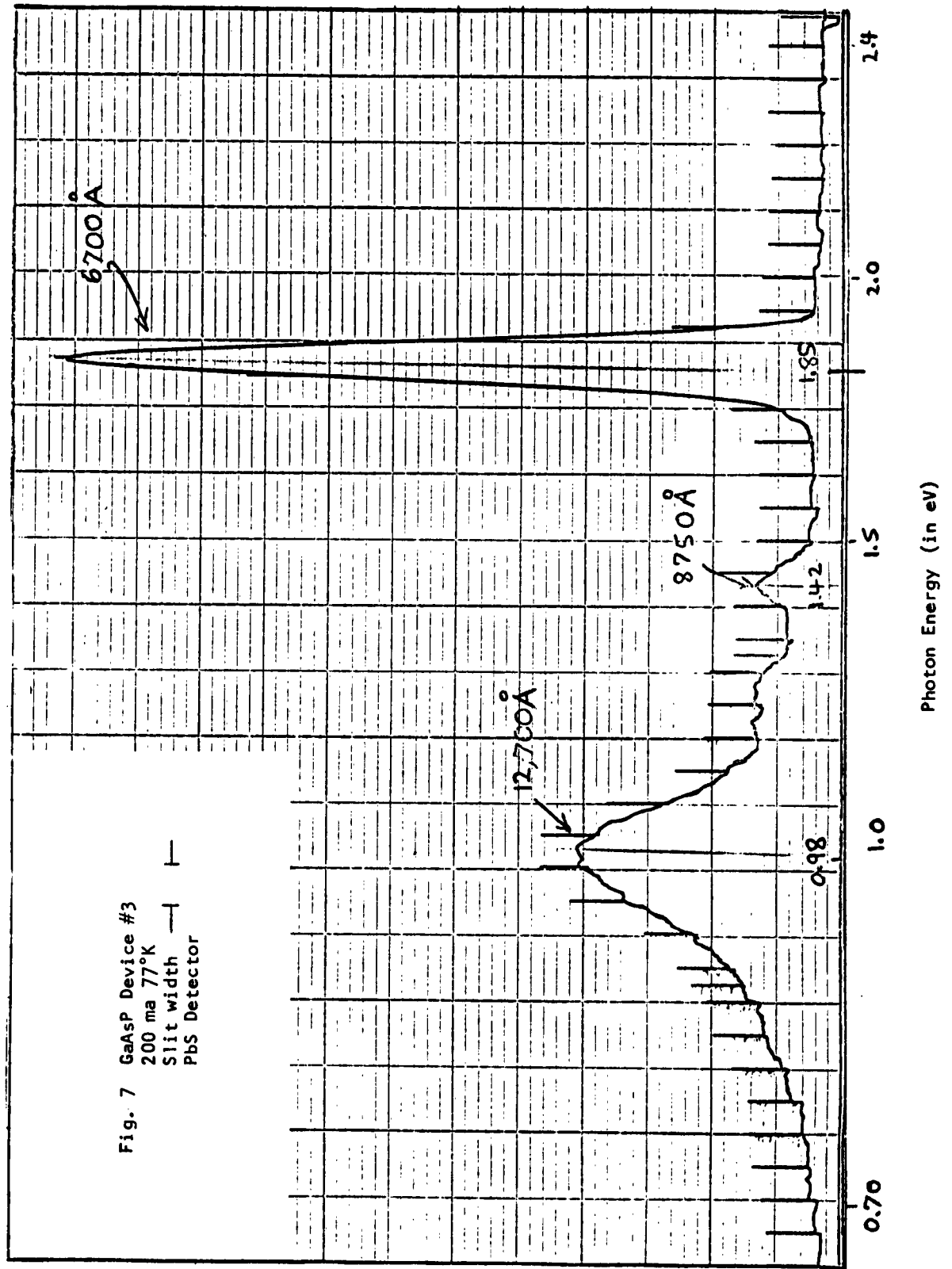


Fig. 6 Light emitted from GaAs<sub>0.6</sub>P<sub>0.4</sub> at a diffused junction at 25°C. The diode is forward-biased. The radiation is about 6800 Å.



### III. PLANS FOR NEXT PERIOD

#### A. Task I

1. Prepare active and inactive circuit elements by diffusion into epitaxial GaAs.
2. Deposit silicon on GaAs.
3. Deposit both doped and higher purity GaAs epitaxial layers.

#### B. Task II

1. Deposit doped GaAs layers for high resistivity.
2. Continue study of high resistivity mechanisms.

#### C. Task III

1. Continue studies on contacts, particularly diodic and blocking.
2. Prepare a simple circuit employing photo-variable diodes.

#### D. Task IV

1. Extend composition range of epitaxial deposition to GaP.
2. Improve purity of GaAsP deposits.
3. Resolve difficulties of diffusion experiments which cause discontinuity at GaAs-GaAsP interface.

### IV. CUMULATIVE PERCENT COMPLETION

This contract is 32% complete.

APPENDIX A

VOLTAGE BREAKDOWN IN HIGH RESISTIVITY GALLIUM ARSENIDE

by

R. W. Haisty

## APPENDIX A

### VOLTAGE BREAKDOWN IN HIGH RESISTIVITY GALLIUM ARSENIDE

#### ABSTRACT

Low-field breakdown in small thicknesses of high resistivity gallium arsenide can greatly limit its usefulness as an insulator between closely stacked functional layers, especially if the breakdown voltage varies as the thickness squared. If the breakdown is the transition to the trap-free Child's law current, occurring at the traps-filled-limit voltage, the way to raise the breakdown voltage is to increase the trap concentration. However, the published trap concentrations calculated from the traps-filled-limit voltage are orders of magnitude lower than the concentrations determined by other methods. It is important to determine the concentration of both the electron and hole traps in comparing traps-filled-limit determinations with other measurements.

Measurements of breakdown voltages in one sample indicated that only the electron trap concentration is very low. The hole trap concentration is much higher; the voltage breakdown point for hole injection is high enough that the material can be used as insulation between p-type layers.

A possible explanation for the low electron trap concentration is given. If it is correct, then it should be possible to increase the electron traps by either increasing the total acceptor concentrations or decreasing the concentration of shallow donors in high resistivity GaAs.

It is not certain that the breakdown is, in fact, simply the traps-filled-limit transition. Preliminary measurements of the breakdown voltage vs thickness showed a  $t^{1.3}$  variation rather than the  $t^2$  dependence expected for the traps-filled-limit voltage, which suggests that a combination of effects is involved.

## VOLTAGE BREAKDOWN IN HIGH RESISTIVITY GALLIUM ARSENIDE

### INTRODUCTION

High resistivity gallium arsenide can be obtained in several ways<sup>32,41-45</sup> and samples from various sources have shown large differences in electrical properties. This kind of material is important for new types of devices (e.g., double injection diodes<sup>21-23</sup>); however, we are mainly concerned here with the properties which relate to the use of high resistivity GaAs as an insulator. Although GaAs can be made into satisfactory insulating substrates, it is clear that not all high resistivity GaAs is suitable.

Allen and Cherry<sup>1</sup> have described space-charge measurements on two samples of GaAs. In one case, for a sample about 0.15 mm thick, the "traps-filled-limit voltage" (Lampert<sup>24</sup>) at which the transition from ohmic to space-charge current occurred was 60 volts. This material would be suitable for insulation between circuit layers in many cases. However, the transition to space-charge limited current was complete at about 3 volts in the other 0.12 mm sample. In the latter case, the apparent resistance changed from  $5 \times 10^7$  ohms in the ohmic region (at 0.5 volt) to about  $1 \times 10^3$  ohms at 3 volts.

If we assume conditions to be such that the transition does, in fact, represent the traps-filled-limit, then in Lampert's simplified theory<sup>24</sup>, the transition voltage depends linearly on the density of traps,  $N_t$ , in the material:

$$V_{TFL} = \frac{e t^2 N_t}{2 \epsilon} \quad (1)$$

Allen and Cherry<sup>1</sup> used this equation to calculate an unfilled trap density of  $8 \times 10^{10} \text{ cm}^{-3}$  for the 3-volt transition and  $3.8 \times 10^{12} \text{ cm}^{-3}$  for the 60-volt transition. (Evidently the fact that the ratio of trap densities is not 20, as expected from the voltage, is due to a slight unspecified difference in thickness,  $t$ , which enters Eq. 1 as  $t^2$ .)

Pursuing this line of reasoning, it seems clear that the thing to do to improve the insulating capability of the material is to increase the content of unfilled traps. We note, however, that these trap concentrations in the range  $10^{12} \text{ cm}^{-3}$  are several orders of magnitude lower than the trap concentrations determined by other measurements such as thermally stimulated emission<sup>33</sup> and photo-Hall effect measurements<sup>34,35</sup> on high resistivity GaAs.

A similar situation exists for CdS. Böer, et al.,<sup>26</sup> found that the portion of defect centers which could be determined by glowcurve, or thermally stimulated measurements, had essentially no effect on the punch-through voltage. Thus, it appears that supplying additional unfilled traps to raise the traps-filled-limit voltage is not a simple matter. It is our purpose here to discuss in some detail the application to this problem of existing models for space-charge-limited currents in insulators with traps, to suggest some experiments for checking certain aspects of this theory, and to present a few preliminary results from the experiments.

#### TECHNICAL DISCUSSION

When electrons or holes are injected into an insulator, quite large space-charge-limited (SCL) currents can be expected. Mott and Gurney<sup>39</sup> pointed this out about 1940, and since then current-voltage characteristics which can be interpreted in terms of SCL current have been observed in a large number of insulating and semi-conducting materials (CdS, ZnS, Ge, Si, GaAs,  $\text{As}_2\text{S}_3$ , I).

Shockley and Prim<sup>2</sup> showed theoretically that a current density analogous to Child's law should be obtained with an n-i-n semiconductor structure. This was verified experimentally by Dacey<sup>3</sup> using highly purified germanium to form the n-i-n structure.

Rose<sup>19</sup> treated SCL currents in insulators with and without traps; Lampert<sup>24</sup> introduced a simplified theory for SCL currents in an insulator

with traps, in which he showed that there are three regions of interest in the current-voltage characteristics. At low applied voltages the injected carriers are trapped and Ohm's law is followed ( $J \propto V$ ). As the voltage is increased, more carriers are injected and the traps are finally filled. At this point there is a sudden transition to the Child's law curve, called the traps-filled-limit (TFL) curve by Lampert. In the TFL region the current can increase by several orders of magnitude for a small change in voltage. After this region is passed, Child's law for solids ( $J \propto V^2$ ) is followed. Further discussions for the cases of the Fermi level above and below the defect level are given by Lampert, Rose and Smith<sup>10</sup> and Lampert<sup>9</sup>. If the thermal-equilibrium Fermi level lies below the defect level, there is a smooth transition from ohmic behavior to SCL current at the voltage at which the density of excess free carrier equals the thermal equilibrium density (the  $V_{tr}$  of Ref. 10). The current continues to follow the square law with increasing voltage until the Fermi level passes the defect level. then, at the voltage  $V_{TFL}$  it makes the sudden large jump to the trap-free Child's law curve; the density of defect states is given by Eq. 1. If the thermal equilibrium Fermi level lies above the defect level no square-law region is observed prior to the traps-filled-limit region. In this case the traps-filled-limit determines only the thermal equilibrium density of holes (for the case of electron injection) in the defect impurity states.<sup>10</sup>

The occurrence of this last situation could explain some of the discrepancy between trap densities calculated from the TFL voltage and other methods. Consider a sample of GaAs with a concentration of deep donors,  $N_{D2}$ , greater than the total acceptor concentration minus the concentration of shallow donors,  $N_{D1}$ . Suppose one or more deep acceptor levels,  $N_{A2}$ ,  $N_{A3}$ , are located below the deep donor, as pictured in Fig. 1. If  $N_{D2} \gg (N_{A1} + N_{A2} + N_{A3} - N_{D1})$ , the Fermi level lies close to  $E_{D2}$  and most of the deep donors are filled. If electrons are now injected, only the few empty deep donor levels have to be filled before the Fermi level moves up near the conduction band and the current increases rapidly to the trap-free-limit curve. For example, a typical high resistivity GaAs sample might have about  $10^8$  free electrons per  $\text{cm}^3$  at 300°K. If we set  $N_{D2}$  equal to  $1 \times 10^{16} \text{ cm}^{-3}$ , we can calculate the quantity

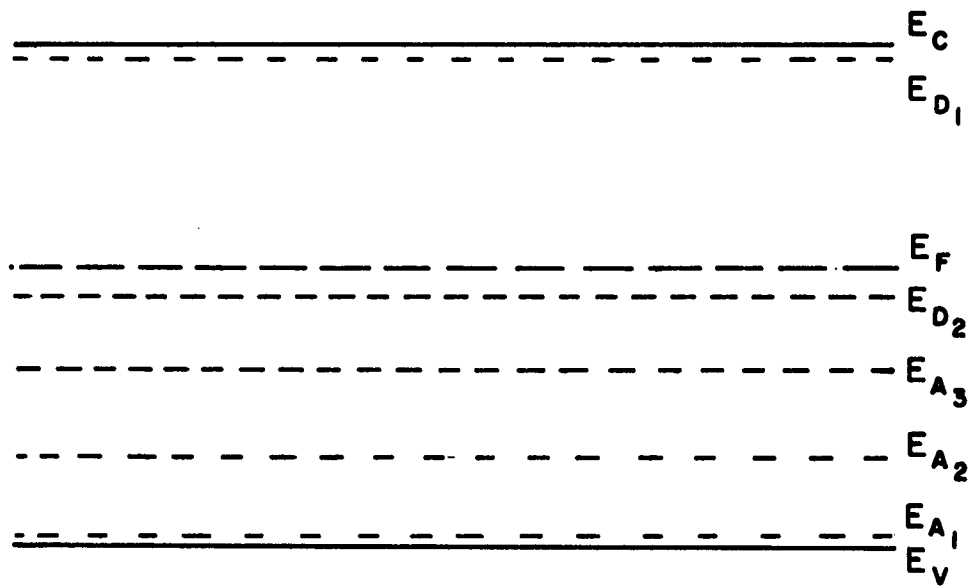


Fig. 1 Distribution of Energy Levels  
Pertaining to Discussion in Text.

$N'_A = (N_{A1} + N_{A2} + N_{A3} - N_{D1})$  from the equation<sup>44</sup>:

$$N'_A = \frac{N_{D2} N_c \exp[(E_c - E_{D2})/kT]}{2n + N_c \exp[(E_c - E_{D2})/kT]} \quad (2)$$

to be about  $2 \times 10^{14}$  for  $E_{D2}$  at 0.66 eV. The thermal equilibrium Fermi level is found<sup>47</sup>,

$$(E_c - E_f) = kT \ln \frac{N_c}{n} \quad (3)$$

to be 0.57 eV below the conduction band, or 0.09 eV above  $E_{D2}$  for  $n = 10^8 \text{ cm}^{-3}$ . The number of positively charged deep donors (i.e., empty electron traps) is given by<sup>47</sup>:

$$N_{D2}^+ = N_{D2} \left[ \frac{1}{1 + 2 \exp[(E_f - E_{D2})/kT]} \right], \quad (4)$$

about 1/60 times  $N_{D2}$ , essentially the calculated acceptor concentration. If electrons were injected, such a distribution of dopants would evidently lead to the transition from Ohm's to trap-free Child's law current without first passing through a square-law region. A trap concentration corresponding to  $2 \times 10^{14} \text{ cm}^{-3}$  would be determined from the traps-filled-limit voltage, even though there are  $10^{16} \text{ cm}^{-3}$  deep donors present and the possibility for a large number of hole traps.

Because the number of positively charged deep donors is (in this model) essentially equal to the quantity  $N'_A = (N_{A1} + N_{A2} + N_{A3} - N_{D1})$ , it is clear that a small number can be obtained even if the sum of the acceptor concentrations is large, provided the shallow donor concentration,  $N_{D1}$ , is approximately equal to the total acceptor concentration. This would be the case if the high resistivity material were obtained by compensating n-type material with copper.<sup>32</sup> The number of hole traps will be larger than the number of electron traps by at least a factor

$$\left( \frac{1}{\frac{\sum N_A}{N_{D1}}} \right),$$

where  $\sum N_A = N_{A1} + N_{A2} \dots + N_{Ai}$  . If we inject holes instead of electrons, the hole quasi-Fermi level will be moving across the hole traps toward the valence band, so the current should go through a square-law region before reaching the traps-filled-limit voltage, and this voltage should be appreciably higher than that for electron injection.

Some preliminary experimental work seems to confirm these ideas. Electron-injecting contacts were prepared by alloying tin into a 0.1 mm wafer of high resistivity GaAs; on a second similar wafer, hole-injecting contacts were made by a shallow zinc diffusion. The voltage-current curves for the two wafers are shown in Fig. 2. The current in the n-i-n structure followed Ohm's law closely out to about 17 volts, then went through a small region in which it actually increased less rapidly than as the first power of the voltage, and broke sharply at 21.5 volts. The current increased about five orders of magnitude for a voltage change from 20 to 40 volts. This transition was completely reproducible. The hole concentration on deep donors corresponding to the transition voltage as given by Eq. 1 is  $2.7 \times 10^{12} \text{ cm}^{-3}$ .

The behavior of the p-i-p structure was essentially consistent with what was expected from the above discussion. The current was ohmic up to about 7 volts, then went through a gradual change to the  $J \propto V^2$  region, beginning at about 30 volts. In this intermediate region between 7 and 30 volts the current varied as  $V^{1.5}$ . It then followed the square law smoothly up to 62 volts, at which point the current began to increase sharply as the voltage was raised, but decayed back to approximately the square-law line in times ranging from 0.1 to 1 minute. This behavior is similar to that observed by Smith and Rose<sup>18</sup> in CdS, and is interpreted as injected carriers slowly filling the traps. The steady-state current continued to approximate the square-law line out to 170 volts. At 180 volts the current was appreciably higher, and at 200 volts an irreversible breakdown occurred. It is not clear whether this breakdown was initiated by reaching the traps-filled-limit voltage, or was some other breakdown phenomenon. The field at which the breakdown occurred ( $2 \times 10^4$  volts/cm) is, by coincidence, the

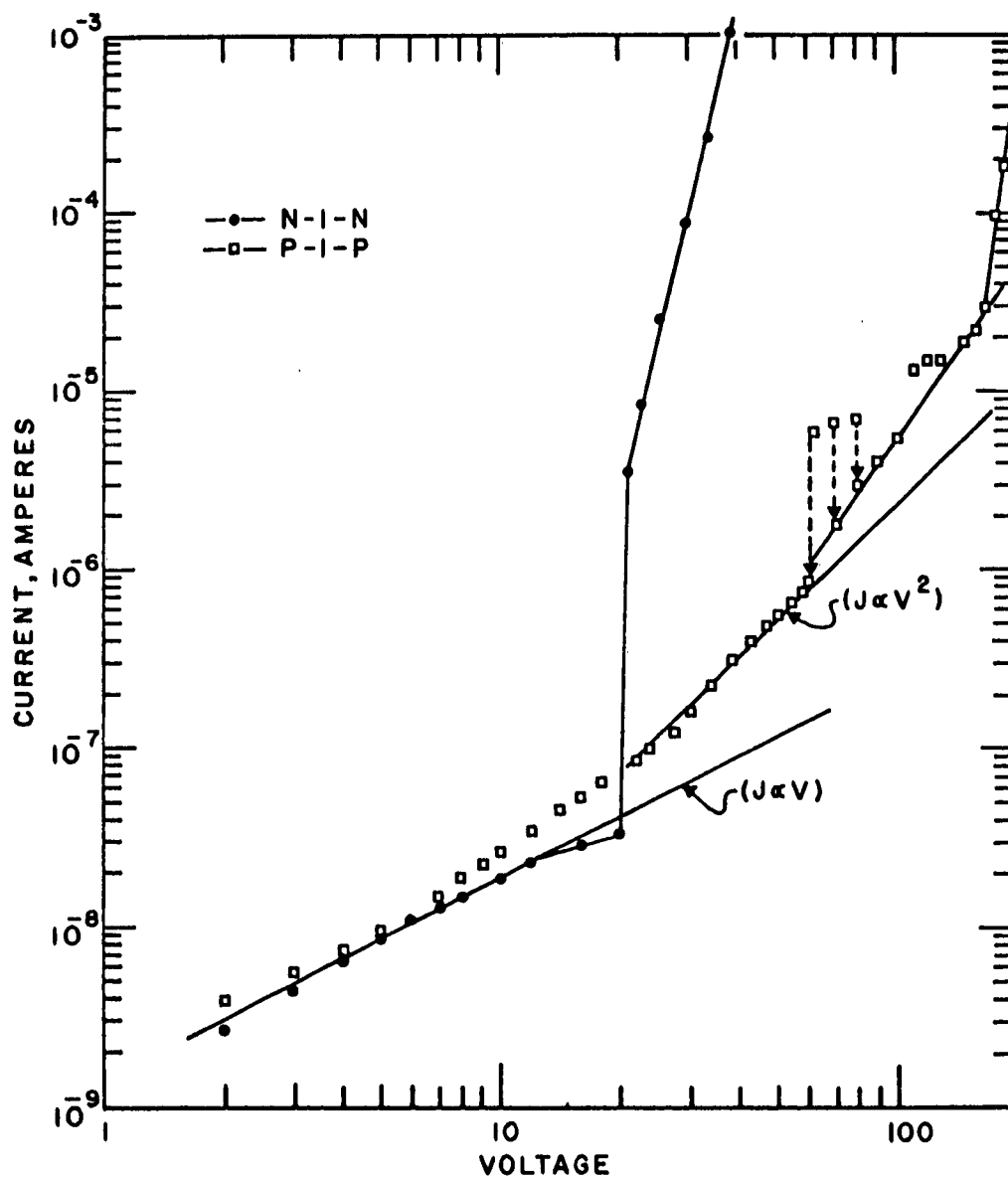


Fig. 2 Voltage-current Characteristics for n- and p-type Contacts on High resistivity GaAs.

same as that found by Gibbons and Reddi<sup>29</sup> for breakdown in gold-doped silicon, which was attributed to impact ionization. Evidence for field-emptying of traps in CdS, using a contact-free method, has been given by Böer and Kümmel<sup>11</sup>. Another possibility is that at higher fields, electrons are injected through the p-layer<sup>30</sup> at the cathode, leading to double injection phenomena.<sup>21-23</sup>

It should be possible to eliminate some of these mechanisms by measuring the breakdown voltage as a function of sample thickness. As Eq. 1 shows, the traps-filled-limit voltage varies as the square of the thickness. It will be of interest to determine the dependence of breakdown on thickness for both electron and hole injection, because in neither case have the theories of space-charge-limited current been thoroughly tested in GaAs. Some such measurements are shown in Fig. 3 for high resistivity GaAs with indium-tin contacts. At 0.96 mm no breakdown occurred up to 325 volts, the maximum available for this preliminary measurement. At the smaller thicknesses, breakdown is observed, following roughly a  $V \propto t^{1.3}$  dependence.

Based on these preliminary measurements we tentatively concluded that two processes operating simultaneously are involved in the breakdown. If the breakdown is only the transition to the trap-free Child's law current, occurring at the traps-filled-limit voltage, the way to raise the breakdown voltage is to increase the trap concentration. However, it is necessary to consider the concentration of both the electron and hole traps.

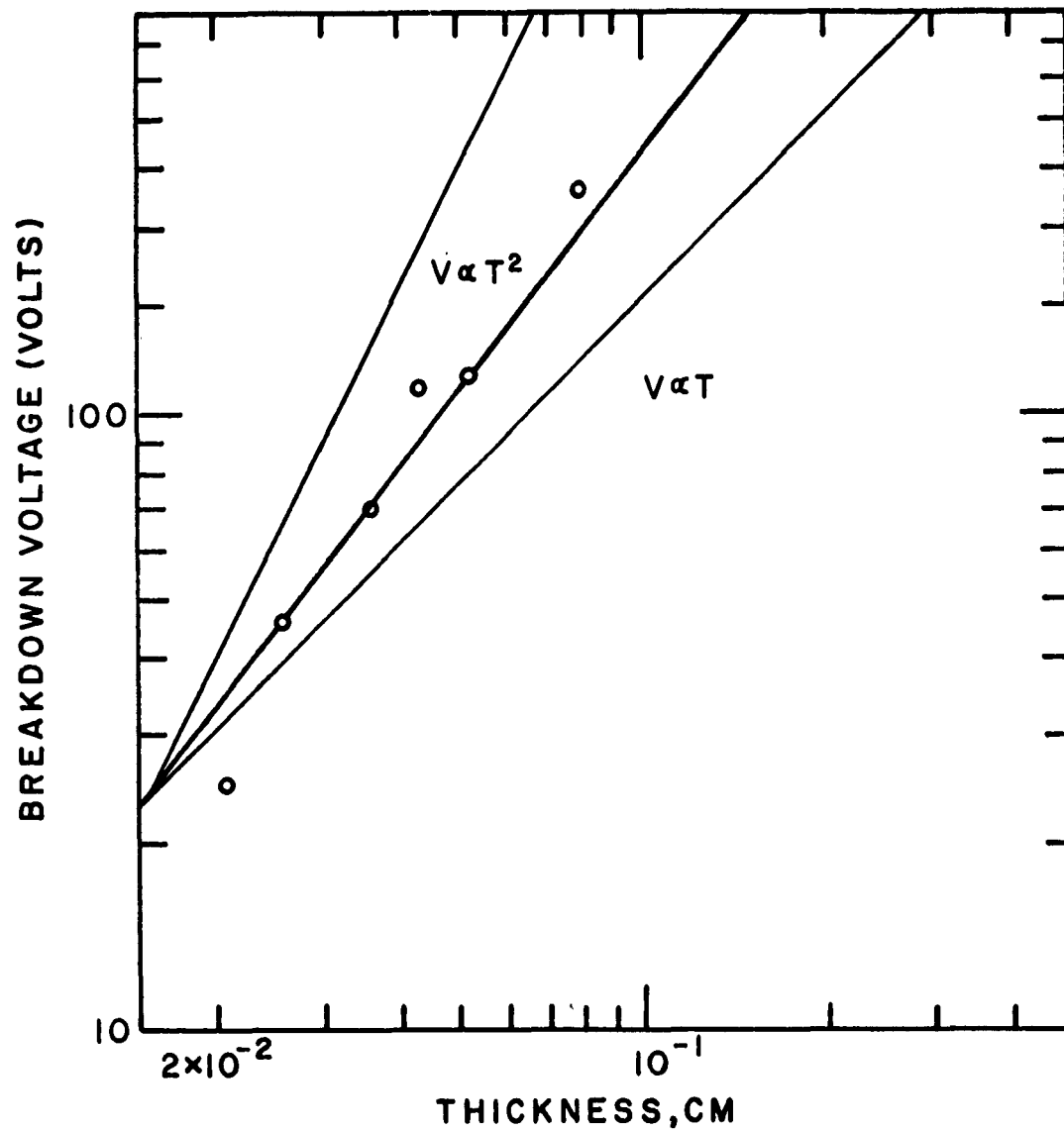


Fig. 3 Breakdown Voltage as a Function of Sample Thickness in High resistivity GaAs with n-type Contacts

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APPENDIX B

GROWTH OF DOPED CdS SINGLE CRYSTALS

by

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## APPENDIX B

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#### ABSTRACT

A vaporization-crystallization process for growing CdS boules uniformly doped with copper or silver has been put into operation. Single crystals measuring  $1 \text{ cm}^3$  that exhibit high resistivity and piezoelectric properties are regularly obtained. These crystals can be readily sawed into slices for use in work on Contract AF 33(657)-9196, Functional Electronic Blocks, Task III. With variations in temperature and ambient gases, the method is expected to be applicable to doping CdS with other impurities and to preparing single crystals of other II-VI compounds.

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### INTRODUCTION

To fulfill obligations of Contract AF 33(657)-9196 Functional Electronic Blocks, Task III: II-VI devices, it is necessary to have a ready supply of custom-grown single crystals. Commercial sources, for reasons of cost, quality, and adequate supply, have not proved satisfactory; consequently, we have set up facilities to produce the necessary crystals. Two furnaces with attendant facilities are now set up to grow boules by a variation of the vaporization crystallization method,<sup>1,2,3</sup> and about 12 runs have been made. This report details pertinent information about these furnaces and the crystals produced.

### BACKGROUND

The intent of Task III of Contract AF 33(657)-9196 is to exploit unique properties of II-VI compounds by fabricating FEB devices unlike or better than devices that can be made with other semiconducting materials. Outstanding properties of the II-VI's are luminescence, photoconductance, and piezoelectric properties. In addition, some II-VI's, notably CdS, show interesting gross interactions between light, electric fields, and acoustical waves. Thus, and because it has been amply demonstrated that CdS can be processed with active and passive devices with bulk resistivities ranging as high as  $10^{14}$  ohm-cm, this material has been selected as initially appropriate for the project. The main drawback in using CdS is the lack of useful p-type conduction; some flexibility may be lost as CdS is exploited

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<sup>1</sup> Green, Reynolds, Czyzak and Baker, J. Chem. Phys. **29**, 1375 (1958).

<sup>2</sup> D. R. Boyd and Y. T. Sihvonen, J. Appl. Phys. **30**, 176 (1959).

<sup>3</sup> W. W. Piper and S. J. Polich, J. Appl. Phys. **32**, 1278 (1961).

for FEB purposes. However, the furnaces to be described were made as versatile as possible so that other II-VI materials could be processed if necessary.

In general, electro-optically uniform, high resistivity FEB substrates as large as 1 cm x 1 cm square x 0.1 cm thick are needed. Further, they must be accurately oriented relative to crystallographic axes, to capitalize on appropriate piezoelectric resonance modes. CdS substrates incorporating only copper or silver dopants have inherently high resistance and are poor photoconductors. We expect that further selective surface treatments with donor dopants, such as indium, will produce functioning islands which will be the desired passive and active components comprising the FEB.

#### FURNACE DESCRIPTION

Figure 1 depicts the apparatus used for growing "pure", Cu-doped and Ag-doped CdS crystals. The basic furnace, purchased from Dispatch Oven Company (Model Sc-32), contains three individually controlled temperature zones. Silicon carbide elements, thyatron tube powered, furnish full proportioning heat input to each zone, and a maximum of 1450°C is attainable. Wheelco temperature controllers, one for each zone, sense temperature via platinum/platinum - 13% rhodium thermocouples and control thyatron firing to maintain set temperature.

The furnace was modified by adding fire brick walls between the second and third heating elements to better confine heat to individual zones. The silicon carbide elements were rewired to decrease the center zone length to 12 inches (4 element pairs) and increase end zones to 5 inches (2 element pairs each). Finally, each control circuit has been sensitized by adding a stage of amplification and rate feedback which reduces the original proportional band from approximately 100°C to 1°C. Temperature at the thermocouples can be held within  $\pm 1^\circ\text{C}$ . Although the system hunts under certain

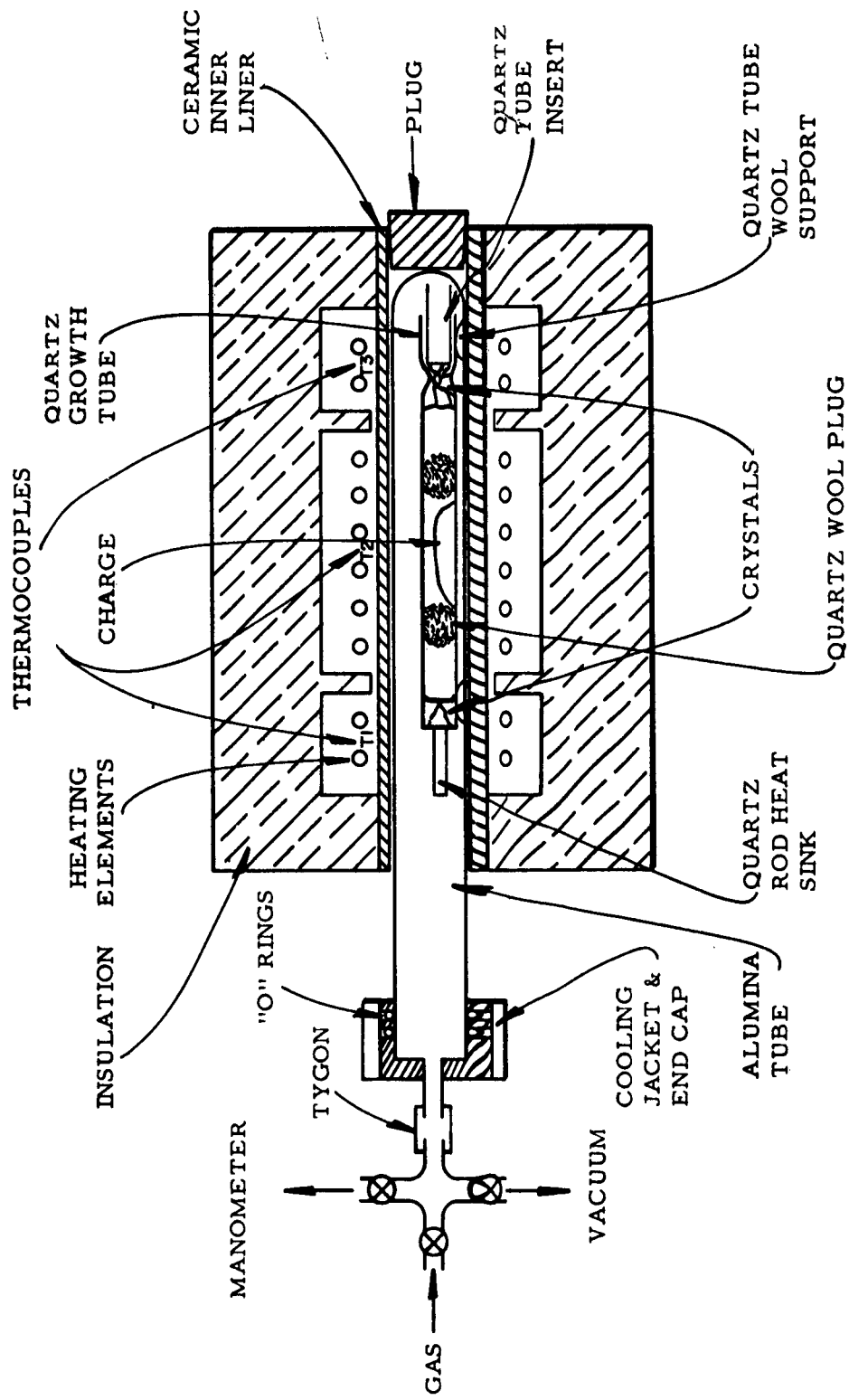


FIGURE 1 Crystal growth apparatus

conditions, negligible temperature variations are observed. System overshoot and undershoot under worst case transient conditions are less than 10°C (typically 3°C). In addition to providing closer temperature regulation of the growth process, the revised control demands reduced operator attendance at the beginning of each run.

A ceramic liner tube with a 2 3/4-inch inside diameter extends the length of the furnace. This tube isolates each zone and serves as support for an aluminum tube, 2 3/8 in. I.D. x 36 in. long, which is closed on one end and extends out of the furnace. A water-cooled end cap, with an access nozzle, clamps over the alumina tube and vacuum seals it via two silicon rubber "O" rings. A manifold, with 3 vacuum stopcocks, attaches to the nozzle and leads to a manometer, a vacuum pump, and a gas bottle.

The crystal growth tube is typically clear quartz, 26 mm I.D. x 21-inches long. One end of this tube is sealed off flat and a solid quartz rod is fastened externally to the center of this flat surface to serve as a cooled nucleating point for initiating crystal growth. The open cavity of the growth tube receives a 4-inch long flat bottomed quartz tube which fits snugly inside it. The flat bottom of this insert tube provides a second crystal growth surface. As vapors deposit in the space between the growth tube and the smaller insert tube, the growth chamber seals itself off, and constant ambient conditions for crystal growth are automatically maintained.

#### CRYSTAL GROWTH

All glassware used in a growth run is soaked in boiling trichloroethylene and rinsed in semiconductor grade methyl alcohol. It is next placed in concentrated semiconductor grade HCl acid, then rinsed several times in distilled water.

Luminescent grade CdS (General Electric) so far has been used exclusively as the basic charge. The first material received, lot 104 in Table I, had an excessive amount of Zn, which tended to permeate our first crystals. However, early runs were made only to optimize techniques and furnace conditions. Subsequent lots, e.g., lot 135, show no detectable Zn.

A 300-gram batch of CdS constitutes the first charge, to which 0.3 grams of copper or silver powder is added when doped crystals are desired. This mix is maintained at 100 to 200°C under vacuum for 20-24 hours to remove moisture. The temperature is raised to 700°C and 1 atmosphere of H<sub>2</sub>S is introduced. The temperature is raised further and maintained at 900°C for four hours. This treatment converts cubic CdS to the wurtzite structure, removes some impurities (as seen in line 3, Table I.), and diffuses the dopant into the granules. After cooling, the sintered material is ground to 10-20 mesh, and 200-250 grams are placed into the center of the growth tube. Quartz wool plugs on both sides of this basic charge prevent powder movement during handling.

The loaded growth tube is next inserted into the alumina tube in the furnace and supported on quartz wool inserts that minimize the radial temperature gradient. Again, preliminary outgassing to remove H<sub>2</sub>O and O<sub>2</sub> is accomplished by pulling a vacuum while heating at 100-200°C for 20 hours. Then, all zones are brought up to 700°C and an argon pressure of 100 mm Hg is admitted to the system. The two end zones are raised to operating temperature (1050 to 1175°C), with the center zone lagging behind. Finally, the center zone is raised to operating temperature and deposition of material begins on the cooler end plates.

Growth conditions are maintained from 5 to 8 days. After the growth period, approximately 20 hours are allowed to bring the crystals to room temperature, after which they are removed by breaking the growth tube.

TABLE I. TYPICAL SPECTROCHEMICAL ANALYSES

<u>Description of Material</u>	<u>Impurities in ppm</u>													
	<u>Si</u>	<u>Pb</u>	<u>Mg</u>	<u>Cu</u>	<u>Zn</u>	<u>Ca</u>	<u>Na</u>	<u>Mn</u>	<u>Sn</u>	<u>Fe</u>	<u>Cr</u>	<u>Al</u>	<u>B</u>	<u>Ag</u>
As received Lot 104	0.88	ND	0.31	0.1	180	0.30	1.8	ND	ND	ND	ND	ND	ND	ND
As received Lot 135	1.5	17	0.27	ND	ND	0.15	ND	ND	ND	ND	ND	ND	ND	ND
Lot 104 after outgas and sinter in H <sub>2</sub> S	7.4	ND	0.08	ND	170	0.13	ND	ND	ND	ND	ND	ND	ND	ND
CdS crystal grown at 1080°C (5-1) (Cu added)	ND	ND	ND	0.4	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND
CdS crystal grown at 1150°C (8A-1) (Cu added)	0.52	<.2	0.14	8.0	<50	<.1	<1	<.05	<.5	<.1	<.5	<.2	<.05	<.02
CdS crystal grown 2" from charge (Cu added)	500	1.5	3.3	37	200	<.1	8	2.2	ND	1.8	0.6	1.8	3.7	0.39
Residue from initial charge (9-2) (Cu added)	14	42	1	38	330	<.1	<.5	0.2	ND	1.5	ND	4.4	16	0.15

It is possible to control the amount of Cu in the CdS crystals by simply regulating the temperature gradient in the growth tube. With the center zone at 1250°C and growth plates at 1175°C, single crystals were obtained with 20-50 ppm Cu. When the temperature at the growth plates was 1150°C, the copper concentration reduced to 8-10 ppm. A further reduction at the end zones to 1080°C results in crystals incorporating less than 1 ppm (run 5-1). In this latter run, a second polycrystalline deposit, graded in color, was obtained 2 to 3 inches from the initial charge (Fig. 2, bottom). These deposits ranged from 40 ppm to 1% copper. The sharp difference in copper content between the mid-deposit, and the end deposit suggests that CdS:Cu has a significantly higher vapor re-crystallization temperature than pure CdS. The charge residue and crystals that grew on top of the original charge assayed to contain from 1 to 10% Cu, and probably have a large  $\text{Cu}_2\text{S}$  component. Figure 2 illustrates some of the deposition behavior obtained at various temperatures, and Fig. 3 is a picture of assorted CdS pieces.

The boules that grow on the end plates are remarkably uniform in composition, as evidenced by their homogeneous appearance, emission spectrochemical analysis, luminescence at 77 and 300°K, and resistivity measurements. Although no boule so far has been entirely single crystal, there are usually several  $1 \text{ cm}^3$  size specimens suitable for slicing and FEB use. These larger crystals are easily cleaved apart from the smaller ones.

A tapered conical surface was tried several times, with the expectation that one large single crystal would favorably develop. However, such a growth surface proved no more productive than a flat surface and furthermore, the larger crystals were harder to separate from their neighbors.

The rate of growth is fixed by the temperature of the charge and the argon pressure in the system before the growth tube sealed itself off. At 1250°C and an argon pressure of 600 mm Hg, the growth rate was about 5 grams per day, while at an argon pressure of 150-200 mm Hg, the growth rate was 15-20 grams per day.

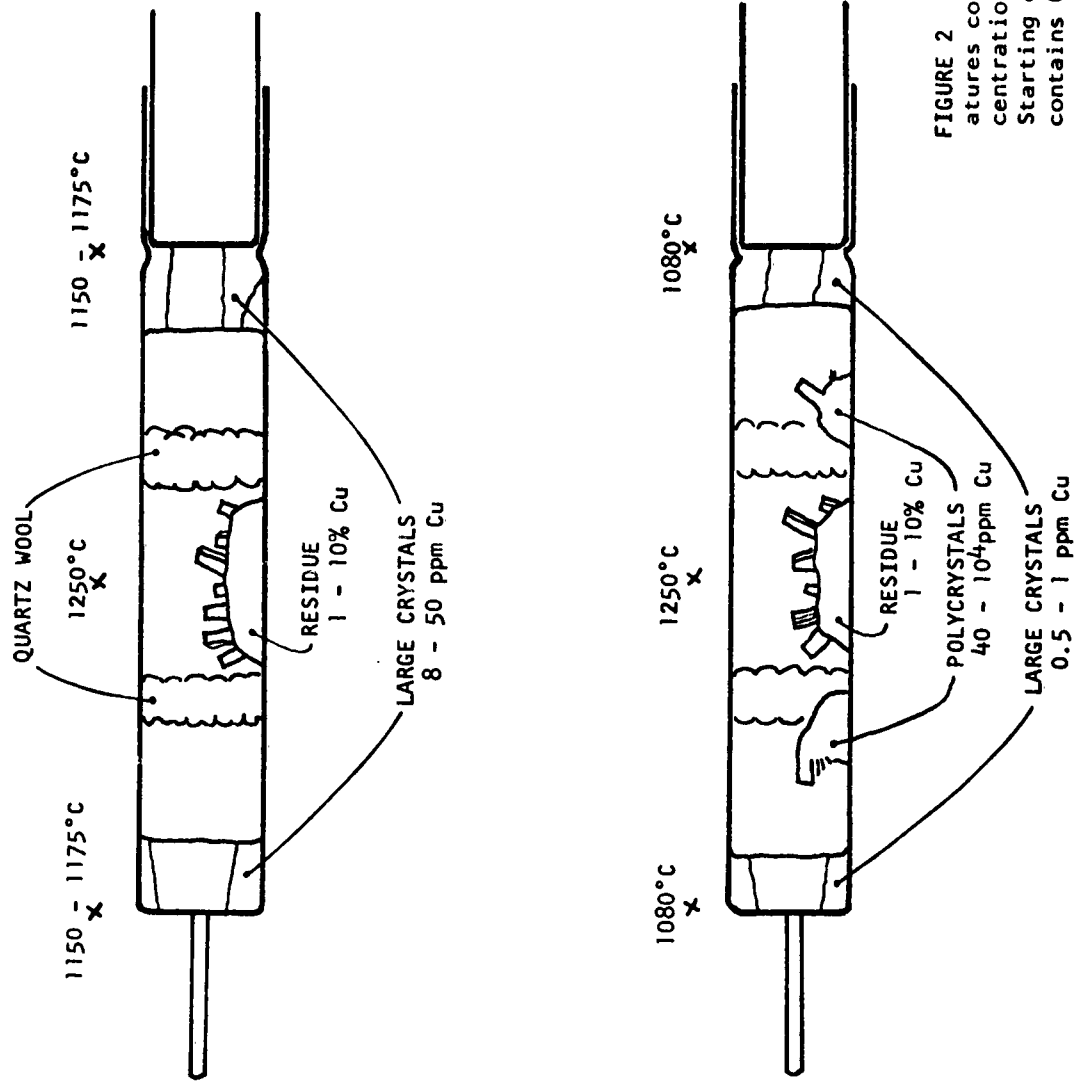


FIGURE 2 End zone temperatures control copper concentration in large crystals. Starting charge typically contains 0.1% copper.

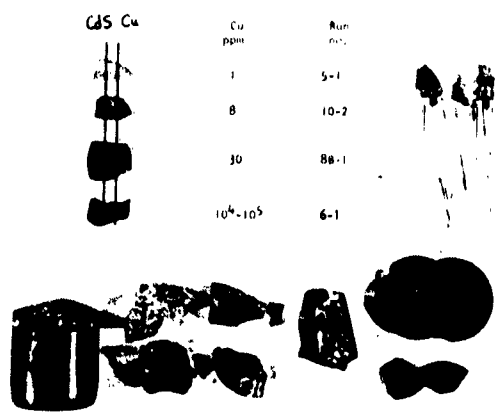


FIGURE 3 As grown boule of CdS:Cu and assorted single crystals and prepared slices.

Silver-doped CdS has been grown by the same procedure used for CdS:Cu. Our first run, using  $\text{AgNO}_3$  as the dopant, has produced very uniform single crystals containing an estimated 100 ppm Ag. Further tests are in process, and optimized growth conditions will be described in a later report, if the resulting CdS:Ag substrate proves superior to CdS:Cu for FEB devices.