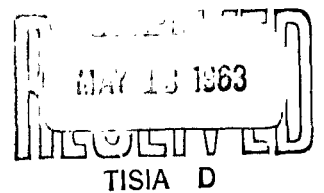


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QUARTERLY REPORT NO. 3
for
GALLIUM ARSENIDE VARACTOR DIODES
THIS REPORT COVERS THE PERIOD
28 DECEMBER 1962 TO 28 MARCH 1963
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NAVY BUREAU OF SHIPS ELECTRONICS DIVISION
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ABSTRACT

Emphasis this quarter was placed on the fabrication of diodes with breakdown voltages in excess of 20 volts. Devices were made using both epitaxial and melt-grown material. The change in material characteristics which occur during diffusion have been investigated. Ten devices meeting the requirements outlined for Phase II of this contract have been delivered.

PART I

I. PURPOSE

The purpose of this contract is to develop a series of gallium arsenide varactor diodes capable of yielding 40% power conversion efficiency from 12 Gc to 24 Gc.

Phase II of this contract is to develop a device that is capable of meeting the following circuit objectives:

- (a) Input frequency of 12 Gc
- (b) Output frequency of 24 Gc
- (c) Input power of 100 mw
- (d) Output power equal to or greater than 40 mw at 25°C

This phase was completed on 2/28/63 with the delivery of 10 samples.

The goal of Phase III of the contract is to develop a device meeting the following objectives:

- (a) Input frequency of 12 Gc
- (b) Output frequency of 24 Gc
- (c) Input power of 250 mw
- (d) Output power of 100 mw minimum at 25°C

A total of ten units will be submitted to the contracting agency together with all the required reports.

II. TECHNICAL DISCUSSION

A. Device Specification

In the first quarterly report of this contract, expressions were derived for the power handling capability and conversion efficiency of a varactor diode. The maximum power input for optimum efficiency was shown to be:

$$P_{in} = \frac{1}{35} \omega C_{min} (\phi + V_B)^2 \dots \dots \dots (1)$$

where:

ω = input angular frequency

C_{min} = minimum junction capacitance

V_B = breakdown voltage

ϕ = built-in potential (1 volt for Gallium Arsenide)

Figure (1) shows the relationship between V_B and C_{min} which must be satisfied at 12 Gc for an input power level of 250 mw in order to obtain optimum conversion efficiency.

The conversion efficiency was shown to be determined by the ratio

$$\frac{f_{in}}{f_{c(max)}}$$

where:

$$f_{in} = \text{input frequency, } f_{c(max)} = \frac{1}{2\pi R C_{min}}$$

R = diode series resistance

To obtain 40% conversion efficiency, $\frac{f_{in}}{f_{c(max)}}$ must be equal to or

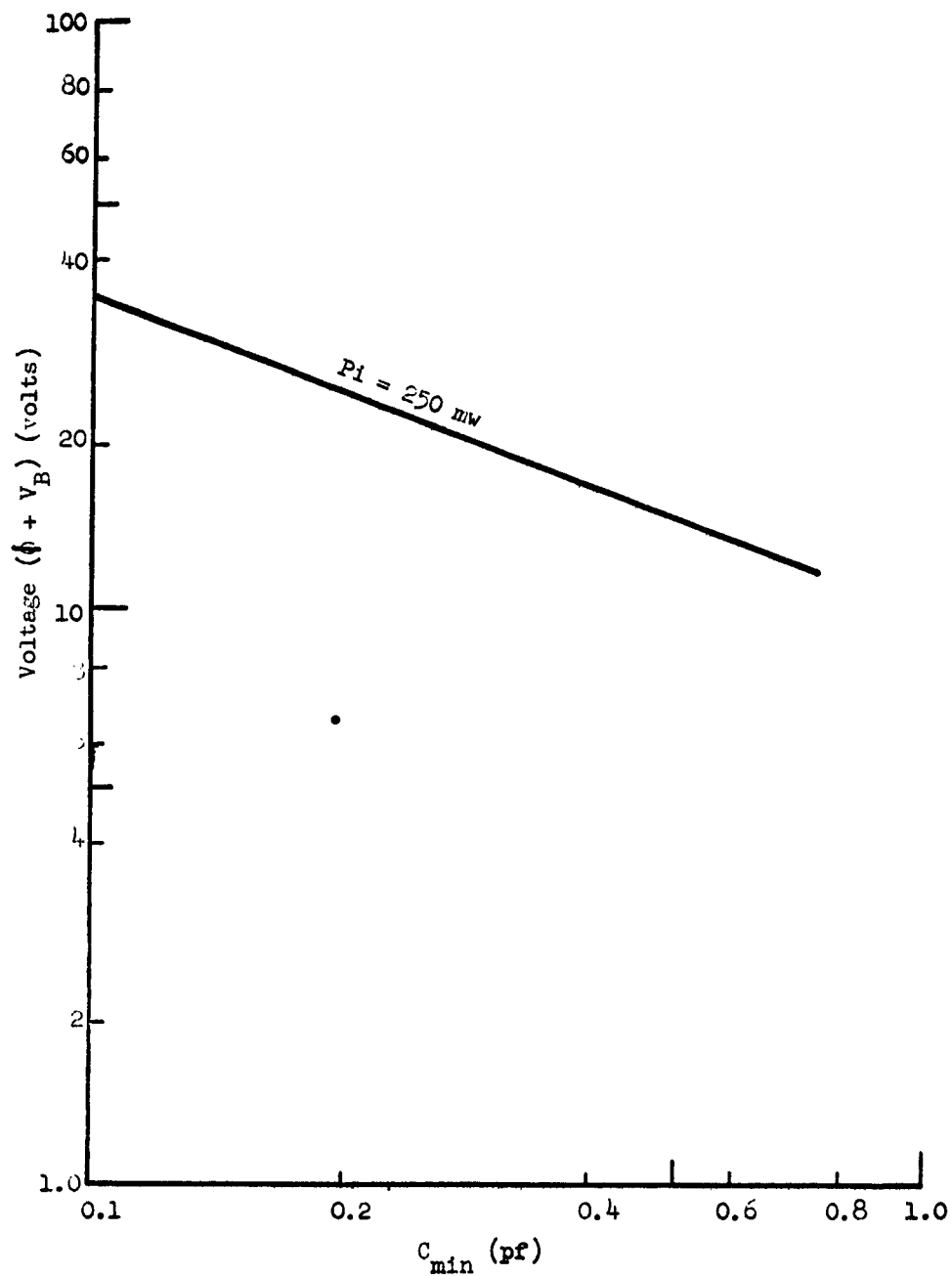


FIGURE 1 BREAKDOWN VOLTAGE vs. MINIMUM CAPACITANCE FOR 250 mW
DIODE INPUT POWER AT 12 GC (BEST CONVERSION EFFICIENCY)

less than 0.050. At 12 Gc input frequency, $f_{c(max)}$ must therefore, be greater than 240 Gc.

B. Process Development

1. General

The second quarterly report outlined the "well" process which was developed to minimize the series resistance of the devices. The well structure consists of a thin base region surrounded by thicker bulk material (Figure 2). Work continued during this quarter on improving the reproducibility of this technique. Two areas in particular have received a great deal of attention: parallel lapping of the wafers; and control of diffusion depth.

Since the wells are etched simultaneously over a whole wafer, the parallel tolerance of the wafer planes is obviously very important. Best results have been obtained by hand lapping, using a lapping fixture which give tolerances to within 0.05 mils. The final wafer thickness is approximately 3 mils.

Close control of the base region when the wells are etched prior to the p-type diffusion also requires close control of the diffusion depth. At the diffusion temperature previously used (1000°C), the diffusion coefficient for zinc in gallium arsenide is such that the typical diffusion run time was approximately 120 seconds for 0.4 mil penetration. Furthermore, the time required to bring the ampoule up to temperature was a very appreciable part of the total time in the furnace. Several experiments have been made with the temperature of diffusion reduced to 800°C which have resulted in substantially improving

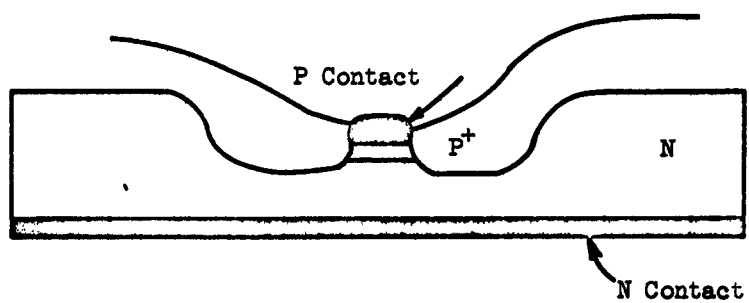


FIGURE 2 WELL STRUCTURE CROSS SECTION

the control of diffusion depth.

Figure 3 is a plot of junction depth X_j , as a function of time for three diffusion runs. The zinc surface concentration is about 5×10^{19} atoms/cc. The variation of X_j as a function of time follows from the normal erfc distribution:

$$X_j \propto \sqrt{t}$$

The calculated diffusion coefficient is equal to about 2×10^{-11} cm²/sec.

2. Effects of Heat Treatment on Crystal Properties

Since the fabrication of relatively high breakdown diodes (greater than 30-40 volts) requires relatively lightly doped starting material, the changes in the property of such crystal during diffusion are of great interest.

It has been observed that, in general, the measured values of cutoff frequency of the diodes fabricated from material with net carrier concentration under 2×10^{16} /cc are substantially below the expected values, if the spreading resistance is computed using the initial crystal resistivity. This discrepancy may be attributed in large part to the reduction in the net carrier concentration which is known to occur during high temperature heat treatment of n-type gallium arsenide. These changes are attributed to the introduction of contaminants during heat treatment which act as p-type impurities.

The degree of compensation has been measured on a number of n-type crystals with starting net carrier concentrations between

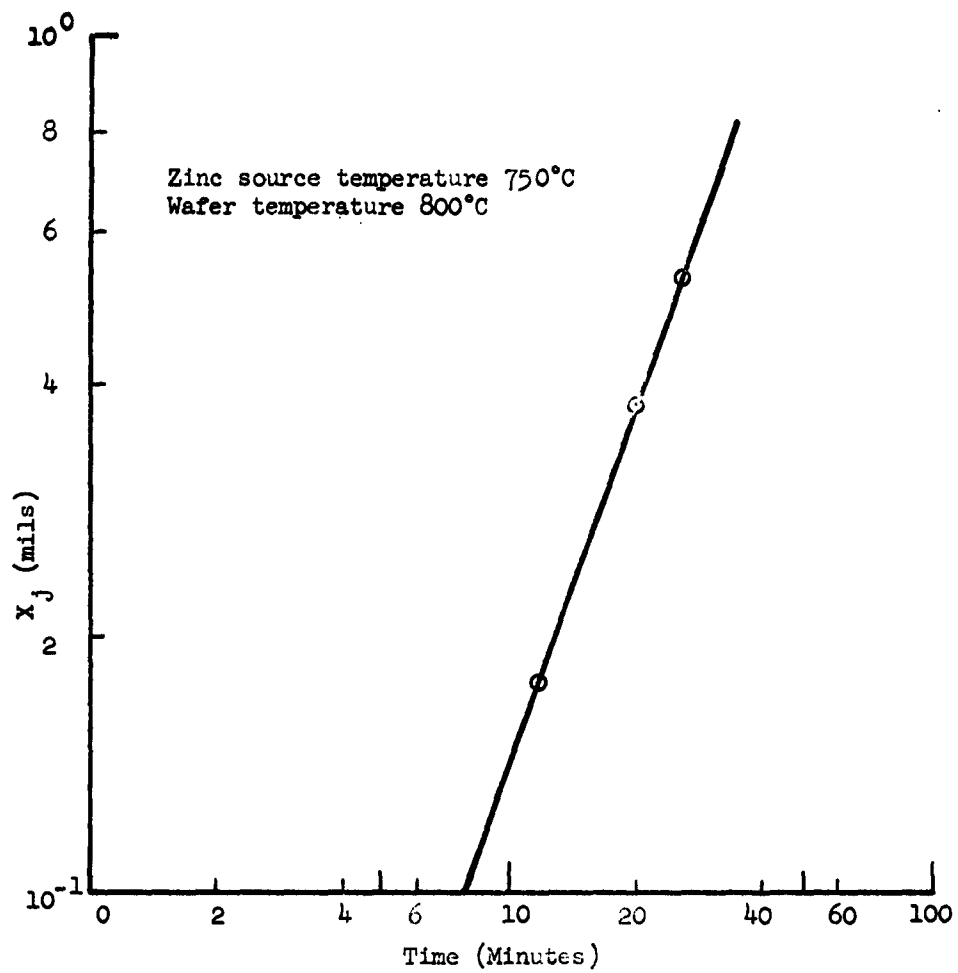


FIGURE 3 JUNCTION DEPTH X_j , AS A FUNCTION OF DIFFUSION TIME FOR ZINC INTO N-TYPE GaAs ($n \approx 4 \times 10^{16}$ DONORS/cc)

$1.5 \times 10^{17}/\text{cm}$ and $3 \times 10^{15}/\text{cm}$ by measuring the electron mobility and carrier concentration before and after a heat treatment which simulated the diffusion conditions normally used, until recently. The sample wafers were cleaned in reagent grade chemicals and sealed with a small amount of arsenic in an evacuated Vitreosil ampoule. They were then heated at 1000°C for three minutes in the glo-bar furnace normally used for diffusion. The data is summarized in Figures 4, 5 and 6. Figure 4 shows the normalized net carrier concentration change versus starting concentration for six samples measured. The average decrease in net donor concentration was about $4 \times 10^{15}/\text{cc}$. However, the electron Hall mobility remained constant, (Figure 5). The observed change in crystal resistivity (Figure 6) is, therefore, the result of the decrease in net carrier concentration only.

One technique which has been suggested to minimize the introduction of acceptors through the indiffusion of contaminants is the use of a radiant heat furnace for diffusion. (Ref.1)

In such a furnace the crystal can be maintained at a higher temperature than the quartz ampoule which is nearly transparent to radiant energy in the near infrared region of the spectrum. As a result, contamination from the quartz may be minimized. This technique will be investigated as a means of reducing the contaminants during diffusion.

3. Ohmic Contacts

A simple method has been devised to evaluate the contact resistance

(Ref.1) T.S. Kinsel and T.E. Seidel, "Heat Treatment of n-type GaAs by Radiant Energy", J.A.P. Feb., 1962.

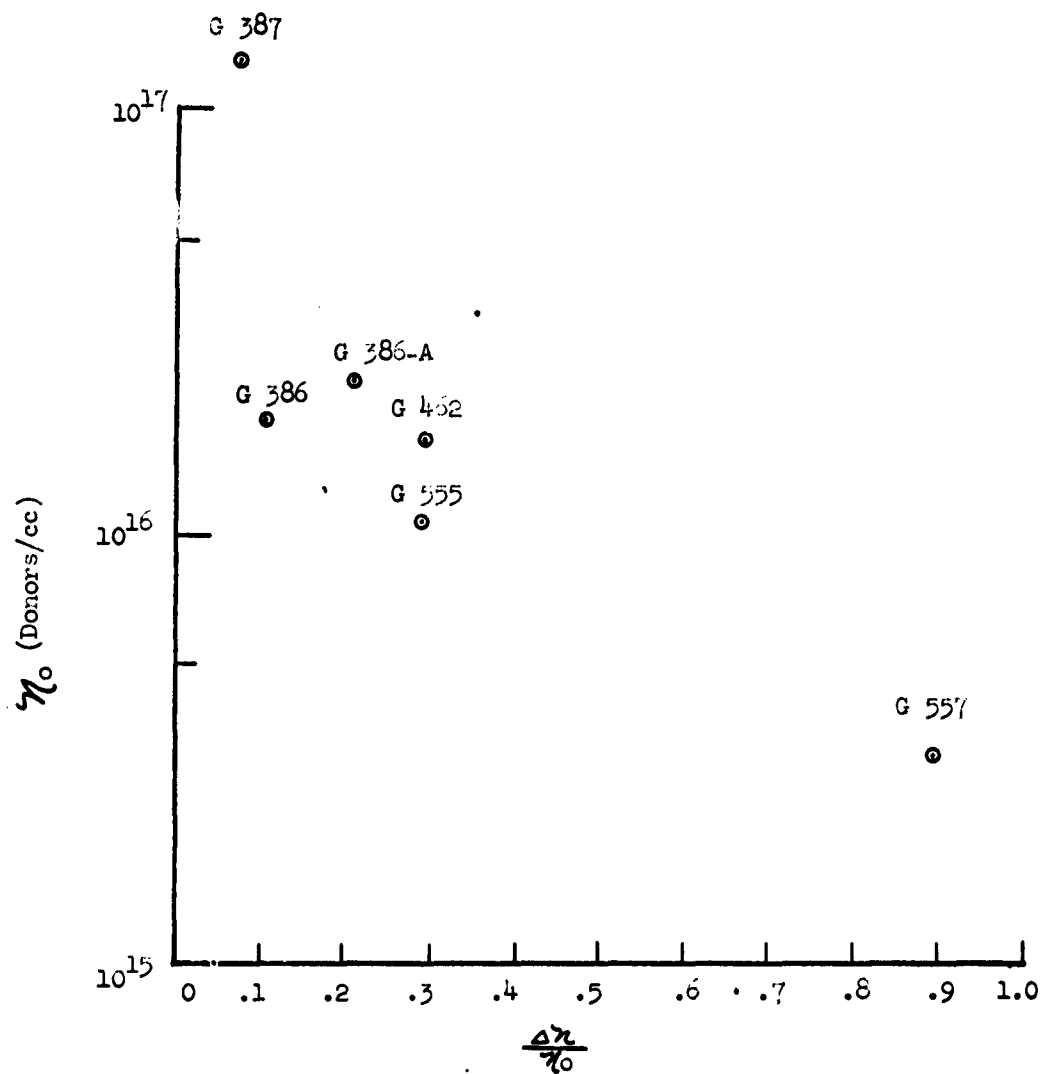


FIGURE 4 NORMALIZED NET CARRIER CONCENTRATION CHANGE vs. STARTING CONCENTRATIONS AFTER 3 MIN AT 1000°C FOR SEVERAL N-TYPE GaAs CRYSTALS

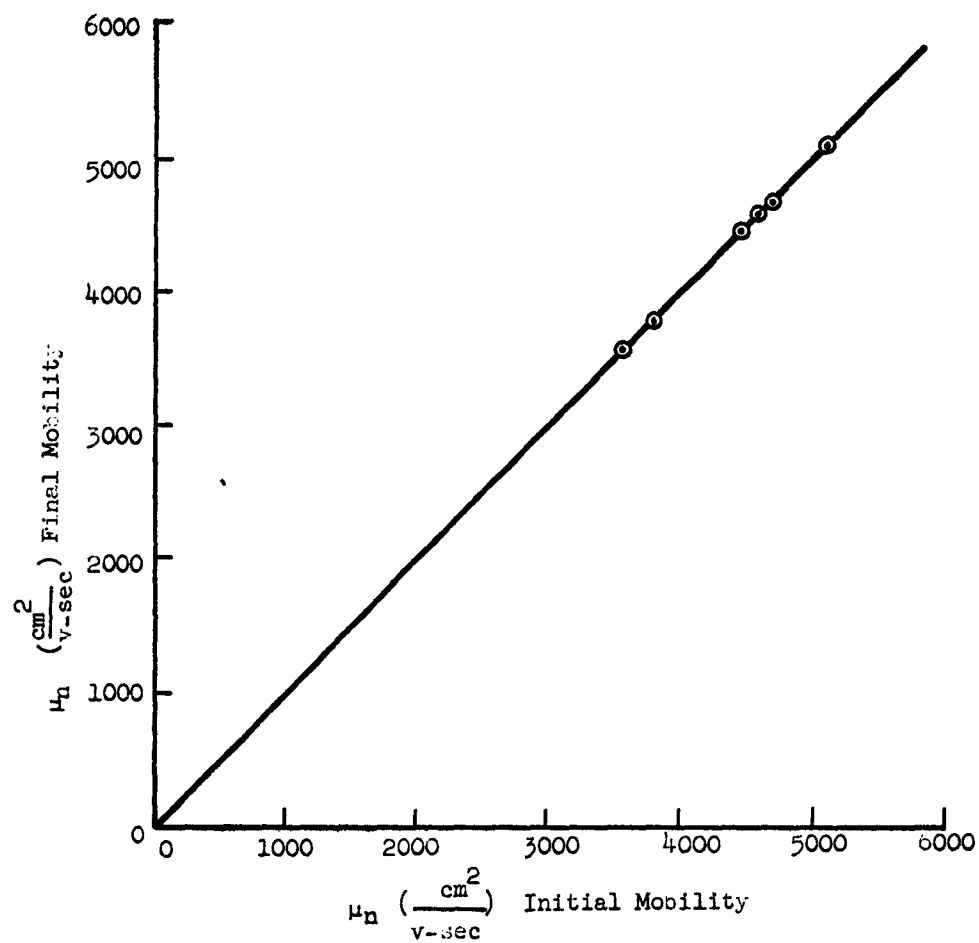


FIGURE 5 ELECTRON MOBILITY BEFORE AND AFTER HEAT TREATMENT
(3 MIN AT 1000°C) FOR SIX N-TYPE GaAs SAMPLES

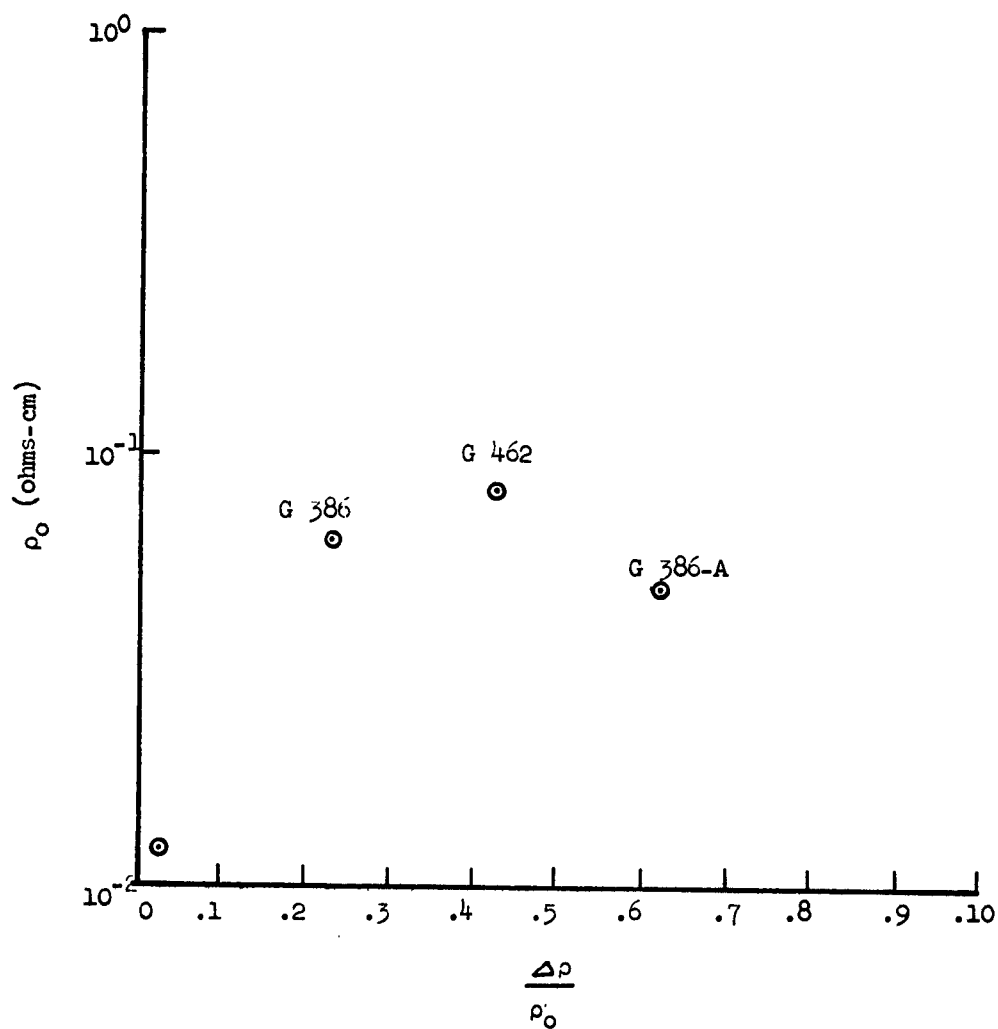


FIGURE 6 NORMALIZED RESISTIVITY CHANGE, $\frac{\Delta \rho}{\rho_0}$, vs. STARTING RESISTIVITY, ρ_0 , FOR SEVERAL N-TYPE GaAs CRYSTALS DIFFUSED FOR 3 MINUTES AT 1000°C

of various alloys on gallium arsenide. A material for evaluation is alloyed into the gallium arsenide crystal in small inline areas across the chip, (Figure 7a). Two current probes and two separate voltage probes are connected to adjacent contact areas, (Figure 7b). A known current, I_1 , is passed through the current probes and the voltage drop, V_1 , is measured through the voltage probes. Figure 7d shows the equivalent circuit for the set-up. $V_1 = I_1 (R_1 + R_s + R_2)$ where R_1 and R_2 are contact resistances and R_s the resistance of the gallium arsenide between the contact areas.

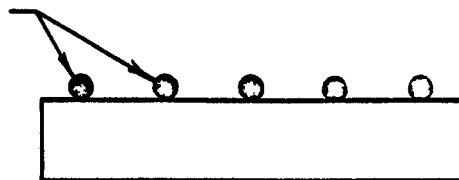
One of the current probes is then moved to another adjacent contact area and a known current I_2 is passed through the current probes (Figure 7c). A voltage drop, V_2 , is measured. From Figure 7e, $V_2 = I_2 (R_1 + R_s)$. If $I_1 = I_2$, then $V_1 - V_2 = I_1 R_2$ and R_2 can be determined.

The accuracy of the method is enhanced by using a relatively narrow crystal chip and small contact areas to minimize current spreading. The evaluation of various alloys is in progress.

4. Epitaxial Diodes

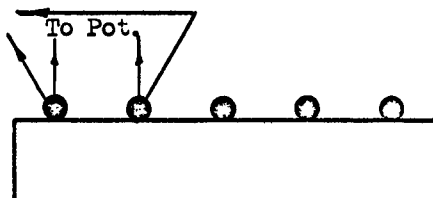
Two epitaxial wafers having grown p^+ regions were evaluated. Such structures are of interest since p-type diffusion is eliminated, thus, reducing the possibility for introduction of contaminants into the crystal. The results are of interest, since the voltage breakdown characteristics of the diodes fabricated from these wafers were unusually uniform. Some of the typical device characteristics are listed in Table I. A85

Alloyed metallic contacts



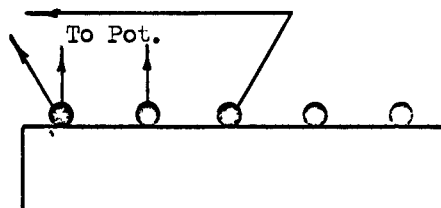
a. Crystal and Contacts

To Current Source

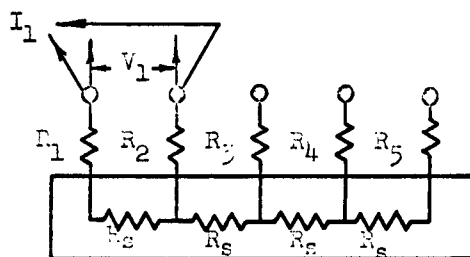


b. First Measurement

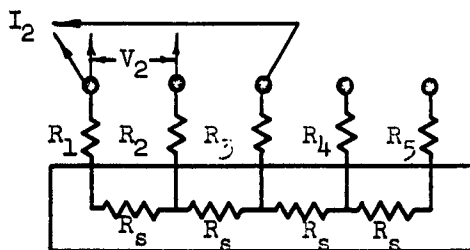
To Current Source



c. Second Measurement



d. Equivalent Circuit



e. Equivalent Circuit

FIGURE 7 CONTACT RESISTANCE DETERMINATION.

yielded diodes with exceptionally high breakdown voltages.

The computed junction impurity gradient calculated from capacitance per unit area data for wafer A85 is 1.2×10^{20} excess donors/cm⁴. From earlier data for non-epitaxial diodes, (Figure 8)⁽²⁾ the observed breakdown voltage should be 90 volts, which agrees with the present results. Similarly for A84, the computed gradient is 4×10^{21} excess donors/cm⁴. The observed and expected breakdown voltage are again in agreement. The cutoff frequencies of these diodes are not higher than those achieved with non-epitaxial material. One possible reason may be the higher contact resistance of the connection to the p side of these pellets, the carrier concentration at the surface being lower than the ones normally achieved with diffused junctions. Furthermore, the n regions of these diodes are not substantially lower than the base of the "well" units fabricated from melt-grown gallium arsenide.

Diodes were also fabricated with diffused junctions on a number of nn⁺ wafers. The best devices were fabricated on slice A75 having an exceptionally thin n-type epitaxial layer (0.15 mils) and a junction depth of 0.128 mils. The n-type layer carrier concentration was estimated to be approximately 3×10^{16} /cc. Three of these devices were submitted in fulfillment of Phase II of the contract (Table II).

(2) H.Kressel and A.Blicher, "Avalanche Breakdown in Graded Gallium Arsenide P-N Junctions" to be Published in J.A.P.

TABLE I
CHARACTERISTIC OF GROWN P⁺ NN⁺ DIODES

Epitaxial Wafer Characteristics

Wafer No. A84

$$n = 3.45 \times 10^{16}, p^+ = 1.42 \times 10^{19}, n^+ = 5.7 \times 10^{18}$$

Thickness of n-region: 0.228 mils

Thickness of p⁺ region: 0.37 mils

Wafer No. A85

$$n = 6.55 \times 10^{16}/\text{cc}, p^+ = 5 \times 10^{18}/\text{cc}, n^+ = 5 \times 10^{18}/\text{cc}$$

Thickness of n-region: 0.266 mils

Thickness of p⁺ region: 0.32 mils

Diode No.	C _{jo} (pf)	V _B (volts)	f _{c-6} (kmc/s) ⁺
A84-6	.246	50.0	56
A84-8	.596	50.0	64
A84-4	.641	49.0	110
A84-7	.777	50.0	150
A85-14	.553	100.0	22
A85-13	.666	100.0	35
A85-8	.629	100.0	41

+ Measured at 10 kmc/sec

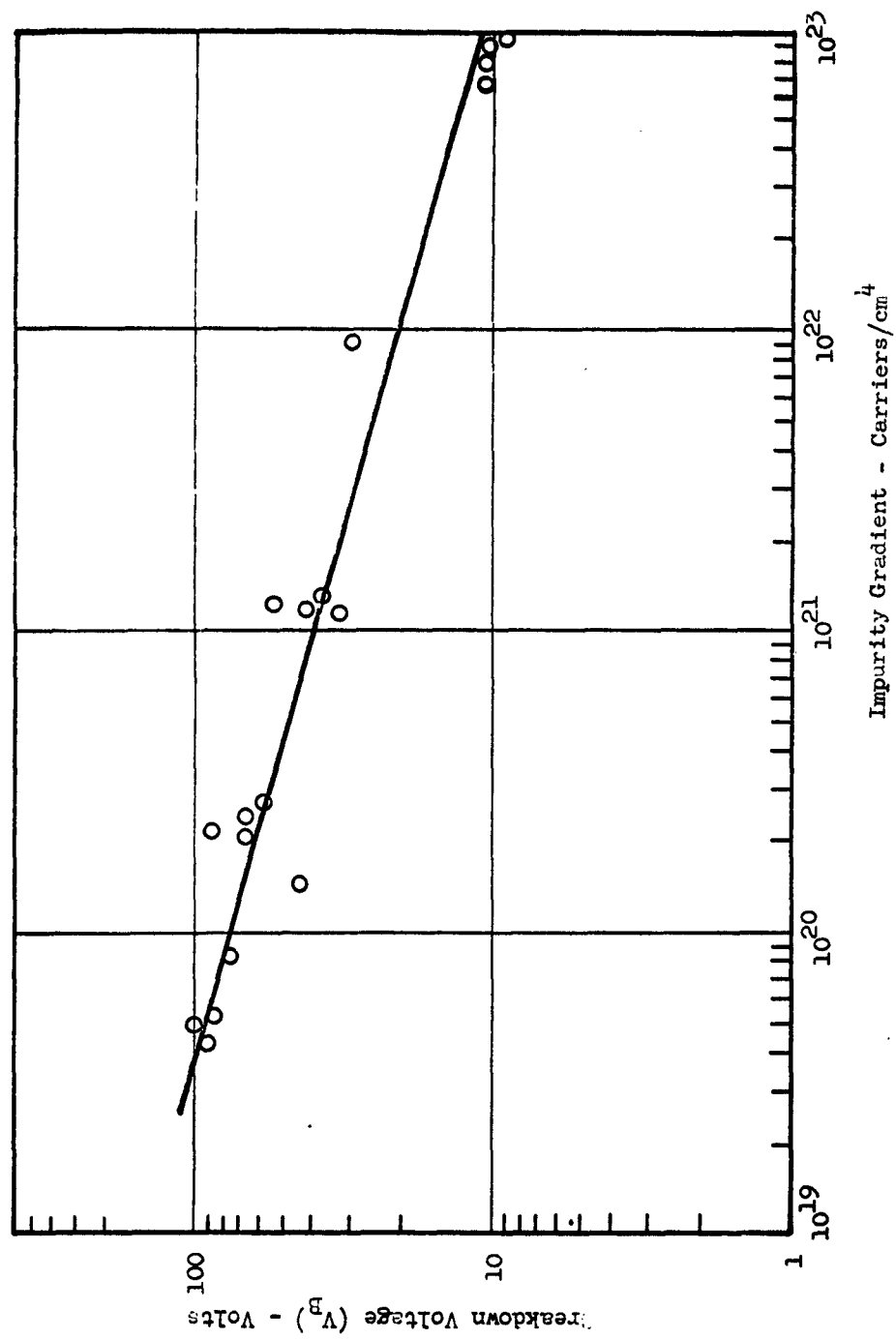


FIGURE 8 BREAKDOWN VOLTAGE AS A FUNCTION OF IMPURITY GRADIENT FOR PN GaAs JUNCTIONS

TABLE II

DATA FOR VARACTOR DIODE - DEVICE B

Diode No.	V_{BD} (volts)	C_{j0} (pf)	C_{j-2} (pf)	$C_{j \text{ min.}}$ (pf)	Q (0-2V)	f_{co-2} kmc	$f_{co \text{ max}}$ kmc
A795-5	33	.575	.388	.171	4.1	126	285
A796-24	32	.414	.293	.148	4.5	153	304
A801-19	44	.748	.512	.197	3.8	120	314
A816-1	33	.552	.381	.183	4.2	138	286
A823-6	30	.402	.288	.154	4.0	140	256
A921-10	28	.469	.330	.168	4.0	134	264
A45-3	38	.416	.302	.158	4.4	160	306
A75-10 ⁺	47	.512	.351	.195	6.9	220	396
A75-2 ⁺	20	.578	.391	.278	8.8	270	380
A75-15 ⁺	30	.579	.374	.223	5.9	168	270

+ Epitaxial Unit

C. Final Results For Phase II

Table II lists the characteristics of the best devices fabricated during Phase II of the contract. These devices were submitted to the Contracting Agency on February 28, 1963. These diodes meet the breakdown voltage junction capacitance and cutoff frequency goals set forth in the Second Quarterly Report. The cutoff frequency was measured using the technique described in the First Quarterly Report.

III. CONCLUSIONS

Improvements in process technology have made possible the fabrication of devices from melt grown GaAs with base widths of the order of 0.5 mils. High Q diodes have been fabricated with breakdown voltages in excess of 30 volts. A serious problem encountered in the fabrication of high breakdown diodes is the uncontrolled introduction during diffusion of p-type impurities which decreased the net carrier concentration of the material. This problem will be further investigated. Grown $p^+ - n - n^+$ diodes appear promising if the p^+ region is sufficiently doped. Diodes with breakdown voltages in excess of 100 volts have been made from such material.

PART II

I. PROGRAM FOR NEXT PERIOD

1. Improve cut-off frequency by reducing ohmic contact resistances.
2. Continue process developments for obtaining high cutoff frequency diode with breakdown voltages in excess of 30 volts.
3. Continue investigation of heat treatment effects on GaAs crystal, including epitaxially grown layers.