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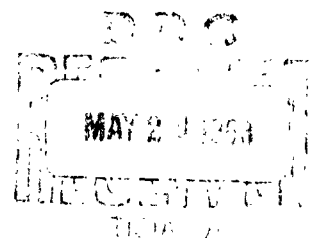
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APPLICATION STUDIES *of* COMBINED ANALOG-DIGITAL COMPUTATION TECHNIQUES

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APPLICATION STUDIES OF COMBINED
ANALOG-DIGITAL COMPUTATION TECHNIQUES

by

Frank B. Hills

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ABSTRACT

The concept of pulsed-analog computation in which high-speed, time-shared analog computing elements operate under the control of a digital computer is described. The design of a demonstration pulsed-analog computer developed at the Electronics Systems Laboratory is presented as well as a brief description of some problems solved by the computer.

The applicability of combined analog-digital computation techniques to a number of computational tasks is discussed. The computation tasks studied were those for which it was felt that combined analog-digital techniques would provide some advantages over purely analog or purely digital techniques. The computational tasks studied were:

1. The solution of partial differential equations— Here the studies indicated that combined analog-digital techniques can provide enough saving in computation time and computer hardware to make them useful in the control of chemical processes.
2. Speech Synthesis —These studies indicated that a general purpose combined analog-digital computer can be a very useful research tool where flexibility in the model of the system under study and the control parameters of that model is desired.
3. Digital Computer Cathode Ray Tube Display— Here the studies indicated that a fairly simple pulsed-analog computer can remove from the digital computer the time-consuming task of generating displays of the line drawing type and perform other tasks such as rotating a figure and stereoscopic display of a figure.

ACKNOWLEDGEMENTS

The studies described in this report have been carried out by a great number of student and staff participants. It would be difficult to give proper credit to all who deserve it, although the text and bibliography do indicate the principal contributors. Special mention should be made of Shu-Kwan Chan, who is co-author of the studies on speech synthesis, and of Alf Solbakken for many illuminating discussions.

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Finally, my thanks go to Mark Connelly, the project engineer, for many profitable technical discussions and for his editorial services. Also, the services of the drafting room and publications department in the preparation of this report are gratefully acknowledged.

FOREWORD

This report concludes a three-year program conducted by the M.I.T. Electronic Systems Laboratory for the Air Force Cambridge Research Laboratories. The program started with the design and construction of a demonstration computer based on a new computational technique conceived at the Electronic Systems Laboratory called pulsed-analog computation. In this computer, high-speed analog computing elements were operated on a time-shared basis under the control of a stored-program digital computer. Such a system combines the flexibility of a stored program, the equipment saving features of time-shared operations, and the speed and simplicity by which complex functions can be generated with analog elements.

After the demonstration computer showed the feasibility of the pulsed-analog techniques, the direction of the project's efforts was changed. Most of the previous investigations, made at the Electronic Systems Laboratory, of combined analog-digital computation techniques were oriented toward the problem of aircraft simulation. It was felt that the analog-digital techniques that had been developed might prove advantageous in other computation areas, and an investigation was started to find some of these areas.

A wide variety of different areas was investigated and, as is to be expected in an exploratory investigation of this sort, varying degrees of success were obtained. The objectives were: first, to find tasks where the combined analog-digital techniques could be applied and would offer distinct advantages over other available techniques, and second, to develop the theory of application to the point where some test computations could be made when a second generation hybrid computer becomes available in mid-1963. The design and construction of this improved analog-digital facility is being sponsored under another Air Force contract.

It is felt that these studies indicate that not only can combined analog-digital techniques be a serious competitor to other techniques, but that in some cases they can be used where other methods seem to be impractical. The studies indicate that combined analog-digital techniques are not limited to use in special-purpose computers, for areas were found where a general purpose combined analog-digital computer (i.e., a general purpose digital computer and a general purpose analog computer communicating with each other through a pulsed-analog interface) could be a powerful research tool.

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CHAPTER I

INTRODUCTION

This report is a summary review of a three-year research program on methods and applications of combined analog-digital computation to various problems in applied mathematics and engineering. This work was carried out by the Electronic Systems Laboratory under the sponsorship of the Air Force Cambridge Research Laboratories.

The first undertaking of this program was to design, construct, and test an experimental pulsed analog-digital computer in which high-speed analog elements operated under the control of a stored-program digital computer. Many of the special circuits required by this system were also developed by the project. Pulsed-analog computation was conceived at the Electronic Systems Laboratory during a previous investigation on computational techniques suitable for use in aircraft simulation.¹

Following the successful demonstration of this system, the research emphasis shifted to the study of a wide range of problem areas in which combined analog-digital computation techniques might be applied. The objective was to develop the theory of application to a point where some test computations could be made when a second generation hybrid computer becomes available in mid-1963. The design and construction of this improved analog-digital facility is being sponsored by another Air Force Contract.

Specifically, three computation areas have been found for which analog-digital computation techniques may be of great value. The areas are:

1. The Solution to Partial Differential Equations. In this area, one goal was to obtain a solution in faster than real-time to provide a basis for controlling systems that are described by partial differential equations. Two specific systems were investigated: a chemical reactor and a distillation column. A second goal was to study the implementation of well-known mathematical procedures for which no practical computer implementation had been devised.

¹ Superscripts refer to numbered items in the Bibliography.

2. Digitally-Controlled Analog Filters. In this effort, very flexible signal filtering systems have been designed and constructed. The flexibility is derived in two ways. First, by setting up a filter with analog elements the basic form of the filter can be easily changed. Second, through the use of pulsed-analog circuitry, parameters of the filter can be put under the control of a digital computer. Such a system should be a valuable tool in areas such as speech analysis and synthesis, the analysis of signals and systems by means of orthogonal functions such as the Laguerre functions, and analyses of signal spectrums.

3. Displays. It is felt that a small pulsed-analog computer between a digital computer and a cathode-ray tube display might reduce significantly the burden on the digital computer when generating line-drawing displays.

Unfortunately, this research program was effectively terminated before any of these ideas could be tried on the new combined analog-digital computer. However, some experimental work has been done in each of the above areas and the results are very promising.

There were four investigations, which, although they do not fit the main theme of analog-digital computation, were of interest to the project and for which the results have been published. They are:

1. Root Locus Displays⁴³
2. Ray-tracing in the Ionosphere^{44, 45}
3. A Time Sharing System for the PDP-1 Computer⁴⁶
4. A Controlled Experiment in Statistical Pattern Classification⁴⁷

The research is discussed in more detail in the following chapters, however, this discussion is quite brief since most of the topics have already been thoroughly documented. This report does contain a detailed description of the research done in the areas of digitally-controlled analog filters and displays for which a documented description does not exist elsewhere.

CHAPTER II

PULSED-ANALOG COMPUTATION

A. PULSED-ANALOG CONCEPT

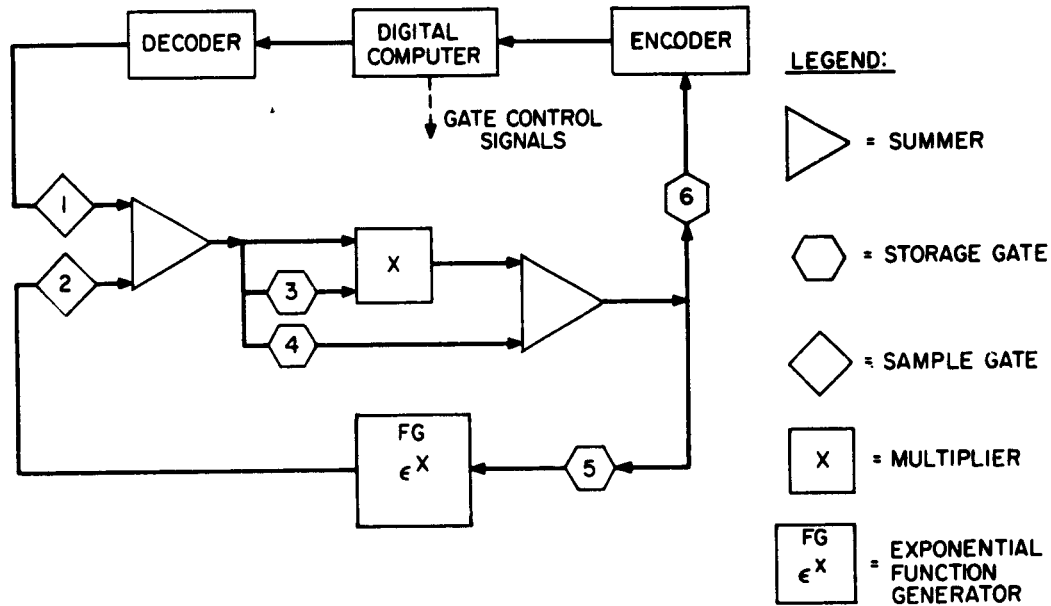
A pulsed-analog computer is made up of high-speed analog computing elements, e.g., summers, multipliers, function generators, etc., whose interconnections and driving signals are under the control of a stored program digital computer. This control is made possible through the use of sample gates and storage gates. The operation of these gates is as follows. A sample gate, when enabled by a digital signal, has an analog output equal to its analog input. When not enabled, the output is zero (ground). A storage gate, when enabled by a digital signal, stores a voltage on a capacitor equal to the analog input. However, when disabled the storage gate continues to supply an output equal to the stored value.

The operation of a pulsed-analog computer is very much like a digital computer in that the following are nearly always true:

1. The action of the computer is specified by programmed instructions, and each instruction is completed within the cycle time of the controlling digital computer.
2. Manipulations are carried out for discrete values of the independent variables.

However, the operation is also like an analog computer in that the data representation and the computations are analog in some cases, on a continuous, parallel basis. An example of a pulsed-analog computer and two programs are given in Fig. 1.

The following properties of the pulsed-analog computer make it attractive. First, a few analog elements operating in parallel can often make computations which would take many instructions to do digitally, thereby providing a simple way to get faster computation. For example, in Program I the complex functions $Ax + B$ and $C(e^{Ax+B}) + D$ have each been computed in one cycle time (instructions 3 and 6 respectively). Done digitally, these computations would require a number of cycle times. Of course, extra instructions are needed to transfer the data between the analog and digital domains. Another example is given in Program II where an implicit function is solved in one cycle time. Digitally this



PROGRAM I

1. DECODE AND STORE A
2. DECODE AND STORE B
3. DECODE x , STORE $Ax+B$
4. DECODE AND STORE C
5. DECODE AND STORE D
6. STORE AND ENCODE Ce^{Ax+B+D}

PROGRAM II

1. DECODE AND STORE E
2. DECODE AND STORE F
3. STORE AND ENCODE y WHERE $y = e^{Ey+F}$

GATES ENABLED

1, 3

1, 4

1, 5

1, 3

1, 4

2, 6

1, 3

1, 4

2, 5, 6

Fig. 1 Pulsed-Analog Computer and Programs

would not only require many cycle times to evaluate the exponential, but also many iterations of this computation before the desired value could be obtained.

The second property of pulsed-analog equipment is that the analog elements necessary for various computations can be time-shared. For example, one set of elements is time-shared in Program I. First they are used to compute $Ax + B$ and then to compute $C(e^{Ax+B}) + D$. With proper values in the storage gates these same elements can be used to multiply or to add.

The examples above illustrate only the properties of the pulsed-analog techniques and not the savings in computation time and equipment that is possible due to these properties. Illustrations of the latter are best given by referring the reader to the original reports covering the research outlined in Chapter II.

The remainder of this chapter outlines briefly the research done in constructing the first experimental pulsed analog-digital computer and computations carried out on it. The research reported in the chapters following make use of more general combined analog-digital computation techniques. However, these and other studies² indicate that the pulsed analog computer can also be useful in the interface between a digital computer and an analog computer, adding a degree of computational sophistication not obtainable with ordinary digital to analog conversion equipment alone.

B. THE TX-0 PULSED-ANALOG COMPUTER

The pulsed-analog computer developed at the start of this research effort consisted of a rack of plug-in pulsed-analog components developed by the project, operating under the control of the TX-0 digital computer. The TX-0 computer is an experimental computer built by the M.I.T. Lincoln Laboratories and since turned over to the Electrical Engineering Department. It is especially suited for experiments like the one being described here. The TX-0 is a general-purpose machine with some very useful input-output equipment for experimental work such as: an on-line Flexowriter, toggle-switch registers, an oscilloscope display, and a light pen input to be used in conjunction with the oscilloscope. Besides this,

the TX-0 has an IN-OUT register (called the Live Register-LR) through which data can be fed to or from external experimental equipment. By means of a special instruction, called the operate instruction, external equipment can be controlled by the program of the computer. In addition there is a generous supply of digital logic blocks available, so that each individual user can, in effect, patch together his own special-purpose input-output logic. An Epsco Datrac encoder (Model B-611) is available to convert analog voltages within the ranges of ± 1.000 , ± 10.00 or ± 100.0 volts into 11-bit digital numbers. Approximately 22 microseconds is required for each conversion.

With the TX-0 available, the design of the pulsed-analog computer consisted primarily of the design of the pulsed analog elements and of a special input-output logic for the control signals. The design goals for the pulsed-analog elements were: an accuracy of 0.1%, a settling time of less than 10 microseconds (an instruction time on the TX-0 is 12 microseconds) and a capability of being interconnected in a desired configuration with other elements of the family in patchboard fashion. Table I summarizes the component development program of the project.

The details of the complete pulsed-analog computer system are given in the report, A Pulsed Analog and Digital Computer for Function Generation (Ref. 9) by Joseph Binsack. This report describes the control logic for the analog gates and the pulsed-analog configuration. It also gives a quite detailed description of all the elements used. A brief description of the system follows. Figure 2 is a block diagram of the pulsed-analog computer. All information transferred between the TX-0 and the pulsed-analog equipment is done via the live register.

A word placed in the live register is interpreted in one of three ways:

1. As an instruction enabling a desired combination of analog storage and sample gates. A ONE in bit position j of the live register enables gate j in the pulsed-analog section.
2. As a data word that must be converted to analog form by the decoder for use in the pulsed-analog section.
3. As a word that is involved solely in digital operations, hence, is to be ignored by the pulsed-analog section.

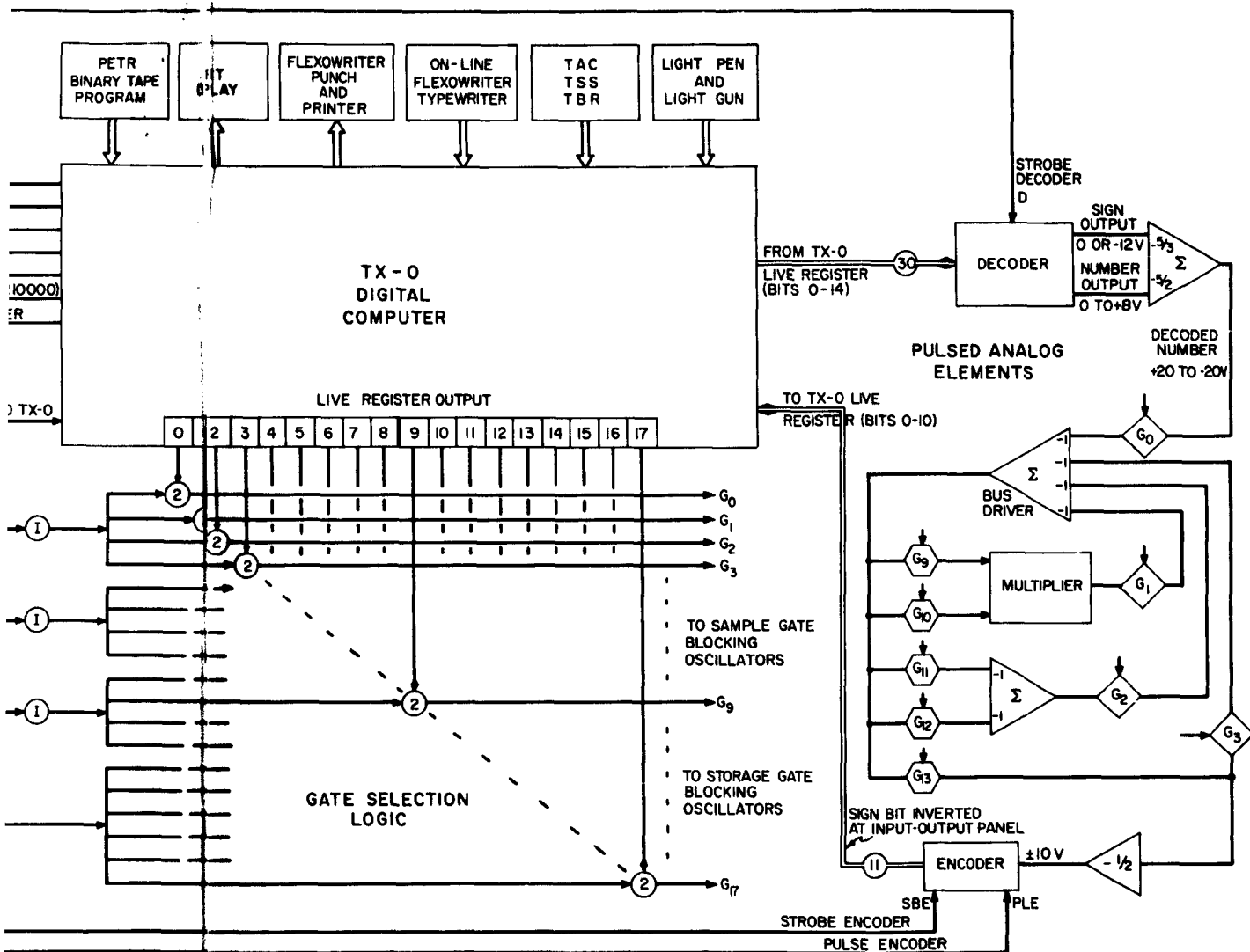


Fig. 2 TX-0 Pulsed-Analog Demonstration System



Table I
Pulsed-Analog Component Development Program

Device	Originator	Ref.	Number of Tubes (T) Trans. (X)	Accuracy	Volt. Range	Execute Time (μ sec)	Drift (mv)	Noise (mv)	Notes
Operational Amplifier	Leith	3	4T	.1%	± 20	4	$\pm .25$ (24 hrs)	10 p. to p.	3 Subminiature tubes, Philbrick K2P chopper stabilization (Goldberg) ± 5 ma. output current, DC Amplifier gain 2000 (open-loop)
Operational Amplifier	Gunion	4	26X	.5%	± 20	18	5 (24 hrs)	30 p. to p.	Solid-State, 25 to 60 kc. Transistor modulator and demodulator (Blecher stabilization) designed to drive capacitive memory cell, ± 160 ma. output current, Non-Linear Compensation
Gates	Massey	5	5X 1T	.25%	± 20	6	---	---	Four-Diode Storage gate with Blocking Osc. Trigger and output CF (Accuracy limited by CF) - hold time 20 ms.
		5	5X	.1%	± 20	6	---	---	Series-Shunt Four-Diode-Pair Sample gate with B.O. Trigger
Reciprocal Function Generator	Garzia	--	8T	.15%	2-20	---	---	---	Six-Segment Diode Function Generation - Leith Amplifiers
Multiplier-Divider	Blum	6	14T 40X	$\pm 1.2\%$	10-20	70 (6 inputs)	---	---	Diode Logarithmic and Anti-Logarithmic Circuits; Output, Five Nos. divided by a Sixth; Inputs limited to Range Machine .5 to 1.0. Outputs range from Machine 2 to 1/32; six Storage gates, two sample gates, 2 amps. required by system
Multiplier	Leith	7	16T	1%	± 20	8	10 (8 hrs.)	10 p. to p.	Quarter-Square Multiplier using Diode Squaring Elements
Encoder	Yates		45X	.75%	0-10	50,000	---	---	Solid-State Up-Down Counter, Decoder, Amp. and Comparator

Which of these interpretations is made is determined by the sequential machine shown in Fig. 2. The sequential machine has four states which produce the actions listed below.

- State 0: In this state, the contents of the live register are used only in digital operations. The sequential machine is put into this state by the instruction ple (pulse encoder), which also brings into the digital domain the results of a pulsed-analog computation. The sequential machine remains in this state until instructed to change state.
- A = 0
B = 0
- State 1: In this state, the contents of the live register are converted into analog form to be used as data in the pulsed-analog computation. Upon the completion of the conversion, the sequential machine goes into state 3 automatically. The sequential machine is put into state 1 by the instruction i01 (one of the special operate commands for external equipment).
- A = 0
B = 1
- State 2: In this state the contents of the live register determine the combination of analog gates that are to be enabled. The sequential machine is put into state 2 by the instruction i02 (one of the special operate commands for external equipment), and remains in this state until instructed to change state.
- A = 1
B = 0
- State 3: In this state the contents of the live register determine the combination of analog gates that are to be enabled. This state is used to direct the data decoded in state 1 to the proper analog storage gate. The sequential machine enters this state only following a conversion made in state 1, and when its gate enabling function is complete the sequential machine returns to state 1 ready to bring more data into the pulsed-analog section.
- A = 1
B = 1

Three simple problems were solved on the TX-0 pulsed-analog computer to investigate its performance. These computations are briefly described below. A complete description can be found in the references cited.

1. Binsack, J.H. - A Pulsed-Analog and Digital Computer for Function Generation - Ref. 9 - This report discusses a pulsed-analog computation in which values of an arbitrary function are computed from a piecewise linear approximation to the function. The values of the approximation F_i at the break points x_i and the slopes of the function between the break points

$$S_i = \frac{F_{i+1} - F_i}{x_{i+1} - x_i}$$

were stored in the memory of the digital computer. Given a value for x , a digital program found the break points such that

$$x_i \leq x < x_{i+1}$$

Using this information, the value of $F(x)$ was computed in the pulsed-analog domain using the equation

$$F(x) = F_i + (x - x_i) S_i$$

2. Massey, J.L. - A Time-Shared Analog Trigonometric Resolver - Ref. 5 - This report discusses a stabilized pulsed-analog computation of the sine and cosine functions. These functions can be computed as solutions to the pair of differential equations

$$\frac{dS}{d\theta} = C$$

$$\frac{dC}{d\theta} = -S$$

Some discrete approximations to these equations are

$$S_{i+1} = S_i + C_i \nabla \theta \quad (2.1a)$$

$$C_{i+1} = C_i - S_i \nabla \theta \quad (2.1b)$$

For various reasons, including the inaccuracies of the pulsed analog computing elements, functions of sine and cosine computed using Eqs. 2.1 are not stable (i.e., they will grow or decay as the computation proceeds). To prevent this instability, Massey made the computations according to the following equations

$$S_{i+1} = S_i + C_i \nabla \theta - \mu(S_i^2 + C_i^2 - 1) S_i \nabla \theta \quad (2.2a)$$

$$C_{i+1} = C_i - S_i \nabla \theta - \mu(S_i^2 + C_i^2 - 1) C_i \nabla \theta \quad (2.2b)$$

in which two terms have been added which force the computed values of the sine and cosine to obey the relation

$$S_i^2 + C_i^2 = 1$$

which insures the stability of the computations.

3. Bell, C.G. - The Pulsed Analog System for Evaluating Correlation Functions for Radar - Ref. 10 - This report discusses a correlation computation in which the correlation function of one hundred samples of simulated radar blip data, stored in digital memory, and thirty five samples of a filter function, stored in digital memory, was computed using pulsed-analog equipment. The correlation function computed was

$$C_j = \sum_{i=1}^N f_i d_{i+j-1}$$

where

C = correlation function

d = radar data

f = filter data

N = 35

j = 18, ..., 82

The above studies demonstrated that the pulsed-analog computation technique is feasible and have been valuable guides in the more advanced computer design now being constructed under another contract.²

CHAPTER III

SOLUTION OF PARTIAL DIFFERENTIAL EQUATIONS

Present digital techniques for solving partial differential equations require too much time and present analog techniques require too much equipment. The primary goal in this area was to see what could be done to remove or minimize these disadvantages with pulsed-analog techniques. Two studies were made of specific sets of partial differential equations that describe distributed process control systems. Two additional investigations were addressed to the solution of a more general class of partial differential equations.

1. Decanini, J. - Dynamic Simulation of a Distillation Column with a Combined Analog-Digital Computer - Ref. 11 - This report investigates the applicability of pulsed-analog computation techniques to the problem of simulating a 100-plate fractional distillation column. Illustrative programs are given showing two alternative ways of solving the distillation column equations. The first approach utilizes time-shared pulsed-analog equipment to reduce analog requirements to a minimum. In the second approach, one pulsed-analog configuration is set up to solve all the equations corresponding to a single plate. The same equipment is used to simulate each of the 100 plates in sequence, the digital computer being employed to store the key results at each plate. The program for the latter setup indicates that the calculations for the entire 100-plate column can be carried out at roughly three solutions per second.

2. Pedersen, E.V. - Chemical Process Control with a Hybrid Analog-Digital Computer - Ref. 12 - This report investigates the applicability of a pulsed-analog computer as an on-line control element for a continuous flow reactor with an unstable response to temperature perturbations. The problem here is that the system is very complex and difficult to return to a proper operating point after temperature perturbations. The solution is to simulate the system faster than real time so that predictions of responses to corrective actions can be obtained providing a means for choosing the best corrective actions. An analog-digital configuration was devised by means of which solutions could be computed 60 times faster than real time.

3. Max, S. - A Preliminary Investigation of the Analog-Digital Solution of Partial Differential Equations - Ref. 13 - The work in this report was partially supported by this project. The report presents a technique for computing solutions to partial differential equations of the form

$$\nabla^2 \phi = a \frac{\partial^2 \phi}{\partial x^2} + b \frac{\partial \phi}{\partial t} + c \phi + d \quad (3.1)$$

The following example shows the basic approach. Consider the one-dimensional diffusion equation

$$\frac{\partial^2 \phi(x, t)}{\partial x^2} = \frac{\partial \phi(x, t)}{\partial t} \quad (3.2)$$

One analog method for computing the solution to Eq. 3.2 produces the solution at only discrete points of x , called nodes, and makes use of the following approximation to Eq. 3.2

$$\frac{\phi(x_{i+1}, t) + \phi(x_{i-1}, t) - 2\phi(x_i, t)}{h_x^2} = \frac{d\phi(x_i, t)}{dt} \quad (3.3)$$

where the subscript i is the number of the node.

An analog computer configuration for Eq. 3.3 is shown in Fig. 3. If there are n nodes in x , $n-2$ such analog circuits will be required to compute the solution to Eq. 3.2 in the analog domain. The solution at the remaining two nodes are determined by the boundary conditions. The technique developed makes use of one configuration as shown in Fig. 3 on a time-shared basis. This approach is shown in Fig. 4. The computation can be explained as follows. As the solution at node x_i , $\phi(x_i, t)$ is computed; it is sampled and the value of the samples are placed in the memory of the digital computer. When the continuous function $\phi(x_i, t)$ is required in the analog computation it is reconstructed from the samples by an analog function generator based on Newton's forward interpolation formula³⁴ like that shown in Fig. 3 where the circuit for a second-order interpolation is shown. That is, the function generated is

$$\phi(x_{i+1}, t) = A_0 + A_1 t + \frac{A_2 t^2}{2!} \quad (3.4)$$

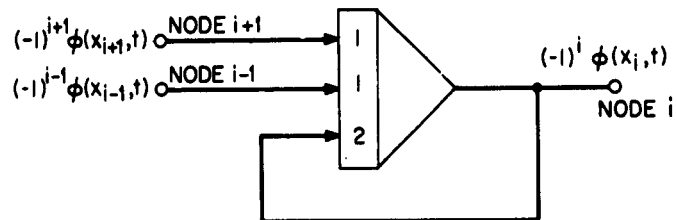


Fig. 3 Analog Configuration for Equation 3.3

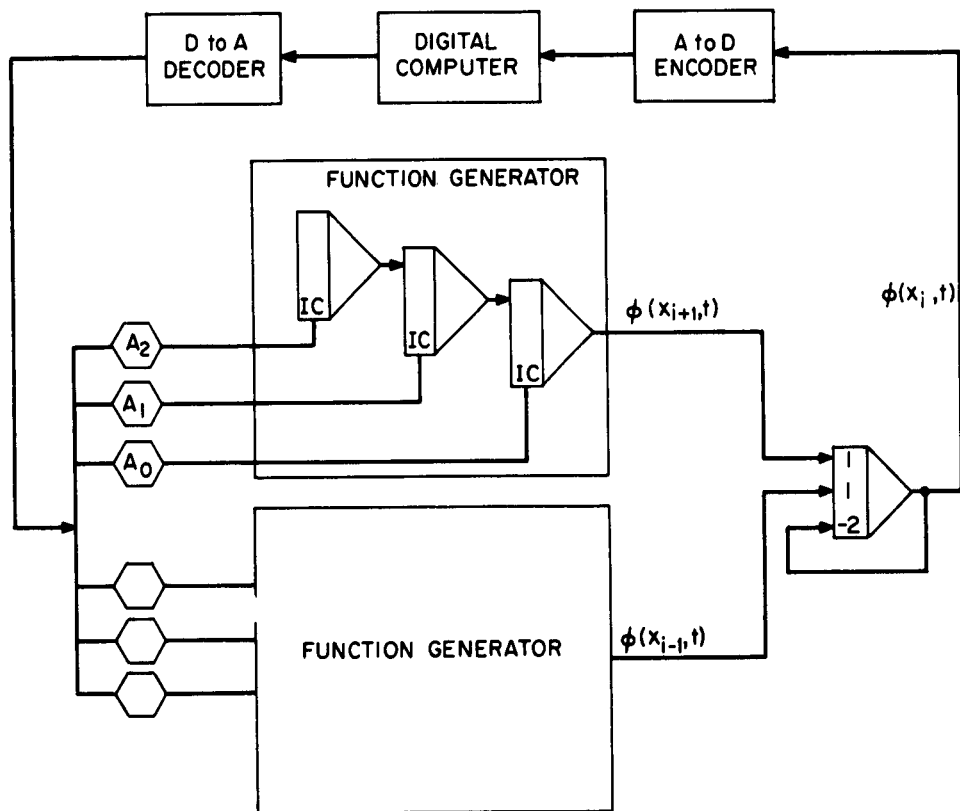


Fig. 4 Pulsed-Analog Configuration for Solving Equation 3.2

The A's are constants that can be computed from the samples stored in the digital memory.

The overall procedure is very much like the relaxation method used in digital computation. First, a set of sampled values for the time solutions at the nodes are chosen. These values can be arbitrary, except that they must satisfy the boundary conditions and the initial conditions. Starting with these assumed sample values, new values are computed by successively recomputing the $\phi(x_i, t)$'s, in the pulsed analog domain, until the result converges on the true solution as it does in the relaxation method.

The report describes this technique in terms of its application to the more general class of partial differential equations given in Eq. 3.1 and investigates the convergence of the computations. It also describes a simulation of the computation described in the example. The simulation was done on the TX-0 digital computer using numerical integration to replace the integrator in Fig. 3. Conservative estimates show that a factor of 10 in speed over a purely digital computation, can be realized by the pulsed-analog technique.

The above studies have shown that pulsed-analog computation techniques can be used to overcome the principal disadvantage of purely analog computations (excessive equipment requirements) and the principal disadvantage of purely digital computations (excessive computation time) in the simulation of systems described by partial differential equations.

The final study on this subject was made from a different point of view.

Moroney, R.M. - A Preliminary Investigation of Various Mathematical Techniques Suitable for Computer Implementation - Ref. 14 - The approach of this study was to investigate known mathematical techniques for solving problems, which have not been used for computation for lack of a suitable way to implement them on a computer. Most of the techniques discussed are for solving partial differential equations; however, other problems, such as linear programming, are also considered. The mathematical procedures are described in detail and some ideas are given for special combined analog-digital computing elements by which the techniques could be implemented.

CHAPTER IV

DIGITALLY-CONTROLLED ANALOG FILTERS

by
S.K. Chan and F.B. Hills

The research reported in this chapter and the following chapter were the last to be undertaken, by the project. Although significant results have been obtained, it is felt that what is reported here is only a beginning of what can be done in the areas. Ideas for extending the work are given at the ends of the chapters. It should be noted that this work has not been formally reported elsewhere and so these chapters will be of a more detailed nature than the previous ones. In fact, the intention is to give enough detail such that it will be a simple task to resume the investigations when the general purpose analog-digital computer is completed.

In our search for computational areas to which combined analog-digital computation techniques might be of value, a number of research areas were found in which filters having at least one of the following properties would be a valuable research tool:

1. Ease of obtaining a number of basic filter characteristics and ease of modifying these characteristics during an experiment, if necessary.
2. Filters with variable parameters and a simple but flexible means for controlling the parameters.

It was felt that if the filters could be constructed with a standard analog configuration in such a way that the proper parameters could be controlled by pulsed-analog techniques, these properties could be realized.

To test this idea, a specific problem was studied. The problem chosen was the synthesis of speech. This choice was made primarily because this is one area in which it would be advantageous to have filters with both of the properties mentioned. Most of this chapter is devoted to describing the research done on the applicability of combined analog-digital techniques to the speech synthesis problem. There is, however, a short discussion at the end of the chapter of other areas in which digitally-controlled filters may be a valuable tool.

A. SPEECH SYNTHESIS

1. Introduction

One way in which speech is synthesized is the following. A model of the vocal tract is set up with certain variable parameters by which the sounds necessary for speech can be generated and controlled. At present, research in this area is directed toward finding useful models and discovering how the parameters of these models should be varied to produce good speech.

In the past, synthesizers have been realized by constructing custom-built circuits. From the standpoint of anyone who is primarily interested in the properties of speech and the synthesis of speech, the design and construction of this special-purpose equipment is an expensive and time-consuming task. This is especially true when an initial investigation reveals that some significant changes in the model or its control are desirable. It is felt that these handicaps can be removed through use of a general purpose analog-digital computer. In such a computer, the synthesizer model could be set up in the analog portion and the digital portion could provide very versatile controls over the variable parameters. Clearly any changes desired will require only changes in the analog computer patching or the digital computer program.

The following is a report on an initial investigation of an analog-digital realization of a speech synthesizer. Although the investigation is only a beginning, some concrete results have been obtained in that fifteen phonemes and two words have been successfully generated on an experimental setup of the analog portion; and the framework for an analog-digital speech synthesizer has been established.

2. Synthesizer Model

The project being computer-oriented and not speech synthesis specialists, have drawn heavily on the literature for the synthesizer model and the parameter data necessary to generate the various phonemes. The basic model, suggested by Prof. K.N. Stevens of M.I.T. as the best one to start with, is the terminal

analog or resonance type synthesizer.^{15, 16} In this synthesizer, the input-output transfer characteristics of the vocal tract from the glottis to the mouth is simulated.

A block diagram of this type of synthesizer is shown in Fig. 5. The operation is as follows. The buzz generator and the modulator generate periodic signals representing those that occur at the glottis. The variable resonant circuits simulate the resonances of the vocal tract that produce the first three formant frequencies (lowest three frequencies that appear in the spectrogram of a phoneme). The control of these circuits is based upon measurements of the values and variations of the formant frequencies that occur in actual speech. The invariant resonant circuit produces an average of the effect of the higher formants that occur in actual speech.¹⁵ The circuit in the lower part of the figure is used to generate fricative sounds.

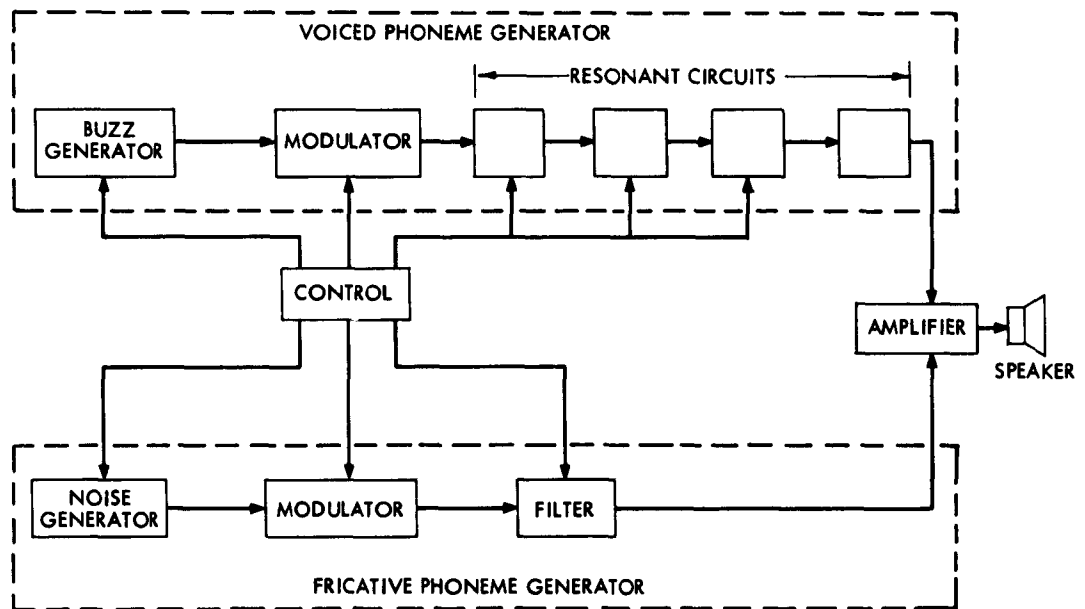


Fig. 5 Terminal Analog Synthesizer

3. Analog-Digital Realization

In this section a description of the various parts of the speech synthesizer is given and an analog digital system proposed for their realization.

a. Resonant Circuits The transfer function used for the resonant circuit can be derived from a circuit given in Reference 15:

$$\frac{e_o}{e_i} = \frac{\omega^2}{s^2 + bs + \omega^2} \quad (4.1)$$

For speech synthesis, the parameters of these circuits that are to be controlled are the resonant frequency and, to a lesser extent, the bandwidth. For sufficiently high Q, the resonant frequency and bandwidth are approximately equal to the quantities ω and b respectively that appear in Eq. 4.1. In any case, the parameters are determined by these quantities.

A way in which Eq. 4.1 can be realized with an analog-digital computer is shown in Fig. 6. This is a standard analog arrangement for Eq. 4.1, except that the coefficients can be controlled by the digital computer.

b. Filter in the Fricative Section The transfer function used for the filter in the fricative section can be found in References 17 and 18:

$$\frac{e_o}{e_i} = \frac{s^2 + Bs + \Omega^2}{s^2 + bs + \omega^2} \quad (4.2)$$

Here the parameters that are to be controlled are the resonant frequency, the bandwidth, the frequency at which the zeros occur and the bandwidth of the anti-resonance. Again for sufficiently high Q's and also for a sufficient difference between the frequencies at which the resonance and anti-resonance occur, the resonant frequency, resonant bandwidth, zero frequency, and anti-resonant bandwidth are approximately equal to the quantities ω , b , Ω , and B respectively. In any case, the parameters are determined by these quantities.

A way in which Eq. 4.2 can be realized with an analog-digital computer is shown in Fig. 7. The actual transfer function of the circuit in Fig. 7 is:

$$\frac{e_o}{e_i} = - \frac{s^2 + (b-b')s + \Omega^2}{s^2 + bs + \omega^2} \quad (4.3)$$

for which

$$B = b-b'$$

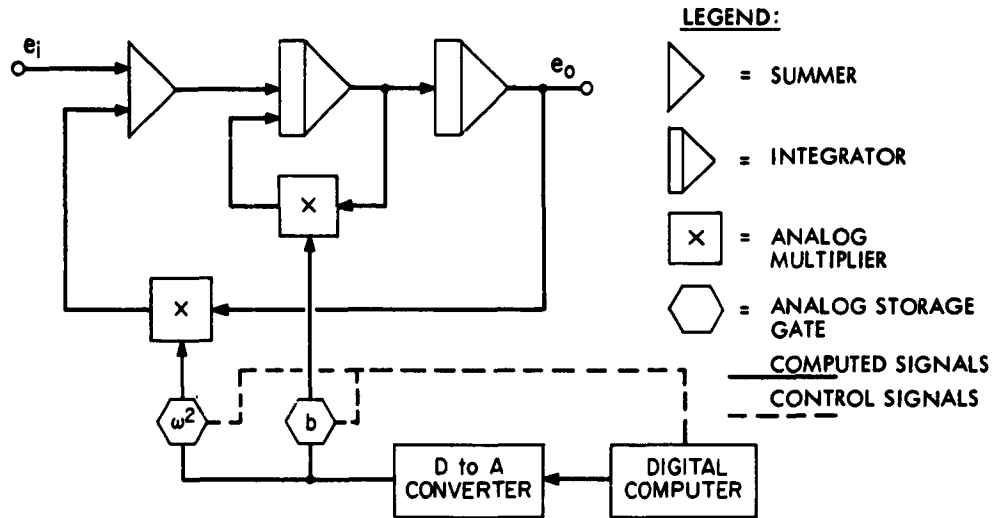


Fig. 6 Analog-Digital Computer Realization of a Variable Resonant Circuit

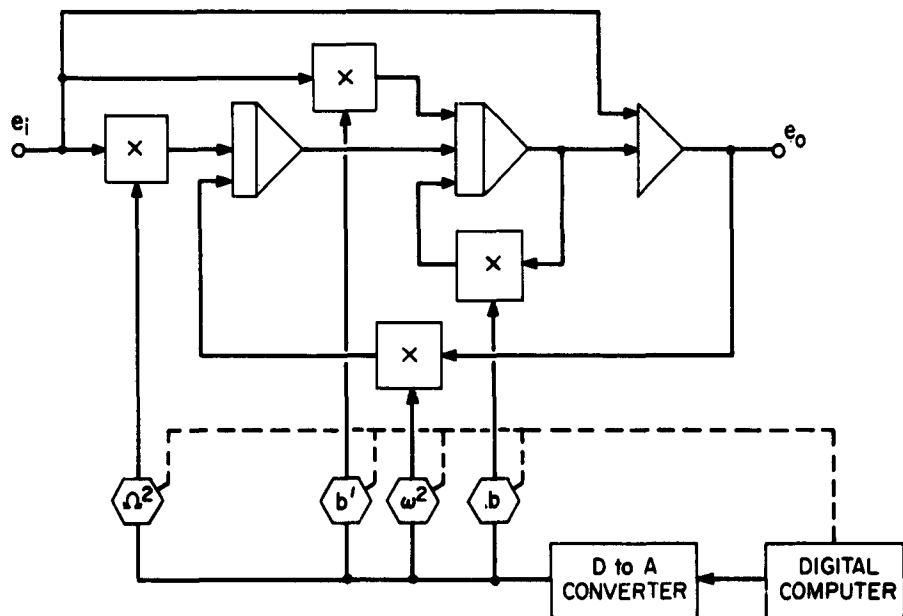


Fig. 7 Analog-Digital Computer Realization of the Filter in the Fricative Generator

c. Buzz Generator The waveform of the buzz generator signal can be found in Reference 19 and is shown in Fig. 8. The parameters of this signal that are to be varied are frequency and amplitude. The latter is controlled by the modulator.

An analog-digital computer realization of the buzz generator and the associated modulator is shown in Fig. 9. The operation of this circuit is as follows. The inner loop is a bistable circuit, the output being plus or minus some fixed voltage. This output voltage is integrated until the integrator output reaches a value which causes the bistable circuit to change state, and the process repeats, generating a square wave. The multiplier, driven by storage gate ω , controls the rate at which the integrator output voltage increases, and, consequently, the frequency of the square wave. The circuit containing C_1 , R_3 and the diode differentiates the square wave and clips the negative-going portions leaving the waveform shown in Fig. 8. The multiplier driven by storage gate A controls the amplitude of the signal.

d. Noise Generator The specifications for the noise generator can be found in Reference 20. The generator has a spectrum which is flat between 3 and 8 kc and drops off at 18 db/octave at higher and lower frequencies.

These are the specifications on the noise generator for the specific fricatives investigated. Other specifications are required for other fricatives.¹⁸ Sufficient investigation has not been made of the noise specifications so that a realization can be proposed. However, as a first approximation a white noise source could be employed, and digitally-controlled filters used to obtain the proper spectrum.

4. Experimental Tests

From the above discussion, it can be seen that the analog-digital computer realization can be regarded primarily as an analog computation with some digital control. Consequently, in studying the feasibility of the realization, the first questions to ask are; "Can the analog portion be set up using standard analog computing elements, and what problems will be encountered in so doing?" These are important questions, for audio frequencies are greater than those normally encountered in analog computation.



Fig. 8 Buzz Generator Signal

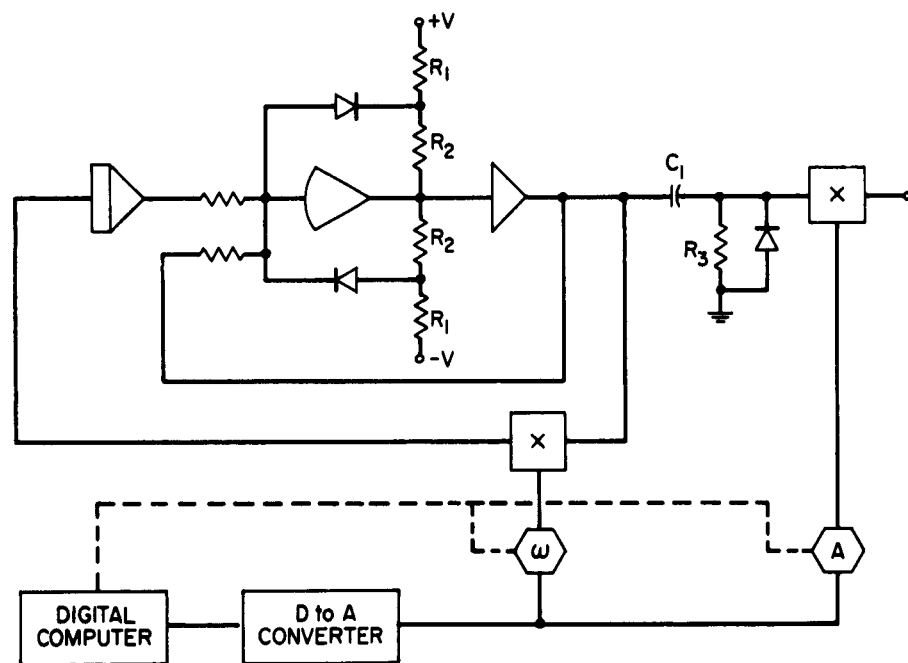


Fig. 9 Buzz Generator and Modulator

To answer these questions the experimental speech synthesizer shown in Fig. 10 was implemented. The upper portion of the figure was set up on a REAC computer with the values shown in Table 2 for the integrator feedback capacitors. No other modifications were necessary. The additional

Table 2

Feedback Capacitors	
Resonant Circuit	Cap. Value pfd
1	2200
2	680
3	470
4	470
K_1	220
K_2	100

amplifier in the buzz generator section was used to eliminate undesired spikes from the derivative of the square wave.

The lower section was set up using Philbrick operational amplifiers, (K2-W's in the noise generator, and K2-X's in the filter section.) Input resistor values of 1 megohm were used for gain of one input. The noise source used was a back-biased diode²¹ followed by a transistor amplifier, the circuit for which is shown in Fig. 11. The noise source was designed to have a flat spectrum over as wide a frequency range as possible so that it could be used as a general source for the generation of fricatives. Consequently, three RC circuits were used to obtain the desired spectrum for the particular fricatives investigated. The RC circuits used are shown in Fig. 12.

The information necessary for the generation of speech sounds using the experimental synthesizer comes from many sources. This data is summarized in Table 3. The sources of this data, some discussion of the data usage, and the results obtained are given below.

a. Vowels The frequencies of the vowel formants 1, 2, and 3 and of the buzz sources were obtained from Reference 22. The bandwidths for formants 1, 2, and 3 are averages of entries in a table in Reference 20. The fourth formant data is from Reference 15.

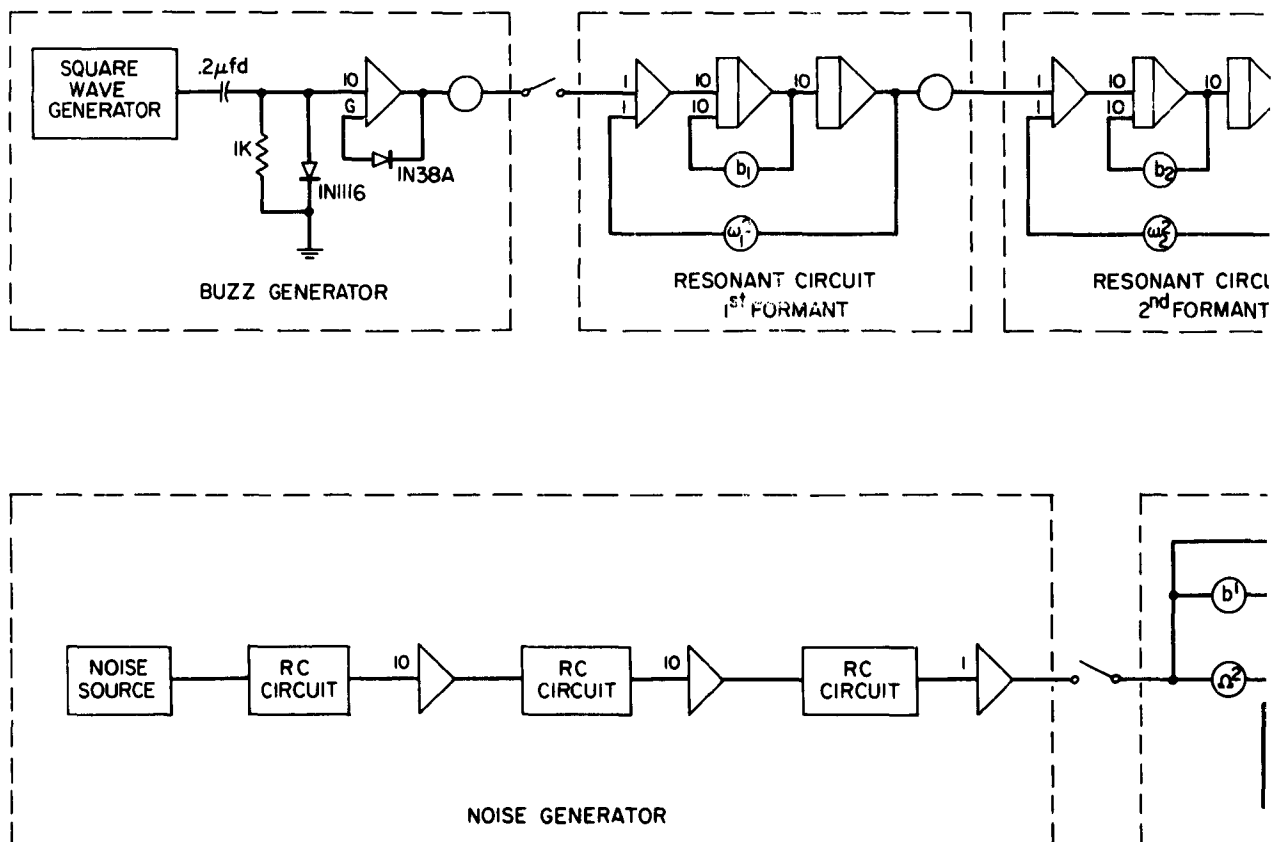
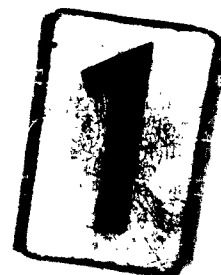


Fig. 10 Exper



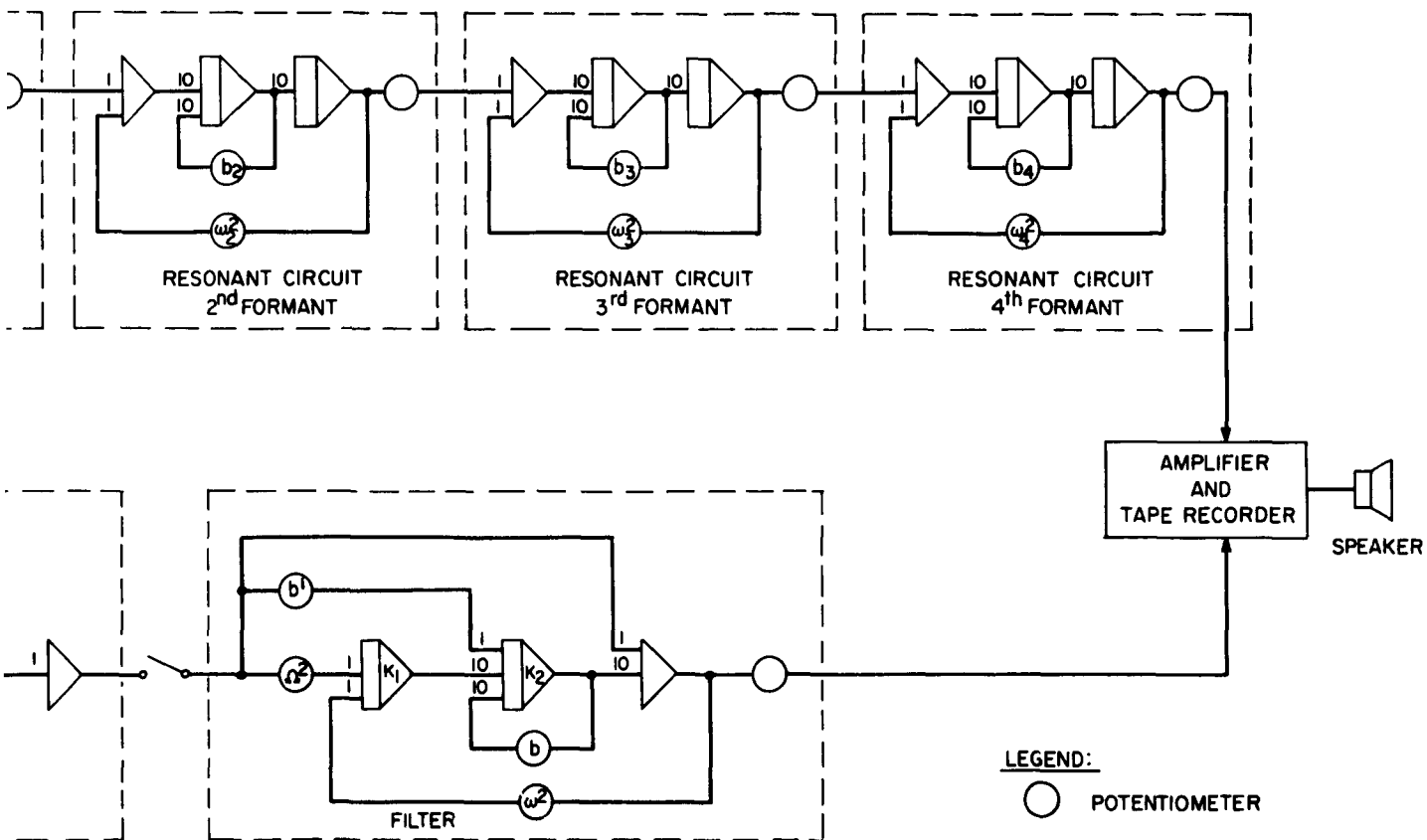


Fig. 10 Experimental Speech Synthesizer

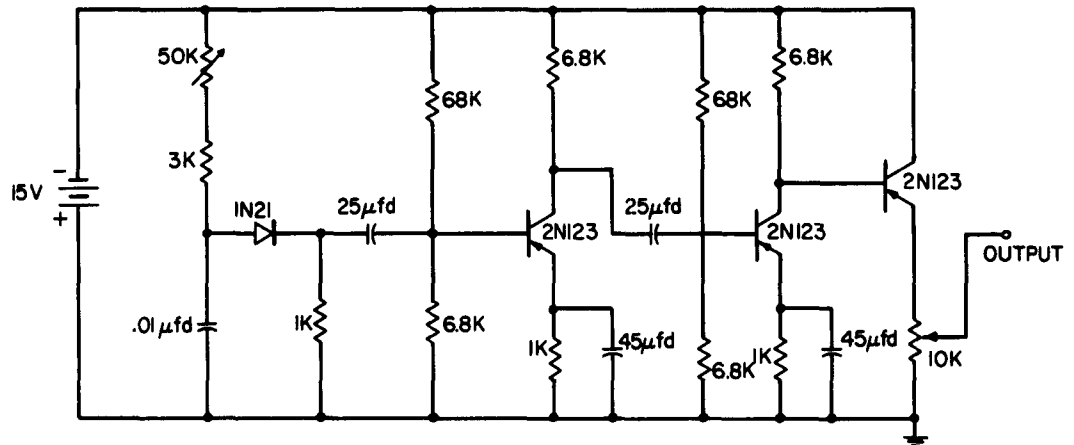


Fig. 11 Noise Source

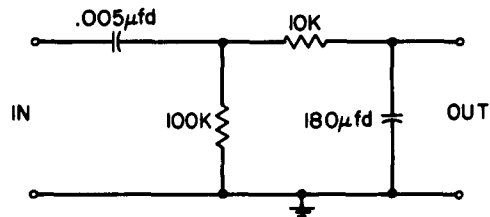


Fig. 12 RC Filter in Noise Generator

The vowel sounds generated by the experimental synthesizer, when tuned according to the above data, were easily recognized.

b. Fricatives The data for the fricatives were obtained from Reference 18. The phonemes $|\int|$ and $|s|$ generated according to the above data, were easily recognized. The phonemes $|f|$ and $|\theta|$ are grouped together, for it is apparently not possible to distinguish between them when they occur as just isolated sounds.¹⁸ According to Reference 18, $|f, \theta|$ requires some additional low frequency noise excitation over that required for $|\int|$ and $|s|$. As a rough approximation for the experimental synthesizer, the noise source was connected directly to the filter, by-passing the spectrum-shaping RC circuits. The resulting sound was recognized as $|f, \theta|$.

c. Other Phonemes The above phonemes have the property that they can be recognized in the form of isolated sounds. For other phonemes, this is not true (for example, the nasals $|m|$, $|n|$, and $|\eta|$). For the nasals it has been observed that the transition between the nasal and the following vowel is important to the proper identification of the nasal consonant.²⁴

Briefly, nasals can be generated in the following way. (This data comes from References 20, 23, 24, and 25.) The resonant circuits of the voiced phoneme generator are tuned so that the formant frequencies vary as shown in Fig. 13. The third and fourth formants are apparently the same

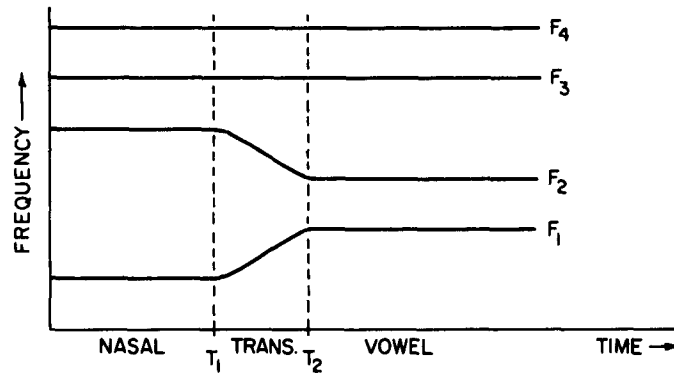


Fig. 13 Formant Transitions for Nasal Consonants

as those of the vowel that follows the nasal. The first formant starts at 200 cps with a bandwidth of 200 cps and changes to those of the vowel. The second formant starts with a bandwidth of 150 cps and the frequencies shown in Table 4, if the vowel following is $|a|$.

Notice in Table 3 and Table 4 that the second formant of $|a|$ lies in the range of the second formant of $|m|$. Consequently, by building one simple control circuit for F_1 the experimental synthesizer could be tested for:

1. the generation of a nasal constant
2. the generation of two phonemes in succession
3. the correct operation of the analog circuitry under the dynamic conditions it will be subject to under digital control.

Table 3

Phoneme Data

Phoneme	F ₁		F ₂		F ₃		F ₄		Zero		Buzz
	Freq*	Bdwth*	Freq	Bw	Freq	Bw	Freq	Bw	Freq	Bw	Frequency
i	270		2290		3010						136
I	390		1990		2550						135
ɛ	530		1840		2480						130
æ	660		1720		2410						127
a	730		1090		2440						124
ə	570	50	840	60	2410	100	3200	100			129
U	440		1020		2240						137
u	300		870		2240						141
ʌ	640		1190		2390						130
ʊ	490		1350		1690						133
ʃ	2500	500							3600	1500	
s	5000	700							2750	1100	
for f	8000	1000							5900	900	
m	200	200	1090	150	See Text						See
b	200	50	1000	150							Text

* Frequencies and Bandwidths in CPS

(The changes in the bandwidths were neglected because their effect is only minor compared to those of the formants.)

Table 4

Second Formants for Nasal Consonants

<u>Nasal</u>	<u>Second Formant Range (vowel a)</u>
m	900 - 1100
n	1600 - 1800
ŋ	2300 - 2500

Figure 14 shows the circuitry used for the control of the first formant. A description of the operation of this circuit follows. As proposed in the analog-digital realization, the coefficient ω^2 was made adjustable by the insertion of a high-speed analog multiplier in the circuit. The multiplier used was designed by Solbakken.²⁶ This multiplier requires as inputs both the variables and the negatives of the variables to be multiplied. This explains the need for two of the amplifiers shown. From Fig. 13 and Tables 3 and 4, it can be seen that to generate $|m_a|$, the first formant must be held at 200 cps for a period of time and then raised to 730 cps. This action is generated by the remainder of the circuit. The function generated and the circuit for the generator are shown in Fig. 15. The voltage levels 1.1 and 10 of the function generated produce the resonant frequencies of 200 and 730 cps respectively when a multiplier with a gain of unity at 10 volts is used (i.e., 10 volts on both inputs produces an output of 10 volts). Potentiometer I in Fig. 14 sets the initial value of the IN voltage of the function generator. The integrator increases the IN voltage linearly at a rate controlled by Potentiometer T. The switch, which applies the step to the integrator and resets the integrator, is ganged to the switch that connects the buzz generator to the resonant circuits. With these controls, the time of the two parts of $|m_a|$ (nasal and transition) can be adjusted. Reference 20 gives the following values for these time periods:

nasal	50 - 100 m sec.
transition	20 - 50 m sec.

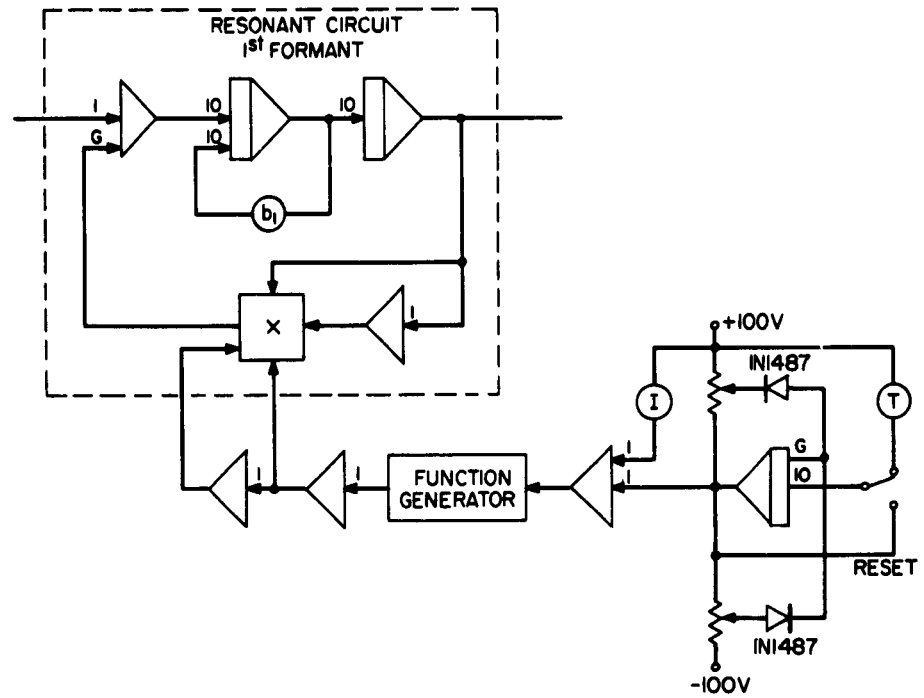


Fig. 14 First Formant Control Circuit

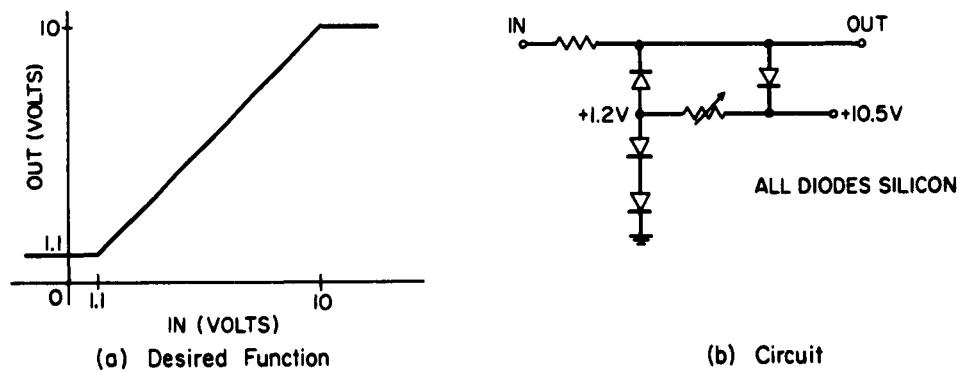


Fig. 15 Function Generator

The sounds generated under the control of this circuit were easily recognized as the word "ma".

A further test was made on the above circuit by using information from Reference 20. This Reference says that by using the circuit for the nasal [m] with a more narrow bandwidth for the first formant and by making the time periods T_1 and $T_2 - T_1$, in Fig. 13 smaller, the phoneme [b] (or with the above control circuit, the word "ba") can be generated. The word "ba", so generated, was easily recognized and differentiated from the word "ma" from recordings of the two words.

5. Characteristics of the Analog Computation

The following is concerned with the characteristics of the analog computer as used in the speech synthesizer. The emphasis here is on the performance of and specifications on the analog elements used at audio frequencies.

To begin, two simple but important facts should be noted. First, because the signals are at audio frequencies, the operational amplifiers must have sufficient bandwidth. This is not a great problem with the elements currently available. However, this was the reason in the experimental synthesizer that the fricative filter was not realized on the REAC, where the amplifier bandwidth is less than 5 kc.¹⁷

Second, at these audio frequencies, there is no need to be specially concerned with amplifier drift. Consequently, the circuits can be constructed with fairly inexpensive operational amplifiers. Actually, the resonant circuits, because of the high dc gain of the integrator amplifiers can be made self-stabilizing by placing the summer last in the forward path. Of course, capacitive coupling will also eliminate any drift problem.

The more enlightening characteristics found for the analog elements are discussed below. The first characteristic is the need for very high gain, as can be seen from the scaling of a resonant circuit. The circuit is shown in Fig. 16. The transfer function of this circuit is:

$$\frac{e_o}{e_i} = \frac{-G_1 G_2 G_3}{s^2 + BG_2s + \Omega^2 G_1 G_2 G_3} \quad (4.4)$$

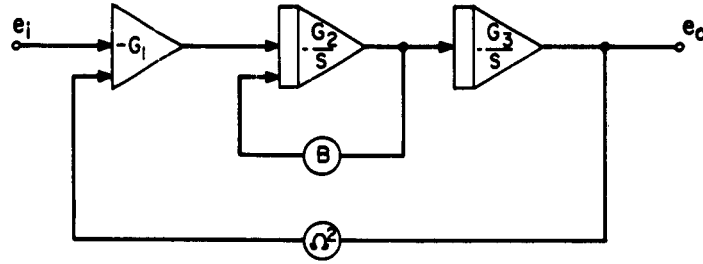


Fig. 16 Resonant Circuit

By comparing Eqs. 4.1 and 4.4 it can be seen that

$$\Omega^2 G_1 G_2 G_3 = \omega^2 \quad (4.5)$$

That is, the loop gain must equal the square of the value of the resonant frequency in radians per second. (The numerators of Eqs. 4.1 and 4.4 need not be the same, for the numerator affects only the amplitude of the signal, i.e., the volume of the sound.) To give some idea of the magnitude of the loop gain, consider the highest resonant frequency given in Table 3, namely 8 kc. For this resonant frequency, a loop gain of 2.5×10^9 is required.

How this gain is obtained can be seen from an analysis of the computing elements. The analysis will be made on the models shown in Fig. 17. These

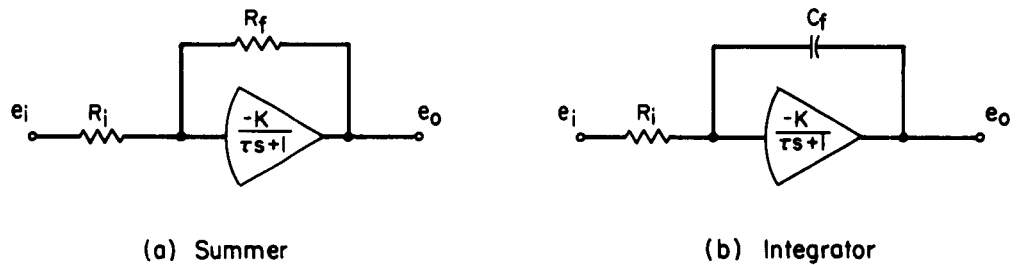


Fig. 17 Computing Element Models

are the simplest models that can be used to show the effect of the high frequencies on computer performance. However, analyses can be made on

more complex models such as those used by Dow.²⁸ Such an analysis should be made by anyone interested in a more complete study, for it shows the effects of stray capacitances and leakage resistances which become significant at high frequencies.

First, it will be shown that very little of the required gain can be obtained from the summer or the multiplier ω^2 , since multipliers are constructed using summers.

The transfer function of the summer model is

$$\frac{e_o}{e_i} = \frac{\frac{-K}{(R_i/R_f)(K+1) + 1}}{\frac{\tau[(R_i/R_f) + 1]}{(R_i/R_f)(K+1) + 1} s + 1} \quad (4.6)$$

From Eq. 4.6, it can be seen that the gain will be approximately constant at the value

$$G = \frac{-K}{(R_i/R_f)(K+1) + 1} \quad (4.7)$$

from d.c. to a frequency of

$$\omega_b = \frac{(R_i/R_f)(K+1) + 1}{\tau[(R_i/R_f) + 1]} \quad (4.8)$$

Now from Eq. 4.7, it can be seen that for the gain to be stable, i.e., independent of variations in the gain, of the operational amplifier, the following must be true:

$$(R_i/R_f)(K+1) \gg 1 \quad (4.9)$$

If this is the case, then Eq. 4.8 reduces to

$$\omega_b \approx \frac{K}{\tau(1+G)} \quad (4.10)$$

From the transfer function of the model for the operational amplifier, the following is approximately true

$$\frac{K}{\tau} = \omega_c \quad (4.11)$$

where ω_c (cross-over frequency) is the frequency at which the open-loop gain of the operational amplifier becomes unity. From Eqs. 4.10 and 4.11, the following can be obtained

$$\omega_b (G+1) = \omega_c \quad (4.12)$$

Values of approximately one megacycle for the cross-over frequency are currently obtainable. If a bandwidth of 10 kc is used in the fricative filter (i.e., filter must resonate at 8 kc), Eq. 12 shows that a gain of only 100 is possible from a summer.

The next step is to show that the necessary loop gain for the resonant circuits can be obtained from the integrators, and to indicate the limitations involved.

The transfer function of the integrator model is

$$\frac{e_o}{e_i} = \frac{-K}{R_i C_f \tau \left[s^2 + \left(\frac{K+1}{\tau} + \frac{1}{R_i C_f} \right) s + \frac{1}{R_i C_f \tau} \right]} \quad (4.13)$$

The denominator of Eq. 4.13 can be factored by the quadratic formula giving

$$\omega_1, \omega_h = \frac{-b \pm b \sqrt{1 - \frac{4c}{b^2}}}{2} \quad (4.14)$$

where

$$b = \frac{K+1}{\tau} + \frac{1}{R_i C_f}$$

$$c = \frac{1}{R_i C_f \tau}$$

Because $K \gg 1$, $4c/b^2 \ll 1$ is also true. Consequently, the radical in Eq. 4.14 can be expanded using the binomial series from which the following can be obtained

$$\omega_1 \approx \frac{-1}{R_i C_f (K+1) + \tau}$$

$$\omega_h \approx - \left[\frac{K+1}{\tau} + \frac{1}{R_i C_f} \right]$$

From this, Eq. 4.13 can be written as

$$\frac{e_o}{e_i} = \frac{1}{R_i C_f} \left[\frac{-K/\tau}{\left(s + \frac{1}{R_i C_f (K+1) + \tau}\right) \left(s + \frac{K+1}{\tau} + \frac{1}{R_i C_f}\right)} \right] \quad (4.15)$$

For frequencies in the range

$$\frac{1}{R_i C_f (K+1) + \tau} < \omega < \frac{K+1}{\tau} + \frac{1}{R_i C_f} \quad (4.16)$$

Equation 4.15 is effectively of the form

$$\frac{e_o}{e_i} = \frac{-G}{s} = \frac{-1}{R_i C_f s} \left[\frac{1}{\frac{K+1}{K} + \frac{\tau}{K R_i C_f}} \right] \quad (4.17)$$

which is the transfer function of an integration. From Eq. 4.17, it can be seen that for the gain to be stable, i.e., independent of variations in the gain of the operational amplifier, the following must be true

$$\frac{\tau}{K R_i C_f} \ll 1 \quad (4.18)$$

In this case the integrator gain simplifies to

$$G = \frac{1}{R_i C_f} \quad (4.19)$$

From Relation 4.18, two restrictions on the gain can be found:

$$G \ll \omega_c \quad (4.20)$$

and Relation 4.16, which reduces to

$$\frac{G}{K+1} < \omega < \omega_c \quad (4.21)$$

Relation 4.21 shows that high gains can be obtained at the expense of an increase in the lowest permissible frequency. However, a gain equal to 6 times the d.c. gain of the operational amplifier produces a lowest permissible frequency of 1 cps, which is well below the audio frequency range. Consequently it is Relation 4.20 that specifies the limit on permissible gain. An illustration of these points follows. Integrator K_2 in the fricative filter of Fig. 10 was constructed from a Philbrick K2-X amplifier and the following impedances

where ω_c (cross-over frequency) is the frequency at which the open-loop gain of the operational amplifier becomes unity. From Eqs. 4.10 and 4.11, the following can be obtained

$$\omega_b (G+1) = \omega_c \quad (4.12)$$

Values of approximately one megacycle for the cross-over frequency are currently obtainable. If a bandwidth of 10 kc is used in the fricative filter (i.e., filter must resonate at 8 kc), Eq. 12 shows that a gain of only 100 is possible from a summer.

The next step is to show that the necessary loop gain for the resonant circuits can be obtained from the integrators, and to indicate the limitations involved.

The transfer function of the integrator model is

$$\frac{e_o}{e_i} = \frac{-K}{R_i C_f \tau \left[s^2 + \left(\frac{K+1}{\tau} + \frac{1}{R_i C_f} \right) s + \frac{1}{R_i C_f \tau} \right]} \quad (4.13)$$

The denominator of Eq. 4.13 can be factored by the quadratic formula giving

$$\omega_1, \omega_h = \frac{-b \pm b \sqrt{1 - \frac{4c}{b^2}}}{2} \quad (4.14)$$

where

$$b = \frac{K+1}{\tau} + \frac{1}{R_i C_f}$$

$$c = \frac{1}{R_i C_f \tau}$$

Because $K \gg 1$, $4c/b^2 \ll 1$ is also true. Consequently, the radical in Eq. 4.14 can be expanded using the binomial series from which the following can be obtained

$$\omega_1 \approx \frac{-1}{R_i C_f (K+1) + \tau}$$

$$\omega_h \approx - \left[\frac{K+1}{\tau} + \frac{1}{R_i C_f} \right]$$

From this, Eq. 4.13 can be written as

$$\frac{e_o}{e_i} = \frac{1}{R_i C_f} \left[\frac{-K/\tau}{\left(s + \frac{1}{R_i C_f (K+1) + \tau}\right) \left(s + \frac{K+1}{\tau} + \frac{1}{R_i C_f}\right)} \right] \quad (4.15)$$

For frequencies in the range

$$\frac{1}{R_i C_f (K+1) + \tau} < \omega < \frac{K+1}{\tau} + \frac{1}{R_i C_f} \quad (4.16)$$

Equation 4.15 is effectively of the form

$$\frac{e_o}{e_i} = \frac{-G}{s} = \frac{-1}{R_i C_f s} \left[\frac{1}{\frac{K+1}{K} + \frac{\tau}{K R_i C_f}} \right] \quad (4.17)$$

which is the transfer function of an integration. From Eq. 4.17, it can be seen that for the gain to be stable, i.e., independent of variations in the gain of the operational amplifier, the following must be true

$$\frac{\tau}{K R_i C_f} \ll 1 \quad (4.18)$$

In this case the integrator gain simplifies to

$$G = \frac{1}{R_i C_f} \quad (4.19)$$

From Relation 4.18, two restrictions on the gain can be found:

$$G \ll \omega_c \quad (4.20)$$

and Relation 4.16, which reduces to

$$\frac{G}{K+1} < \omega < \omega_c \quad (4.21)$$

Relation 4.21 shows that high gains can be obtained at the expense of an increase in the lowest permissible frequency. However, a gain equal to 6 times the d.c. gain of the operational amplifier produces a lowest permissible frequency of 1 cps, which is well below the audio frequency range. Consequently it is Relation 4.20 that specifies the limit on permissible gain. An illustration of these points follows. Integrator K_2 in the fricative filter of Fig. 10 was constructed from a Philbrick K2-X amplifier and the following impedances

$$R_i = 100 \text{ k}\Omega$$

$$C_f = 100 \text{ pf}$$

Philbrick gives the following data for the K2-X amplifier :

$$\text{Bandwidth at unity gain} = 250 \text{ kc.}$$

$$K = 3 \times 10^4$$

From Eq. 4.10 and the bandwidth figure given above ω_c can be calculated

$$\omega_c = 500 \text{ kc}$$

With this data the following characteristics of the integrator can be calculated from the relations derived above.

$$G = 10^5$$

$$3 \text{ cps} < \omega < 500 \text{ kc}$$

$$\tau/KR_iC_i \approx .03 \ll 1$$

The last relation above and Eq. 4.17 shows that the integrator gain is stable, e.g., a decrease in K to half its normal value would change the integrator gain by only 3 percent. This data gives some indication of the characteristics of the integrators used in the fricative filter, and also indicates the order of magnitude of the gain that can be obtained with currently available equipment.

Another characteristic became evident when the resonant circuits were set up and tuned. It was found that the error in the square of the resonant frequency was on the order of one percent. (more precise measurements were not possible with the equipment available). The damping required, however, was much larger than that specified by the analysis. This is the reason why the loop gain in the fricative filter was not divided evenly between the two integrators (i.e., the gain was needed in K_2 to provide the extra damping).

The additional damping necessary was found by measurement to increase at a rate proportional to the square of the resonant frequency. An explanation for this phenomenon has been given by Macnee.²⁹ If the solution to the differential equation

$$\frac{d^2y}{dt^2} + \omega^2 y = 0 \quad (4.22)$$

is computed using analog summers and integrators, the computed solutions will be

$$y = e^{\left[\omega^2 (1/\omega_h + 1/\omega_p) - \omega \right] t} (C_1' \cos \omega t + C_2' \sin \omega t) \quad (4.23)$$

rather than the correct solution which is

$$y = C_1 \cos \omega t + C_2 \sin \omega t \quad (4.24)$$

Observe that the computed solution has an exponential term whose exponent increases at a rate proportional to ω^2 . This exponential term can, of course, be removed by adding a damping term to the computation.

This analysis suggests the compensation scheme shown in Fig. 18. A

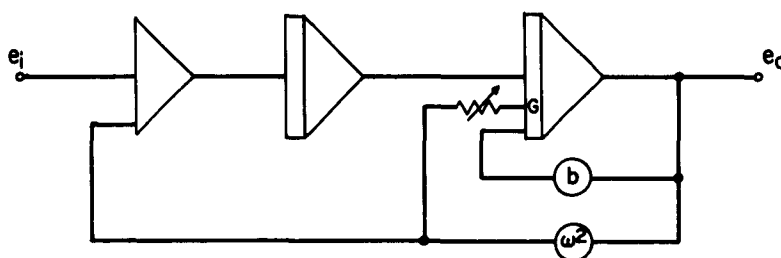


Fig. 18 Resonant Circuit with Compensation

preliminary test of this compensation in the third formant resonant circuit has shown that it works.

6. Conclusion and Recommendations

The experiments described above have shown that the analog portion of the proposed analog-digital speech synthesizer can be realized with standard analog computing elements. Also, an analysis has been made which shows the characteristics of the analog computation and some of the requirements on the computing elements. The analysis has also led to a method of compensation by which the only significantly bad characteristic of the analog realization of the resonant circuits can be eliminated through the use of extra damping.

The following references and ideas are given to aid further study in this area. The next factor to investigate is the digital control. Here information on the transitions between phonemes will be necessary and can be found in References 20, 30, 31, and 32. Because of the fairly large number of parameters that the digital computer must supply, it will probably be advantageous to add additional analog elements to the circuits shown in Figs. 6 and 7.

For example, if integrators are inserted following the storage gates, then linear transitions of the coefficients can be generated by rate information given by the digital computer. If integrators with feedback are inserted, then exponential transitions can be generated from gross changes in the coefficients given by the digital computer. Either of these additions will reduce the rate at which data must pass from the digital to the analog computer.

As a final point, it appears that an extension of the number of phonemes that can be generated with the above synthesizer is fairly easy. The first extension has already been mentioned, namely, by narrowing the bandwidth of the first formant in the nasals $|m|$, $|n|$, and $|\eta|$. The voiced stop consonants $|b|$, $|d|$, and $|g|$ respectively can be generated.²⁰ Reference 30 broadens this extension further by stating that, through an elimination of the first formant transition in the stop consonants $|b|$, $|d|$, and $|g|$, the unvoiced stop consonants $|p|$, $|t|$, and $|k|$ respectively can be generated. Finally Reference 33 says that by adding a strong component to the frequency spectrum in the region below 700 cps, the voiced fricatives $|z|$, $|\mathfrak{z}|$, $|v|$, and $|\mathfrak{v}|$ can be generated from the fricatives $|s|$, $|\mathfrak{s}|$, $|f|$, and $|\mathfrak{f}|$ respectively.

B. OTHER APPLICATIONS FOR DIGITALLY-CONTROLLED ANALOG FILTERS

It is felt, in view of the results obtained from the speech synthesis, that the project's ideas concerning the application of combined analog-digital computation techniques to other filtering problems may be of value. Consequently, these ideas are presented below.

1. Complex Problems Involving the Spectrum Analysis of Signals

Measurements of the performance of the resonant circuits of the speech synthesizer have shown that the resonant frequency can be adjusted over more than a decade of frequencies and that narrow bandwidths are possible. Q's of 100 were measured, but higher Q's were found possible. (Better data than this was not obtainable with the time and equipment available)

It is felt that digitally-controlled filters with the above performance might prove very useful when a digital computer is used to process signal spectral data. They would be particularly useful in research where the relationship between the signal spectrum and the desired result of the data processing must be found by experimentation.

An example of this type of research task is that of machine recognition of speech.³⁵ One way in which speech recognition is now done is as follows. The speech signal is fed through a bank of filters each of which is tuned to pass a particular band of frequencies. The strength of the signal passing through each of the filters is measured. On the basis of the values of these measurements, a decision is made as to what was said, and an output is generated, which might be a typewritten copy or synthesized speech in the same or a different language.³⁶

One aspect of the current research in this area is concerned with determining what spectral information is necessary for good recognition. The versatility of the digitally-controlled filter might be useful for finding this information. This is especially true in view of the fact that sometimes it is the way in which the spectrum changes during the transition between phonemes that is important to the identification of the phonemes.^{24, 37}

2. Analysis of Signals and Systems by Means of Orthogonal Functions

The analysis of signals by means of orthogonal functions is an old technique, e.g., Fourier Series for periodic signals. Recently, however, use has been made of orthogonal functions which have the property that they can be generated as the impulse responses of linear filters (referred to hereafter as orthogonal filters). This property provides a simple way in which certain functions, useful in signal analysis, can be computed. That is, the function will be the weighted sum of the impulse responses of the orthogonal filters. The weights are also easily calculated. The calculations are made from the response of the orthogonal filters to the input signals. Some of the functions for which the above is true are the exponential expansion of a signal³⁸ and of a correlation function of one or more signals.^{39, 40}

In another application Wiener⁴¹ has shown that a great number of systems, nonlinear as well as linear, can be simulated with a system containing orthogonal filters in which the only nonlinear elements required are multipliers. He has also shown that the parameters in a simulation system can be found by making measurements on the response of the system to be simulated to white noise. This provides a way in which models of complex systems such as biological systems can be formulated and studied.

Apparently, present exploitation of these uses of orthogonal filters is handicapped by the lack of a suitable realization. The orthogonal filters can be realized with analog computing elements. However, the problem is that a great deal of analog equipment is often necessary, as illustrated by the studies of Aron and Solbakken.⁴² It is felt that a few digitally-controlled filters, time-shared through the use of some method for storing continuous analog signals perhaps the one described in Chapter III, might provide a solution to the equipment complexity problem.

CHAPTER V

DISPLAYS

A. INTRODUCTION

The display system to be discussed here is a cathode-ray tube output display for a digital computer, and the type of display consists of line drawings, i.e., figures or graphs constructed from curved or straight lines. At present, the most common way in which cathode-ray tube (CRT) displays are generated by a digital computer is on a point-by-point basis. That is, the computer places the x and y coordinates of a point to be displayed into two registers. The numbers in these registers are decoded and the corresponding voltages applied to the deflection circuits of the CRT. When the transients in the deflection voltages have settled, the screen is intensified.

Making line drawings on this point-by-point basis consumes a large percentage of the available digital computer time and memory. Recent approaches made to reduce these requirements have been to add special-purpose, peripheral devices which construct the display with a minimum of direction from the digital computer. One example of such a special device is a character generator which is capable of generating a fixed set of patterns, usually the alphabet and the digits 0-9. Here, all the digital computer does is specify the symbol desired through a code number and the coordinates of the position the symbol is to occupy in the display. The character generator then automatically and independently generates the appropriate voltages for the deflection and intensification circuits.

Another example is a special-purpose digital computer that will generate figures made up of arbitrary straight lines and circles. This special computer also performs other useful computations such as those necessary to rotate the displayed figure or provide a stereoscopic display.⁴⁸ It was felt by the project that pulsed-analog techniques might be advantageous in the realization of such a special computer. The ideas generated by the project are discussed below. Unfortunately, due to the lack of the necessary pulsed-analog equipment, complete experimental testing of the ideas was not possible.

B. PULSED-ANALOG DISPLAY COMPUTER

1. Basic System

The basic pulsed-analog display circuit that has been devised is shown in Fig. 19. The operation of this circuit is as follows:

1. The system displays figures constructed from straight lines.
2. The coordinates of the initial point to be displayed are set into the integrators by the digital computer through gates x_o , y_o , and z_o .
3. Values of the length of a line in the x, y, and z directions are stored in gates ∇x_a , ∇y_a , and ∇z_a respectively. Also a value for the intensity of the display is placed in gate I_a .
4. The "a" gates are enabled for a fixed period of time. During this time the integrators will generate deflection voltages which will produce a straight line on the CRT. Also during this time the values of ∇x , ∇y , ∇z , and I for the next line (which will start where the preceding line ends) will be stored in gates ∇x_b , ∇y_b , and ∇z_b , and I_b .
5. At the conclusion of the fixed line-drawing period, the "a" gates are disabled and the "b" gates are enabled. The second line will then be generated and the data for the third line stored in the gates ∇x_a , ∇y_a , ∇z_a , and I_a .
6. This process of alternating between the a and b gates continues until the figure to be displayed is completed, at which time both the a and the b gates are disabled.

The intensity control serves three purposes.

1. To draw lines of different intensity within a figure.
2. To provide intensity compensation. This is required because all lines, regardless of their length, are displayed in a fixed period of time. Consequently, the intensity of each line, if uncompensated, will be inversely proportional to the length of the line.
3. To blank out undesirable lines. For example, the line generated to move the electron beam between two unconnected parts of a figure. Of course, this action can also be done by resetting the initial conditions of the integrators. Obviously the least time consuming of these methods should be used.

The capabilities of this display system and the specifications for the pulsed-analog elements will be found using the following assumptions.

1. The digital computer is a Digital Equipment Corporation PDP-1.
2. A decoder has been connected to the accumulator to make available, at all times, an analog representation of the contents of the accumulator.

3. An instruction operate gates (opg) has been added, which enables the gates specified by the address portion of the instruction. This instruction is completed in 10 μ sec.

The above features are those that have been proposed for the combined analog-digital flight simulator.² The last two assumptions are concerned with the operation of the gates.

4. The sample gates x_o , y_o , and z_o permit the setting of the initial conditions of the integrators. These gates differ from those previously described in that when they are disabled, their output must be floating, i.e., the gate just opens the circuit and does not provide the customary grounded output.
5. Some special digital circuitry is provided so that the remaining gates operate as follows. When a display is being generated either gate set "a" or gate set "b", never both, is enabled. Under this condition the instructions produce the following actions:
 - a. If gate set "a" is enabled the instruction opg a-b will disable set "a" and enable set "b". If gate set "b" is enabled the instruction opg a-b disables set "b" and enables set "a".
 - b. When gate set "a" is enabled the instructions opg ∇x , opg ∇y , opg ∇z , and opg I will enable gates ∇x_b , ∇y_b , ∇z_b , and I_b respectively for 10 μ sec. When gate set "b" is enabled these instructions will enable gates ∇x_a , ∇y_a , ∇z_a , and I_a respectively for 10 μ sec.
 - c. A display is terminated by the instruction opg $\overline{a-b}$ which does the following. First, it causes an action identical to that caused by the instruction opg a-b. Second, after a delay, during which the last line specified to the display computer is generated, both gate sets "a" and "b" are disabled.

When a display is not being generated the digital circuitry remembers whether gate set "a" or gate set "b" was the last to be enabled. Under this condition the instruction produces the following actions:

- d. If set "a" was the last enabled the instructions opg ∇x , opg ∇y , opg ∇z , and opg I enable gates ∇x_b , ∇y_b , ∇z_b , and I_b respectively for 10 μ sec. If set "b" was the last enabled these instructions enable gates ∇x_a , ∇y_a , ∇z_a , and I_a respectively for 10 μ sec.
- e. A display is initiated by the instruction opg a-b. If set "a" was the last enabled in the previous display, set "b" will be enabled first on the initiation of the next display and vice versa.

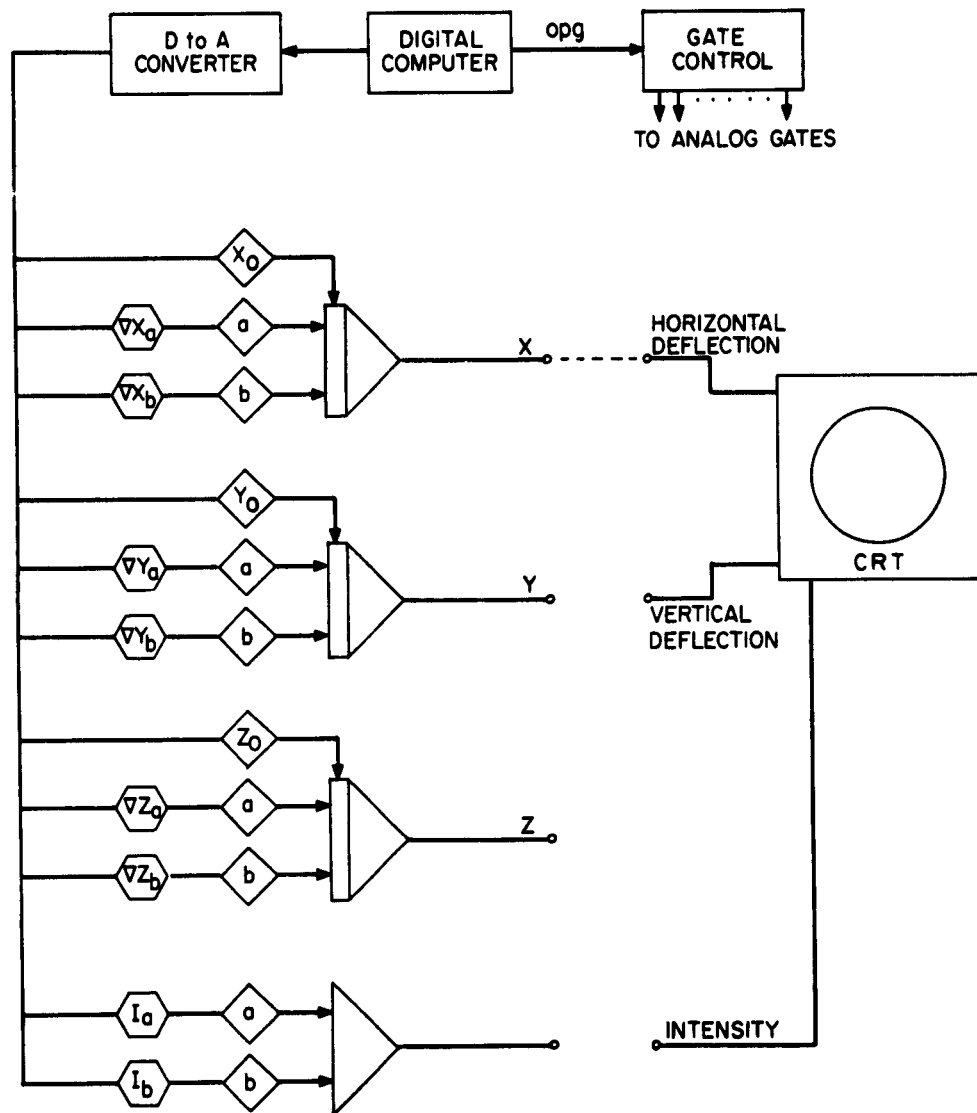


Fig. 19 Basic Pulsed-Analog Display Circuit

With these assumptions, the sample display program given in Fig. 20 has been written using the PDP-1 mnemonic code.⁴⁹ Parentheses indicate the address of the quantity enclosed. The portion of the program from int to cont initiates a display. The portion of the program from cont to ext-1 continues the display until the data for the last line has been stored in the analog gates. The portion of the program from ext to ext + 8 resets the program for the next frame, and initiates the display of the last line and the disabling of the display circuit. The data is stored as shown following the program.

This program displays the figure just once (one frame). To produce a flicker free display, it must be repeated approximately sixty times a second. (This estimate for the necessary frame speed was obtained from observations made on oscilloscope traces. Conceivably the screen persistence could affect the estimate considerably.) This can be accomplished by providing a clock so that the main program can be interrupted, using the sequence break feature of the PDP-1, at the proper intervals to generate the display. What is important at present, however, is to determine the maximum number of lines that can be drawn in 1/60th of a second. Consequently the last instruction has been added to start the new frame immediately.

Totaling the program execution times, it takes 145 μ sec. to put the line data in the storage gates and do the necessary indexing. Consequently, the time spent drawing a line cannot be less than this. Of course, it is desirable to obtain the display in the shortest time, consequently the time allowed to draw a line will be fixed at 145 μ sec. Following the initiation of the display of the last line (opg a-b) 150 μ sec. pass before the initial conditions are reset. This allows the last line to be completed, and leaves only 60 μ sec. of the initiation portion of the program to be completed before the display of the next frame begins. Therefore, within a sixtieth of a second, the number of lines that can be drawn is

$$\frac{1/60 - 60 \times 10^{-6}}{145 \times 10^{-6}} \approx 114 = n_{\max}$$

<u>Address</u>	<u>Instruction</u>	<u>Execution Time (μsec.)</u>
int	lac (∇x_1)	10
	opg ∇x	10
	lac (∇y_1)	10
	opg ∇y	10
	lac (∇z_1)	10
	opg ∇z	10
	lac (I)	10
	opg I	10
	lac (x_0)	10
	opg x	10
	lac (y_0)	10
	opg y	10
	lac (z_0)	10
	opg z	10
cont	opg a-b	10
	lac (∇x_2)	10
	opg ∇x	10
	lac (∇y_2)	10
	opg ∇y	10
	lac (∇z_2)	10
	opg ∇z	10
	lac (I_2)	10
	opg I	10
	idx cont + 1	10
	sad (lac (∇x_{n+1}))	10
	jmp ext	5
	idx cont + 3	10
	idx cont + 5	10
	idx cont + 7	10
ext	jmp cont	5
	lac (lac (∇x_2))	10
	dac cont + 1	10
	add (n+1)	10

Fig. 20 Display Program

<u>Address</u>	<u>Instruction</u>	<u>Execution Time (μsec.)</u>
	opg a - b	10
	dac cont + 3	10
	add (n - 1)	10
	dac cont + 5	10
	add (n - 1)	10
	dac cont + 7	10
	jmp int	5
(x ₀)		
(y ₀)		
(z ₀)		
(∇x ₁)		
.		
.		
.		
(∇x _n)		
(∇y ₁)		
.		
.		
.		
(∇y _n)		
(∇z ₁)		
.		
.		
.		
(∇z _n)		
(I ₁)		
.		
.		
.		
(I _n)		

Fig. 20 Display Program (Continued)

How adequate this number of lines is for line drawings only experience can tell. However, since 1024 horizontal lines will fill the display area of the PDP-1 scope, this display generator can cover 11 percent of the available area.

2. Analog Element Specifications

a. Integrators The specifications on the integrators are derived as follows. It will be assumed that the allowable input and output voltage ranges of the integrators are the same, and are $\pm E$. In order to draw a line of maximum length, a step of E volts applied to the integrator must cause the output to rise $2E$ volts (i.e., from $-E$ to $+E$) in $145 \mu\text{sec}$. This requires that the integrator have a gain of

$$K = \frac{2E}{E \cdot 145 \times 10^{-6}} \approx 13,793$$

The integrator must also integrate levels that change 6896 times a second. A test with the following:

operational amplifier - Philbrick K2-x
 $R_i = 100 \text{ k}$
 $C_f = 470 \text{ pf}$ } Integrator gain $\approx 21,000$
input - 4 kc square wave (levels change 8 kc)

produced a triangular wave output with clear sharp peaks and straight sides. Drift in the integrators should not be a problem, for the initial conditions will be reset sixty times per second. The above indicates that the integrator specifications can be met with currently available elements.

b. Storage Gates The storage gates must be able to settle to the value to be stored within $10 \mu\text{sec}$., and hold the value for $265 \mu\text{sec}$. Some measurements made on a prototype Adage storage gate have shown that it has a store time of $10 \mu\text{sec}$. and a hold time of 60 msec . which is adequate for the display computer.

c. Sample Gates Due to the high gain of the integrators, the transient response of the sample gates is important. To see this, consider Fig. 21.

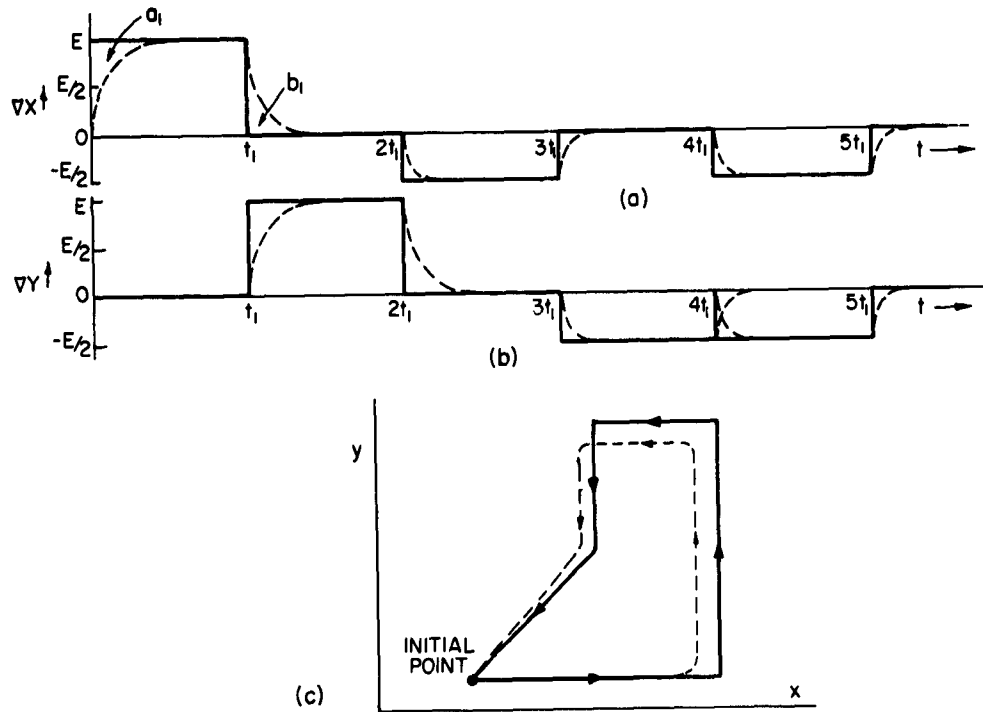


Fig. 21 The Effects of the Sample Gate Response

Parts a and b show a set of ∇x and ∇y inputs and part c shows the figure generated. The solid lines show the desired quantities and the dashed lines the quantities that can be expected in practice. In the ∇x and ∇y signals, it is the difference in the integrals between the desired and actual signals that is important. Observe that the value of the integral lost in the enabling (a_1) is at least partially cancelled by the value of the integral gained in the disabling (b_1). However, this correction comes after the next line is started and will cause a rounding of the corner. Also, if $b_1 \neq a_1$ then there will be an error in the final value of x for the input ∇x_1 . This is shown in Fig. 21-C where it has been assumed that the disable time is less than the enable time. To get an estimate of the required response of the sample gate, a pessimistic case will be assumed, namely that an enable transient occurs and no disable

transient occurs. The greatest error will be generated when the input, e.g., ∇x , is largest. Assuming the transient is a simple exponential, the error will be

$$\epsilon_{\max} = KE_{\max} \int_0^{t_1} -e^{-at} dt = KE_{\max} \left[\frac{e^{-at_1}}{a} - \frac{1}{a} \right] \approx - \frac{KE_{\max}}{a}$$

To obtain 0.1 percent error, the sample gate must have a time constant of

$$\frac{1}{a} = \frac{10^{-3}}{K} \approx .07 \mu\text{sec.}$$

One way the response of sample gates have been specified is the time it takes for the output to settle to within 0.1 percent of the input. For an exponential transient, this is about seven time constants. For this case then, a settling time of about 0.5 $\mu\text{sec.}$ is required. A comparison of this figure with the 2 $\mu\text{sec.}$ settling time for the gates developed by Solbakken,⁵⁰ indicates that an improvement of a factor of four would be desirable.

A final point concerning the Solbakken sample gates should be discussed. There is a small transient which occurs during the enabling and disabling process, and is due to the charge stored in the transistors. A rough estimate of the integral under these transients, obtained from Reference 50, is 12.5 mv $\mu\text{sec.}$ each, and they are both positive. A maximum of 114 of each of these transients can occur, and each will be multiplied by the gain of the integrator. This will produce the following error:

$$2 \times 12.5 \times 10^{-9} \times 114 \times 13,793 = .0393 \text{ volts}$$

Compared with the maximum voltage (the gate is designed for 10 volts) this is a 0.4 percent error. This result indicates another aspect of the sample gate performance which it would be desirable to improve.

C. OTHER COMPUTATIONS

Besides the computations necessary to the generation of the displayed figure, there are other computations that are useful in generating displays. These can be time consuming for the digital computer, but can be done quite easily with analog elements independent of the digital computer. Three of these computations are discussed briefly in this section.

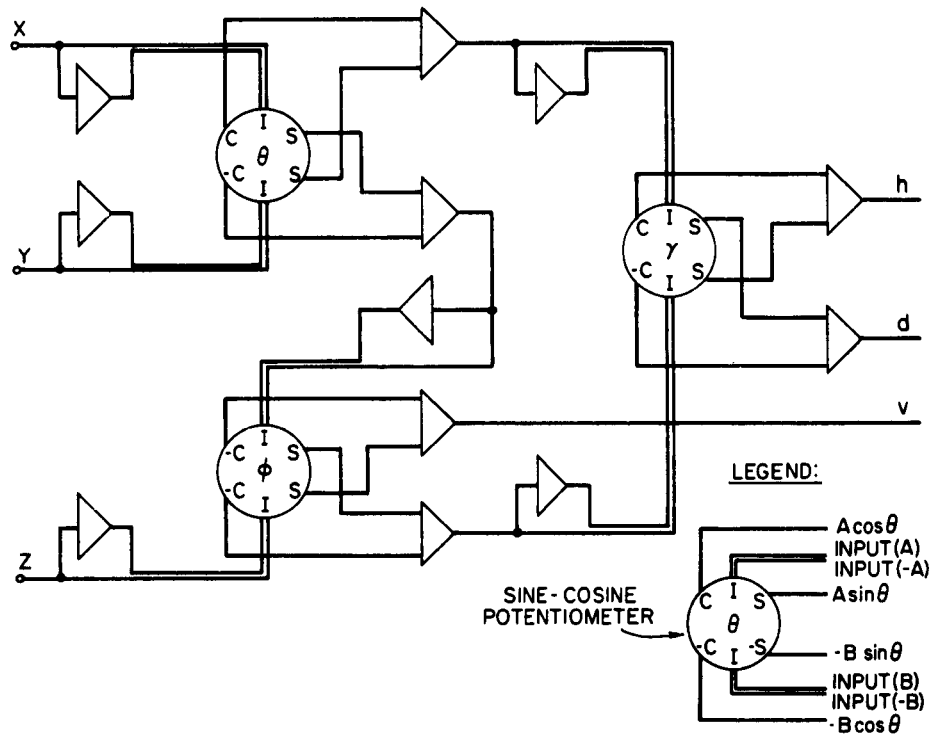


Fig. 22 Rotation Circuit

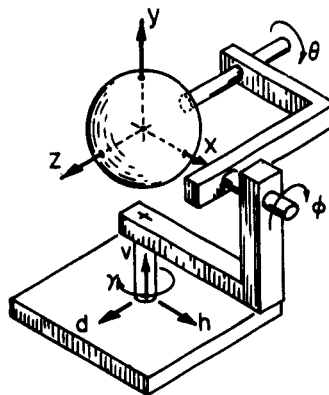


Fig. 23 Coordinate System and Rotation Angles

1. Rotation of Displayed Figure

A useful feature for a display is the ability to rotate the displayed figure, so that it can be viewed from different angles. Rotation would be primarily for the convenience of the viewer, and consequently, it would be advantageous for the necessary computations to be done independent of the digital computer. These computations can be performed with the analog circuit shown in Fig. 22. A pictorial interpretation of the rotation generated by this circuit is shown in Fig. 23. The coordinates x , y , and z are those of the figure to be displayed as it is described by the contents of the digital computer memory. The coordinates h , v , and d are those of the display, the definitions for which are illustrated in Fig. 23. Their origin is the same as that of the x , y , and z coordinates. In Fig. 23 the orientation of the x , y , and z coordinates is for the case where $\theta = \phi = \gamma = 0$.

The mechanical device shown in Fig. 23 would also facilitate the manipulation of the sine-cosine potentiometers to obtain a desired rotation. That is, if the potentiometers were mounted at the appropriate bearings, the operator of the display could grasp the sphere, as though it were the figure being displayed, and turn it to the position desired.

2. Perspective Projection and Stereoscopic Display

Other useful features for a display are aids for visualizing the depth of three dimensional figures, such as the perspective projection and the stereoscopic display. The computations necessary for these displays are closely related and are derived below. Following the derivation, some observations are made which permit a simplification of the computations. The simplification has been used before. However, the observations discussed here which show the validity of the simplifications have not been presented previously to the author's knowledge.

The geometry related to these displays is shown in Fig. 24. The display is presented on the h - v -plane. The viewer's eyes are a distance s from the h - v -plane and perpendicular to it. The origin of the coordinate system for the object to be displayed is assumed to lie on the h - v -plane.

Part a of Fig. 24 shows the geometrical relationship between the v coordinate value (v_o) of a point on the object, and the v coordinate value (v_i)

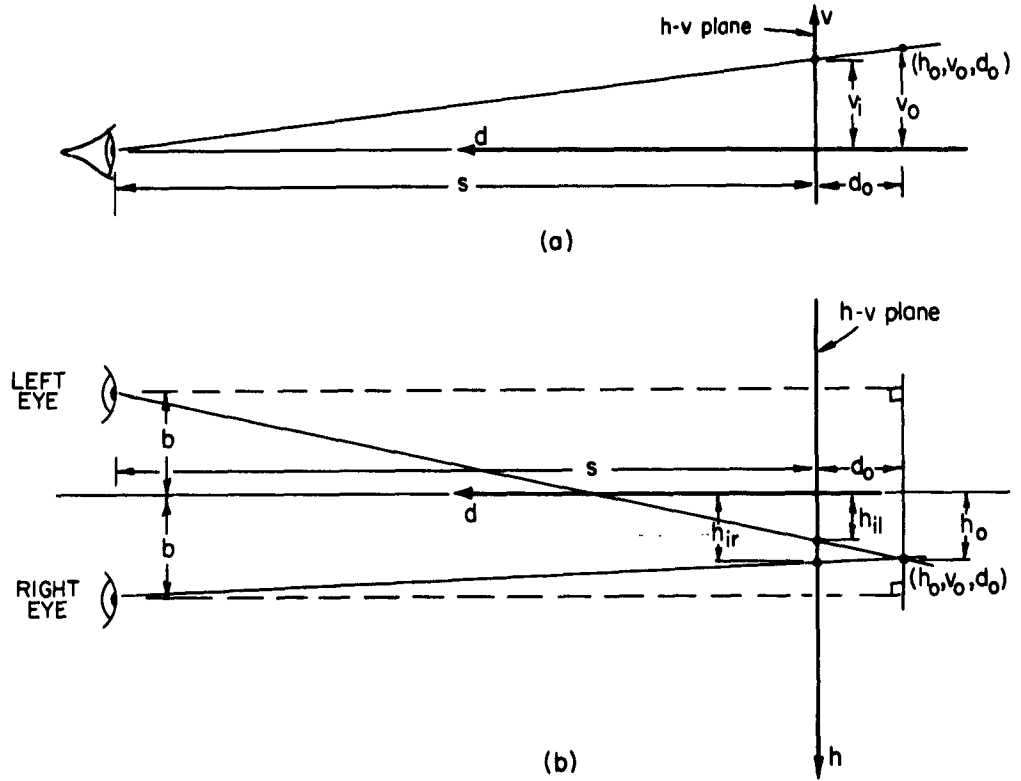


Fig. 24 The Geometry of Perspective Projection and Stereoscopic Displays

of the corresponding point in the displayed image. From the symmetry of the triangles the following can be obtained:

$$v_i = \frac{v_o}{1 - \frac{d_o}{s}} \quad (5.1)$$

This equation is true for both perspective projection and stereoscopic display. A similar equation is true for the image h coordinate value in a perspective projection, e.g.,

$$h_i = \frac{h_o}{1 - \frac{d_o}{s}} \quad (5.2)$$

Part b of Fig. 24 shows the geometrical relationship between the h coordinate value (h_o) of a point on the object and the h coordinate values (h_{il} and h_{ir}) of the corresponding points in the images for the left and right eyes of a stereoscopic display. From the symmetry of the triangles, the following can be obtained:

$$h_{ir} = \frac{h_o - \frac{bd_o}{s}}{1 - \frac{d_o}{s}} \quad (5.3)$$

$$h_{il} = \frac{h_o + \frac{bd_o}{s}}{1 - \frac{d_o}{s}} \quad (5.4)$$

Observe that Eqs. 5.3 and 5.4 are the same as the perspective projection equation (Eq. 5.2) except for an additional term that takes into account the separation of the eyes.

A computational difficulty with all four of the above equations is the division by $(1 - \frac{d_o}{s})$, which presents problems in either digital or analog computation. One way around this problem, that has been used, is to assume that

$$\left| \frac{d_o}{s} \right| \ll 1 \quad (5.5)$$

and approximate the division by a few terms of the binomial series

$$\frac{1}{1 - \frac{d_o}{s}} = 1 + \frac{d_o}{s} + \left(\frac{d_o}{s}\right)^2 + \left(\frac{d_o}{s}\right)^3 + \dots \quad (5.6)$$

Relation 5.5 may appear to be a severe assumption to make for some display problems. However, the following observations show that it is somewhat a necessity.

First, for a display, the quantities b and s are constants. The distance between the eyes does not vary greatly from person to person, so variations

in b should not be too important. The value of s , however, is quite likely to change unless there is some eyepiece arrangement that forces the viewer to observe from the proper distance. Consequently, to be commensurate with the computational accuracy, the distortion of the viewed figure caused by slight misalignments in the position of the viewers head must be small. As can be seen from Eqs. 5.1 through 5.4 the effect of changes in s will be small if Relation 5.5 is true.

Second, in normal vision the eyes focus at the point where their two lines of sight cross. In a stereoscopic display the eyes must focus at the plane of the display, which is unnatural. This is probably the primary reason some people have difficulty in viewing stereoscopic displays. To limit this difficulty, the distance to the display must be approximately equal to the apparent distance to the point being viewed. This, of course, will be the case if Relation 5.5 is true.

For variations in s of the order of

$$\frac{\nabla s}{s} = \frac{d_o}{s}$$

there is little value in retaining d_o/s terms of order two or greater in the computations. With this approximation Eqs. 5.1 through Eq. 5.4 become

$$v_i \approx v_o + \frac{v_o d_o}{s} \quad (5.7)$$

$$h_i \approx h_o + \frac{h_o v_o}{s} \quad (5.8)$$

$$h_{ir} \approx h_o + \frac{h_o d_o}{s} + \frac{b d_o}{s} \quad (5.9)$$

$$h_{il} \approx h_o + \frac{h_o d_o}{s} - \frac{b d_o}{s} \quad (5.10)$$

An analog circuit for generating these functions is shown in Fig. 25. By setting potentiometer b to zero, the circuit will generate a perspective projection.

To view the stereoscopic display a method for presenting each eye with the proper image is required. A simple optical device for this purpose is shown in Fig. 26. To see the stereoscopic image, glasses with polarized lenses must be worn. Observe that, because of the mirror, the display

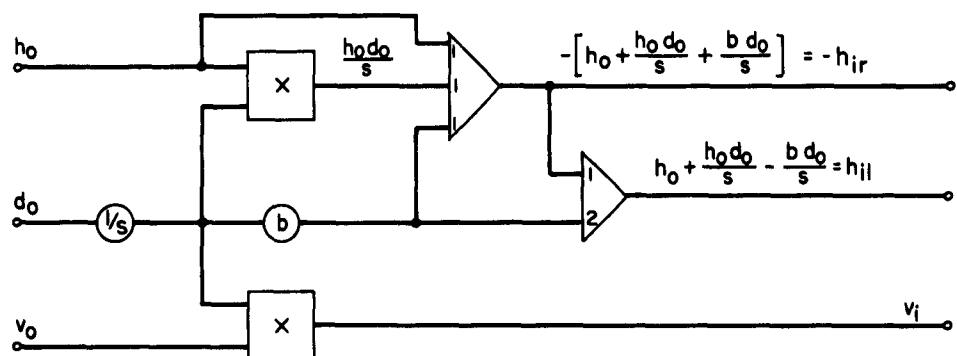


Fig. 25 Analog Circuit for Generating a Stereoscopic Display

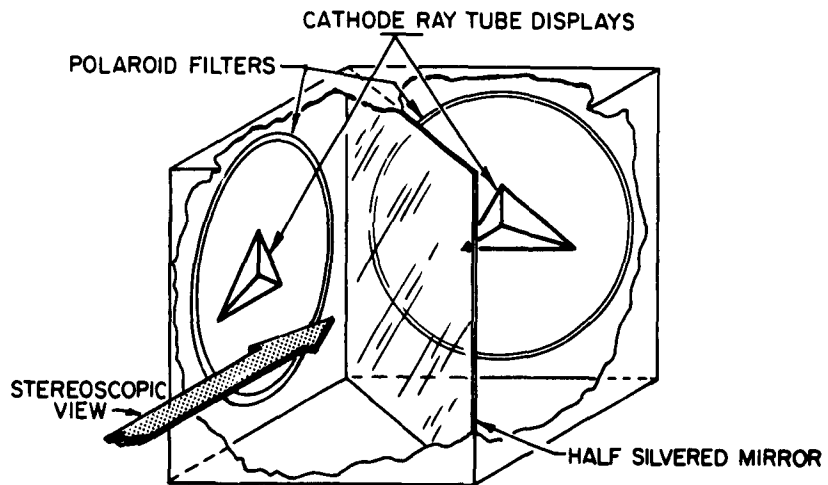


Fig. 26 Optical Device for Presenting Stereoscopic Image

entering from the side of the optical device must be the mirror image of the figure to be seen. The mirror image is generated by using $-h$ instead of h . In Fig. 25 $-h_{ir}$ is computed so the display for the right eye is the one to be presented through the side of the optical device.

A device like that shown in Fig. 26 was constructed by the project and tested on some displays generated by Stotz during his investigations.⁴⁸ The stereoscopic image was easily seen by all who looked. A simpler, but more awkward, method for viewing a stereoscopic image was also found and is shown in Fig. 27. Here the reflected image appears to the left eye to be in the same position as the image for the right eye. This eliminates the problem usually encountered in stereoscopic printed material,^{52, 53} of attempting to focus the eyes on individual images which are separated.

3. Intensity Compensation

The need for intensity compensation was discussed previously. Recall that all lines, regardless of length are generated in the same length of time. Consequently, the intensity of a line will be inversely proportional to its length if the intensity is not compensated. This compensation can be computed by the digital computer for the figure as it is stored in the digital memory. However, computations on the display data by the analog elements such as in the rotation of the displayed figure will cause changes in the lengths of the lines displayed. Consequently, the compensation cannot be supplied by the digital computer in these cases. The compensation that is required, is to make the intensity of the electron beam proportional to the length of the line displayed. That is

$$I = K \sqrt{(\nabla v)^2 + (\nabla h)^2} \quad (5.11)$$

where ∇v and ∇h are the vertical and horizontal components of the line displayed. An analog circuit for performing the intensity compensation is shown in Fig. 27. The squaring circuits and the square root circuit can be realized with diode function generators. The quantities ∇v and ∇h can be computed by feeding ∇x , ∇y , and ∇z into the rotation circuit of Fig. 22 which will produce ∇v , ∇h , and ∇d . In other words the integrations can be done after the rotation computation. If a stereoscopic display is desired, that circuit can be inserted between the rotation circuit and the line-generating integrators.

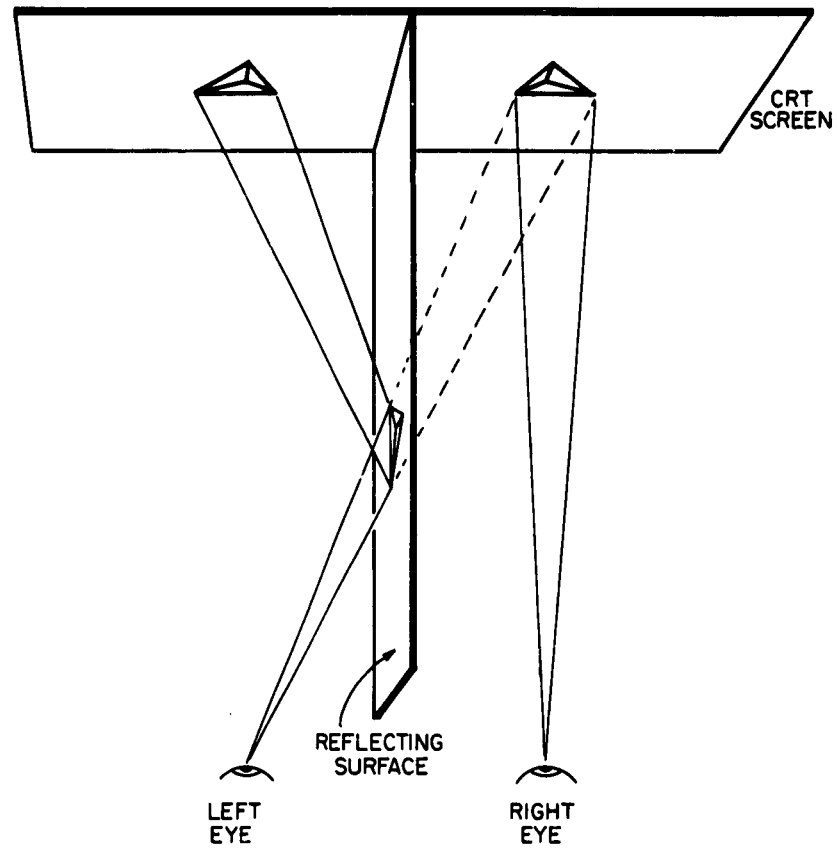


Fig. 27 Simple Method for Presenting Stereoscopic Image

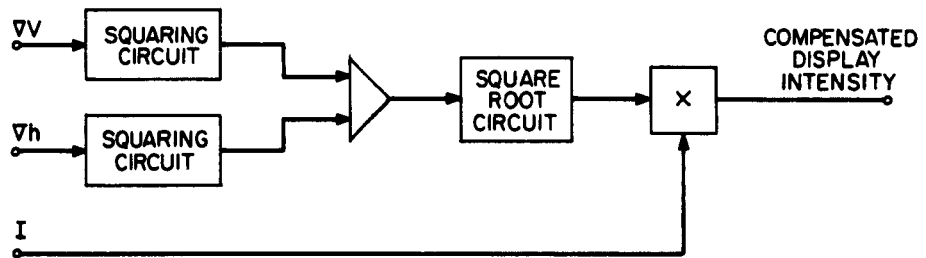


Fig. 28 Analog Circuit for Intensity Compensation

The only difficulty with computing the ∇ quantities is that the initial values for the integrators cannot be supplied directly by the digital computer. Probably the best solution to this problem is to always start at the origin and use one undisplayed line to get to the initial point of the displayed figure.

D. SUMMARY AND RECOMMENDATIONS

In this chapter, the design of a pulsed-analog display computer has been presented. The design was formulated around a proposed analog-digital computer to be constructed at the Electronics Systems Laboratory. This was done so that the design might be tested with a minimum of effort when that computer is completed.

Investigations into the required performance of the pulsed-analog elements have shown that, except for the sample gates, currently-available elements are satisfactory.

It was also shown how two useful display computations can be done with analog elements independent of the digital computer. Specifically these computations were those necessary to rotate the displayed figure and to generate perspective projections and stereoscopic displays.

Areas that need to be investigated are given below:

1. The response of the sample gate appears to be the factor that limits the performance of the system at present. So this is the first short coming to remedy in the pulsed-analog portion.
2. The response of the deflection circuits in the computer CRT displays to continuously varying analog signals may be a limiting factor in the speed of display.
3. One poor feature of the design presented is that only 114 lines can be drawn, and this can be done only at the expense of full time use of the digital computer on the display generation. A better approach can probably be made through use of the high speed data channel of the PDP-1 and some special digital circuitry to automatically operate the analog gates as the data is supplied by the data channel. Through these the display could be generated independent of the digital computer except for the memory cycles taken by the high speed data channel in extracting the display data.

4. Another useful display computation is that of expanding and shrinking the size of the figure over great ranges.⁵¹ This allows one to view the over-all figure, or to investigate small parts of it as though looking through a microscope. Extremely wide ranges of signal magnitudes cannot be handled solely with analog elements. However, the digital computer can be used to scale numerical values to proper signal levels. The best way to combine the analog and digital operations to perform this computation should be investigated.
5. Analog circuits for the generation of curved lines particularly conic sections should be investigated.
6. Finally the problem of how to feed information back to the digital computer via a light pen from an analog generated display should be investigated.

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