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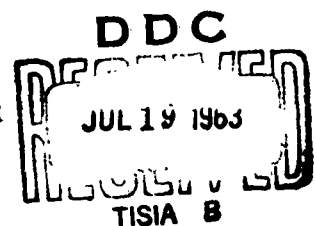
DEMONSTRATION OF THE FEASIBILITY OF USING
DELTA MODULATION FOR PICTORIAL TRANSMISSION

TECHNICAL DOCUMENTARY REPORT ASD-TDR-63-528

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AF Avionics Laboratory
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(Prepared under Contract No. AF 33(657)-8478
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FOREWORD

This report was prepared by the Philco Corporation Advanced Technology Laboratory, Blue Bell, Pennsylvania, on Air Force Contract No. AF 33(657)-8478, Task No. 433521 of Project No. 4335, "Demonstration of the Feasibility of Delta Modulation for Pictorial Transmission." The work was administered under the direction of Electronic Warfare Division of the AF Avionics Laboratory, Aeronautical Systems Division. Mr. Robert Remm was project engineer for the Laboratory.

The studies presented began 15 April 1962, were concluded 15 May 1963, and represent an effort of the Pictorial Data Processing Group of the Philco Corporation Advanced Technology Laboratory. Mr. Robert V. Cotton was the engineer responsible for research activity of the Philco Corporation.

Although the studies were a group effort, the chief contributors were: Richard A. Schaphorst, George R. Strohmeyer, Albert F. Tillman, Robert D. Vernot, Richard W. Yutz, and Ronald D. Lewars.

This report covers the work on Phases I and II of Contract No. AF 33(657)-8478. The contractor's report number is V040-F.

ABSTRACT

An extensive investigation of Delta Modulation techniques for encoding pictorial data was made to determine the parameters of Delta Modulation systems for various image communication applications by (1) system analysis, (2) computer simulation, and (3) experimentation. The analysis and computer simulation included one-bit and two-bit systems with linear integration, double linear integration with prediction, and exponential integration. Fifteen different Delta Modulation encoding logics were simulated during the program. Most importantly, the performance of these logics, as well as that of PCM, in the presence of data-link noise has been simulated and evaluated. Images of all these simulations are presented for evaluation. A feasibility model of a 25-Mc two-bit exponential integration Delta Modulation encoding and decoding system with a serial bit rate of 100 Mpps was designed, constructed, and tested.

A table of the key parameters of PCM and Delta Modulation encoding systems, based upon the analysis, simulation, and implementation, is presented. Using this table and the images, the image communication system designer can choose the best technique and combination of parameters to fulfill his particular application.

It is concluded that for a typical image communication system, two-bit Delta Modulation with exponential integration and sampling at two to three times the information bandwidth represents the best compromise of parameters. The resultant compaction over six-bit PCM is two to three.

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I. INTRODUCTION

This technical report describes the effort conducted by the Philco Corporation under a program entitled "Demonstration of the Feasibility of Using Delta Modulation for Pictorial Transmission," U.S. Air Force Contract No. AF 33(657)-8478. Phase I, which comprised the first six months of effort, was concerned with the analysis and computer simulation of candidate Delta Modulation logics for encoding pictorial data and with studies of high-speed circuits suitable for implementing a 25-Mc Delta Modulation system. The results of the Phase I efforts were described in detail in a Technical Note,¹ published in November 1962.

The main tasks of both phases of the contract are listed below.

Phase I

- (1) Survey and theoretically analyze Delta Modulation and PCM systems.
- (2) Simulate PCM and various Delta Modulation logics by means of a computer.
- (3) Design, analyze, and experimentally test high-speed circuits for possible implementation in the 25-Mc feasibility model.

Phase II

- (4) Continue the study by analysis and computer simulation of Delta Modulation logics.
- (5) Design, construct, and test a two-bit Delta Modulation system operating at a sampling rate of 50 Mc with a serial bit rate of 100 Mpps.

This final report does not repeat all the details contained in the Technical Note. For example, the theoretical analysis and experimental tasks in Phase I have been largely deleted from this final report. Only the highlights of these tasks and the computer simulation work closely related to the Phase II program are included.

The work on these tasks is described in Sections III and IV, respectively.

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Section II describes the broad spectrum of Delta Modulation techniques applicable to this program and presents the mathematical equations representing their operation.

Section V presents the conclusions developed during both phases of the program. It was concluded at the termination of Phase I that two-bit Delta Modulation with a single, exponential integrator is the best compromise between the many parameters of candidate coding logics -- bit rate, noise performance, fidelity, size, weight, and power. This conclusion is further borne out by the fact that images produced by linear, double integration with prediction during the computer simulation of Phase II are inferior in quality to those employing single integration at relatively low ratios (2 to 4) of sampling rate/highest analog frequency.

Section VI outlines several areas of consideration for future investigations of Delta Modulation techniques as applied to image encoding. Included are two new Delta Modulation logics which appear to warrant further consideration.

II. GENERAL DESCRIPTION OF DELTA MODULATION SYSTEMS

A. Description of Techniques

1. One-Bit Delta Modulation²

The one-bit Delta Modulation system represents the simplest form of a digital communications system which will yield usable results. Figure 1 shows the encoding process of an arbitrary analog waveform of such a system. The analog signal is introduced to a subtraction network where the feedback signal, assumed zero for the first comparison, is subtracted from it. The resulting error signal, the difference between the analog signal, e_s , and the feedback signal, e_f , is then compared with the reference level of the comparator, in this case zero. The comparator provides an output pulse upon a clock pulse command. The output pulse, e_d in Figure 1, is positive if the error signal is positive and negative if the error signal is negative. These pulses comprise the digital output of the system to be transmitted to the decoder and are also integrated in the feedback loop of the Delta Modulation encoder to form the feedback signal, e_f , as shown in Figure 1.

The Delta Modulation encoder is a slope-limited system rather than an amplitude-limited system. The maximum slope that can be attained is dependent on the pulse height, h , and the clock or sample pulse period, τ . This relation is expressed as

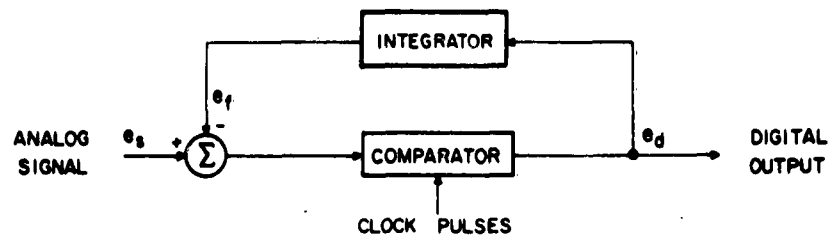
$$\text{Maximum slope} = h/\tau.$$

Therefore, the response time of the encoder to a step function depends on the amplitude of the step function. Obviously, if the step function amplitude were equal to the pulse height, h , the encoder would respond exactly. The upper frequency limit of the encoder is then specified by the maximum permissible amplitude of the analog as well as the clock-pulse frequency and the pulse height.

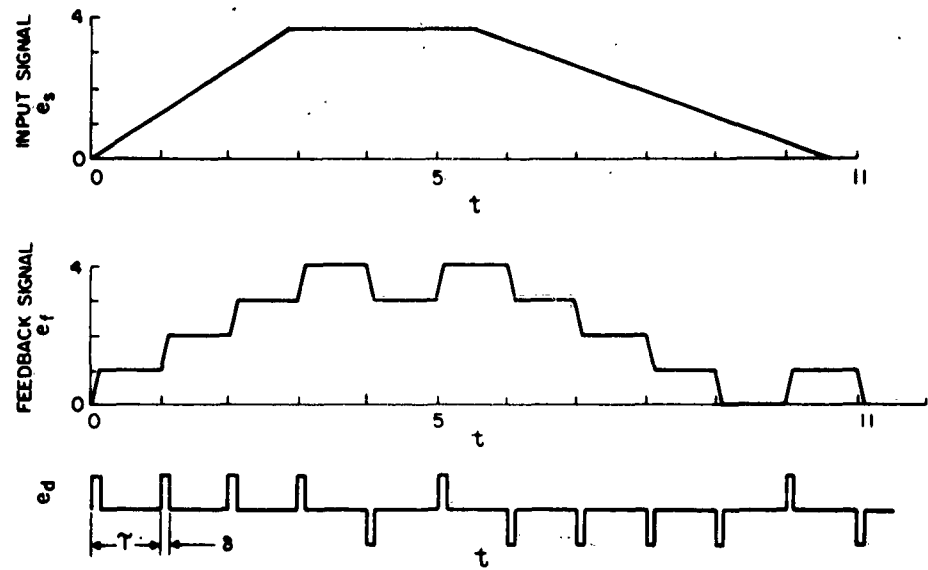
The decoder contains an integrator similar to that in the encoder and an output filter.

2. Multibit Delta Modulation³

The multibit Delta Modulation encoder is similar in operation to the one-bit, except that the error signal is now quantized into 2^N levels where N equals the precision of quantization or encoding. This increased precision describes the error signal more accurately on an amplitude basis and therefore



a. BLOCK DIAGRAM



b. WAVEFORMS

Figure 1 One-Bit Delta Modulation System

provides a better correction to the reconstructed signal in the feedback loop. Judicious methods for specifying the relationship between quantization intervals and step sizes, or increments added to the output of the integrator due to integration of input pulses, are described in Section II-B-2-c.

The construction of the quantizer of a multibit Delta Modulation encoder may take several forms. A general block diagram is shown in Figure 2a. The single comparator of the one-bit case is replaced with a quantizer providing a parallel output code of n digits, which are added algebraically to uniquely define each quantization interval of the error signal. Each of the n digits obeys the same rule as in the one-bit case; a positive pulse is generated if the error signal is greater than the reference level and a negative pulse if the signal is less than the reference level. The number of comparisons required for a parallel quantizer is

$$n = 2^N - 1,$$

where N equals the precision of encoding in binary bits and n is the number of digits or pulses which must be added algebraically to define the quantization of the error signal.

An example of the encoding process for a two-bit Delta Modulation system is shown in the waveforms of Figure 2b. By combining the pulse outputs of the three comparators in the parallel quantizer, 2^N or four step heights are obtained; assuming a unit pulse height for each comparator, e_0 , e_1 , e_2 , the steps are +3, +1, -1, -3. The reference levels for the three comparisons are +1.5 for e_2 , 0 for e_1 , and -1.5 for e_0 . Assuming the feedback (integrator) signal to be zero at the first sample pulse and the input signal, e_s slightly positive, the first comparison yields a positive pulse at e_0 , a positive pulse at e_1 , and a negative pulse at e_2 , as shown in Figure 2b. The resultant summation is a pulse of +1 amplitude which is integrated to form the feedback signal. At the beginning of the next sample period, the error signal, $e_s - e_f$, is equal to +1; therefore, the same set of pulses are produced by the quantizer, summed, and integrated. At sample time 2, the error signal is equal to +2.3; therefore, all quantizer outputs are positive. This provides a pulse of amplitude +3 to be integrated. The effect of this large step of amplitude +3 is observed in the integrated waveform or feedback signal, e_f .

The maximum slope of the multibit Delta Modulation encoder is given by

$$\text{Maximum slope} = \frac{(2^N - 1)h}{T},$$

provides a better correction to the reconstructed signal in the feedback loop. Judicious methods for specifying the relationship between quantization intervals and step sizes, or increments added to the output of the integrator due to integration of input pulses, are described in Section II-B-2-c.

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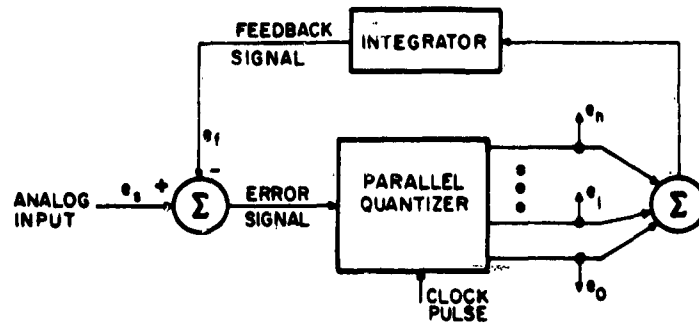
$$n = 2^N - 1,$$

where N equals the precision of encoding in binary bits and n is the number of digits or pulses which must be added algebraically to define the quantization of the error signal.

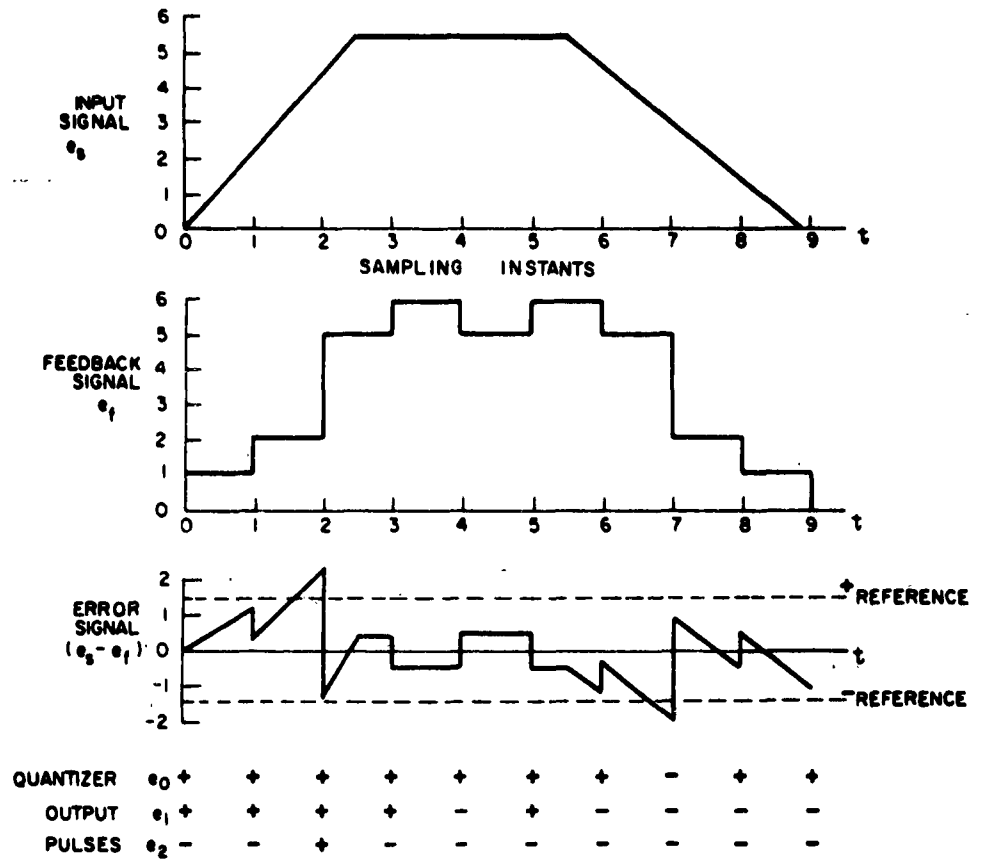
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The maximum slope of the multibit Delta Modulation encoder is given by

$$\text{Maximum slope} = \frac{(2^N - 1)h}{T}$$



a. BLOCK DIAGRAM



b. WAVEFORMS

Figure 2 Multibit Delta Modulation System

where h = pulse height. Therefore, for a two-bit system with a step height and sampling period similar to a one-bit system, the maximum slope is three times as great. If the maximum signal amplitude were equal for both systems, the response of the two-bit system to a maximum amplitude input step function would be three times faster than the time required for the one-bit system for identical sampling rates.

The output pulses from the quantizer are generated in parallel form; three transmission channels would be required to transmit this code. If it is desired to transmit the code in a single channel, the quantizer output code must be either serialized in its present form or converted to a more efficient code such as conventional binary, requiring only N digits rather than $2^N - 1$ digits as in its present form. Thus, the output serial bit rate of the system is Nf_s , where f_s is the frequency of the sampling pulses.

3. Linear and Exponential Integrators

a. Single Linear Integration²

A simple type of Delta Modulation system is obtained by using a linear integrator in the feedback loop. The response of the integrator to an impulse or narrow pulse approximates a step function, provided the integrator has a long time constant. The response of such a circuit to a series of positive and negative narrow pulses is a signal built up from positive and negative steps to form a step curve oscillating around the input signal to the Delta Modulator. Figure 1b shows the output of a linear integrator, e_f , in response to a train of narrow pulses, e_d . Linear integrators used in Delta Modulation systems have several important characteristics.

(1) Contouring

The output of the integrator is quantized into fixed levels because the contribution from each succeeding input pulse is always a fixed increment. Therefore, the number of reproducible levels is limited and constant for any particular step size or increment. As a consequence, such Delta Modulation systems suffer from a threshold effect. Signals which approach dc are represented by an oscillation composed of an alternating sequence of steps. The amplitude of oscillation is equal to the increment produced by a single input pulse to the integrator.

(2) Transient Response

Another characteristic is concerned with the transient response of the system. The maximum rise time response available from a

linear integrator is directly dependent upon the number of steps required to traverse the entire dynamic range of the input signal. Large step sizes will reproduce faster rise times but will also reduce the number of distinguishable levels obtainable from the integrator. Therefore, the maximum frequency that can be faithfully reproduced is directly proportional to step size. Obviously, some compromise must be made between transient response and the number of gray-scale levels desired to reduce contouring.

(3) Noise Immunity

The final characteristic to be discussed is noise immunity. Delta Modulation systems employing linear integrators have relatively poor noise performance as compared with PCM. A transmission error is propagated for the entire scan line or until the integrator is reset at the beginning of the next scan line because a linear integrator has memory. There is no decay of the output signal between input pulses. To cancel out the effect of the noise prior to resetting the integrator, linear integrators need as many positive error pulses as negative error noise pulses.

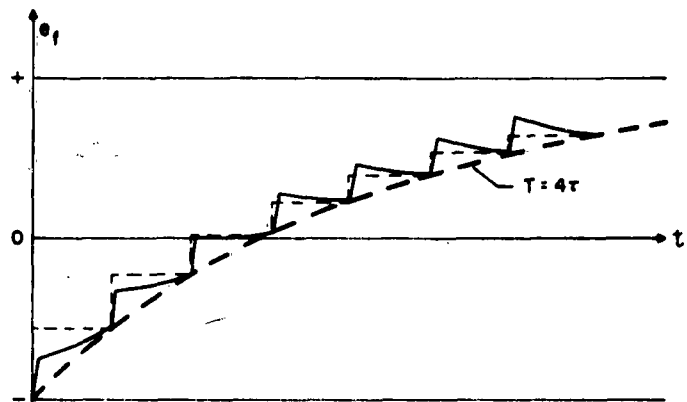
b. Exponential Integration^{4, 5}

Decreasing the time constant of a linear integrator to some small finite value produces an exponential integrator. Such an integrator used in a Delta Modulator has several important characteristics.

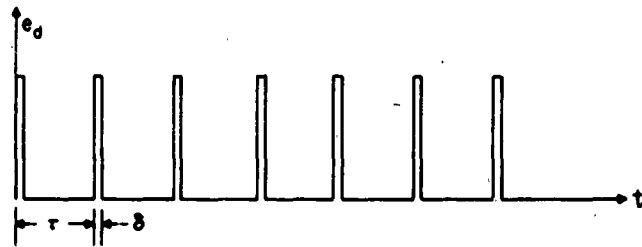
(1) Utilization of Image Statistics

Figure 3 (a and b) shows the output of an exponential integrator fed by a series of equal-amplitude pulses of width δ . The exponential shown has a time constant of approximately 4τ , where τ is the interval between input pulses. Notice that the contribution from each pulse is not a constant amount but varies as the integrator output approaches the upper limit. Equal pulses fed into such an integrator will produce more of a change when the integrator is discharged than when it is nearly charged. This can be seen by comparing the dotted steps in Figure 3a which show the amount of signal contributed by each input pulse. Thus, one of the attributes of an exponential integrator is the fact that at either extreme there is a maximum chance of increase or decrease. When reproducing an increasingly lighter or darker gray level, there is a progressively smaller chance that the next sample will be toward white or black as the extremes are approached.

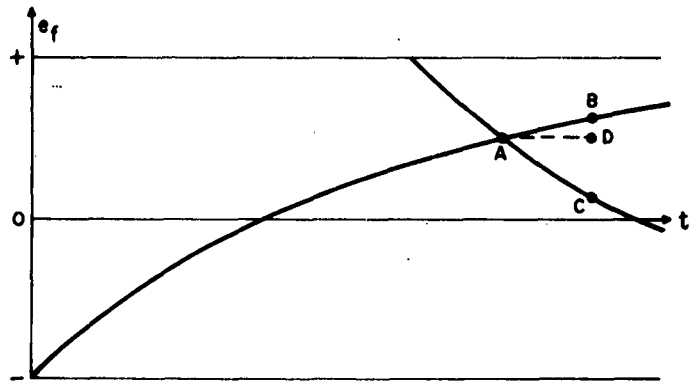
Figure 3c illustrates the change which would occur along two different integrating paths whose time constants are identical. If the last output of the integrator is at level A, a point near the upper extreme, the next input pulse can move the signal along either path. If the input pulse is



a. OUTPUT OF INTEGRATOR



b. INPUT PULSE TRAIN



c. CHARGING PATH AS A FUNCTION OF POSITION AND DIRECTION

Figure 3 Characteristics of Exponential Integration

positive, the output will be at level B; if the pulse is negative, the output will be at level C. Notice that DC is greater than DB, the maximum change being in the direction of most probable direction of the input signal -- toward the lower extreme. Thus various step sizes are used where they are most likely to occur.

(2) Reduced Contouring

Contouring effects are reduced using exponential integration. Two steps rarely occur at exactly the same gray level because of the nonlinear nature of an exponential curve. Thus distinct contours which would ordinarily occur with a linear integrator are broken up and do not appear as objectionable in the generated output image.

(3) Better Rise Time Response

The initial slope of an exponential curve can be made quite high, thereby introducing larger steps initially to follow fast changes in the input waveform without introducing the attendant contouring problems, as in the linear integration system. Therefore, higher bandwidth signals can be reproduced.

(4) Good Noise Performance

An exponential integrator has relatively good performance in the presence of data-link noise. The fact that the time constant of the integrator is finite means that between input pulses the integrator decays exponentially with the same time constant that is used for integrating the pulse. This decay can be seen in Figure 3a. The integrator, therefore, has a short memory and the system recovers very quickly from a noise pulse. The length of time it takes the integrator to recover is directly proportional to the time constant of the exponential. As pointed out previously, linear integrators which have long time constants require long times to recover. Exponential integrators, with their shorter time constants, are in a much more favorable position in this respect.

(5) Oscillation Effect

An undesirable effect occurs if the input pulse rate or sampling rate is too low. Operation in a region away from the midpoint of the dynamic range dictates that a step in one direction will be greater than a step in the other direction (see Figure 3c). When point A is near the upper extreme, several positive steps are required to balance one negative step and a large amplitude oscillation having a frequency low relative to the sampling frequency is

encountered in this region. The amplitude and frequency of this oscillation are a function of the location of the input in the dynamic range. At the midpoint, the amplitude is minimum and the frequency maximum. The frequency of oscillation can be made subjectively unobjectionable by increasing the sampling rate or increasing the time constant of the integrator. Therefore, a compromise must be made between τ , the sampling period, and T , the time constant of the integrator, to achieve acceptable output images.

4. Double Integration

a. Straight Double Integration²

In the Delta Modulation systems discussed above, every input pulse to the integrator had the effect of increasing or decreasing the level of the output signal by a certain amount. An integration process where every input pulse has the effect of changing the slope instead of the amplitude of the output signal has been reported in the literature. A train of pulses derived from the Delta Modulation quantizer is converted to the signal, e_f , shown in Figure 4 by the use of a double integrating network. The output of the first linear integrator is a step waveform. Linear integration of a step function is a signal of constant slope. The train of pulses to be integrated is derived by subtracting e_f from e_s , the input signal, and quantizing the resultant error signal. Every pulse changes the slope of e_f by the same amount in the positive or negative direction.

Double integration has several important characteristics. Contouring is a function of the initial slope, S , shown in Figure 4. Here S has been specified in terms of the step size, I , of the first linear integrator. Since S is one-half the value of I , the number of reproducible levels available from the double integrator would be twice that from the single linear integrator, thereby decreasing the contouring associated with such systems. Double integration systems have better transient response. Notice in Figure 4 that, for a single linear integrator, seven steps would be required to reproduce the rise of e_s (solid plus dotted steps). However, only four steps (solid steps) from the first integrator were required for the double integration system.

All of the previous comments concerning noise performance for a linear integrator apply to double integration because any transmission noise will alter the input pulse train and be reflected for a long time in the output of the first integrator. One other disadvantage is readily seen in Figure 4. The output signal, e_f , crosses e_s with a high value of its first derivative and causes the system to produce negative pulses during a long time interval. Consequently, e_f will again cross e_s with a high negative value of its first derivative, and large amplitude oscillation is maintained causing a great deal of overshooting.

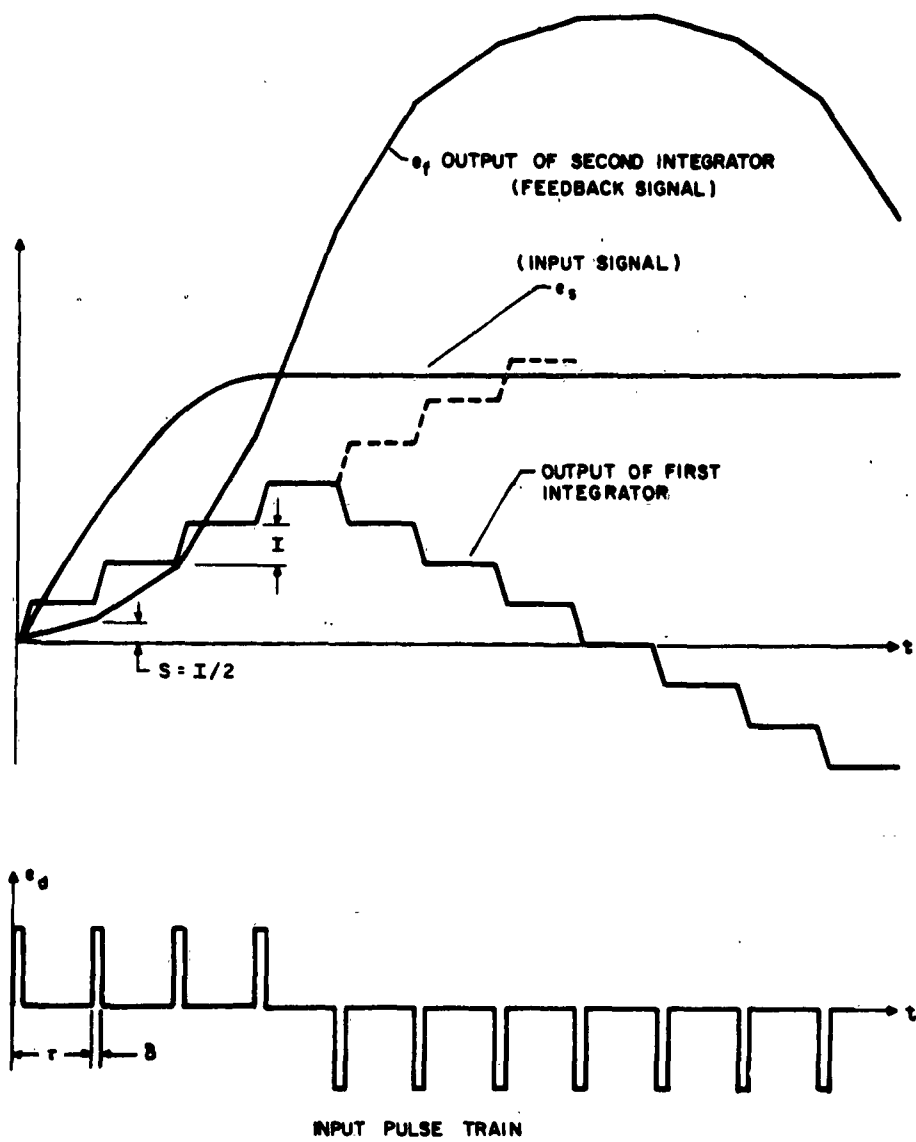


Figure 4 Delta Modulation Using Double Integration

b. Double Integration with Prediction² (DIWP)

One logical way to prevent this overshooting is to have the ability to look ahead and foretell the future value of the signal. In this manner, the first derivative of e_f , when it crosses e_s , will not be quite as large and less overshooting will occur. Figure 5 shows a Delta Modulation system using double integration with prediction. With this system, values of the signal, e_s , are predicted assuming the present slope of e_f does not change -- hence the dotted lines in the figure. These predicted values are compared with e_s to generate an error signal and the train of input pulses. A comparison of Figures 4 and 5, where e_s is the same signal for both systems, shows that overshooting is reduced considerably. The prediction interval can be as long as desired. However, transient response is directly related to the length of this interval. As the prediction interval approaches zero, the transient response approaches the maximum available from double linear integration. As the interval is lengthened the transient response becomes poorer and approaches the response of a single linear integrator. Thus, one advantage of double integration would be lost. The prediction interval shown in Figure 5 is 1τ , where τ is the pulse rate period.

Double integration with prediction has the same advantages as double integration without prediction with respect to contouring and transient response. Its noise immunity is poor, since double integration with prediction uses linear integrators with long time constants.

c. Double Integration with Phase Reversal⁶

A second technique for reducing the overshoot and oscillation characteristic of straight double integrators has recently been developed. This approach is more effective than double integration with prediction because it provides the means for instantaneous reversal of the slope of the output waveform. This system contains an integrator which sums the waveforms of two exponential generators together to form the output signal. Conventional one-bit Delta Modulation sends only one unit change of level per pulse. Information theory suggests that, with a sequence of n pulses, all of the same polarity, the level should vary as 2^n or exponentially (the logarithm base two). The system to be described here can provide increments which vary exponentially with time. The equations below illustrate the correspondence between 2^n and the naperian function e^t . If

$$e^t = 2^n,$$

then

$$t = n \ln 2 = 0.693 n.$$

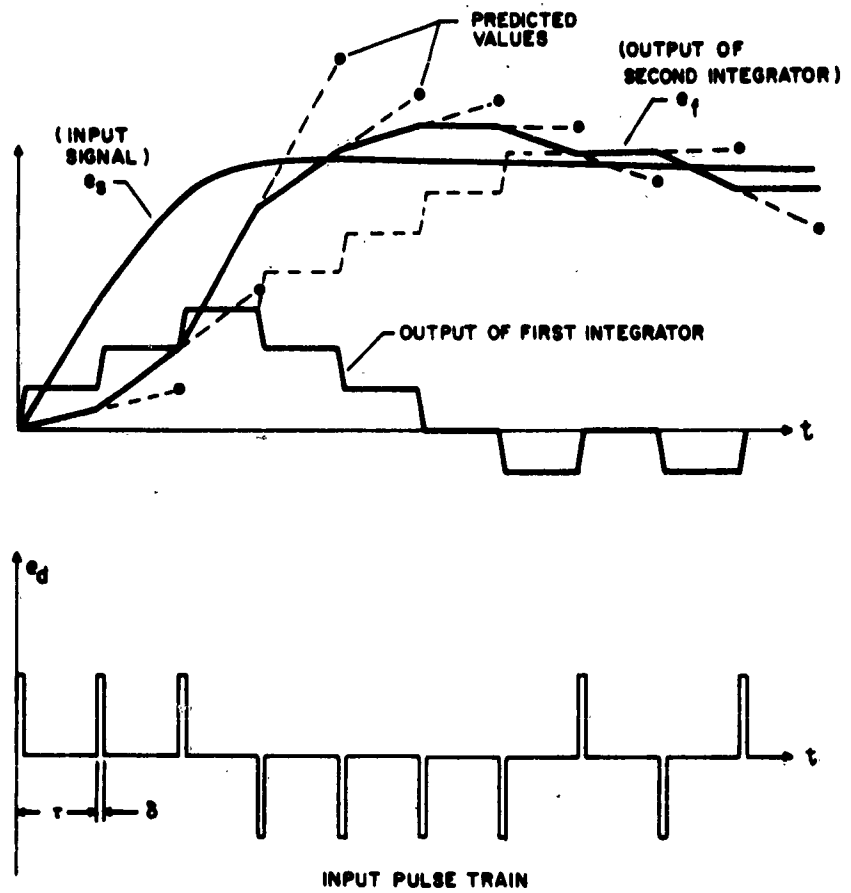


Figure 5 Delta Modulation Using Double Integration with Prediction

Figure 6 is a block diagram of the double exponential integrator. The flip-flop takes a state depending on the polarity of the pulses derived from the one-bit quantizer in the Delta Modulation system. The exponential generators are used alternately, one generating positive waveforms for positive pulses and the other, negative waveforms for negative pulses. The impulse device delivers the proper initial impulse to the exponential generators whose outputs are summed in an integrator to provide the desired output.

The exponential level change is illustrated in Figure 7, which shows the approximated system response to a step function. Initially, with the positive start pulse, a transmitted level might be one unit of amplitude. If this is insufficient, another pulse of the same polarity adds another unit, doubling the quantity. If this is again insufficient, another positive pulse adds two more units, again doubling the quantity. Thus, the total count proceeds exponentially with pulses transmitted according to 2^n . Should the increment be too large, the pulse signal reverses and the count direction reverses, reducing in magnitude by a factor of two. In two steps (see Figure 7) it retraces the over-correction searching for the correct magnitude. This situation is contrasted with double linear integration which may take many steps to retrace the over-correction.

This type of integrator has several important characteristics. Contouring would be virtually eliminated because increments as small as ± 1 unit are possible. The high frequency response of the system would be good because of its fast phase reversal characteristic. Its noise immunity characteristics would be an improvement over that for double linear integration because of the finite time constants of the exponential generators.

Several disadvantages are apparent, however. As can be seen in Figure 7 the system overshoots by a rather large amount, depending upon the amplitude of the step input. Incorporating a prediction feature or slope limiter would limit this. The response of the system to large-amplitude step inputs starts out rather slowly and builds up faster and faster. This is contrasted with single exponential integration Delta Modulation systems which have the largest contributions with the initial pulses. Succeeding increments get smaller and smaller. The phase reversal system does not make use of the probability characteristics of image data as does the exponential integrator.

Table 1 summarizes the important characteristics of the integrators used in Delta Modulation systems.

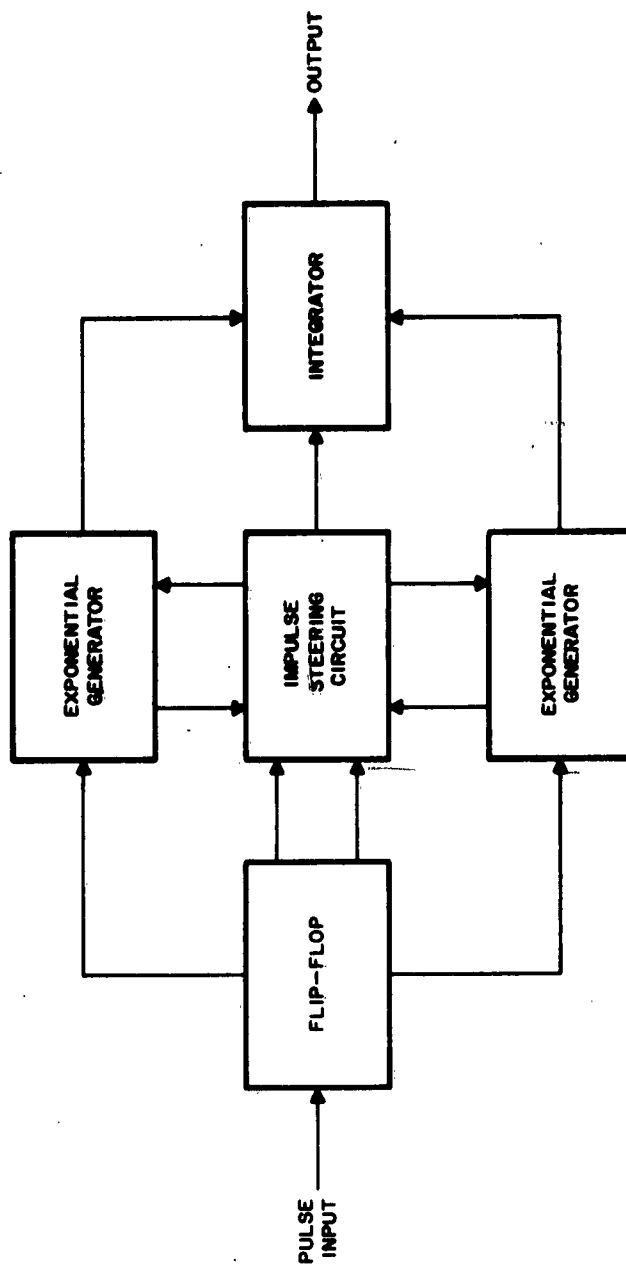


Figure 6. Double Exponential Integrator

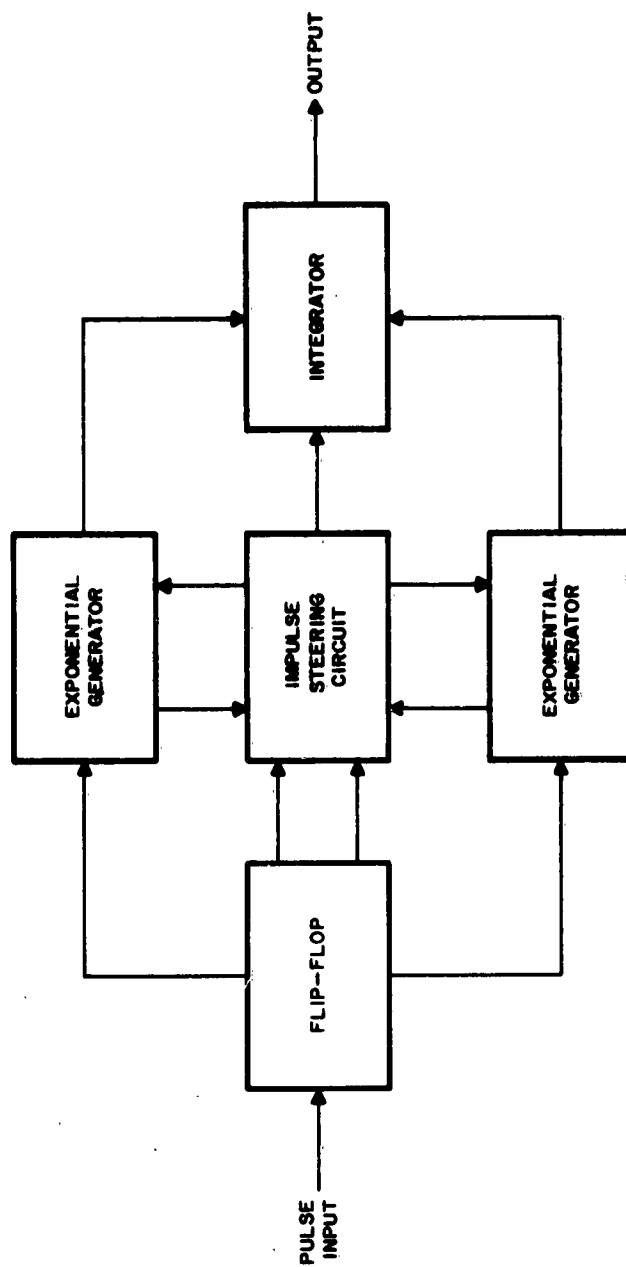


Figure 6. Double Exponential Integrator

TABLE 1
INTEGRATOR CHARACTERISTICS

Type	Increment	Number of Reproducible Levels	Effects of Transmission Errors	Length of Time Constant	Transient Response	Implementation Considerations	Advantages	Disadvantages
Single Linear	Fixed steps	Limited by step size	Entire scan line or until integrator is reset.	Long	Limited by number of steps to cover dynamic range of input signal to Delta system.	Attenuation in integrator network. Gain required in feedback loop.		Contouring. Poor noise immunity. Poor transient response.
Double Linear	Fixed slopes	Limited by initial slope	Entire scan line or until integrator is reset.	Long	Limited by initial slope.	Same	Reduced contouring. Better rise time response.	Overshoot. Poor noise immunity. Loss of high-frequency detail at low sampling rates.
Double Linear with Prediction	Fixed slopes	Same	Entire scan line or until integrator is reset.	Long	Same; also, limited by prediction interval used.	Same	Reduced overshoot. Good rise time response.	Poor noise immunity. Loss of high-frequency detail at low sampling rates.
Exponential	Variable steps	Continuous	Few elements. Time of recovery directly proportional to time constant.	Short	Limited by time constant.	Relatively easy to implement.	Reduced contouring. Good noise immunity. Makes use of probability characteristics of image data.	High amplitude oscillation about DC at extremes of dynamic range.
Double Integration with Phase Reversal	Variable steps in accordance with $\log_2$	Continuous	Few elements	Short	Limited by number of binary steps required to cover dynamic range of input signal.	More components required.	Reduced contouring. Good noise immunity. Good rise time response. Good high-frequency response.	Large overshoot. Does not make use of probability characteristics of image data.

B. Mathematical Description

1. Derivation of General Equation

An equation for the output voltage of an RC integrating network of a Delta Modulation system whose input is a pulse has been set forth by Holzer.⁴

$$V_n(t) = \left[V_{n-1}(t) + h(e^{\delta/T} - 1) \right] e^{-t/T}, \quad (1)$$
$$\delta \leq t \leq \infty$$

where

$V_{n-1}(t)$ = voltage across the capacitor at the beginning of the pulse,

h = pulse height,

δ = pulse width,

T = time constant of RC integrator.

As pointed out by Holzer, each pulse yields an instantaneous increase of

$$G = h(e^{\delta/T} - 1) \quad (2)$$

in the input voltage, independent of the charge across the capacitor; however, the effective increase of output voltage between two instants of time, T , is dependent on the initial charge of the capacitor. A sequence of pulses will produce an output waveform similar to that shown in Figure 8. Mathematically, the output voltage at the end of each T , the pulse period, is:

$$V_n = Ge^{-T/T} + Ge^{-2T/T} + \dots + Ge^{-nT/T}$$
$$V_n = G \sum_{n=1}^{n=\infty} e^{-nT/T} \quad (3)$$

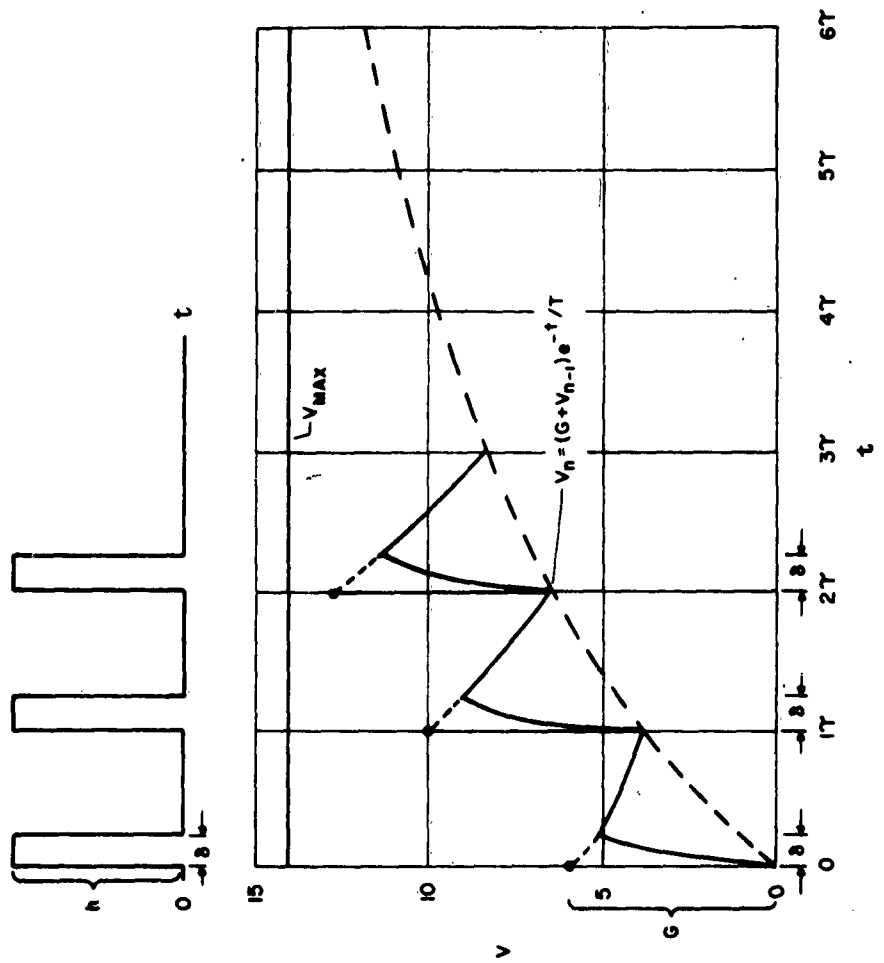


Figure 8 Response of RC Integrating Network

As n increases, it is clear that V_n approaches a limit:

$$\begin{aligned} V_{\max} &= \frac{h(e^{\delta/T} - 1)}{e^{\tau/T} - 1} \\ &= \frac{G}{e^{\tau/T} - 1} \end{aligned} \quad (4)$$

It is straightforward to generalize Equations 1 to 4 to include multibit Delta Modulation systems with both linear and exponential integration. In the multibit case, G , the instantaneous increase of voltage at the beginning of a sample period takes on more than one value and for a two-bit system is designated

G_L = large increment,

G_S = small increment.

The decision to use G_L or G_S in any sample period is determined by the magnitude of the error signal existing at the beginning of the sample period. Therefore, the output voltage at the end of the sample period is:

$$V_n = (\pm G_{L,S} + V_{n-1}) e^{-\tau/T} \quad (5)$$

For systems employing a single linear integrator, the time constant, T , becomes very large so that Equation 5 reduces to

$$V_n = \pm G_{L,S} + V_{n-1} \quad (6)$$

Cascading of two linear integrators together produces the double integration process, described in Section II-A-4. For a one-bit system, the value of G takes on only one value, and consequently the output of the first linear integrator becomes

$$V_n = \pm G + V_{n-1} \quad (7)$$

Since V_n is the input to the second linear integrator, the output of this integrator at any instant of time depends upon the amplitude of V_n and its sign. A measure

of this amplitude is given by the count number, C_n , where

$$C_n = \frac{V_n}{G} \quad (8)$$

Essentially, C_n counts the number of steps of the staircase which are above or below zero, the center of the dynamic range of V_n . Also, C_n may be thought of as counting the net number of input pulses to the first integrator at any instant of time. From this standpoint, the first integrator may be replaced by a pulse counter which keeps track of the net number of positive and negative pulses received from the one-bit quantizer. The minimum or initial output of the second integrator (in amplitude units per sample time) corresponding to a count number of plus or minus one is called the initial slope, S . Succeeding slopes corresponding to other count numbers are multiples of this initial slope. Therefore, the contribution to the output at the end of each sample period provided by the various count numbers or outputs from the first integrator is SC_n . The final output from the double integrator is given by

$$V_n = SC_n + V_{n-1} \quad (9)$$

where the V_{n-1} , here, signifies the previous output from the second integrator.

For the double integration with prediction system the second integrator incorporates a prediction circuit which predicts the output at some time interval later, assuming that the present slope of SC_n does not change. If the prediction interval is labeled P , and specified in terms of τ , the sample period, the two outputs of the second integrator for the one-bit DIWP system are

$$V_n = SC_n + V_{n-1}$$

and

$$V_{pn} = SC_n P + V_n \quad (10)$$

where V_{pn} is the predicted signal.

In summary, a set of general equations for the output voltage of various Delta Modulation systems is shown in Table 2.

TABLE 2
GENERAL EQUATIONS FOR
VARIOUS DELTA MODULATION SYSTEMS

System	General Equations
1-bit Exponential	$V_n = (\pm G + V_{n-1}) e^{-\tau/T}$ (11a)
1-bit Linear	$V_n = \pm G + V_{n-1}$ (11b)
1-bit DIWP	$V_n = SC_n + V_{n-1}$ (11c)
	$V_{pn} = SC_n P + V_n$ (11d)
2-bit Exponential	$V_n = (\pm G_{L,S} + V_{n-1}) e^{-\tau/T}$ (11e)
2-bit Linear	$V_n = \pm G_{L,S} + V_{n-1}$ (11f)

2. Discussion of Parameters

a. Maximum Integrator Voltage

In a linear Delta Modulation system, the maximum output voltage, in theory, is not limited (see Equation 6). However, in practice, the maximum voltage is limited by supply voltages and the inability of achieving a perfectly linear integrator. If noise in the transmission path causes errors in the received code, voltages which fall outside the signal dynamic range can be obtained from the Delta Modulator decoder. Furthermore, a transmission error results in dc shift in all succeeding picture elements until the integrators are again reset.

For exponential Delta Modulation systems, the maximum output voltage has a limit as described by Equation 4. In a practical system, parameters such as pulse width, δ , and pulse height, h , are usually fixed, and the remaining variable is the time constant, T . Figure 9 shows a curve of the maximum output voltage, normalized to the pulse height, as a function of the time constant of the integrator for a fixed pulse width. Further calculations show that this maximum output voltage is linearly related to the pulse

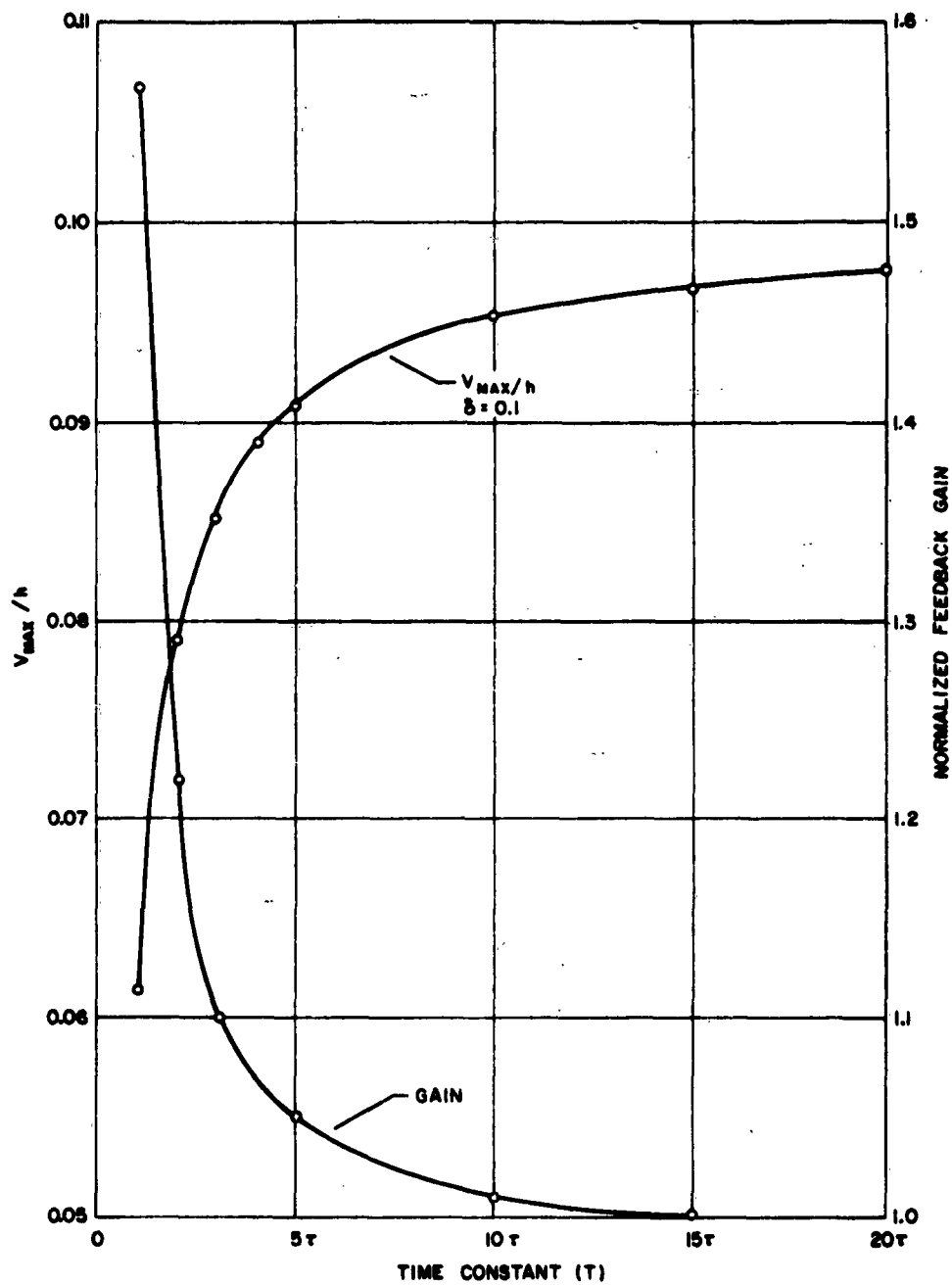


Figure 9 Maximum Integrator Voltage and Gain Requirements

height and nearly linear to the pulse width. Also shown in Figure 9 is the relative gain required in the feedback loop as a function of the time constant, T . The gain has been normalized to that required to make the integrator output dynamic range equal to the input dynamic range at a time constant of 15τ . Notice that the maximum integrator output voltage drops off rather suddenly in the region from 0 to 5τ . Therefore, more feedback gain would be required in this region to maintain the integrator dynamic range equal to that necessary at $T = 15\tau$.

As pointed out previously, one advantage of exponential integration is that it makes use of one of the probability characteristics of image data in such a manner that the magnitude of the change of integrator voltage from one sample period to the next is related to the probability of the change. As shown in Figure 8, the increase in voltage in any sample period is a function of the amplitude of the voltage on the integrator existing at the beginning of the sample period. It is apparent that, to take full advantage of this exponential characteristic of the integrator, it is necessary to make $V_{\max}$ identical with the maximum amplitude of the input signal by providing the required amount of linear gain in the feedback loop. By using this design procedure, signal voltages produced by the decoder must all lie within the input signal range. Therefore, errors due to transmission noise cannot produce voltages outside the signal range.

b. Integrator Time Constant

Referring to Equation 5 and rearranging,

$$V_n = \pm G_{L,S} e^{-\tau/T} + V_{n-1} e^{-\tau/T}, \quad (12)$$

it is seen that as T , the time constant of the integrator, becomes smaller, the value of K in Equation 13 decreases.

$$K = e^{-\tau/T}. \quad (13)$$

In effect, the value of T determines the number of previous samples used in calculating the new value of the integrator voltage. Therefore, as T increases and K approaches 1.0, as in a linear integrator, all previous samples (the second term of the right-hand side of Equation 12) are used in the new value. The first term is also affected by T in that, for a given G , the effective value of G at the end of the sample period is dependent on K . For example, if T is small so that K is small, then a very small change in output voltage occurs due to G . On the other hand as K approaches 1.0, the output voltage is modified by the entire magnitude of G .

As noted earlier, the value of T differentiates the two main types of integration and, consequently, two classes of Delta Modulation systems. When the value of T approaches infinity, a class of linear systems is obtained. As T approaches the range of 0 to 20τ , a class of nonlinear, or exponential, systems is realized.

c. Step Sizes and Reference Levels

Reference levels and step sizes are fundamental parameters associated with the quantization of analog signals into binary form and the reconversion of the binary words into analog form. In Delta Modulation systems, these parameters have the same association as in conventional analog-to-digital systems, but their significance is somewhat different. For instance, the precision of encoding directly determines how fine a quantization of the encoded signal is achieved; however, the error signal, rather than input signal, is encoded. The reference levels in a multibit quantizer directly determine the output code and, consequently, which step size is to be used in the integration process in the feedback loop.

A combination of reference levels and step sizes may be chosen to obtain a nonlinear encoding characteristic which enhances the performance of a Delta Modulation system. As an example, in a two-bit system with a linear integrator, one may choose a set of reference levels and step sizes as shown in Figure 10. The encoding range is divided into four unequal quantization intervals by the three reference levels, R_1 , R_2 , and R_3 , to form a nonlinear encoding characteristic. An appropriate code group is transmitted for each sample representing the sign and magnitude of the error signal during that sample period. At the receiver the code groups are decoded into the various step sizes as shown and integrated with the previous integrator values.

Generally, code groups 11 and 00 represent error signals which have been generated because of fast rise times or transitions in the input signal. By assigning relatively large step sizes for these code groups (see Figure 10), an advantage in rise-time response is gained by using a nonlinear encoding characteristic. On the other hand, code groups 10 and 01 represent small values of error signals which indicate that the input signal is not changing rapidly and probably represents a uniform brightness area in the image. Since the decoded words yield the small step sizes shown in Figure 10, small-amplitude detail is not lost by the quantization process. Other combinations of reference levels and step sizes can be derived to gain certain advantages such as even faster rise-time response or better small-detail response.

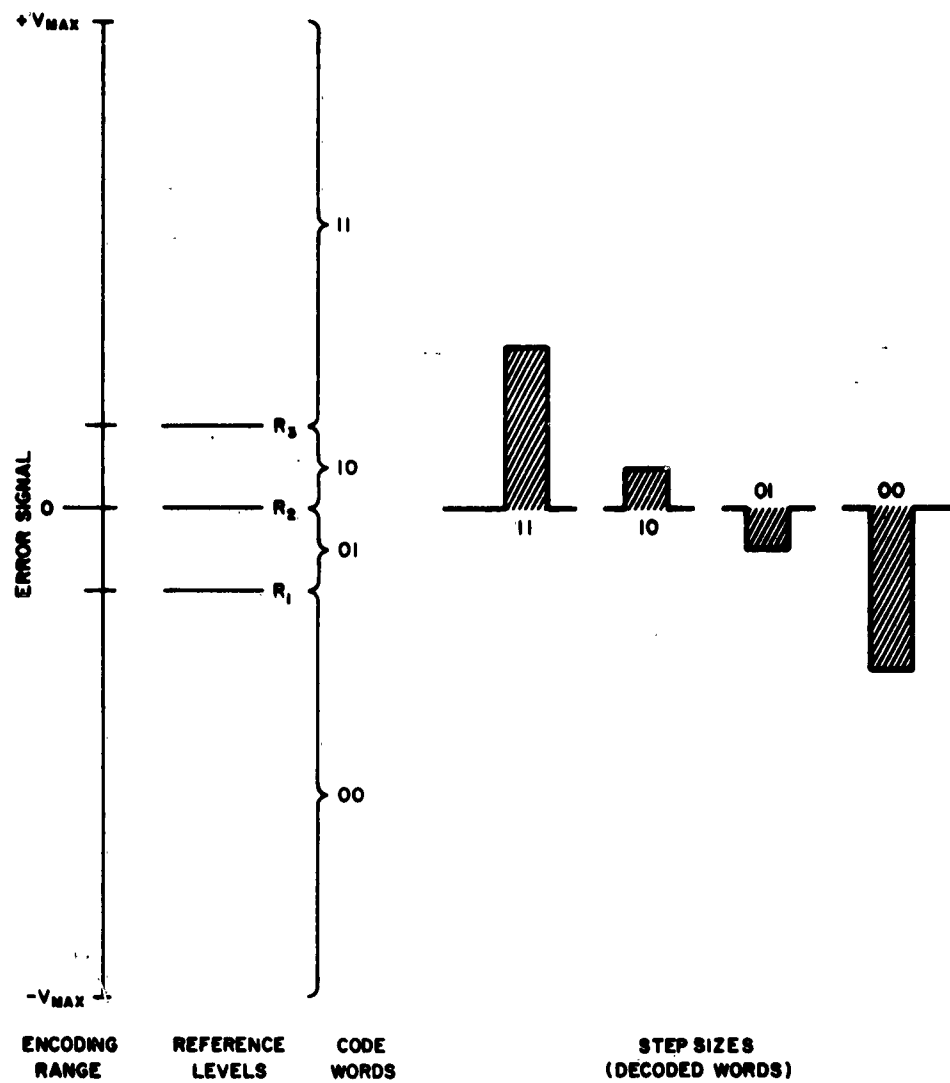


Figure 10 Typical Reference Levels and Step Sizes

d. A Limitation of Multibit Exponential Integration

It has been noted previously that the use of an exponential integrator results in output integrator voltages which are dependent on the magnitude of the integrator voltage. Also it was shown that there is a $V_{\max}$ associated with a given set of system parameters. In multibit exponential systems, a particular problem associated with the use of more than one pulse height and reference level arises.

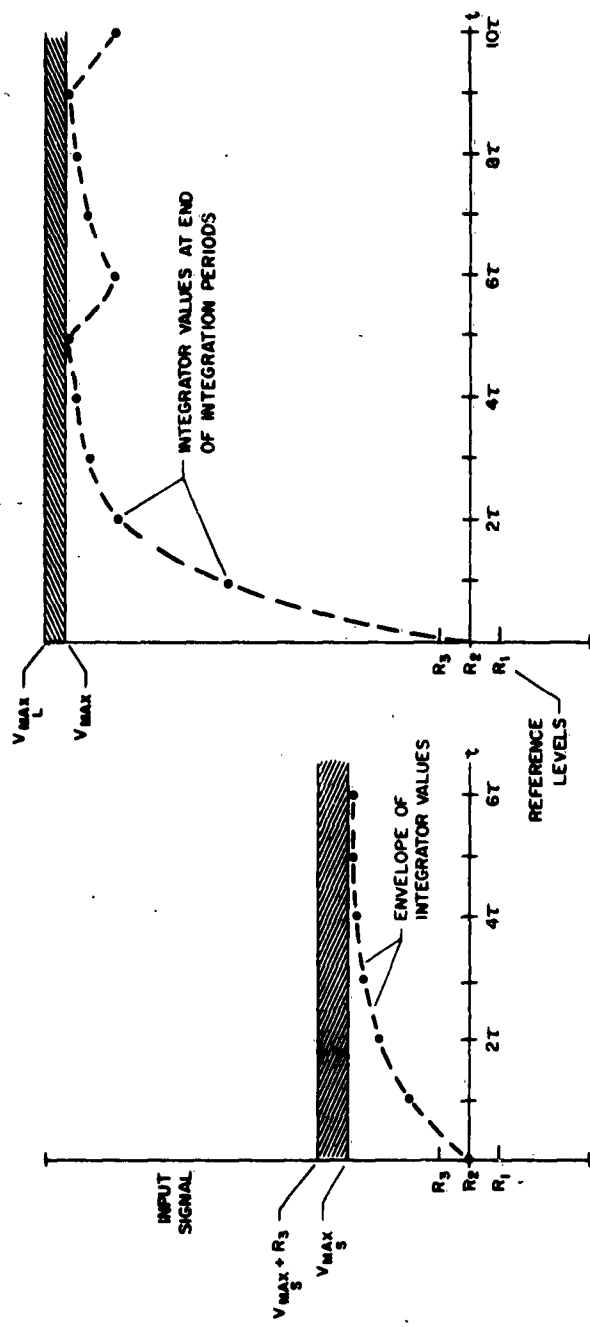
A detailed analysis of two-bit exponential Delta Modulation systems revealed that four regions existed in the integrated output signal range for which integrator values could not be produced except under certain transient conditions. Two of these regions exist at the ends of the dynamic range of the integrator and the other two at points just beyond the maximum integrator voltage that is obtained by integrating a sequence of small pulses.

The exact location of the latter regions is determined by substituting the value of G_S in Equation 4.

$$V_{\max S} = \frac{G_S}{e^{\tau/T} - 1} \quad (14)$$

where $V_{\max S}$ is the maximum voltage obtainable with a sequence of small pulses. The magnitude or width of these regions is equal to the magnitude of the largest reference level.

Recalling that Equation 14 is the limit of the integral of a sequence of small pulses and referring to Figure 11a, the mechanism leading to these regions is described. From Figure 10 it is recalled that an error signal falling between reference levels R_2 and R_3 is decoded at the receiver as a small positive pulse or step. In Figure 11a the integrator build-up due to a sequence of these small pulses is shown. The sequence of small pulses will continue as long as the difference (error signal) between the input signal and the integrator signal is less than the magnitude of reference level, R_3 . Therefore, after about 4τ in Figure 11a, an input dc signal whose magnitude lies between $V_{\max S}$ and $V_{\max S} + R_3$ will sustain this sequence of small pulses. But the maximum voltage that can be obtained from this sequence is $V_{\max S}$. Therefore, all dc input voltages in the shaded area of Figure 11a are decoded as $V_{\max S}$. Effectively, then, a quantization of part



6.

0.

Figure 11 Limitations of Exponential Integration

of the input signal range occurs at $V_{\max_S}$ and the magnitude of this quantization region is equal to the magnitude of large reference level, R_3 . A similar region occurs at $-V_{\max_S}$.

The region of quantization at the extreme of the input signal range is shown in Figure 11b. Recalling again that a sequence of large pulses will build up an integrator voltage $V_{\max_L}$, assume that the input dc signal is $V_{\max_L}$. When the difference between the input signal and integrator signal is less than the large reference level, a small pulse is integrated resulting in a net decrease in the integrator voltage, shown at $6T$ in Figure 11b. It is apparent, then, that the integrator voltage cannot build up to $V_{\max_L}$, since a sequence of large pulses is not sustained. The maximum voltage that can be obtained by a mixed sequence of large and small pulses is shown as $V_{\max_L}$ in Figure 11b. All input dc signals between $V_{\max_L}$ and $V_{\max_L}$ are decoded as $V_{\max_L}$, resulting in another quantization at the extreme of the input signal range. The magnitude of this region is less than the reference level, R_3 . An identical region exists at the negative extreme of the input signal range. In effect, these regions at the extremes reduce the dynamic range of the Delta Modulation system.

One method for eliminating these regions at the extremes in a noiseless data-link environment is to choose a set of system parameters (pulse height, pulse width, and reference levels) which would insure that these regions exist just beyond the limits of the signal dynamic range. In a practical system subjected to data-link noise, an error in the transmitted code could cause the receiver to produce a decoded signal value that is outside the dynamic range of the image reconstruction equipment. However, it would appear that suitable limiters in this equipment would minimize this type of error.

The effect of the first regions described upon the over-all system performance does not appear to degrade the high-detail areas of an image, since integrator values can be produced within these regions under transient conditions. In low-detail areas, the resulting quantization of uniform brightness areas within the regions produces contouring similar to that obtained in low-precision PCM systems and in Delta Modulation systems using linear integration. Summarizing, it is expected that these regions will not be noticeable in high-detail areas and, since the probability of occurrence is small in the low-detail areas, insignificant contouring will be introduced.

III. COMPUTER SIMULATION

A. Introduction

Computer simulation of candidate Delta Modulation concepts has provided a thorough, low-cost investigation and evaluation of the performance of each system so that a feasibility model could be proposed with its parameters optimized at the end of Phase I. The use of a computer has allowed the rapid evaluation of several types of Delta Modulation logics using many different sets of parameters. By trading off competitive system performances in terms of image quality with system costs in terms of size, weight, and power, the best compromise system was selected.

Fifteen different Delta Modulation logics were simulated during the course of the program, eleven during Phase I and four during Phase II. Table 3 defines each system simulated in terms of the following descriptive parameters:

- (1) Precision of encoding - one or two bit.
- (2) Sampling rate - 2 or 4 samples per cycle.
- (3) Type of integrator - single linear, single exponential, and double linear with prediction.
- (4) Threshold levels and step sizes.

The one- and two-bit simulations were written as separate programs primarily because this arrangement provided ease of program "debugging" and also produced processed output pictures for more economical evaluation with less computer running time.

TABLE 3
SUMMARY OF DELTA MODULATION SYSTEMS SIMULATED

Precision of Encoding	Number of Samples per Cycle	PHASE I		PHASE II
		Single Linear Integration	Exponential Integration	
1-Bit	2	1. Step Size = ± 5 Levels. Reference Level = 0 Limiting Required.	5. $T = 4.048 \tau$. $H = \pm 7.0$ Levels. Reference Level = 0.	
	4	2. Step Size = ± 5 Levels. Reference Level = 0. Limiting Required.	6. $T = 4.048 \tau$. $H = \pm 7.0$ Levels. Reference Level = 0	12. $S = 4$ Levels; $P = 1 \tau$. Reference Level = 0. Limiting Required.
				13. $S = 4$ Levels; $P = 2 \tau$. Reference Level = 0 Limiting Required.
				14. $S = 4$ Levels; $P = 3 \tau$. Reference Level = 0. Limiting Required.
				15. $S = 3$ Levels; $P = 2 \tau$. Reference Level = 0. Limiting Required.
2-Bit		3. Step Sizes: ± 15 Levels and ± 4 Levels. Reference Levels: ± 8 and 0. Limiting Required.	7. $T = 1.787 \tau$. $H_L = \pm 15$ Levels; $H_S = 4$ Levels. Reference Levels = ± 8 and 0.	
	2		8. $T = 3 \tau$. $H_L = \pm 9.1$ Levels; $H_S = \pm 2.4$ Levels Reference Levels = ± 8 and 0.	
			9. $T = 4 \tau$. $H_L = \pm 15$ Levels; $H_S = \pm 4$ Levels Reference Levels = ± 8 and 0.	
	4	4. Step Sizes: ± 15 Levels and ± 4 Levels. Reference Levels: ± 8 and 0. Limiting Required.	10. $T = 3 \tau$. $H_L = \pm 9.1$ Levels; $H_S = \pm 2.4$ Levels Reference Levels = ± 8 and 0. 11. $T = 4 \tau$. $H_L = \pm 15$ Levels; $H_S = \pm 4$ Levels. Reference Levels = ± 8 and 0. Limiting Required.	

B. Brief Description of the Delta Modulation Systems Simulated

The primary purpose of these simulations was to determine the effect of changing Delta Modulation system parameters and thus select an optimum set of parameters for a candidate system. Table 4 lists those parameters, common to all programs written, which may be varied in the simulation programs.

1. Linear Integration

The one- and two-bit single linear integration system programs are discussed together since they are quite similar. As the name implies, the integrator has a linear characteristic, and its computed equivalent is simply a "running" summer, since the computer has data only at the sample points of the six-bit PCM input data. Essentially, this means that the linear integrator is integrating a pulse one sample period wide and of sufficient amplitude to produce the desired step or rise in the integrator signal. A step size⁵ of something less than 10 percent of the dynamic range has been suggested as necessary for a working system. Therefore, a tentative value of ± 5 levels (image signal range is 64 levels) was chosen as a starting point for the first program run of the one-bit simulation. Various steps sizes and their corresponding percentages of image signal range are shown in Table 5.

The third column of Table 5 shows the equivalent precision of a PCM system having the same step-size resolution. Therefore, considering only step size, one would expect contouring due to quantization in an image which has been processed by a linear Delta Modulation system with a step size of 5 levels to be similar to that obtained by a PCM system with a precision of 3.7 bits.

It can be shown that the encoder integrator can produce all 64 levels of the input signal using a step-size value of ± 5 levels, provided limiting or clipping is included in the program to prevent the integrator from producing values outside the dynamic range of the input signal. The size of the step or increment will affect the fidelity with which high-detail areas are reproduced. Larger increments produce more rise-time information; however, they also produce more contouring in low-detail regions. For example, if the step size is increased to 8 (see Table 5), contouring corresponding to a three-bit PCM system would be observed (see Figure 12d). In the one-bit program, the polarity of the error signal determines whether the step is added to or subtracted from the "running" sum, the reference level obviously being zero. For the two-bit program, four step sizes and three reference levels are necessary, as shown in Figure 13.

TABLE 4

PROGRAM PARAMETERS OF DELTA MODULATION SIMULATIONS

Parameter	Range of Variation
Precision of Encoding	1- and 2-bits
Integrator Input Pulse	Amplitude variable over dynamic range of input signal. Pulse width variable over width of sampling period.
Reference Level	Variable over dynamic range of error signal.
Integration Characteristic	a. Linear - time constant assumed infinite. b. Exponential - time constant can be made equal to any desired number of sampling periods.
Sampling Rate	May be doubled both horizontally and vertically.
Noise Addition	Noise threshold variable over range of possible values that the random numbers can have.

TABLE 5
STEP SIZES

Delta Modulation Step Size (in levels)	% of Input Video Range (64 levels)	Equivalent Precision of PCM System (in bits)
2	3.1	5.0
3	4.7	4.4
4	6.3	4.0
5	7.8	3.7
6	9.4	3.4
7	10.9	3.2
8	12.5	3.0
9	14.1	2.8
10	15.6	2.7

The one-bit DIWP system consists of two linear integrators cascaded together with a prediction circuit included in the second integrator. A double mathematical integration of a pulse is a ramp or line of constant slope. The output signal then consists of a sequence of line segments at various slopes. The first parameter of importance is the initial slope, S , or the slope of the output from a single pulse input to the double integrator. All other slopes produced are multiples of S . Therefore, the amount of contouring to be expected and the amplitude of oscillation in constant brightness areas is directly dependent upon the initial slope. The second important parameter is the prediction interval which controls the amount of overshooting and the rise time response.

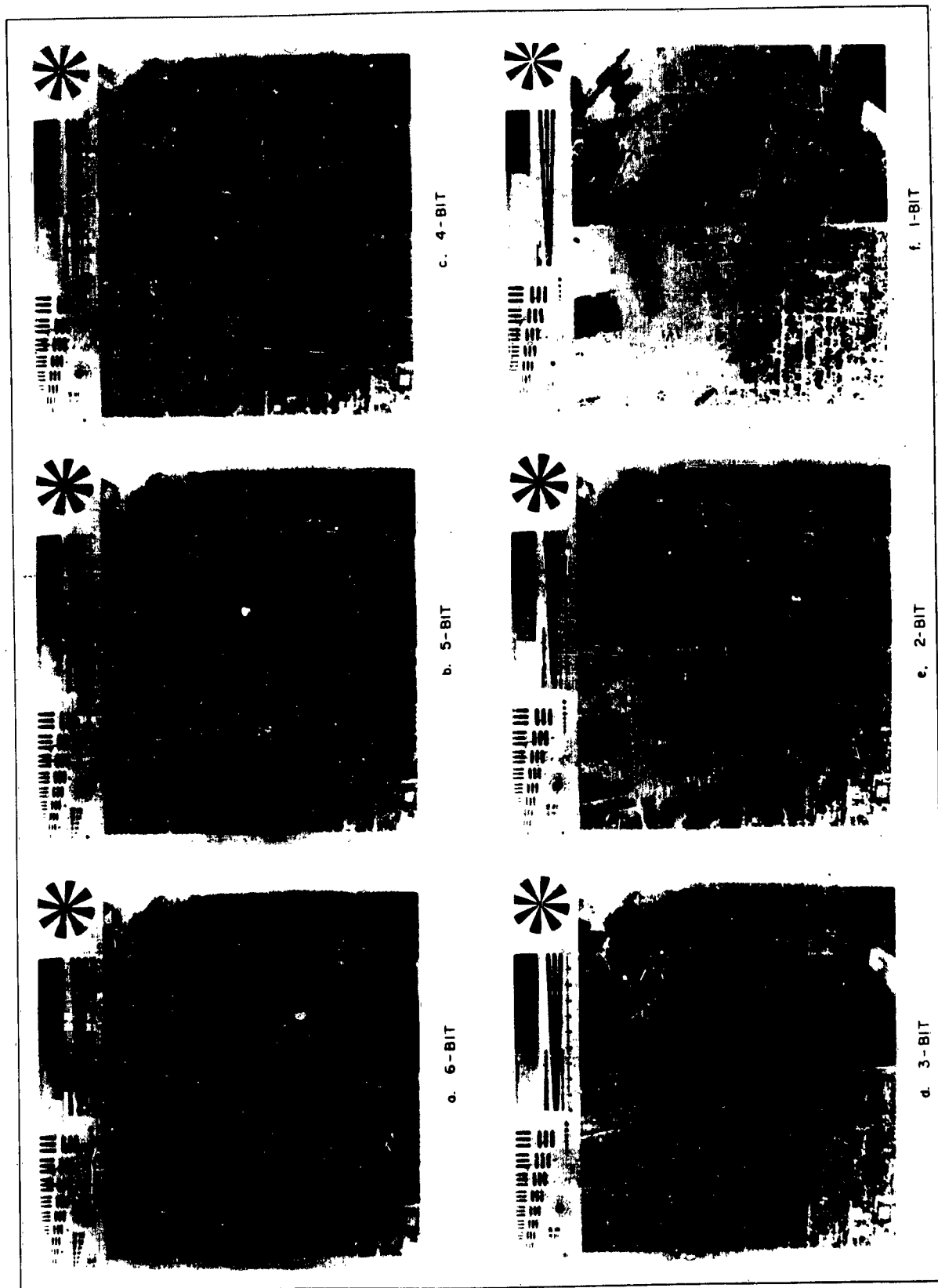


Figure 12 Various Precision PCM - 1024 x 512 Elements

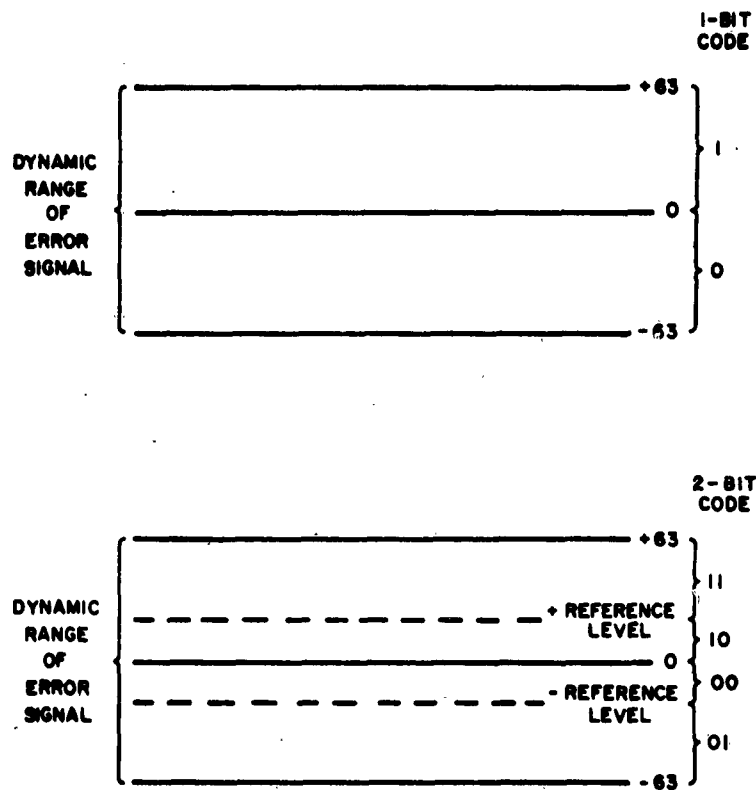


Figure 13 Quantization of Error Signal for One- and Two-Bit Systems

The computer solved the following equations at the sample points:

$$V_n = SC_n + V_{n-1} \quad (15)$$

and

$$V_{pn} = SC_n P + V_n, \quad (16)$$

where:

V_n = the output of the second linear integrator,

S = initial slope in amplitude units or levels per sample period,

C_n = net count of input pulses,

V_{pn} = the predicted signal,

P = prediction interval specified as a number of sample periods.

Section II-B contains a detailed description of these equations.

2. Exponential Integration

In the one- and two-bit exponential integration programs, the time constant of the integrator is not infinite but equal to some finite number of sampling periods. The computer solves the following equation at the sample points:

$$V_n = \left[h(e^{\delta/T} - 1) + V_{n-1} \right] e^{-\tau/T}$$

or

$$V_n = H + V_{n-1} e^{-\tau/T}, \quad (17)$$

where

$$H = h(e^{\delta/T} - 1)e^{-\tau/T}$$

and

V_n = the output of the integrator,

h = input pulse amplitude,

δ = input pulse width,

T = time constant of the RC integrator,

V_{n-1} = previous output of the integrator,

τ = sampling period.

Section II-B contains more information on the derivation of this question. The quantities, h , δ , and T , are the program variables concerned with the integration. The input pulse amplitude, h , has associated with it a sign; it may be positive or negative depending upon the polarity of the error signal. As mentioned in Section II, there is an upper limit on the maximum voltage that the integrator may build up (see Equation 4). This V_{max} , depending upon the parameters chosen, may extend beyond the limits of the input signal range to the Delta Modulator. Therefore, limiting was required to confine the range of the integrator output.

All of the programs written for this contract contained the ability to add data-link noise to the several Delta Modulation systems. As a matter of economy, two different noise thresholds were used for each program run so that the first half of the output picture used one error rate and the second half, another.

C. Simulation Considerations

1. Program Input Data

The image to be used as the input to all of the programs listed above is shown in Figure 14a. It was decided to use a composite image to aid in an economic evaluation of the degradation effects of each system on specific types of picture information and photographic characteristics. Notice that the composite image contains a city area with high detail and high contrast, a residential area with low detail and low contrast, a farmland area with low detail and high contrast, and an industrial area with a river containing slowly changing brightness. Also included in the composite image is a test chart area to aid in the evaluation of the linearity and resolution limits of the IMITAC, magnetic tape, film-transfer process required to place the image data in the proper format for the Philco 2000 digital computer. IMITAC is a laboratory equipment capable of transforming pictorial data into a six-bit binary signal (64 levels) and then storing this data on Philco 2000 compatible magnetic tape via the Universal Buffer Controller.

Appendix II contains a more detailed description of IMITAC as it is used in the simulations to be discussed. IMITAC may be adjusted to scan with a square raster at several different sampling rates; the horizontal rate can be different from the vertical rate. The size of the CRT spot in IMITAC as focused on the image plane was adjusted for a horizontal and vertical resolution of 256 spatial cycles across the widths of the picture. The calibration was accomplished by noting the 3-db down point of the video signal as the CRT spot scanned across a resolution bar chart having 256 line pairs per image width. Also, measurements made, using a slit aperture to measure the spot profile, indicated that it was approximately six mils wide in both the horizontal and vertical directions, the proper size for a raster three inches square. IMITAC was operated with 512 vertical scanning lines which is appropriate for the 256 line pairs per width resolution; it could be adjusted to sample each scanning line with either 512 or 1024 samples. Figures 14 and 15 show several images scanned with 512 and 1024 horizontal samples for the one-bit simulations. Variation of the sampling rate is desirable in order to make several important comparisons (see Table 6). For example, it would be advantageous to compare the one-bit Delta Modulation system at a sampling rate of "2a" with the two-bit system at a sampling rate of "a," since the bit rates are identical in both cases. Such a consideration is obviously desirable from an equipment complexity standpoint.

Using IMITAC, two separate input magnetic tapes were made, one scanned by a 512-x-512-element raster and the other scanned by a 1024-x-512-element raster. Each time a program was run the input tape was

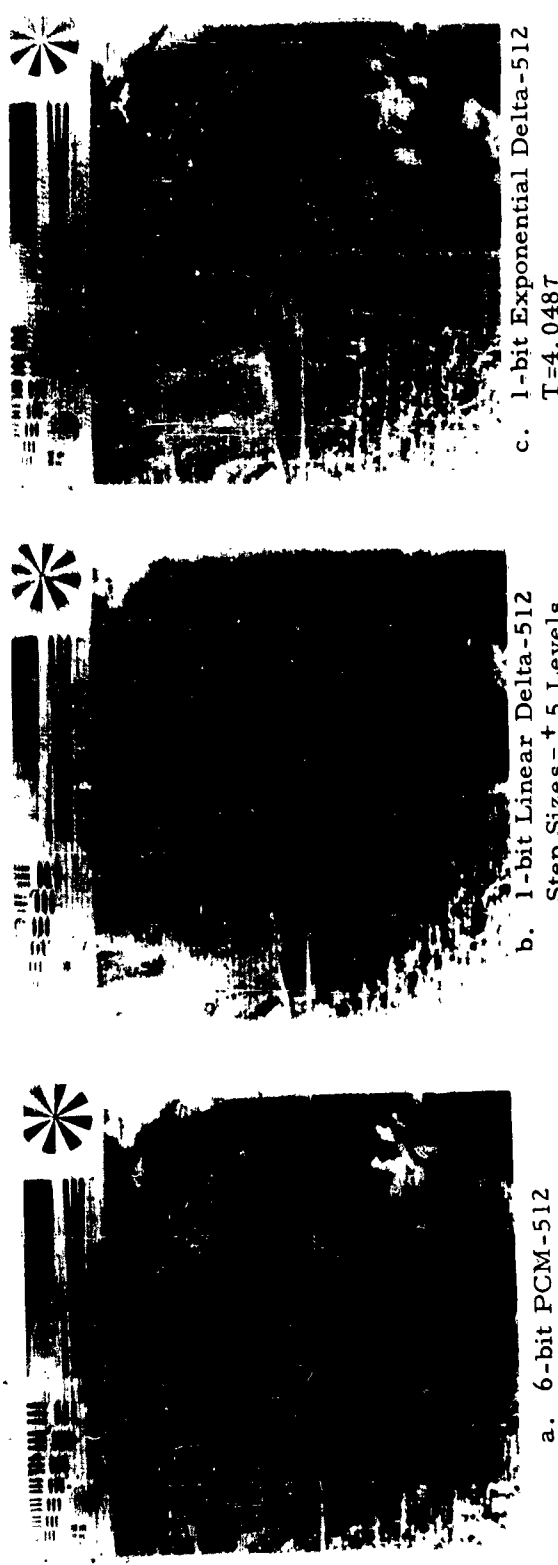


Figure 14 One-Bit Delta Modulation Systems Sampling at the Nyquist Interval



Figure 15 One-Bit Delta Modulation Systems Sampling at Twice the Nyquist Interval

played back through IMITAC to obtain a six-bit PCM copy of the input data. The output pictures obtained from that computer simulation could then be compared with this reference image to evaluate the system performance subjectively. This procedure eliminates small differences that may arise in IMITAC's performance from day to day because of variations in power supply and operating levels due to human error in adjusting the equipment.

TABLE 6
SAMPLING RATE VERSUS BIT RATE

	Sampling Rate	Bit Rate
1-bit	a	a
	2a	2a
2-bit	a	2a

2. Considerations Peculiar to Computer Simulation

In order to evaluate the results of these simulations, it is well to keep in mind several important properties peculiar to the simulation process as it is utilized for the Delta system. The video input signal to the computer program has been quantized into 64 levels and, consequently, is no longer an analog signal. Therefore, the standard to be used in subjective comparisons is a quantized six-bit PCM picture, the best picture that could be obtained from a six-bit PCM communication channel. The question to be asked is, "How well did the one- or two-bit digital Delta Modulation system, including the digital communication channel, perform as compared with straight six-bit PCM transmitted over a similar digital channel?" The answer to this question can be readily determined by comparing the output picture with the six-bit input picture to the computer program. Another consideration is the fact that the output video or integrator signal must be quantized into 64 levels to be acceptable to IMITAC for film print-out. In simulations involving exponential integration where output signal values have fractional parts, rounding-off to a whole number must be accomplished prior to putting the data on magnetic tape for playback through IMITAC. However, this property

is not a limitation of the simulation, since the presence of a fractional number indicates a precision of at least seven bits, one bit more than that in the input picture. It is doubtful that, subjectively, the eye can tell the difference between a six- and a seven-bit picture; as a matter of fact, it is difficult without close examination to differentiate between five- and six-bit PCM images.

The final consideration is the fact that computer processing of the input image data produces information only at the sample points. However, since the width of the pulse to be integrated is less than a sample period in the physical equipment, there will be a rise and decay during this period (see Figure 8). Since the program computes only sample point values, it acts as a smoothing filter on the output signal; a similar type process would be performed on the output of the physical system (decoder integrator).

D. Discussion of Results of the Simulations

1. One-Bit Systems

a. Single Linear Integration

The first Delta Modulation system simulated was the one-bit linear integration system with step sizes ± 5 levels using the 512-x-512-element raster. The standard used for evaluation purposes is the input six-bit PCM image scanned by a 512-x-512-element raster (Figure 14a). The resultant output image is shown in Figure 14b. The general softening and blurring of the image indicates that resolution has been lost. Also, contouring is evident in low detail areas, especially, in the water area in the upper right of the image. The loss of resolution or rise-time information is explained by the fact that it takes many samples to respond to a step input, whereas with PCM only one is required. Figure 16c graphically illustrates this fact for a large-amplitude step input and a one-bit step size of ± 5 levels. Larger step sizes would have produced better resolution but would have also markedly increased contouring which would be objectionable in low-detail regions. One other effect of large step sizes is the large-amplitude oscillation in uniform brightness areas. The amplitude of the oscillation equals the step size and has a frequency of one-half the sampling frequency. This effect is shown graphically in Figure 16c and in expanded areas taken from an output image processed by a one-bit linear integrator (Figure 17 (a and b)). The character of this oscillation does not vary throughout the dynamic range as it does for exponential integration systems to be discussed later. One way to increase resolution by a factor of two is to double the sampling rate. Figure 15a shows the results of the one-bit linear simulation using the same image input scanned with a 1024-x-512-element raster where the step sizes were maintained at ± 5 levels. The improvement gained is immediately obvious, especially in the city areas where buildings appear sharper. However, contouring has not been materially reduced and in some areas appears to be enhanced, simply because the smearing effect of low resolution has disappeared somewhat. It should be kept in mind, also, that the bit rate has been doubled to achieve this better resolution and thus caused an attendant increase in equipment complexity. Figure 18c illustrates graphically the 100-Mb one-bit system corresponding to a simulation using the 1024-x-512-element raster. Notice that only approximately 110 ns are required to produce the band-limited 25-Mc step input, whereas for the 50-Mb system (512-x-512-element raster) approximately 220 ns are required (see Figure 16c).

b. Double Linear Integration with Prediction (DIWP)

Several of the limitations inherent with single linear integration can be eliminated by cascading two linear integrators together and providing a prediction feature. Contouring can be reduced without the attendant

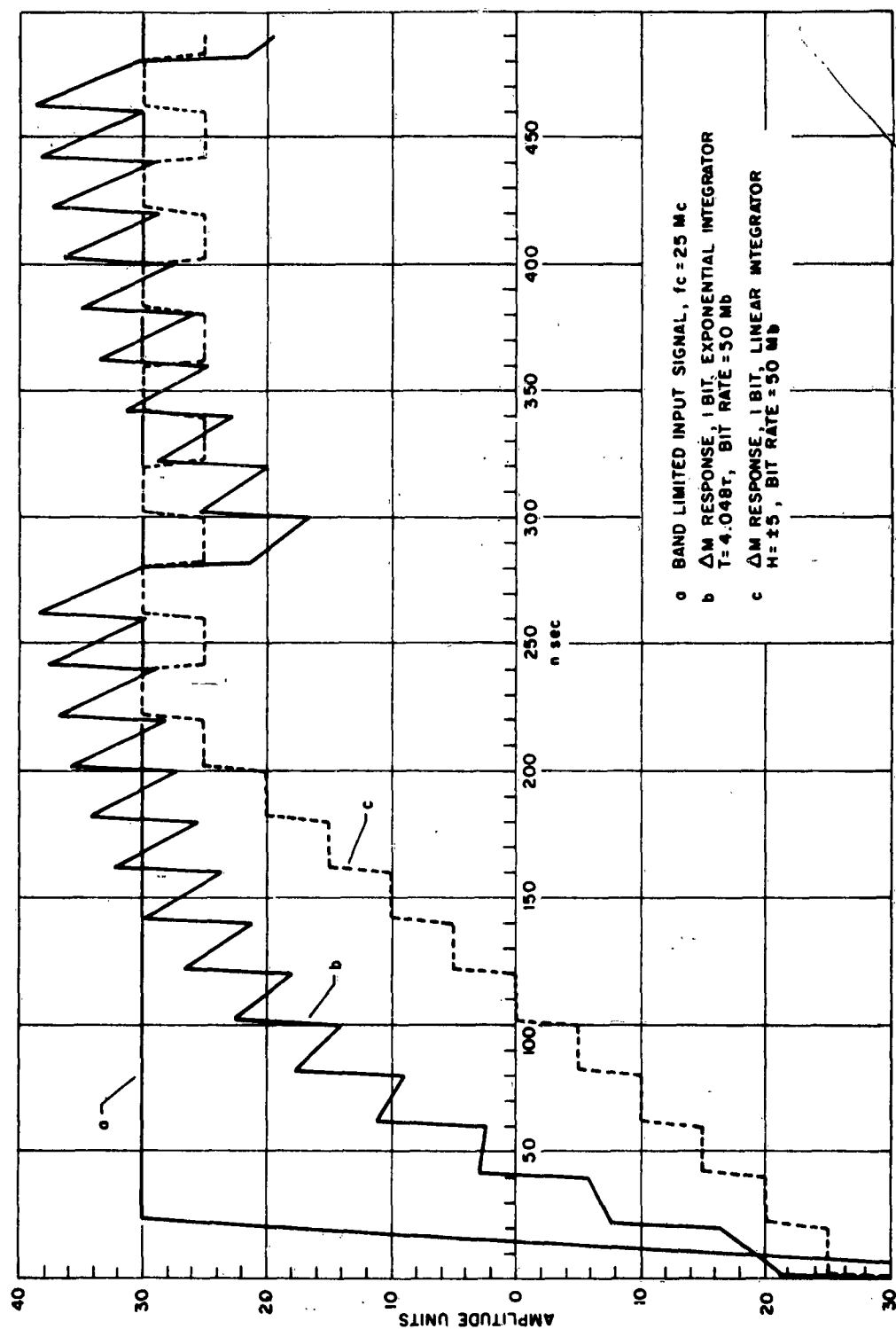
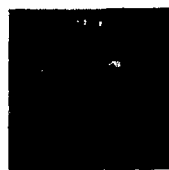


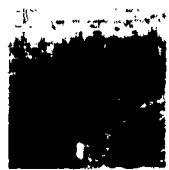
Figure 16. Comparison of One-Bit Delta Modulation Systems



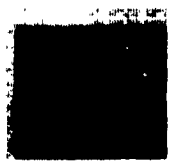
a. Midpoint Area
1-bit Linear
Delta-512



b. Black Area
1-bit Linear
Delta-512



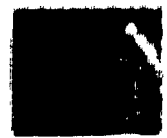
c. Midpoint Area
1-bit Exponential
Delta-512



d. Black Area
1-bit Exponential
Delta-512



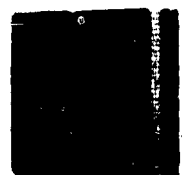
e. Midpoint Area
1-bit Exponential
Delta-1024



f. Black Area
1-bit Exponential
Delta-1024



g. Metropolitan Area
2-bit Exponential
Delta-512 T=1.7877



h. Black Area
2-bit Exponential
Delta-512 T=37

Figure 17 Expanded Areas Taken from Results of the Simulations

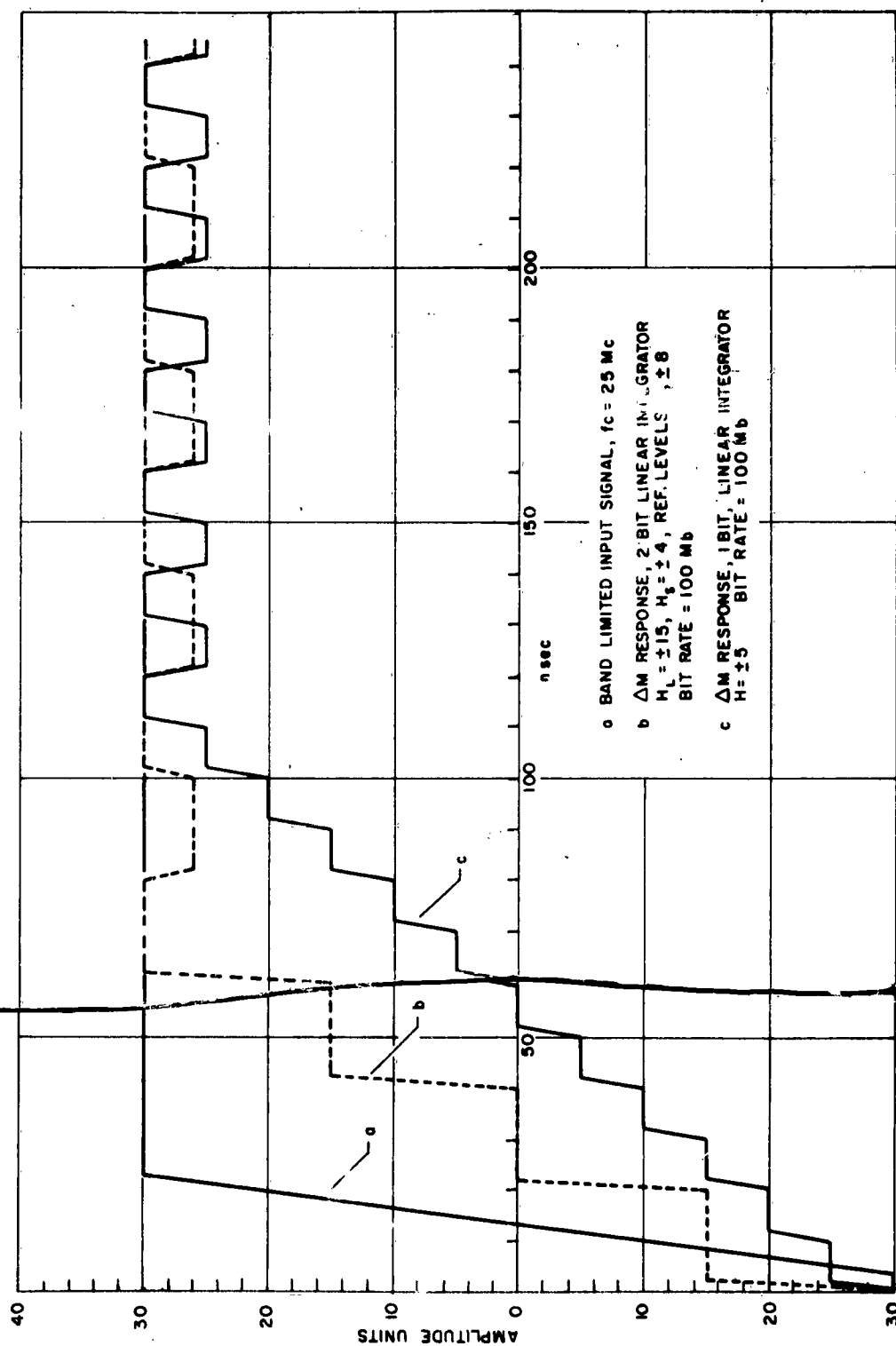


Figure 18. Comparison of Two-Bit and One-Bit Delta Modulation Systems with Equal Bit Rates

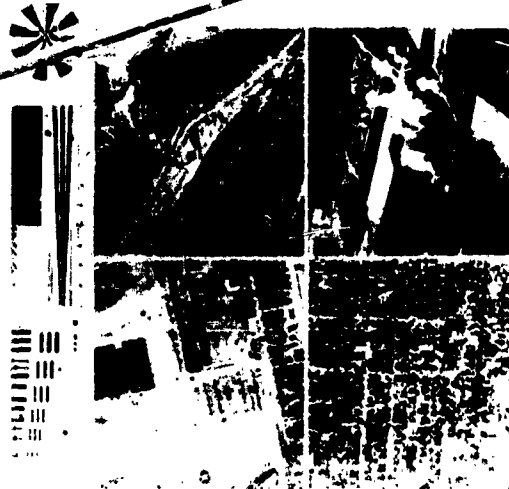
loss of resolution or smearing of the output image. Work on this particular simulation proceeded during the second phase of this contract. Therefore, it is reported on in more detail than those simulations that were accomplished during the first phase. The series of output images resulting from the DIWP simulation are shown in Figure 19. Figure 19a is the input image to the DIWP program scanned with a 1024-x-512-element raster. This discussion will proceed in terms of the basic image coding parameters of interest.

(1) Sampling Rate

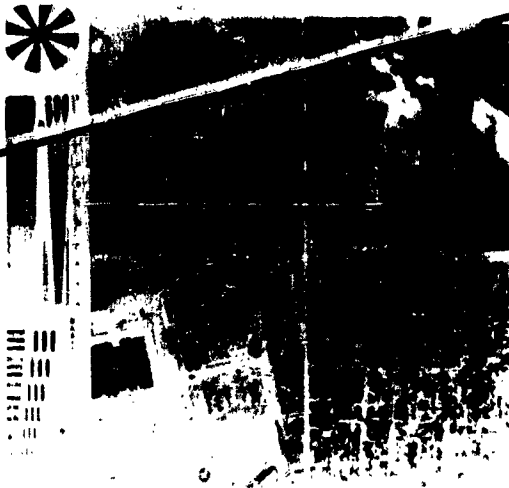
Previous discussions in the literature concerning DIWP have assumed a high sampling rate as compared to the input signal bandwidth. This is particularly true for speech compression systems using Delta Modulation.² However, for digital pictorial transmission, high sampling rates generally are prohibitive because of the high bit rates that are involved. Consequently, an attempt has been made to sample the input signal at twice the Nyquist interval (reciprocal of twice the information bandwidth) in this simulation to determine if acceptable DIWP system parameters could be found by computer simulation. In DIWP, the presence of a low sampling rate and excessive overshooting combine to cause loss of high-frequency detail because the sign of the slope of the output signal cannot change instantaneously. When the output overshoots the input with a high value of its first derivative, it takes a definite number of samples for the derivative to change its sign and cross back over the input. The minimum number of samples required is two, since the first derivative must go through zero to give zero slope (horizontal line). For single integration, the minimum number is one sample. This process of passing through zero slope when reversing the sign of the derivative is shown in Figure 20a. It can be seen that the minimum time interval for the output to reverse itself when it is oscillating about the input is $2T$, where T is the sampling interval. Any signal information which is changing faster than this is lost in the encoding process. The character of this phenomenon is dependent upon the slope of the output when it crosses the input. The greater the absolute value of the slope, the more samples are required to respond to the change. Figure 21 presents three examples of DIWP systems for various sampling rates. For the lowest rate, the notch in the input is practically entirely lost. As the rate is increased, the output follows the input much more closely. Curve (a) might represent an acceptable system. However, for a 25-Mc input, obtaining a sampling rate of $1/4$ of the Nyquist interval, or 5 nanoseconds, becomes a serious problem in circuit implementation. For full amplitude changes occurring in the Nyquist interval, many more samples per interval would be required. The number would depend upon the number of changes in slope required to traverse the full dynamic range and, consequently, upon the initial slope and prediction interval. From the foregoing, it is clear there would be no advantage in using as an input to DIWP program an image scanned with a 512-x-512-element raster.



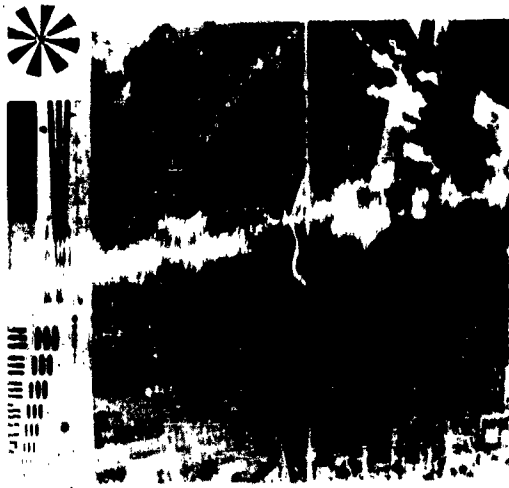
a. 6-bit PCM-1024



b. 1-bit DIWP Delta-1024
S=4 Levels P=17



c. 1-bit DIWP Delta-1024
S=4 Levels P=27



d. 1-bit DIWP Delta-1024
S=4 Levels P=7

e. 1-bit DIWP Delta-1024
S=3 Levels P=27

Figure 19 One-Bit Double Integration with Prediction Delta Modulation Systems

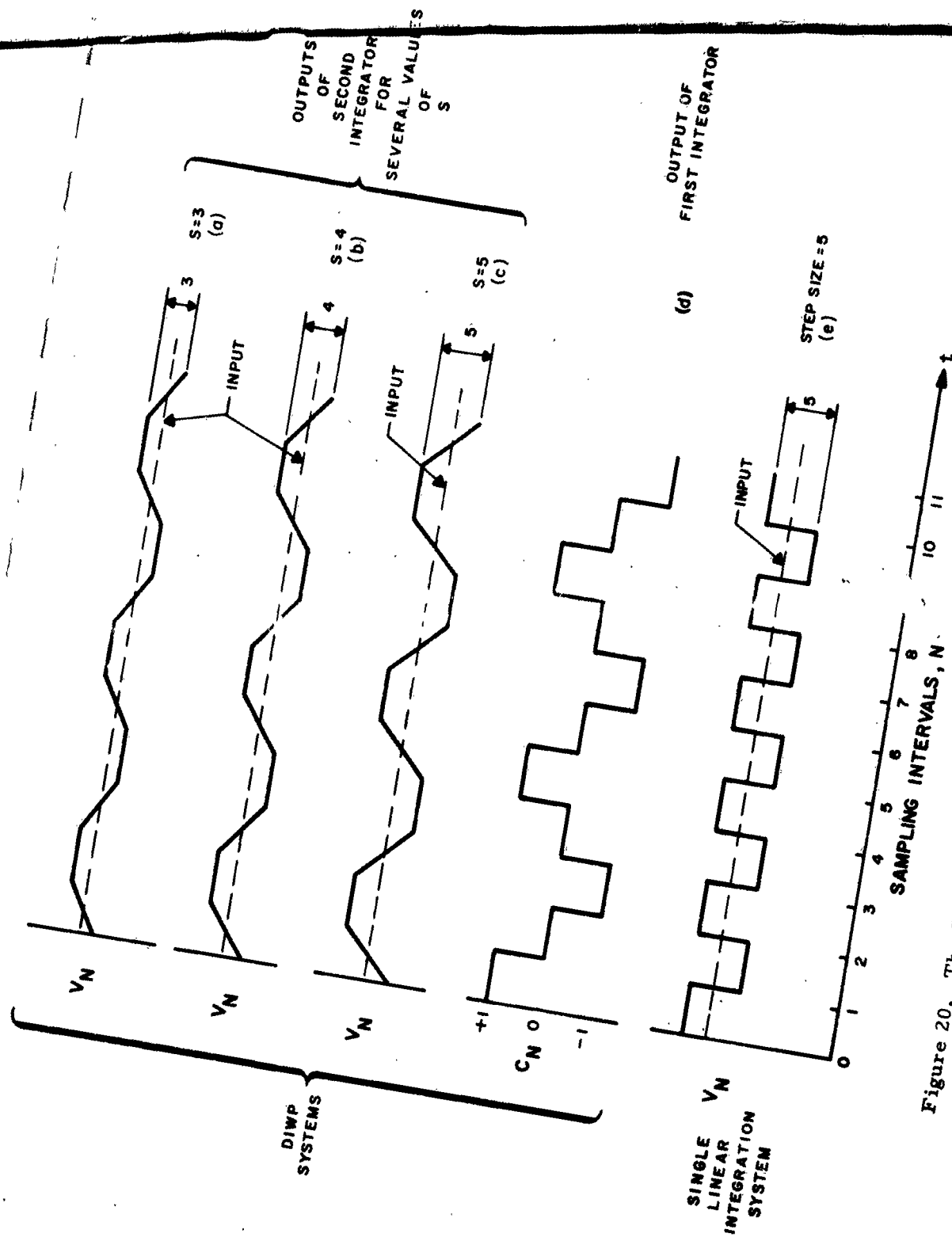


Figure 20. The DC Response of the One-Bit LIWP Delta Modulation System for Various Values of S , the Initial Slope

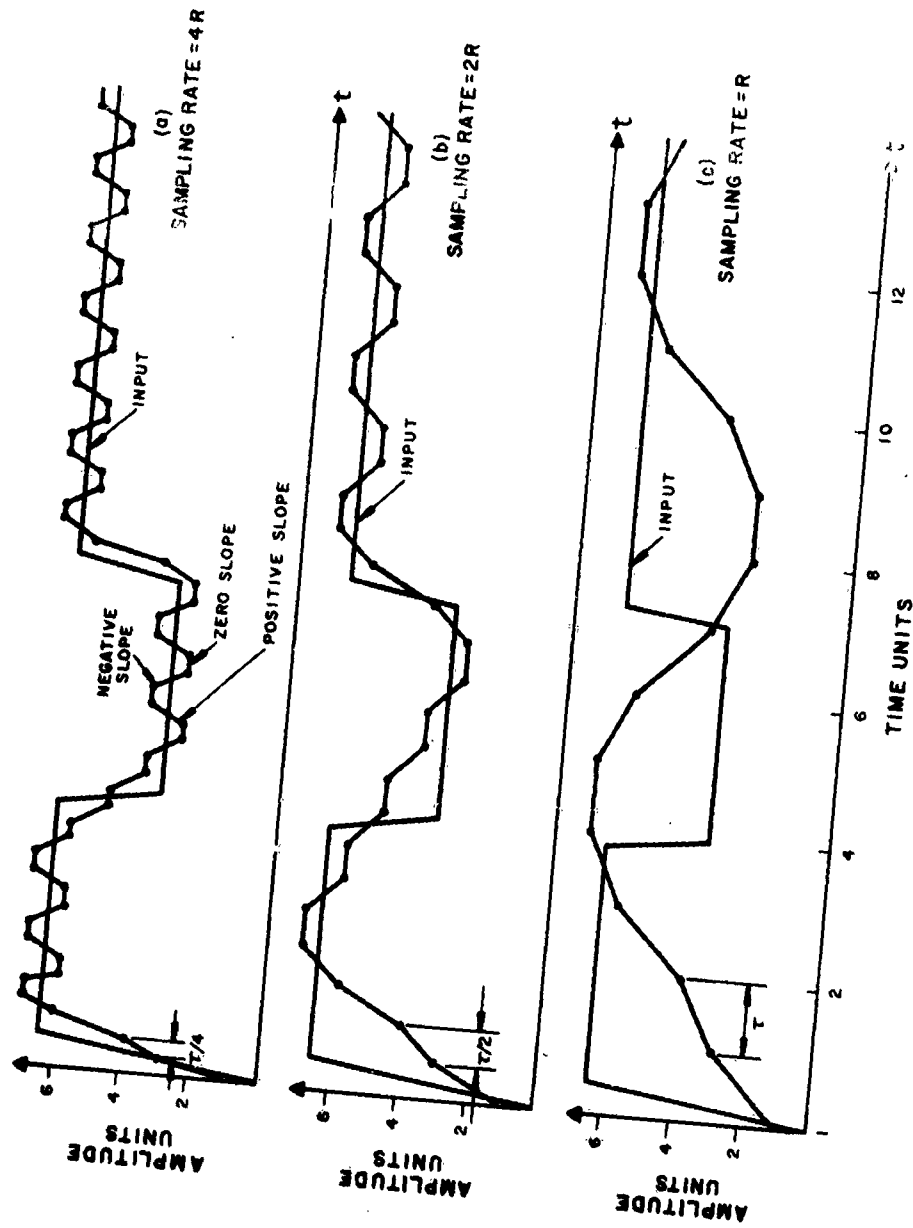


Figure 21 Response of DIWP System for Various Sampling Rates
(System Characteristics: $S=1$, $P=2\tau$)

(2) Contouring

The contouring associated with one-bit DIWP is directly related to the initial slope, S , which is provided by the second integrator in the feedback loop when the count number C_n is plus or minus 1. This is true because all other slopes are whole number multiples of S . This initial slope is specified as the number of amplitude units rise in one sampling interval. A count number, C_n , of +2 provides a contribution of +2 S to the output. In general, it is possible to predict the contouring associated with any particular initial slope from the following equation:

$$N_L = \frac{\text{Dynamic Range (amplitude units)}}{S \text{ (amplitude units)}}$$

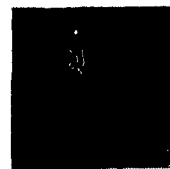
where N_L = number of levels that can be reproduced. These N_L levels are separated from each other by the value of S . As an example, if we have a dynamic range of 64 levels and our initial slope is four levels, N_L becomes 16 and this particular DIWP system would have contouring associated with a four-bit PCM system. Obviously, the smaller the value of S , the less contouring we have. Also, a low-pass filter on the output of the decoder in a practical system implementation would reduce this contouring.

Output images (b), (c), and (d) of Figure 19 were obtained for a system having an initial slope of four levels. Notice that the contouring in all three images is very similar. This can be seen by viewing the water area in the upper right square of each image. As pointed out previously, the contouring associated with these DIWP images for an initial slope of four levels when the input is six-bit PCM is approximately equivalent to $64/4 = 16$ levels or four-bit PCM. Image (c) of Figure 12 is a four-bit PCM representation of the input.

Figure 19e is an output image obtained for an initial slope of three levels. Here the associated contouring is considerably improved over that for $S = 4$ levels. However, contouring is still evident, being approximately equivalent to that associated with $64/3 = 21.3$ levels, or between four- and five-bit PCM. Image (b) of Figure 12 is a five-bit PCM representation of the input. Figure 22 (a and b) presents two expanded areas for $S = 3$ and $S = 4$ levels, showing the difference in contouring associated with these initial slopes.

(3) DC Response

The value of the initial slope also determines the amplitude of oscillation about constant brightness areas of the input image. Several examples of this oscillation have been plotted for various values of



a. Pin Wheel
Area
S=4 Levels
P=17



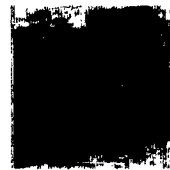
e. Pin Wheel
Area
S=4 Levels
P=17



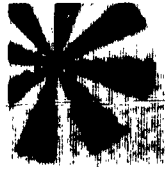
b. Metropolitan
Area
S=3 Levels
P=17



f. Metropolitan
Area
S=4 Levels
P=17



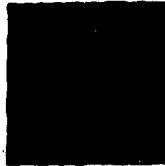
c. Pin Wheel
Area
S=4 Levels
P=27



g. Pin Wheel
Area
S=4 Levels
P=27



d. Metropolitan
Area
S=3 Levels
P=27



h. Metropolitan
Area
S=4 Levels
P=27



i. Horizontal
Resolution
Bar Area
S=3 Levels
P=27



j. Horizontal
Resolution
Bar Area
S=3 Levels
P=27



k. Horizontal
Resolution
Bar Area
S=3 Levels
P=27



l. Horizontal
Resolution
Bar Area
S=3 Levels
P=27

Figure 22 Expanded Areas Taken from the Results of the One-Bit DIWP System Simulations

initial slope in Figure 20. The amplitude of oscillation is equal to the value of S for one-bit DIWP. Curve (e) of this figure shows the response of a one-bit single integration system with a step size of ± 5 levels. A comparison of this curve with curves (a), (b), and (c) shows that the frequency of oscillation for the DIWP systems is one-half that for a single linear integration Delta Modulator. This is brought about by the fact that the second integrator must produce zero slope before the output can reverse itself after a rise or fall. Curve (d) shows the sequence of count numbers required to produce oscillation about constant brightness areas. This lower frequency of oscillation for DIWP systems may be objectionable upon subjective analysis of the output image if the input pulse rate or sampling rate is too low. A compromise must be made between high sampling rate, or bit rate, and the initial slope to make the oscillation acceptable. All of the output images generated by the DIWP program show evidence of dc oscillation, as can be seen in two expanded areas shown in Figure 22 (c and d).

(4) Rise Time Response

One important advantage gained by a one-bit DIWP system is its improved rise time response as compared with one-bit single linear Delta Modulators. Figure 23 indicates the rise time response of several different Delta Modulation systems for a square-wave input, curve (f). The ideal response of a single linear integrator with a step size of I is shown in curve (a). Seven samples, or a period of $7T$, are required for the output curve (a) to reach the input curve (f). Such Delta systems are consequently slope limited by the size of I . In comparison, three DIWP systems are plotted for various values of the initial slope, S . Notice that larger values of S produce faster rise time responses. For $S = I$, approximately $3.5T$ is required for the output to cross the input, a system which is two to one better for this input than the single-integration system. Both systems would have the same amplitude of oscillation about dc. The DIWP system requires much shorter times to respond to fast high-amplitude transitions because the slope of the output is changing by ever increasing amounts rather than the amplitude by a constant amount as for the linear system. Also shown for comparison purposes on the figure is curve (e), the response of a one-bit exponential integration system with a time constant $T = 3T$. This system responds slightly better than the DIWP for inputs whose amplitudes are equal to or smaller than curve (f). However, the oscillation about dc is not of a constant amplitude but depends upon the amplitude of the input, being the largest at the extremes of the encoding range (approximately equal to $3I$).

Although the prediction interval also has an effect upon the rise time response, the initial speed with which the system attempts to respond to a single large amplitude change of the input is independent of

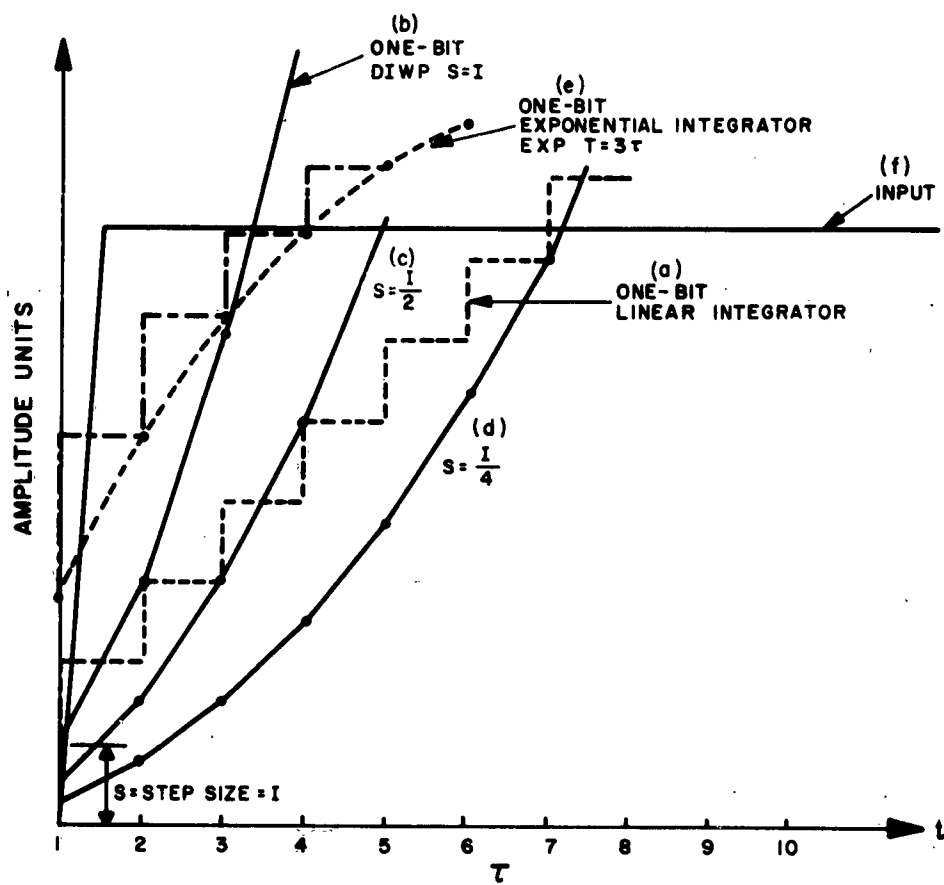


Figure 23. Rise Time Response of Several Delta Modulation Systems

this interval and determines the sharpness or crispness of this change as viewed by the eye. It is expected, therefore, that the system with the larger initial slope would produce the "sharper" image. This fact is borne out by a close inspection of the images of Figures 19 (c) and 21 (e) where the prediction interval for both is two sample periods. The image for $S = 4$ levels is generally crisper and sharper than that for $S = 3$ levels. However, because of overshooting and a low sampling rate, the good rise time response inherent in the double-integration process is diminished, as discussed later.

(5) Overshooting and Prediction

As mentioned previously, DIWP systems are accompanied by large amounts of overshooting caused by the high value of the signal's first derivative as it crosses the input signal. This overshooting may be markedly decreased by extrapolating the output signal to a point at some later time interval, assuming the present slope is maintained; this predicted value is then compared with the input signal. The longer the time or prediction interval, the smaller the value of the first derivative of the output as it reaches the value of the input. The amplitude and period of the overshoot is then made smaller. Figure 24 illustrates the effects of the prediction interval upon the overshoot for a step function input. Curve (a) indicates that, for this particular input and a prediction of 1τ , the overshoot is excessive, being a maximum about 38% of the input amplitude. Lengthening the interval to 3τ produces minimum overshoot but with an excessive loss of resolution or rise-time response, as evidenced by curve (c). The optimum prediction interval for this input waveform is shown in curve (b) for $P = 2 \tau$. Here a compromise has been made between rise-time response and oscillation to produce minimum overshoot. The minimum overshoot and undershoot are determined by the initial slope S as discussed earlier. Notice that after many samples, (11 for this example) the outputs are identical for all three systems, being independent of the prediction interval.

The effects of excessive overshooting are demonstrated very well by Figure 19b for $S = 4$ levels and $P = 1 \tau$. The pinwheel on the test chart shows a darkening of the leading edges, indicating that the output, in going from white to gray, went beyond the gray to black. Also it is evident that after overshooting to black and attempting to come back to the right gray level, the output went beyond this level toward the white extreme. An expanded pin wheel is shown in Figure 22e. Measurements of this area indicate that approximately 12 sample periods were required for the output to settle down finally to the proper gray level. It is clear that this excessive overshooting has distorted the output image and brought about an unacceptable loss of resolution in high-detail areas. An expanded metropolitan area is shown in Figure 22f.

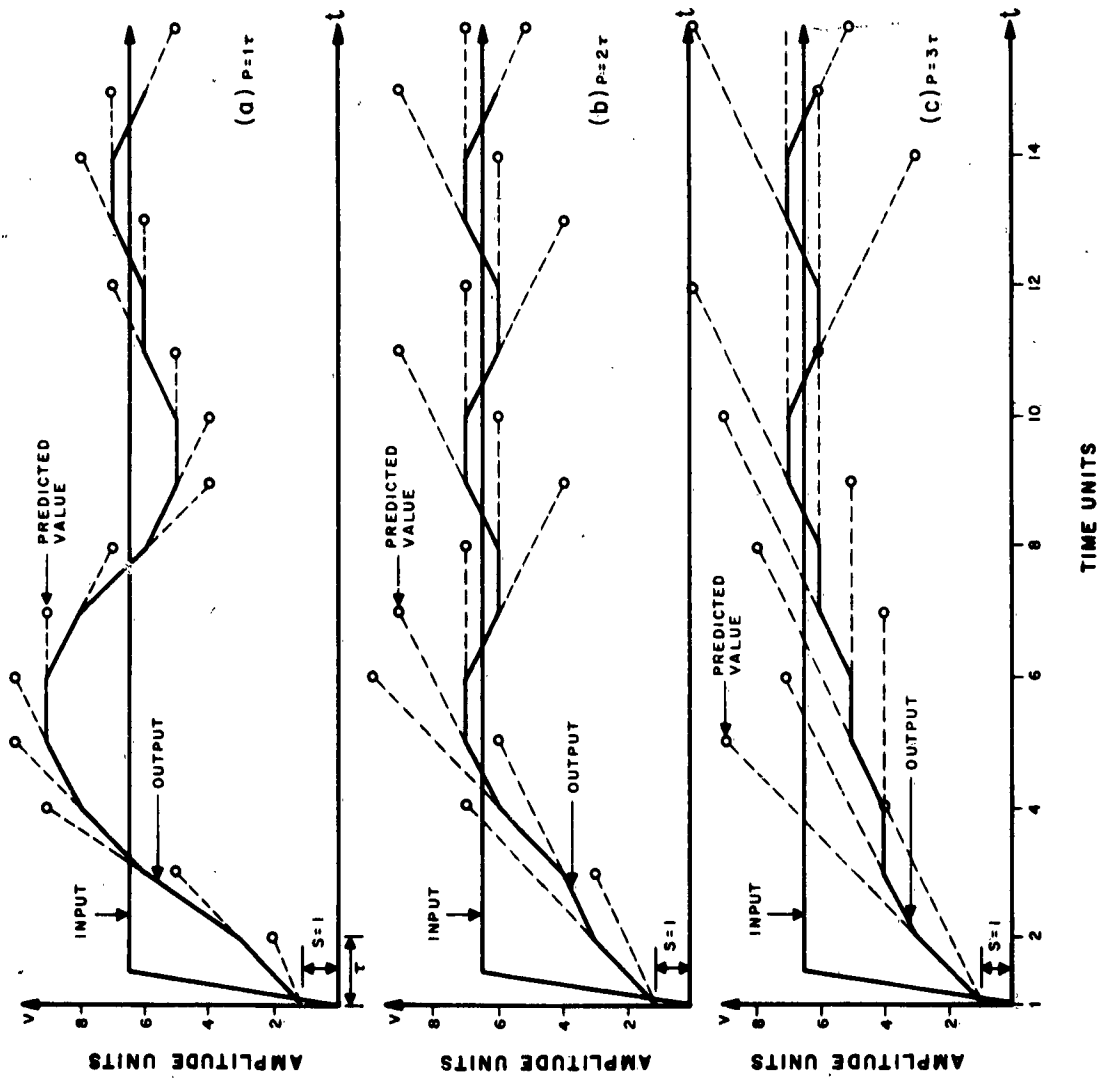


Figure 24. Response of the DIWP System to a Step Input for Various Values of Prediction Interval

Lengthening the prediction interval to two sample periods considerably decreases this overshooting, as can be shown by Figure 19c. Expanded pinwheel and metropolitan areas are shown in Figure 22 (g and h). No overshooting is noticeable in the pinwheel and there is an increase in high-frequency detail. These same expanded areas, taken from the input image, are shown in Figure 22 (i and j). The effect of a further increase in the prediction interval to three sample periods is shown in Figure 19d. A careful scrutiny of this image and that for $P = 2T$, indicates that the increase of P has caused a slight smearing effect, or loss of resolution, as graphically demonstrated by curve (c) of Figure 24.

The loss of resolution caused by overshooting and low sampling rates is dramatically illustrated by all of the output images generated by the one-bit DIWP program. The vertical bars in the upper left-hand part of the test chart area in the images show evidence of (1) "drop out" where some bars are missed completely and (2) nonuniform gray-scale representation; an expanded area of these bars taken from Figure 19e is shown in Figure 22k. In Figure 22l the bars are shown as they appear in the input image. These horizontal resolution bars present a severe test of the double-integration logic. High-frequency changes of near-maximum amplitude are presented to the system. The loss of resolution is caused by the low sampling rate as compared with the information rate and the long recovery time of the double integrator due to overshooting. Figure 25 is a graphical plot of the input and output waveforms, actually taken from this bar area. The input and output tapes containing the data in binary form were printed out on paper by the Philco High-Speed Printer. These values were converted from binary to decimal form so that they could be plotted. The "drop out" areas are clearly visible from this plot. Also, it is evident that the gray-scale level of the reproduced waveform is not correct in most instances.

(6) Error Signal Image Analysis

Incorporated in the one-bit DIWP program was a subroutine for generating an error signal image for printout on film by IMITAC. This error signal is the difference between the input and output signals. The group of error signal images generated is shown in Figure 26. If the encoding logic were perfect, the error signal would be zero for the entire image, and the error signal image would be blank or uniformly gray. Errors in encoding show up as whiter and darker areas in these images. In general, the more information there is in the error signal image the poorer the system is for image coding.

It appears from Figure 26 that image (b) contains less information than the other images shown. Image (a), for $S = 4$ levels and

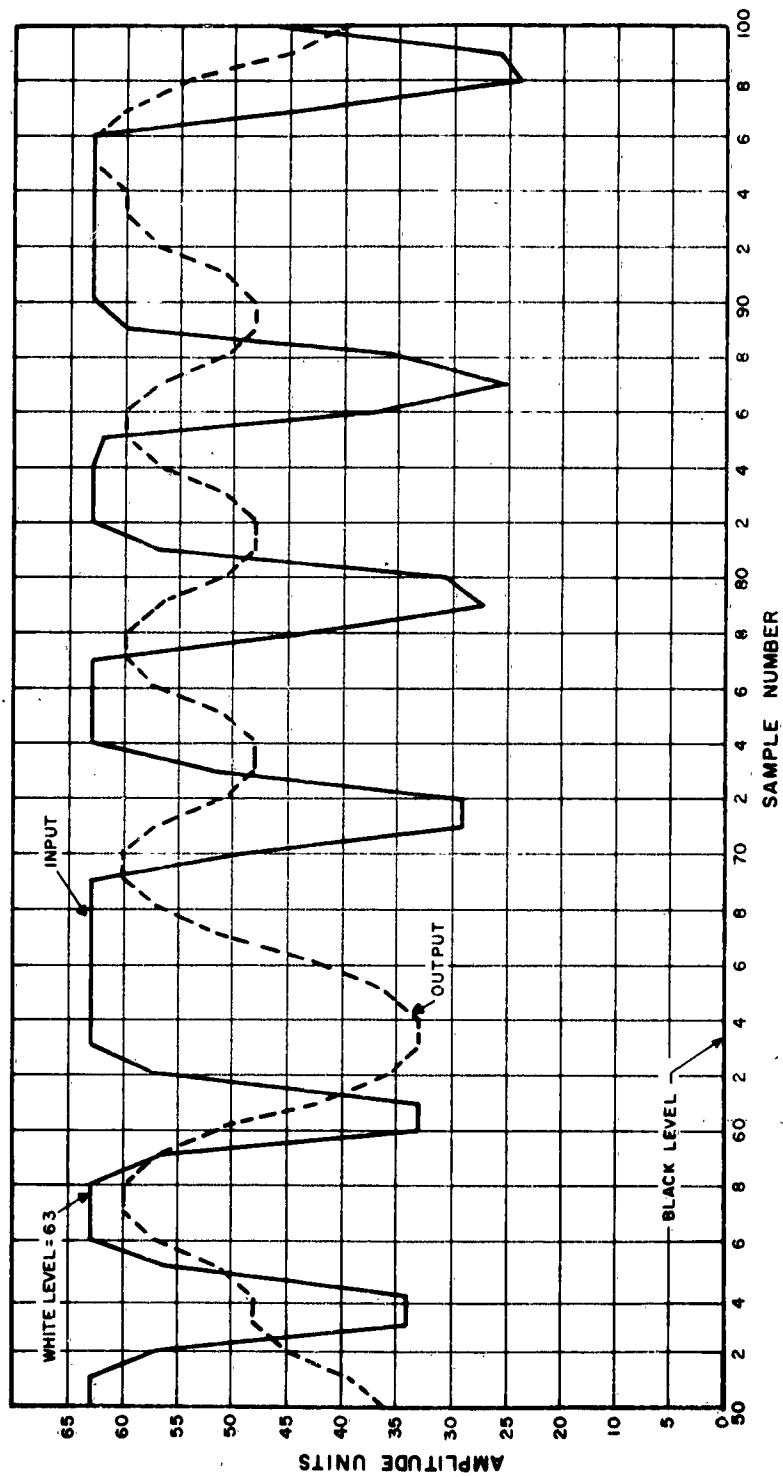
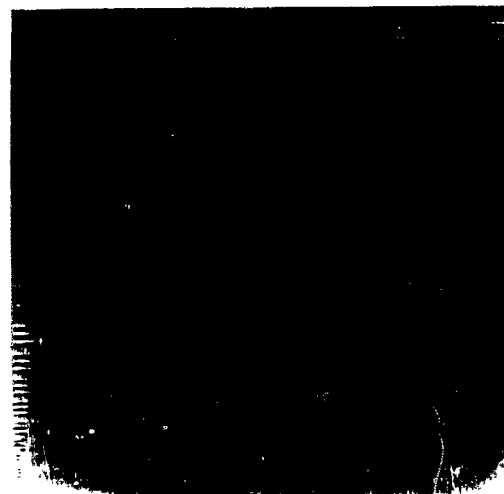


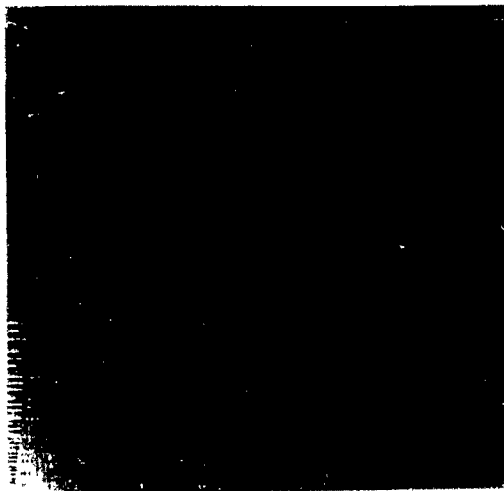
Figure 25 Input and Output of the DIWP Program for $S = 3$ Levels,
 $P = 2\tau$, Scan Line No. 9



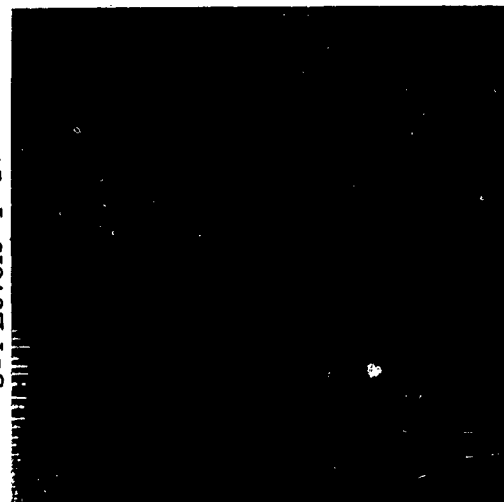
a. 1-bit DIWP Delta-1024
S=4 Levels P=17



b. 1-bit DIWP Delta-1024
S=4 Levels P=27



c. 1-bit DIWP Delta-1024
S=4 Levels P=37



d. 1-bit DIWP Delta-1024
S=3 Levels P=27

Figure 26 Error Signal Images for One-Bit DIWP Delta Modulation Systems

$P = 1 \tau$, demonstrates the effects of excessive overshoot and loss of resolution. Notice the broad areas of error in the pinwheel and the large errors in the city areas. A comparison of the vertical resolution bars in the upper left-hand corner indicates that in all images there are large errors in this area. In general, DIWP systems suffer from a loss of resolution when the sampling rates are low compared with the input information rate. Again, it is evident that image (b), for $S = 4$ levels and $P = 2 \tau$, has less error in this bar area. The errors involved in overshooting and undershooting are shown in the horizontal bars in the same area in these images. These errors exist as dots at the beginning and end of the bars. At the beginning the dots are black because the input is going from near-white to gray. At the end of the bars the dots are white because the input is going from gray to near-white. The width of the dots in the direction of scan gives an indication of the amount of recovery time required by the system after overshooting a dc level.

(7) Output Signal-to-Noise Ratios

The one-bit DIWP program, as explained in Appendix I, calculated mean-square error and mean-square input signal values so that S/N ratios could be determined for the various sets of parameters. Table 7 presents these values.

TABLE 7
MEASURED OUTPUT S/N RATIOS
FOR ONE-BIT DIWP SYSTEMS

Parameters	S/N (db)
$S = 4$ levels, $P = 1 \tau$	8.2
$S = 4$ levels, $P = 2 \tau$	11.1
$S = 4$ levels, $P = 3 \tau$	11.3
$S = 3$ levels, $P = 2 \tau$	10.0

It is apparent that the system for $S = 4$ levels and $P = 2 \tau$, giving the most acceptable output image for the DIWP system studied, does not have the largest measured S/N. This points out the fact that measured statistics, in themselves, cannot be the only criterion for picking the best encoding logic; however, trends are often indicated. It is not surprising that the system for $S = 4$ levels and $P = 1 \tau$ has given the lowest S/N; it is the poorest for pictorial encoding because of excessive overshooting.

(8) Amplitude Distributions

During the second phase of this contract, some statistical data concerning amplitude distributions of the various signals involved with the one-bit DIWP system were determined. The number of signals of specific amplitudes were calculated by the computer and printed out by the high-speed printer. For a six-bit PCM image, there are 64 different signal amplitudes (0 through 63) possible. The input image contained a predominance of signal levels near the upper extreme, that is, from level 42 to level 63 (white areas in the photographs presented in this report). Another image used as input data might have an entirely different distribution. It is helpful to know what the distribution is so that the output distribution may be compared with it.

An output signal amplitude distribution is plotted in Figure 27 for $S = 4$ levels and $P = 2\tau$. This distribution reflects the fact that the input image was predominantly white, as can be seen by the ever increasing number of signals near the upper extreme. Also shown is the contouring produced by the initial slope of four levels. As pointed out earlier, this system produces contouring equivalent to four-bit PCM where 16 levels are possible. Notice in Figure 27 that there are 16 predominant signal values. Associated with each possible signal value is its neighbor occurring with much less frequency. These adjacent values are caused by limiting which was put in the program to prevent the output signal values from exceeding level 63. At the beginning of each scan line, the integrator is reset to level 32, one-half the dynamic range. Since each output signal level is separated by the value of the initial slope, values of 36, 40, 44, 48, 52, 56, 60, and 64 would be possible. However, level 64 is outside of the dynamic range and would be limited to level 63. Now values of 59, 55, 51, 47, 43, 39, 35, 31, etc., are possible. Because of the predominance of "white" information in the input these odd-numbered values predominate.

Figure 28 shows the error signal amplitude distribution for $S = 4$ levels and $P = 2\tau$. Only those error signals occurring with significant frequency were plotted. Notice that the curve is sharply peaked at zero error, a desirable condition. Some of these zero errors were caused by the predominance of level 63 in the input and the limiting required to contain the output to level 63. Although not shown, the other two curves for $S = 4$ levels and $P = 1\tau$ and 3τ are quite similar in shape. The error signal distribution for $S = 3$ levels and $P = 2\tau$ is shown in Figure 29. This curve is more sharply peaked than the others. This fact might lead one to the conclusion that this system would be superior to those for $S = 4$ levels. However, a subjective analysis of the images obtained from these systems tells a different story. The large number of zero errors is due to the fact that level 63 is a possible value for this system without limiting. Since the input also contains a large number of this level, it is not surprising that there are many zero errors.

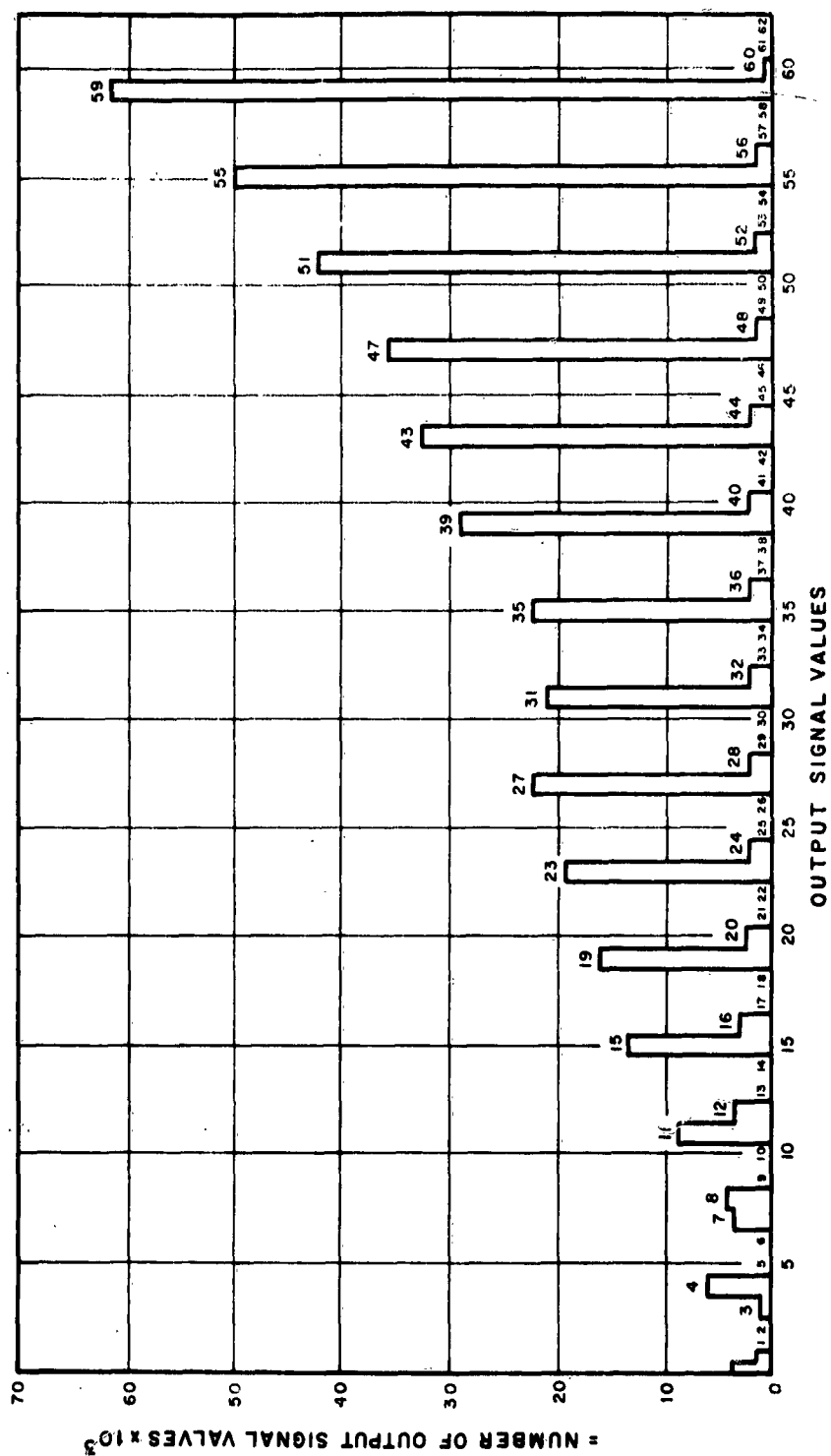


Figure 27. Output Signal Amplitude Distribution for $S = 4$ Levels
 $P = 2$

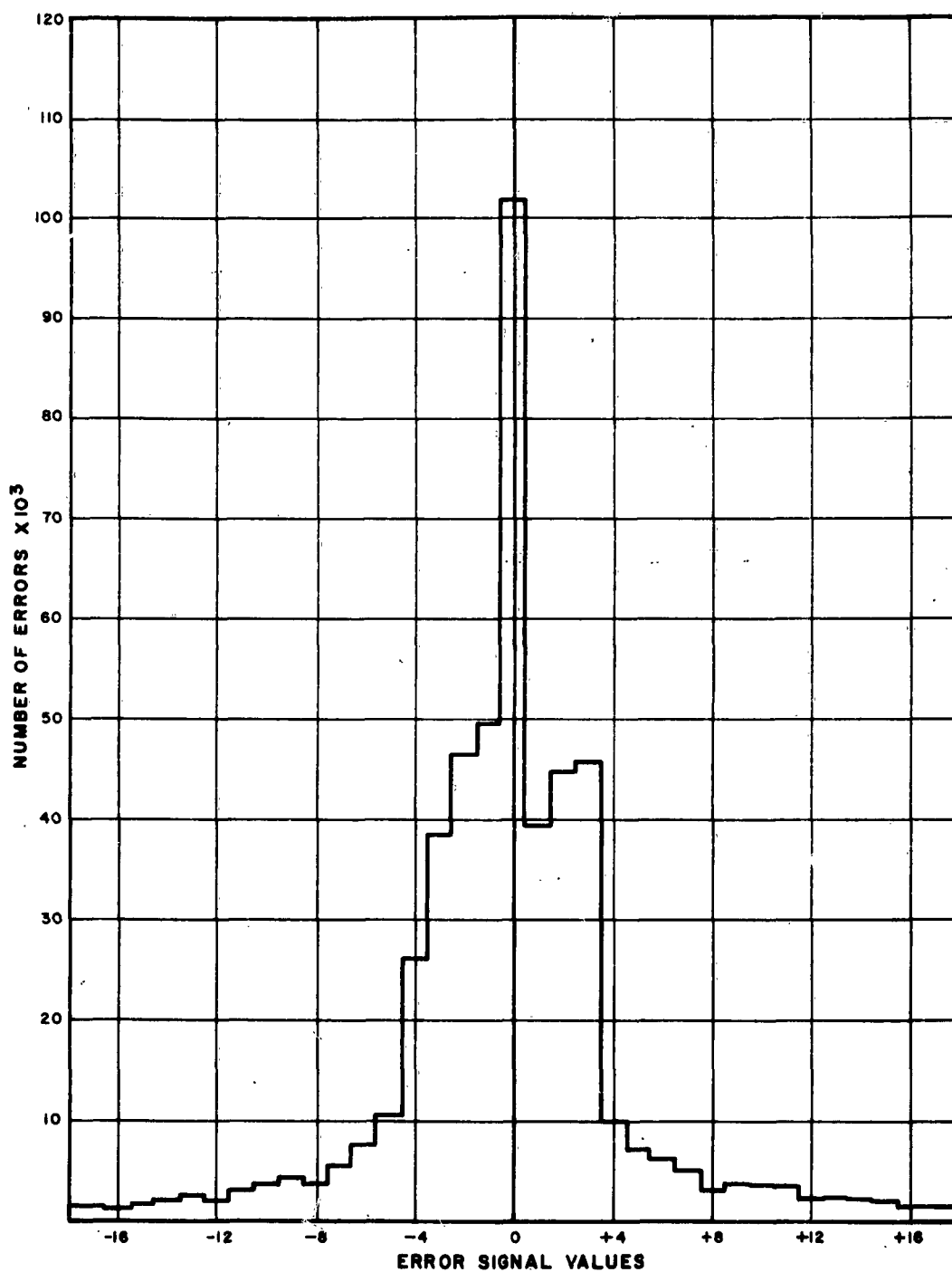


Figure 28. Error Signal Amplitude Distribution for $S = 4$ Levels,
 $P = 2 \tau$

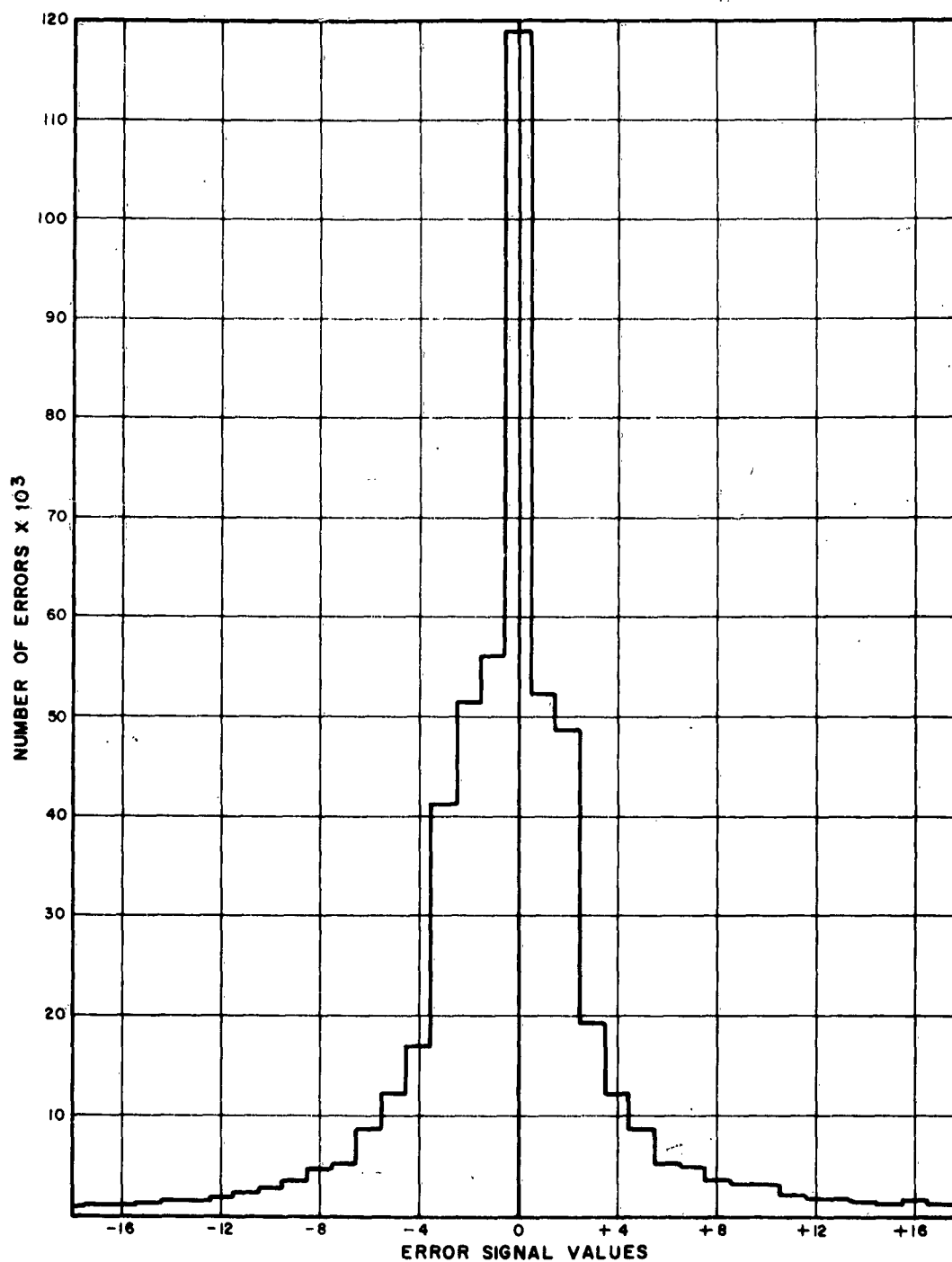


Figure 29. Error Signal Amplitude Distribution for $S = 3$ Levels,
 $P = 2\tau$

c. One-Bit Exponential Integration

Several advantages can be obtained by using an integrator with a limited time constant. Contouring is reduced because the number of reproducible levels is practically continuous. The exponential integrator makes use of the probability characteristics of images by using step sizes that are proportional to the probability of occurrence. As an example, when reproducing an increasingly lighter gray level, there is a progressively smaller chance that the next sample will be lighter than the previous sample.

The integrator parameters of interest for the simulations are the time constant, pulse height, and bit rate. The pulse width was held constant at 0.1 times the sample period. Varying this width does not appreciably affect the performance of the system with regard to image degradation. Its primary effect is to vary the maximum value of the output signal obtainable from the integrator and therefore the feedback gain requirements. Pulse heights were chosen to be those values which would give the desired contribution to the output of the integrator at the midpoint of the dynamic range of the input signal to the system. Various values of time constant were evaluated in order to select an optimum value consistent with good rise time response and small oscillation about dc. A result of exponential integration is the pronounced effect of the oscillation inherent in all Delta Modulation systems when adjacent samples of the image have the same brightness value. At the midpoint of the dynamic range these oscillations are similar to those produced in linear integration systems, being approximately equal to the pulse or step height with a period equal to one-half the sampling period. Figure 30 shows a graphical plot of oscillations for several different Delta Modulation systems. An excellent example of this oscillation may be found in Figure 17c. An area was taken from Figure 14c, the output image from a one-bit exponential integration system with $T = 4.048 \tau$ and $H = \pm 7.0$ levels, and expanded. The parameter H (Equation 17) is the contribution added to the output of the integrator from an input pulse when the integrator has been charged up to a voltage near the midpoint of the dynamic range. As the dc level moves away from the midpoint, these oscillations become larger in amplitude and have a longer period. The graphical plot of Figure 16b shows that the amplitude of oscillation has increased to approximately twice its value at the midpoint with a period of 9τ for an input signal near one extreme of the dynamic range. An example of this effect is shown in an expanded section of a black region from the same image in Figure 17d. Doubling the bit rate makes these oscillations less objectionable on a subjective basis because the period between oscillations has been halved. Figure 15c shows the output image processed with the same set of parameters used for the one-bit exponential previously mentioned, except that the bit rate has been doubled. Expanded portions of this image are shown in Figure 17, (e and f), where (e) is an area around the midpoint and (f) is an area near one extreme (black).

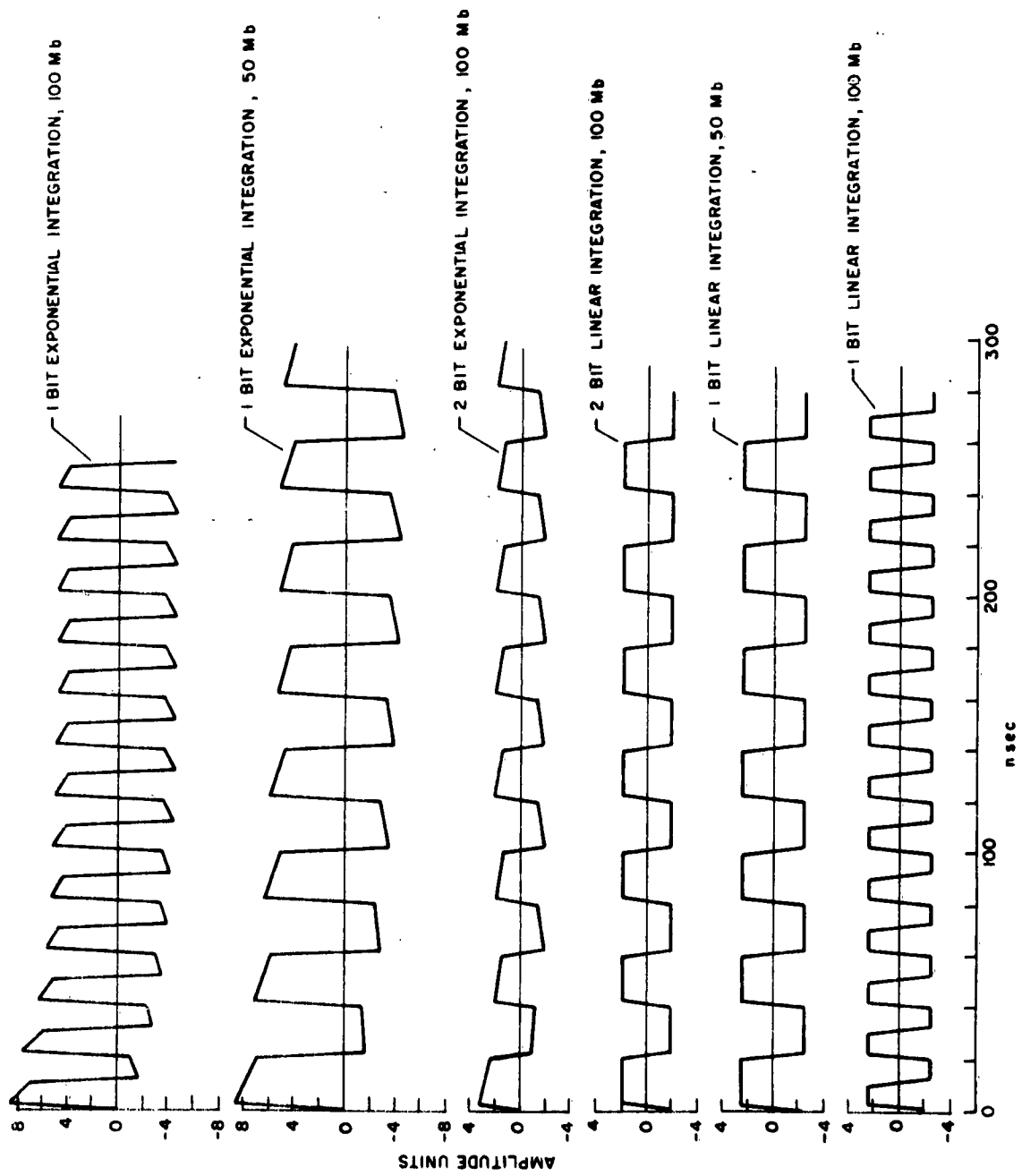


Figure 30. Response of Delta Modulation Systems to Zero Level

In spite of this large amplitude oscillation peculiar to exponential Delta Modulation systems, a comparison of a one-bit linear system and a one-bit exponential system at the same bit rate is favorable to the exponential system in that resolution or rise time response is considerably enhanced. Although contouring has been reduced, this benefit is somewhat nullified because of the large amplitude oscillation in low-detail regions. Compare Figures 15a and 15c scanned with 1024-x-512-element rasters. The one-bit exponential integration parameters were determined by setting $V_{\max}$ equal to the maximum value required by IMITAC to reproduce the image. A midpoint contribution, H , of ± 7 levels, was chosen as a value for the initial simulation; the value of the time constant T was then calculated to be 4.048τ (see Equation 4). Notice that this midpoint value is larger than the step sizes of the ± 5 levels used in the one-bit linear integration simulation. This points out one of the inherent advantages of an exponential integrator in this application. Larger increments may be used to reproduce fast rise times better without the attendant disadvantages of overshooting and contouring that arise in linear integrators with large step sizes.

2. Two-Bit Systems

a. Linear Integration

A problem associated with the one-bit linear integration system is the by-product contouring that results from gaining fidelity in reproducing fast changes in the image. A two-bit system, where a smaller step would be used for slow changes or dc, would reduce contouring. Figure 31a is the output image obtained from a two-bit, linear-integration simulation with step sizes of ± 15 and ± 4 levels, and reference levels of 0 and ± 8 levels, where the input image was scanned by a 512-x-512-element raster. The large step size was chosen to be about one-quarter of the dynamic range of the input signal so that good rise-time information could be obtained, but overshooting would be kept to a minimum. The small step size was chosen to be smaller than the value used for the one-bit system so that contouring would be reduced.

The set of parameters initially chosen appears to have been a good compromise. Resolution was increased over the one-bit system, as evidenced by the city area in the lower-left-hand part of the image. Individual buildings and transitions can be distinguished. Contouring was markedly decreased throughout the image; this is especially apparent in the water areas. A comparison of the graphical plots of Figure 18 (b and c) will help to demonstrate the advantages that the two-bit system has over the one-bit system for step inputs at the same rate. If the sampling rate, and consequently the bit rate, is doubled in a two-bit Delta Modulation system, a very sharp, clear image is obtained as shown in Figure 31b. How much better the two-bit linear



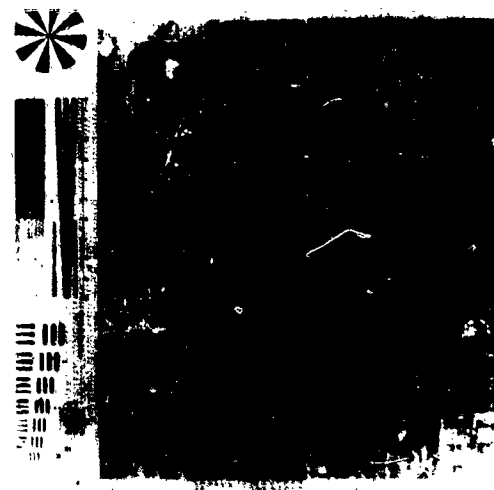
c. 2-bit Exponential Delta-512
T=1.7877



f. 2-bit Exponential Delta-1024
T=37



b. 2-bit Linear Delta-1024
Step Sizes = ± 15 and ± 4 Levels



e. 2-bit Exponential Delta-512
T=47



a. 2-bit Linear Delta-512
Step Sizes = ± 15 and ± 4 Levels



d. 2-bit Exponential Delta-512
T=37

Figure 31 Two-Bit Delta Modulation Systems

integration Delta Modulation system image is than a two-bit PCM image can be seen by comparing Figure 31b and Figure 12e, where the over-all subjective analysis favors the Delta Modulation system, primarily because of the loss of gray scale in the two-bit PCM image.

b. Exponential Integration

The final Delta Modulation system simulated was a two-bit exponential system with several values of time constant. Figure 31c is an output image obtained using $T = 1.787 \tau$. Obviously such a short time constant is not desirable because large amplitude oscillations are generated. An expanded metropolitan area from Figure 31c is shown in Figure 17g. Figure 31d is an output image processed with a $T = 3 \tau$ and integrator contributions of ± 9.1 and ± 2.4 levels at the midpoint. Softening of the dc oscillations has been achieved but at the expense of less resolution. An important fact to keep in mind is that, once $V_{\max}$ and T are specified, the amplitude of the large contribution, H_L , is determined from the equations cited previously in Section II-B. The small contribution is determined primarily from a consideration of the maximum amplitude oscillation that is acceptable about dc at the midpoint of the signal range. Since the ratio of step sizes in the two-bit linear integration system was $15/4$, it was decided to use the same ratio to determine the H_S , given H_L .

The use of a small step in a two-bit exponential system produces an interesting effect for dc levels near the extremes of the signal range. As the integrator signal level approaches the input signal so that the small step is required, the input pulse to the integrator is smaller than the level of the integrator output. After integration the integrator has actually lost energy instead of gaining the small amount desired to approach the input signal level more closely. The next integration may then use a large amplitude pulse and the integrator output again approaches the input. This type of oscillation changes character depending upon the actual dc input level. A graphical example is plotted in Figure 32b. Notice in this case that the period of oscillation is 3τ , the time constant of the integrator. Changing the reference levels and small step size will affect the character of this oscillation.

Specifying $V_{\max}$ and T has two effects which should be noted. The output image obtained with such a system is essentially compressed to a dynamic range less than that of the input as described in Section II-B so that the whites are not quite as white and the blacks are not as black as the input image. However, no loss of detail is apparent. The other effect is that the value of H_L is fixed and cannot be changed unless either $V_{\max}$ or T are changed (see Equations 4 and 5). One reason for the loss of resolution in Figure 31d is the small value of H_L . It is apparent that making T smaller, which would give a larger H_L , produces large amplitude oscillations. Hence, the approach

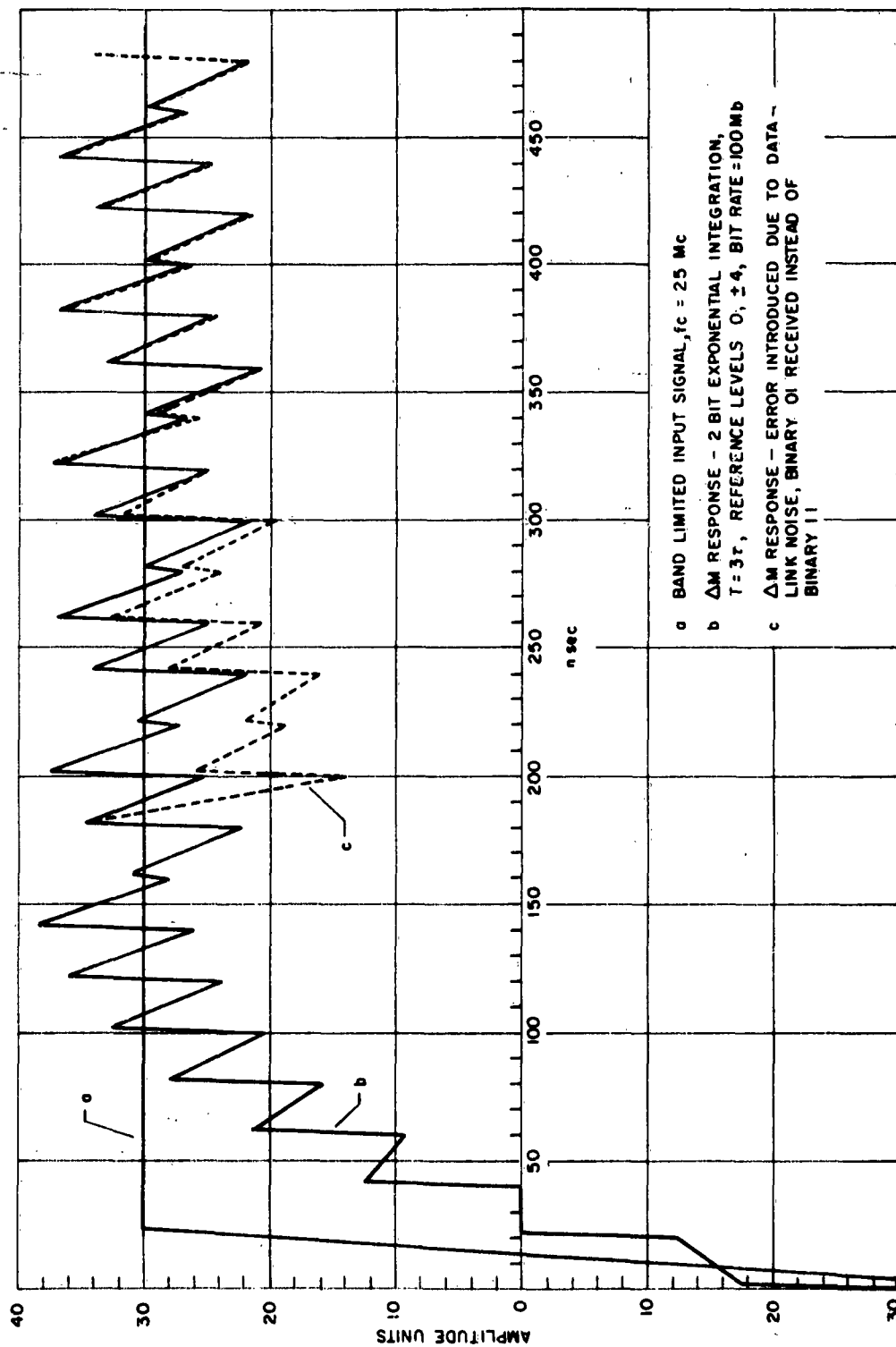


Figure 32. Effect of Data-Link Noise on Two-Bit Exponential System

for choosing parameters was to specify T and H_L and calculate $V_{\max}$. This required that the integrator values be limited for some simulations, since $V_{\max}$ was larger than the range usable by IMITAC. The pulse width, δ , was considered a constant equal to 0.1τ for these calculations.

Figure 3le shows an output image processed by a two-bit exponential system with $T = 4 \tau$, $H_L = \pm 15$ levels, and $H_S = \pm 4$ levels. Limiting was required for this combination of parameters. It is apparent that better rise time has been produced. However, there is significant oscillation because of the large size of H_S .

Figure 3lf shows the output image for $T = 3 \tau$, $H_L = \pm 9.1$ levels, and $H_S = \pm 2.4$ levels, where the horizontal sampling rate has been doubled. Notice that oscillation in regions of constant brightness was improved over that associated with the same system at half the sampling rate shown in Figure 3ld. Also, high-frequency response was improved, as can be seen by comparing the city areas in both images. These improvements have come at the expense of equipment complexity (for a 25-Mc signal, this is a bit rate of 200 Mb).

3. Noise Performance

Linear integration systems have poor performance in the presence of data-link noise, as evidenced by comparing the linear systems in Figure 33 (b and c) with the six-bit PCM reference image in Figure 33a. In each picture, two noise error rates were used. In PCM the noise errors become small dots, and in Delta systems with linear integration, the noise errors become long streaks which hold for many elements, or until the integrator is reset. Errors due to noise have a long-term effect because of the memory in a linear integrator. As a matter of fact, an error in any scan line will affect the rest of the entire scan line. Error rates for linear integrator systems, then, must be quite a bit lower than those for PCM. Error rates for single linear integration systems of the order of 0.0005 corresponding to an S/N of 9.0 db, for differentially coherent PSK transmission, appear to be acceptable (see Figure 34, Curve B).

The effect of noise errors in the DIWP system is shown in Figure 33c. The error rate for the top half of the image is 0.0005 or approximately one error every two scan lines. A single error encountered can eventually cause the second integrator in the decoder to limit at either end of the dynamic range and stay there until several errors occur in the opposite direction or the first integrator is reset at the beginning of the next scan line. This limiting is clearly evident in Figure 33c where long black and white streaks can be seen. The decoder integrator may also be brought out of limiting by large-



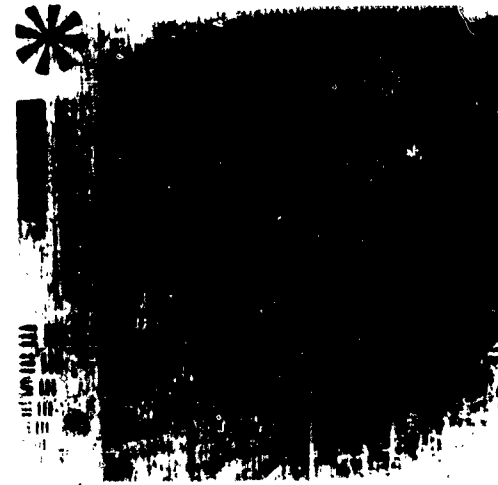
c. 1-bit DIWP Delta-1024
S=4 Levels P=17



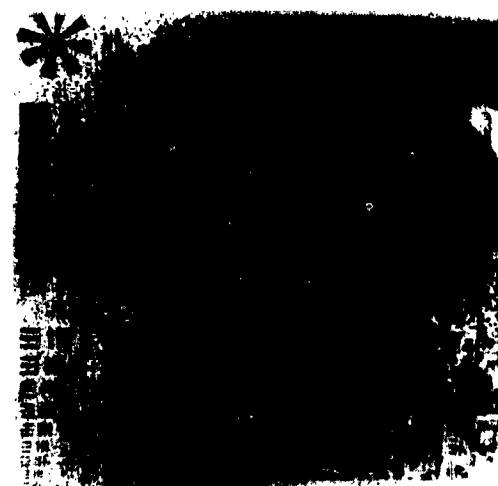
f. 1-bit Exponential Delta-512
T=4.0487



b. 2-bit Linear Delta-512



e. 2-bit Exponential Delta-512
T=37



a. 6-bit PCM-512



d. 2-bit Exponential Delta-512
T=1.7877

Figure 33 Data-Link Noise Simulations

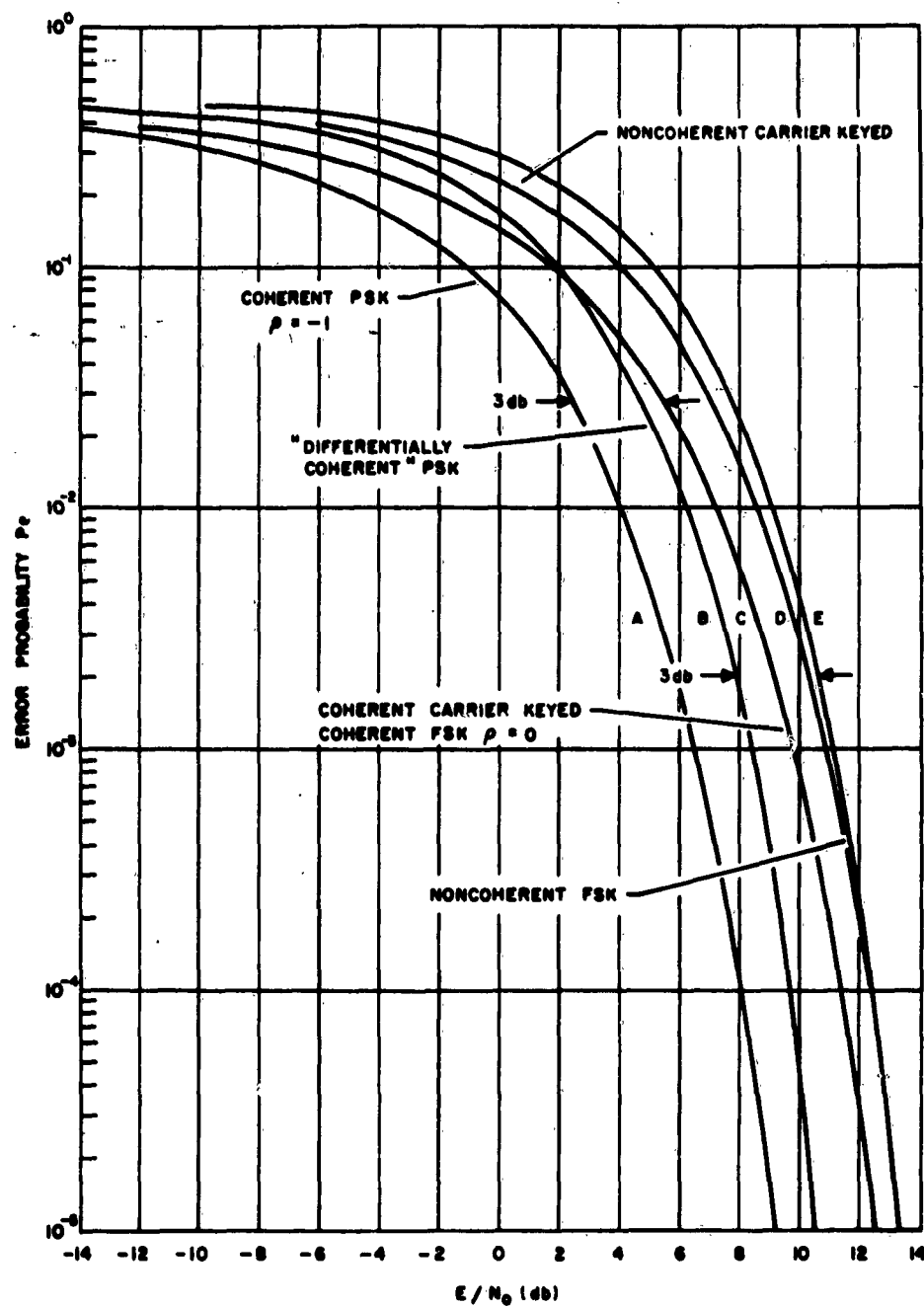


Figure 34 Probability of Error versus Signal Energy
(Per Bit)/Noise Power Density

amplitude changes of information in the opposite direction. However, as soon as constant-brightness areas are encountered, the decoder integrator may again limit. It is concluded that error rates of the order of 0.0001 may be acceptable for DIWP systems.

Much higher error rates can be tolerated with exponential integrators because the effect of the noise is not held over many sampling periods. The shorter the time constant the less effect the noise has. This is readily apparent in Figure 33d where a $T = 1.787 \tau$ was used. The noise pulses exist as elongated dots, approaching those obtained with PCM (Figure 33a). As the time constant is increased, the noise-elongated dots become longer dashes. This effect can be seen in Figure 33e for $T = 3 \tau$ with an error rate of 0.05, or approximately 50 errors per scan line in the upper half of the image. Figure 32 (b and c) shows a two-bit exponential system with $T = 3 \tau$ where an error has been introduced into the most significant bit of the two-bit code. Notice that the system quickly recovers and that after six sampling periods or two time constants the error has practically disappeared. The top half of Figure 33f shows an exponential integration system with an error rate of 0.1. It is evident that this error rate is too severe for the Delta Modulator. Subjectively, it would appear that an error rate of 0.05, corresponding to an S/N of 3.6 db, is the maximum upper limit with such systems (see Figure 34).

Table 8 shows the bit error rates used in the noise simulations shown in Figure 33, and the corresponding data link S/N ratios for "Differentially Coherent" PSK transmission (see Figure 34).

TABLE 8
BIT ERROR RATES USED FOR DATA-LINK NOISE SIMULATIONS

Figure No.	Error Rates		S/N Ratios	
	Top Half	Bottom Half	Top Half	Bottom Half
33a	0.1	0.002	2.0 db	8.0 db
33b	0.05	0.001	3.5 db	8.4 db
33c	0.0005	0.001	8.8 db	8.4 db
33d	0.05	0.005	3.5 db	7.0 db
33e	0.05	0.001	3.5 db	8.4 db
33f	0.1	0.002	2.0 db	8.0 db

E. Comparison of Candidate Systems

A primary consideration in choosing a Delta Modulation system for image coding is the maximum bit rate allowable; it is determined by circuit considerations and the bandwidth reduction desired. What is required is the lowest bit rate possible consistent with good image fidelity as determined, in the final analysis, by a subjective evaluation of the output images. In the discussion which follows it is assumed that the bandwidth of the analog input is 25 Mc. The candidate systems are shown in Figures 14, 15, 35, and 36. Figure 14(b and c) presents images generated by one-bit systems sampling at the Nyquist interval for a 50-Mb rate. There is little doubt that neither the exponential nor the linear system has provided an acceptable output image. The one-bit linear system suffers from loss of high-frequency information and contouring. The exponential system improved the resolution but produced objectionable oscillation in regions of constant brightness. Contouring, while being improved, is still evident, although the large-amplitude oscillation has a tendency to break up the contours and make them less apparent.

Figures 15 and 35 present images generated by 100-Mb systems. Images generated by one-bit systems sampling at twice the Nyquist interval are shown in Figure 15. The improvement gained by doubling the sampling rate is immediately apparent for the linear system. Resolution has improved to the extent that buildings can now be distinguished in the city area. However, contouring is still quite evident because the single step size has not changed from the ± 5 levels. It is further apparent that linear systems require more than one-bit to reduce contouring while still maintaining high-frequency detail, especially at the high bandwidth analog input signal of 25 Mc. The exponential image has improved to the extent that the frequency of oscillation in regions of constant brightness has been doubled, making it less objectionable but still quite noticeable. There also has been an improvement in the detail content of the city area. From a subjective evaluation and considering the discussion in Part D of this section, the system for $S = 4$ levels and $P = 27$ produced the most acceptable output image of the DIWP group. However, when compared with single linear integration and exponential systems, the DIWP system does not fare too well. High-detail information is lost in the encoding process because of the length of recovery time required by the double integrator before it can respond to new change. A computer simulation evaluation of the double integration with phase reversal system discussed in Section II-A may indicate that this undesirable characteristic of the DIWP system at low sampling rates can be decreased. Double linear integration systems will always suffer from a certain amount of contouring because of the finite value of the initial slope, S . An appropriate filter on the output of the system would serve to eliminate some of this.



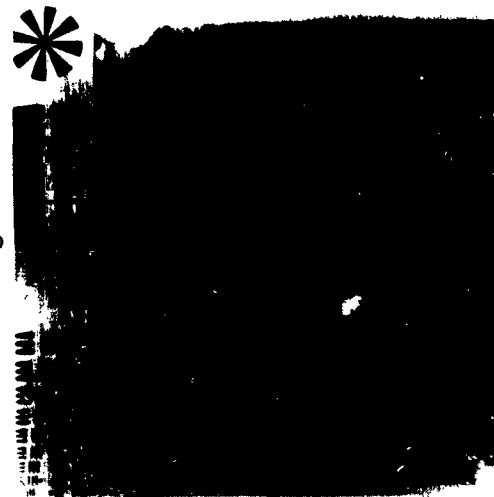
a. 6-bit PCM-512



b. 2-bit Linear Delta-512

Step Sizes = ± 15 and ± 4 Levels

Figure 35 Two-Bit Delta Modulation Systems Sampling at the Nyquist Interval



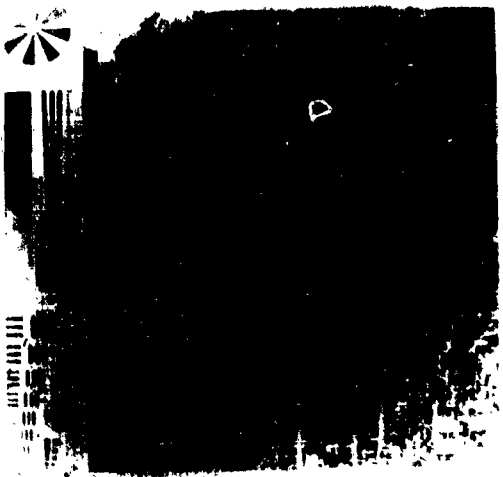
a. 6-bit PCM-1024



b. 2-bit Linear Delta-1024

Step Sizes = ± 15 and ± 4 Levels

Figure 36 Two-Bit Delta Modulation Systems Sampling at Twice the Nyquist Interval



c. 2-bit Exponential Delta-512

T=37



c. 2-bit Exponential Delta-1024

T=37

A 100-Mb rate may be generated by a two-bit system sampling at the Nyquist interval, at the cost of slightly increased equipment complexity. Two-bit images are shown in Figure 35. The two-bit linear system with a small step size of ± 4 levels has reduced the contouring associated with the one-bit system. Also, high-frequency detail has been reproduced more faithfully because of the larger step size of ± 15 levels used.

The two-bit exponential system with $T = 3\tau$ has faithfully reproduced the input with minimum contouring and good rise time response. This system is superior to the one-bit 100-Mb system for $T = 4.048\tau$ (shown in Figure 15 c) because of the reduced oscillation in constant-brightness areas. Considering all factors, it is concluded that the optimum 100-Mb system simulated was the two-bit exponential system with $T = 3\tau$. The two-bit linear system produces acceptable images but is limited in its usefulness for digital communication because of the very low noise error rates that can be tolerated.

Doubling the sampling rate of the two-bit system produces a bit rate of 200 Mb. Images from linear and exponential systems are shown in Figure 36 (b and c). A comparison of the two-bit linear image and the six-bit PCM input image indicates that the linear system reproduces the rise-time information as well as the PCM system does. However, the linear system does have slightly more contouring associated with it, as is evident in the water areas in the images. The exponential system also produces a very acceptable image and, in addition, has the merit of being able to function under much greater noise error rates than the linear system.

In summary, it is concluded that the Delta Modulation systems using exponential integrators produce the most acceptable encoded image when transmission is required in actual communication data links. A time constant of three times the sampling interval appears to be the optimum value.

IV. IMPLEMENTATION OF TWO-BIT DELTA MODULATION SYSTEM

A. Introduction

This section describes a two-bit Delta Modulation system constructed in accordance with the requirements of Phase II of this contract and the design recommendations of the Phase I study. The system consists of an encoder and decoder with one program generator serving both units, thereby eliminating duplicate program generators and the need of synchronization between the encoder and decoder.

Special test equipment for the evaluation of the system is provided in the form of waveform generators and a closed circuit television system. The system can be evaluated on a "response to an input" basis by observing the encoded waveform; also the evaluation of the degradation of pictorial information due to the encoding process can be made by viewing the encoded video information on the television monitor. More detailed pictorial analysis can further be made by photographing a frame of the displayed data on the monitor.

The three modes of operation of the system employ clock frequencies between 20 Mc and 100 Mc in order to provide the demonstration capabilities shown in Table 9.

TABLE 9 - MODES OF SYSTEM OPERATION

Mode	Serial Bit Rate	Sampling Frequency	Information Bandwidth	Demonstration Capabilities
III	20 Mc	10 Mc	5 Mc Maximum	Display encoded video sampled at twice the information bandwidth.
II	40 Mc	20 Mc	5 Mc Typical 10 Mc Maximum	Display encoded video sampled at four times the information bandwidth.
I	100 Mc	50 Mc	25 Mc Maximum	Show encoded waveforms containing frequencies up to 25 Mc; display encoded ramp function as intensity modulated signal on scope to show spatial degradation.

The three clock frequencies shown in the table are provided in the system; however, an external generator may be used to operate at intermediate frequencies if desired. The purpose of the lower frequency operation is to allow evaluation of the effects of encoding pictorial information from a relatively inexpensive source such as the closed circuit television system provided.

Special waveform generators including a square wave and ramp function generator are provided for testing the system at high-frequency operation (50 Mc sampling rate). The response of the system to the square wave is presented on an oscilloscope in the conventional manner, while the encoded (ramp function) waveform is used to intensity modulate the oscilloscope, thereby providing the spatial response of the system at high frequency in the form of a continuous gray scale.

The system is designed to operate basically as a two-bit system; however, simple wiring modifications allow the system to operate as a one-bit encoder and decoder and thus permit comparison of one-bit and two-bit Delta Modulation systems.

The integrator time constant may be varied to provide exponential or linear integration in either the one-bit or two-bit mode. In summary, the demonstration capabilities of the system listed in Table 9 can be performed in a one- or two-bit system using either a linear or exponential integration function.

B. General Operation

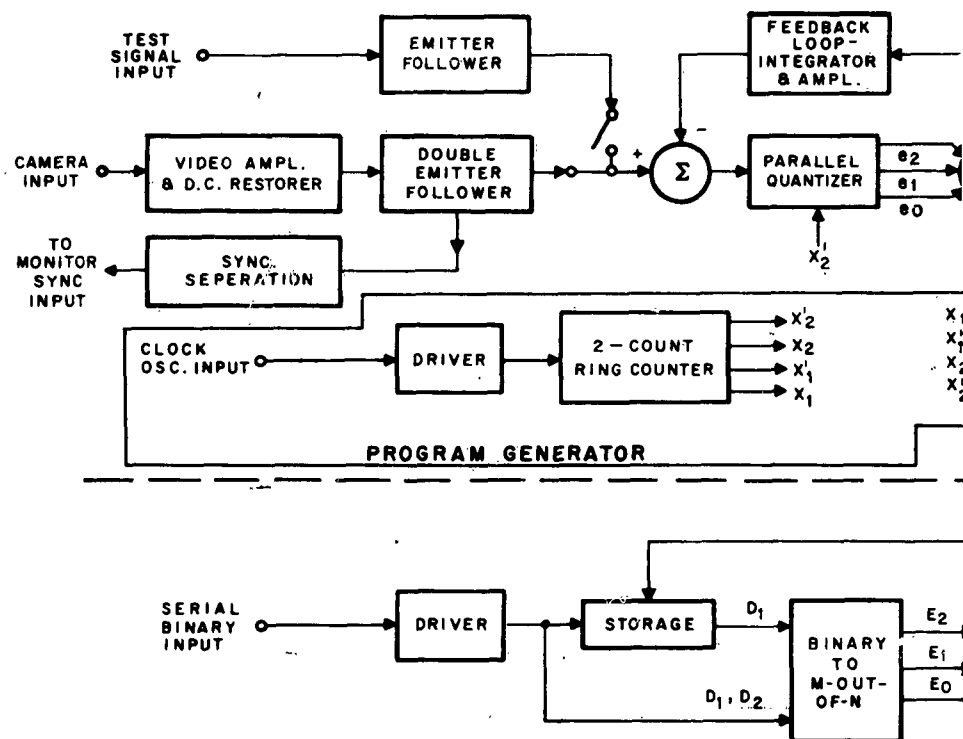
1. System Description

The complete encoder and decoder block diagram is shown in Figure 37. The heart of the system is the quantizer and feedback loop which comprise the Delta Modulation encoding. The quantizer consists of a two-bit parallel encoder which quantizes the error signal in amplitude and time in one operation. The quantizer output pulses are bi-polar and form an m-out-of-n code typical of a parallel encoder. The output pulses are then summed in a linear weighting network resulting in a pulse which may be one of the four levels, $+3k$, $+1k$, $-1k$, or $-3k$, depending on the amplitude of the error signal at the sampling instant. The constant k is a summation attenuation factor which may make the step sizes linear or nonlinear. The output pulses are then integrated in the feedback loop and result in a feedback signal which is a replica of the input analog signal. The feedback signal is continuously subtracted from the analog signal, again providing the error signal for quantization.

The quantizer output pulses are in the form of an m-out-of-n code containing 2^N-1 digits, where N is the precision of encoding in bits, in this case two bits. The three output digits in the m-out-of-n code are converted to the more efficient full-bauded binary code in order to provide a minimum bandwidth transmission channel. The binary digits at the output of the m-out-of-n to binary gates, shown in the block diagram, are in parallel form. The two digits are then read into storage in order that they may be read out of the encoder in serial form by means of the readout gates. The serial code is now full bauded, or non-return to zero, and suitable for single-channel transmission.

The program generator, which consists of the two-count ring counter and transfer gates, provides the basic timing for sampling and parallel-to-serial conversion of the code groups. The program generator serves both the encoder and decoder, thereby eliminating the need of synchronization between the two. This implies that interconnection will be made between the central program generator and the encoder and between the program generator and the decoder. In an actual communication link implementation, the transmitter and receiver would contain separate program generators and synchronization between the two would have to be provided.

The serial output digits are introduced to the decoder, where they are converted to parallel form and into the original m-out-of-n code by means of the storage and binary m-out-of-n gates. A pulse regenerator provides output pulses in the decoder which are identical to the quantizer output pulses in the encoder; integration of these pulses provides an output signal at the decoder which is identical to the feedback signal in the encoder.



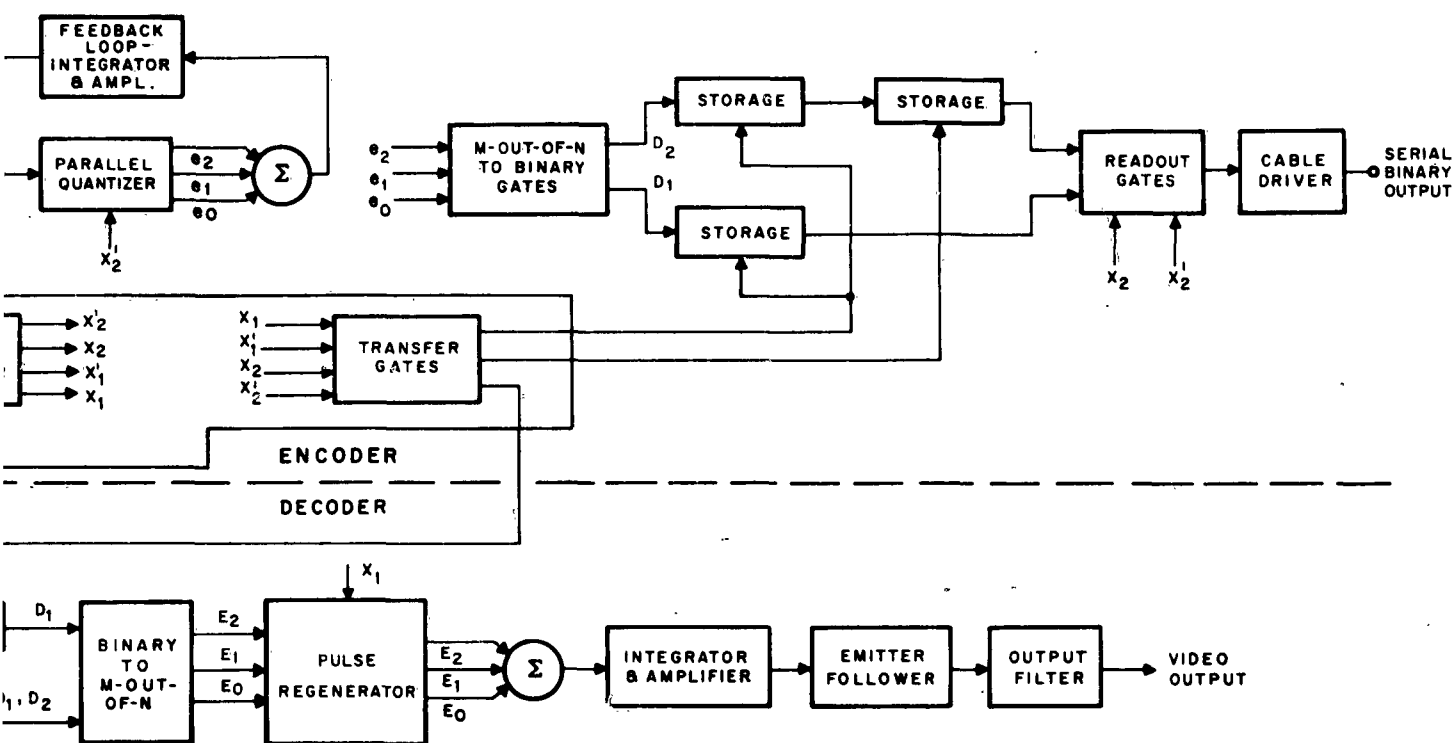


Figure 37. Delta Modulation Encoder and Decoder, Block Diagram

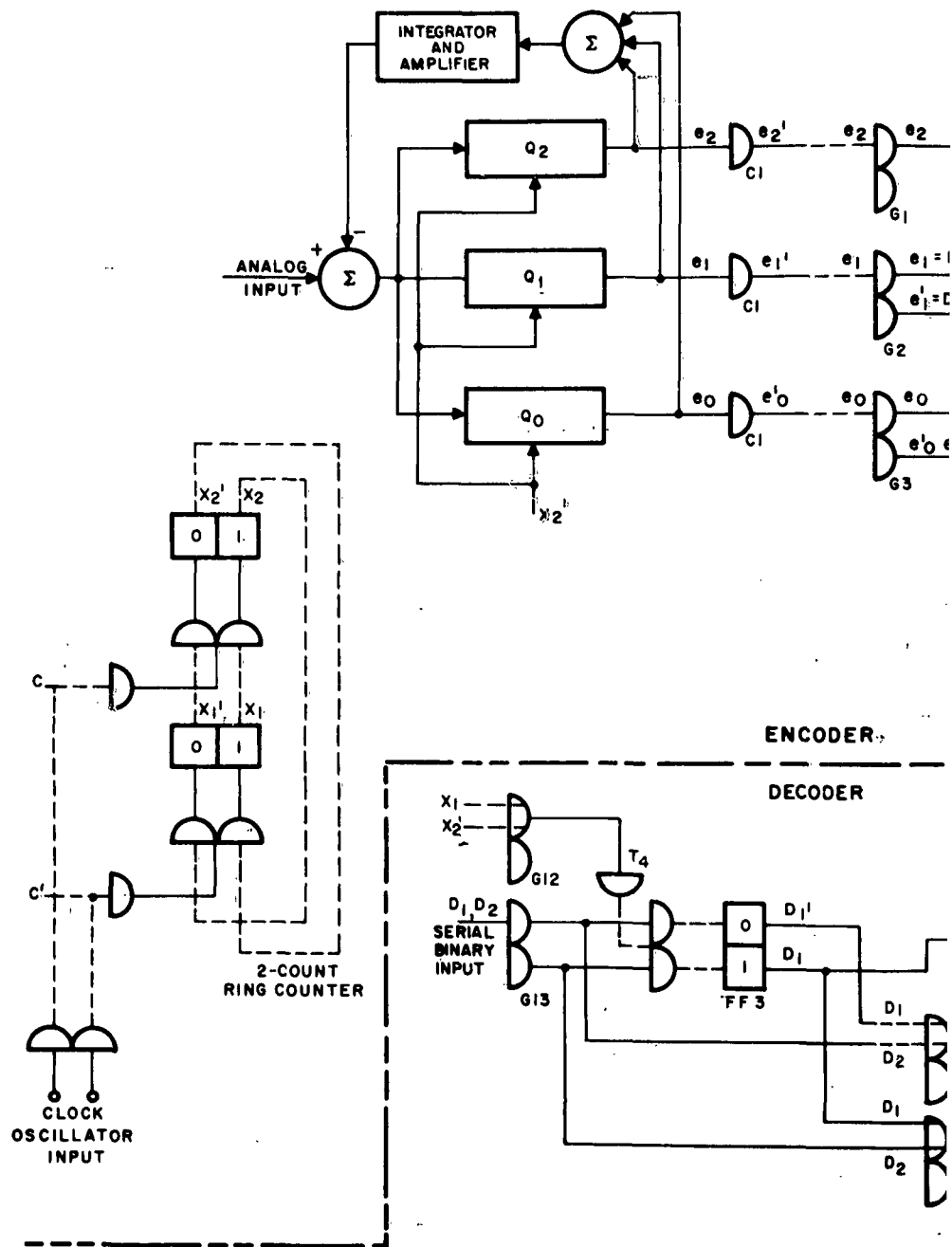
Two input amplifiers are provided, one for the periodic waveform test signals and the second for the composite video of the closed circuit television system. The video input circuit contains a dc restorer and sync separation circuit. The sync pulses are then clipped from the video so that they are not encoded, thus making the most efficient use of the input dynamic range of the encoder.

2. System Logic

The Delta Modulation encoder and decoder actually requires two logic and timing diagrams, since the system must operate at two clock frequency extremes. The switching delays in the various gate and flip-flop circuits are nearly equal to the time of one-half the clock interval, which is 5 ns at the 100 Mc clock frequency. These delays are negligible at the 20 Mc clock frequency, since a clock interval is 25 ns. In summary then, the typical 2.5 ns switching delay is 50% of a clock interval at 100 Mc and only 10% of a clock interval at 20 Mc.

a. Low-Frequency Operation

The logic diagram of the system appears in Figure 38, while the low-frequency, or "ideal," timing diagram is shown in Figure 39. The basic timing is derived from the two-count ring counter, which is driven by the clock oscillator as shown in the logic diagram of Figure 38. Line 1 in the timing diagram represents the clock frequency, where each clock interval is defined as 25 ns for the 20 Mc case. Lines 2 and 3 show the relative phase of the counter outputs X_1 and X_2 with respect to the clock. The sampling interval is derived from X_2' and is shown as S on line 4 of the timing diagram. The sampling pulses trigger the parallel quantizer circuits generating the three resultant quantizer output pulses. These are converted to two binary digits by the m-out-of-n to binary gates shown in the logic diagram. No system delay is incurred in this operation and, since the total circuit delay is small compared with a clock interval, it is not shown on the timing diagram. The converted binary code digits, in parallel form, are therefore shown on lines 5 and 6 as occurring at the same time as the sample pulse. The digits D_1 and D_2 are now read into storage flip-flops FF_1 and FF_{2a} by means of the transfer pulse T_2 , as shown on the logic and timing diagrams. Digit D_2 is then shifted into flip-flop FF_{2b} by transfer pulse T_4 . The relative timing between D_1 and D_2 of the storage and shifting is shown on lines 8 and 10 of the timing diagram. The gates G_9 , G_{10} , and G_{11} then produce the digits D_1 and D_2 in serial form by reading the digits out of storage by means of X_2 and X_2' , as shown on the logic diagram and on line 11 of the timing diagram.



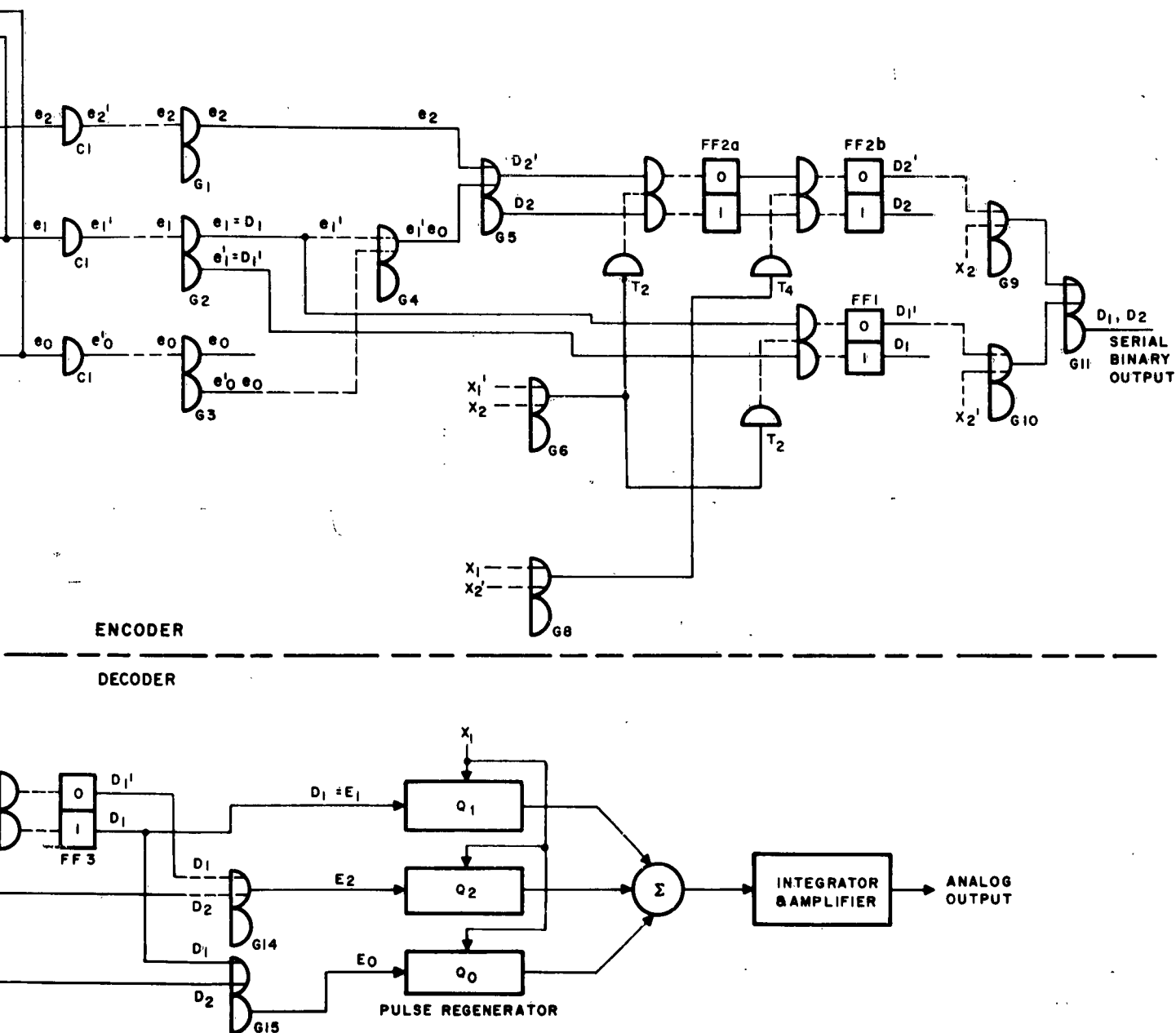


Figure 38. Logic Diagram for Low-Frequency Delta Modulation Encoder and Decoder

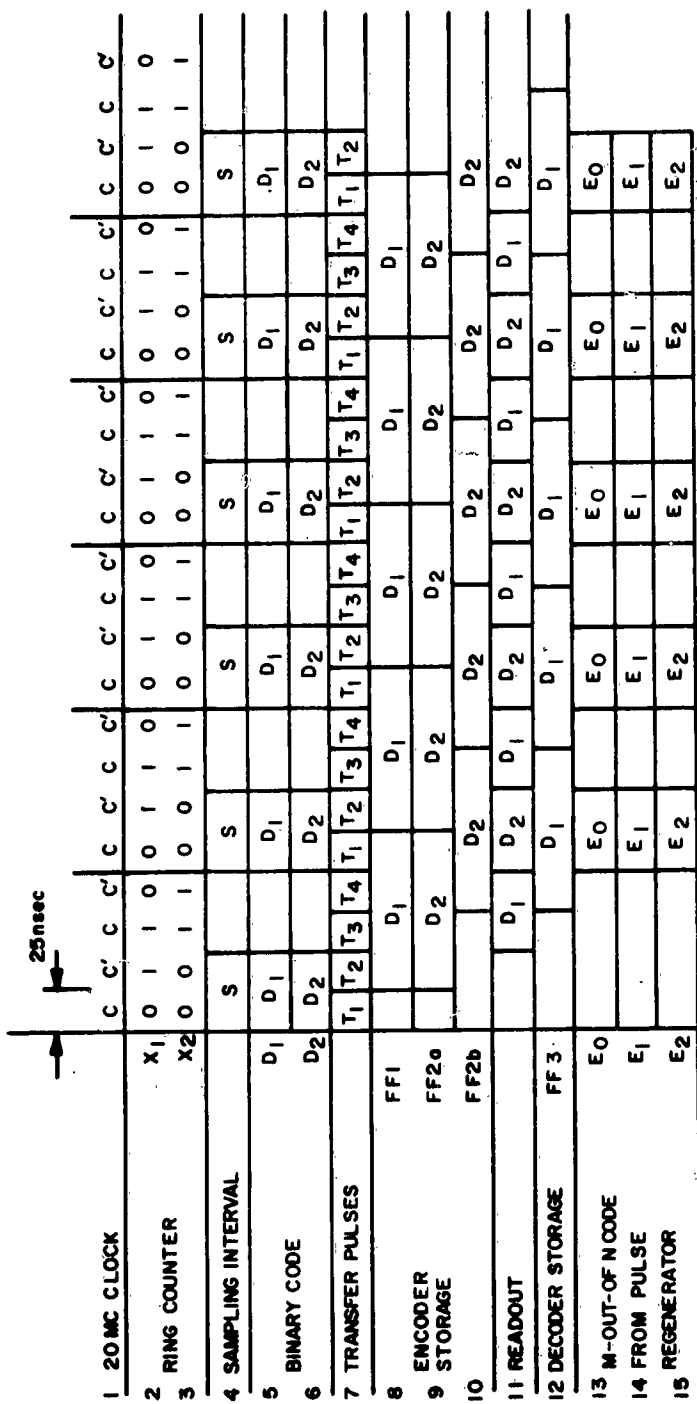


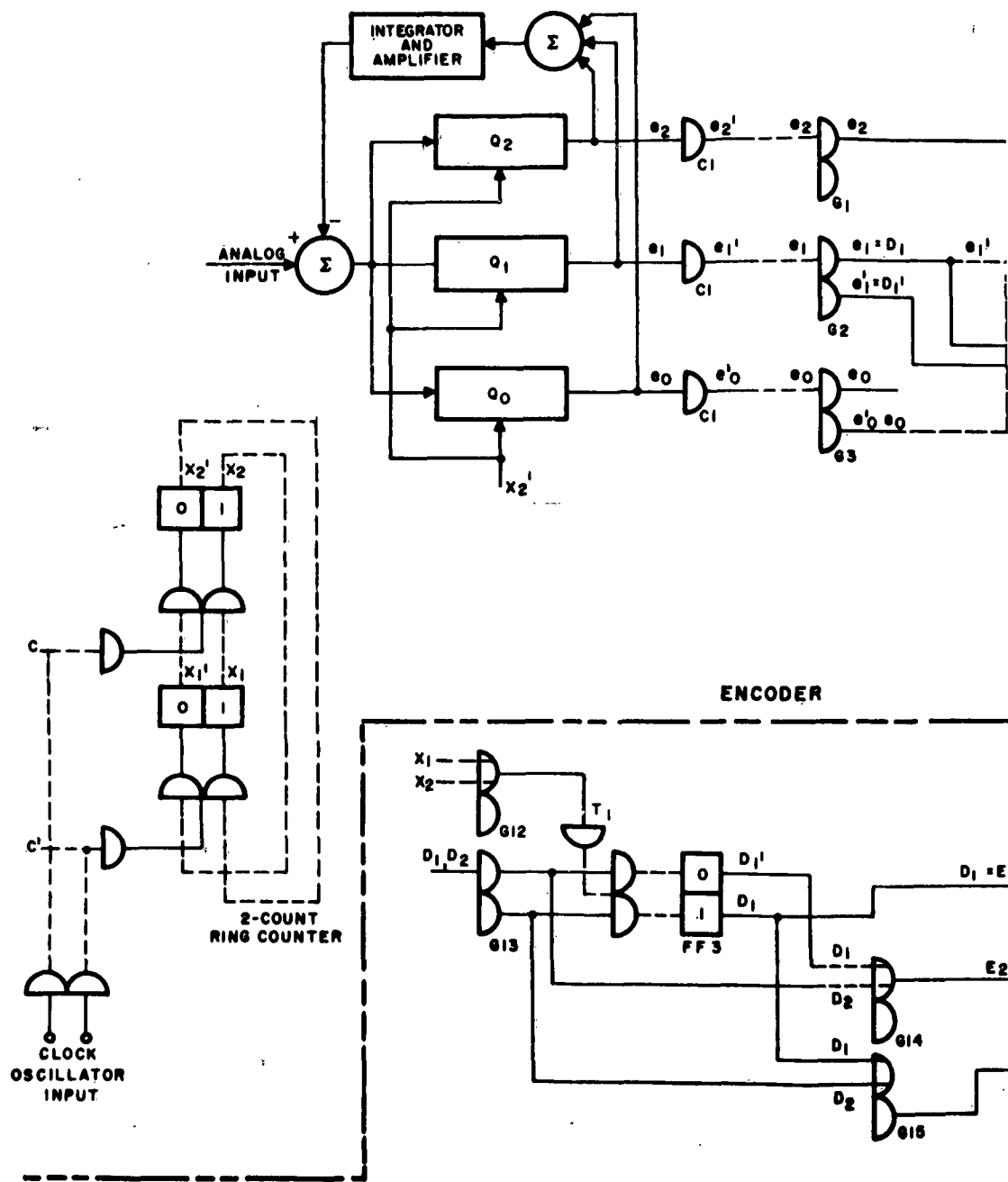
Figure 39. Low-Frequency Timing Diagram

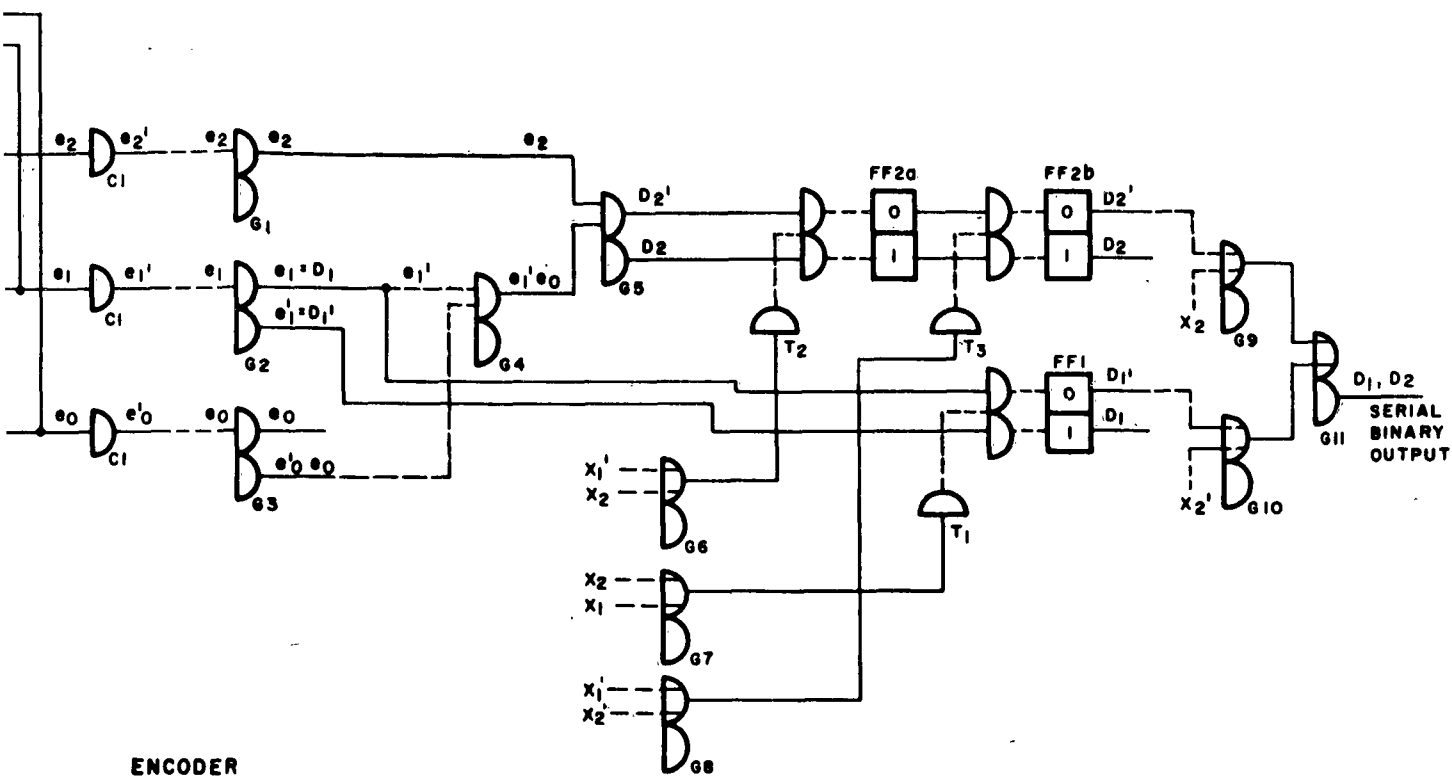
The digits D_1 and D_2 are then transmitted on a single-channel basis to the decoder. Digit D_1 is read into storage flip-flop FF_3 by means of transfer pulse T_4 . Digit D_2 is presented directly to the binary to m-out-of-n conversion gates. This is allowable because the m-out-of-n pulses are requantized both in time and amplitude in the pulse regenerator by means of X_1 . Therefore, the three m-out-of-n digits E_0 , E_1 , and E_2 appear in parallel, as shown in lines 13 through 15 of the timing diagram. The pulses are then summed in a linear weighting network and integrated as in the encoder. This provides an output signal which is identical to the feedback signal in the encoder.

b. High-Frequency Operation

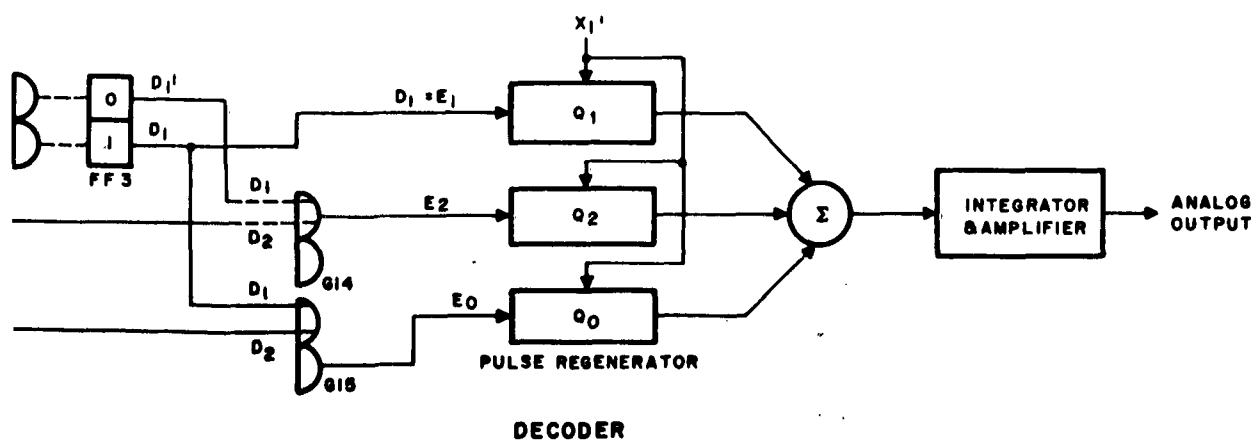
The high-frequency logic diagram is shown in Figure 40 and the timing diagram in Figure 41. The timing diagram for the high frequency operation of the system is more complex than that of the low-frequency, since it shows the switching delays of the circuit which, as mentioned previously, amounts to 50% of a clock interval. Lines 1, 2, and 3 of the timing diagram show the clock and counter outputs as before. In the logic diagram, the counter output X_2' is again used as the sampling waveform; however, notice that the sampling interval is delayed 10 ns, or two clock intervals from X_2' . The logic gates necessary to convert the m-out-of-n code pulses which occur at the sampling time S add an additional delay of one clock interval from time S to D_1 . The formation of D_2 requires two more logical operations than does D_1 , as shown in the logic diagram; therefore, D_2 is delayed an additional clock interval from D_1 , as shown on lines 5 and 6 of the timing diagram. As a matter of safety, D_1 and D_2 are not read into the storage flip-flops FF_1 and FF_{2a} with the same transfer pulse as in the low-frequency case; instead, T_1 is used to read D_1 into FF_1 , and T_2 is used to read D_2 into FF_{2a} , as shown in lines 7 through 9 of the timing diagram of Figure 41 and the logic diagram of Figure 40. Transfer pulse T_3 is then used to shift D_2 from FF_{2a} to FF_{2b} , as shown in line 10 of the timing diagram. The digits are read out serially by X_2 and X_2' , shown on line 11.

These digits are then introduced to the decoder, with additional delay due to the interconnecting cable and input drive circuits, as shown in line 12. Transfer pulse T_2 now reads the serial digit D_1 into FF_3 , with some additional delay as shown in line 14 of Figure 40. Counter output X_1' is used to retime the output pulses E_0 , E_1 , and E_2 , as shown in lines 15 to 17 of the timing diagram.





ENCODER



DECODER

2

Figure 40. Logic Diagram for High-Frequency Delta Modulation Encoder and Decoder

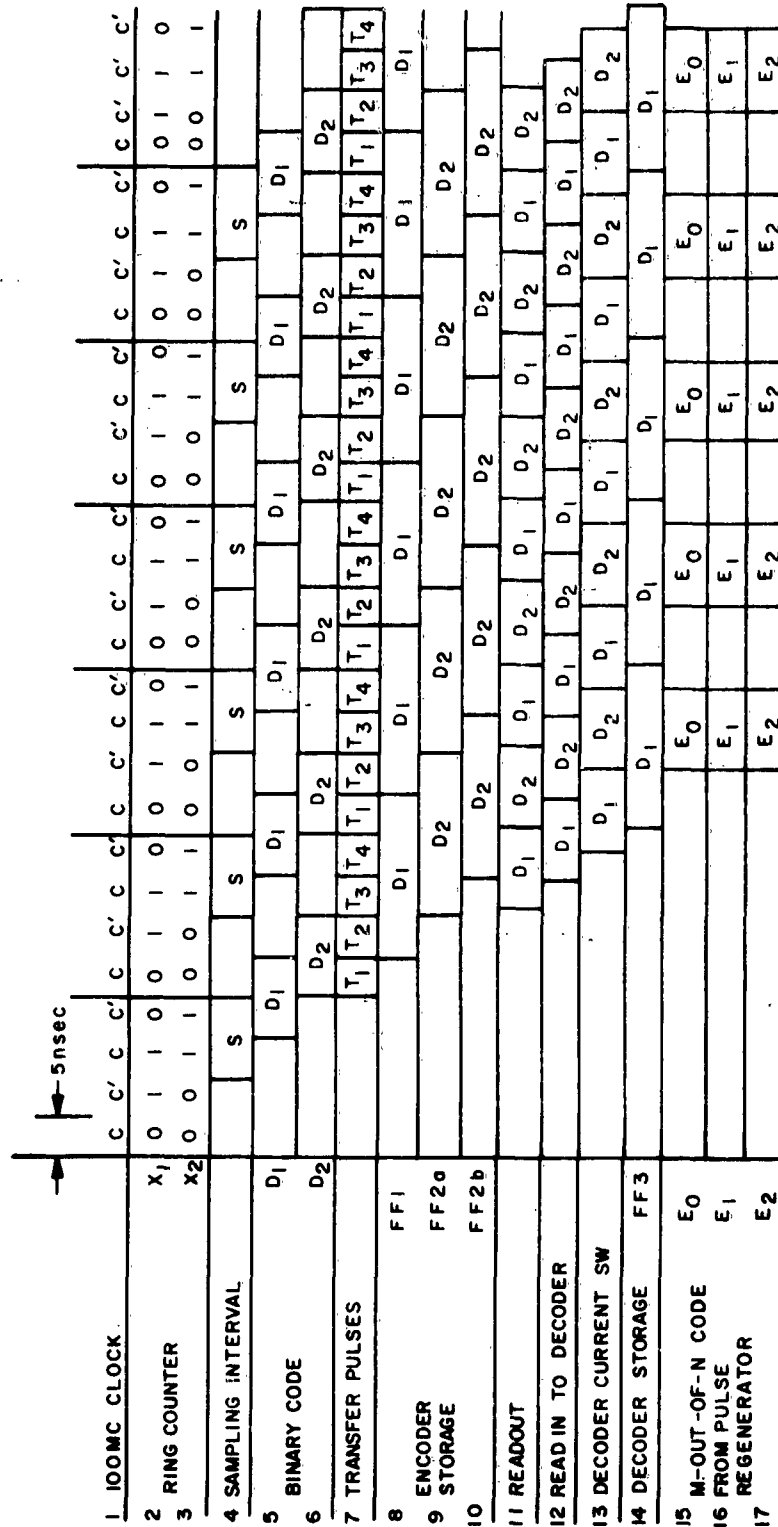


Figure 41. High-Frequency Timing Diagram

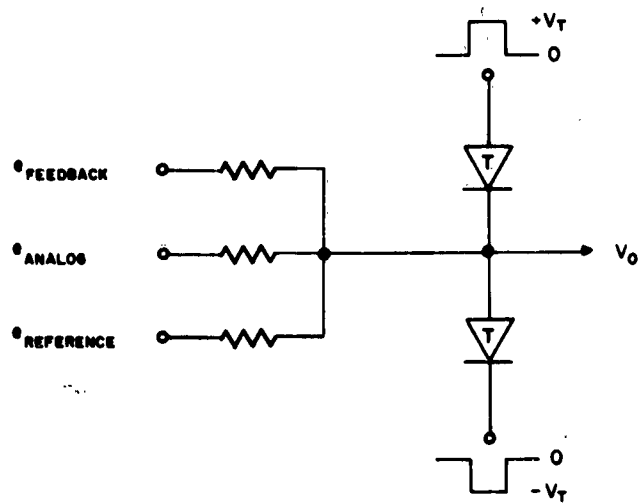
C. Circuit Description

1. Quantizer

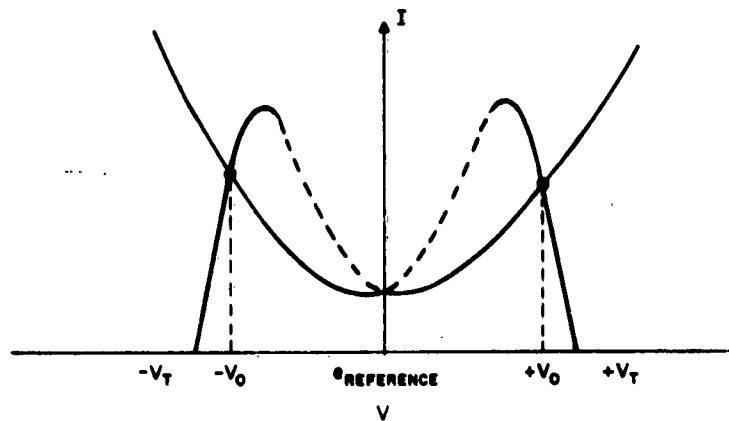
The two-bit quantizer and feedback loop, previously discussed in the block diagram, is shown in Figure 42. The basic element of the quantizer is the tunnel-diode balanced pair, which is triggered by complementary voltage pulses $\pm V_T$, as shown in Figure 43. The tunnel diodes are matched and the trigger source is balanced. The balanced trigger source is provided by the transformers, shown in Figure 42. The amplitude of the trigger source must be sufficient to maintain one diode, but not both, in the high-level state. This level is on the order of 200 Mv for most germanium tunnel diodes. The balanced pair circuit is restricted to two output levels, shown as $\pm V_O$ in the V-I characteristic of Figure 43. The output of zero volts is prohibited, since both diodes are in their negative resistance regions at this point. The circuit is receptive to an input only during the time that the trigger pulses are building up, that is, the time occupied by a change in level of the trigger pulses from their low level to their high level. After this time, the circuit "locks" into one of its two allowable states, plus or minus V_O , depending upon whether the value of the linear summation of inputs is positive or negative at this time.

The tunnel-diode balance pair provides an ideal decision circuit to be used in the time and amplitude quantizing mode, where the sampling pulses now provide the complementary trigger voltage V_T . The linear summation of the input voltages is given by $e_{\text{analog}} + e_{\text{feedback signal}} + e_{\text{reference level}}$. Because the feedback signal is inverted in phase with respect to the analog signal, an effective subtraction results. This subtraction provides the error signal which is added to the self-contained reference level of each of the three quantizers. Upon the occurrence of a sampling pulse, the output of the locked pair will switch to either $\pm V_O$, depending upon the magnitude and polarity of the error signal with respect to the reference level at the beginning of the sample pulse.

The original breadboard model of the balanced pair quantizer provided an output pulse of only 2 ns in width. The trigger, or sampling, waveform is a 50-Mc square wave which has a period of 20 ns. It therefore follows that the pulse width generated could be approximately one-half of the 20 ns period, since the diodes are triggered on during this time. Additional investigation into this problem disclosed that the tunnel diode pair was being operated in an unstable region. The analysis of this circuit by Herzog⁷ shows that three regions of stability can exist, one of which is unconditionally stable and the other two, conditionally stable and unstable. The equivalent circuit of the locked pair is shown in Figure 44 where r is the total driving source resistance,



a. CIRCUIT DIAGRAM



b. V-I CHARACTERISTIC

Figure 43. Tunnel Diode Locked Pair

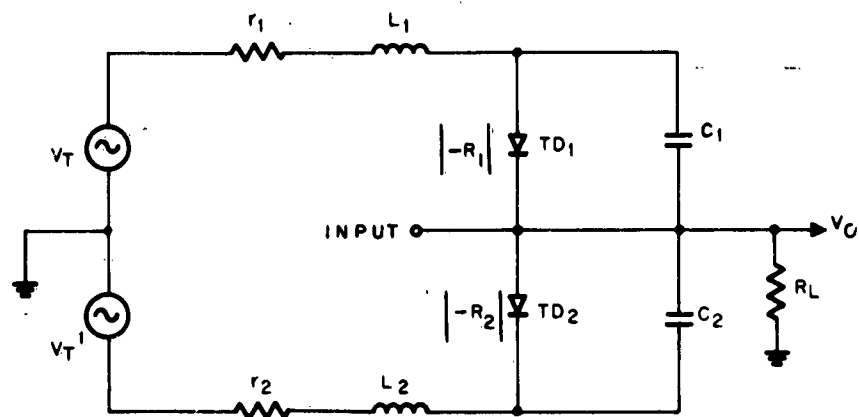


Figure 44. Equivalent Circuit of Tunnel Diode Balanced Pair

L is the series inductance of the tunnel diode plus circuit inductance, and C is the shunt capacitance of the diode plus circuit capacitance. The criterion for unconditionally stable operation is that

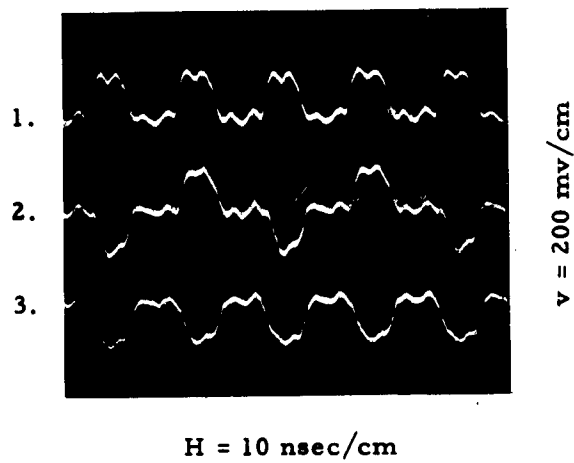
$$\frac{L}{rC} < |-R|, \quad (18)$$

where $|-R|$ is the absolute magnitude of the greatest negative resistance of the tunnel diode. Examination of Equation 18 shows that the series inductance of the diode plus stray circuit inductance must be kept at a minimum, while the diode shunt capacitance plus circuit capacitance may be increased for a given source resistance. Examination of the circuit layout and components showed that operation in the stable region could be easily achieved by going to a slower, higher capacitance diode and taking some layout precautions to minimize the series stray circuit inductance. The results of this effort are shown in the photograph of Figure 45 which shows the three quantizer output pulses for the encoded value of zero volts or the mid-range value. Under the stable operating condition, the pulses are approximately one half the 50-Mc period or 10 ns.

The transmission line transformers were discarded in favor of a quadafilar wound toroid. Because this transformer provides much better operation at low frequencies, it allows improved performance at the 10-Mc sampling rate.

2. Feedback Loop

The output pulses are summed in the 47-ohm resistor at the base of one of the transistors in the difference amplifier through the three 220-ohm weighting resistors as shown in Figure 42. The other side of the difference amplifier is driven by a cancellation signal which is derived from a summing network with impedance characteristics equivalent to parallel combination of the three balanced pairs. This configuration eliminates error signal feedthrough which accompanies the quantization of the error signal by the balanced-pair quantizer. The feedthrough is inherent to the tunnel diode balanced pair since the circuit is bilateral and affords no isolation between input and output. Thus, the signal sum at the summing point consists of quantizer output pulses plus error signal feedthrough. After compensation and amplification have been performed in the difference amplifier, the pulses are integrated at the capacitance C_1 . This capacitance may be varied to control the integration time constant, thereby allowing either exponential or linear integration.



- 1. e_2 - Reference Level = $+v$
- 2. e_1 - Reference Level = 0
- 3. e_0 - Reference Level = $-v$

Figure 45 Balanced Pair Output Pulses

The integrated signal is further amplified by the common emitter stage, which provides inversion of the signal and a means of controlling the feedback gain. The variable gain is necessary because more gain is required for linear integration than for exponential integration. An emitter follower buffer is provided to drive the summation network where the feedback signal is summed with the analog signal and the reference level. The result of this summation, the error signal, is then quantized and the process repeated.

3. Program Generator

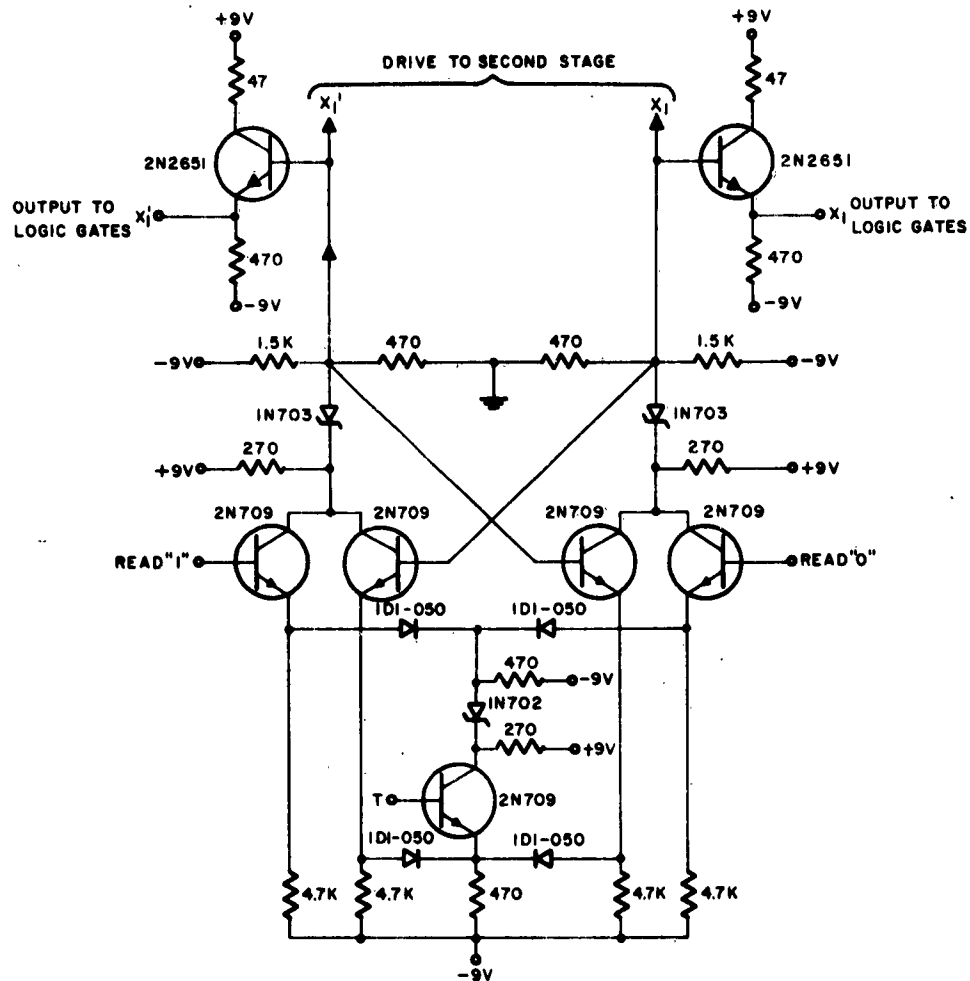
a. Two-Count Ring Counter

The program generator is comprised of the two-count ring counter and transfer gates, as shown in the logic diagrams of Figures 38 and 40. A circuit diagram of a typical stage of the ring counter, along with the logical representation, is shown in Figure 46. The circuit is a rapid-transfer flip-flop which is patterned after the Flashy circuits⁸ which have operated successfully up to 240 Mc. The clock pulses are introduced to the transfer transistor at point T. During the positive portion of the clock pulse, this transistor is turned on, providing an "AND" operation with the pull-over transistor whose input is also positive at that time, allowing the flip-flop to be set to a "ONE" or a "ZERO." When the clock pulse returns negative the flip-flop remains in this preset state.

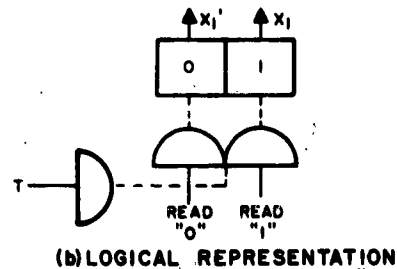
The photograph in Figure 47 shows the two counter outputs and clock input corresponding to the notation in lines 1 to 3 in the timing diagram of Figure 39. The switching time of the counter flip-flops is approximately 2 ns for rise and fall times.

The counter flip-flops are implemented with the 2N709 silicon transistor, which has a gain bandwidth product of 900 Mc and a maximum dissipation of 300 Mw. Because of the loading on the counter these transistors are used in the counter states to allow a nominally high switching current without over dissipating the transistors.

The flip-flops are interconnected by means of the load-resistor output (see Figure 46), while the transfer gate inputs are connected to the emitter follower outputs. This prohibits the loading of the transfer gates from reducing the counter output amplitude to the point where it would become inoperative.

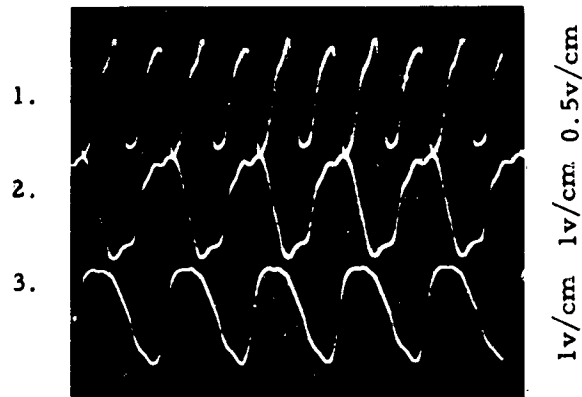


(a) CIRCUIT DIAGRAM



(b) LOGICAL REPRESENTATION

Figure 46. Rapid Transfer Flip-Flop Typical Ring Counter Counter Stage, Type FFI



$H = 10 \text{ nsec/cm}$

- 1. Clock Pulses
- 2. Output x_1
- 3. Output x_2

Figure 47 Ring Counter Output

b. Transfer Gates

The transfer gates are shown in Figure 48. This is a conventional current switch AND gate with a bias network on the inactive side. The bias network is required because of the negative voltage drop from base to emitter in the output emitter followers in the counter. The output voltage swing of these emitter follower outputs is plus and minus about a negative level and does not go positive enough to allow the inactive side of the current switch to be grounded in the conventional manner. By placing the identical negative level of the emitter follower outputs on the inactive side of the current switch, proper operation can be attained.

The photograph in Figure 49 shows a typical transfer pulse along with the gate input signals. The rise time of the pulse is observed to be approximately 2 ns. These gates are implemented with the Philco 2N769 transistor with a gain bandwidth product of 900 Mc. A typical stage delay is under 2.5 ns.

The logical representation, along with a truth table for the AND gate is also shown in Figure 48. The truth table shows that the output will be negative if and only if both inputs are positive, hence denoting the AND function, $T_n = AB$. If "1" is assumed negative, the inputs A and B must be connected to their complements A' and B' in order to obtain the positive levels when A and B are "ones". The transfer gates connect to the counter so that both the signal and its complement are available for use. Therefore, no inverters are needed between the counter and the gate input.

4. Binary Code Converter

The function of the m-out-of-n to binary converter is to provide a two-bit digital code from the three parallel outputs of the quantizer.

The truth table below along with the Boolean equations shown contain all the logical information pertinent to the function of the converter.

e_0	e_1	e_2	D_1	D_2
0	0	0	0	0
1	0	0	0	1
1	1	0	1	0
1	1	1	1	1

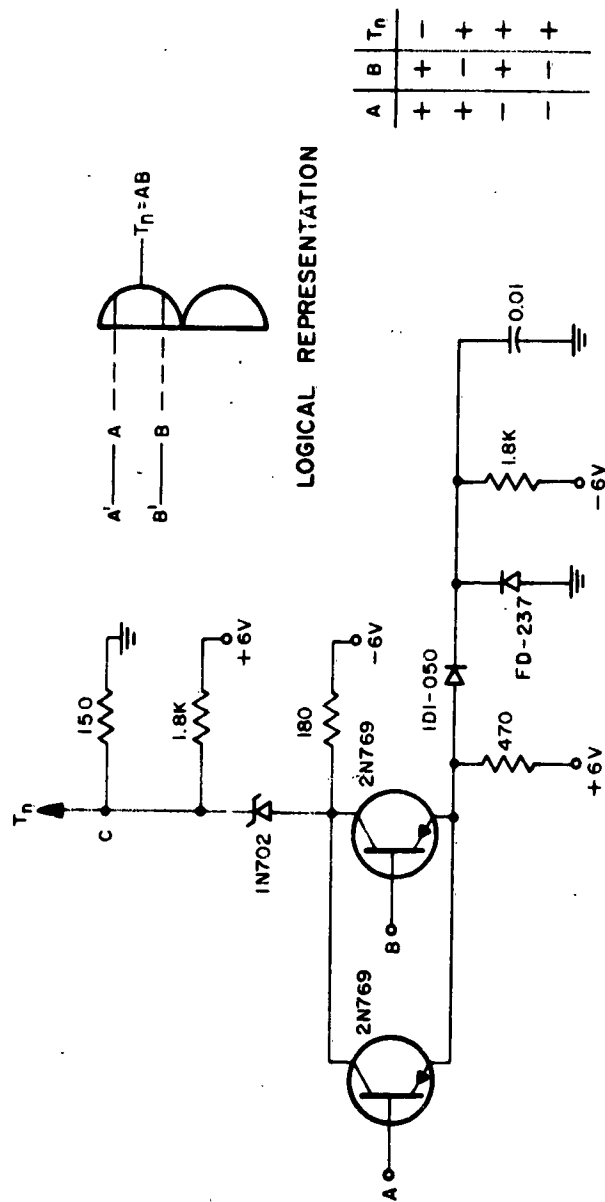
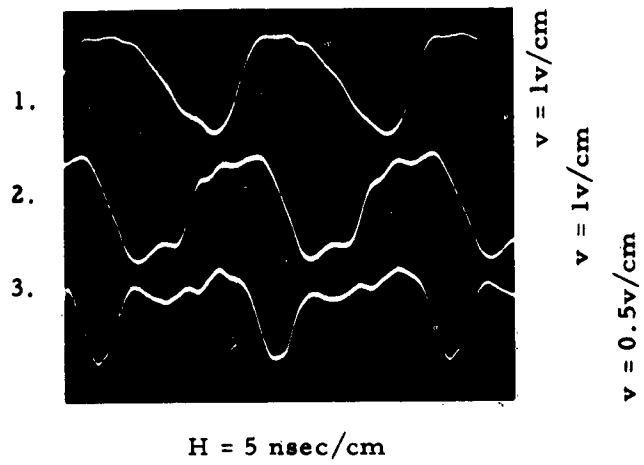


Figure 48. Transfer "And" Gates



1. Input x_1^i
2. Input x_2
3. Transfer Pulse $T_2 = x_1^i x_2$

Figure 49 Transfer Gate Output

$$D_1 = e_1$$

$$D_2 = e_2 + e_1' e_0$$

This is not a complete truth table for a three-input system but accounts for the four possible combinations of quantizer outputs only.

Since the converter must have the capability of driving rapid-transfer flip-flops, the complementary outputs D_1' and D_2' are also provided.

The converter is made up of five current switching circuits which provide the necessary logical functions. These switching circuits are driven by three special amplifier and buffer circuits.

a. Buffer Amplifier

The amplifier and buffer circuit, shown in Figure 50, performs the four basic functions of isolation, amplification, level translation, and conversion from a three-level code to a two-level code. Isolation is provided by the emitter follower and is necessary because the amplifier itself would cause undesirable loading of the quantizer.

The second stage provides amplification through a simple inverter amplifier with a forward biased diode in the emitter circuit to eliminate the positive portion of the input signal. This in effect generates a two-level output signal from a three-level input signal. The positive response of the quantizer is considered binary ZERO and appears as the same level as the baseline between pulses. The necessary translation to drive the current switch inverters is provided by the forward voltage drop of the diode in the collector circuit.

b. Logic Gates

The logic gates used in the code converter, as well as in the rest of the system, are low-dissipation current-mode switching circuits. The buffer amplifiers in the code converter section are followed by an inverter of the types shown in Figure 51 (a and b). The inverter shown in Figure 51a has a single ended output and provides signal polarity inversion. The inverter in Figure 51b is a double-ended circuit which provides both the function and its complement, as shown in the logical representation in the figure.

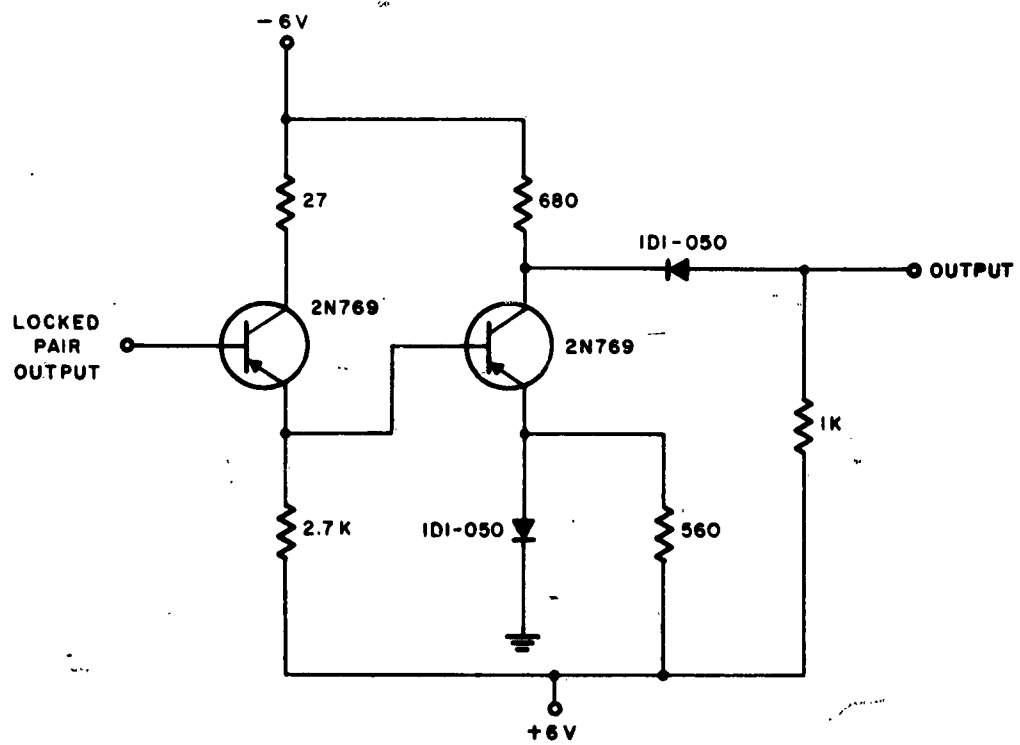
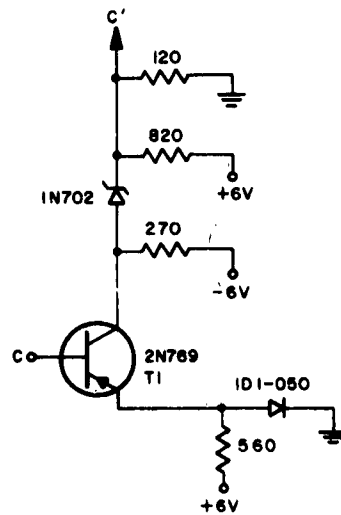
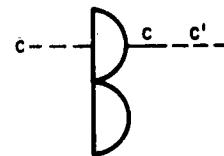


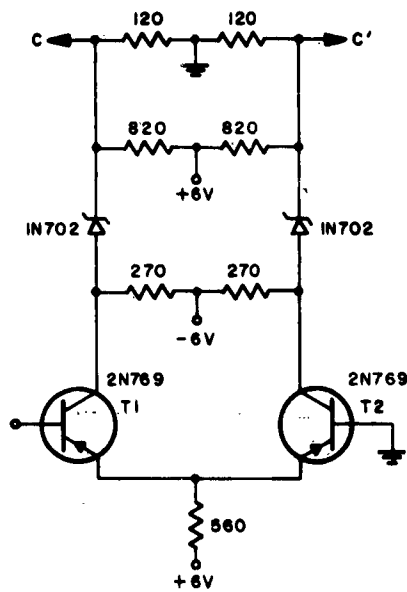
Figure 50. Quantizer Output Amplifier and Buffer, Type CBI



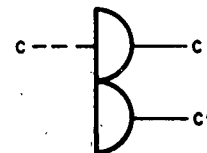
(a) CURRENT SWITCH INVERTER
SINGLE ENDED OUTPUT



LOGICAL REPRESENTATION



(b) CURRENT SWITCH INVERTER
DOUBLE ENDED OUTPUT



LOGICAL REPRESENTATION

Figure 51. Current Switch Inverters

The AND gate shown in Figure 52a is similar to the transfer AND gate discussed previously, except that the inputs to the gate in the figure must be positive and negative about ground, which is the usual arrangement with current switch gates.

The OR gate, along with the logical representation and truth table, is shown in Figure 52b. Again, letting binary ONE be represented by a negative voltage level and binary ZERO by a positive voltage level, the truth table shows that the output will be a "1," or negative, if either or both inputs is a ONE, or negative, thereby generating the OR function.

These gates and inverter circuits are implemented with the Philco 2N769 transistor, which has a typical gain bandwidth product of 900 Mc. Switching speeds on the order of the 2 ns rise or fall times have been observed, with a typical stage delay of 2.5 ns.

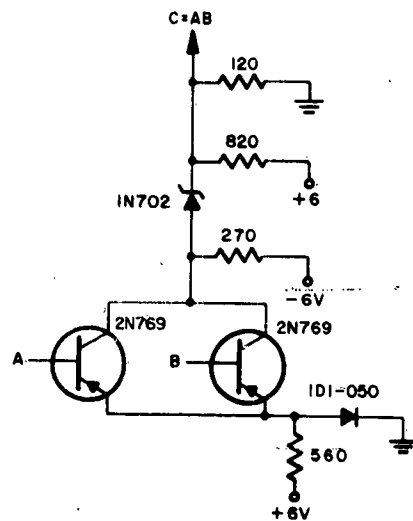
5. Storage Flip-Flops

The storage flip-flops used in the encoder and decoder are of the type shown in Figure 53. These flip-flops differ from the ring-counter flip-flops only by the omission of the switching diodes in the emitter circuit. The storage flip-flops do not have the same loading or speed requirement as the ring-counter circuits and therefore do not require the same complexity.

The storage flip-flops and readout gates are implemented with the Philco 2N2699 transistor, which has a typical gain bandwidth of 450 Mc. These transistors were originally intended to be used in the saturated switching mode; however, the saturated circuits were not reliable enough under load and their use was abandoned in favor of the faster current switching mode of operation.

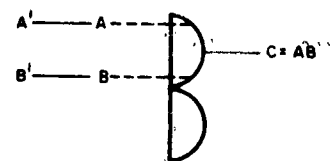
6. Pulse Regenerator and Output Amplifier

The pulse regenerator and output amplifier are shown in Figure 54. The pulse regenerators are identical in operation to the balanced pair quantizer in the encoder. The only difference is that they are driven with the digital signal from the binary m-out-of-n gates. Thus a positive level at the output of a gate which implies binary ZERO will produce a positive pulse from the pulse regenerator identical to the encoder quantizer output pulse. The output amplifiers are identical to the feedback loop amplifier; therefore, the integrator time constant can be varied in the same manner as in the encoder, by varying the capacitor C_I .

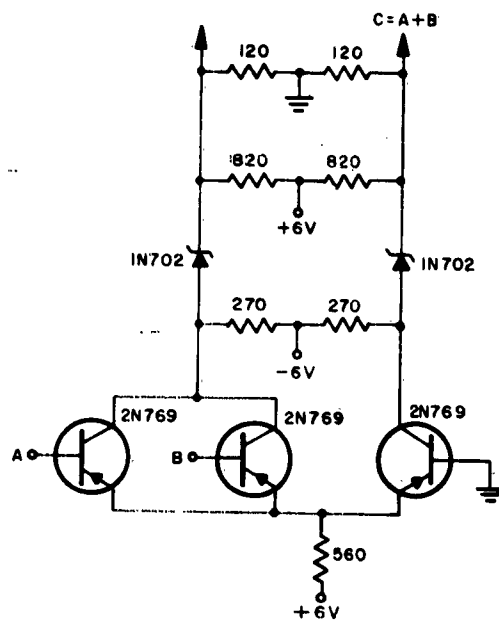


(a) CURRENT SWITCH "AND" GATE

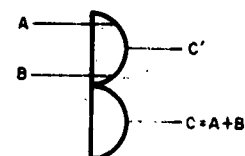
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



LOGICAL REPRESENTATION



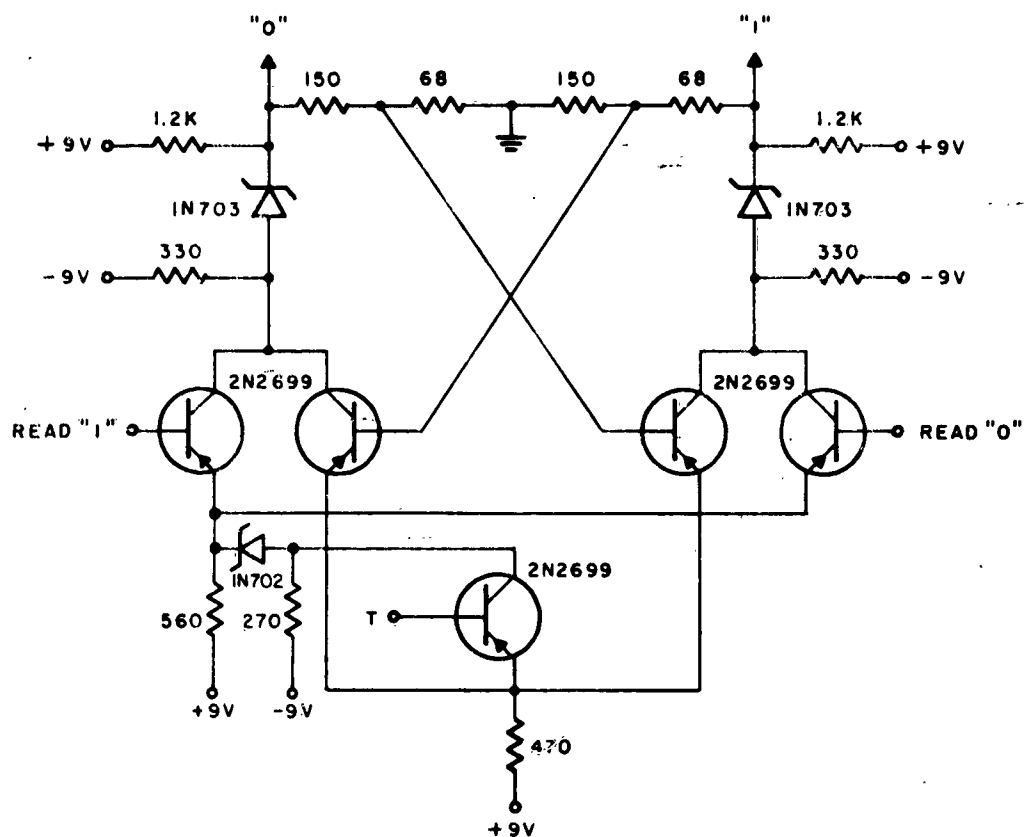
(b) CURRENT SWITCH "OR" GATE



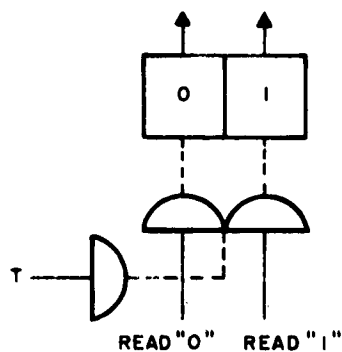
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

LOGICAL REPRESENTATION

Figure 52. Current Switch Gates



(a) CIRCUIT DIAGRAM



(b) LOGICAL REPRESENTATION

Figure 53. Current Switch Storage Flip-Flop, Type FF2

TRIGGER PULSES FROM
X₂ ON
COUNTER

3109

DRIVER
GAIN

500

0.01 μ f

-9V

3.9K

2N2699

39 pf

0.01 μ f

150

560

TR₂

TR₃

TR₁

SAMPLE PULSE DRIVER

E₂

820

470

470

P₂

E₁

820

470

470

P₂

E₀

820

470

470

P₂

-6V

2K

-DL

47

TRA
FORI

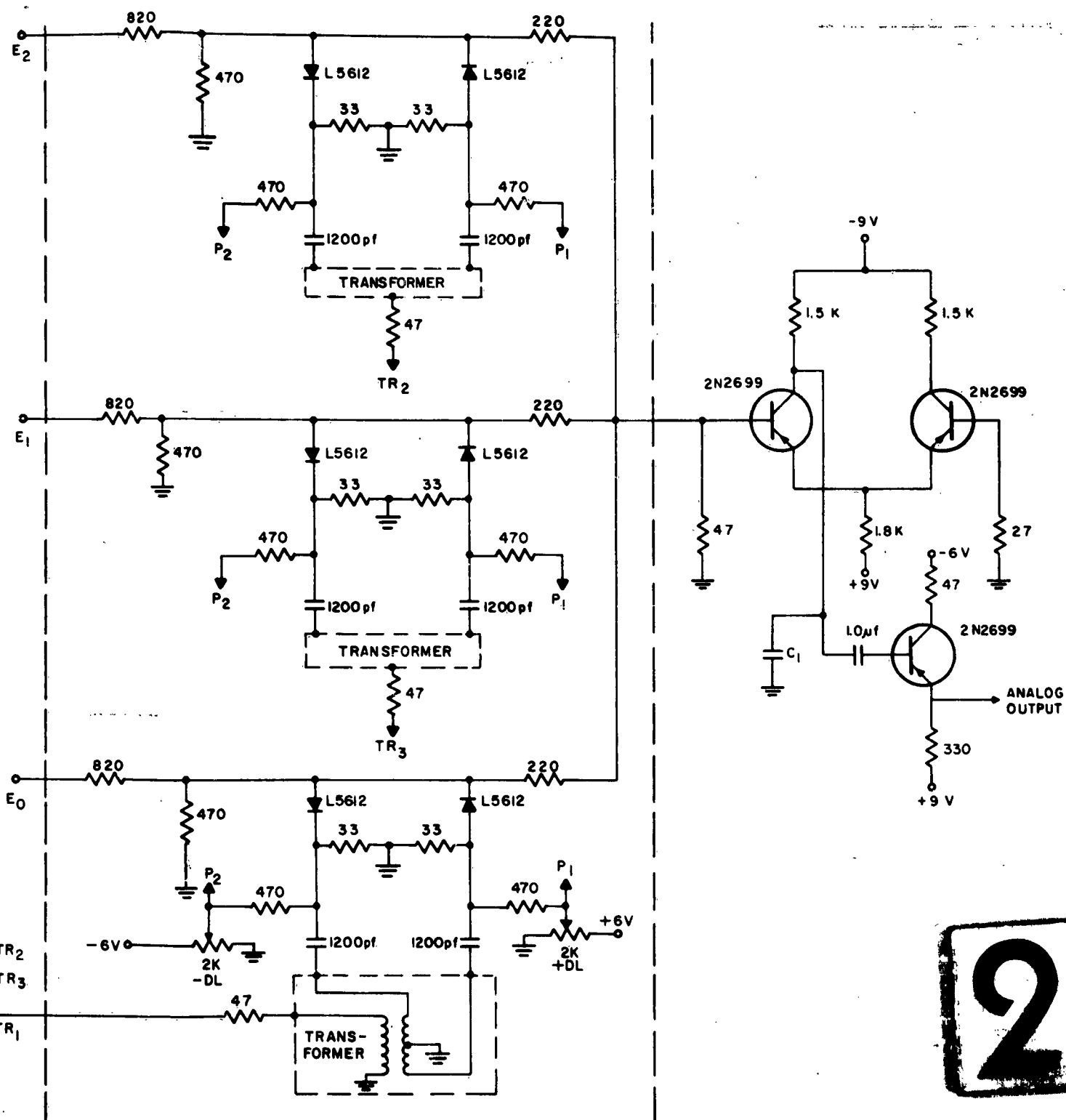


Figure 54. Pulse Regenerator and Integrator Amplifier

V. SPECIAL TEST EQUIPMENT

A. Square Wave Generator

The square wave generator provides a test signal to demonstrate the high-frequency encoding capabilities of the Delta Modulation system. The rise and fall times of the test signal are approximately 16 ns which corresponds to a band-limited signal of 25 Mc.

The circuit diagram of a typical stage of the generator is shown in Figure 55. The generator consists of a four-count binary counter which is triggered by the ring counter in the program generator. Thus, a square wave of 3.12 Mc, which is synchronized with the program generator, is obtained. The response of the system to the square wave may now be seen with the scope synchronized with the input signal, which is in turn synchronized with the program generator. This allows one specific cycle of the square wave to be seen with no overlap of previous traces.

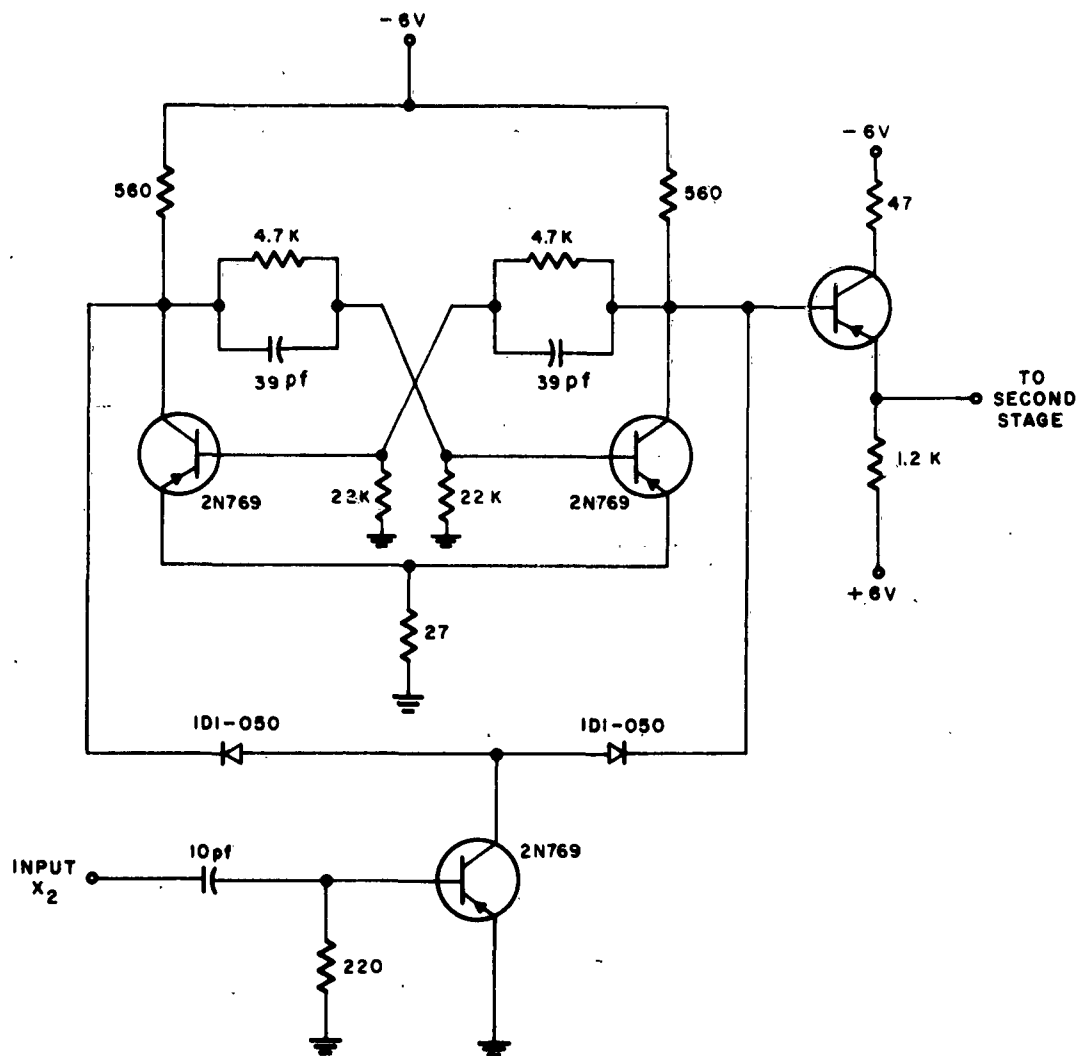
The amplitude of the square wave is continuously variable from zero to 4 volts, which covers the input dynamic range of the system.

B. Ramp Function

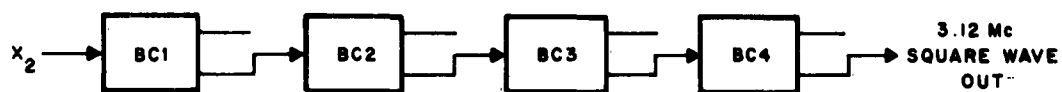
The ramp function is provided by the horizontal sweep sawtooth in the Tektronix Type 581 oscilloscope. The purpose of the ramp function is to simulate a continuous gray-scale input signal. The signal is encoded and the resulting decoded output is used to intensity modulate the oscilloscope. Thus, the spatial degradation of the continuous gray scale is observed by means of the varying beam intensity on the oscilloscope. This test is provided primarily for the high-frequency mode of operation of the system. The horizontal time base of the scope determines the length of the ramp function and can be set to as high a frequency or as short a time as desired. Thus a small number of samples may be observed in the full-range gray-scale presentation showing the effect of each sample point.

C. Closed Circuit TV System

The closed circuit TV system provided as special test equipment is a Sylvania VRF 400 camera and Sylvania RM 14, 14-inch monitor. The system is capable of 400-line resolution and has an over-all video bandwidth of 4 Mc.



(a) CIRCUIT DIAGRAM TYPICAL BINARY COUNTER STAGE



(b) INTERCONNECTION OF BINARY COUNTER STAGES

Figure 55. Square Wave Generator

The TV system is a useful demonstration at both the low sampling rate and the high sampling rate of the encoding system. The encoded display of the video at the 50-Mc sampling rate shows the small amount of degradation of low-frequency information which is present in all video signals, wideband or narrowband.

The primary video demonstration is at the low sampling rates of 10 Mc and 20 Mc, since these rates show the spatial degradation of the information sampled at two to four times the maximum video bandwidth. Thus, the picture information, with regard to contouring the fineness of detail, should appear as it would if 25-Mc video were available to be encoded at the maximum sampling rate of 50 Mc.

1. Video Processing Circuits

A separate video-input to the encoder is provided as shown in the circuit diagram of Figure 42 and the block diagram of Figure 37. A video amplifier with a variable gain control and dc restorer allows the video signal to be set to the optimum amplitude and dc level in order to make the most efficient use of the maximum input dynamic range of the encoder. A sync separator follows the dc restorer. The sync pulses are introduced directly to the monitor, providing stable sync even while adjustments are made on the equipment. The sync pulses are then clipped prior to encoding such that the input dynamic range of the encoder is not exceeded.

D. Oscilloscope

The Tektronix Type 581 oscilloscope, also provided as special test equipment, gives a display for the encoded ramp function at the high sampling rate, as mentioned previously, and allows set-up and trouble-shooting capabilities. The maximum bandwidth of the scope with the Type 86 preamp and passive probe is 95 Mc, which allows a minimum rise time of 4 ns. This is adequate for all set-up and for most trouble-shooting operations. The fidelity of the quantizer pulses and switching waveforms is degraded if they are viewed on this scope; however, the signal is preserved well enough to detect an inoperative circuit or one that is not operating properly.

E. Power Supplies

Four power supplies with a voltage range of 0 to 18 V and maximum load current of 1.5 amperes are provided as primary power for the encoder and decoder. The supply voltages required for the system are as follows:

+9 V	at	500 ma
-9 V	at	500 ma
+6 V	at	500 ma
-6 V	at	500 ma

The power supplies provided are Harrison Labs Model 855B with rack mounting panels. The stability and load regulation specification for the supplies are as follows:

Stability:	< 30 Mv total drift for 8 hours
Load Regulation:	0.03% or 6 Mv (whichever is greater) for a 1.5 ampere level charge.

VI. TEST PROCEDURES AND RESULTS

The following tests and measurements were made on the two-bit Delta Modulation feasibility model.

1. Analog waveform tests using square wave, sine wave, and ramp.
2. Closed circuit television encoding.

The operating conditions of the equipment were as follows:

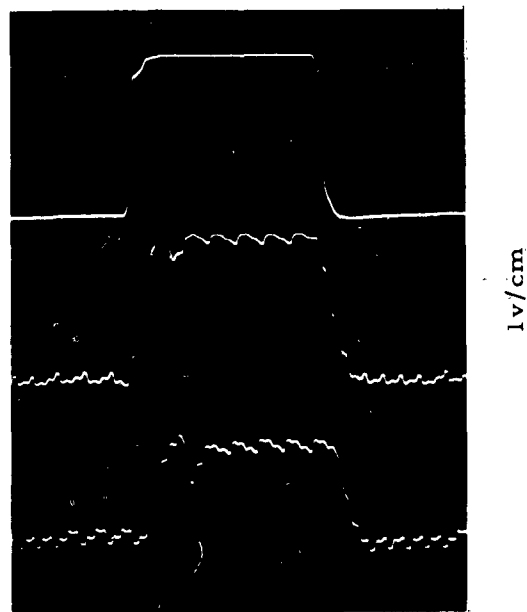
- | | | |
|-----------------------------|---|--------------------------|
| 1. Sampling Rate | - | 50 Mc |
| 2. Bit Rate | - | 100 Mb |
| 3. Precision of Encoding | - | 2 bits |
| 4. Integrator Time Constant | - | $3 \tau = 60 \text{ ns}$ |
| 5. Decoder Output | - | Not filtered |

A. Square Wave Measurement

In Figure 56, the measured response to a full dynamic range 1-Mc square wave (a) is shown at the feedback loop of the encoder (b) and the output of decoder (c). Since the rise and fall times of the input square wave representing the fastest black-to-white transition in an image whose video bandwidth is 25 Mc are faster than the sampling period (20 ns) of the encoder, the encoder takes approximately three and one-half samples to respond (10% to 90%) to the fast change in input signal. Theoretically, this is shown in Figure 32. In the photograph observe that the decoder response is identical to that of the encoder. The dc oscillation at the extremes of the encoding range is shown on an expanded time scale in the photograph of Figure 57 and theoretically in Figure 32.

B. Sine Wave Response

Sine waves of frequencies from 1 kc to 10 Mc were encoded by the Delta Modulation equipment and are shown in Figures 58, 59, and 60. Notice in the response of the lower frequency sine waves that the small step only is used in reproducing the input sine wave due to the slowly changing amplitude of the input (that is, the error signal is small at all times). However, at the higher input frequencies a mixture of small and large increments is needed by the encoder to follow the input. At all measured frequencies the encoder and decoder reproduce exactly the sine wave input as predicted by theoretical



100nsec/cm

- a. Input Signal
- b. Output of Encoder Feedback Loop
- c. Output of Decoder

Figure 56 Response of Delta Modulation to 1 Mc Square Wave

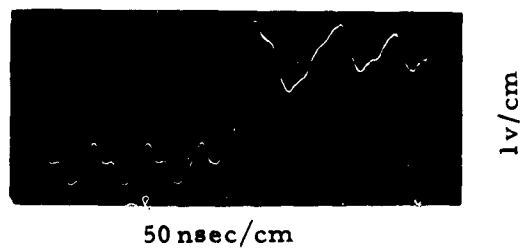


Figure 57 Response of Delta Modulation Encoder to a Constant Level

analysis. In the expanded time scale photograph of Figure 60, the actual increments or step sizes are shown on a per-sample basis.

C. Ramp Waveforms

In Figure 61 the response of the system is shown for a ramp signal corresponding to a continuous gradient in an image. Notice that many small plateaus appear in the reproduced waveform due to the quantization process of the encoder. The magnitude between plateaus is directly related to the step sizes, reference levels, and time constant of the integrator.

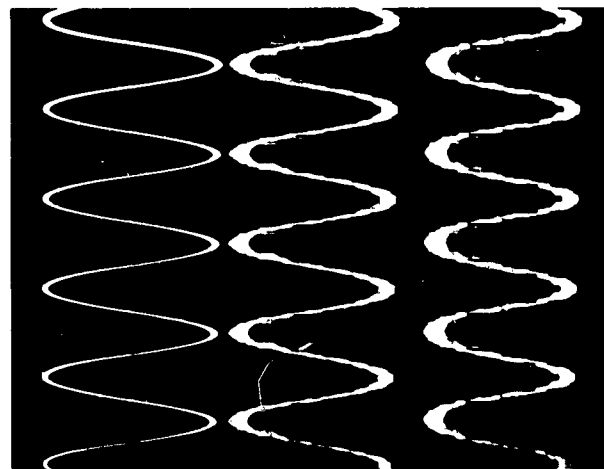
D. Video Encoding

The video signal from a closed circuit television system was encoded and decoded by the experimental equipment. The block diagram for the system test is shown in Figure 62. Pictures of the monitor were taken of the uncoded and coded video displays, as shown in Figure 63. It should be noted again that the sampling rate is 50 Mc, while the input video bandwidth is restricted to about 4 Mc; thus, a much higher ratio of sampling frequency to video bandwidth than would be employed in an actual communication system has been used in this measurement. It is clearly evident from the photographs that hardly any perceivable degradation in gray scale and resolution has been introduced by the encoding process.

E. DC Response

Encoder code groups, in response to various DC levels applied at the input to the system with a 10-Mc sampling rate, are shown in Figure 64. As is characteristic of exponential integration, each level has a unique response both in periodicity and amplitude.

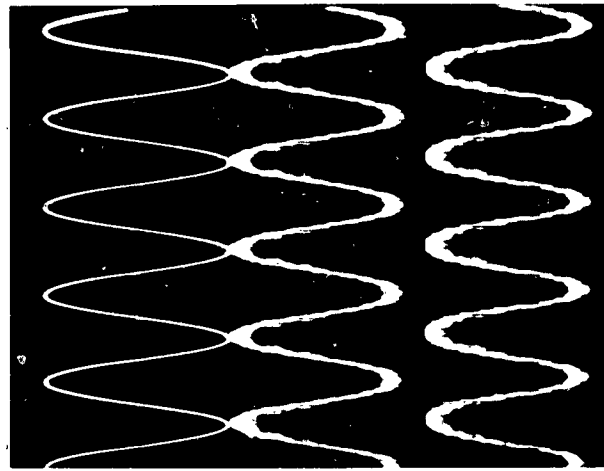
Notice the response to a -100 mv level is the mirror image of the response to a +100 mv level which is indicative of proper operation. Figure 64-D3 shows the response of the system to a DC level input which is within a quantization region. This region is explained in detail in Section II-B-2d. The period of the code group in the quantization region is exactly that of the sampling pulses and is therefore the highest frequency of oscillation exhibited in any of the code groups.



50 μ sec/cm

1. Input
2. Encoder Feedback Signal
3. Decoder Output

a. 10kc Input Signal



500 μ sec/cm

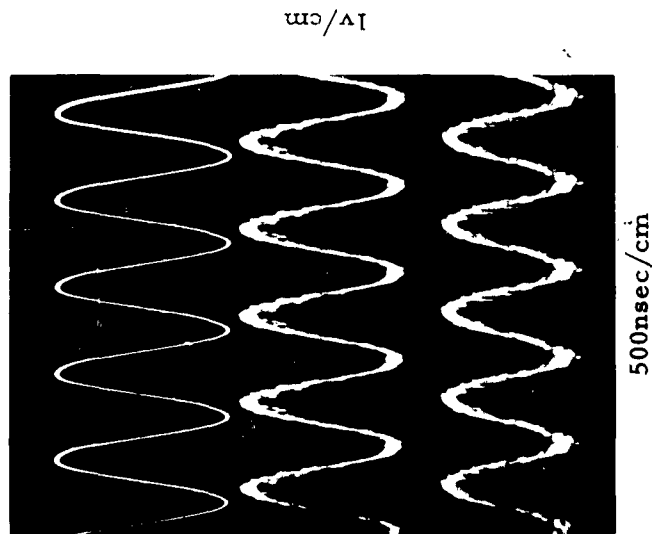
1. Input
2. Encoder Feedback Signal
3. Decoder Output

b. 1kc Input Signal

1v/cm

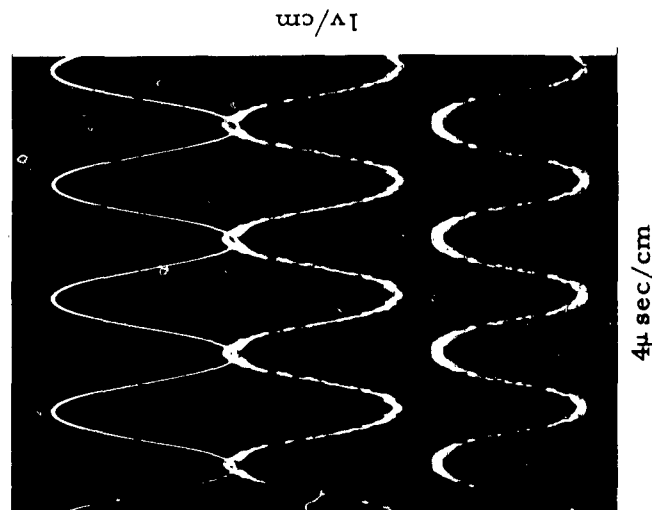
1v/cm

Figure 58 Sine Wave Response of Delta Modulation System



1. Input
2. Encoder Feedback Signal
3. Decoder Output

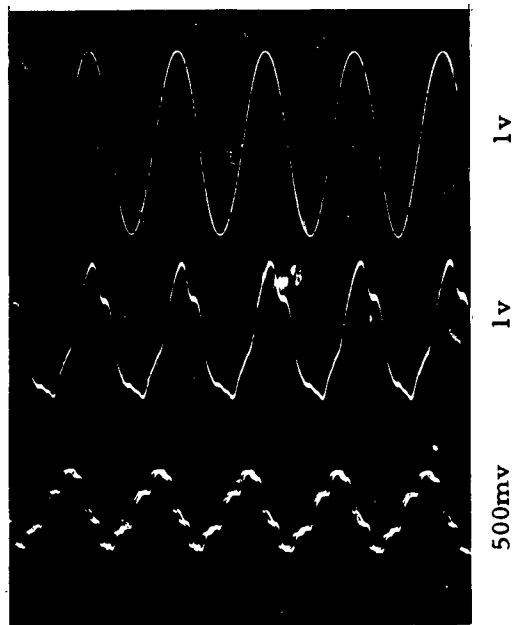
a. 1Mc Input Signal



1. Input
2. Encoder Feedback Signal
3. Decoder Output

b. 100kc Input Signal

Figure 59 Sine Wave Response of Delta Modulation System

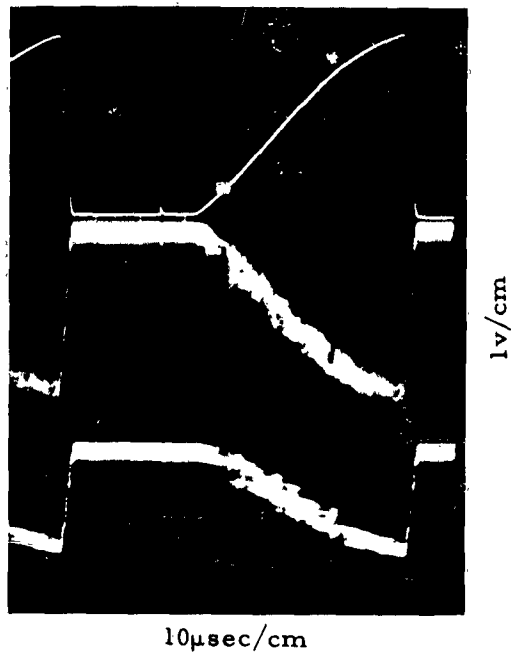


50nsec/cm

1. Input
2. Encoder Feedback Signal
3. Decoder Output

10Mc Input Signal

Figure 60 Sine Wave Response of Delta Modulation System



1. Input Signal
2. Encoder Feedback Signal
3. Decoder Output

Figure 61 Response of Delta Modulation System to Ramp Function

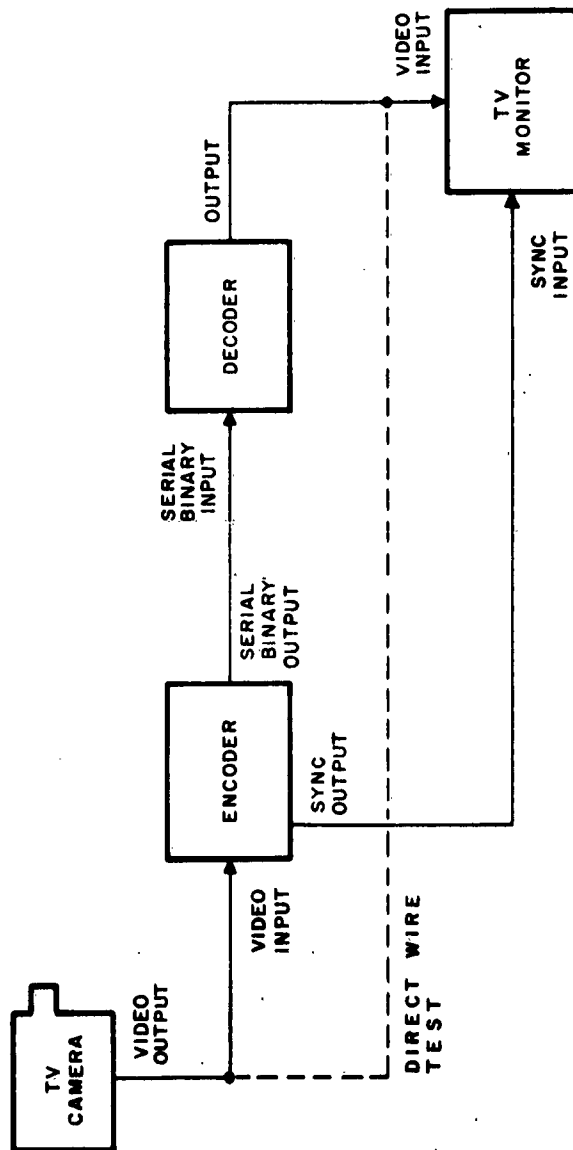
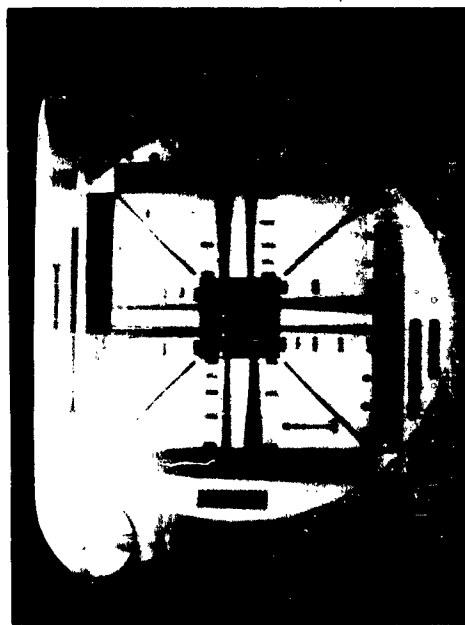
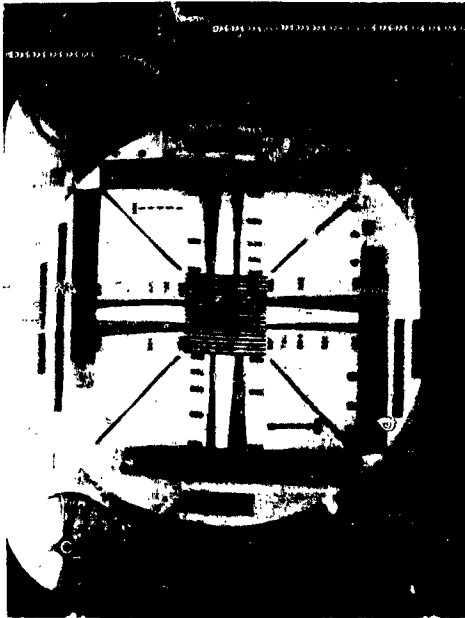


Figure 62. Block Diagram - Closed Circuit TV Presentation

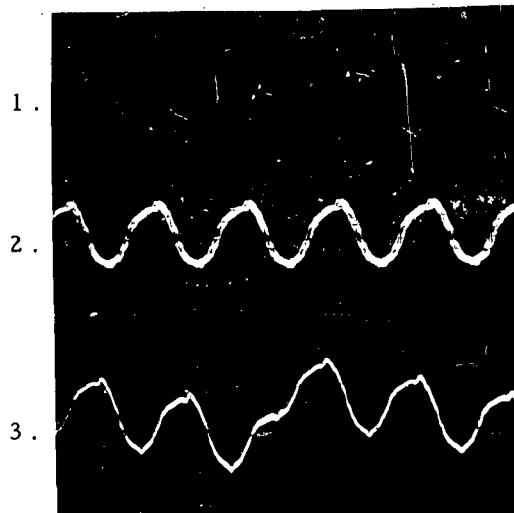


a. Direct Camera to Monitor



b. Encoded Video

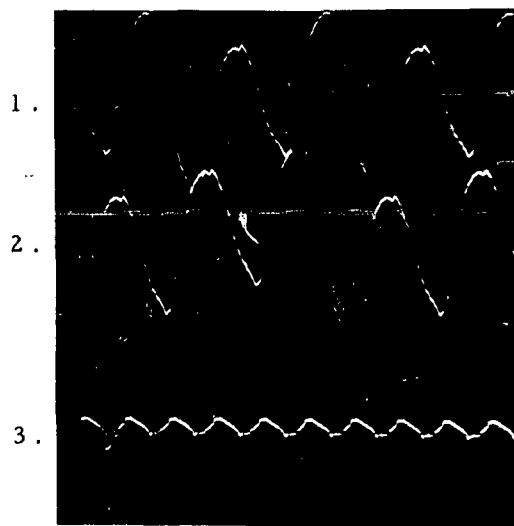
Figure 63 Encoded Video Display



A: 1. -100mv, 2. 0mv, 3. +100mv



B: 1. 150mv



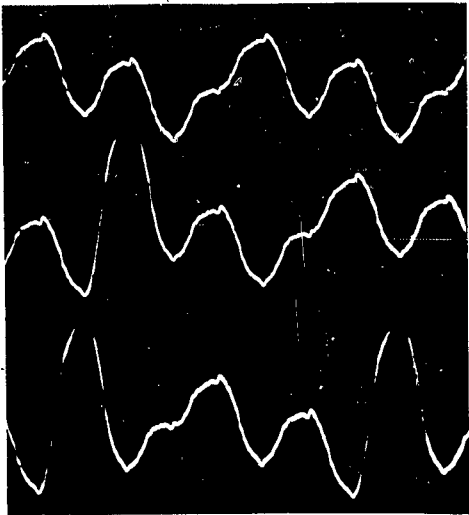
D: 1. 600mv, 2. 700mv, 3. 800mv



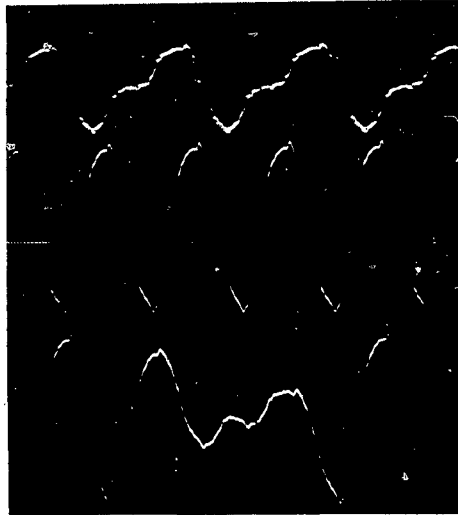
E: 1. 900mv

200mv/cm

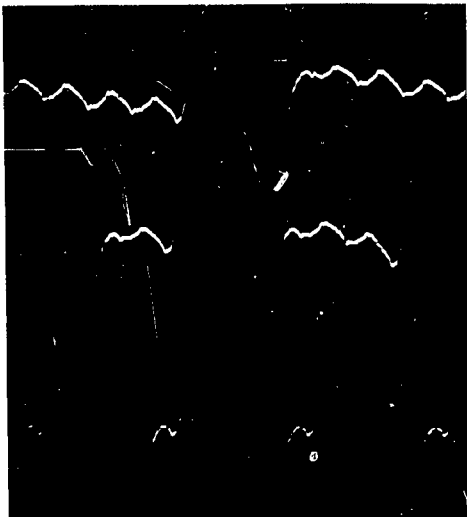
1



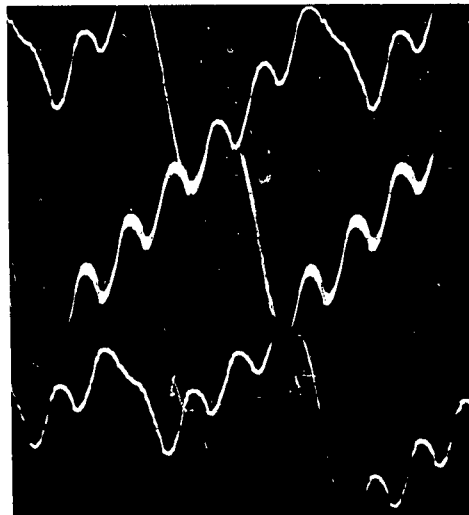
B: 1. 150mv, 2. 200mv, 3. 250mv



C: 1. 300mv, 2. 400mv, 3. 500mv



E: 1. 900mv, 2. 1.0v, 3. 1.1v



F: 1. 1.8v, 2. 1.9v, 3. 2.0v

200mv/cm at 100nsec/cm

Figure 64 Encoder Code Groups in Response to a DC Level Input



TABLE 10
SUMMARY OF KEY PARAMETERS OF CANDIDATE CODING TECHNIQUES

Coding Techniques	Relative Sampling Rate $N = \frac{\text{sampling rate}}{\text{analog BW}}$ (samples/cycle)	Bit Rate (N) $\left(\frac{\text{bits}}{\text{sample}} \right)$ = bits/cycle	Compression Normalized to 6-Bit PCM	Picture Quality			Number of Active Elements and Power Required in Encoder Normalized to 6-Bit PCM	Permissible Bit Error Rate	Data Link S/N Required for Differentially Coherent PSK Modulation (db)
				Step Response (10 - 90%) Normalized to 6-Bit PCM (units of time)	S/N Out for 5-Mc Input (db)	Maximum Amplitude of Oscillation Relative to Dynamic Range (%)	Natural Period of Osc. for BW max = 25 Mc (nsec)		
6-Bit PCM	2	12	1	1	Not Measured	0.0	0	0.01	6
2-Bit Δ Linear	2	4	3	3	14	6.25	40	0.0005	9
2-Bit Δ Exponential	2	4	3	4	12.3	11.0	40	0.004	7
1-Bit Δ Exponential	4	4	3	3.5	14.3	18.0	100	0.004	7
1-Bit Δ Linear	4	4	3	5	16.9	8.0	20	0.0005	9
1-Bit DWP	4	4	3	2.2	14	6.25	40	0.0001	10
2-Bit Δ Exponential	4	8	1.5	2	Not Measured	11.0	20	0.004	7

4. Referring to Table 10, the images in Figures 14, 15, 33, 35, and 36, and the previously mentioned conclusions, it is concluded that two-bit Delta Modulation employing an exponential integrator with a time constant of 3τ produces better images than all other Delta Modulation systems analyzed, considering (1) bandwidth reduction, (2) image quality, (3) susceptibility to data-link noise, (4) size, weight, and power, and (5) reliability and complexity.

5. It is further concluded that, depending on the application, a bandwidth compression of between 2 to 3:1 can be achieved by using Delta Modulation. Evidence of this conclusion can be visually verified by referring to the images for two-bit exponential Delta at 512 samples (Figure 35c), two-bit exponential Delta at 1024 samples (Figure 36c), and six-bit PCM at 512 samples (Figure 35a). The comparison of two-bit Delta at 512 with six-bit PCM (compression of 3:1) shows that nearly all information is retained by the Delta Modulation process. The comparison of two-bit Delta at 1024 with six-bit PCM (compression 1.5:1) shows that the Delta image actually has more information than the six-bit PCM because of the higher spatial sampling density. It is therefore reasonably concluded that an optimum compression between 2 to 3:1 can be achieved by Delta Modulation encoding such that no perceptible information is lost.

6. By referring to the waveforms of the performance of the Delta Modulation experimental model, Figures 18, 30, and 32, it is concluded that it is both feasible and practical (1) to sample video signals at 50 Mc, (2) to encode these samples to two-bit precision, and (3) to obtain a 100-megabit serial bit rate.

7. The final conclusion reached is that there is a direct correspondence between (1) the computer simulation images, (2) the graphical analysis, and (3) the performance waveforms of the two-bit, 100-megabit rate, Delta Modulation feasibility model. Typical of this correspondence is the period of oscillation for uniform-brightness areas, as can be observed in the enlarged black region of Figure 17h, the graphical plot of Figure 32b, and the test waveform of Figure 57. Notice that each has an identical period of oscillation. Therefore, the images obtained by computer simulation do, indeed, represent the actual performance of an operating equipment.

VIII. RECOMMENDATIONS FOR FUTURE WORK

As a result of the combined efforts under this contract, Philco recommends to the Air Force that the following areas be strongly considered for future work.

A. Delta Modulation Systems

Philco recommends that the study and evaluation of Delta Modulation techniques for pictorial coding and transmission be continued in the search for a better technique. In particular, it is felt that two relatively new techniques deserve immediate attention. The double integration with phase reversal system recently published seems to solve the basic problem of loss of high-frequency detail at low-sampling rates associated with the double-linear integration systems studied during Phase II of this contract. Although this technique was developed for use with speech where large overshooting can probably be tolerated, Philco feels that incorporating a prediction feature into the logic may make it readily adaptable for use with pictorial transmission systems. The second Delta Modulation technique, developed by Philco, is one which attempts to solve the problem of large-amplitude low-frequency oscillations in constant-brightness area associated with exponential integration. The system consists of two integrators operating in parallel. One is a linear integrator to provide small steps when the input is essentially dc; the other is an exponential integrator to provide large-amplitude increments necessary for large-amplitude changes in the input. The output of these two integrators are summed together to provide the feedback signal of the system. This linear-exponential (LEX) system seems to provide the advantages of both types of integrators, while, at the same time, the combination cancels some of their disadvantages. Further study using graphical plotting and computer simulation evaluation is strongly indicated for these two techniques.

B. Recognition Techniques

Philco believes that it is feasible to study and develop logics for recognizing areas of constant brightness or dc at the receiver of Delta Modulation systems. This is particularly applicable to exponential integration systems because there are definite and distinct code groups associated with various dc levels throughout the dynamic range. By recognizing these code groups and their length, the receiver could substitute the correct dc levels for these code groups. Such recognition techniques would be of significant value for removing objectionable oscillations from exponential systems, as well as other Delta Modulation systems.

C. Feedback Loop Delay

Construction of implementation circuitry has brought to light a problem associated with the delay in the feedback loop of the Delta Modulator. At the high sampling rates required by systems handling high bandwidth input signals, the tolerable delay associated with the integration process in the feedback loop becomes prohibitively small. It is indeed questionable if such short delays can be practically realized in an equipment. Preliminary thoughts concerning the problem lead one to the unsupported conclusion that multibit systems would be superior to one-bit systems at the same bit rate because of the lower sampling rate (and, consequently, a longer tolerable delay) required by the multibit systems. It is recommended that this problem of feedback delay be thoroughly investigated for video bandwidths above 25 Mc in terms of sampling rate, bit rate, and equipment feasibility and complexity.

D. Second-Order Statistics

Philco believes that further savings in bandwidth reduction and better image fidelity may be accomplished with Delta Modulation systems by using the second-order statistics of the input-image data. If the feedback signal subtracted from the input depended not upon the previous output but upon the two previous outputs, the output of the integrator would follow the input with less error. Such a system would have incorporated in the feedback loop a prediction circuit which would determine a signal value dependent upon the two past outputs of the integrator. This might be accomplished by slope prediction. Philco recommends that such systems be studied and evaluated by the use of computer simulation to determine their feasibility for pictorial coding and transmission.

E. Comparison of Pictorial Coding Techniques

Delta Modulation is but one of the techniques for reducing redundancy in pictorial data. Other techniques such as PCM-Pseudorandom Noise, Split-Band Quantization and Dual-Mode Coding will yield bandwidth compression ratios similar to Delta Modulation with similar equipment complexity. Philco recommends that a unified analysis and computer simulation be conducted to determine the comparative performance of the above techniques including Delta Modulation in terms of bandwidth reduction, image reproduction, sensitivity to noise, and implementation complexity.

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APPENDIX I

COMPUTER SIMULATION OF ONE-BIT DOUBLE INTEGRATION WITH PREDICTION

During the advanced study phase of this contract, a computer program was written to simulate the one-bit double integration with prediction Delta Modulation system (DIWP). A block diagram of this system is shown in Figure I-1 showing the encoder, decoder, and noisy data link. Shown in Figure I-2 is a flow diagram of the computer program. A correspondence can be drawn between Figures I-1 and I-2 on a block-for-block basis. The following is a description of the program.

At the start of the program, the input tape containing the IMITAC-scanned image data in binary form is read into the computer memory. The program indexing command picks the proper signal value and the encoding process begins. The predicted signal value, V_{pn} , is subtracted from the analog input signal value to determine the quantizer input signal, e_n . The initial value of the predicted signal, V_{po} , is set at one-half the maximum value obtainable by the input signal. At the start of each scan line of data, V_{pn} is reset to this value. The quantizer tests e_n for polarity to determine the one-bit binary code for transmission over the data link. This code is also decoded into positive and negative pulses for input to the first linear integrator. The integrator is represented by a running counter. A positive or negative pulse causes a "1" to be added to or subtracted from the counter. This count is amplified and becomes C_n , the staircase input to the second integrator. The output of the second integrator becomes

$$V_n = SC_n + V_{n-1} \quad (I-1)$$

where S is the initial slope or increment added to the output for a count of plus or minus one. The sequence of values represented by V_n is the output image without data-link noise added, since the encoder and decoder double integrators are identical. In a practical system, however, it is not necessary that values of V_n be generated in the encoder because only the predicted signal is used for the encoding process. The value V_n is subtracted from the input signal from which this output was generated to form an error signal E_n , which, later in the program, is used to generate an error signal image. Also, this error signal value is used for signal-to-noise ratio calculations.

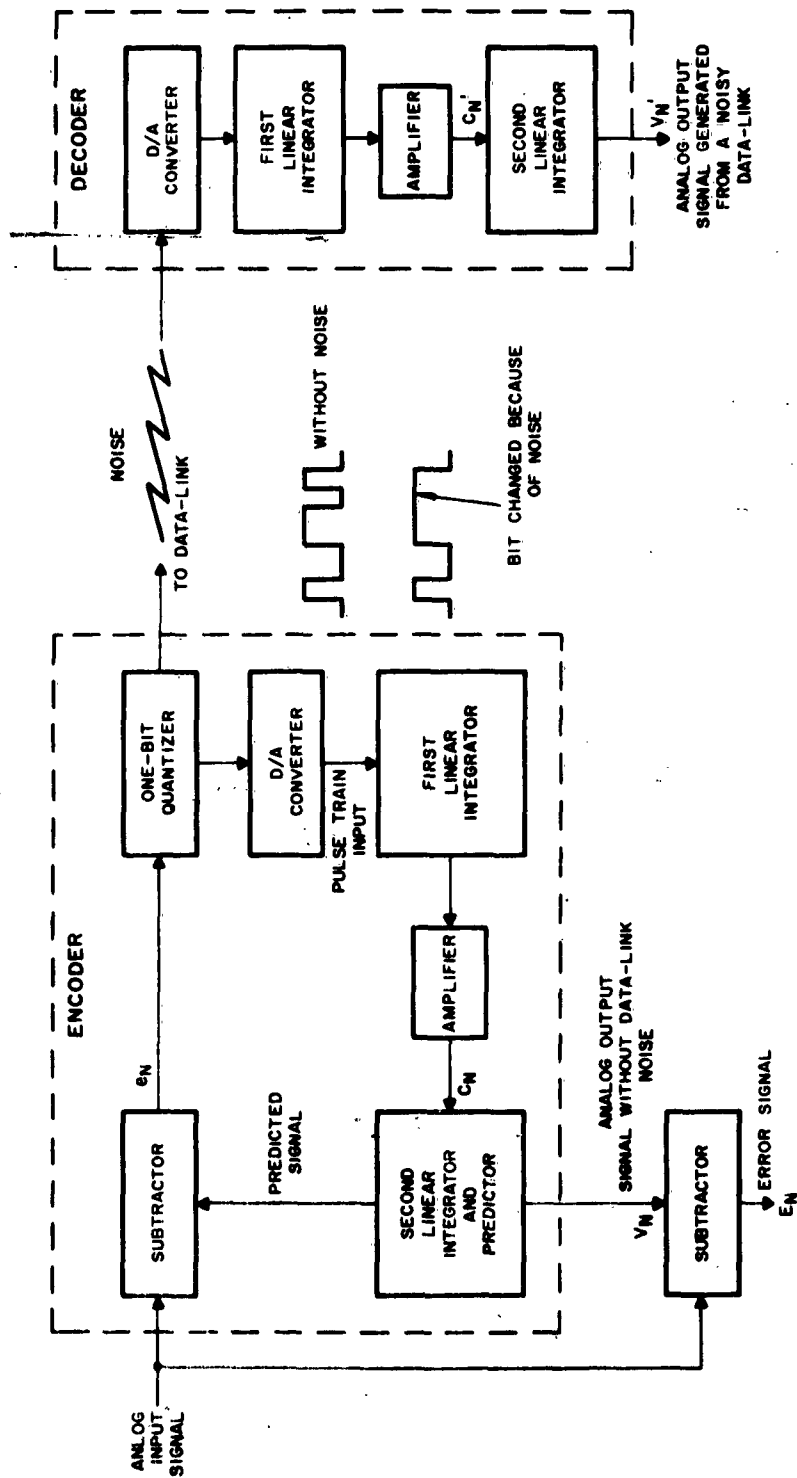


Figure I-1 DIWP Delta Modulation System Simulation Including the Effects of Data-Link Noise

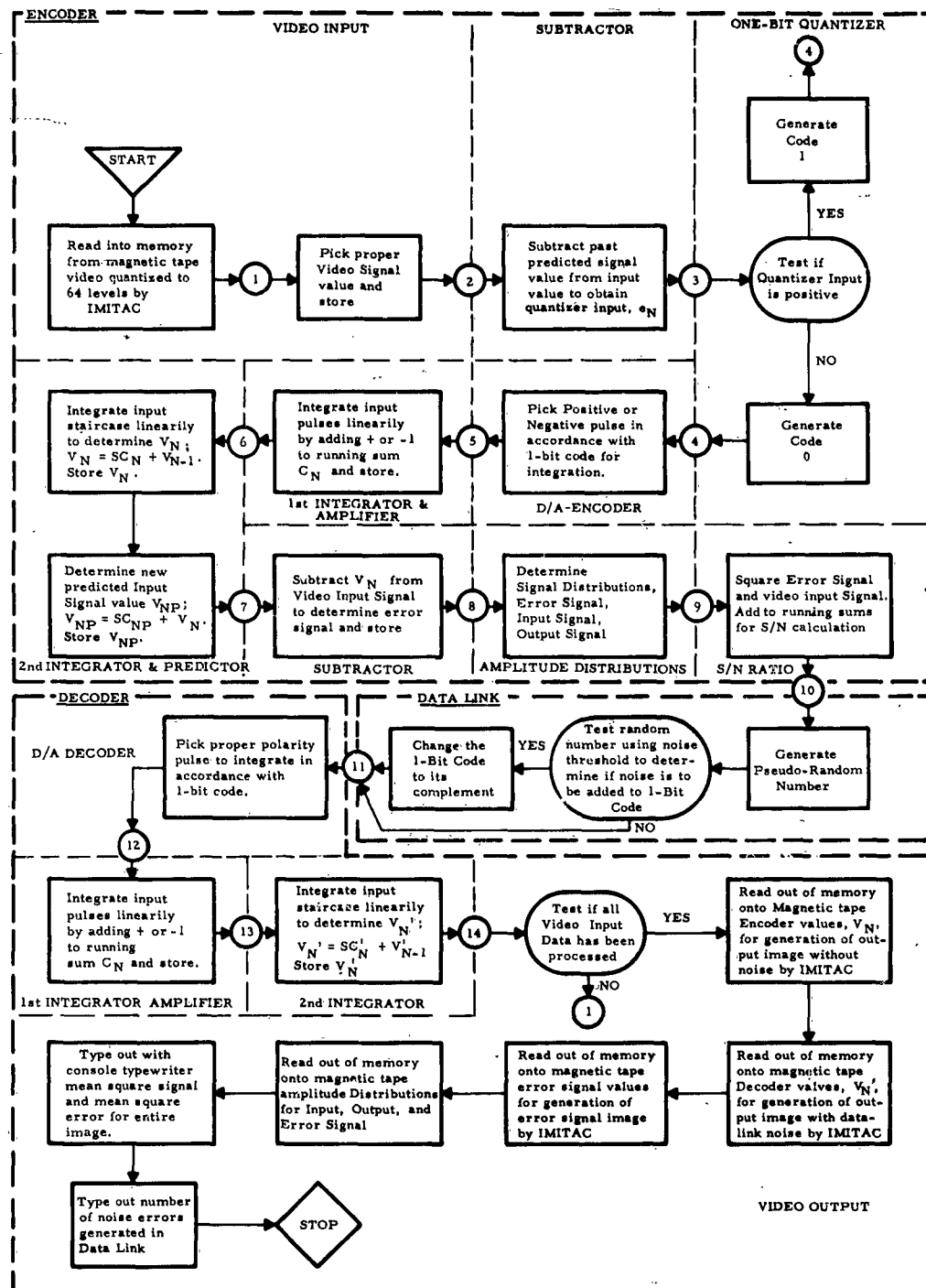


Figure I-2 Block Diagram of the Computer Program to Simulate a One-Bit Double Integration with Prediction Delta Modulation System

The predicted signal is also calculated by the second integrator from the equation

$$V_{pn} = SC_n P + V_n \quad (I-2)$$

where P is the prediction interval specified as a number of sample periods. V_{pn} is stored for future use with the next video input signal.

At this point, amplitude distributions are calculated by the program. Set aside in the computer are a number of memory locations or "bins" corresponding to all possible values that the signal in question can have. As an example, the input video signal can have any one of 64 different values (0 through 63). Sixty four "bins" are reserved for the input signal amplitude distribution. A "1" is added to the proper bin, depending upon the value of the input-signal sample. At the end of the computer program, the "0" bin would contain a number equal to the total number of signal samples equal to zero in the input image and, correspondingly, for all other bins. These 64 numbers can be plotted versus the corresponding signal values to obtain the distribution. Similar distributions are calculated for the output-signal image without data-link noise and the error-signal image.

Provision has been made to calculate mean-square-signal and mean-square-error values. The input signal value is squared and added to a running sum. At the end of the program, the mean-square signal (MSS) is calculated from the following equation

$$MSS = \frac{1}{M} \sum_{n=1}^M V_{In}^2 \quad (I-3)$$

where V_{In} are the input signal values and M is the total number of samples in the image. Correspondingly, for the mean square error (MSE)

$$MSE = \frac{1}{M} \sum_{n=1}^M E_n^2 \quad (I-4)$$

The output signal-to-noise ratio is, then,

$$S/N_{OUT} = \frac{MSS}{MSE} \quad (I-5)$$

The values of MSS and MSE are typed out by the console typewriter at the end of the program run after all M samples have been processed.

After calculating V_n and V_{pn} , the distributions, and MSE and MSS, the program enters the data link and a decision is made as to whether or not noise is to be added to the one-bit code. A pseudorandom number generated by a Philco preprogrammed subroutine called RAND1* is compared with a preset noise threshold and the noise decision is made. From this point two paths are provided. In the noise path the code is changed to its complement and the sign of the pulse is changed. Double integration takes place in the decoder and the values of V_n' , the output signal with data-link noise, are calculated from the equation

$$V_n' = SC_n' + V_{n-1}' \quad (I-6)$$

where the prime indicates values in the decoder. If the data link were noise-free, this equation would be identical with Equation I-1, the corresponding one in the encoder.

The program, up to this point, has processed one input signal value. A test is made to determine if all input signal values have been processed. If they have not, the indexing portion jumps back to the beginning and picks up the next sample. Processing begins once again. When all processing is done, that is, all M samples have been encoded and decoded, the output values are placed on magnetic tape in binary form or are typed out on the console typewriter in decimal form. Three images are generated: the values of V_n , V_n' , and E_n . These images are obtained by using IMITAC to convert the digital signal on tape to an analog signal on the sheet or polaroid film. A fourth output tape contains the amplitude distributions which are printed out in decimal form using Philco's High-Speed Printer. The console typewriter types out the number of noise errors generated in the data link and MSS and MSE.

The program has been written so that the one-bit DIWP parameters may be varied. These variables include the initial slope, S; the prediction interval, P; the horizontal and vertical sampling rates; and the data-link noise threshold. Also, it is possible to run the program without data-link noise added, without MSS and MSE, without the amplitude distributions, and without the error-signal image. Average program running time is 17 minutes.

* The Subroutine RAND1, Catalog Number SMK1 dated May 8, 1959, Philco Corporation, Computer Division, Marketing Services

APPENDIX II

IMITAC

A. Introduction

IMITAC (Image Input To Automatic Computer) is an input-output device for the Philco 2000 computer capable of transferring image data to magnetic tape for use in simulating image processing logics. (This process is referred to as the READ mode in this appendix). IMITAC is also capable of the reverse process of transferring simulation results from magnetic tape to image form on photographic film (called the WRITE mode in this appendix). Furthermore, in addition to the straightforward transducer functions described above, IMITAC is capable of elementary processing such as spatial filtering and level slicing.

In its basic mode of operation, IMITAC scans a photograph, samples the resulting analog voltage at each of as many as 10^6 elemental positions, quantizes these samples into as many as 64 levels, and then transforms the quantized sample into a six-bit binary code suitable for the 2000 computer. The analog voltage is sampled at a 20-Kc rate; the total time to sample 10^6 positions and transfer the data to magnetic tape via the 2000 Universal Buffer Controller (UBC) is 70 seconds.

B. Description of IMITAC

As shown in the block diagram of Figure II-1, the two basic IMITAC components are the flying-spot scanner and the control logic. These operate in conjunction with the Universal Buffer Controller (UBC) and Magnetic Tape Transport (MTT), which are satellite devices of the Philco 2000 Computer.

The UBC provides temporary storage of information being transmitted in either direction between any two input-output units of the Philco 2000 system. In this case, it transmits data between IMITAC and the MTT at speeds and formats compatible with each unit.

A photographic transparency is scanned (READ mode) by the flying-spot of the IMITAC CRT, and the transmitted light is collected and fed to a phototube shunted by a nonlinear diode which produces a video signal inversely proportional to the density of the transparency. This logarithmic READ characteristic gives equal weight to equal density differences, thus matching data processing to the logarithmic characteristic of the eye. Thus, noise or spurious effects such as contouring introduced during simulations will appear uniform to the eye over the entire range of image gray shades.

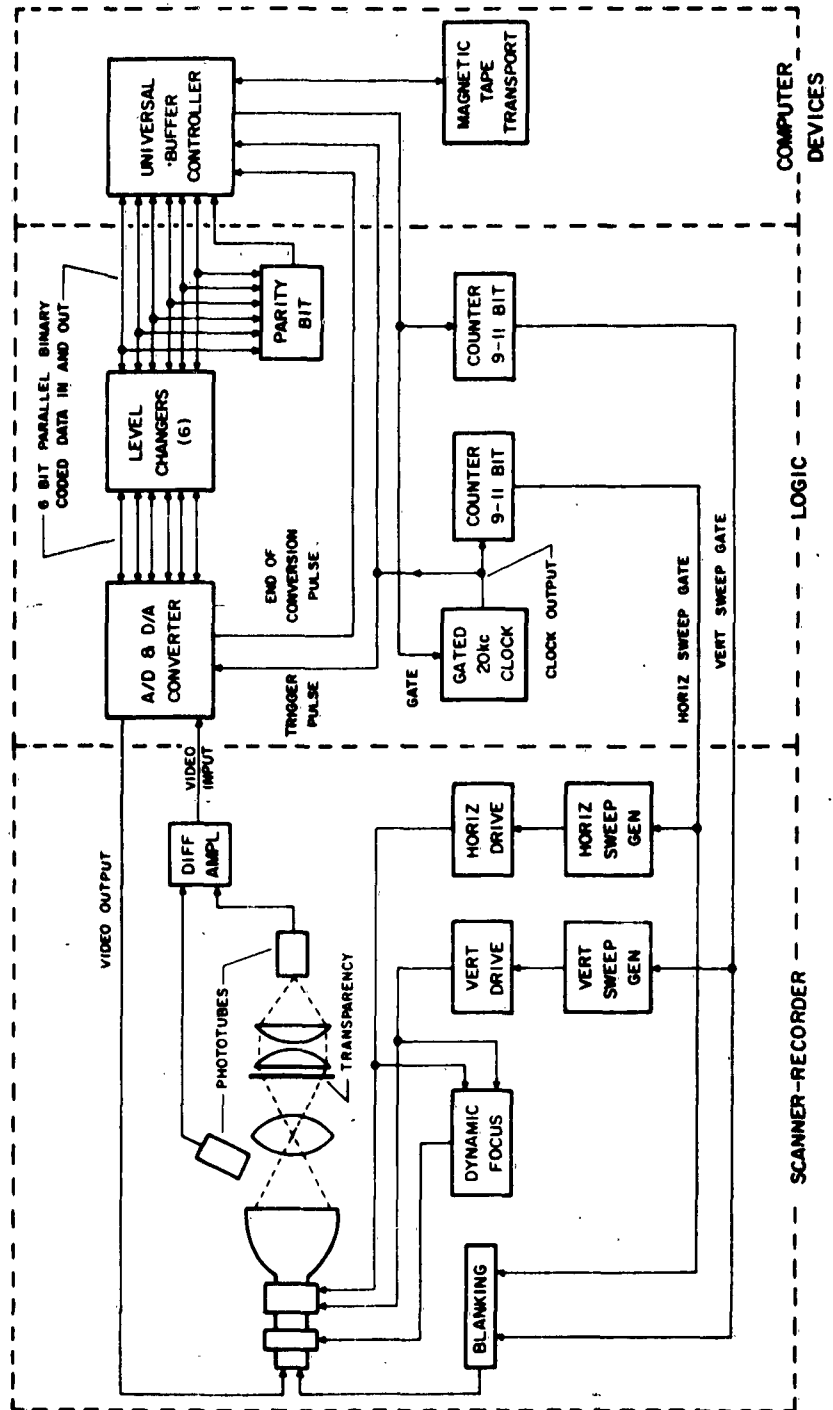


FIGURE II-1 BLOCK DIAGRAM OF IMITAC SYSTEM

The use of a logarithmic characteristic provides two system benefits, viz., it compensates the nonlinearity of the CRT transfer characteristic in the Write Mode and allows simple, automatic cancellation of CRT phosphor grain noise over the entire range of image gray shades during the Read Mode.

Noise produced by CRT phosphor grain is cancelled from the video signal by subtracting the logarithm of the output of a special photomultiplier (which directly views the CRT) from the logarithm of the video.*

The video is converted to a six-bit binary signal (64 levels) which is suitable for storage on Philco 2000 magnetic tape via the Universal Buffer Controller (UBC). The UBC has a magnetic core storage which is loaded one block at a time at IMITAC speed and unloaded onto magnetic tape a block at a time at computer speed. Each IMITAC scan line is recorded in a separate magnetic tape block. IMITAC generates parity check bits required for 2000 computer operation and also the proper control signals for interlock with the UBC.

Directly coupled dynamic focus circuits counteract the off-axis defocus due to the geometry of the electron optics, thus providing optimum focus over the entire scan-raster area.

Off-Axis "pincushion" distortion of the scan raster due to the geometry of electron optics is corrected by a special coil assembly attached to the deflection yoke:

C. IMITAC Characteristics

1. General

The input to IMITAC consists of an image on a 4- x 5-inch glass plate which provides a rigid surface for the emulsion. Image size is nominally

* The signal reaching the main photomultiplier is of the form SN , where

S = amplitude variation due to slide opacity,
 N = amplitude variation due to phosphor noise.

Cancellation is as follows:

$$\begin{aligned}\text{Output} &= \log SN - \log N, \\ &= \log \frac{SN}{N}, \\ &= \log S.\end{aligned}$$

3 x 3 inches. The number of scan lines can be either 256, 512, or 1024. The size of the raster imaged on the glass slide is kept constant as the number of scan lines is changed. In addition, the number of sample points can also be varied. At the present time, the combinations of sample points and scan lines that can be obtained are shown in Table II-1.

TABLE II-1

IMITAC SAMPLING PATTERNS

Sample Points	Scan Lines	Total Picture Elements
1024	1024	1,048,576
1024	512	524,288
512	512	262,144
256	256	65,536

2. System Frequency Response

The major factor which determines system resolution is the size of the CRT spot when it is imaged on the input photo.* The size of the scanning spot can be changed by changing either optical or CRT-spot focus. The method of adjusting spot size is to scan a special rectangular bar test chart (see Figure II-2) and plot a curve of video amplitude versus line spacing. Focus is adjusted until the point on the curve which is down 3 db occurs at the desired line spacing. Figure II-3 shows a typical curve taken in the READ mode of operation in which the 3-db point has been adjusted to 512 lines per raster. The ultimate capability of IMITAC is a 3-db point at 1024 lines per raster.

A similar curve could be obtained in the WRITE mode by printing out a special test tape containing binary data representing the pattern on the READ test chart. Microdensitometer measurements of this photo would yield a WRITE Resolution Response Curve.

* The band limiting effect of the phosphor time constant (1.4 μ sec for P24 phosphor) is negligible compared with the 50 μ sec sampling interval. Also, the video amplifiers are wideband compared with the 10 kc maximum video rate; thus, they produce no degradation of the video waveform.

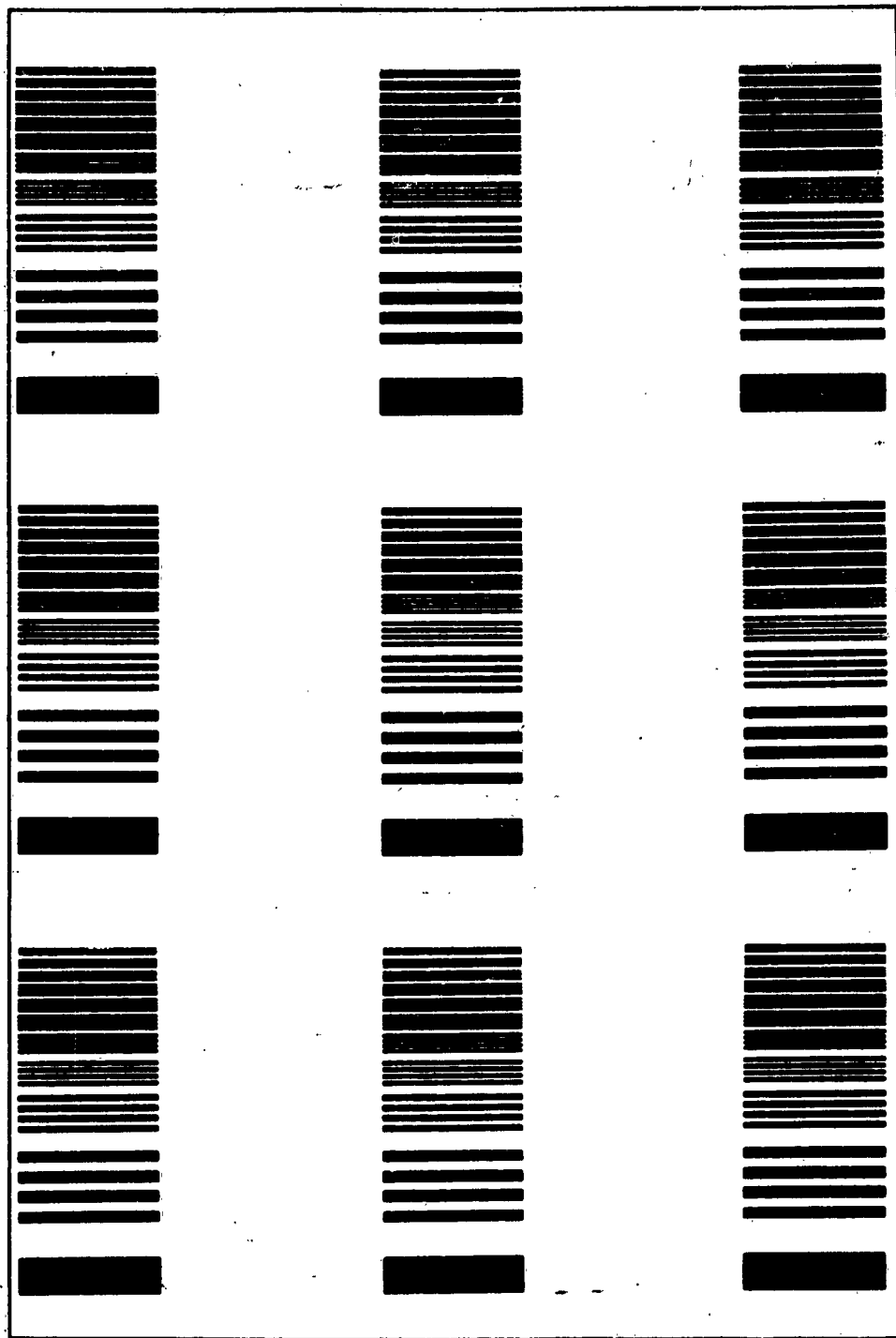


FIGURE II-2 WESTINGHOUSE RESOLUTION CHART

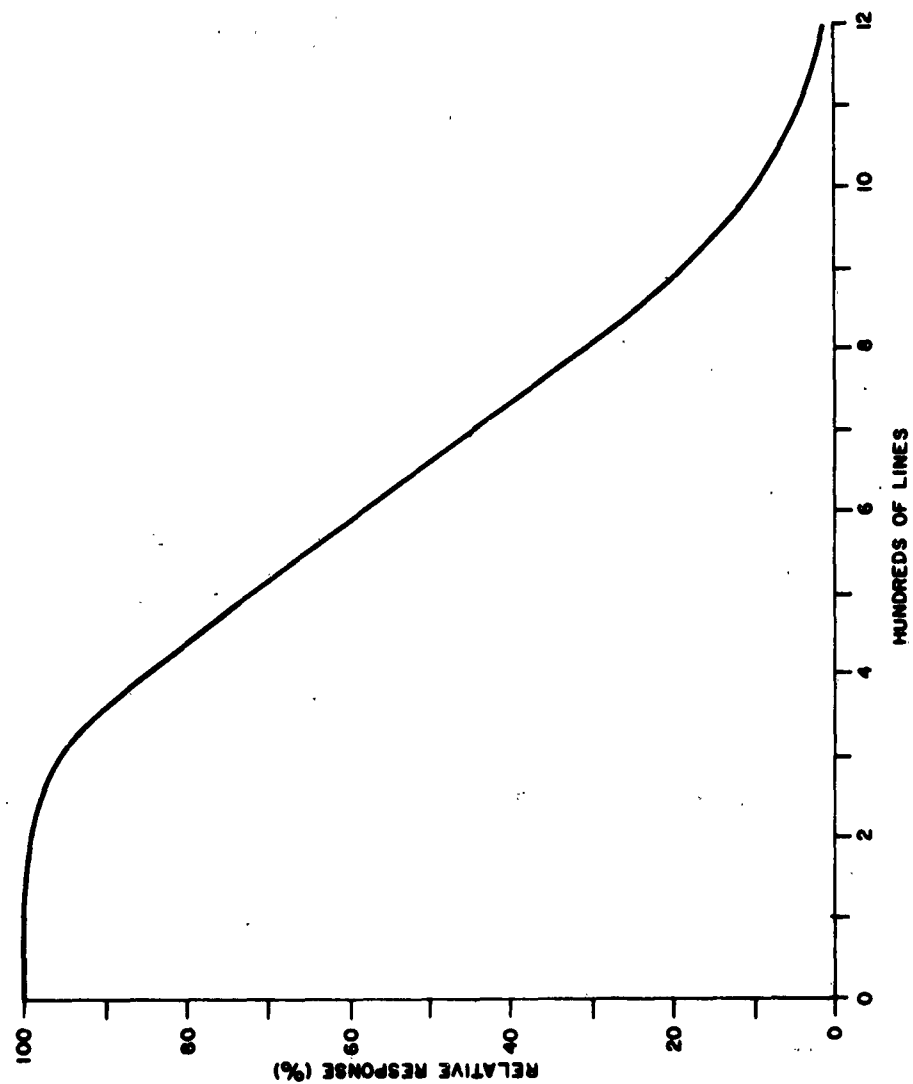


FIGURE II-3 TYPICAL IMITAC "READ" RESPONSE TO WESTINGHOUSE CHART

The resolving powers of the photographic materials used in IMITAC are shown in Table II-2.

TABLE II-2
PHOTOGRAPHIC MATERIALS USED IN IMITAC

Material	Use	Resolving Power		Spatial Frequency at 3-db Point
		Line Pairs per mm	Lines per 3-inch Raster	
4"x5" Continuous Tone Glass Photo- graphic Plate	Input image	75-90	11,000 to 13,500	
Polaroid Film	Output check print (positive)	30	4,500	
4"x5" Sheet Film	Output negative	75-90	11,000 to 13,500	4572 lines/raster

3. System Transfer Function

Figure II-4, the READ Transfer Characteristic, is a curve of video voltage into the analog-to-digital converter versus the density of a gray-scale test photograph. The log diode in the IMITAC video amplifier should cause this voltage-density curve to be a straight line. The curvature of the line is due to stray light effects, in particular the halo surrounding the CRT spot. The straight curve of Figure II-4 was obtained by artificially eliminating most of the stray light by masking all but a small slit surrounding the bar chart on the test slide. Because this artifice cannot be utilized in an actual raster scan, operation is restricted to the nearly linear portion of the curve between subject densities of 0 and 1.0.

Figure II-5, the WRITE Characteristic, shows a nearly linear relationship between the log of CRT brightness and voltage out of the digital-to-analog converter. (This relationship is due to the nonlinearity of the CRT transfer characteristic.) Fortunately, most films have a linear density versus log exposure characteristic; therefore, it is merely necessary to adjust the

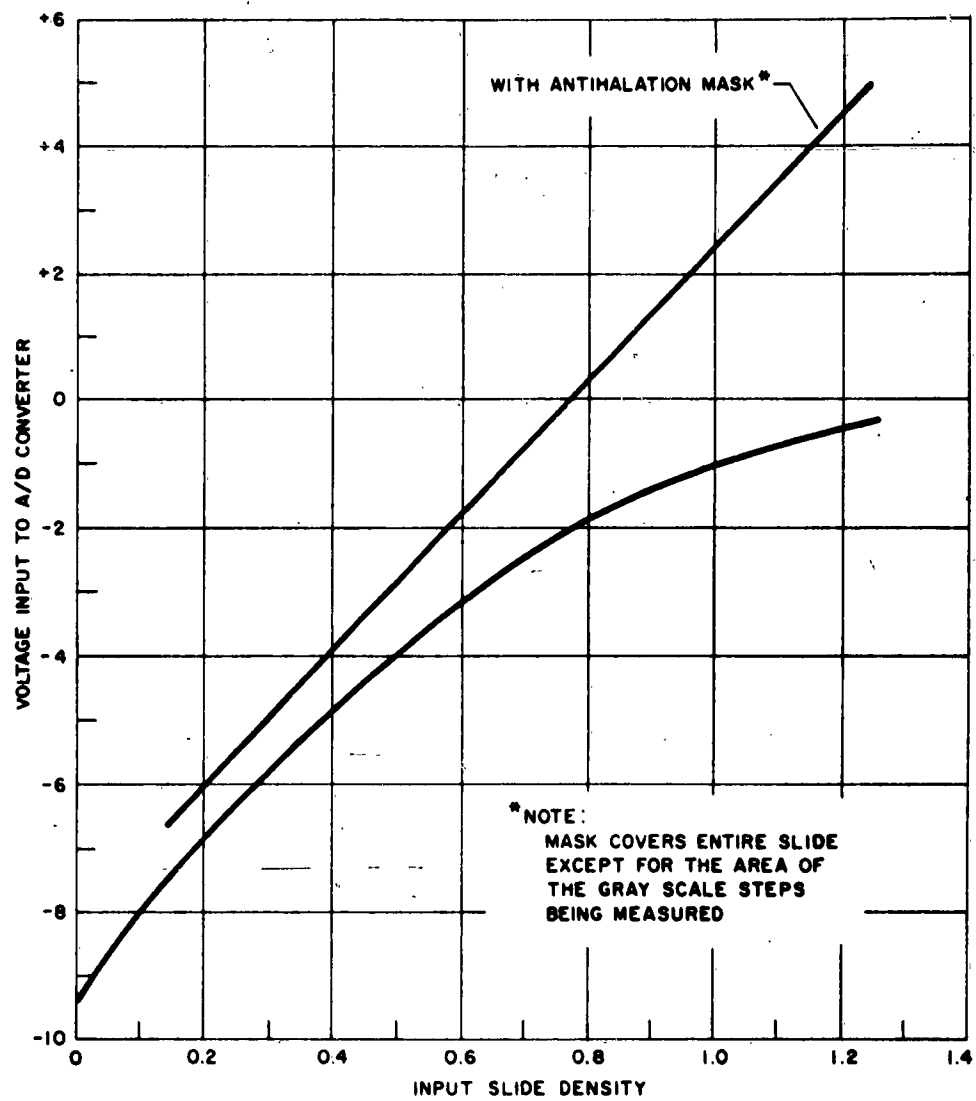


FIGURE II-4 IMITAC "READ" TRANSFER CHARACTERISTIC

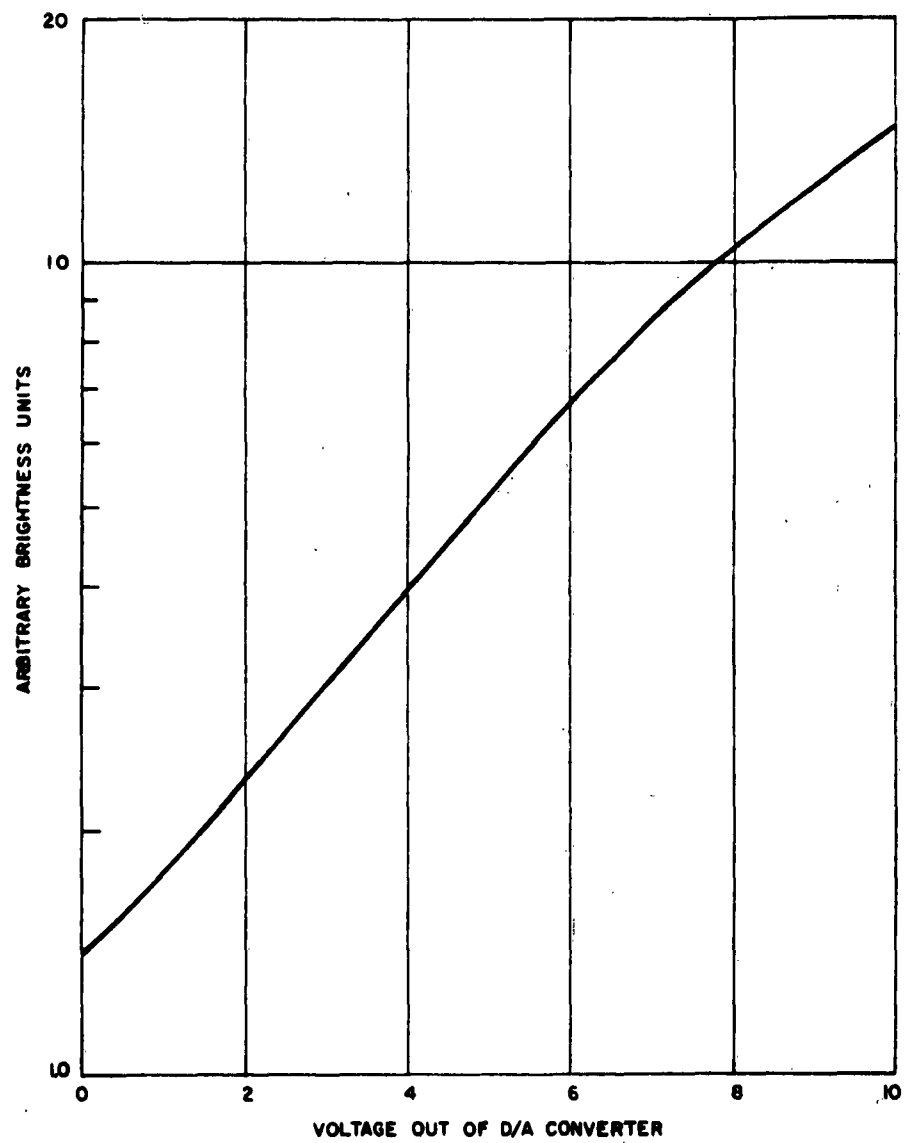


FIGURE II-5 IMITAC "WRITE" TRANSFER CHARACTERISTIC

amount of light transmitted through the optical system to match the linear region of the recording film. (See Figures II-6 and II-7 for exposure curves for two films used in IMITAC.)

The net result of combining all the above transfer characteristics is the over-all transfer characteristic shown in Figure II-8. This shows that the density of the 4" x 5" sheet film negative is a linear function of the density of test bars on the continuous-tone photographic glass plate positive input slide. Also shown is a similar linear curve for a print made from the 4" x 5" sheet film negative.

D. Auxiliary IMITAC Features

One auxiliary feature of IMITAC is the ability to short out individual bit channels when operating in the WRITE mode. Six switches permit the removal of any combination of bits. One use for this feature is the simulation of 6-, 5-, 4-, 3-, 2-, or 1-bit PCM using a single 6-bit input tape.

Another use for this feature is to provide a threshold for making decisions in special simulations.

In addition to the components shown in Figure II-1, the components and connections which enable the extraction of simple features from the photograph as it is scanned have been added. These consist of a beam splitter which produces a second optical channel from the transparency to a new photomultiplier, a special aperture consisting of two-color transparent filters in the objective-lens plane, and circuitry for the second channel. In combination, these components enable the generation of a video signal that represents scanning by an aperture of arbitrarily adjustable shape and with both positively and negatively weighted areas. This signal is processed by a threshold amplifier. An output from this amplifier indicates the detection of a feature defined by the aperture shape.

For the detection of straight-line segments, the aperture consists of two adjacent rectangular slits. Each slit (or bar) consists of a different colored optical filter. The filter colors are separated sufficiently in wavelength to prevent crosstalk. Each of two photomultiplier tubes covered with corresponding filters receives the light energy passing through one of the aperture slits. The logarithms of the outputs of the photomultiplier tubes are generated by nonlinear diodes across the phototube outputs. The two outputs are weighted, one positively and the other negatively, and then added to produce the ratio of the densities of two small adjacent areas of the original transparency enclosed by the composite slit. When the density of the transparency being traversed is uniform, the output ratio is unity. (Unity output is considered zero signal.) When the boundary

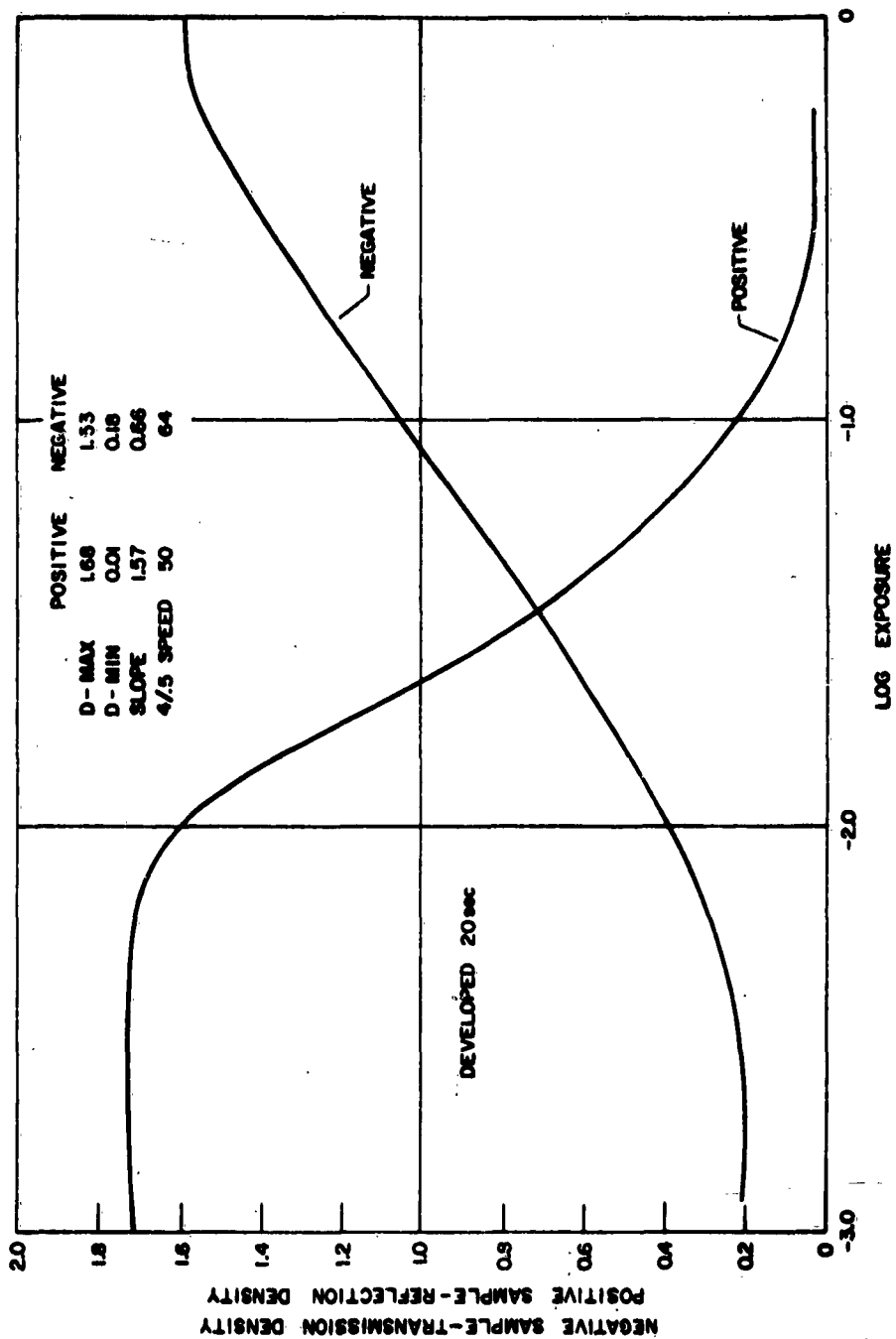


FIGURE II-6 EXPOSURE CURVES FOR TYPICAL POLAROID LAND FILM PACKETS

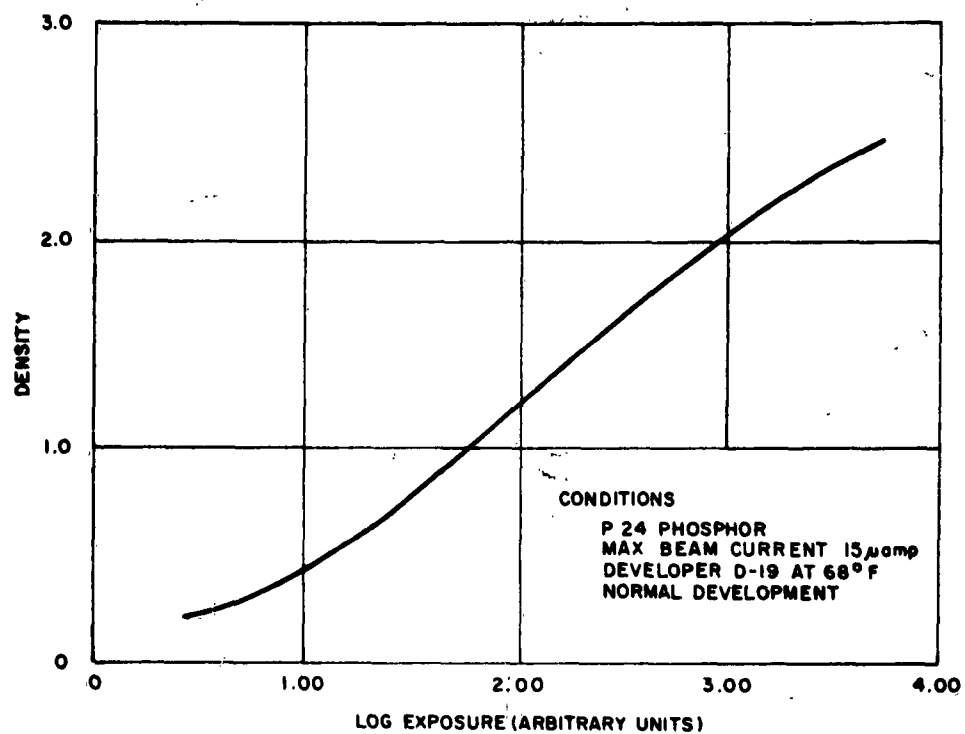


FIGURE II-7 EXPOSURE CURVE FOR 4" x 5" SHEET FILM

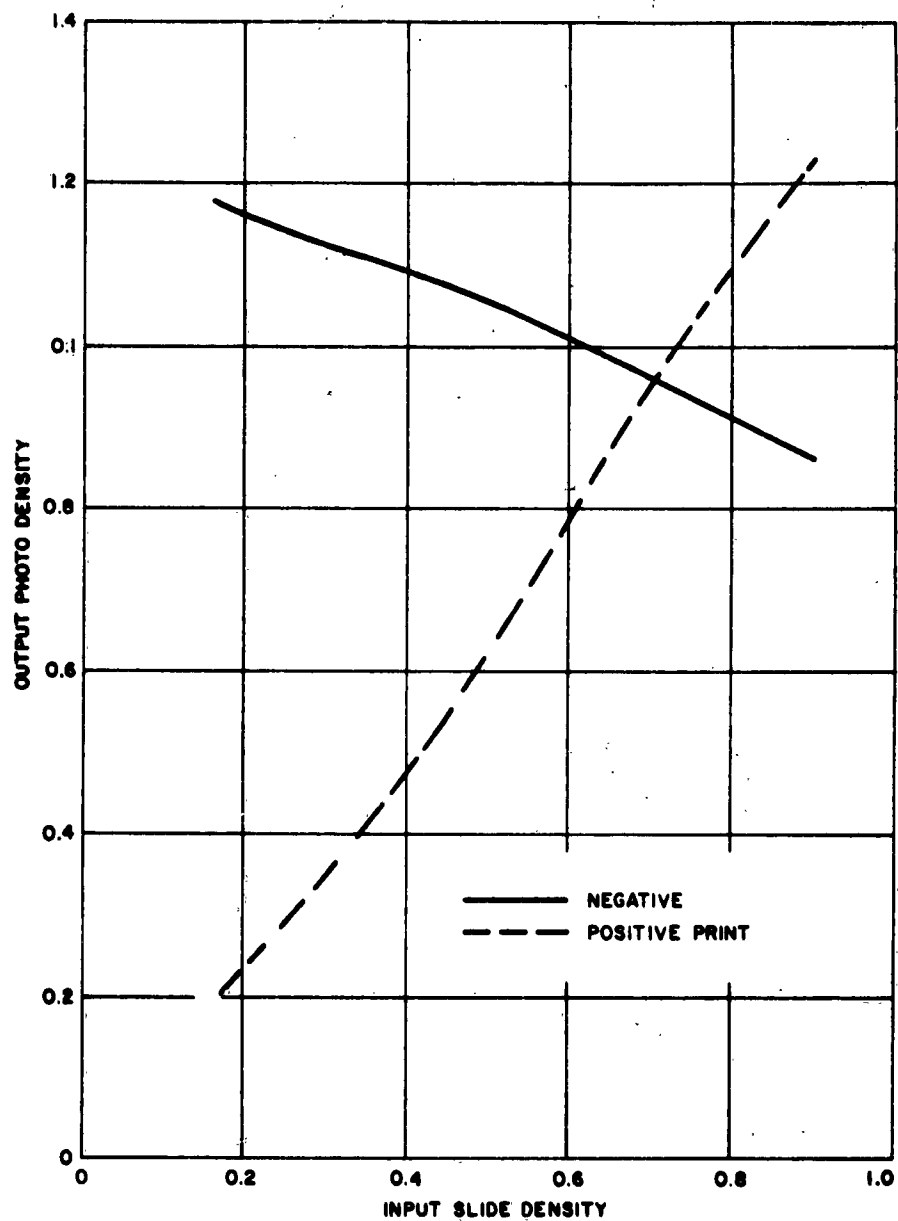


FIGURE II-8 OVERALL IMITAC TRANSFER CHARACTERISTICS

between two different densities is scanned and the boundary is parallel to the composite slit there is a maximum output signal. Thus, the slit-aperture arrangement "detects" density changes whose boundaries are parallel or nearly parallel to the slit. As the angle of the density transitions changes from 0 to 90 degrees with respect to the slit, the output drops from a maximum to a minimum.

A concentric ring aperture also has been used to detect gradients without regard to their direction.

Aeronautical Systems Division, AF Avionics Laboratory, Electronic Warfare Division, Wright-Patterson AFB, Ohio. Rpt AF ASD-TDR-63-528, DEMONSTRATION OF THE FEASIBILITY OF USING DELTA MODULATION FOR PICTORIAL TRANSMISSION, final technical report, May 1963, 161 p. Incl. illus., tables, 39 refs. Unclassified Report An extensive investigation of Delta Modulation techniques for encoding pictorial data was made to determine the parameters of Delta Modulation systems for various image communication applications by (1) system analysis, (2) computer simulation, and (3) experimentation. The analysis and computer simulation included one-bit and two-bit systems with linear integration, double linear integration with prediction, and exponential integration. Fifteen different Delta Modulation encoding logics were simulated during the program. Most importantly, the performance of these logics, as well as that of PCM, in the presence of data-link noise has been simulated and evaluated. Images of all these simulations are presented for evaluation. A feasibility model of a 25-Mc two-bit exponential integration Delta Modulation encoding and decoding system with a serial bit rate of 100 Mbps was designed, constructed, and tested. A table of the key parameters of PCM and Delta Modulation encoding systems, based upon the analysis, simulation, and implementation, is presented. Using this table and the images, the image communication system designer can choose the best technique and combination of parameters to fulfill his particular application. It is concluded that for a typical image communication system, two-bit Delta Modulation with exponential integration and sampling at two to three times the information bandwidth represents the best compromise of parameters. The resultant compaction over six-bit PCM is two to three. Unclassified Abstract	UNCLASSIFIED 1. Digital communications 2. Delta modulation 3. Facsimile transmission I. AFSC Project 4335, Task 433521 II. Contract AF 33(657)-8478 III. Philips Corporation Advanced Technology Laboratory, Blue Bell, Pennsylvania IV. R. V. Cotton, G. R. Strohmeyer, A. F. Tillman V. R. D. Vernon VI. Philco Nr V040-F VII. Not avail fr OTS VIII. In ASTIA collection	UNCLASSIFIED 1. Digital communications 2. Delta modulation 3. Facsimile transmission I. AFSC Project 4335, Task 433521 II. Contract AF 33(657)-8478 III. Philips Corporation Advanced Technology Laboratory, Blue Bell, Pennsylvania IV. R. V. Cotton, G. R. Strohmeyer, A. F. Tillman V. R. D. Vernon VI. Philco Nr V040-F VII. Not avail fr OTS VIII. In ASTIA collection	Aeronautical Systems Division, AF Avionics Laboratory, Electronic Warfare Division, Wright-Patterson AFB, Ohio. Rpt AF ASD-TDR-63-528, DEMONSTRATION OF THE FEASIBILITY OF USING DELTA MODULATION FOR PICTORIAL TRANSMISSION, final technical report, May 1963, 161 p. Incl. illus., tables, 39 refs. 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R. Strohmeyer, A. F. Tillman V. R. D. Vernon VI. Philco Nr V040-F VII. Not avail fr OTS VIII. In ASTIA collection
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