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Aeronautical Electronic and Electrical Laboratory

REPORT NO. NADC-EL-6319 5 JUN 1963

LL -NOTES NO. 3

INFORMATION ON MICROELECTRONICS
FOR NAVY AVIONICS EQUIPMENT

WEPTASK NO. RAV03J002/2021/R008-03-01
Problem No. 14

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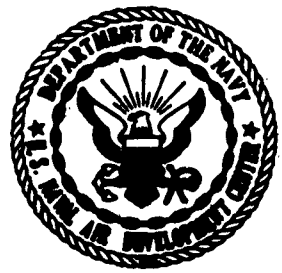


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# U. S. NAVAL AIR DEVELOPMENT CENTER
## JOHNSVILLE, PENNSYLVANIA

Aeronautical Electronic and Electrical Laboratory

REPORT NO. NADC-EL-6319 - $\mu$-NOTES NO. 3

INFORMATION ON MICROELECTRONICS FOR NAVY AVIONICS EQUIPMENT

WEPTASK NO. RAVO3J002/2021/R008-03-01
Problem No. 14

5 June 1963

The U. S. Naval Air Development Center has been designated as evaluation activity and information source for the Avionics Branch of the Bureau of Naval Weapons in the field of integrated electronic circuit assemblies. The directive[1] indicated that the Center should publish a monthly newsletter about the results of pertinent evaluations and general information on microelectronics.

The purpose of the newsletter (microminiaturized to $\mu$-NOTES) is to promote the application of microelectronics in avionics equipment from technical information on evaluation, application, research and development, availability of microelectronic hardware, and standardization activities. Comments and suggestions are invited by addressing them to Commanding Officer, U. S. Naval Air Development Center, Johnsville, Pennsylvania; Attention: EL-56

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1. *BUWEPS ltr RAAV-111:MCS of 29 Jun 1962*

# TABLE OF CONTENTS


| | Page |
|---|---|
| LIST OF FIGURES | ii |
| PRODUCT LIST | 1 |
| STANDARDIZATION | 1 |
| RESEARCH AND DEVELOPMENT | 2 |
| EVALUATION | 3 |
| Signetics Logic Elements | 3 |
| RCA DMC-100 Digital Microcircuit Logic Element | 8 |
| Pacific Semiconductors Microcircuit Logic Elements | 9 |
| TEST RESULTS FOR SIGNETICS CORPORATION LOGIC ELEMENTS | 12 |
| TEST RESULTS FOR RCA DMC-100 DIGITAL MICROCIRCUIT ELEMENT | 66 |
| TEST RESULTS FOR PACIFIC SEMICONDUCTORS MICROCIRCUIT LOGIC ELEMENTS | 77 |
| APPENDIX A - "Handbook - Preferred Microelectronic Functions, Navy Aeronautical Electronic Equipment," Battelle Memorial Institute | A-1 |

# LIST OF FIGURES


| Figure | Title | Page |
|---|---|---|
| 1 | Schematic - SE100T DTL NAND/NOR Gate. . . . . | 4 |
| 2 | Schematic - SE200T TTL NAND/NOR Gate. . . . . | 5 |
| 3a | Schematic - SE120T DTL Binary Element . . . . . | 6 |
| 3b | Load Lines for Transistors - SE120T DTL Binary Element . . . . . | 7 |
| 4 | Schematic - RCA DMC-100 Digital Microcircuit. . . | 8 |
| 5 | DMC-100 Falltime Definition . . . . . | 9 |
| 6 | Test A - SE100T DTL NAND/NOR Gate Test Circuit. . | 17 |
| 7 | Test B - SE100T DTL NAND/NOR Gate Test Circuit. . | 18 |
| 8 | Test Circuit - SE200T TTL NAND/NOR Gate . . . . . | 31 |
| 9 | Test Circuit - SE120T DTL Binary Element. . . . . | 41 |
| 10 | Test Circuit - SE130T DTL Buffer. . . . . | 52 |
| 11 | Test Circuit - SE140T DTL Exclusive-OR Network. . | 65 |
| 12 | Test Circuit - RCA DMC-100 Digital Microcircuit . | 76 |
| 13 | Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 1). . . . . | 83 |
| 14 | Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 2). . . . . | 84 |
| 15 | Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 3). . . . . | 85 |
| 16 | PCG-101 Dual NAND Gate. . . . . | 90 |
| 17 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 93 |
| 18 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 98 |
| 19 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 100 |
| 20 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 105 |
| 21 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 107 |
| 22 | Propagation Delay Diagram - PCG-101 Dual NAND Gate. . . . . | 108 |
| 23 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 111 |
| 24 | Test Circuit - PCG-101 Dual NAND Gate . . . . . | 112 |
| 25 | Test Circuit - PCH-101 Half-Adder . . . . . | 119 |
| 26 | Test Circuit - PCR-101 Full-Shift Register. . . . | 125 |

## PRODUCT LIST

The following items, in addition to those listed in the two previous $\mu$-NOTES, have been received for evaluation:

Signetics Corporation

Type SE130T DTL Buffer
Type SE140T DTL Exclusive-OR Network

Westinghouse Electric Corporation

Type WM2101 Double NAND Gate
Type WM2104 Single NAND Gate
Type WX2501 Binary Counter
Type WM1105 Audio Amplifier
Type WX016 Video Amplifier

Pacific Semiconductors, Incorporated

Type PCG-102 Three-Input NAND Gate
Type PCG-103 Dual NAND Gate
Type PCH-103 Dual Exclusive-OR
Type PCR-101 Full Shift Register

These items are all solid-state integrated circuits.

This $\mu$-NOTES reports the evaluation of all Signetics and Pacific Semiconductors units received thus far, as well as the Radio Corporation of America DMC-100 unit.

## STANDARDIZATION

The Battelle Memorial Institute has completed its initial effort in the preparation of functional descriptions for microelectronic assemblies. (See appendix A.) In this first effort, Battelle was contractually limited to elements within the sphere of the preferred circuits work sponsored for a number of years by the Bureau of Naval Weapons. As a result, the functional descriptions may not be completely realistic in terms of currently more advanced technologies in microelectronics, but they are all functions that can be microminiaturized by one or more of the common techniques. The greatest value of this first effort has been, therefore, in the development of techniques for specifying microelectronic elements on a functional basis. In the extension of the Battelle contract, it is planned to apply these techniques to actual microelectronic elements.

Readers of $\mu$-NOTES are requested to comment on the method (appendix A) of presenting these functional descriptions. It should be remembered that none of these functions are being proposed as standards at this time, and it is possible that none may ever be proposed as standards. The comments should therefore be restricted to the adequacy and type of information presented, and should also indicate whether they express the viewpoint of a user or a producer of microelectronic assemblies.

## RESEARCH AND DEVELOPMENT

The final report from the General Electric Company, prepared under Contract No. N62269-1335, and abstracted in $\mu$-NOTES No. 2, has been reproduced and distributed. Copies may be obtained through ASTIA by requesting Report No. NADC-EL-6264, "Development of Microelectronic Circuits for Linear Applications," of 16 October 1962; ASTIA Accession No. AD-287650.

Under the current Contract No. N62269-1685 with the General Electric Company, for the development of 10-megacycle thin-film logic elements, a logic system has been selected and designs are being optimized. The functions will utilize diode and transistor- or emitter-coupled logic (DATO-ECLO). With this system, all of the required functions can be realized, while using only two different circuit substrates. Basic performance information will be published when design optimization is complete.

# E V A L U A T I O N

## SIGNETICS LOGIC ELEMENTS

The Signetics logic elements are a family of digital-computer building blocks using diode transistor logic (DTL) and, in the case of one gate element, transistor-coupled transistor logic (TTL). The units are formed, by planar techniques, in single silicon chips. All units evaluated were mounted in eight-lead TO-5 headers, although they are also available in a flat package. Signetics tentative data sheets of August 1962, were used as a basis for the evaluation. These sheets provide only a minimum of information, however, and it is difficult to understand fully the operation of the units. Signetics is publishing more complete data sheets, and it is suggested that potential users refer to these sheets for future evaluations.

The fullowing Signetics units were evaluated:

| Type | Function |
|---|---|
| SE100T | DTL NAND/NOR Gate |
| SE200T | TTL NAND Gate |
| SE120T | DTL Binary Element |
| SE130T | DTL Buffer |
| SE140T | DTL Exclusive-OR Network |

The Signetics family also includes the Type SE104 diode array, but this unit was not evaluated.

Evaluations were performed with varying input voltage levels. Minimum input voltage levels were not established for all units, but were determined when found to be particularly critical.

Although the noise immunity of the DTL and TTL logic systems is discussed in general terms, no actual observations were made of any phenomena that could be attributed to interference, nor were any tests made to measure noise immunity. It is anticipated that this information will be developed at a future date for all microminiature logic elements.

### SE100T DTL NAND/NOR Gate

The manner in which the SE100T DTL NAND/NOR gate operates (See figure 1.) depends upon whether or not the transistor $T_1$ is conducting.

If transistor $T_1$ is not conducting, the voltage at $Q_1$ is virtually equal to $V_{CC}$. Current will therefore flow from $V_{CC}$ through the two series diodes and then through the two parallel paths formed by the negative bias line and transistor $T_2$. Under these conditions, the voltage at point A is equal to $V_{CC}$, minus the voltage drop across the 4-k resistor; and the voltage at point B is equal to the voltage at point A,

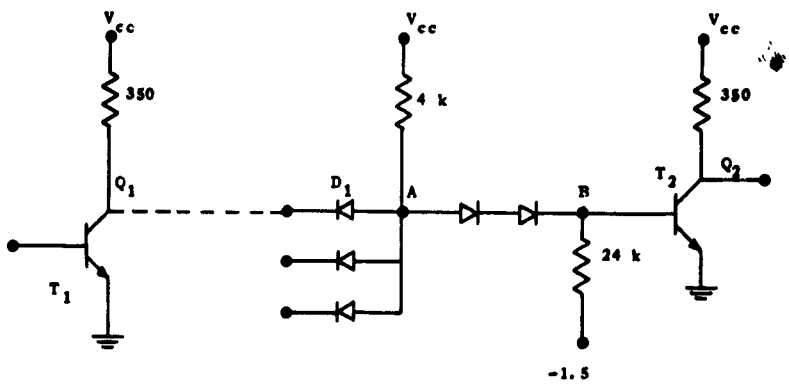



FIGURE 1 - Schematic - SE100T DTL NAND/NOR Gate

minus the forward voltage drop of the two diodes. Since the voltage at point B, is positive, it is able to drive transistor $T_2$ into saturation, and $Q_2$ will be at almost ground potential and equal to $V_{CE(sat)}$. In this state, a positive disturbance (noise) picked up between $Q_1$ and $D_1$ will not affect the operation of the gate, but will merely increase the reverse bias on $D_1$. A negative disturbance will affect the operation, but must be of sufficient magnitude to overcome the reverse voltage of $D_1$, the forward voltage of $D_1$, plus the voltage necessary to deenergize $T_2$.

When $T_1$ is conducting, the situation is somewhat different. When any of the gate inputs, $D_1$ for example, is conducting to a low resistance path, such as the saturated collector of $T_1$, the voltage level at point A is equal to the $V_{CE(sat)}$ of $T_1$, plus the forward voltage drop of $D_1$; the voltage level at point B is at ground or below ground potential. Thus, the base of $T_2$ is biased beyond cutoff. Although a positive disturbance at the input will affect the operation of the gate, it must be large enough to overcome the forward voltage drop of the two series base diodes and the voltage required to change $T_2$ to its conducting state.

Thus, the SE100T DTL NAND/NOR gate has a relatively high noise immunity, provides diode isolation, and has no fan-in limitations.

This unit was evaluated at different frequencies under maximum fan-out conditions, at temperatures of -55°, +25°, and +125° C. The tabulated data and the waveforms included in the TEST RESULTS show that the gates performed satisfactorily. The propagation delay averaged 30 nanoseconds (ns).

SE200T TTL NAND/NOR Gate

The SE200T TTL NAND/NOR Gate (See figure 2.) is characterized by the coupling transistor $T_3$, which uses a multiple emitter structure.

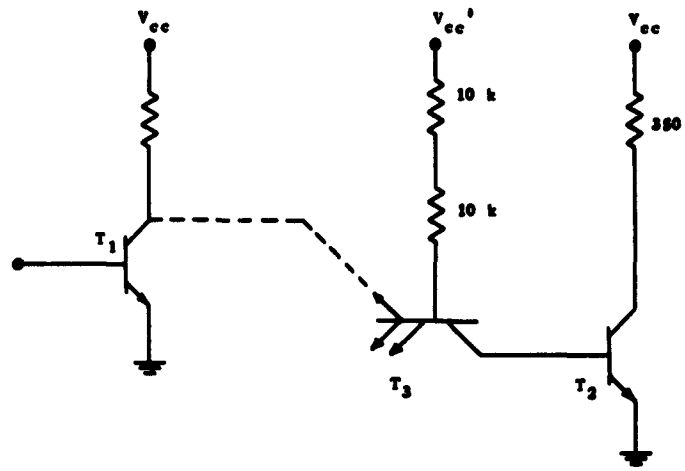



FIGURE 2 - Schematic - SE200T TTL NAND/NOR Gate

When the driving transistor $T_1$ is cut off, the emitter of $T_3$ encounters a very high impedance (approximately 500 k). This is virtually equivalent to an open circuit, and effectively steers the current from $V_{CC}'$ through the collector of $T_3$ ($T_3$ acts as a diode in this case.), and into the base of $T_2$. When $T_1$ is saturated, the base current of $T_3$ is steered away from its collector, into its emitter, and then into the collector of $T_1$. This clamps the base of $T_2$ to a potential low enough to take it beyond cutoff. In this case, the emitter of $T_3$ is clamped at almost ground potential through $T_1$; and, since the $V_{BE}$ of $T_3$ is much smaller than the $V_{BC}$ of $T_3$ plus the $V_{BE}$ of $T_2$, the current is naturally steered through the emitter. It should also be observed that when $T_1$ is cut off, $T_2$ is saturated, and $T_1$ is then driven to saturation, not only is the base current of $T_3$ steered into its emitter, but the saturating base current of $T_2$ is diverted out through the collector and emitter of $T_3$.

This gate configuration is suitable for high-frequency operation, since the long time normally required to bring a transistor out of saturation is reduced by the steering action of $T_3$. The only difference between the SE100T and SE200T gates is in circuit design; there is no difference in logic function. The SE100T is, however, more compatible with the other units in the Signetics family.

The SE200T was evaluated at different frequencies under maximum fan-out conditions, at temperatures of -55°, +25°, and +125° C. (Signetics rates the SE200T from -55° through an upper limit of only +55° C.) In general, operation was more satisfactory at the higher temperatures than at the lower temperatures. The propagation delay averaged 25 ns.

SE120T DTL Binary Element

The SE120T DTL Binary Element (figure 3a) is a set-reset flip-flop. To speed the operation, two load lines are used (figure 3b), one when the transistor begins to conduct, and the other after the collector voltage has dropped 0.6 volt below $V_{CC}$.

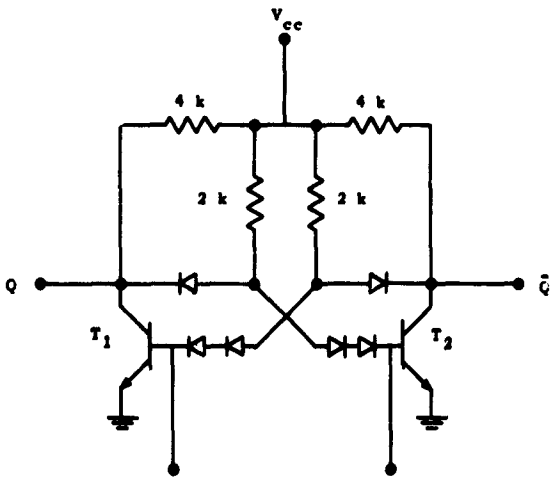



FIGURE 3a - Schematic - SE120T DTL Binary Element

When transistor $T_1$ begins to conduct, the collector current is flowing through the 4-k resistor only (figure 3a), represented by load line A (figure 3b), since there can be no current flow through the other path until the potential difference across the diode exceeds 0.6 volt. Thus, the instant after $T_1$ conducts, and the voltage difference between $V_{CC}$ and the collector of $T_1$ exceeds 0.6 volt, the load resistance of $T_1$ has changed from 4 k to less than 2 k, as represented by load line B. Transistor $T_1$ can therefore be switched out of saturation quite easily since

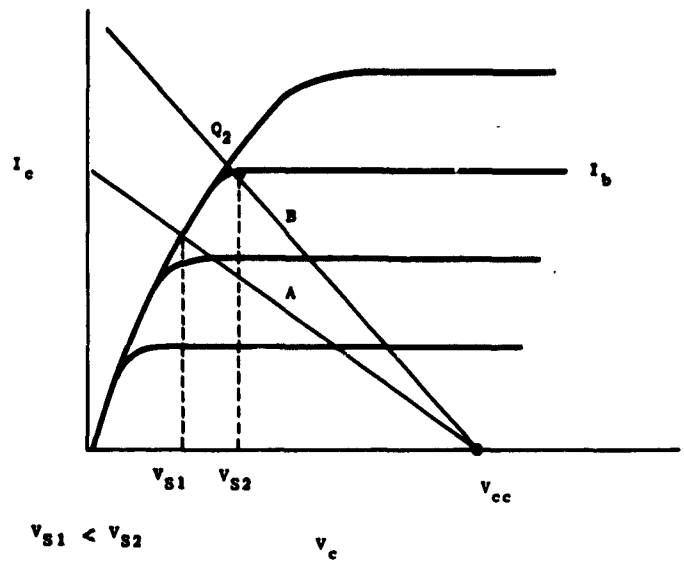



FIGURE 3b - Load Lines for Transistors - SE120T DTL Binary Element

$V_{S2}$ (the saturation voltage associated with load line B) is larger than $V_{S1}$ (the saturation voltage associated with load line A). This permits higher flip-flop speeds than would normally be possible.

The SE120T was evaluated at different frequencies under maximum fanout conditions at temperatures of -55°, +25°, and +125° C. TEST RESULTS show that at a clock rate of 5 mc, and under maximum fanout conditions, the minimum clock voltage at room temperature and at +125° C is 1.8 volts peak-to-peak. (Although not indicated in the data, the flip-flop operated satisfactorily at a clock rate of 10 mc.) The propagation delay between the clock pulse and the output averaged 30 ns.

SE130T DTL Buffer

The SE130T DTL Buffer is designed for driving capacitive lines, and for use as a buffer when a fanout beyond the capability of one of the logic elements is required. The SE130T has a rated fanout of 20 (N = 20) identical units. Although test results are not tabulated for N = 20, the unit operated satisfactorily at that rate. The data presented in the TEST RESULTS are for N = 16 at different frequencies and at temperatures of -55°, +25°, and +125° C.

SE140T DTL Exclusive-OR Network

The SE140T uses both AND and OR diode gating with inversion to obtain the exclusive-OR function. Evaluation was performed at maximum fanout conditions and different frequencies at temperatures of -55°, +25°, and +125° C. The unit performed satisfactorily, with an average propagation delay of 50 ns.

RCA DMC-100 DIGITAL MICROCIRCUIT LOGIC ELEMENT

The RCA DMC-100 (figure 4) is a high-speed, diode-coupled, digital circuit element for logic application. By itself, or in combination with other DMC-100 elements, it can be used as an inverter, amplifier, logic gate (positive NAND), flip-flop, or shift register. The circuit is

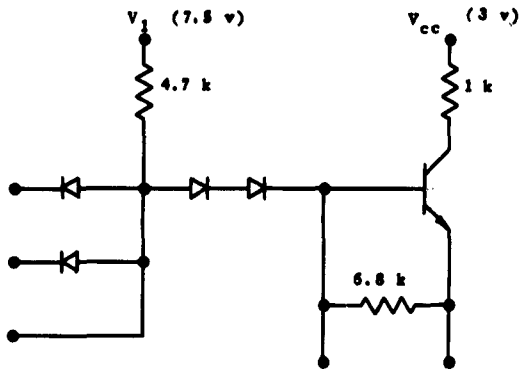



FIGURE 4 - Schematic - RCA DMC-100 Digital Microcircuit

constructed of microminiature, discrete, passive components, and passivated-chip active elements. The transistor is similar to the type 2N2475, and the diodes are similar to the type 1N914. The element is packaged in an eight-lead metal and ceramic header having the diameter of a TO-5 can (0.325 inch) and an overall height of 0.1 inch.

Operation of the DMC-100 is basically the same as that of the Signetics SE100T. The resistor values have been chosen so that the noise immunity at the input is approximately 50 percent of the switching level, or approximately 1.5 volts in both the on and the off conditions.

The unit was evaluated at various frequencies under maximum fanout conditions, at temperatures of -55°, +25°, and +125° C, using RCA tentative data sheet of May 1962, and RCA Application Note SMA-8, "Design and Application of the RCA DMC-100 Digital Micro-Circuit," of August 1962, as test guides. The results obtained compare favorably with RCA's

published data, except for the falltime. This difference, however, is due primarily to a difference in definition. The NAVAIRDEVCEN evaluations defined falltime as the time required to go from the 90-percent level to the 10-percent level defined as $T_f'$ in figure 5. RCA, however, defines falltime as the time required to go from the 90-percent level to the 1.6-volt level defined as $T_f$ in figure 5. (The 1.6-volt level, characterized by the "wiggle" in the waveform of figure 5, represents the triggering level, and the variation is caused by an abrupt change in input impedance at the moment of triggering.)

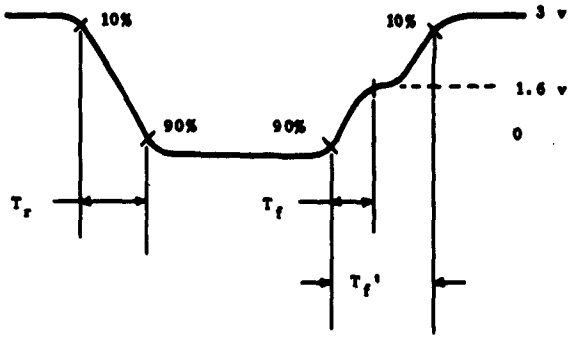



FIGURE 5 - DMC-100 Falltime Definition

The tabulated data included in the TEST RESULTS show values for both $T_f$ and $T_f'$. The measured values of $T_f$ were in close agreement with the RCA data; values for $T_f'$ were much larger, but did not affect the circuit delays. The units operated satisfactorily under all conditions, although the waveform distortion was severe at high frequencies.

PACIFIC SEMICONDUCTORS MICROCIRCUIT LOGIC ELEMENTS

The Pacific Semiconductors, Incorporated, microcircuit logic elements are a family of digital computer building blocks using TTL. They were the first complete family of TTL logic elements available commercially, although individual units had been introduced by others.

The following elements were evaluated, using Pacific Semiconductors tentative specifications of March 1962:

| Type | Function |
|---|---|
| PCF-101 | Set-Reset Flip-Flop |
| PCG-101 | Dual NAND Gate |
| PCH-101 | Half-Adder |
| PCR-101 | Full Shift Register |

The family also includes the following elements. These elements were not evaluated, inasmuch as they are functionally similar to those listed above, the differences being only in the number of inputs and outputs -

| Type | Function |
|---|---|
| PCG-102 | Three-Input NAND Gate |
| PCG-103 | Dual NAND Gate |
| PCH-103 | Dual Exclusive-OR Network |

PCF-101 Set-Reset Flip-Flop

This element is a direct-coupled flip-flop triggered by parallel pullover transistors. Multiple emitter transistors provide input gating, to minimize driving and loading requirements.

The flip-flop was evaluated under the following three conditions:

1. Source and test unit were in the test chamber, and the load was maintained at room temperature.

2. Test unit was in the test chamber, and the source and load were at room temperature.

3. Test unit and load were in the test chamber, and the source was at room temperature.

Under the first condition, the unit operated satisfactorily to -45° C, while under the second and third conditions, it operated satisfactorily at -55° C.

PCG-101 Dual NAND Gate

The PCG-101 contains two 3-input NAND gates that provide both direct and inverted outputs. Operation of this unit is similar to other TTL gates.

The PCG-101 was evaluated as a NAND gate; as an AND gate; and, by using the inverter transistor alone, as an inverter. The "worst case" input condition occurs when each emitter is driven from a different transistor collector. The evaluation was performed at temperatures of -55°, +25°, and +125° C, at frequencies from 0 to 5 megacycles. The units were also operated at a frequency of 10 megacycles at 125° C and a fanout of four. TEST RESULTS show that the two parameters subject to the widest variation were the falltime $T_f$ and the output voltage $V_{pp}$; $T_f$ increases and $V_{pp}$ decreases as the temperature is lowered to -55° C.

PCH-101 Half-Adder

The PCH-101 consists of two 2-input AND gates, followed by a NOR gate, and provides sum and carry outputs from four single-digit inputs. The sum output normally provides the exclusive-OR function, but it is possible, through alternate connections, to obtain inclusive-OR or "sum" and "borrow" terms for use as a half-subtractor.

This unit was evaluated at different frequencies and at temperatures of -55°, +25°, and +125° C. The results indicate that both the rise time $T_r$ and the $V_{pp}$ vary considerably with temperature.

PCR-101 Full-Shift Register

The PCR-101 is basically two PCF-101 elements in a single chip, connected as a shift register. This unit was evaluated from 0 to 1.5 megacycles at temperatures of -55°, +25°, and +125° C, and operated satisfactorily.

# TEST RESULTS FOR SIGNETICS CORPORATION LOGIC ELEMENTS

## SE100T DTL NAND/NOR GATE
(See figures 6 and 7)

Temp = 25° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T

Top Trace - output = 4.0 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.065 us

$T_f$ = 0.120 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 vdc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 3.0 $V_{pp}$

$T_r$ = 0.029 us

$T_f$ = 0.220 us

Temp = 25° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T

Top Trace - output = 3.0 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.050 us

$T_f$ = 0.089 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 2.4 $V_{pp}$

$T_r$ = 0.023 us

$T_f$ = 0.108 us

## SE100T DTL NAND/NOR GATE (Continued)
## (See figures 6 and 7)

Temp = 25° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T

Top Trace - output = 2.0 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.034 us

$T_f$ = 0.068 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 2.1 $V_{pp}$

$T_r$ = 0.022 us

$T_f$ = 0.082 us

Temp = 125° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load SE200T

Top Trace - output = 4.0 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.052 us

$T_f$ = 0.124 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 2.9 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.190 us

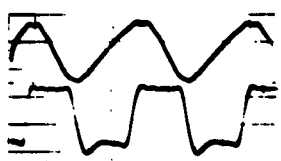
SE100T DTL NAND/NOR GATE (Continued)
(See figures 6 and 7)

Temp = 125° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T



Top Trace - output = 3.2 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.048 us

$T_f$ = 0.081 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 2.0 $V_{pp}$

$T_r$ = 0.017 us

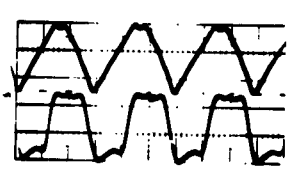
$T_f$ = 0.090 us

Temp = 125° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T



Top Trace - output = 2.45 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.039 us

$T_f$ = 0.056 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.3 $V_{pp}$

Output = 1.7 $V_{pp}$

$T_r$ = 0.016 us

$T_f$ = 0.074 us

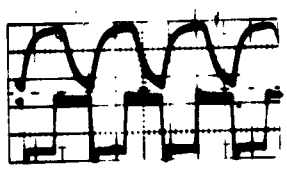
SE100T DTL NAND/NOR GATE (Continued)
(See figures 6 and 7)

Temp = -55° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

Test A

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T



Top Trace - output = 2.6 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.029 us

$T_f$ = 0.117 us

Test B

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.5 $V_{pp}$

Output = 1.9 $V_{pp}$

$T_r$ = 0.044 us

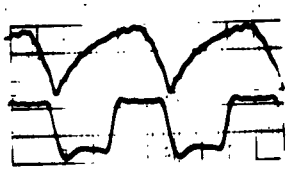
$T_f$ = 0.124 us

Temp = -55° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

Test A

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T



Top Trace - output = 2.0 $V_{pp}$

Bottom Trace - input = 1.2 $V_{pp}$

$T_r$ = 0.038 us

$T_f$ = 0.100 us

Test B

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.5 $V_{pp}$

Output = 1.7 $V_{pp}$

$T_r$ = 0.033 us

$T_f$ = 0.094 us

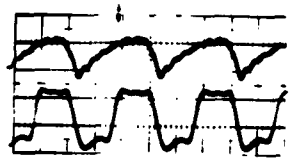
SE100T DTL NAND/NOR GATE (Continued)
(See figures 6 and 7)

Temp = -55° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

**Test A**

$V_{cc}$ = +6 v dc, -1.5 v dc

Driver - SE100T
Load - SE200T



Top Trace - output = 0.6 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

$T_r$ = 0.019 us

$T_f$ = 0.079 us

**Test B**

$V_{cc}$ = +4 v dc, -1.5 v dc

Driver - SE100T
Load - SE100T

Input = 1.5 $V_{pp}$

Output = 2.0 $V_{pp}$

$T_r$ = 0.026 us

$T_f$ = 0.096 us

NOTE: At 5.2 mc, output is less than 1.5 v input. If input is increased to 2.0 v, maximum frequency = 6.0 mc.

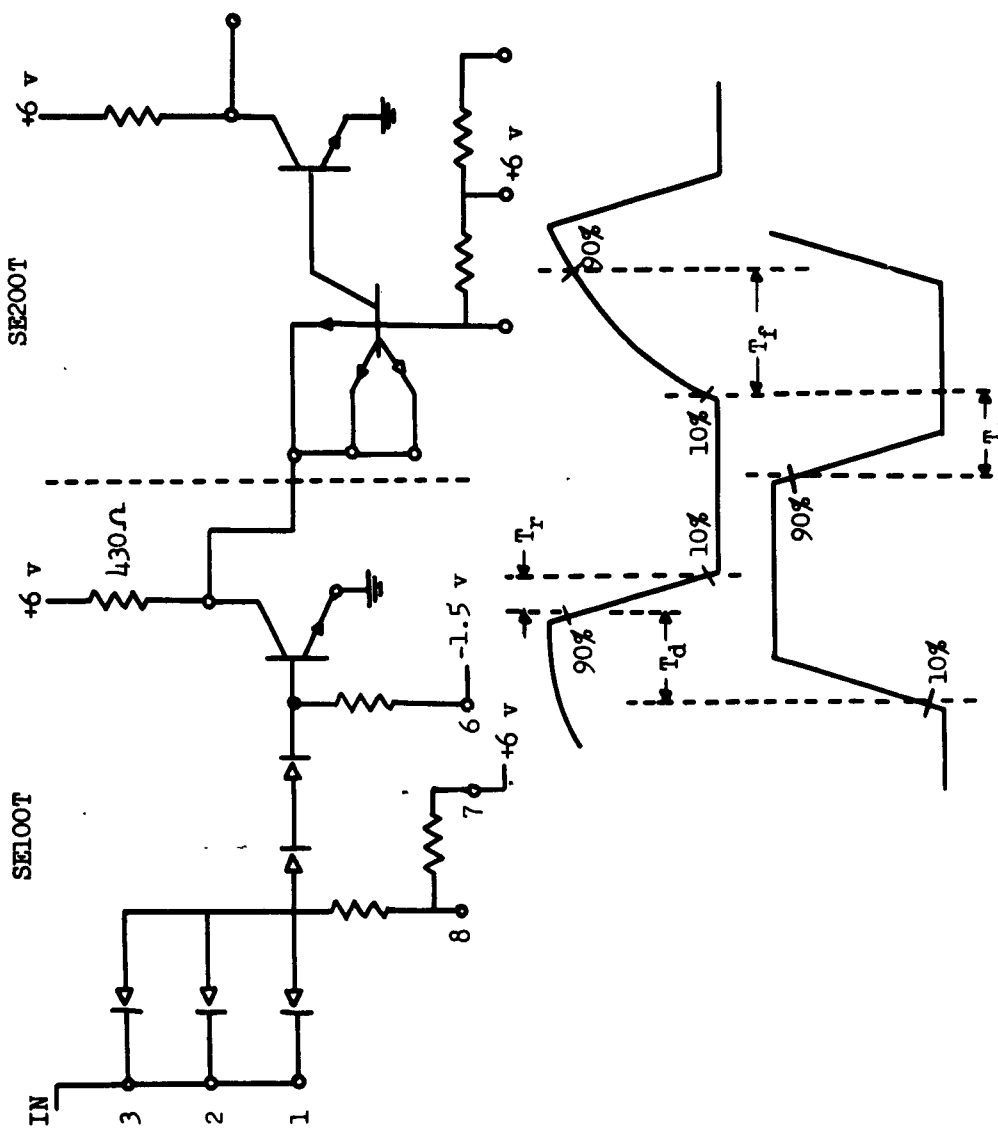



FIGURE 6 - Test A - SE100T DTL NAND/NOR Gate Test Circuit

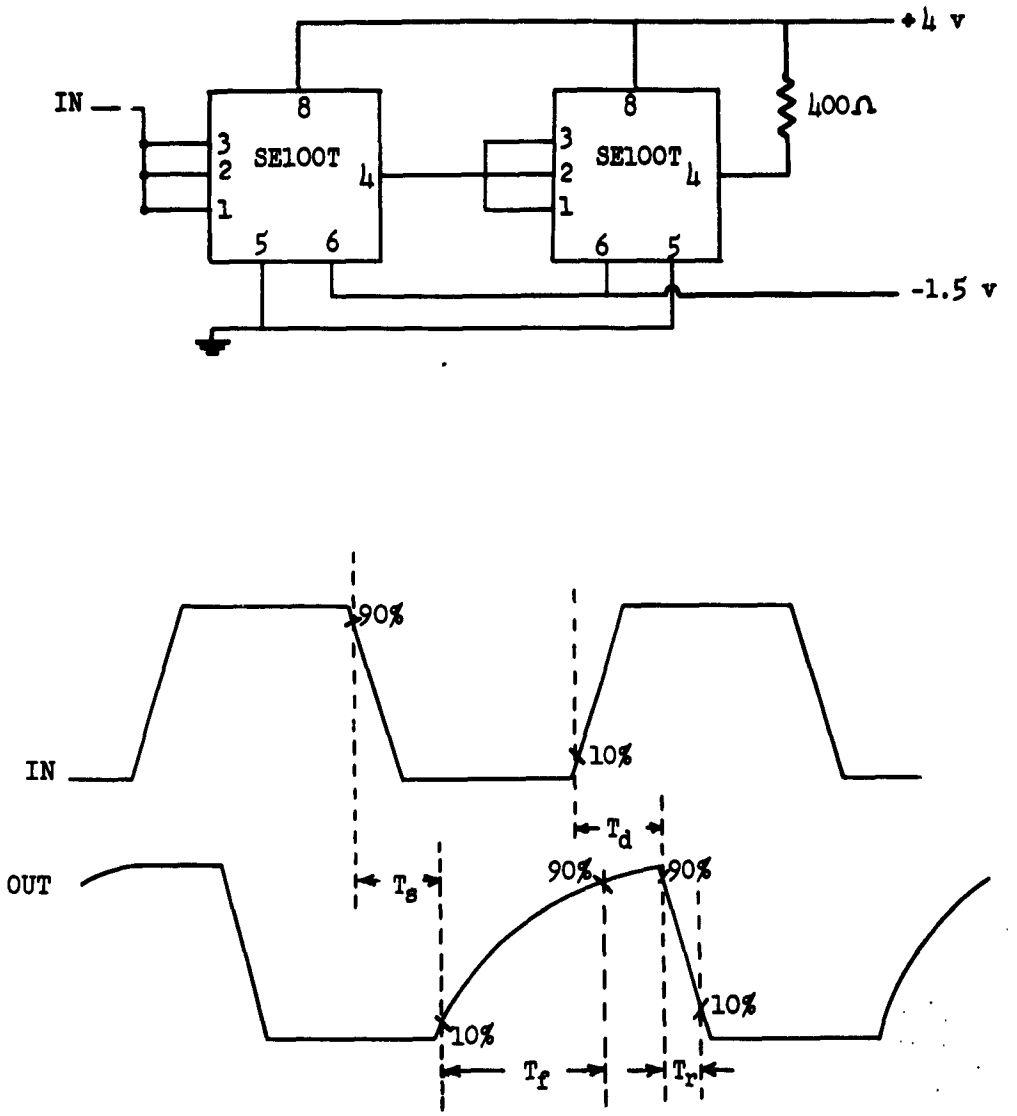


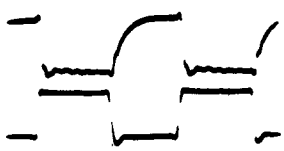

FIGURE 7 - Test B - SE100T DTL NAND/NOR Gate Test Circuit

## SE200T TTL NAND/NOR GATE
(See figure 8)

Temp = 25° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 1.5 $V_{pp}$

Bottom Trace -
input = 2.75 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.086 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.6 $V_{pp}$

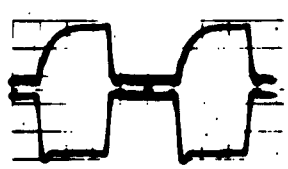
Output = 0.8 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.090 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 4.0 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.011 us

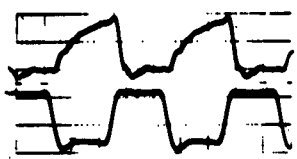
$T_f$ = 0.078 us

SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 25° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 1.5 $V_{pp}$

Bottom Trace -
input = 2.75 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.086 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.6 $V_{pp}$

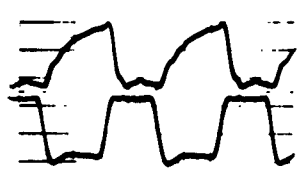
Output = 0.7 $V_{pp}$

$T_r$ = 0.023 us

$T_f$ = 0.086 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 4.0 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.011 us

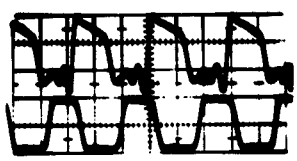
$T_f$ = 0.071 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 25° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 2.8 $V_{pp}$

Bottom Trace -
input = 0.8 $V_{pp}$

$T_r$ = 0.007 us

$T_f$ = 0.012 us

Propagation delay = 0.018 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.6 $V_{pp}$

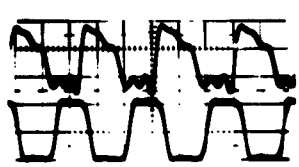
Output = 0.6 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.070 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 5.5 $V_{pp}$

Bottom Trace -
input = 0.8 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.014 us

Propagation delay = 0.018 us

SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 25° C; F = 10.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 1.5 $V_{pp}$

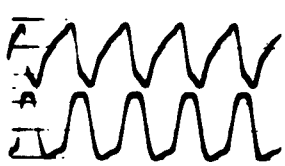
Bottom Trace -
input = 3.0 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.045 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 3.7 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.012 us

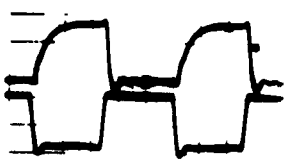
$T_f$ = 0.049 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 125° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 2.15 $V_{pp}$

Bottom Trace -
input = 3.0 $V_{pp}$

$T_r$ = 0.012 us

$T_f$ = 0.090 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.5 $V_{pp}$

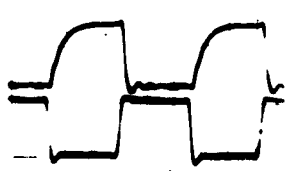
Output = 0.6 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.100 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 4.55 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.014 us

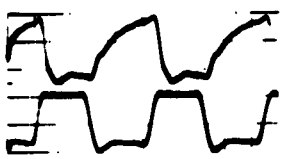
$T_f$ = 0.084 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 125° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 2.15 $V_{pp}$

Bottom Trace -
input = 3.0 $V_{pp}$

$T_r$ = 0.012 us

$T_f$ = 0.081 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.5 $V_{pp}$

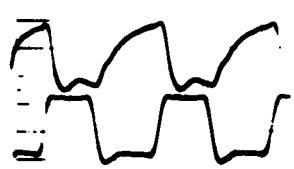
Output = 0.55 $V_{pp}$

$T_r$ = 0.019 us

$T_f$ = 0.090 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 4.55 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.014 us

$T_f$ = 0.081 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 125° C; F = 6.0 mc (max); N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

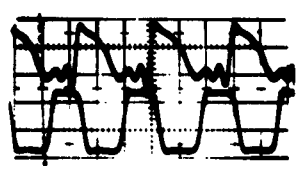
Input = 0.5 $V_{pp}$ $T_r$ = 0.020 us

Output = 0.5 $V_{pp}$ $T_f$ = 0.090 us

Temp = 125° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace - output = 2.5 $V_{pp}$

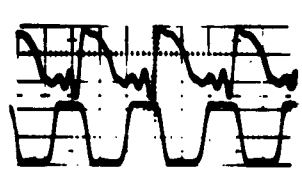
Bottom Trace - input = 0.8 $V_{pp}$

$T_r$ = 0.008 us

$T_f$ = 0.013 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace - output = 5.0 $V_{pp}$

Bottom Trace - input = 0.8 $V_{pp}$

$T_r$ = 0.008 us

$T_f$ = 0.013 us

Propagation delay = 0.026 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = 125° C; F = 10.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 1.13 $V_{pp}$

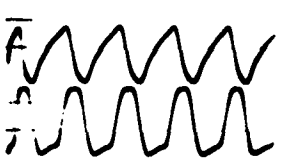
Bottom Trace -
input = 3.0 $V_{pp}$

$T_r$ = 0.012 us

$T_f$ = 0.044 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 4.15 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.016 us

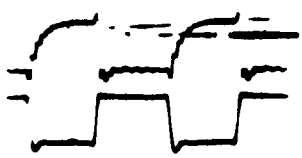
$T_f$ = 0.047 us

## SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = -55° C; F = 2.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 0.65 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.006 us

$T_f$ = 0.075 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.75 $V_{pp}$

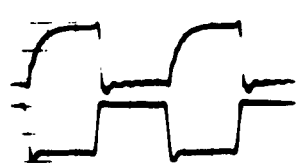
Output = 0.8 $V_{pp}$

$T_r$ = 0.043 us

$T_f$ = 0.106 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 2.8 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.011 us

$T_f$ = 0.081 us

SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = -55° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 0.80 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.008 us

$T_f$ = 0.088 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.75 $V_{pp}$

Output = 0.80 $V_{pp}$

$T_r$ = 0.037 us

$T_f$ = 0.100 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 2.10 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.075 us

SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = -55° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 2.9 $V_{pp}$

Bottom Trace -
input = 0.8 $V_{pp}$

$T_r$ = 0.008 us

$T_f$ = 0.016 us

Propagation delay = 0.0225 us

$V_{cc}$ = 4 v dc

Driver - SE200T
Load - SE200T

Input = 0.75 $V_{pp}$

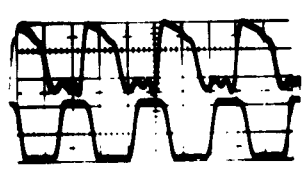
Output = 0.70 $V_{pp}$

$T_r$ = 0.031 us

$T_f$ = 0.078 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T



Top Trace -
output = 6.0 $V_{pp}$

Bottom Trace -
input = 0.8 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.014 us

Propagation delay = 0.022 us

SE200T TTL NAND/NOR GATE (Continued)
(See figure 8)

Temp = -55° C; F = 10.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = 3 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 0.80 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.008 us

$T_f$ = 0.044 us

$V_{cc}$ = 6 v dc

Driver - SE200T
Load - SE200T

Top Trace -
output = 2.0 $V_{pp}$

Bottom Trace -
input = 4.0 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.045 us

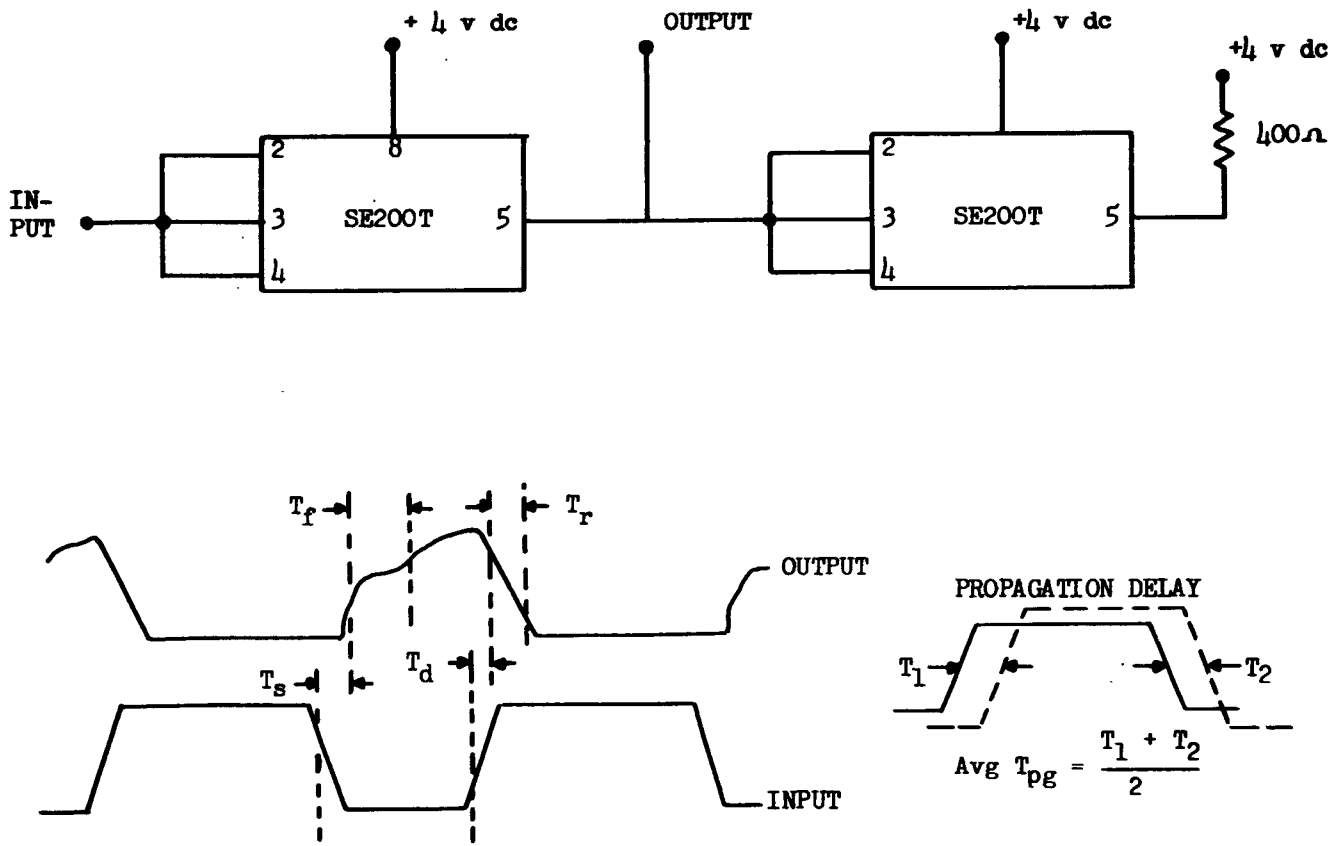



FIGURE 8 - Test Circuit - SE200T TTL NAND/NOR GATE

## SE120T DTL BINARY ELEMENT
(See figure 9)

Temp = 25° C; F = 2.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

Top Trace -
output = 2.2 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r5}$ = 0.028 us

$T_{f5}$ = 0.131 us

Driver - SE120T
Load - SE200T

Top Trace -
output = 2.1 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r1}$ = 0.026 us

$T_{f1}$ = 0.154 us

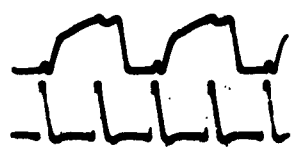
* *Input - Pulse amplitude: 6.0 $V_{pp}$ max, 1.8 $V_{pp}$ min*

## SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = 25° C; F = 5.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T



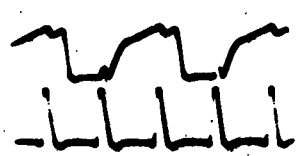
Top Trace -
output = 2.1 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r5}$ = 0.028 us

$T_{f5}$ = 0.172 us

Driver - SE120T
Load - SE200T



Top Trace -
output = 1.9 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.022 us

$T_{f1}$ = 0.192 us

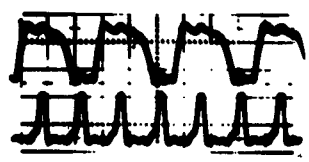
* *Input - Pulse amplitude: 4.8 $V_{pp}$ max, 1.8 $V_{pp}$ min*

## SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = 25° C; F = 7.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE130T



Top Trace -
output = 1.9 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r5}$ = 0.026 us

$T_f$ = **

Driver - SE120T
Load - SE120T

Top Trace -
output = 1.8 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.026 us

$T_{f1}$ = 0.038 us

---

* *Input - Pulse amplitude: 3.5 $V_{pp}$ max, 2.0 $V_{pp}$ min*

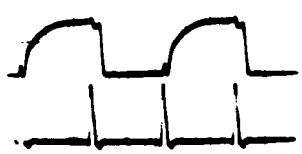
** *$T_f$ at 1.7 v = 0.037 us; $T_f$ at 1.9 v = 0.059 us*

## SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = 125° C; F = 2.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T



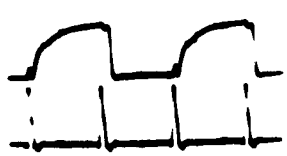
Top Trace -
output = 2.0 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r5}$ = 0.029 us

$T_{f5}$ = 0.209 us

Driver - SE120T
Load - SE200T



Top Trace -
output = 1.8 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r1}$ = 0.019 us

$T_{f1}$ = 0.239 us

* *Input - Pulse amplitude: 4.0 $V_{pp}$ max, 1.8 $V_{pp}$ min*

SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = 125° C; F = 5.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

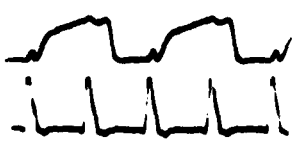
Top Trace -
output = 1.5 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r5}$ = 0.020 us

$T_{f5}$ = 0.090 us

Driver - SE120T
Load - SE200T



Top Trace -
output = 1.4 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.020 us

$T_{f1}$ = 0.156 us

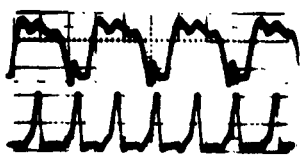
* *Input - Pulse amplitude: 3.0 $V_{pp}$ max, 1.8 $V_{pp}$ min*

SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = 125° C; F = 7.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

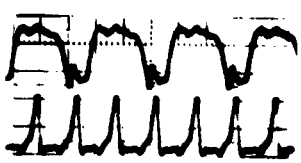


Top Trace -
output = 1.4 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r5}$ = 0.023 us

$T_f$ = **



Top Trace -
output = 1.4 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.027 us

$T_f$ = ***

---

* *Input - Pulse amplitude: 3.0 $V_{pp}$ max, 1.8 $V_{pp}$ min*

** *$t_f$ at 1.3 v = 0.032; $t_f$ at 1.4 v = 0.062 us*

*** *$t_f$ at 1.3 v = 0.034; $t_f$ at 1.4 v = 0.044 us*

SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = -55° C; F = 2.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

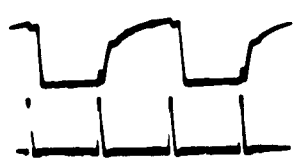
Top Trace -
output = 2.3 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r5}$ = 0.036 us

$T_{f5}$ = 0.20 us

Driver - SE120T
Load - SE200T



Top Trace -
output = 2.3 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.030 us

$T_{f1}$ = 0.260 us

* *Input - Pulse amplitude: 6.0 $V_{pp}$ max, 2.0 $V_{pp}$ min*

SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = -55° C; F = 5.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

Top Trace -
output = 2.3 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.02 us)

$T_{r5}$ = 0.045 us

$T_{f5}$ = 0.185 us

Driver - SE120T
Load - SE200T

Top Trace -
output = 2.0 $V_{pp}$ (0.020 us)

Bottom Trace -
input = 2.0 $V_{pp}$ (0.20 us)

$T_{r1}$ = 0.034 us

$T_{f1}$ = 0.214 us

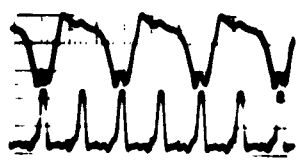
* *Input - Pulse amplitude: 4.2 $V_{pp}$ max, 2.0 $V_{pp}$ min*

SE120T DTL BINARY ELEMENT (Continued)
(See figure 9)

Temp = -55° C; F = 7.0 mc; N = 4; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE120T
Load - SE100T

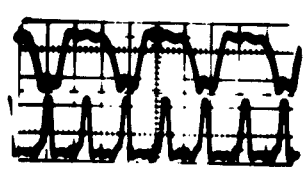


Top Trace -
output = 1.9 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r5}$ = 0.032 us

$T_f$ = **



Top Trace -
output = 1.7 $V_{pp}$

* Bottom Trace -
input = 2.0 $V_{pp}$ (0.020 us)

$T_{r1}$ = 0.026 us

$T_{f1}$ = 0.048 us

---

* *Input - Pulse amplitude: 3.6 $V_{pp}$ max, 2.0 $V_{pp}$ min*

** *$T_f$ at 1.7 v = 0.032; $T_f$ at 1.9 v = 0.092 us*

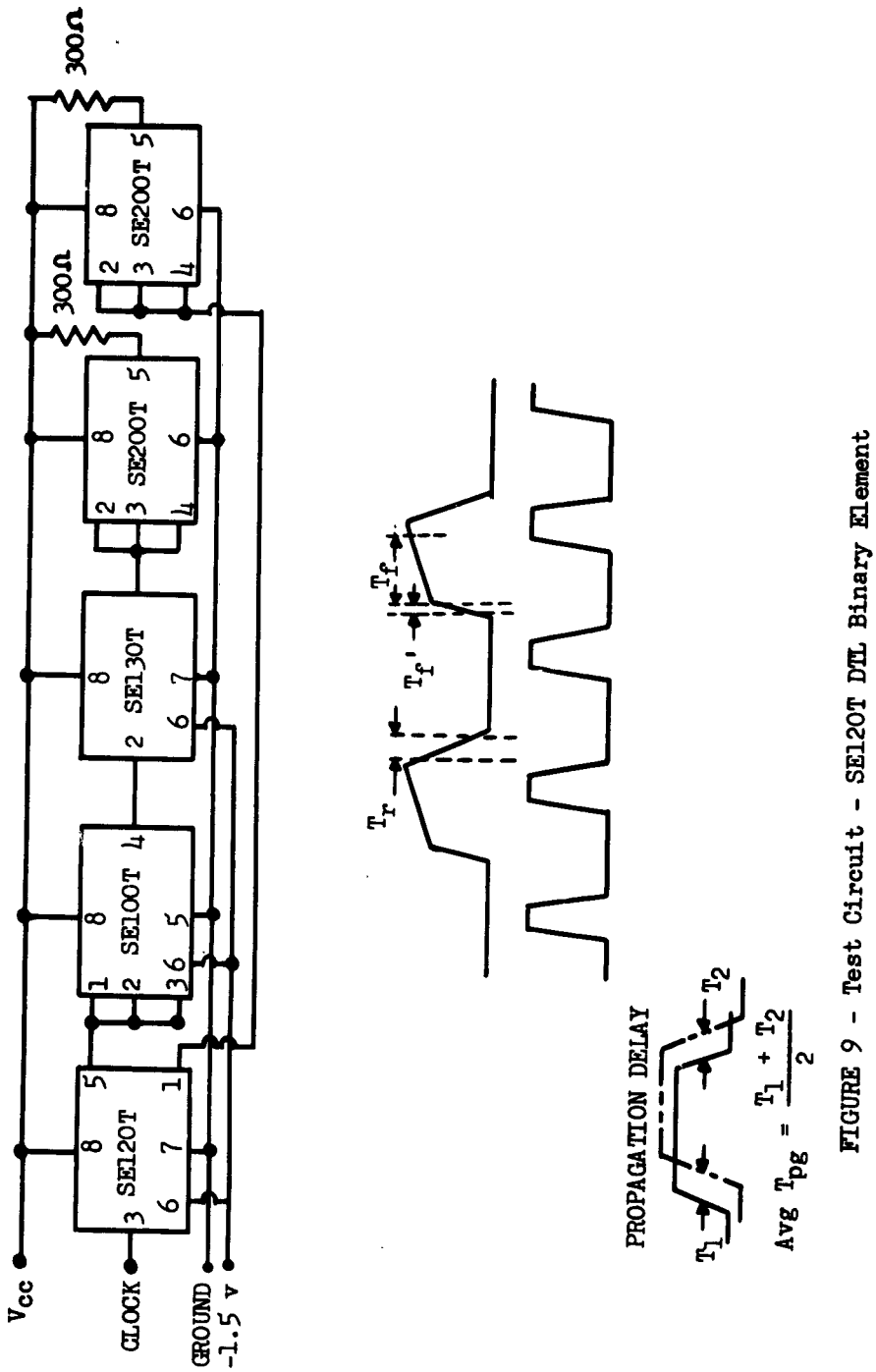



FIGURE 9 - Test Circuit - SE12OT DTL Binary Element

## SE130T DTL BUFFER
(See figure 10)

Temp = 25° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

F = 2.0 mc

Input = 1.5 $V_{pp}$

Output = 2.4 $V_{pp}$

$T_r$ = 0.025 us

$T_f$' = 0.065 us

F = 5.0 mc

Input = 1.5 $V_{pp}$

Output = 1.9 $V_{pp}$

$T_r$ = 0.021 us

$T_f$ = 0.049 us

F = 7.0 mc

Input = 1.5 $V_{pp}$

Output = 1.6 $V_{pp}$

$T_r$ = 0.021 us

$T_f$ = 0.038 us

## SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 25° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

F = 1.0 mc

Top Trace - output = 3.0 $V_{pp}$

Bottom Trace - input = 2.5 $V_{pp}$

$T_r$ = 0.030 us

$T_f$ = 0.031 us

$T_f'$ = 0.030 us

F = 2.5 mc

Top Trace - output = 2.1 $V_{pp}$

Bottom Trace - input = 2.5 $V_{pp}$

$T_r$ = 0.028 us

$T_f$ = 0.148 us

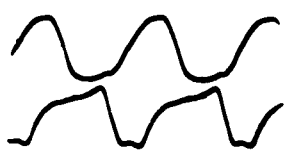
$T_f'$ = 0.042 us

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 25° C; F = 5.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

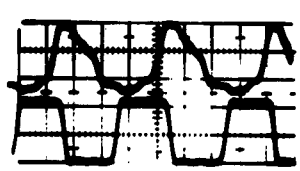


Top Trace -
output = 1.7 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.03 us

$T_f$ = 0.052 us



Top Trace -
output = 1.7 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.020 us

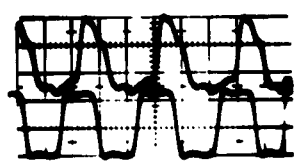
$T_f$ = 0.052 us

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 25° C; F = 7.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T



Top Trace -
output = 1.3 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.033 us

Temp = 125° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

F = 2.0 mc

Input = 1.5 $V_{pp}$

Output = 2.3 $V_{pp}$

$T_r$ = 0.020 us

$T_f$' = 0.100 us

F = 5.0 mc

Input = 1.5 $V_{pp}$

Output = 1.6 $V_{pp}$

$T_r$ = 0.040 us

$T_f$ = 0.050 us

## SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 125° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

F = 1.0 mc

Top Trace - output = 2.7 $V_{pp}$

Bottom Trace - input = 2.5 $V_{pp}$

$T_r$ = 0.028 us

$T_f$ = 0.37 us

$T_f'$ = 0.035 us

F = 2.5 mc

Top Trace - output = 1.6 $V_{pp}$

Bottom Trace - input = 2.0 $V_{pp}$

* $T_r$ = 0.027 us

$T_f$ = 0.137 us

* $t_f$ = 0.047 at 1.2 v

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 125° C; F = 5.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

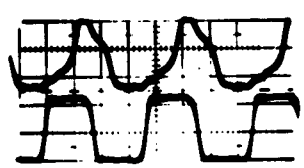
Driver - SE130T; Load - SE100T, SE140T, SE200T

Top Trace -
output = 1.2 $V_{pp}$

Bottom Trace -
input = 1.0 $V_{pp}$

$T_r$ = 0.033 us

$T_f$ = 0.043 us



Top Trace -
output = 1.2 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.043 us (10-90%)

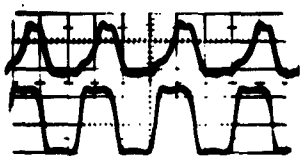
$T_r$ = 0.023 us (10-50%)

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = 125° C; F = 7.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T



Top Trace -
output = 1.0 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.024 us

$T_f$ = 0.021 us

Temp = -55° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T

F = 2.0 mc

Input = 1.75 $V_{pp}$

Output = 2.0 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.082 us

F = 5.0 mc

Input = 1.75 $V_{pp}$

Output = 1.9 $V_{pp}$

$T_r$ = 0.020 us

$T_f$ = 0.060 us

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = -55° C; N = 16; $V_{pp}$ = Voltage peak-to-peak

Driver - SE130T; Load - SE100T, SE140T, SE200T

$V_{cc}$ = +4.5 v dc, -1.5 v dc

F = 7.0 mc

Input = 1.75 $V_{pp}$

Output = 1.9 $V_{pp}$

$T_r$ = 0.025 us

$T_f$ = 0.065 us

$V_{cc}$ = +4.5 v dc

F = 1.0 mc

Top Trace - output = 3.1 $V_{pp}$

Bottom Trace - input = 2.3 $V_{pp}$

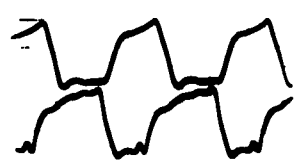
$T_r$ = 0.046 us

$T_f$ = 0.300 us

$T_f'$ = 0.040 us

$V_{cc}$ = +4.5 v dc

F = 1.0 mc



Top Trace - output = 2.3 $V_{pp}$

Bottom Trace - input = 2.5 $V_{pp}$

$T_r$ = 0.045 us

$T_f$ = 0.132 us

$T_f'$ = 0.042 us

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = -55° C; F = 5.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

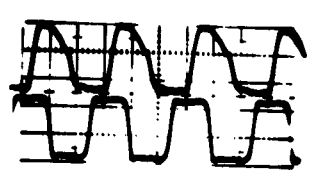
Driver - SE130T; Load - SE100T, SE140T, SE200T

Top Trace -
output = 2.0 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.045 us

$T_f$ = 0.065 us



Top Trace -
output = 1.9 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.018 us

$T_f$ = 0.049 us

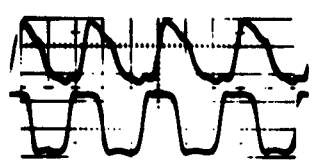
Propagation delay = 0.0475 us

SE130T DTL BUFFER (Continued)
(See figure 10)

Temp = -55° C; F = 7.0 mc; N = 16; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc

Driver - SE130T; Load - SE100T, SE140T, SE200T



Top Trace -
output = 1.9 $V_{pp}$

Bottom Trace -
input = 2.2 $V_{pp}$

$T_r$ = 0.018 us

$T_f$ = 0.052 us

Propagation delay = 0.0275 us

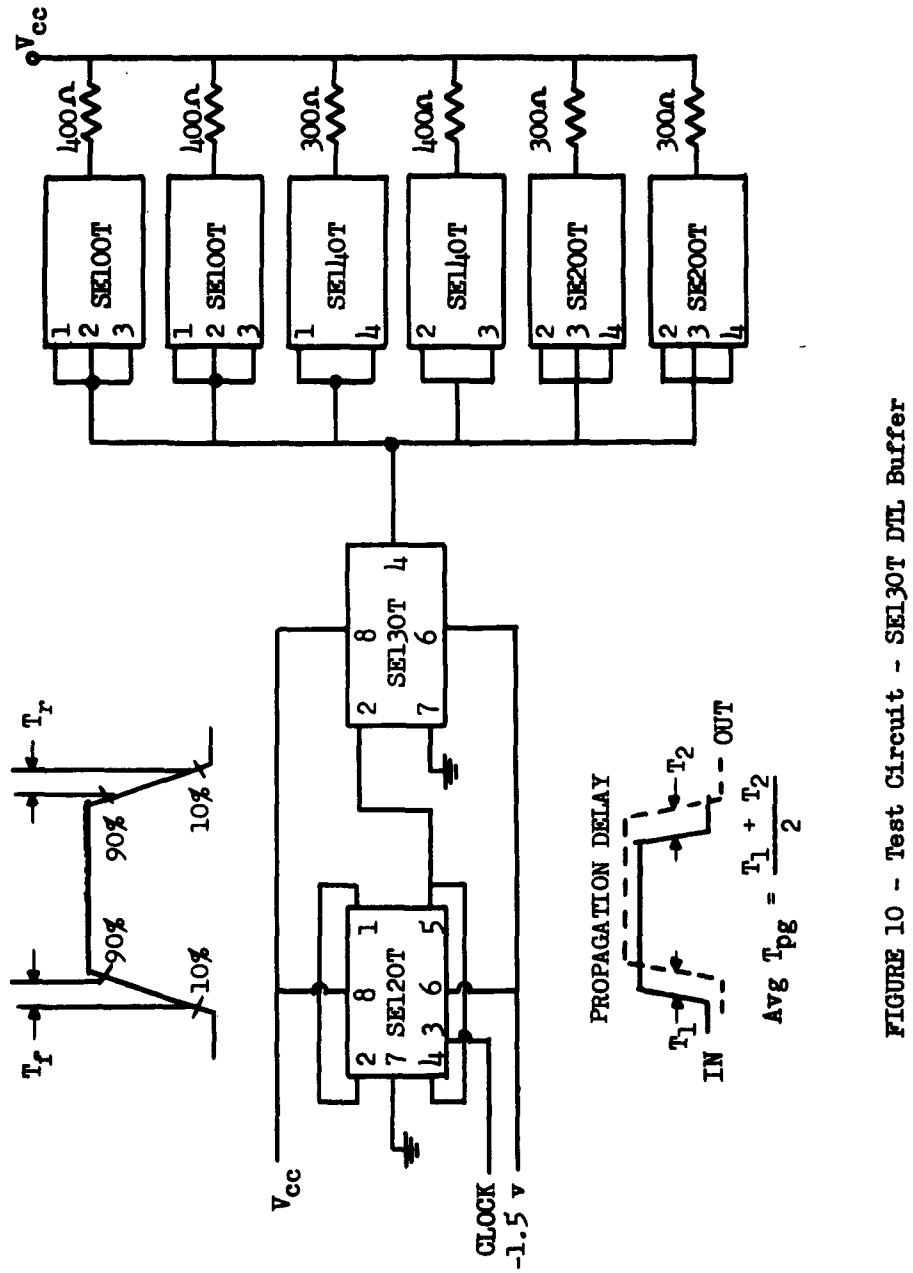



FIGURE 10 - Test Circuit - SE130T DTL Buffer

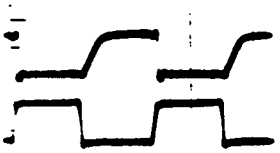
## SE140T DTL EXCLUSIVE-OR NETWORK
## (See figure 11)

Temp = 25° C; F = 1.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = A $\overline{B}$ (1,4)



Top Trace -
output = 0.75 $V_{pp}$

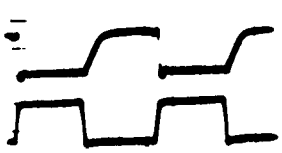
Bottom Trace -
input = 1.5 $V_{pp}$

$T_{r5}$ = 0.010 us

$T_f$ = 0.120 us

Propagation delay = 0.050 us

Input = $\overline{A}$ B (2, 3)



Top Trace -
output = 0.75 $V_{pp}$

Bottom Trace -
input = 1.5 $V_{pp}$

$T_{r5}$ = 0.010 us

$T_{f5}$ = 0.120 us

Propagation delay = 0.050 us

SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 25° C; F = 2.5 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = $A \cdot \overline{B}$

Top Trace -
output = 0.75 $V_{pp}$

Bottom Trace -
input = 1.5 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.050 us

Input = $\overline{A}$ B

Top Trace -
output = 0.75 $V_{pp}$

Bottom Trace -
input = 1.5 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.050 us

SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 25° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = A $\overline{B}$

Top Trace -
output = 1.7 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.089 us

Driver - SE140T
Load - SE140T

Input = $\overline{A}$ B

Top Trace -
output = 1.7 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.079 us

## SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 25° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = A $\overline{B}$

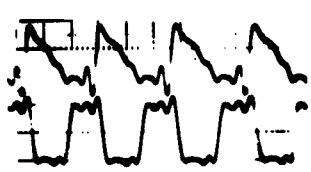
Top Trace -
output = 1.25 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.006 us

$T_f$ = 0.054 us

Input = $\overline{A}$ B



Top Trace -
output = 1.25 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.006 us

$T_f$ = 0.056 us

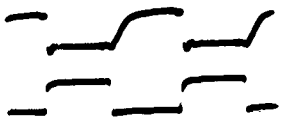
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 125° C; F = 1 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = A $\overline{B}$



Top Trace -
output = 0.60 $V_{pp}$

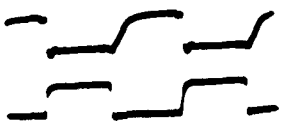
Bottom Trace -
input = 1.3 $V_{pp}$

$T_r$ = 0.10 us

$T_f$ = 0.110 us

Propagation delay = 0.045 us

Input = $\overline{A}$ B



Top Trace -
output = 0.60 $V_{pp}$

Bottom Trace -
input = 1.3 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.045 us

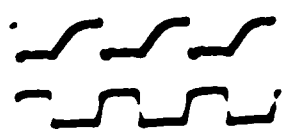
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 125° C; F = 2.5 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = A $\overline{B}$



Top Trace -
output = 0.60 $V_{pp}$

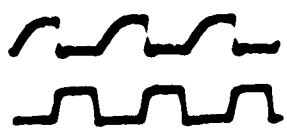
Bottom Trace -
input = 1.3 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.040 us

Input $\overline{A}$ B



Top Trace -
output = 0.60 $V_{pp}$

Bottom Trace -
input = 1.3 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.040 us

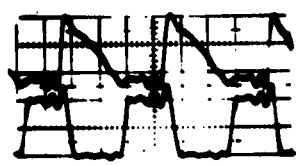
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 125° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = $A\bar{B}$



Top Trace -
output = 1.2 $V_{pp}$

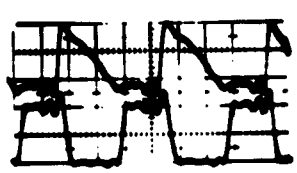
Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.079 us

Propagation delay = 0.033 us

Input = $\bar{A}B$



Top Trace -
output = 1.2 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.078 us

Propagation delay = 0.033 us

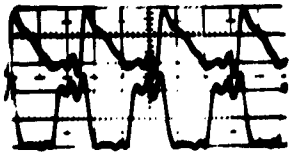
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = 125° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = A $\bar{B}$



Top Trace -
output = 1.0 $V_{pp}$

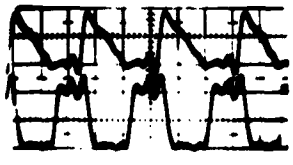
Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.057 us

Propagation delay = 0.0275 us

Input = $\bar{A}$ B



Top Trace -
output = 1.00 $V_{pp}$

Bottom Trace -
input = 2.0 $V_{pp}$

$T_r$ = 0.009 us

$T_f$ = 0.057 us

Propagation delay = 0.0275 us

SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = -55° C; F = 1.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = A $\overline{B}$

Top Trace -
output = 0.80 $V_{pp}$

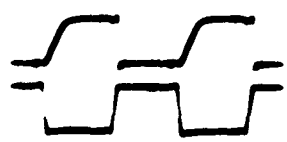
Bottom Trace -
input = 1.6 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.0475 us

Input = $\overline{A}$ B



Top Trace -
output = 0.80 $V_{pp}$

Bottom Trace -
input = 1.6 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.0475 us

SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = -55° C; F = 2.5 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE200T

Input = $A'\overline{B}$

Top Trace -
output = 0.80 $V_{pp}$

Bottom Trace -
input = 1.6 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.050 us

Input = $\overline{A}$ B

Top Trace -
output = 0.80 $V_{pp}$

Bottom Trace -
input = 1.6 $V_{pp}$

$T_r$ = 0.010 us

$T_f$ = 0.110 us

Propagation delay = 0.050 us

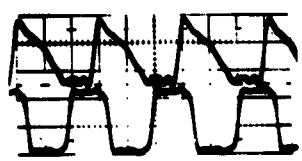
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = -55° C; F = 5.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = A $\overline{B}$



Top Trace -
output = 1.9 $V_{pp}$

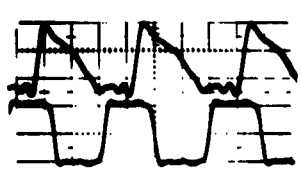
Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.018 us

$T_f$ = 0.085 us

Propagation delay = 0.050 us

Input = $\overline{A}$ B



Top Trace -
output = 1.9 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.014 us

$T_f$ = 0.084 us

Propagation delay = 0.050 us

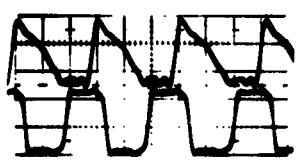
SE140T DTL EXCLUSIVE-OR NETWORK (Continued)
(See figure 11)

Temp = -55° C; F = 7.0 mc; N = 3; $V_{pp}$ = Voltage peak-to-peak

$V_{cc}$ = +4.5 v dc, -1.5 v dc

Driver - SE140T
Load - SE100T

Input = A $\overline{B}$



Top Trace -
output = 1.6 $V_{pp}$

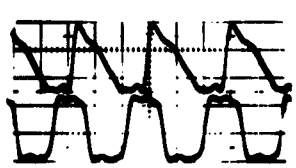
Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.011 us

$T_f$ = 0.065 us

Propagation delay = 0.050 us

Input = $\overline{A}$ B



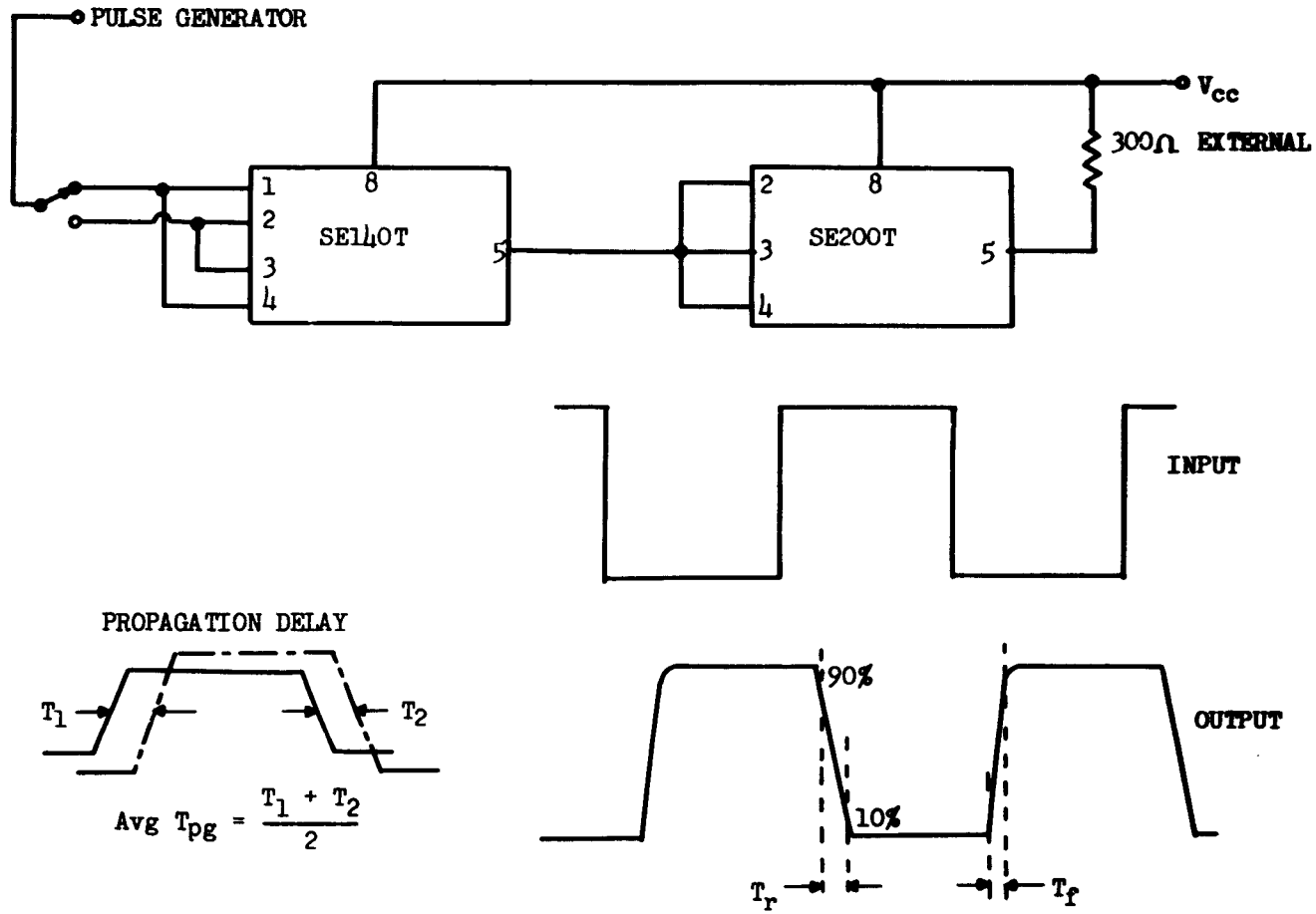
Top Trace -
output = 1.6 $V_{pp}$

Bottom Trace -
input = 2.5 $V_{pp}$

$T_r$ = 0.011 us

$T_f$ = 0.068 us

Propagation delay = 0.050 us



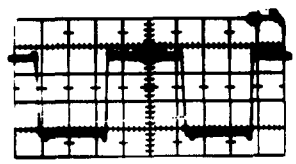

NADC-EL-6319

FIGURE 11 - Test Circuit - SE140T DTL Exclusive-OR Network

# TEST RESULTS FOR RCA DMC-100 DIGITAL MICROCIRCUIT ELEMENT
(See figure 12)

An Intercontinental pulse generator with a square wave input and pulse characteristics as shown below was used for the following tests:

($V_{pp}$ = Voltage peak-to-peak)



$T_r$ = 0.008 us

$T_f$ = 0.007 us

$V_{pp}$ = 1.35 v

F = 5 mc

Temp = +25° C; F = 100 cycles; N = 1

Driver - DMC-100
Load - DMC-100

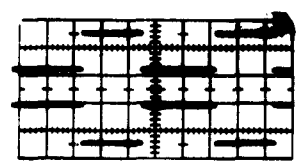
$T_{r2}$ = *

$T_{f2}$ = *

$T_{s2}$ = *

$T_{d2}$ = *

$V_{pp2}$ = *



Top Trace - input

Bottom Trace - output

* *too fast to measure at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = 25° C; F = 2 mc; N = 1

Driver - DMC-100
Load - DMC-100

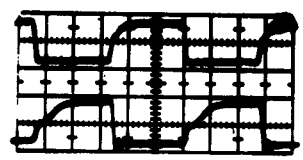
$T_{r2}$ = 0.009 us

$T_{f2}$ = 1.16 (90%) - 0.046 (50%) us

$T_{s2}$ = 0.011 us

$T_{d2}$ = 0.013 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = +25° C; F = 5 mc; N = 1

Driver - DMC-100
Load - DMC-100

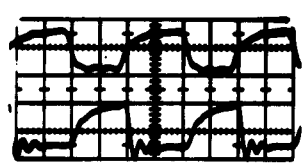
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.061 (90%) - 0.013 (50%) us

$T_{s2}$ = 0.014 us

$T_{d2}$ = 0.014 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = +25° C; F = 10 mc; N = 1

Driver - DMC-100
Load - DMC-100

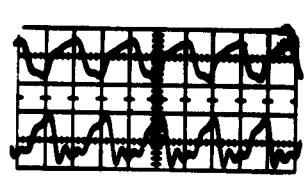
$T_{r2}$ = 0.007 us

$T_{f2}$ = 0.025 (90%) - 0.005 (10%) us

$T_{s2}$ = 0.014 us

$T_{d2}$ = 0.013 us

$V_{pp2}$ = 2.4 v



Top Trace - input

Bottom Trace - output

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = -55° C; F = 100 cycles; N = 1

Driver - DMC-100
Load - DMC-100

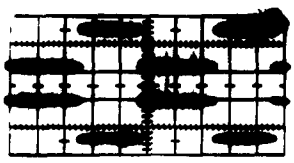
$T_{r2}$ = *

$T_{f2}$ = *

$T_{s2}$ = *

$T_{d2}$ = *

$V_{pp2}$ = *



Top Trace - input

Bottom Trace - output

Temp = -55° C; F = 2 mc; N = 1

Driver - DMC-100
Load - DMC-100

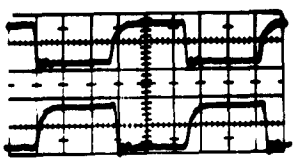
$T_{r2}$ = 0.010 us

$T_{f2}$ = 0.060 (90%) - 0.017 (50%) us

$T_{s2}$ = 0.090 us

$T_{d2}$ = 0.010 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = -55° C; F = 5 mc; N = 1

Driver - DMC-100
Load - DMC-100

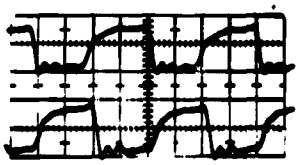
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.053 (90%) - 0.012 (50%) us

$T_{s2}$ = 0.014 us

$T_{d2}$ = 0.017 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

* *Too fast to measure at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = -55° C; F = 10 mc; N = 1

Driver - DMC-100
Load - DMC-100

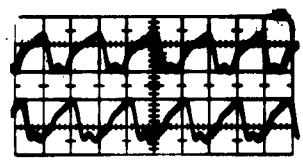
$T_{r2}$ = 0.010 us

$T_{f2}$ = 0.044 (90%) - 0.022 (50%) us

$T_{s2}$ = *

$T_{d2}$ = *

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = +125° C; F = 100 cycles; N = 1

Driver - DMC-100
Load - DMC-100

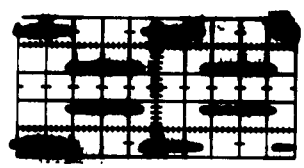
$T_{r2}$ = **

$T_{f2}$ = **

$T_{s2}$ = **

$T_{d2}$ = **

$V_{pp2}$ = **



Top Trace - input

Bottom Trace - output

Temp = +125° C; F = 2 mc; N = 1

Driver - DMC-100
Load - DMC-100

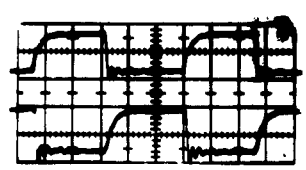
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.050 (90%) - 0.014 (50%) us

$T_{s2}$ = 0.006 us

$T_{d2}$ = 0.006 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

* *No reading obtained because of distortion.*

** *Too fast to measure at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = +125° C; F = 5 mc; N = 1

Driver - DMC-100
Load - DMC-100

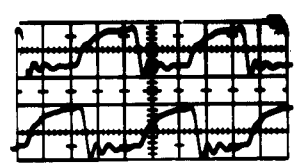
$T_{r2}$ = 0.009 us

$T_{f2}$ = 0.048 (90%) - 0.011 (50%) us

$T_{s2}$ = 0.010 us

$T_{d2}$ = 0.008 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = +125° C; F = 10 mc; N = 1

Driver - DMC-100
Load - DMC-100

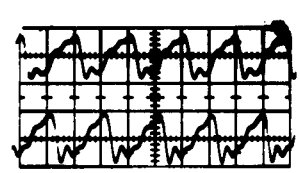
$T_{r2}$ = 0.007 us

$T_{f2}$ = 0.042 (90%) - 0.020 (50%) us

$T_{s2}$ = *

$T_{d2}$ = 0.011 us

$V_{pp2}$ = 2.9 v

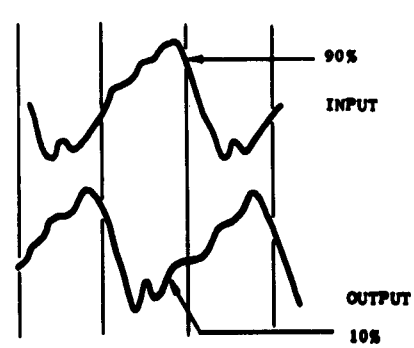


Top Trace - input

Bottom Trace - output

* *No reading obtained because of distortion.*

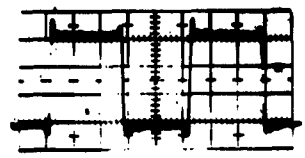
*No reading was recorded for $T_s$ at 10 mc because it appears as though the output 10% precedes the input 90%.*



DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

An Intercontinental pulse generator with a square wave input and pulse characteristics as shown below was used for the following tests:

($V_{pp}$ = Voltage peak-to-peak)

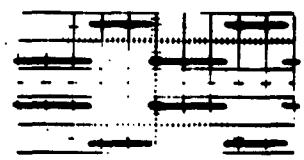


$T_r$ = 0.010 us
$T_f$ = 0.011 us
$V_{pp}$ = 1.68 v
F = 5 mc

Temp = 25° C; F = 100 cycles; N = 4

Driver - DMC-100
Load - DMC-100

$T_{r2}$ = *
$T_{f2}$ = *
$T_{s2}$ = *
$T_{d2}$ = *
$V_{pp2}$ = *



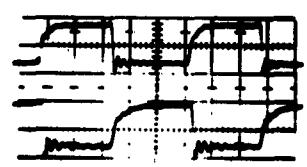
Top Trace - input

Bottom Trace - output

Temp = 25° C; F = 2 mc; N = 4

Driver - DMC-100
Load - DMC-100

$T_{r2}$ = 0.008 us
$T_{f2}$ = 0.081 (90%) - 0.013 (50%) us
$T_{s2}$ = 0.005 us
$T_{d2}$ = 0.012 us
$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

* *Too fast to measure at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = 25° C; F = 5 mc; N = 4

Driver - DMC-100
Load - DMC-100

$T_{r2}$ = 0.012 us

$T_{f2}$ = 0.074 (90%) - 0.013 (50%) us

$T_{s2}$ = 0.005 us

$T_{d2}$ = 0.011 us

$V_{pp2}$ = 2.8 v

Top Trace - input

Bottom Trace - output

Temp = 25° C; F = 10 mc; N = 4

Driver - DMC-100
Load - DMC-100

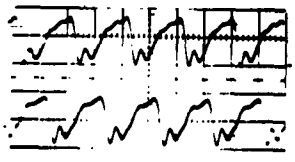
$T_{r2}$ = 0.007 us

$T_{f2}$ = 0.046 (90%) - 0.015 (50%) us

$T_{s2}$ = *

$T_{d2}$ = 0.015

$V_{pp2}$ = 2.8 v



Top Trace - input

Bottom Trace - output

Temp = -55° C; F = 100 cycles; N = 4

Driver - DMC-100
Load - DMC-100

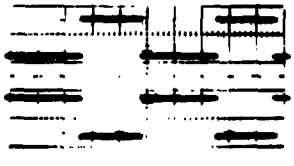
$T_{r2}$ = **

$T_{f2}$ = **

$T_{s2}$ = **

$T_{d2}$ = **

$V_{pp2}$ = **



Top Trace - input

Bottom Trace - output

* *No reading obtained because of distortion.*

** *Too fast to measure at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = -55° C; F = 2 mc; N = 4

Driver - DMC-100
Load - DMC-100

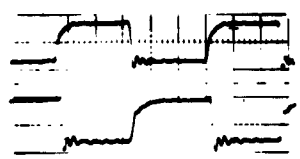
$T_{r2}$ = 0.010 us

$T_{f2}$ = 0.050 (90%) - 0.009 (50%) us

$T_{s2}$ = 0.009 us

$T_{d2}$ = 0.015 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = -55° C; F = 5 mc; N = 4

Driver - DMC-100
Load - DMC-100

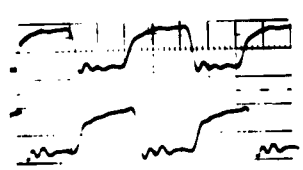
$T_{r2}$ = 0.007 us

$T_{f2}$ = 0.045 (90%) - 0.006 (50%) us

$T_{s2}$ = 0.010 us

$T_{d2}$ = 0.018 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

Temp = -55° C; F = 10 mc; N = 4

Driver - DMC-100
Load - DMC-100

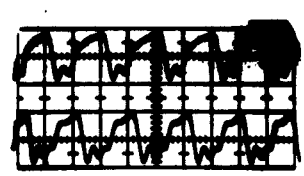
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.039 (90%) - 0.019 (50%) us

$T_{s2}$ = *

$T_{d2}$ = 0.014 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

* *No reading obtained because of distortion.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = 125° C; F = 100 cycles; N = 4

Driver - DMC-100
Load - DMC-100

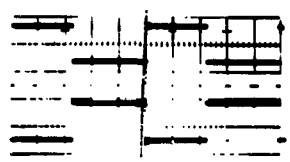
$T_{r2}$ = *

$T_{f2}$ = *

$T_{s2}$ = *

$T_{d2}$ = *

$V_{pp2}$ = *



Top Trace - input

Bottom Trace - output

Temp = 125° C; F = 2 mc; N = 4

Driver - DMC-100
Load - DMC-100

$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.080 (90%) - 0.017 (50%) us

$T_{s2}$ = 0.004 us

$T_{d2}$ = 0.007 us

$V_{pp2}$ = 2.9 v

Top Trace - input

Bottom Trace - output

Temp = 125° C; F = 5 mc; N = 4

Driver - DMC-100
Load - DMC-100

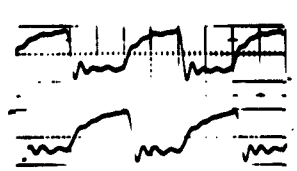
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.075 (90%) - 0.012 (50%) us

$T_{s2}$ = 0.004 us

$T_{d2}$ = 0.007 us

$V_{pp2}$ = 2.9 v



Top Trace - input

Bottom Trace - output

* *Too fast to obtain reading at this low frequency.*

DMC-100 DIGITAL MICROCIRCUIT ELEMENT (Continued)
(See figure 12)

Temp = 125° C; F = 10 mc; N = 4

Driver - DMC-100
Load - DMC-100

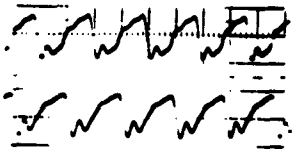
$T_{r2}$ = 0.008 us

$T_{f2}$ = 0.041 (90%) - 0.017 (50%) us

$T_{s2}$ = *

$T_{d2}$ = 0.019 us

$V_{pp2}$ = 2.5 v



Top Trace - input

Bottom Trace - output

* *No reading obtained because of distortion.*

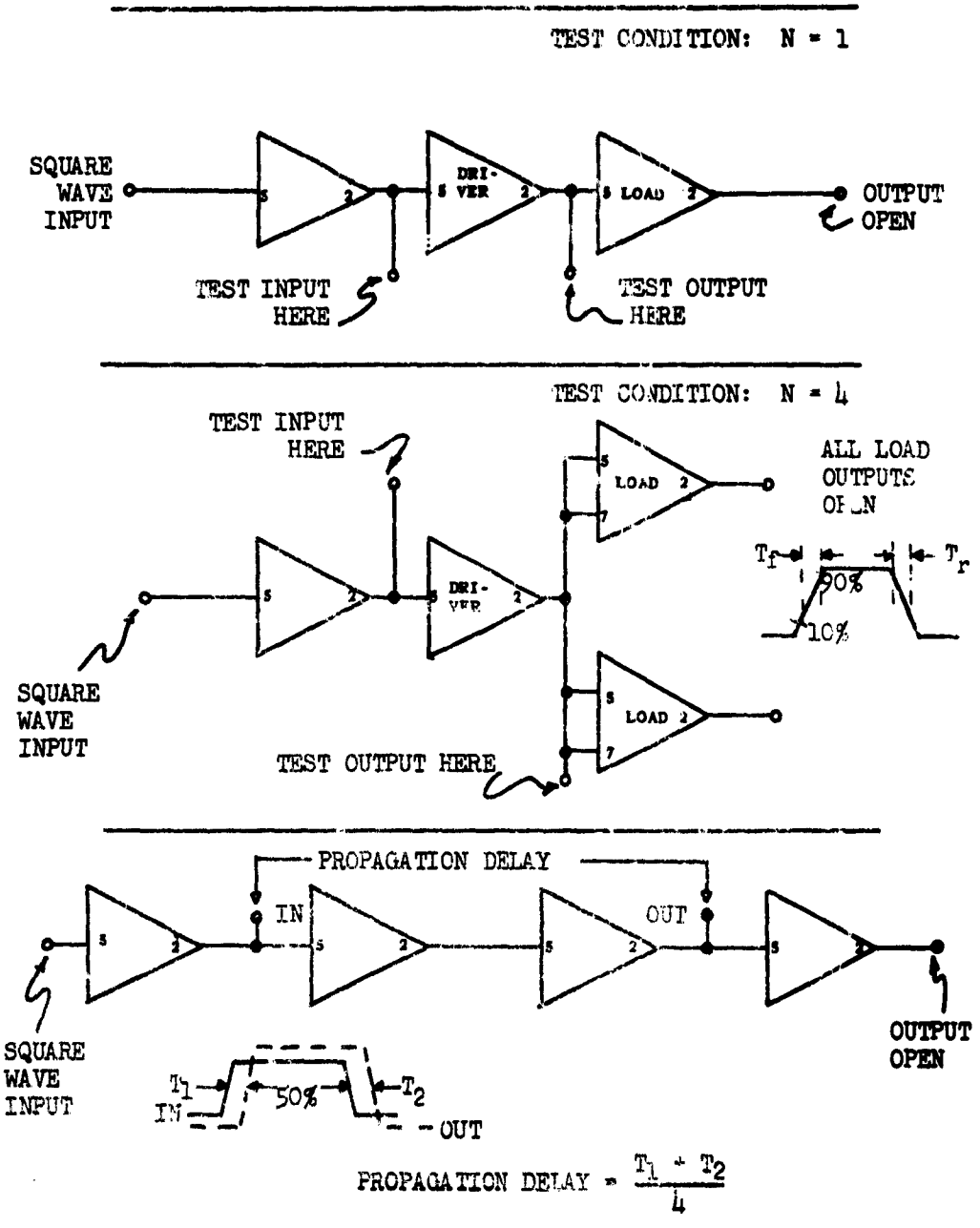



FIGURE 12 - Test Circuit - RCA DMC-100 Digital Microcircuit

# TEST RESULTS FOR PACIFIC SEMICONDUCTORS MICROCIRCUIT LOGIC ELEMENTS

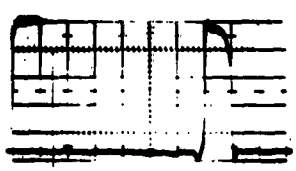
## PCF-101 SET-RESET FLIP-FLOP

Test Condition 1: Source and test unit in test chamber; load maintained at room temperature.

(See figure 13)

A pulse generator was used for the clock in the following tests. The clock pulse characteristics for tests at +25° and +125° C are shown below:

($V_{pp}$ = Voltage peak-to-peak)



Top Trace - input = 0.9 $V_{pp}$

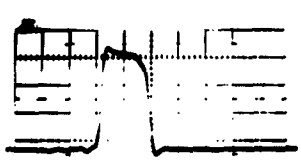
Bottom Trace - output

$T_r$ = 0.010 us

$T_f$ = 0.015 us

Pulse width = 0.095 us at 50 percent

The clock pulse characteristics for tests at -45° C were as follows:



Top Trace - input = 1.82 $V_{pp}$

Bottom Trace - output

$T_r$ = 0.010 us

$T_f$ = 0.013 us

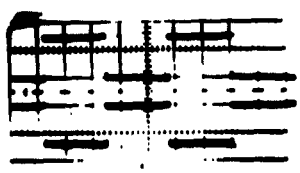
Pulse width = 0.086 us at 50 percent

## PCF-101 SET-RESET FLIP-FLOP (Continued)

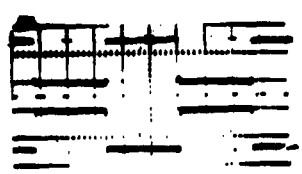
Test Condition 1
(See figure 13)

Temp = +25° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

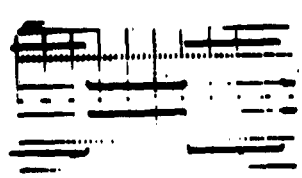
F = 1.0 mc
Output = 0.79 $V_{pp}$
$T_r$ = 0.054 us
$T_f$ = 0.075 us

F = 1.0 mc
Output = 0.74 $V_{pp}$
$T_r$ = 0.058 us
$T_f$ = 0.062 us

F = 2.0 mc
Output = 0.79 $V_{pp}$
$T_r$ = 0.045 us
$T_f$ = 0.065 us



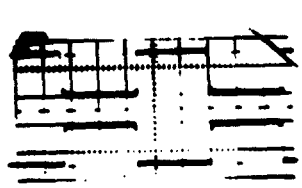
F = 2.0 mc
Output = 0.76 $V_{pp}$
$T_r$ = 0.056 us
$T_f$ = 0.058 us

F = 3.0 mc
Output = 0.79 $V_{pp}$
$T_r$ = 0.040 us
$T_f$ = 0.059 us



F = 3.0 mc
Output = 0.79 $V_{pp}$
$T_r$ = 0.057 us
$T_f$ = 0.049 us

F = 4.0 mc
Output = 0.79 $V_{pp}$
$T_r$ = 0.045 us
$T_f$ = 0.064 us



F = 4.0 mc
Output = 0.77 $V_{pp}$
$T_r$ = 0.065 us
$T_f$ = 0.059 us

PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 1
(See figure 13)

Temp = +25° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

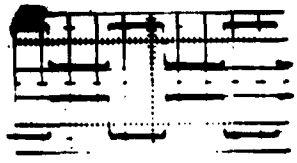
Driver - PCF-101; Load - PCG-101

F = 5.0 mc

Output = 0.79 $V_{pp}$

$T_r$ = 0.043 us

$T_f$ = 0.066 us



F = 5.0 mc

Output = 0.77 $V_{pp}$

$T_r$ = 0.059 us

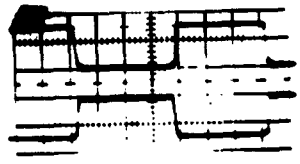
$T_f$ = 0.059 us

F = 6.0 mc

Output = 0.79 $V_{pp}$

$T_r$ = 0.047 us

$T_f$ = 0.067 us



F = 6.0 mc

Output = 0.77 $V_{pp}$

$T_r$ = 0.060 us

$T_f$ = 0.058 us

Temp = +125° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

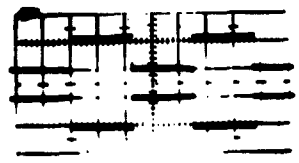
Driver - PCF-101; Load PCG-101

F = 1.0 mc

Output = 0.60 $V_{pp}$

$T_r$ = 0.055 us

$T_f$ = 0.060 us



F = 1.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.040 us

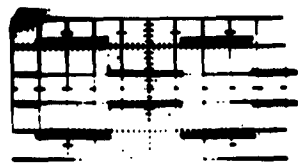
$T_f$ = 0.034 us

F = 2.0 mc

Output = 0.060 $V_{pp}$

$T_r$ = 0.038 us

$T_f$ = 0.060 us



F = 2.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.040 us

$T_f$ = 0.048 us

PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 1
(See figure 13)

Temp = +125° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

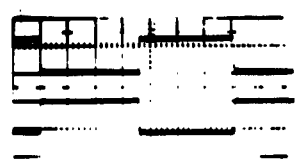
Driver - PCF-101; Load - PCG-101

F = 3.0 mc

Output = 0.60 $V_{pp}$

$T_r$ = 0.035 us

$T_f$ = 0.054 us



F = 3.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.037 us

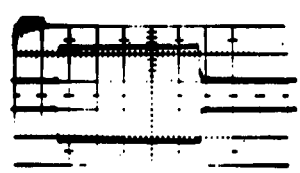
$T_f$ = 0.040 us

F = 4.0 mc

Output = 0.060 $V_{pp}$

$T_r$ = 0.037 us

$T_f$ = 0.065 us



F = 4.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.030 us

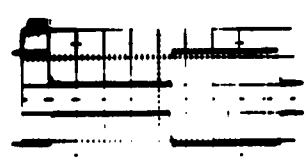
$T_f$ = 0.043 us

F = 5.0 mc

Output = 0.60 $V_{pp}$

$T_r$ = 0.025 us

$T_f$ = 0.058 us



F = 5.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.028 us

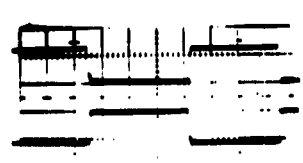
$T_f$ = 0.042 us

F = 6.0 mc

Output = 0.60 $V_{pp}$

$T_r$ = 0.028 us

$T_f$ = 0.067 us



F = 6.0 mc

Output = 0.58 $V_{pp}$

$T_r$ = 0.030 us

$T_f$ = 0.048 us

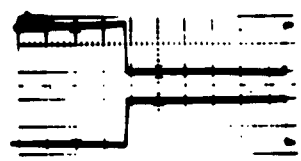
## PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 1
(See figure 13)

Temp = -45° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

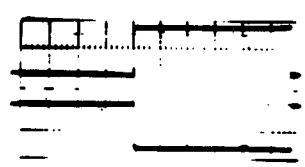
Driver - PCF-101; Load - PCG-101

F = 1.0 mc
Output = 0.92 $V_{pp}$
$T_r$ = 0.110 us
$T_f$ = 0.097 us



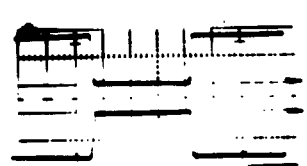
F = 1.0 mc
Output = 0.92 $V_{pp}$
$T_r$ = 0.155 us
$T_f$ = 0.091 us

F = 2.0 mc
Input = 0.92 $V_{pp}$
$T_r$ = 0.109 us
$T_f$ = 0.093 us



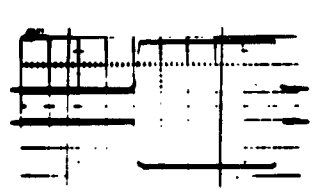
F = 2.0 mc
Input = 0.92 $V_{pp}$
$T_r$ = 0.156 us
$T_f$ = 0.083 us

F = 3.0 mc
Output = 0.93 $V_{pp}$
$T_r$ = 0.110 us
$T_f$ = 0.101 us



F = 3.0 mc
Output = 0.89 $V_{pp}$
$T_r$ = 0.153 us
$T_f$ = 0.082 us

F = 4.0 mc
Output = 0.93 $V_{pp}$
$T_r$ = 0.110 us
$T_f$ = 0.102 us



F = 4.0 mc
Output = 0.88 $V_{pp}$
$T_r$ = 0.146 us
$T_f$ = 0.081 us

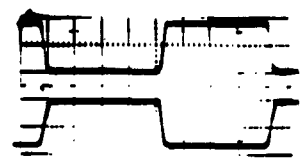
PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 1
(See figure 13)

Temp = -45° C; N = 4; $V_{cc}$ = +3.0 v dc; $V_{pp}$ = Voltage peak-to-peak

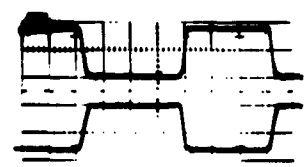
Driver - PCF-101; Load - PCG-101

F = 5.0 mc
Output = 0.93 $V_{pp}$
$T_r$ = 0.106 us
$T_f$ = 0.093 us



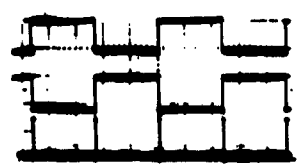
F = 5.0 mc
Output = 0.88 $V_{pp}$
$T_r$ = 0.158 us
$T_f$ = 0.087 us

F = 6.0 mc
Output = 0.93 $V_{pp}$
$T_r$ = 0.099 us
$T_f$ = 0.096 us



F = 6.0 mc
Output = 0.88 $V_{pp}$
$T_r$ = 0.142 us
$T_f$ = 0.088 us

Temp = +25° or +125° C; Clock input pulse between 0.9 and 2.72 v dc



Top Trace - outputs of test circuit to load

Bottom Trace - clock pulse from pulse generator

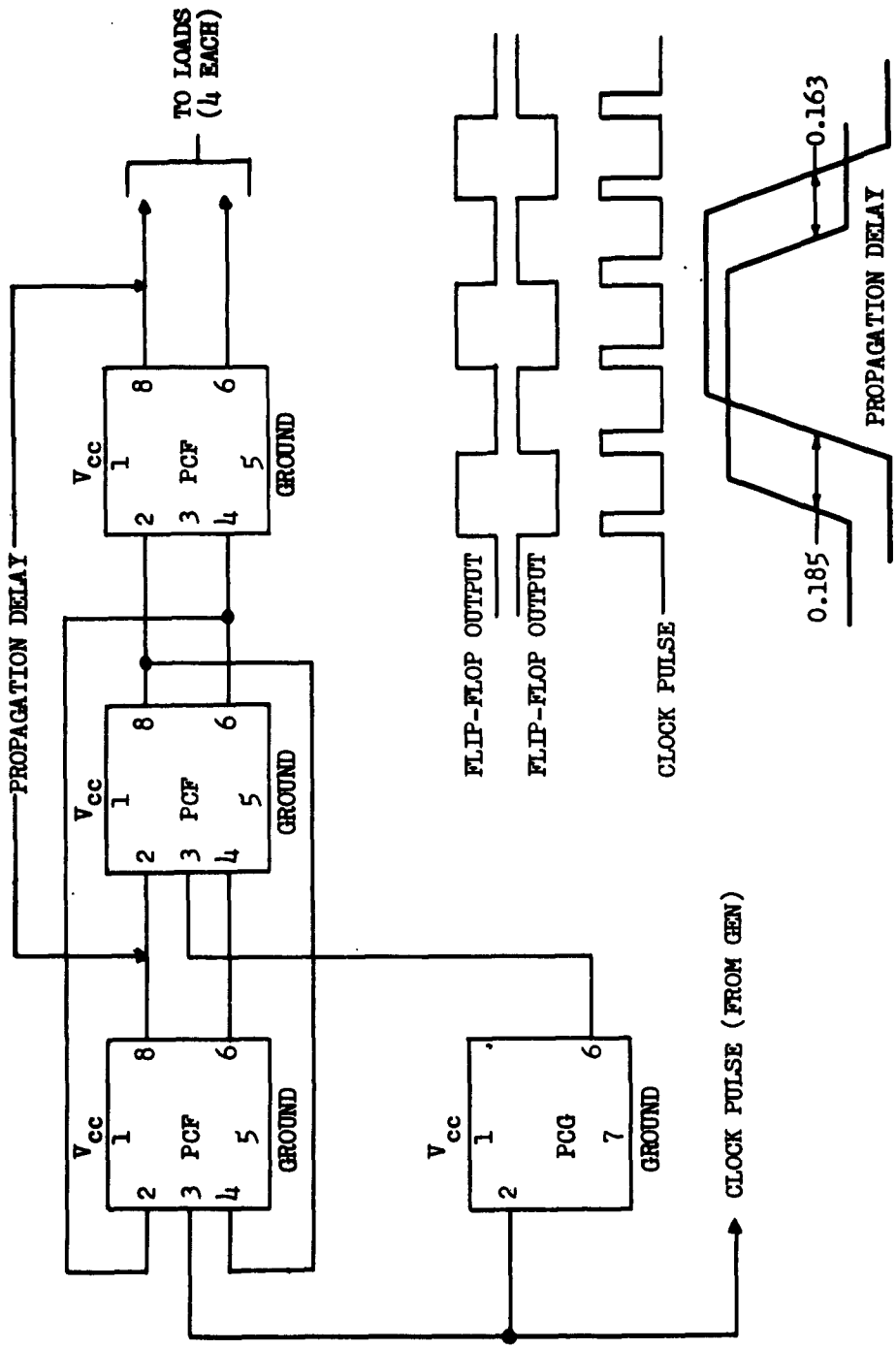



FIGURE 13 - Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 1)

PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 2: Test unit in test chamber at -55° C; Source and load maintained at room temperature (See figure 14)

| Freq (mc) | Input $V_{pp}$ (v dc) | Output $V_{pp}$ (v dc) | $T_r$ (us) | $T_f$ (us) |
|---|---|---|---|---|
| 1.0 | 1 | 0.86 | 0.171 | 0.087 |
| | 1 | 0.89 | 0.143 | 0.110 |
| 2.0 | 1 | 0.86 | 0.176 | 0.093 |
| | 1 | 0.89 | 0.145 | 0.115 |
| 3.0 | 1 | 0.86 | 0.176 | 0.088 |
| | 1 | 0.89 | 0.143 | 0.112 |
| 4.0 | 1 | 0.86 | 0.178 | 0.088 |
| | 1 | 0.89 | 0.146 | 0.111 |
| 5.0 | 1 | 0.86 | 0.176 | 0.091 |
| | 1 | 0.89 | 0.144 | 0.106 |
| 6.0 | 1 | 0.86 | 0.176 | 0.089 |
| | 1 | 0.89 | 0.143 | 0.107 |

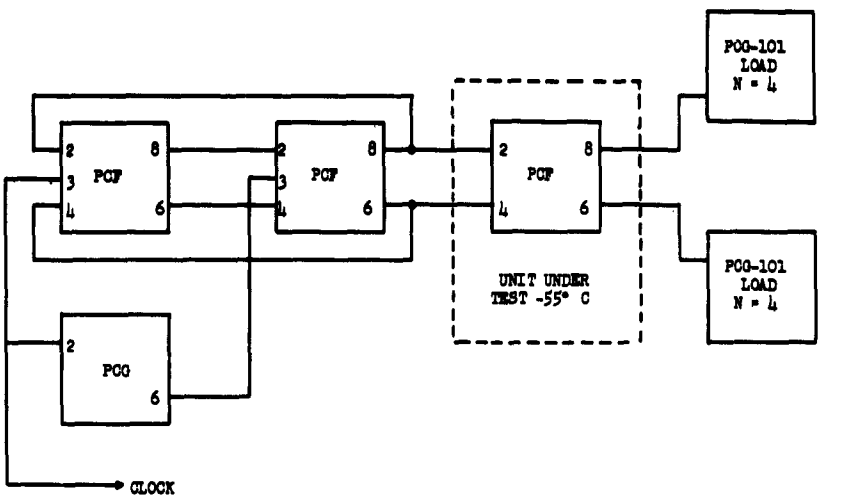



FIGURE 14 - Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 2)

PCF-101 SET-RESET FLIP-FLOP (Continued)

Test Condition 3: Test unit and load in test chamber at -55° C; Source maintained at room temperature (See figure 15)

| Freq (mc) | Input $V_{pp}$ (v dc) | Output $V_{pp}$ (v dc) | $T_r$ (us) | $T_f$ (us) |
|---|---|---|---|---|
| 1.0 | 0.87 | 0.87 | 0.142 | 0.079 |
| | 0.87 | 0.91 | 0.136 | 0.089 |
| 2.0 | 0.87 | 0.87 | 0.139 | 0.085 |
| | 0.87 | 0.91 | 0.127 | 0.093 |
| 3.0 | 0.87 | 0.87 | 0.132 | 0.081 |
| | 0.87 | 0.91 | 0.139 | 0.098 |
| 4.0 | 0.87 | 0.87 | 0.163 | 0.099 |
| | 0.87 | 0.91 | 0.166 | 0.108 |
| 5.0 | 0.87 | 0.87 | 0.181 | 0.101 |
| | 0.87 | 0.91 | 0.133 | 0.084 |
| 6.0 | 0.87 | 0.87 | 0.143 | 0.080 |
| | 0.87 | 0.91 | 0.128 | 0.089 |

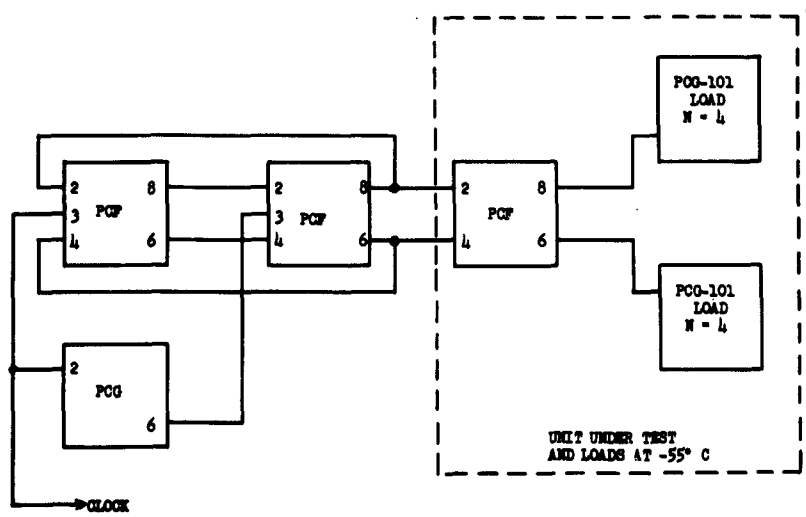
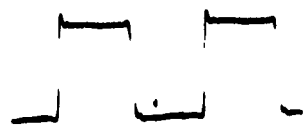



FIGURE 15 - Test Circuit - PCF-101 Set-Reset Flip-Flop (Test Condition 3)

PCG-101 DUAL NAND GATE
(See figure 16)

In each of the following tests, an Intercontinental pulse generator was used for the clock. Outputs of the pulse generator are as follows:



F = 2.0 mc

$T_r$ = 0.012 us

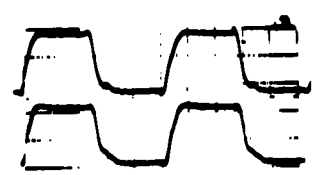
$T_f$ = 0.012 us

$V_{pp}$ = 0.9 v dc

Temp = +25° C; $V_{cc}$ = 3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc



$T_{s5}$ = 0.010 us

$T_{d5}$ = 0.010 us

$T_{r5}$ = 0.037 us

$T_{f5}$ = 0.063 us (10% to 90%)

$T_{f5}$ = 0.014 us (10% to 50%)

$V_{pp5}$ = 0.5 v dc

Top Trace - input

Bottom Trace - output

## PCG-101 DUAL NAND GATE (Continued)
(See figure 16)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

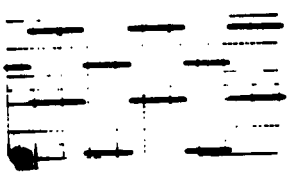
$T_{s5}$ = *

$T_{d5}$ = *

$T_{r5}$ = *

$T_{f5}$ = *

$V_{pp5}$ = *



Top Trace - input

Bottom Trace - output

F = 2.0 mc

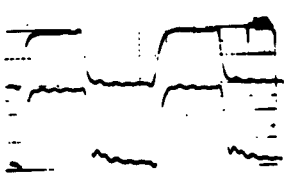
$T_{s5}$ = 0.007 us

$T_{d5}$ = 0.007 us

$T_{r5}$ = 0.024 us

$T_{f5}$ = 0.019 us

$V_{pp5}$ = 0.28 v dc



Top Trace - input

Bottom Trace - output

F = 5.0 mc

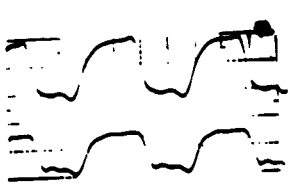
$T_{s5}$ = 0.007 us

$T_{d5}$ = 0.007 us

$T_{r5}$ = 0.034 us

$T_{f5}$ = 0.021 us

$V_{pp5}$ = 0.29 v dc



Top Trace - input

Bottom Trace - output

* *Too fast to measure at this low frequency*

PCG-101 DUAL NAND GATE (Continued)
(See figure 16)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 10.0 mc

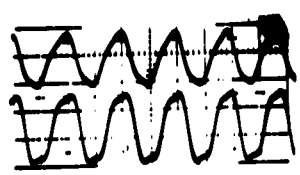
$T_{s5}$ = 0.008 us

$T_{d5}$ = 0.013 us

$T_{r5}$ = 0.032 us

$T_{f5}$ = 0.017 us

$V_{pp5}$ = 0.25 v dc



Top Trace - input

Bottom Trace - output

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

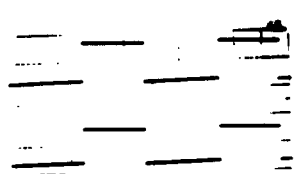
$T_{s5}$ = *

$T_{d5}$ = *

$T_{r5}$ = *

$T_{f5}$ = *

$V_{pp5}$ = *



Top Trace - input

Bottom Trace - output

* *too fast to measure at this low frequency*

PCG-101 DUAL NAND GATE (Continued)
(See figure 16)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc

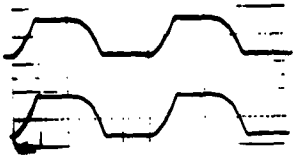
$T_{s5}$ = 0.007 us

$T_{d5}$ = 0.008 us

$T_{r5}$ = 0.063 us

$T_{f5}$ = 0.076 us

$V_{pp5}$ = 0.70 v dc



Top Trace - input

Bottom Trace - output

F = 5.0 mc

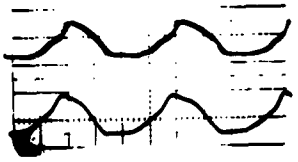
$T_{s5}$ = 0.016 us

$T_{d5}$ = 0.010 us

$T_{r5}$ = 0.052 us

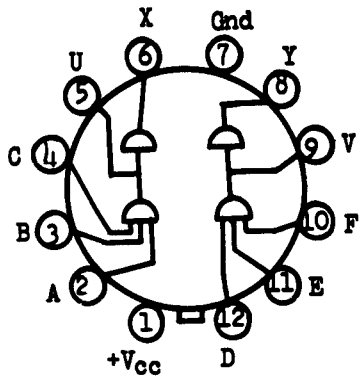
$T_{f5}$ = 0.059 us

$V_{pp5}$ = 0.62 v dc

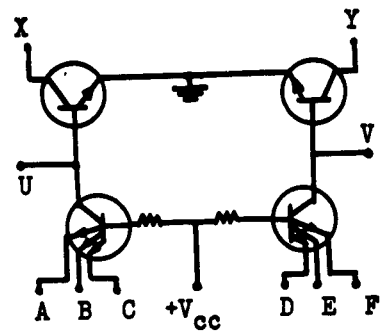


Top Trace - input

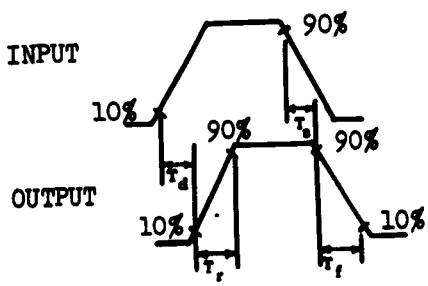
Bottom Trace - output

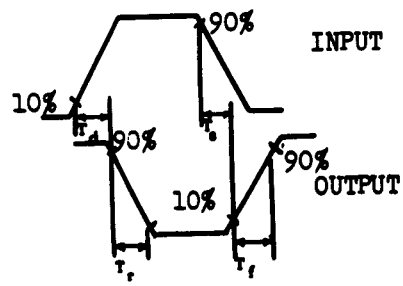


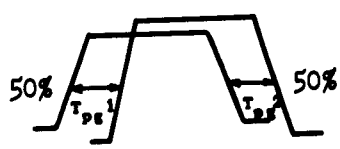

BOTTOM VIEW




SCHEMATIC




PROPAGATION DELAY

$X = \overline{ABC} + \overline{U}$

$Y = \overline{DEF} + \overline{V}$

$U = ABC$

$V = DEF$

FIGURE 16 - PCG-101 Dual NAND Gate

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 17)

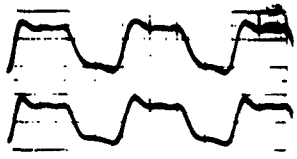
In the following tests, outputs at pins 5 and 9 were compared to see if both circuits in the same can are identical.

Temp = +25° C; $V_{cc}$ = 3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s5}$ = 0.008 us
$T_{d5}$ = 0.008 us
$T_{r5}$ = 0.014 us
$T_{f5}$ = 0.018 us
$V_{pp5}$ = 0.30 v dc



$T_{s9}$ = 0.008 us
$T_{d9}$ = 0.007 us
$T_{r9}$ = 0.013 us
$T_{f9}$ = 0.019 us
$V_{pp9}$ = 0.25 v dc

Top Trace - pin 5

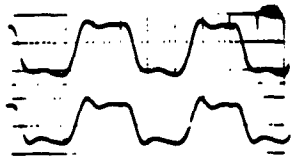
Bottom Trace - pin 9

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s5}$ = 0.008 us
$T_{d5}$ = 0.008 us
$T_{r5}$ = 0.022 us
$T_{f5}$ = 0.014 us
$V_{pp5}$ = 0.20 v dc



$T_{s9}$ = 0.007 us
$T_{d9}$ = 0.006 us
$T_{r9}$ = 0.020 us
$T_{f9}$ = 0.012 us
$V_{pp9}$ = 0.135 v dc

Top Trace - pin 5

Bottom Trace - pin 9

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 17)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s5}$ = 0.010 us

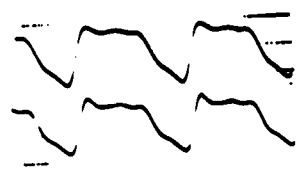
$T_{d5}$ = 0.008 us

$T_{r5}$ = 0.013 us

$T_{f5}$ = 0.052 us (10% to 90%)

$T_{f5}$ = 0.015 us (10% to 50%)

$V_{pp5}$ = 0.330 v dc



Top Trace - pin 5

Bottom Trace - pin 9

$T_{s9}$ = 0.010 us

$T_{d9}$ = 0.009 us

$T_{r9}$ = 0.015 us

$T_{f9}$ = 0.054 us (10% to 90%)

$T_{f9}$ = 0.015 us (10% to 50%)

$V_{pp9}$ = 0.40 v dc

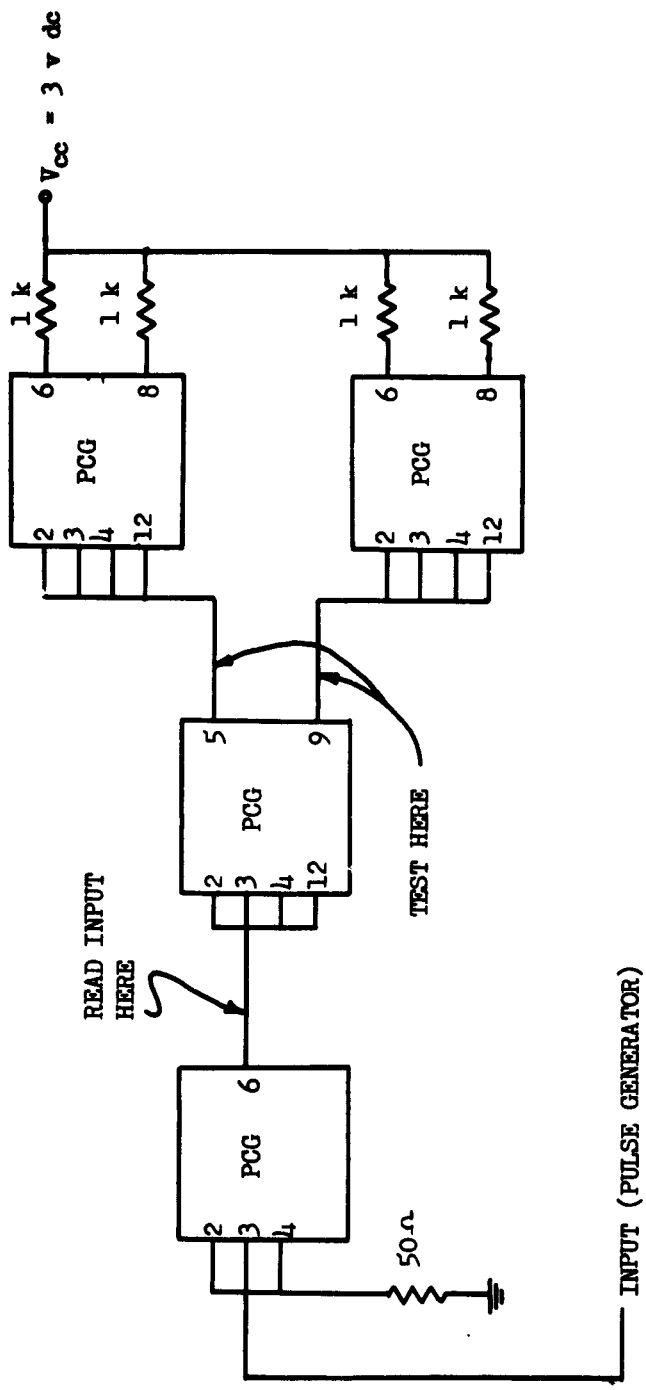
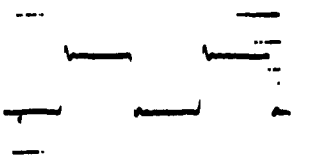



FIGURE 17 - Test Circuit - PCG-101 Dual NAND Gate

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 18)

Output of Intercontinental pulse generator was used for this test:



F = 2.0 mc

$T_r$ = 0.011 us

$T_f$ = 0.011 us

$V_{pp}$ = 1.0 v dc

Temp = +25° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc

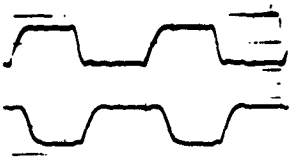
$T_{s6}$ = 0.021 us

$T_{d6}$ = 0.054 us

$T_{r6}$ = 0.047 us

$T_{f6}$ = 0.038 us

$V_{pp6}$ = 0.69 v dc



Top Trace - input

Bottom Trace - output

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 18)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

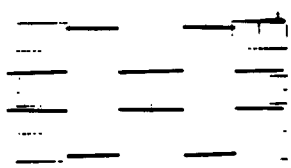
$T_{s6}$ = *

$T_{d6}$ = *

$T_{r6}$ = *

$T_{f6}$ = *

$V_{pp6}$ = *



Top Trace - input

Bottom Trace - output

F = 2.0 mc

$T_{s6}$ = 0.029 us

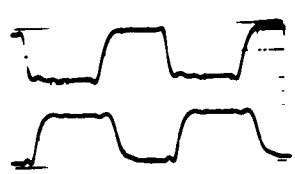
$T_{d6}$ = 0.037 us

$T_{r6}$ = 0.070 us (10% to 90%)

$T_{r6}$ = 0.021 us (10% to 50%)

$T_{f6}$ = 0.044 us

$V_{pp6}$ = 0.55 v dc



Top Trace - input

Bottom Trace - output

* *too fast to measure at this low frequency*

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 18)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

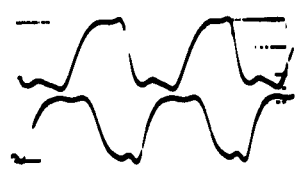
$T_{s6}$ = 0.028 us

$T_{d6}$ = 0.037 us

$T_{r6}$ = 0.031 us

$T_{f6}$ = 0.033 us

$V_{pp6}$ = 0.433 v dc



Top Trace - input

Bottom Trace - output

F = 10.0 mc

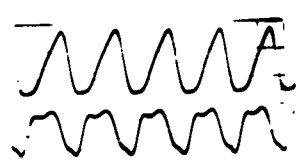
$T_{s6}$ = 0.024 us

$T_{d6}$ = 0.039 us

$T_{r6}$ = 0.015 us

$T_{f6}$ = 0.022 us

$V_{pp6}$ = 0.14 v dc



Top Trace - input

Bottom Trace - output

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 18)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

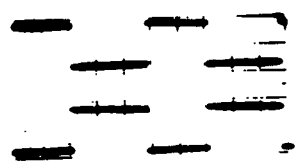
$T_{s6}$ = *

$T_{d6}$ = *

$T_{r6}$ = *

$T_{f6}$ = *

$V_{pp6}$ = *



Top Trace - input

Bottom Trace - output

F = 2.0 mc

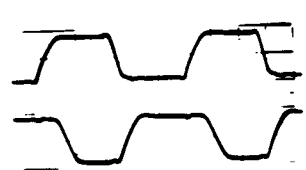
$T_{s6}$ = 0.027 us

$T_{d6}$ = 0.079 us

$T_{r6}$ = 0.058 us

$T_{f6}$ = 0.051 us

$V_{pp6}$ = 0.83 v dc



Top Trace - input

Bottom Trace - output

* *Too fast to measure at this low frequency*

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 18)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

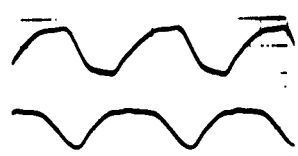
$T_{s6}$ = 0.024 us

$T_{d6}$ = 0.064 us

$T_{r6}$ = 0.051 us

$T_{f6}$ = 0.048 us

$V_{pp6}$ = 0.69 v dc



Top Trace - input

Bottom Trace - output

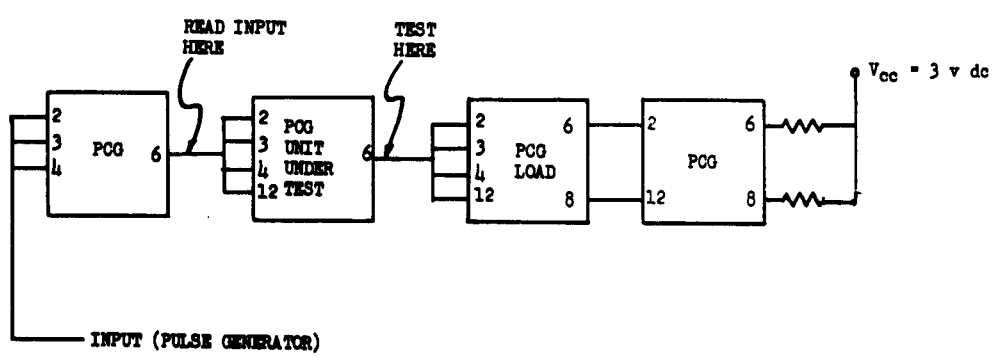



FIGURE 18 - Test Circuit - PCG-101 Dual NAND Gate

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 19)

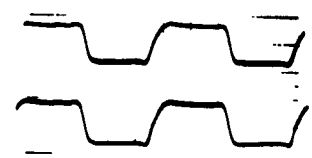
In the following tests, outputs at pins 6 and 8 were compared to see if both circuits in the same can are identical.

Temp = +25° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc

$T_{s6}$ = 0.063 us
$T_{d6}$ = 0.078 us
$T_{r6}$ = 0.039 us
$T_{f6}$ = 0.028 us
$V_{pp6}$ = 0.71 v dc



$T_{s8}$ = 0.057 us
$T_{d8}$ = 0.085 us
$T_{r8}$ = 0.037 us
$T_{f8}$ = 0.030 us
$V_{pp8}$ = 0.74 v dc

Top Trace - pin 6

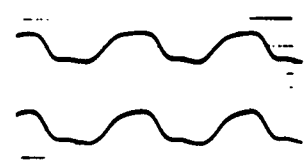
Bottom Trace - pin 8

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s6}$ = 0.034 us
$T_{d6}$ = 0.033 us
$T_{r6}$ = 0.041 us
$T_{f6}$ = 0.040 us
$V_{pp6}$ = 0.66 v dc



$T_{s8}$ = 0.042 us
$T_{d8}$ = 0.038 us
$T_{r8}$ = 0.056 us
$T_{f8}$ = 0.040 us
$V_{pp8}$ = 0.60 v dc

Top Trace - pin 6

Bottom Trace - pin 8

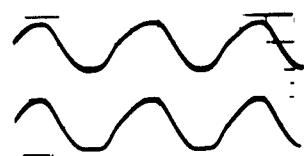
PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 19)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s6}$ = 0.050 us
$T_{d6}$ = 0.053 us
$T_{r6}$ = 0.042 us
$T_{f6}$ = 0.050 us
$V_{pp6}$ = 0.96 v dc



$T_{s8}$ = 0.050 us
$T_{d8}$ = 0.055 us
$T_{r8}$ = 0.031 us
$T_{f8}$ = 0.043 us
$V_{pp8}$ = 0.90 v dc

Top Trace - pin 6

Bottom Trace - pin 8

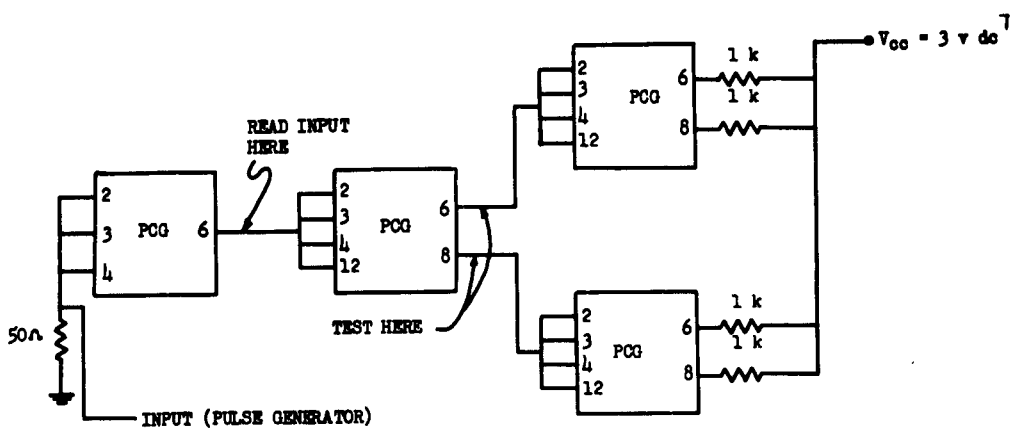
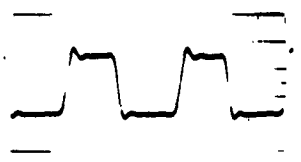



FIGURE 19 - Test Circuit - PCG-101 Dual NAND Gate

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 20)

In each of the following tests, an Intercontinental pulse generator was used for the clock. Outputs of the pulse generator are as follows:



F = 5.0 mc

$T_r$ = 0.011 us

$T_f$ = 0.011 us

$V_{pp}$ = 1.0 v dc

Temp = +25° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc

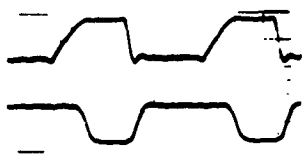
$T_{p6}$ = 0.024 us

$T_{d6}$ = 0.096 us

$T_{r6}$ = 0.050 us

$T_{f6}$ = 0.042 us

$V_{pp6}$ = 0.69 v dc



Top Trace - input

Bottom Trace - output

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 20)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

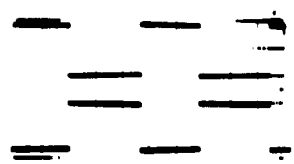
$T_{s6}$ = *

$T_{d6}$ = *

$T_{r6}$ = *

$T_{f6}$ = *

$V_{pp6}$ = *



Top Trace - input

Bottom Trace - output

F = 2.0 mc

$T_{s6}$ = 0.030 us

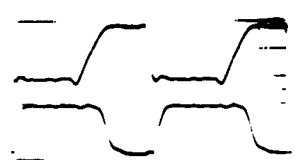
$T_{d6}$ = 0.075 us

$T_{r6}$ = 0.066 us (10% to 90%)

$T_{r6}$ = 0.018 us (10% to 50%)

$T_{f6}$ = 0.032 us

• $V_{pp6}$ = 0.36 v dc



Top Trace - input

Bottom Trace - output

* *too fast to measure at this low frequency*

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 20)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

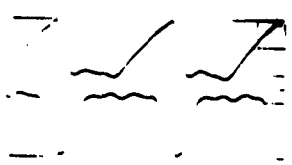
$T_{s6}$ = 0.014 us

$T_{d6}$ = 0.067 us

$T_{r6}$ = 0.027 us

$T_{f6}$ = 0.024 us

$V_{pp6}$ = 0.210 v dc



Top Trace - input

Bottom Trace - output

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 100 cycles

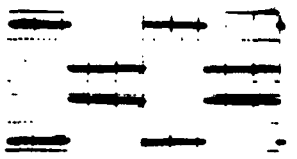
$T_{s6}$ = *

$T_{d6}$ = *

$T_{r6}$ = *

$T_{f6}$ = *

$V_{pp6}$ = *



Top Trace - input

Bottom Trace - output

* *too fast to measure at this low frequency*

## PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 20)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 2.0 mc

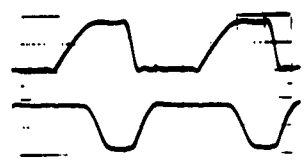
$T_{s6}$ = 0.024 us

$T_{d6}$ = 0.119 us

$T_{r6}$ = 0.055 us

$T_{f6}$ = 0.052 us

$V_{pp6}$ = 0.82 v dc



Top Trace - input

Bottom Trace - output

F = 4.34 mc*

$T_{s6}$ = 0.008 us

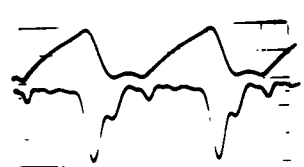
$T_{d6}$ = 0.102 us

$T_{r6}$ = 0.017 us

$T_{f6}$ = 0.040 us (10% to 90%)

$T_{f6}$ = 0.012 us (10% to 50%)

$V_{pp6}$ = 0.12 v dc



Top Trace - input

Bottom Trace - output

* *Will not operate at 5 mc*

PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 20)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.7 mc*

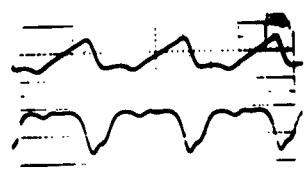
$T_{s6}$ = 0.009 us

$T_{d6}$ = 0.017 us

$T_{r6}$ = 0.018 us

$T_{f6}$ = 0.033 us

$V_{pp6}$ = 0.15 v dc



Top Trace - input

Bottom Trace - output

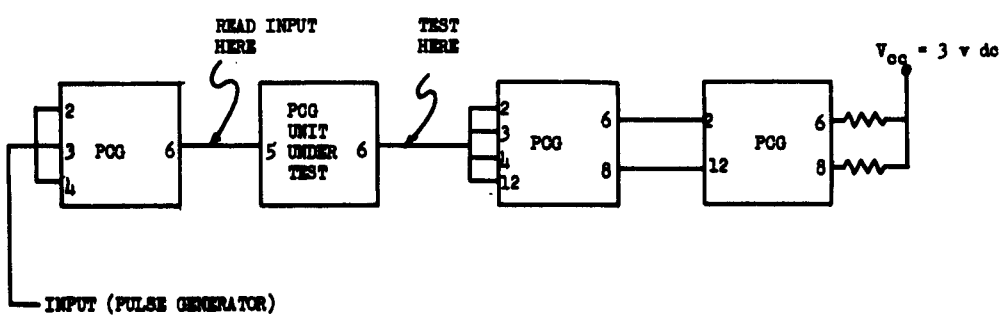



FIGURE 20 - Test Circuit - PCG-101 Dual NAND Gate

* *This is the highest frequency at which this circuit will operate under these conditions.*

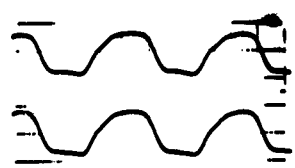
PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 21)

Temp = +25° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s6}$ = 0.020 us
$T_{d6}$ = 0.053 us
$T_{r6}$ = 0.034 us
$T_{f6}$ = 0.040 us
$V_{pp6}$ = 0.71 v dc



$T_{s8}$ = 0.019 us
$T_{d8}$ = 0.052 us
$T_{r8}$ = 0.037 us
$T_{f8}$ = 0.040 us
$V_{pp8}$ = 0.72 v dc

Top Trace - pin 6

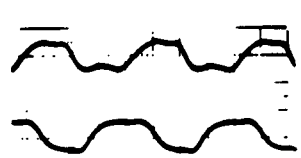
Bottom Trace - pin 8

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s6}$ = 0.028 us
$T_{d6}$ = 0.043 us
$T_{r6}$ = 0.042 us
$T_{f6}$ = 0.039 us
$V_{pp6}$ = 0.52 v dc



$T_{s8}$ = 0.028 us
$T_{d8}$ = 0.042 us
$T_{r8}$ = 0.043 us
$T_{f8}$ = 0.043 us
$V_{pp8}$ = 0.56 v dc

Top Trace - pin 6

Bottom Trace - pin 8

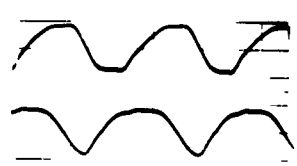
PCG-101 DUAL NAND GATE (Continued)
(See figures 16 and 21)

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCG-101; Load - PCG-101

F = 5.0 mc

$T_{s6}$ = 0.024 us
$T_{d6}$ = 0.069 us
$T_{r6}$ = 0.045 us
$T_{f6}$ = 0.044 us
$V_{pp6}$ = 0.76 v dc



$T_{s8}$ = 0.027 us
$T_{d8}$ = 0.069 us
$T_{r8}$ = 0.048 us
$T_{f8}$ = 0.052 us
$V_{pp8}$ = 0.82 v dc

Top Trace - pin 6

Bottom Trace - pin 8

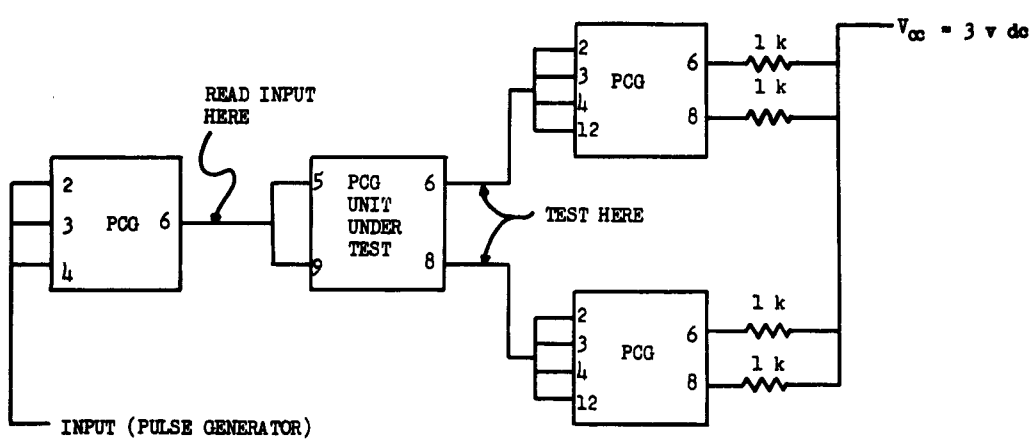



FIGURE 21 - Test Circuit - PCG-101 Dual NAND Gate

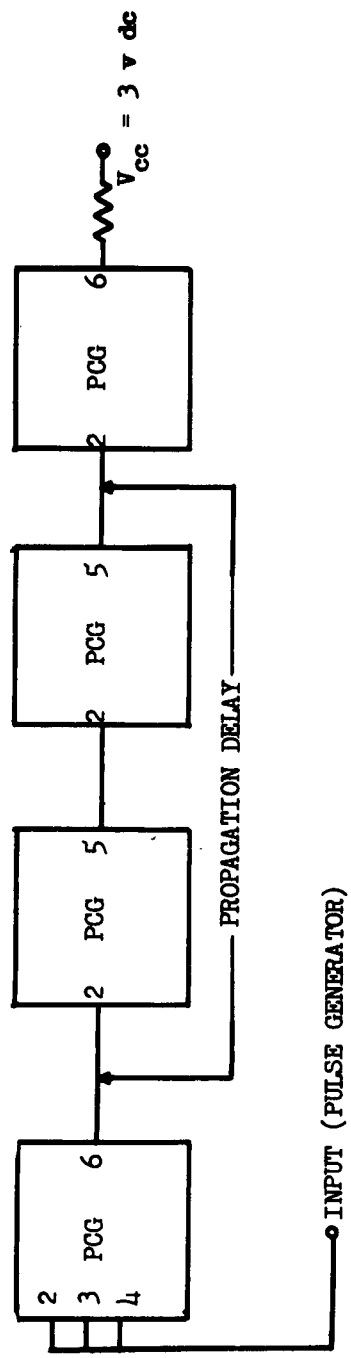



FIGURE 22 - Propagation Delay Diagram - PCG-101 Dual NAND Gate

## PCG-101 DUAL NAND GATE (Continued)
(See figures 16, 23, and 24)

Temp = +25° C; $V_{cc}$ = 3 v dc; N = 4

| Pin 2 | Pin 6 | | | Pin 4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.8 v | A | 0 v | Cutoff | 0.82 v | A |
| 0.6 v | Saturated | 0.12 v | | 0.6 v | Saturated | 0.14 v | |
| 0.6 v | Cutoff | 0.86 v | B | 0.6 v | Cutoff | 0.85 v | B |
| 0 v | Saturated | 0.1 v | | 0 v | Saturated | 0.12 v | |

| Pin 3 | Pin 6 | | | Pin 2,3,4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.82 v | A | 0 v | Cutoff | 0.82 v | A |
| 0.6 v | Saturated | 0.17 v | | 0.65 v | Saturated | 0.14 v | |
| 0.6 v | Cutoff | 0.85 v | B | 0.65 v | Cutoff | 0.85 v | B |
| 0 v | Saturated | 0.12 v | | 0 v | Saturated | 0.12 v | |

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4

| Pin 2 | Pin 6 | | | Pin 4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.69 v | A | 0 v | Cutoff | 0.7 v | A |
| 0.6 v | Saturated | 0.14 v | | 0.57 v | Saturated | 0.14 v | |
| 0.5 v | Cutoff | 0.73 v | B | 0.43 v | Cutoff | 0.71 v | B |
| 0 v | Saturated | 0.15 v | | 0 v | Saturated | 0.13 v | |

PCG-101 DUAL NAND GATE (Continued)
(See figures 16, 23, and 24)

Temp = +125° C; $V_{cc}$ = 3 v dc; N = 4

| Pin 3 | Pin 6 | | | Pin 2,3,4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.68 v | A | 0 v | Cutoff | 0.69 v | A |
| 0.55 v | Saturated | 0.13 v | | 0.57 v | Saturated | 0.13 v | |
| 0.48 v | Cutoff | 0.71 v | B | 0.5 v | Cutoff | 0.72 v | B |
| 0 v | Saturated | 0.13 v | | 0 v | Saturated | 0.13 v | |

Temp = -55° C; $V_{cc}$ = 3 v dc; N = 4

| Pin 2 | Pin 6 | | | Pin 4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.94 v | A | 0 v | Cutoff | 0.94 v | A |
| 0.83 v | Saturated | 0.1 v | | 0.82 v | Saturated | 0.1 v | |
| 0.75 v | Cutoff | 0.95 v | B | 0.82 v | Cutoff | 0.95 v | B |
| 0 v | Saturated | 0.1 v | | 0 v | Saturated | 0.1 v | |

| Pin 3 | Pin 6 | | | Pin 2,3,4 | Pin 6 | | |
|---|---|---|---|---|---|---|---|
| 0 v | Cutoff | 0.95 v | A | 0 v | Cutoff | 0.94 v | A |
| 0.81 v | Saturated | 0.1 v | | 0.82 v | Saturated | 0.1 v | |
| 0.75 v | Cutoff | 0.96 v | B | 0.8 v | Cutoff | 0.96 v | B |
| 0 v | Saturated | 0.1 v | | 0 v | Saturated | 0.1 v | |

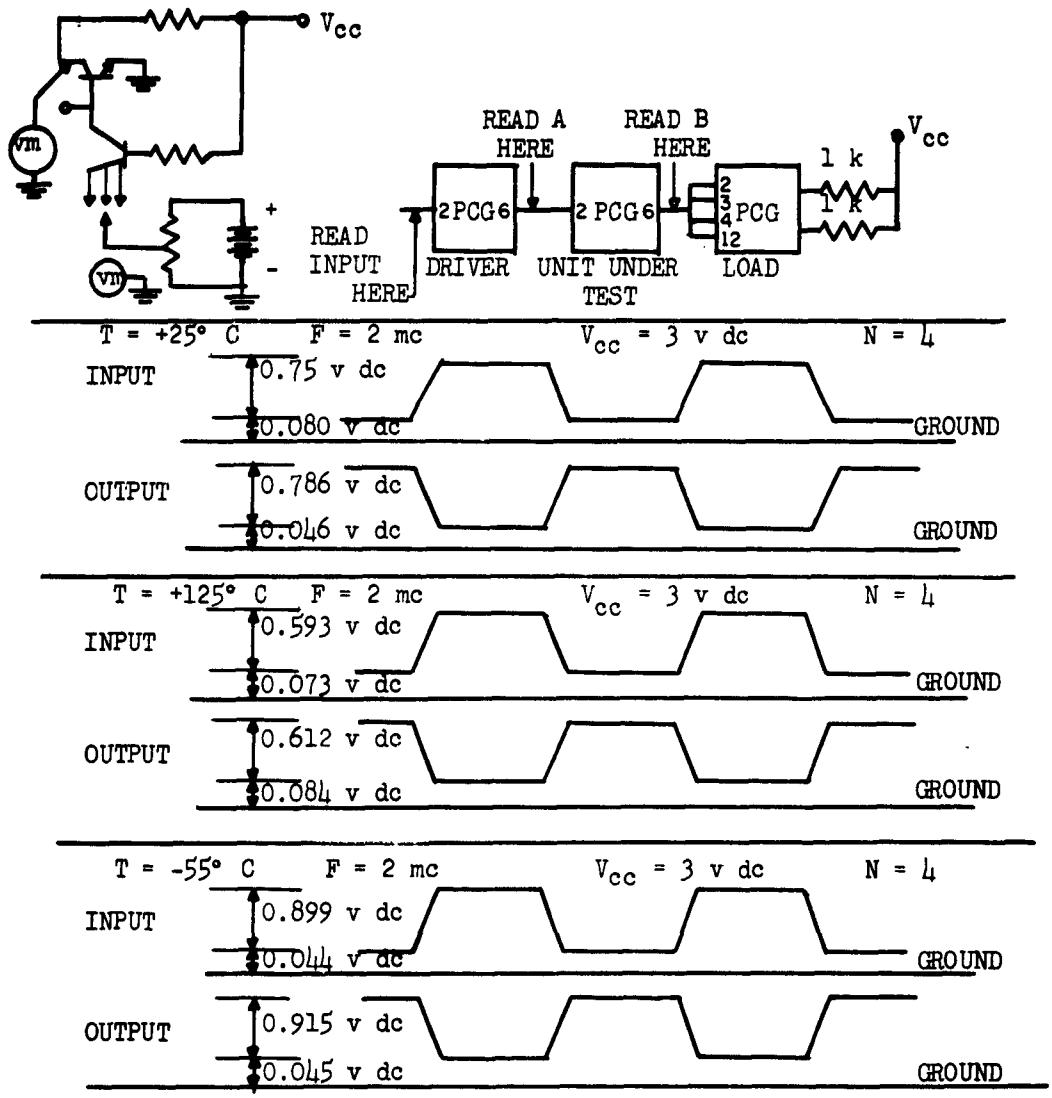



FIGURE 23 - Test Circuit - PCG-101 Dual NAND Gate

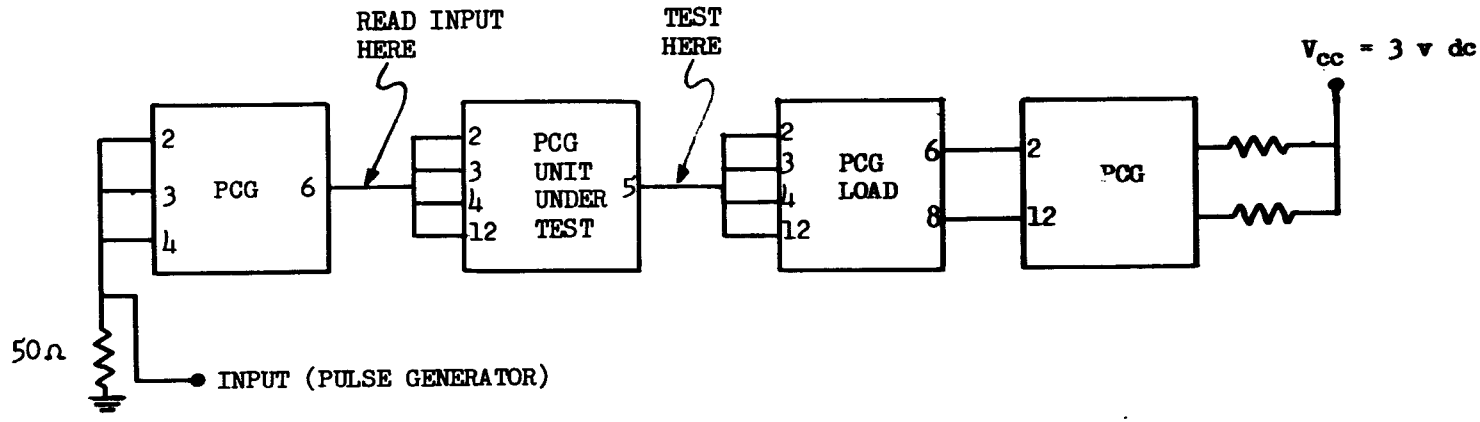
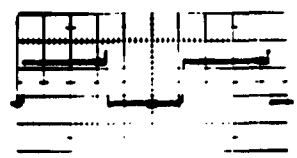



FIGURE 24 - Test Circuit - PCG-101 Dual NAND Gate

PCH-101 HALF-ADDER
(See figure 25)

In each of the following tests, a pulse generator was used for the clock in the PCF-1 flip-flop used to drive the unit under test. The clock pulse characteristics are shown below:



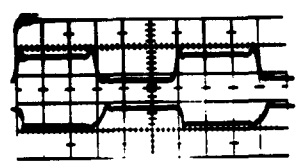
Top Trace -
input = 0.8 $V_{pp}$

Bottom Trace -
output

$T_r$ = 0.01 us

$T_f$ = 0.01 us

Outputs of the PCF-1 flip-flop used to drive the unit under tests are as follows:



Top Trace -
input = 0.47 $V_{pp}$

$T_r$ = 0.032 us

$T_f$ = 0.032 us

Bottom Trace -
output = 0.28 $V_{pp}$

$T_r$ = 0.070 us

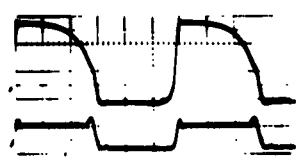
$T_f$ = 0.029 us

PCH-101 HALF-ADDER (Continued)
(See figure 25)

Temp = 25° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 1.0 mc



Bottom Trace -
input = 0.28 $V_{pp}$

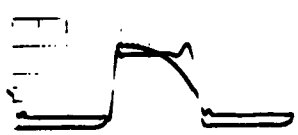
Top Trace -
output = 1.44 $V_{pp}$

$T_r$ (10-90%) = 0.263 us

$T_r$ (10-50%) = 0.055 us

$T_f$ (10-90%) = 0.058 us

$T_f$ (10-50%) = 0.043 us



* Propagation delay = 0.023 us

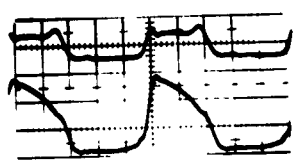
* *Measured between pin 3 ($\bar{B}$) and pin 4 (S).*

PCH-101 HALF-ADDER (Continued)
(See figure 25)

Temp = 25° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 2.0 mc



Top Trace - input = 0.28 $V_{pp}$

Bottom Trace - output = 1.26 $V_{pp}$

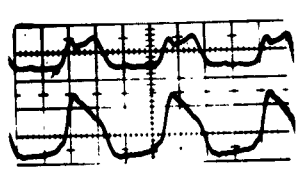
$T_r$ (10-90%) = 0.155 us

$T_r$ (10-50%) = 0.069 us

$T_f$ (10-90%) = 0.050 us

$T_f$ (10-50%) = 0.028 us

F = 3.0 mc



Top Trace - input = 0.28 $V_{pp}$

Bottom Trace - output = 1.10 $V_{pp}$

$T_r$ (10-90%) = 0.118 us

$T_r$ (10-50%) = 0.033 us

$T_f$ (10-90%) = 0.068 us

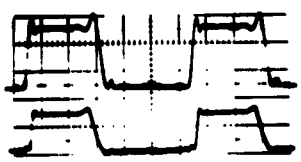
$T_f$ (10-50%) = 0.058 us

PCH-101 HALF-ADDER (Continued)
(See figure 25)

Temp = 125° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 1.0 mc



Top Trace - input = 0.28 $V_{pp}$

Bottom Trace - output = 0.275 $V_{pp}$

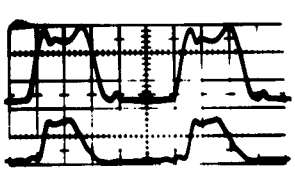
$T_r$ (10-90%) = 0.067 us

$T_r$ (10-50%) = 0.042 us

$T_f$ (10-90%) = 0.024 us

$T_f$ (10-50%) = 0.010 us

F = 2.0 mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 0.285 $V_{pp}$

$T_r$ (10-90%) = 0.066 us

$T_r$ (10-50%) = 0.040 us

$T_f$ (10-90%) = 0.022 us

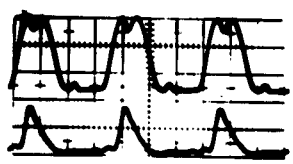
$T_f$ (10-50%) = 0.015 us

PCH-101 HALF-ADDER (Continued)
(See figure 25)

Temp = 125° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 3.0 mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 0.315 $V_{pp}$

$T_r$ (10-90%) = 0.069 us

$T_r$ (10-50%) = 0.043 us

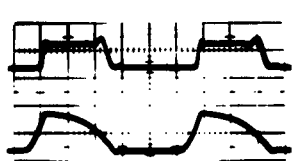
$T_f$ (10-90%) = 0.024 us

$T_f$ (10-50%) = 0.014 us

Temp = -55° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 1.0 mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 1.40 $V_{pp}$

$T_r$ (10-90%) = 0.310 us

$T_r$ (10-50%) = 0.100 us

$T_f$ (10-90%) = 0.100 us

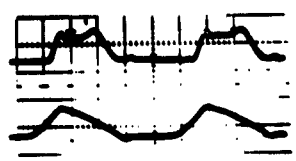
$T_f$ (10-50%) = 0.070 us

PCH-101 HALF-ADDER (Continued)
(See figure 25)

Temp = -55° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCF-101; Load - PCG-101

F = 2.C mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 1.10 $V_{pp}$

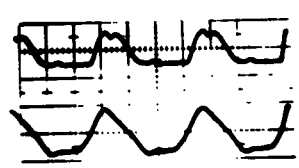
$T_r$ (10-90%) = 0.172 us

$T_r$ (10-50%) = 0.079 us

$T_f$ (10-90%) = 0.081 us

$T_f$ (10-50%) = 0.053 us

F = 3.0 mc



Top Trace - input = 0.47 $V_{pp}$

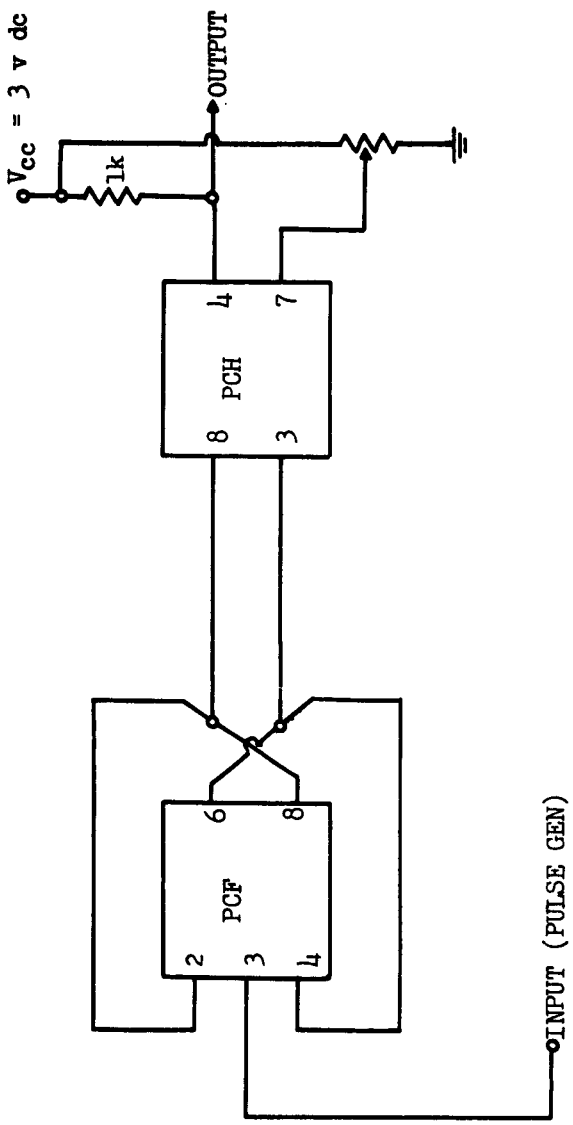
Bottom Trace - output = 0.80 $V_{pp}$

$T_r$ (10-90%) = 0.104 us

$T_r$ (10-50%) = 0.045 us

$T_f$ (10-90%) = 0.068 us

$T_f$ (10-50%) = 0.037 us



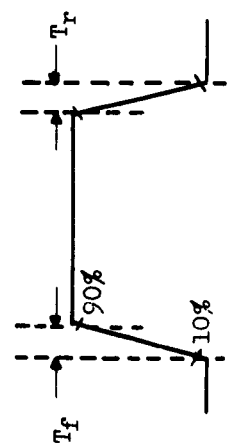
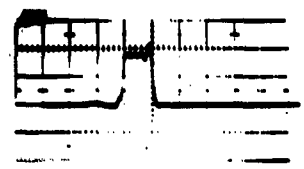




FIGURE 25 - Test Circuit - PCH-101 Half-Adder

## PCR-101 FULL-SHIFT REGISTER
(See figure 26)

A pulse generator was used for the clock in the following tests. The clock pulse characteristics are as follows:



Top Trace - input = 0.94 $V_{pp}$

Bottom Trace - output

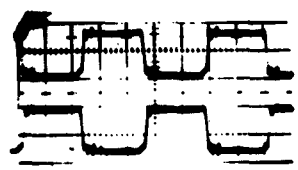
$T_r$ = 0.014 us

$T_f$ = 0.014 us

Temp = +25° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCR-101; Load PCG-101

F = 1.0 mc



Top Trace - input = 0.94 $V_{pp}$

Bottom Trace - output = 0.8 $V_{pp}$

$T_r$ = 0.068 us; $T_f$ = 0.062 us

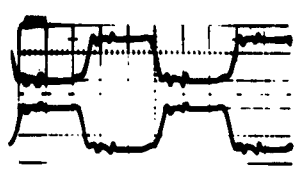
$T_r$ = 0.073 us; $T_f$ = 0.056 us

PCR-101 FULL-SHIFT REGISTER (Continued)
(See figure 26)

Temp = +25° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCR-101; Load - PCG-101

F = 2.0 mc



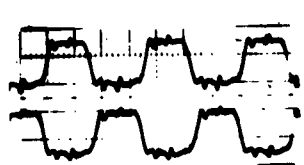
Top Trace - input = 0.94 $V_{pp}$

Bottom Trace - output = 0.80 $V_{pp}$

$T_r$ = 0.068 us; $T_f$ = 0.058 us

$T_r$ = 0.074 us; $T_f$ = 0.052 us

F = 3.0 mc



Top Trace - input = 0.94 $V_{pp}$

Bottom Trace - output = 0.80 $V_{pp}$

$T_r$ = 0.067 us; $T_f$ = 0.061 us

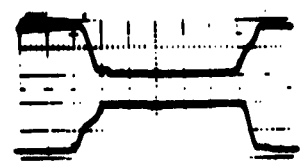
$T_r$ = 0.067 us; $T_f$ = 0.056 us

PCR-101 FULL-SHIFT REGISTER (Continued)
(See figure 26)

Temp = +125° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCR-101; Load PCG-101

F = 1.0 mc



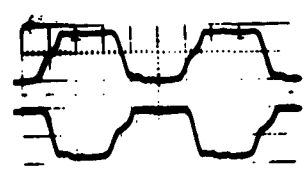
Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 0.63 $V_{pp}$

$T_r$ = 0.032 us; $T_f$ = 0.053 us

$T_r$ = 0.032 us; $T_f$ = 0.041 us

F = 2.0 mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 0.62 $V_{pp}$

$T_r$ = 0.033 us; $T_f$ = 0.047 us

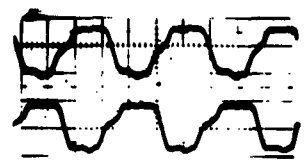
$T_r$ = 0.031 us; $T_f$ = 0.042 us

PCR-101 FULL-SHIFT REGISTER (Continued)
(See figure 26)

Temp = +125° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCR-101; Load - PCG-101

F = 3.0 mc



Top Trace - input = 0.47 $V_{pp}$

Bottom Trace - output = 0.62 $V_{pp}$

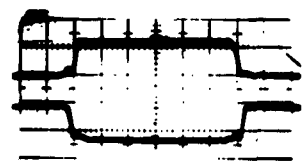
$T_r$ = 0.031 us; $T_f$ = 0.052 us

$T_r$ = 0.033 us; $T_f$ = 0.042 us

Temp = -55° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ = Voltage peak-to-peak

Driver - PCR-101; Load - PCG-101

F = 1.0 mc



Top Trace - input = 0.94 $V_{pp}$

Bottom Trace - output = 0.90 $V_{pp}$

$T_r$ = 0.160 us; $T_f$ = 0.086 us

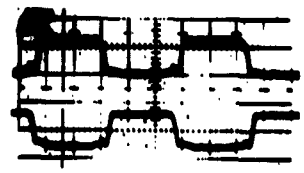
$T_r$ = 0.168 us; $T_f$ = 0.075 us

PCR-101 FULL-SHIFT REGISTER (Continued)
(See figure 26)

Temp = -55° C; $V_{cc}$ = +3.0 v dc; N = 4; $V_{pp}$ - Voltage peak-to-peak

Driver - PCR-101; Load - PCG-101

F = 2.0 mc



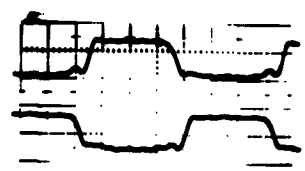
Top Trace -
input = 0.94 $V_{pp}$

Bottom Trace -
output = 0.90 $V_{pp}$

$T_r$ = 0.162 us; $T_f$ = 0.082 us

$T_r$ = 0.170 us; $T_f$ = 0.075 us

F = 3.0 mc

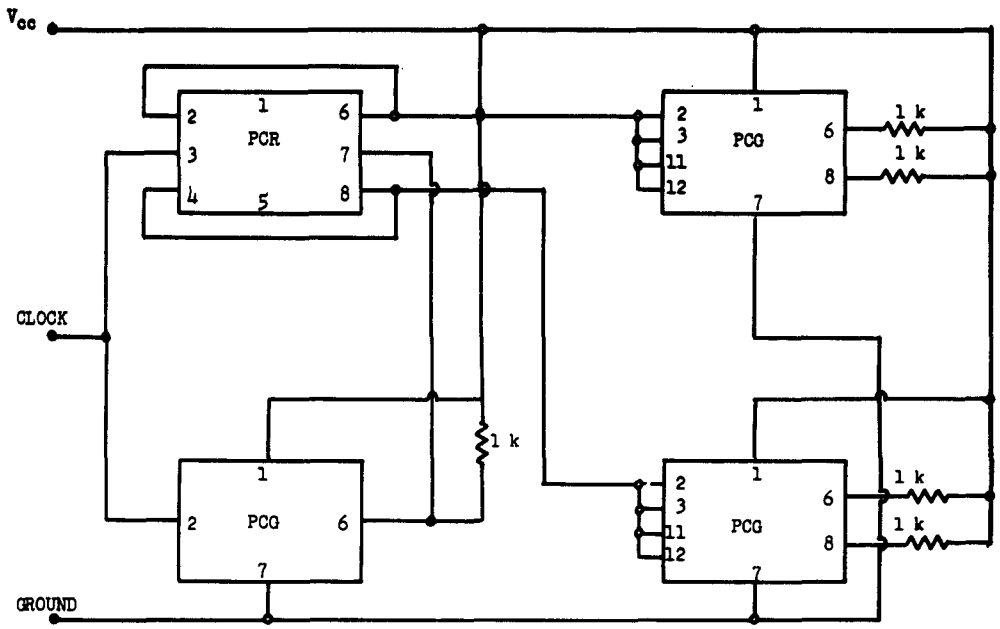


Top Trace -
input = 0.94 $V_{pp}$

Bottom Trace -
output = 0.90 $V_{pp}$

$T_r$ = 0.160 us; $T_f$ = 0.087 us

$T_r$ = 0.167 us; $T_f$ = 0.079 us



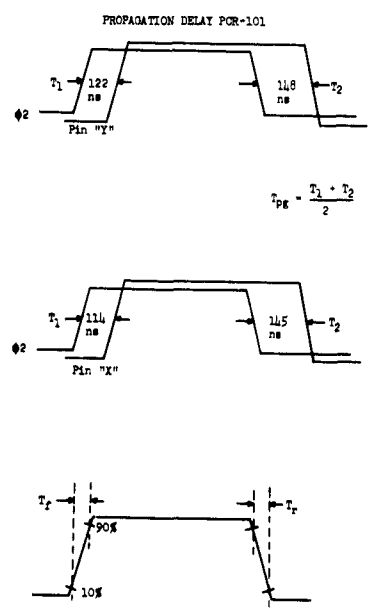




**FIGURE 26 - Test Circuit - PCR-101 Full-Shift Register**

# A P P E N D I X  A

HANDBOOK
Preferred Microelectronic Functions
Navy Aeronautical Electronic Equipment

Reliability Engineering Division
Battelle Memorial Institute
(Contract No. N62269-1717)

# HANDBOOK

# PREFERRED MICROELECTRONIC FUNCTIONS

# NAVY AERONAUTICAL ELECTRONIC EQUIPMENT

## INTRODUCTION

This handbook specifies certain electronic functions and has been written with a view toward over-all functional characteristics. These specifications are intended to apply to microelectronic functional modules, where the circuit need not be specified in terms of individually recognizable component parts. Emphasis is placed on over-all description in terms of the electrical outputs resulting from specific electrical inputs operating on energy supplies under prescribed conditions. The specified performance and tolerances are to be taken as expected performance capabilities. This implies that the system designer may expect this performance over the life of the function. In writing the handbook certain advances in the state of the art of microminiaturization have been assumed. The possibility exists that, for the present, these advances may not be realized and that certain discrete components may be used external to the functional module.

The specification of a circuit, function module, component, or other device can be accomplished by describing adequately, the output, input, and transfer characteristics of the device and their variations. The terms input, output, and transfer are used in the general sense. For example, the input to a device will consist not only of the usual controlling signal with its time and temperature variations, but also noise input, energy-source variations, temperature, and any other factor affecting the circuit. Also, the output characteristics will include the output signal, output impedance relationships, current variations introduced into the energy source, heat dissipation, light, sound, and electromagnetic radiations and their variations. Not all these items will be significant in every case, and in the interest of brevity and practicaity, those found to be insignificant will not be mentioned.

Certain definitions are presented which are intended to be consistent with previous practice as much as possible:*

(1) Delay time. The time required for the module output to start to turn on (current increasing) after input signal is applied. This is measured from the instant when the input signal completes 10 per cent of its total voltage change to the instant when the output voltage completes 10 per cent of its total change.

(2) Storage time. The time required for the module output to start to turn off (current decreasing) after the input turn-off signal is applied. This is measured from the instant when the input signal completes 10 per cent of its total turn-off change (voltage change) to the instant when the output voltage completes 10 per cent of its total turn-off voltage change.

(3) Turn-on time. The time required for the module to complete its voltage change when turning on. This is measured from the instant when the input signal completes 10 per cent of its total voltage change to the instant when the output voltage completes 90 per cent of its total change. Turn-on time includes the delay time and the rise time.

(4) Turn-off time. The time required for the module to complete its voltage change when turning off. This is measured from the instant when the input signal completes 10 per cent of its total turn-off change (voltage change) to the instant when output voltage

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* Notes to the Preferred Circuits Manual, NAVWEPS 16-1-519, p N17-2 to N17-4 and p 215-4

completes 90 per cent of its total turn-off voltage change. Turn-on time includes storage time and fall time.

(5) Rise time. In general, rise time is the time for a transition to go from 10 per cent to 90 per cent of its full amplitude. In particular, rise time is included in turn-on time and is the difference between turn-on time and delay time.

(6) Fall time. Fall time is included in turn-off time and is the difference between turn-off time and storage time.

(7) Linear operation. The condition where the output is directly proportional to the input; more exactly, if $x(t)$ and $y(t)$ are two input signals, and $f(x)$ is the output then the operation is linear if $f(x) + f(y) = f(x + y)$ within specified limits.

(8) Nonlinear operation. The condition where the output of primary concern is outside of the region of linear operation. Examples are diode rectifier, bistable devices, multivibrators of any kind, and sweep generators.

For convenience, certain loading conditions are defined. These are approximations to the actual loads presented by pulse circuit inputs:

(1) "F" Load. The "F" load is a series combination of a 560-pf capacitor and a 3.3 K-ohm resistor.

(2) "G" Load. The "G" load is a parallel combination of a 180-pf capacitor and a 5.62 K-ohm resistor.

(3) "H" Load. The "H" load is a series-parallel combination. A 2200-pf capacitor is in series with a parallel combination of a 200-pf capacitor and a 5.1 K-ohm resistor.

Primarily, a function is represented not by a circuit diagram but by a rectangular block with connection terminals indicated. Signal input terminals are numbered from [1 - 0] to [1 - n], output terminals from [2 - 0] to [2 - n], terminals to be connected to energy sources from [3 - 0] to [3 - n], test points from [4 - 0] to [4 - n], external-component or jumper terminals from [5 - 0] to [5 - n], and the common ground terminal [C]. Terminals are included only as needed. Certain oscillators will need no signal input connection; this signal can be regarded as being furnished internally. No energy-source connections will be shown where the energy is supplied through the input signal, as in detectors; or by way of external components, as in a transformer output audio amplifier. No attempt has been made to indicate all the test points or external connections that may be found necessary. As a practical consideration, test points are needed only to indicate some internal marginal operation. Since the internal circuitry has not been specified, the manufacturer is free to use various means to attain the specified response, and only after the module is designed can the necessity of test points be determined. Thus, no [4 - n] numbered test points appear. D-C energy-source voltages required may vary from those listed for the prototype depending on the module design. The flexibility in voltage selection will permit some design decisions for optimization of power levels, reliability, and system coordination under the constraints imposed by the functional requirements. Energy-source voltages are expected to conform to NAVAIRDEVCEN EL5-13A specification, however.

The probability exists that the functional module as designed for manufacture is not represented by the prototype circuit. The prototype schematic is included only as a guide as to the function desired. For example consider

Figure 1 which is a preferred semiconductor circuit pulse power amplifier. In this conventional preferred circuit, a circuit diagram is shown, the circuit topology is laid out, values of components are indicated, the type of active elements, and primary power-source voltages and currents are shown. The description accompanying the circuit describes the operation and capabilities of the circuit. It should be noted that the circuit operation and, to a certain extent, the limitations of the circuit can be deduced from a study of the circuit diagram. Further, if certain design or operation information should not be given in sufficient detail, the circuit user can breadboard the circuit and make any necessary measurements. Also, reliability improvements can be designed into a circuit by derating components. For example, a 1-watt resistor which operates under marginal dissipation conditions can be replaced by a 2-watt resistor to relieve the operating stress. The analogous situation in a microelectronic function is somewhat more difficult to handle. Figure 2 illustrates the same electronic function specified as a microelectronic module symbol.

Certain conventions have been followed throughout the handbook:

(1) An attempt has been made to differentiate between a-c and d-c voltages on the block diagram. A half-arrow (with a small triangular head on one side of the shaft ( ——▷ ) will indicate that a d-c connection is expected at that point. Arrow with symmetrical head ( ——▷ ) is reserved for a-c or pulse connections, where the d-c level is not significant (within limits).

(2) Input signals are shown at the left side of the functional block, outputs at the right side, connections to energy sources at the

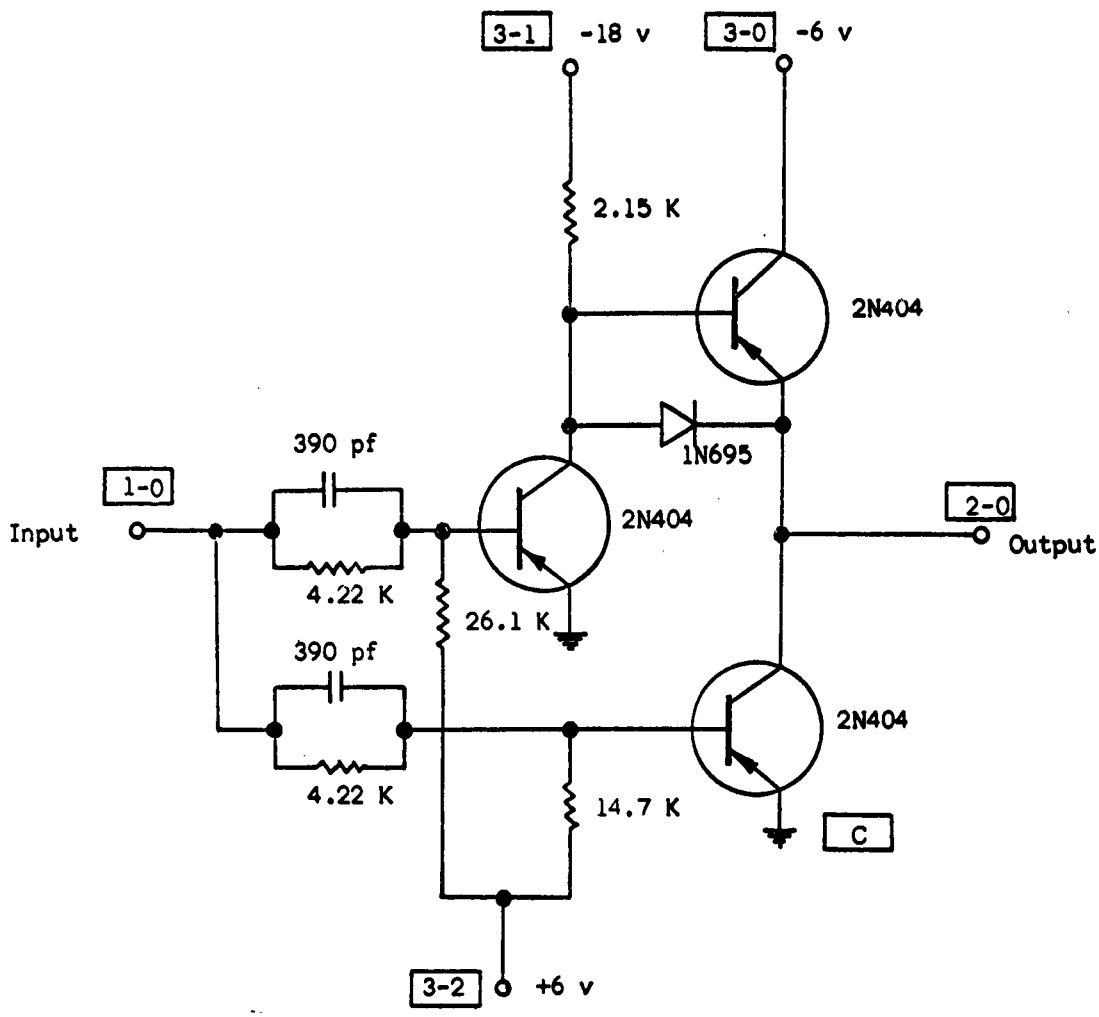



FIGURE 1. PREFERRED SEMICONDUCTOR CIRCUIT NO. 12, PULSE POWER AMPLIFIER

(Pulse Power Amplifier)

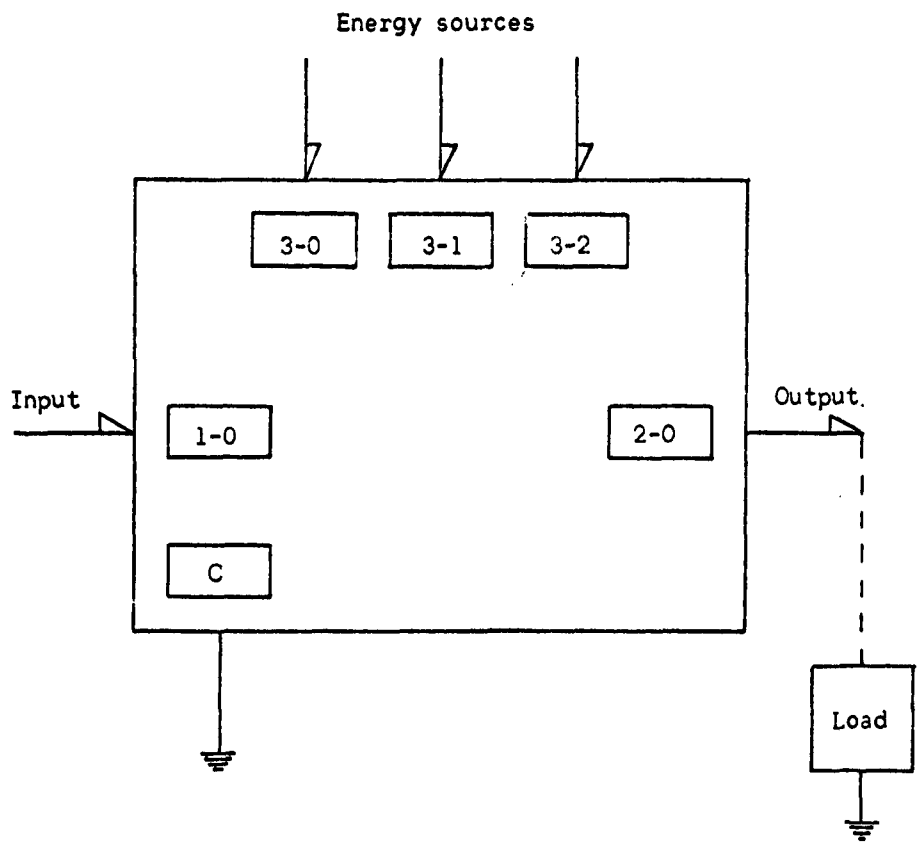



FIGURE 2. MICROELECTRONIC FUNCTION

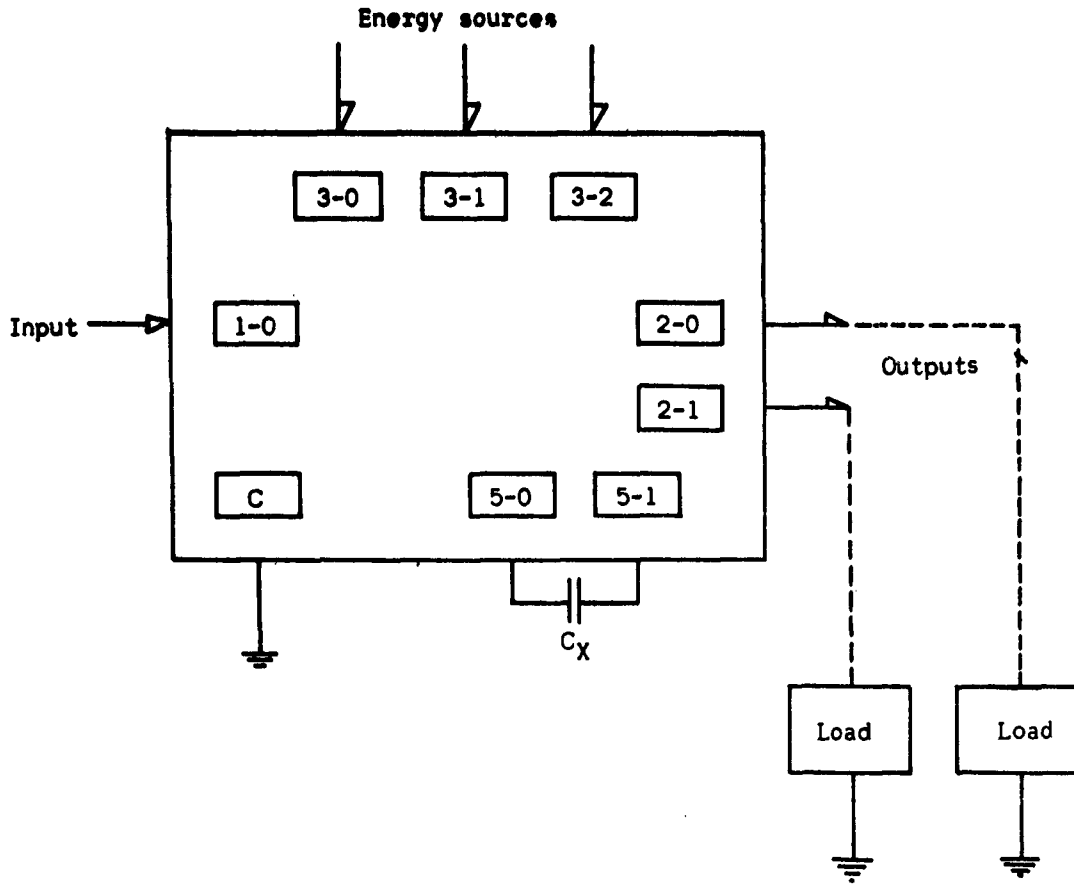
top, and terminals for test points and external components at the bottom.

Graphical information is used where it can be properly substituted for the written word. A special form of graph, the performance profile plot, is used where applicable. The performance profile plot is a graphical representation of function limitations or failure points resulting from varying two parameters at a time, and shows the interaction of parameter variations where such exists. The plot furnishes a picture of the operating region where the function is performed within specifications, and may show valid operating regions outside of the nominal operating area. In general, a number of performance profile plots can be obtained for a function and a number of parameter pairs can be charted on a plot. The shaded boundary on the plot indicates an unacceptable performance or a forbidden area due to limitations of minimum output amplitude, maximum voltage ratings, or other difficulty.

Satisfactory functional performance includes reliability under specified conditions. Reliability of a circuit of standard component parts can be estimated, when data on the reliability of the component-part types are available and the stresses upon them are known. The reliability of a circuit is critically dependent on proper selection of parts and use of a design tolerant to their expected variability. With microelectronic functional modules, the reliability is built in at manufacture, and this leaves the systems designer with limited control. Therefore, circuit design must be optimized, and the maximum stresses upon portions of the functional module which affect the reliability of the module must be minimized by the manufacturer.

# PREFERRED MICROELECTRONIC FUNCTION MA/02 XX

## (Monostable Multivibrator)




**Prototype:** Preferred Semiconductor Circuit No. 10 (NAVWEPS 16-519-2)
Formerly Preferred Circuit No. 213 (NAVWEPS 16-1-519)
(See Section 5)

1. GENERAL

MA/02 XX is a monostable multivibrator designed to perform the delay function in a compatible set of digital logic circuits for use in computer, control, and communications equipment. The limiting repetition rate is 400 kc.

The preferred energy sources are one or more of the following:

3 - 0, +6 volts ± 10 per cent at 0.25 ma max

3 - 1, -6 volts ± 10 per cent at 10 ma max

3 - 2, -18 volts ± 10 per cent at 10 ma max.

In addition, any of the standard voltages in Section 3.5.1 of Specification NAVAIRDEVCEN EL5-13A are acceptable. However, the -6 volt source 3 - 1 is in the nature of a reference and changing it will affect both the output amplitude and timing.

## 2. APPLICATION

MA/02 XX is a monostable multivibrator which can provide a time delay of 2 microseconds to 100 milliseconds depending on the external capacitance, $C_X$, added between terminals [5 - 0] and [5 - 1]. The effect of external capacitance on the time delay is shown in Figure 1.

MA/02 XX can be used as a pulse generator to produce pulses with a width determined by $C_X$. It can also be used as a driver provided that loading limits are not exceeded.

Normally, the input is at ground potential. Under this condition, output [2 - 0] is clamped to the potential of energy source [3 - 1], and [2 - 1] is at ground level. When a negative input pulse is received, the output levels are reversed for the length of the time delay (neglecting recovery time). Thus, [2 - 0] becomes ground potential and [2 - 1] becomes the potential of energy source [3 - 1]. After the time delay, the outputs return to their normal state.

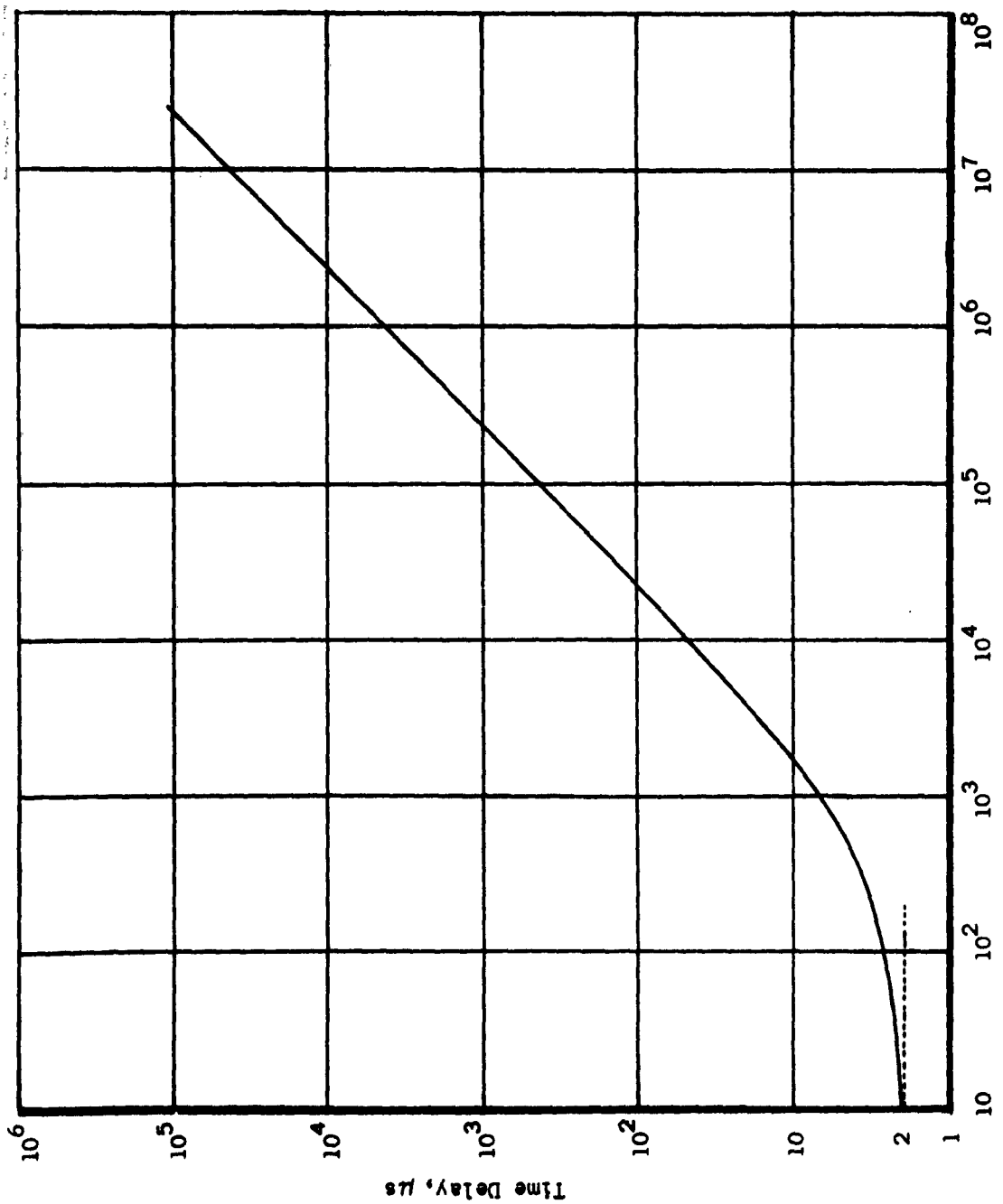



FIGURE 1. TIME DELAY VERSUS EXTERNAL CAPACITANCE

## 3. PERFORMANCE

Normal operating limits are given in Table 1. The actual performance of MA/02 XX is shown in Figures 5 and 6.

The area of reliable triggering of MA/02 XX is shown in Figure 2. The effects of loading are shown in Figures 3 through 6. As indicated in Table 1, 2 - 0 is not normally used with an R.C. load.

The turn-on times shown in Figures 3 and 4 are the times required for the respective outputs to reach 90 per cent of full amplitude once the input signal has reached 10 per cent of its full amplitude. Recovery time is the time required after the time delay is completed until MA/02 XX is ready to receive another input impulse. This time is measured from the time the trailing edge of the 2 - 1 waveform has returned 10 per cent towards its normal amplitude to the time that the trailing edge of the 2 - 0 waveform has returned 90 per cent towards its normal amplitude. Under normal operating conditions, the recovery time is approximately 25 per cent of total time delay.

Internal heat dissipation is limited to 130 milliwatts. The module must be operated at ambient temperature between -55 C and +125 C.

TABLE 1. BASIC FUNCTION PERFORMANCE RANGES

| Parameter | Minimum | Design Center | Ninety-Fifth Percentile | Maximum |
|---|---|---|---|---|
| Input level; negative[a] | -5.4 v | -6.0 v | | -6.6 v |
| Input level; ground | -0.5 v | -0.15 v | | + 12 v[b] |
| Input pulse rise time | -- | -- | | 0.4 μs |
| Input pulse width at 50 per cent amplitude | 0.5 μs | -- | | -- |
| Input impedance[c] | -- | 1 "F" load | | -- |
| Energy source 3-1 noise level | -- | -- | | 1.7 v |
| Noise current to energy source 3-2 [d] | -- | 0.05 ma | 0.01 ma | 0.15 ma |
| Output voltage | -5.6 v | -6.2 v | | -6.8 v |
| Output capability: | | | | |
| 2-0 R.C. load | not used | -- | | -- |
| 2-1 R.C. load | -- | -- | | 2 "F" or "G"[c] |
| 2-0 Direct-current load | -- | -- | | 1.7 KΩ |
| 2-1 Direct-current load | -- | -- | | 2.3 KΩ |

(a) See Figure 2.

(b) The +12 v specification is the maximum voltage limit for the active element in the prototype circuit.

(c) Definition of loads:

"F" - 3300 Ω in series with 560 pf
"G" - 5620 Ω in parallel with 180 pf

More than one of either load indicates parallel combination.
For "F" and "G" load tolerances, see introduction to this manual.

(d) Noise current determined by measuring voltage across 100 Ω in series with 3 - 2 and using worst-case parameters with respect to noise generation.

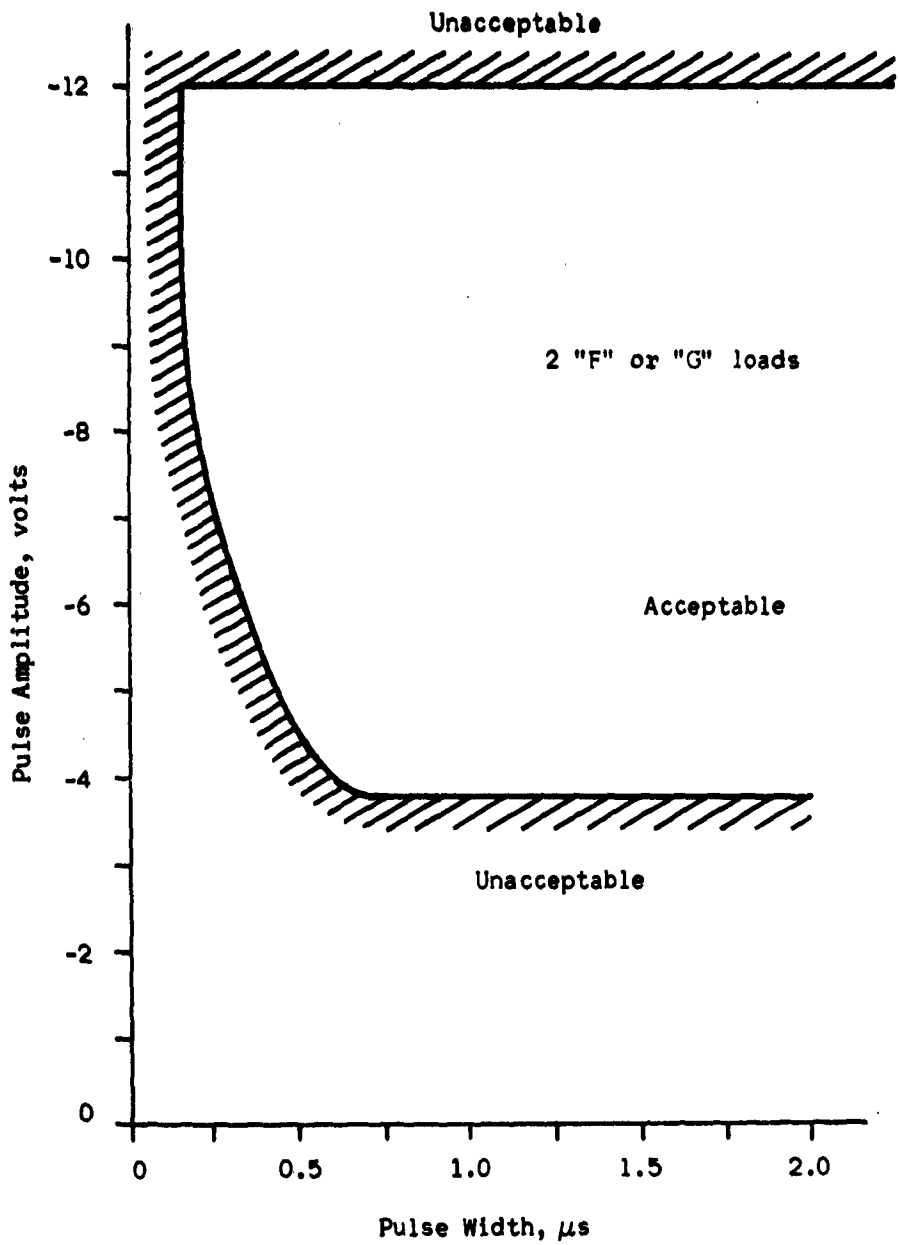



FIGURE 2. TRIGGER REQUIREMENTS

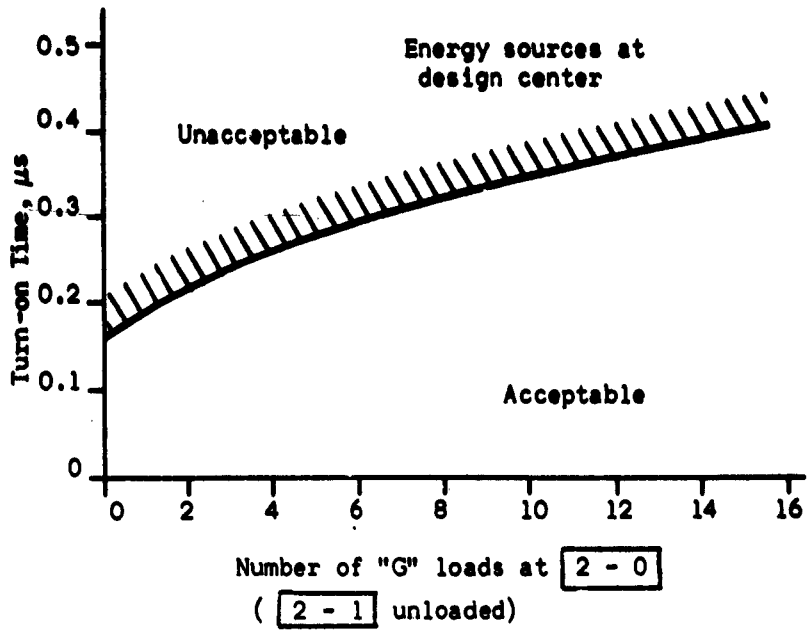



FIGURE 3. LOADING EFFECT ON 2 - 0 TURN-ON TIME

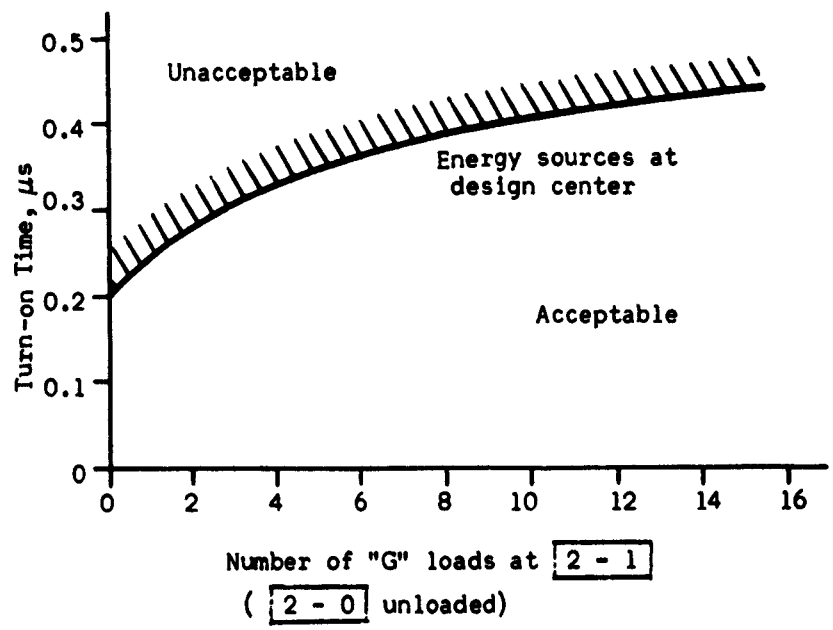



FIGURE 4. LOADING EFFECT ON 2 - 1 TURN-ON TIME

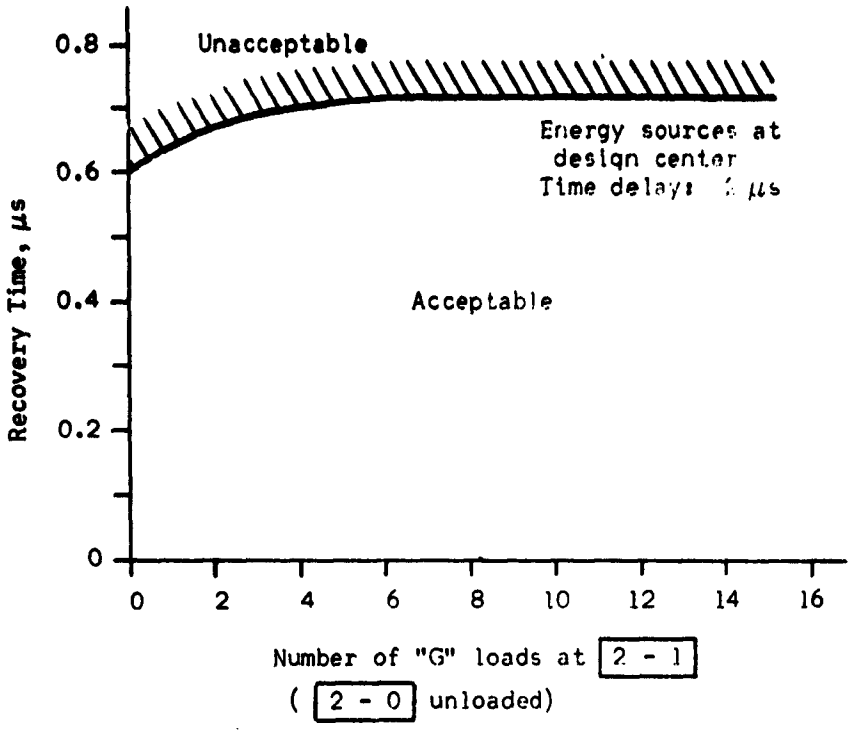



FIGURE 5. EFFECT OF LOADING 2 - 1 ON RECOVERY TIME

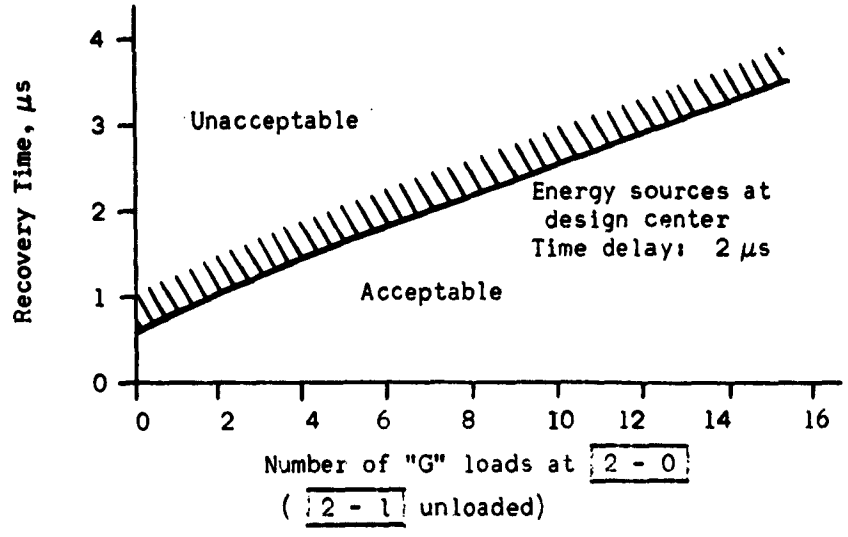



FIGURE 6. EFFECT OF LOADING 2 - 0 ON RECOVERY TIME

## 4. DESIGN CONSIDERATIONS

In the prototype circuit, voltages of +6, -6, and -18 volts are required for operation of the monostable multivibrator. The -18-volt supply is made by connecting the positive side of a 12-volt floating source to the negative side of the -6-volt supply. This arrangement prevents flow of current in the reverse direction through the -6-volt supply. Such reverse current can occur, for example, when Transistor Q1 is cut off and the -18-volt potential is supplied from a separate source. Here, positive current will flow from ground, up through the -6-volt supply, then through CR1 and R1 to the negative terminal of the -18-volt supply and back to ground. If, however, the -18-volt potential is derived from a floating 12-volt supply which is connected in series with the -6-volt supply, the current will flow from the positive side of the 12-volt supply, through CR2 and R1 to the negative terminal of the 12-volt supply. Thus, no current (neglecting $I_{CBO}$) will flow through the -6-volt supply.

The floating source is not considered satisfactory for module application. It is desirable to eliminate this method. However, the effects of using separate sources must be considered by the module manufacturer.

In the prototype circuit, the total capacitance ($C_1$) appearing between terminals [5 - 0] and [5 - 1] controls the time delay in the manner given by the following formula:

$$C_1(\text{pf}) = \frac{\text{Time delay } (\mu\text{s})}{3.9 \times 10^{-3}}$$

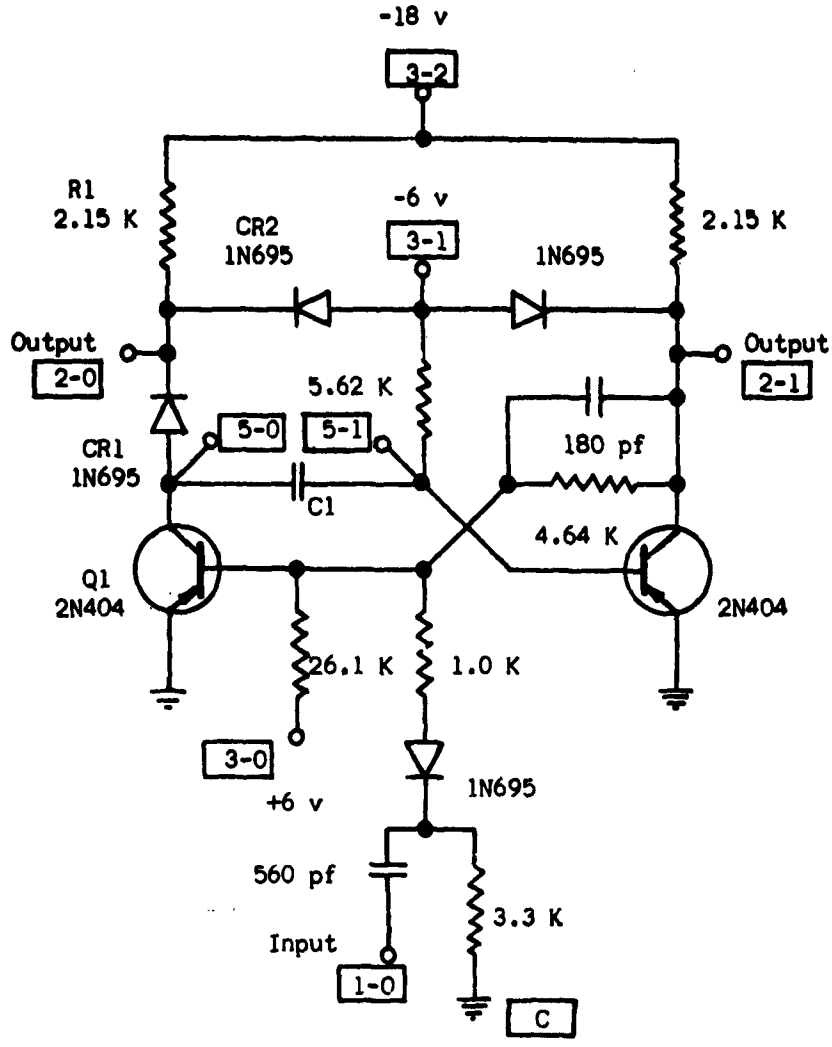
Provision has been made to include a capacitive effect of 500 pf internal to the function module. Thus, the total capacitive effect between the terminals [5 - 0] and [5 - 1] of the function module is 500 pf plus the external capacitance,

$C_X$. The relationship between $C_X$ and time delay is shown in Figure 1. The tolerance in time delay is ±0.1 microsecond. It is expected that the MA/02 XX functional modules will ultimately be specified for a series of fixed time delays covering the present time-delay range. This step should be taken to minimize the need for external connections.

## 5. PROTOTYPE CIRCUIT

PREFERRED SEMICONDUCTOR CIRCUIT NO. 10

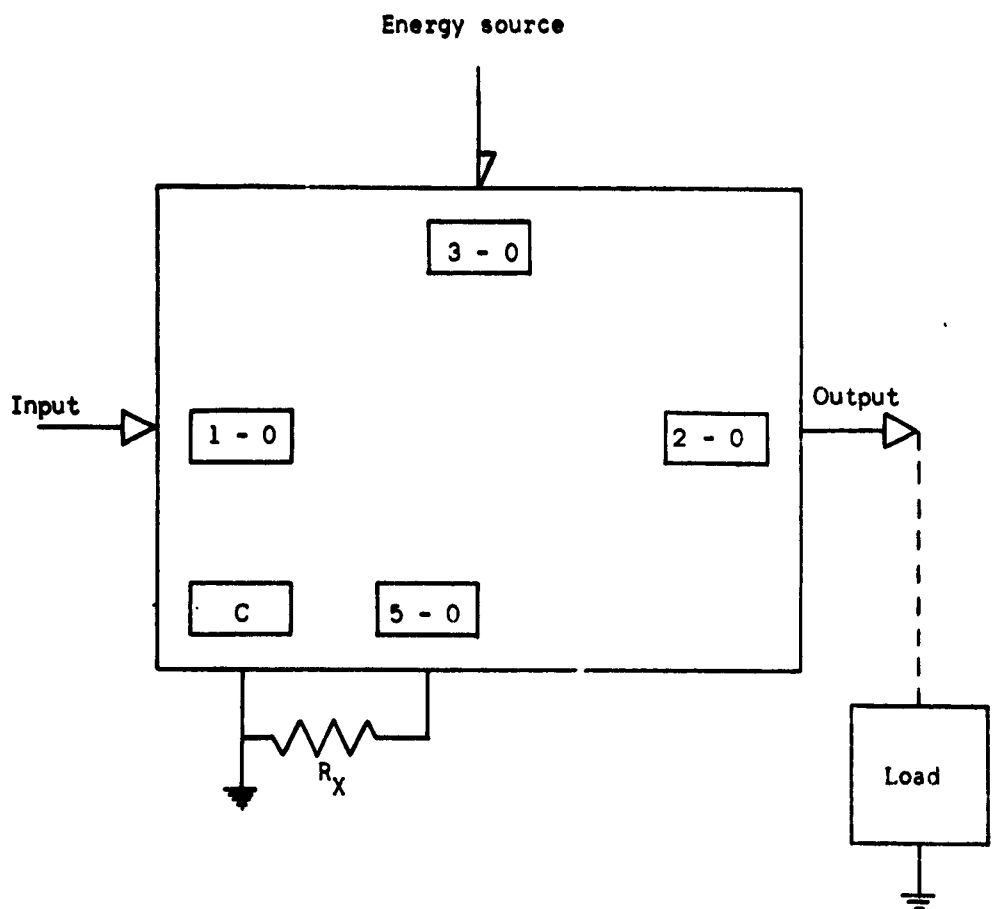
(Monostable Multivibrator)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

PREFERRED MICROELECTRONIC FUNCTION MA/03 XX

(Audio Preamplifier)




Prototype: Preferred Semiconductor Circuit No. 23 (NAVWEPS 16-1-519-?)
(See Section 5)

## 1. GENERAL

MA/03 XX is a preamplifier designed to function at the audio frequency range. It is to be used in communications or other equipment operating in the audio range to amplify audio signals to the level necessary to drive another stage.

The preferred energy source is:

3 - 0, +25 volts ± 10 per cent at 6 ma max.

In addition, any of the standard voltages in Section 3.5.1 of Specification NAVAIRDEVCEN EL5-13A are acceptable.

## 2. APPLICATION

MA/03 XX is an audio preamplifier which provides a voltage gain of 50 to 250 depending on the external resistance, $R_X$, connected between terminals [5 - 0] and [C]. The effect of $R_X$ on the gain with a 1000-ohm load resistance is shown in Figure 9. The frequency response is stable within ±1 db from 10 cps to 30,000 cps, and the operating temperature range is -55 C to +125 C.

MA/03 XX was designed primarily to drive MA/29 XXX (PSC24), which is an audio driver.

## 3. PERFORMANCE

TABLE 1. BASIC FUNCTION PERFORMANCE RANGES

| Parameter | Minimum | Fifth Percentile | Design Center | Ninety-fifth Percentile | Maximum |
|---|---|---|---|---|---|
| Output signal voltage to 1000-ohm load | | | | | 1 vrms |
| Input resistance, $R_X$ = 53 ohms | 11,000 ohms | 16,000 ohms | 26,000 ohms | | |
| Gain, $R_X$ = 53 ohms | 110 | 125 | 150 | | |
| Distortion, $R_X$ = 53 ohms | | | 0.5% | 0.6% | 0.7% |
| Load resistance | 400 ohms | | 1,000 ohms | | |

The nominal gain characteristics for the preamplifier are shown in Figures 1 and 2.

The circuit-performance profiles are presented in Figures 3 through 8. The region labeled acceptable is the minimum acceptable operating region over which the preamplifier must be operable with respect to the two variables indicated with gain and distortion within the limits specified (see Table 1), and the remaining external variables held at their nominal values. Figure 3 presents the performance profile for supply voltage [3 - 0] versus frequency; Figure 4 is the profile of the input voltage [1 - 0] versus frequency; Figure 5 presents the profile of the load resistance versus frequency; Figure 6 is the performance profile of the supply voltage [3 - 0] versus load resistance; Figure 7 presents

the profile of the input voltage [1 - 0] versus load resistance; and Figure 8 is the performance profile of the supply voltage [3 - 0] versus input signal [1 - 0].

The preamplifier's nominal gain performance with respect to temperature is given in Table 2.

TABLE 2. TEMPERATURE EFFECTS ON GAIN

| Temperature | -55 C | 25 C | 125 C |
|---|---|---|---|
| Gain | 80 | 150 | 150 |

The distortion should not vary greater than ±3 per cent from the +25 C value over in temperature range from 125 C to -55 C.

The internal power dissipation of the circuit is limited to 75 milliwatts.

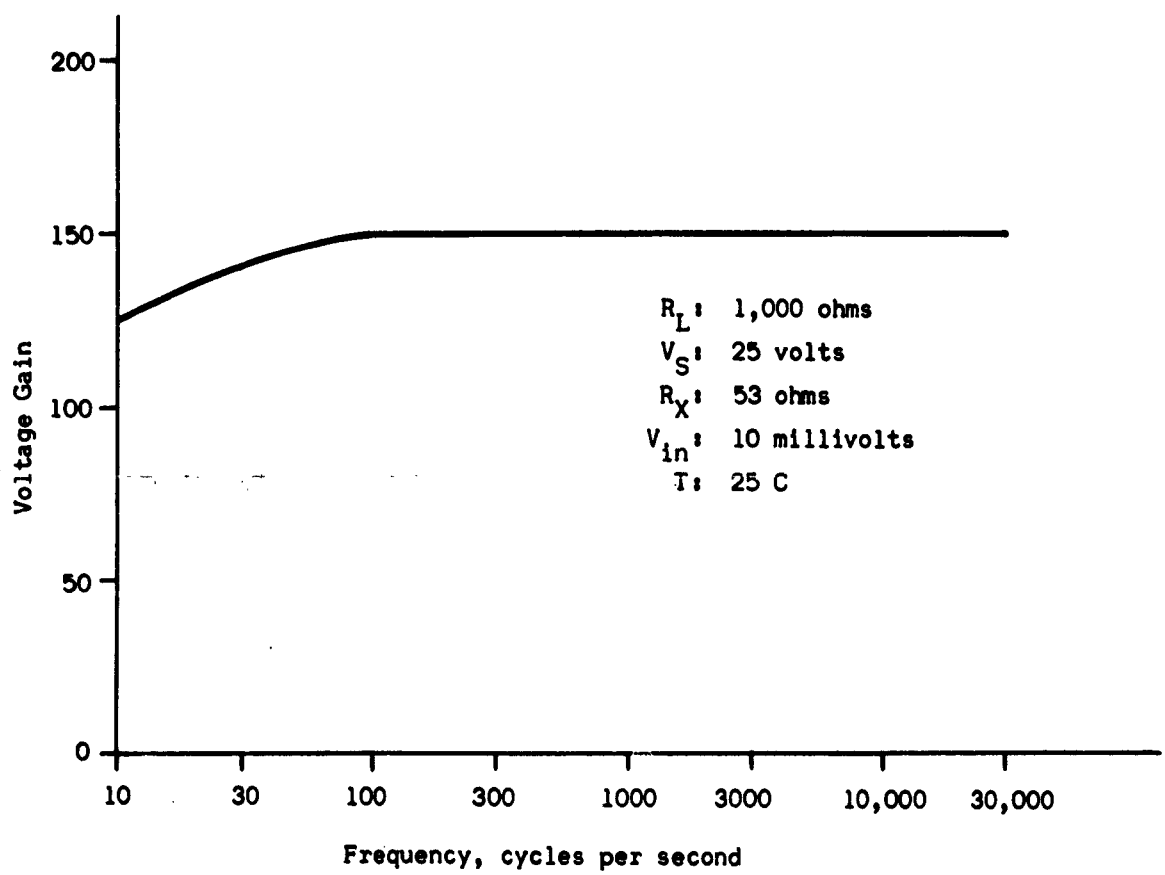



FIGURE 1. NOMINAL FREQUENCY RESPONSE

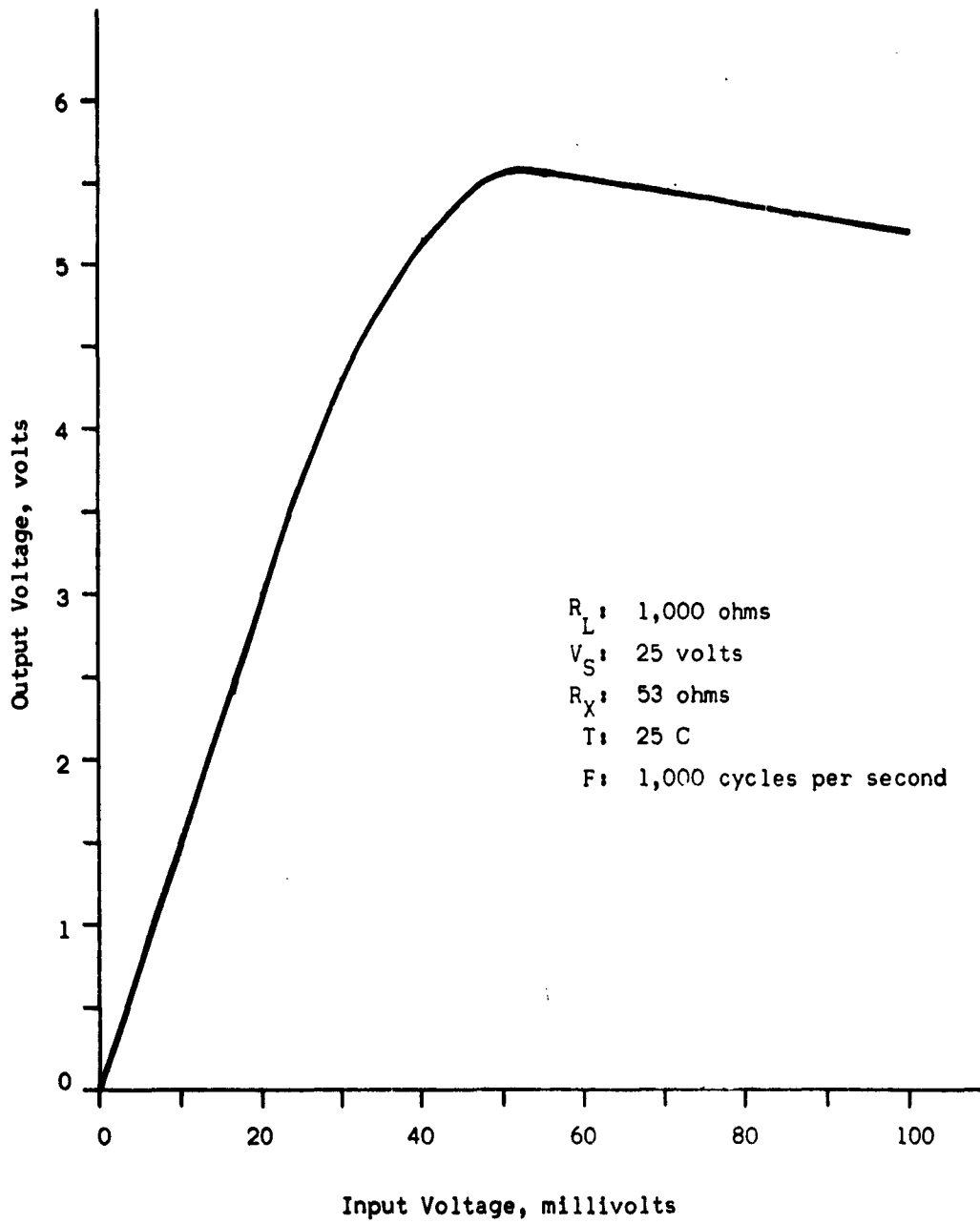



FIGURE 2. NOMINAL GAIN CHARACTERISTICS

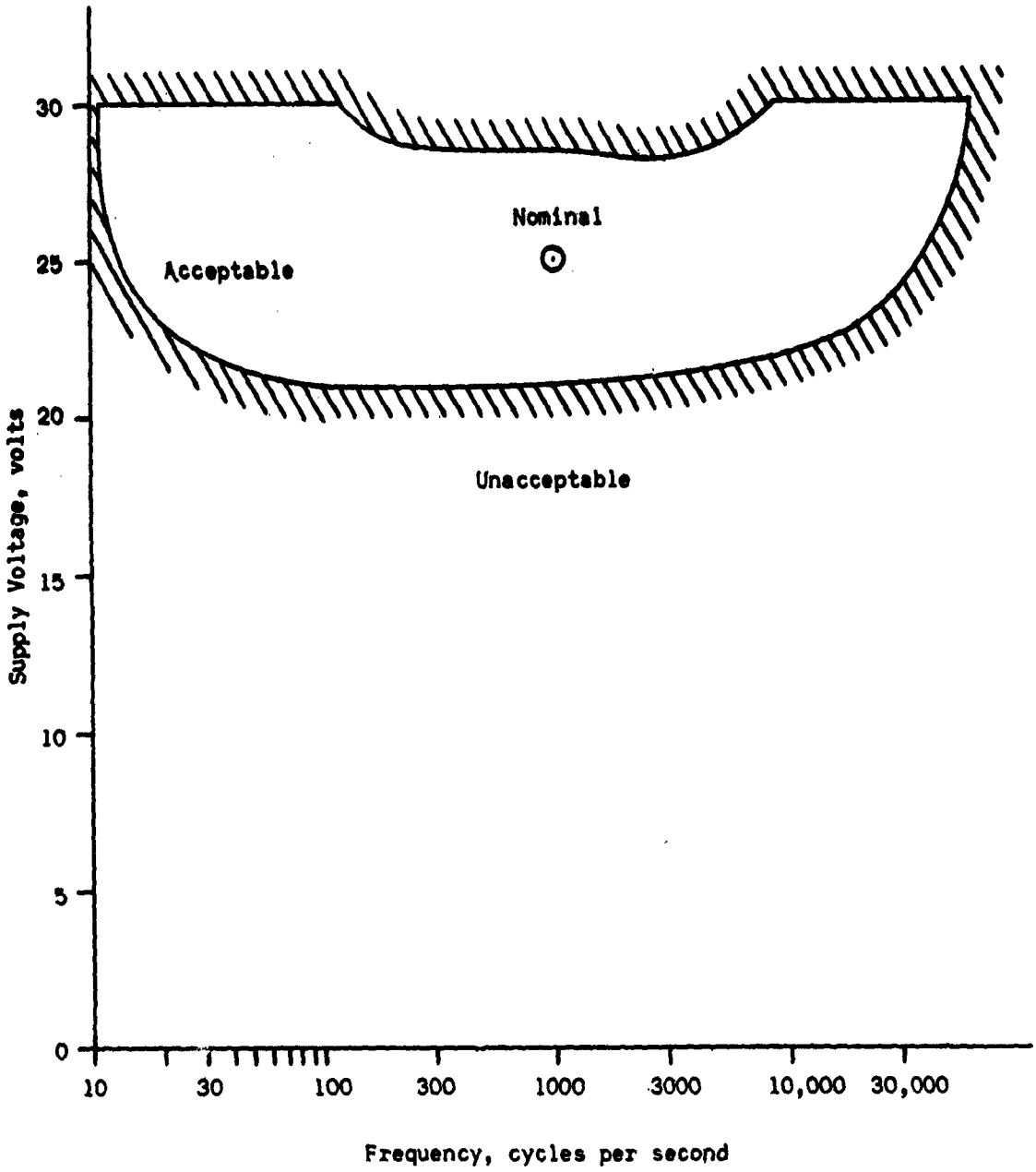



FIGURE 3. PERFORMANCE PROFILE FOR SUPPLY VOLTAGE AND FREQUENCY

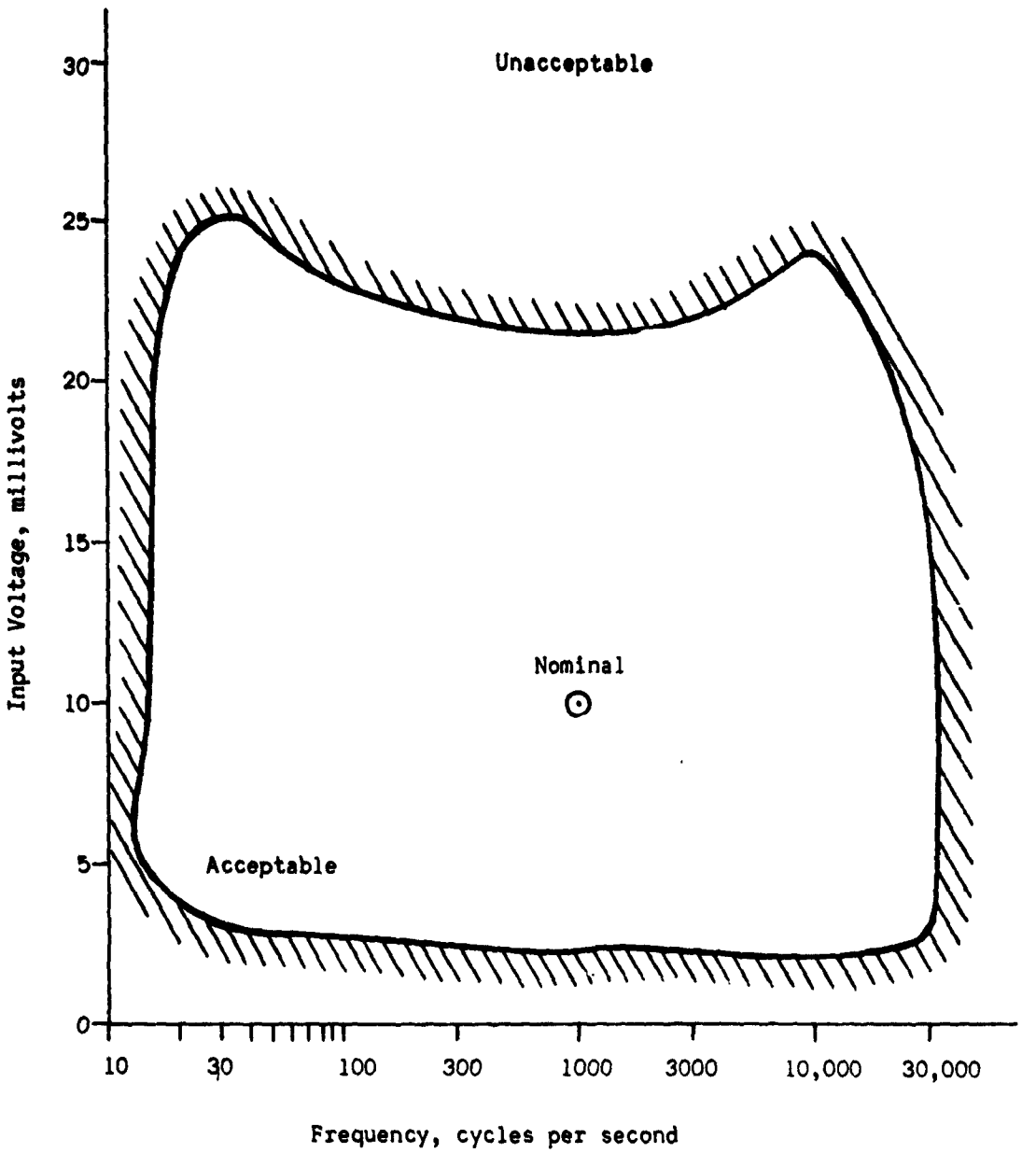



FIGURE 4. PERFORMANCE PROFILE FOR INPUT VOLTAGE AND FREQUENCY

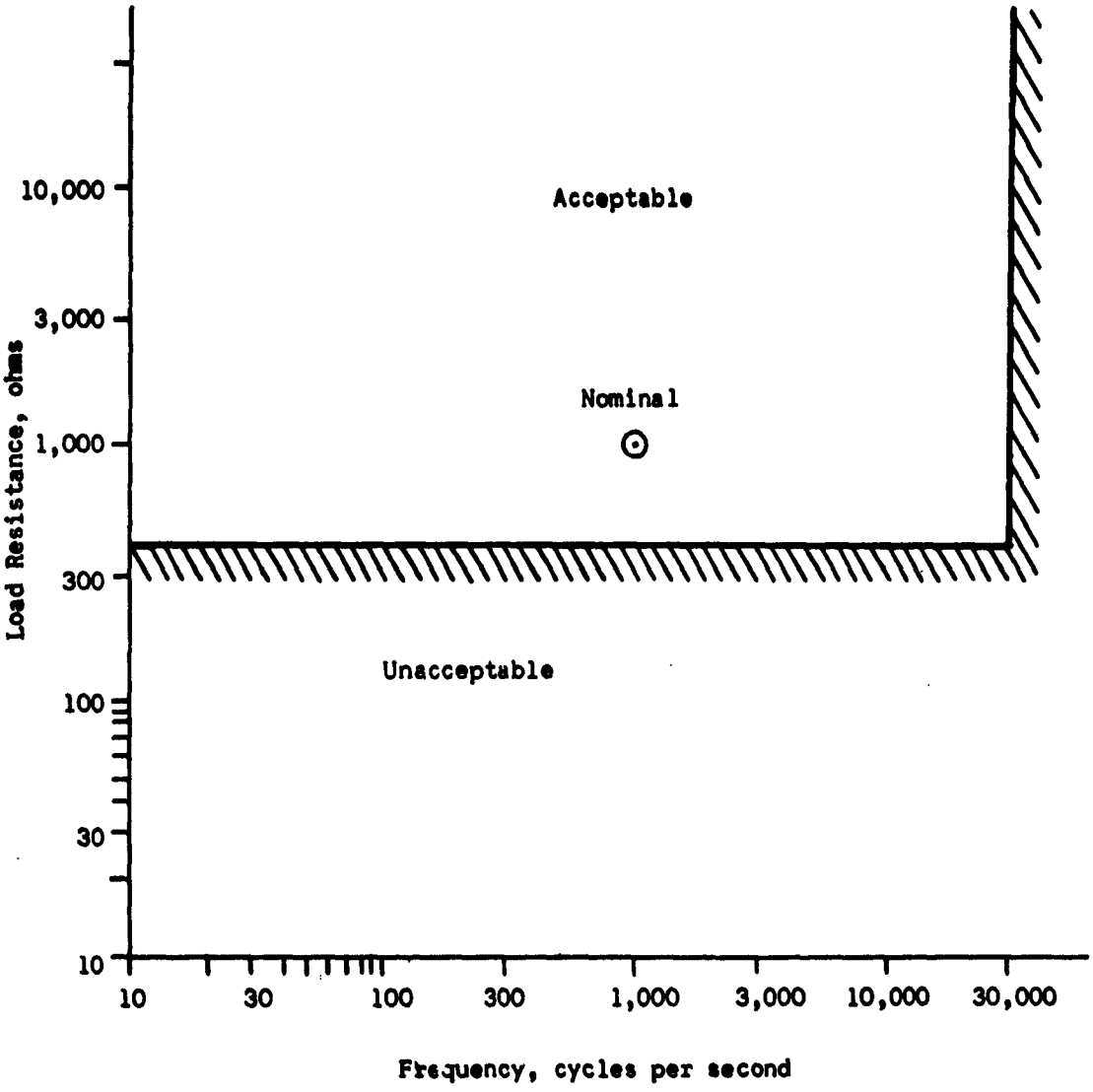



FIGURE 5. PERFORMANCE PROFILE FOR LOAD RESISTANCE AND FREQUENCY

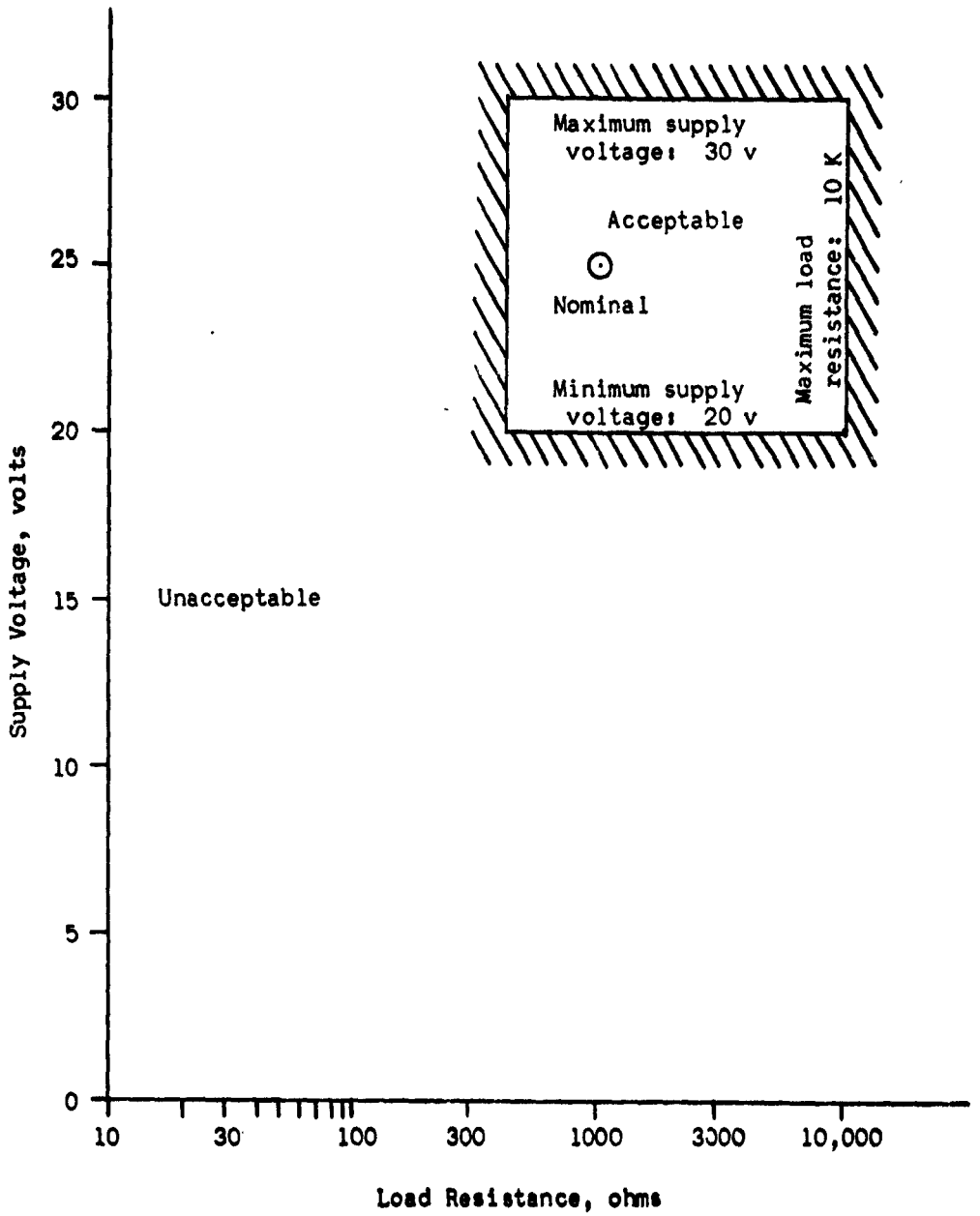



FIGURE 6. PERFORMANCE PROFILE FOR SUPPLY VOLTAGE AND LOAD RESISTANCE

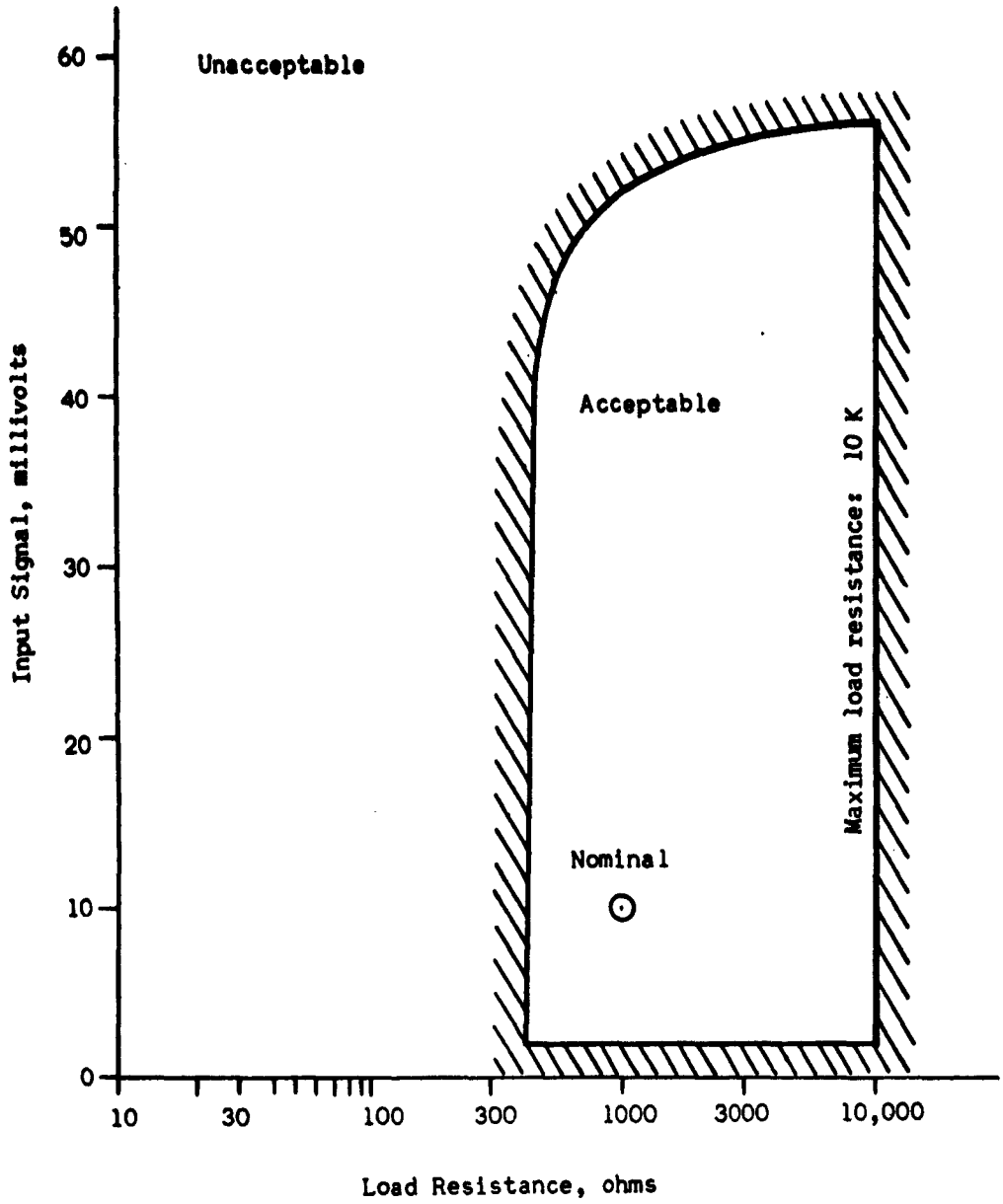



FIGURE 7. PERFORMANCE PROFILE FOR INPUT SIGNAL AND LOAD RESISTANCE

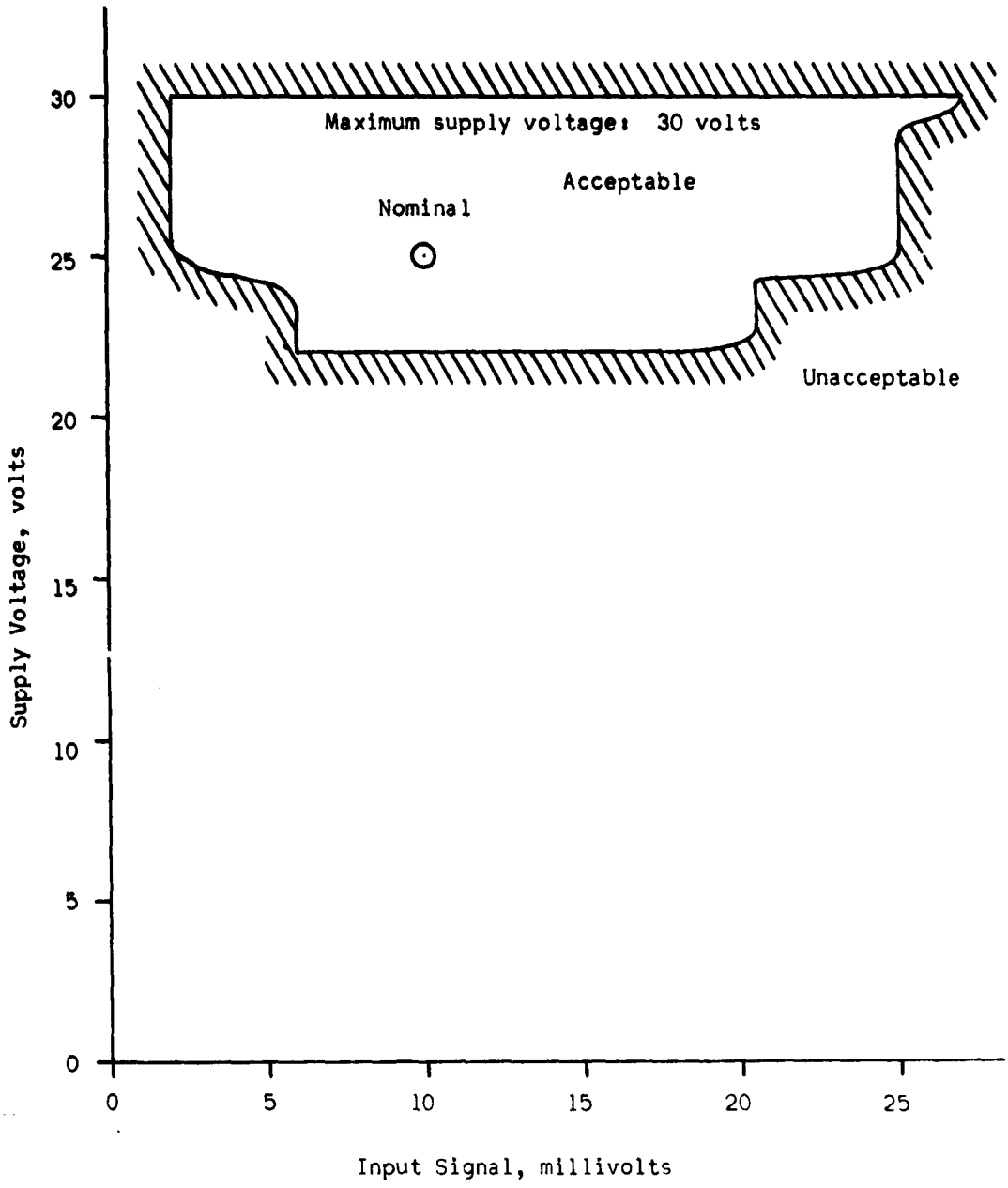



FIGURE 8. PERFORMANCE PROFILE FOR SUPPLY VOLTAGE AND INPUT SIGNAL

## 4. DESIGN CONSIDERATIONS

The gain of MA/03 XX is controlled by the resistance between terminals [5 - 0] and [C]. Provision has been made to include a resistive effect of 130 ohms internal to the module. This will provide for the minimum gain of 50. Then an external resistor connected between terminals [5 - 0] and [C] (in parallel with the 130 ohms) can be used to increase the gain. Figure 9 is a curve showing the value of external resistance needed to obtain a designated value of gain. The tolerance on the gain is ±2 per cent. It is expected that the MA 03 XX functional modules will ultimately be specified for a series of fixed gains covering the present gain range. This step should be taken to minimize the need for external connections.

The present preamplifier design has an output limited to 1 volt rms, at which point clipping begins. It would be advantageous in many instances to have more than 1 volt rms output available, and any design improvements providing greater output voltage without clipping would be desirable.

The main factors affecting distortion are the load resistance and input voltage.

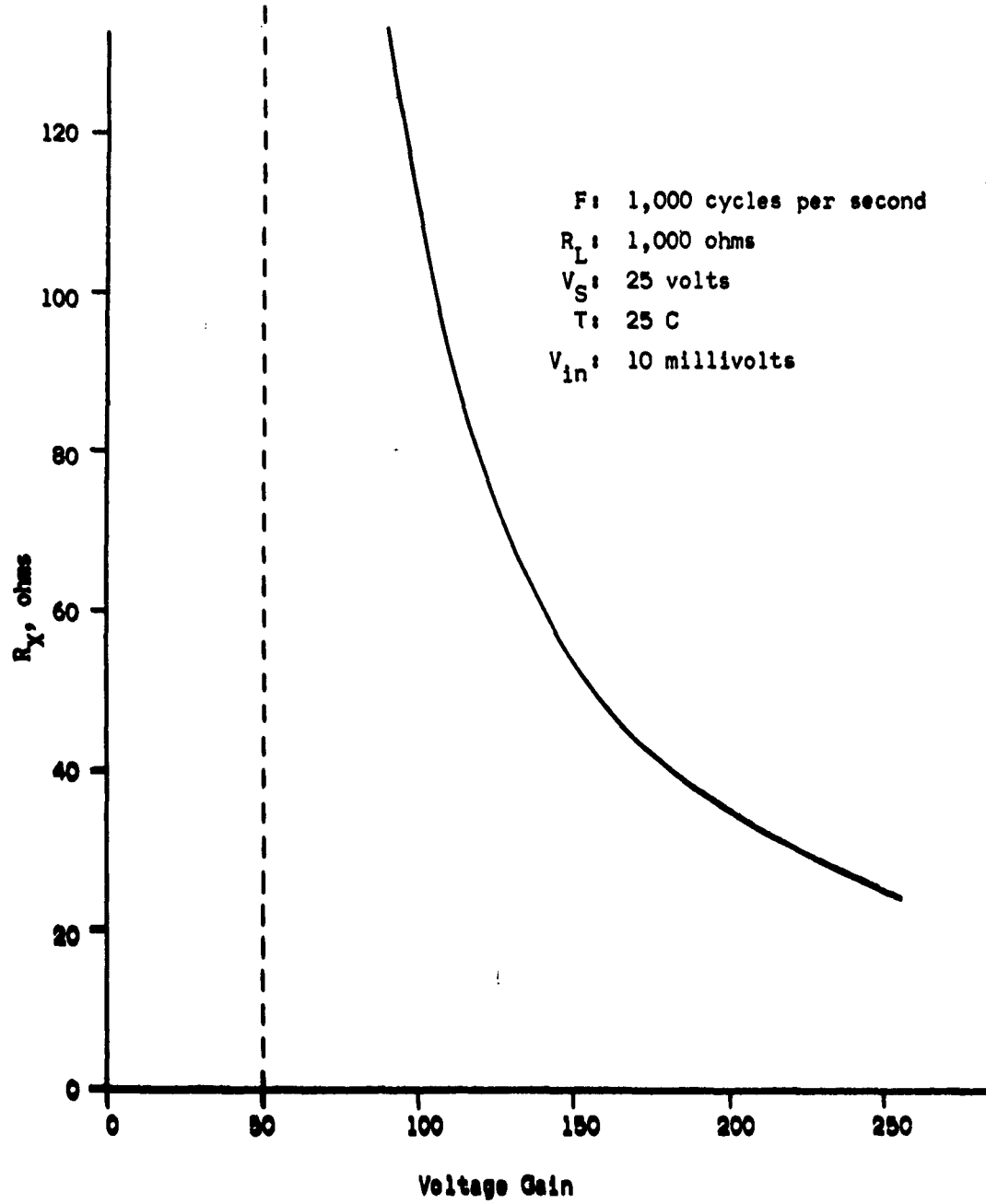
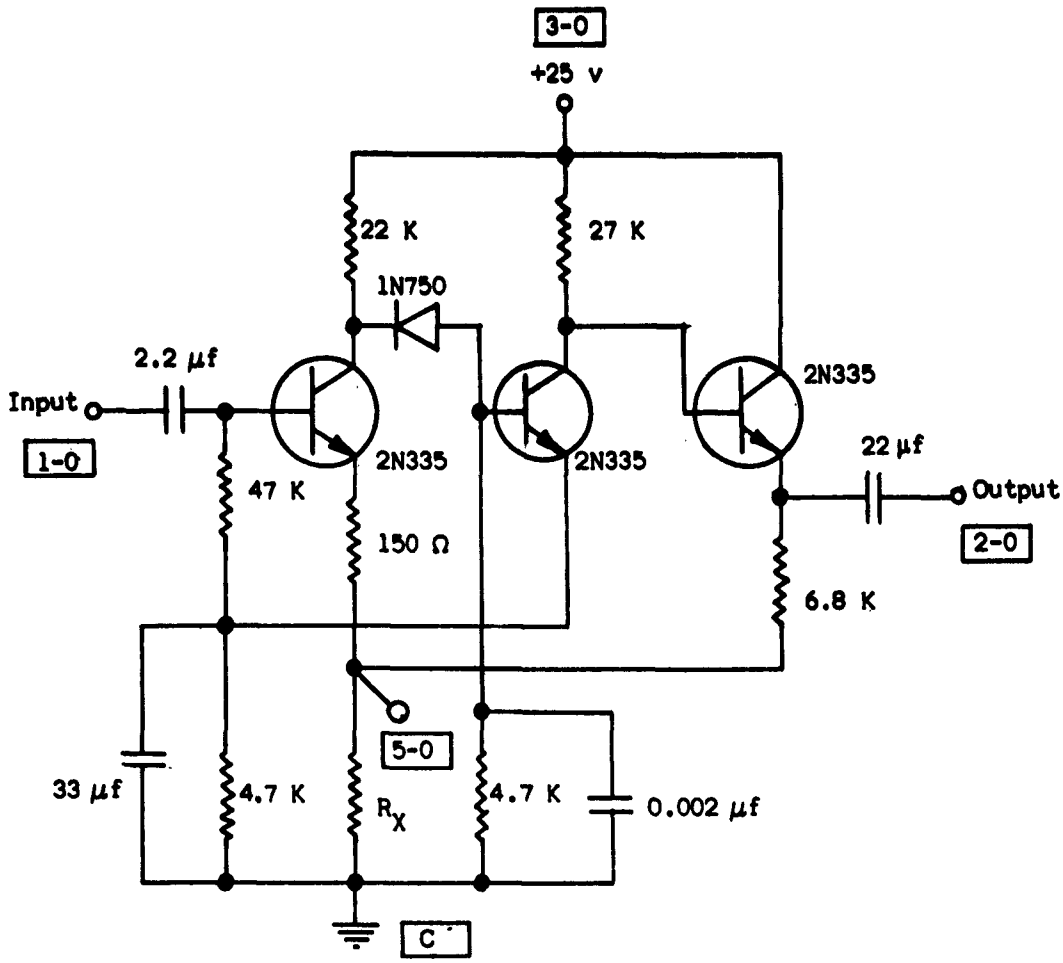



FIGURE 9. EXTERNAL RESISTOR VERSUS VOLTAGE GAIN

## 5. PROTOTYPE CIRCUIT

PREFERRED SEMICONDUCTOR CIRCUIT NO. 23

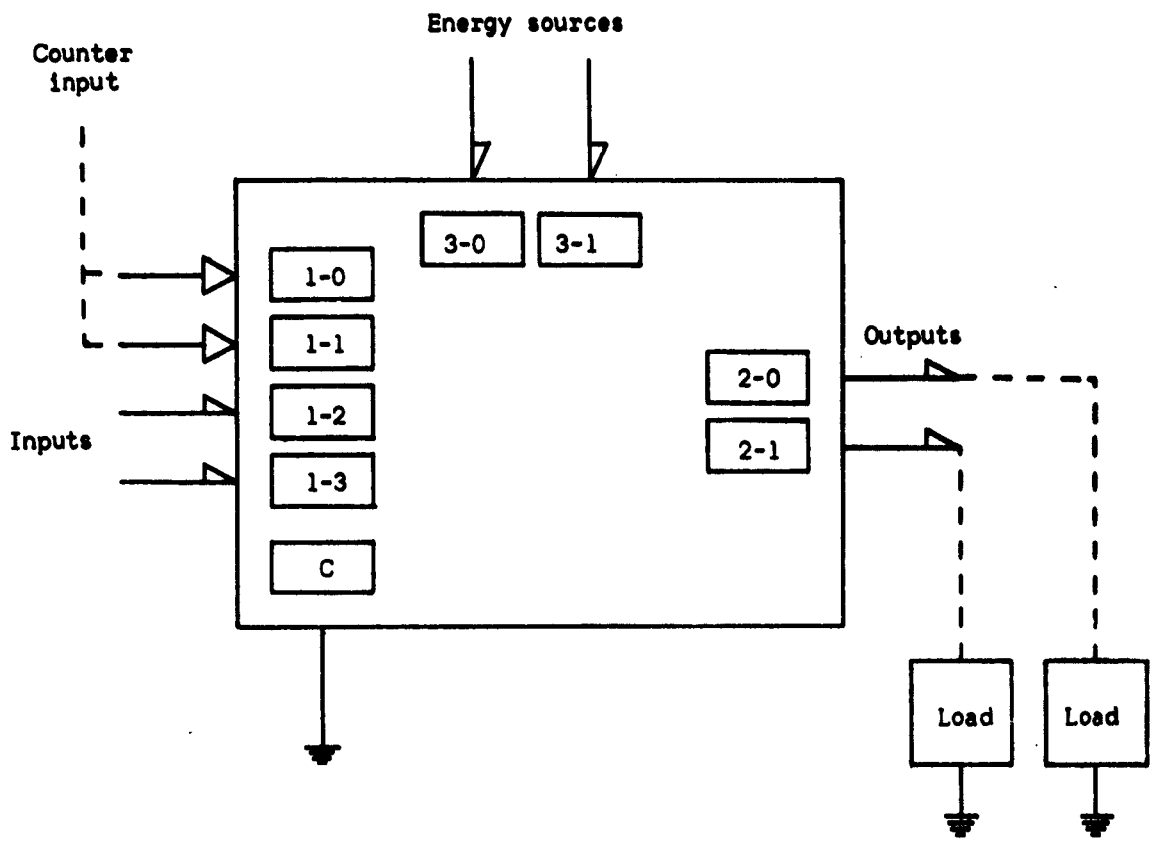
(Audio Preamplifier)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

# PREFERRED MICROELECTRONIC FUNCTION MA/13 XX

## (Bistable Multivibrator)




Prototype: Preferred Semiconductor Circuit No. 14 Adaption No. 3
(NAVWEPS 16-1-519-2)
Formerly Preferred Circuit No. 250, Adaption No. 3
(NAVWEPS 16-1-519)
(See Section 5)

## 1. GENERAL

MA/13 XX is a slow-speed bistable functional module (multivibrator) which provides complementary two state outputs on two terminals, 2 - 0 and 2 - 1. The two output states are approximately +1 and +18 volts. The nominal output speed of MA/13 XX is 40 kc maximum depending on load and input pulse characteristics.

The preferred energy sources are one or more of the following:

3 - 0, +25 volts ± 10 per cent at 10 ma max

3 - 1, - 6 volts ± 10 per cent at 0.7 ma max.

In addition, any of the standard voltages in Section 3.5.1 of Specification NAVAIRDEVCEN EL5-13A are acceptable.

## 2. APPLICATION

MA/13 XX may be used as a gate or switch, or may be cascaded without buffer amplifiers for use as a counter (Figure 1). The module responds to input signals applied to four terminals: [1 - 0] and [1 - 1] for pulse inputs, and [1 - 2] and [1 - 3] for direct connections. Which of the two possible states is present on a particular output terminal depends upon the last signals applied to the four input terminals. The module responds to negative pulse inputs of a nominal 14-volt amplitude and 3 $\mu$s duration at the pulse input terminals and to d-c inputs of +1 ma (for 10 $\mu$s duration minimum) or -4 ma (for 5 $\mu$s duration minimum) at the direct connection terminals. How MA/133 XX responds to input pulses depends on the state of the module before the pulse arrives. (The state of the module is defined by the voltage levels on the output terminals.) The response to pulse inputs with no direct connections is shown in Table 1. The last two rows in Table 1 correspond to the condition that exists when the pulse inputs are connected together for a counting operation, while the others show the effect of separate inputs when the module is used as a gate or switch.

The module will respond also to inputs at terminals [1 - 2] and [1 - 3]: +1 ma for 10 $\mu$s applied at [1 - 2] will turn on output [2 - 1] (to the +1 volt level), and +1 ma applied at [1 - 3] will turn on [2 - 0]. The outputs are complementary such that when [2 - 0] is on, [2 - 1] is off. Conversely, negative current of -4 ma can be used at [1 - 2] to turn off output [2 - 1] and at [1 - 3] to turn off [2 - 0].

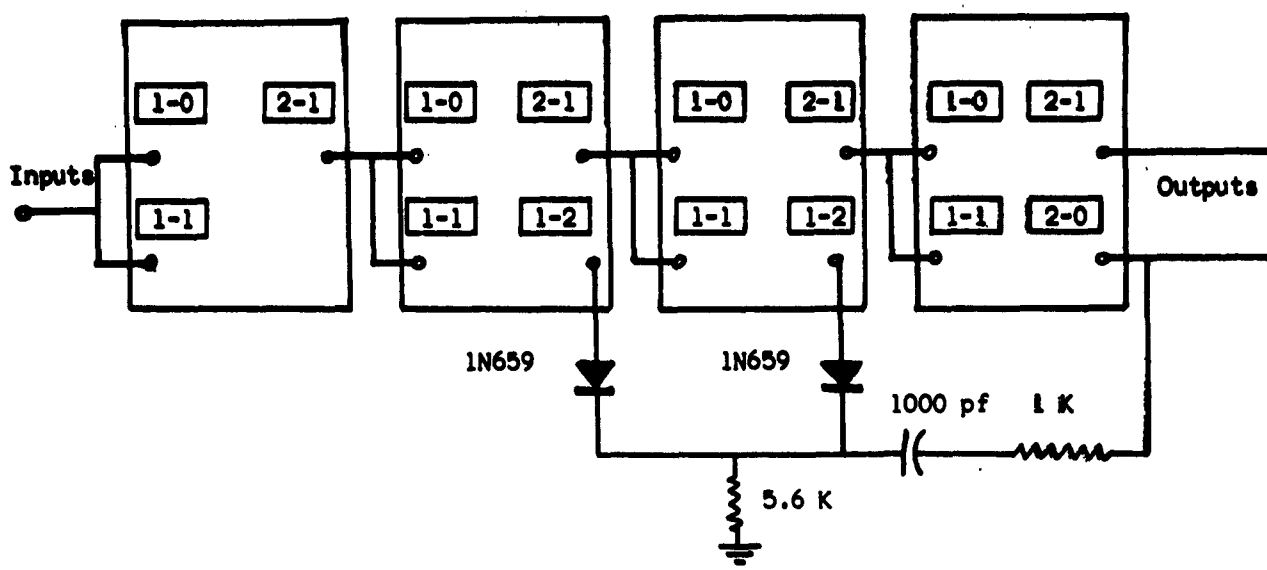



FIGURE 1. FOUR STAGES OF MA/13 XX CONNECTED FOR OPERATION AS A DECADE COUNTER

TABLE 1. INPUT-OUTPUT CHARACTERISTICS OF MA/13 XX WITH INPUTS TO TERMINALS [1 - 0] and [1 - 1]

| Output State Before Input Pulse | | Pulse Inputs(a) | | Output State After Input Pulse | |
|---|---|---|---|---|---|
| [2 - 0] | [2 - 1] | [1 - 0] | [1 - 1] | [2 - 0] | [2 - 1] |
| Either | | 0 | 0 | No change | |
| 1 v | 18 v | 0 | 1 | 18 v | 1 v |
| 18 v | 1 v | 0 | 1 | No change | |
| 1 v | 18 v | 1 | 0 | No change | |
| 18 v | 1 v | 1 | 0 | 1 v | 18 v |
| 1 v | 18 v | 1 | 1 | 18 v | 1 v |
| 18 v | 1 v | 1 | 1 | 1 v | 18 v |

(a) 0 = no input, 1 = negative 14-volt input pulse. No inputs to [1 - 2] and [1 - 3].

Note: In the prototype circuit the application of -4 ma to the inputs can cause the inputs can cause the input reverse voltage rating of the active element to be exceeded. The microcircuit module should be designed to avoid this difficulty.

When signals are applied to more than one input terminal, the result is predictable under certain circumstances. Table 2 gives the response of MA/13 XX where there are inputs to the direct connection terminals [1 - 2] and [1 - 3]. In general, inputs at the direct connections take precedence over pulse inputs.

TABLE 2. INPUT-OUTPUT RESPONSE OF MA/13 XX WITH ADDITIONAL INPUTS

| Inputs[a, b] | | Output State After Input[c] | |
|---|---|---|---|
| 1 - 2 | 1 - 3 | 2 - 0 | 2 - 1 |
| + | + | Indeterminate | |
| - | - | Indeterminate | |
| 0 or + | - | 18 v | 1 v |
| - | 0 or + | 1 v | 18 v |
| + | 0 or - | 18 v | 1 v |
| 0 or - | + | 1 v | 18 v |

(a) Input pulses may be present at terminals 1 - 0 and 1 - 1 without affecting the final state.

(b) 0 = no input, or input source disconnected from module.
(+) = +1 ma input with duration greater than 10 $\mu$s.
(-) = -4 ma input with duration greater than 5 $\mu$s.

The table is valid only when these inputs are present after the pulse inputs at terminals 1 - 0 and 1 - 1 for the minimum times shown above.

(c) The state of the outputs before inputs has no effect on the final state.

In terms of logic design* MA/13 XX can be regarded as a JK flip-flop with pulse inputs at terminals [1 - 0] and [1 - 1] only. Also the module will function as an RS flip-flop with inputs at terminals [1 - 2] and [1 - 3] only. There are, however, certain qualifications. The RS function overrides the JK function when both sets of inputs are present although JK inputs may delay the RS function for the duration of the JK inputs. Also there are three levels (+, -, and 0) which can be used as RS inputs. Any pair of the three levels can be used to satisfy RS requirements. When terminals [1 - 0] and [1 - 1] are connected together as for counter operation, the device can be labeled a T flip-flop with an overriding RS function or as a modified RST flip-flop which has an overriding RS function with three input levels as above. A truth table for the combined operation is given in the Addendum to the MA/13 XX functional description.

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* For details that are implied by these flip-flop types, see: Phister, Jr., M., Logical Design of Digital Computers, John Wiley & Sons, 1958, pp 121-132.

## 3. PERFORMANCE

Parameter limits under nominal operating conditions are summarized in Table 3. Operating characteristics which extend beyond nominal conditions are given in Figures 2 to 11. Inputs [1 - 0] and [1 - 1] are connected together as in counter operation for all of the following graphs and tables.

TABLE 3. BASIC FUNCTION PERFORMANCE RANGES AND LIMITS

| Parameter | Minimum | Design Center | Maximum |
|---|---|---|---|
| Input pulse amplitude | -14 v | -18 v | (a) |
| Nominal Input pulse duration | 3 $\mu$s | 4 $\mu$s | 5 $\mu$s |
| Input pulse duration, absolute limit | 1/2 $\mu$s | -- | -- |
| Input pulse rise time(b) | -- | -- | -- |
| Input impedance, [1 - 0] and [1 - 1] connected together | (c) | 1 "H" load | (c) |
| Output voltage, high level | (d) | +19 v | (d) |
| Output voltage, low level, d-c(e) | -- | -- | +1 v |
| Peak a-c component of current from source [3 - 0] at change of state | -- | -- | 3 ma |

(a) Maximum trigger voltage for the prototype is -25 v; however, care must be exercised to stay within the reverse voltage rating of the active device.

(b) The interaction of input pulse rise time variation and required pulse amplitude is given in Figure 10.

(c) The input impedance of module MA/13 XX is approximated by a 2200 pf capacitor in series with a parallel combination of a 200 pf capacitor and a 5.1 K resistor. This combination with one terminal grounded is tentatively labeled an "H" load. Since an "H" load is an approximation to the module input impedance (nonlinear), but is not exact, no tolerances on the "H" load are defined.

(d) The high level output voltage level at no load or with loads with no resistive (d-c) path to ground is approximately 70 per cent of the [3 - 0] source

voltage. Also not more than 70 per cent of the source voltage variations (ripple, etc.) will exist at the outputs in the high voltage state. Figure 6 gives data for resistive loads (with d-c path to ground).

(p) Not more than 3 per cent of the 3 - 0 source voltage variations (rise, ripple, etc.) will exist at the outputs in the on state (low voltage) superimposed on the d-c voltage.

Figures 2 and 3 show acceptable output rise time and fall time variations resulting from different numbers of "H" loads. The amplitude of the output depends on the voltage of the source at 3 - 0 and the type of load. For loads without a d-c path to ground, the amplitude will be not less than 70 per cent of the source voltage. For loads that have a d-c component, the resulting output amplitude can be determined with the aid of Figure 6. Capacity variations in the load will result in changes in output time delay and fall time, and also in the required duration of the input pulse. These are shown in Figures 4, 5, and 7.

Input pulse amplitude and duration will control, to some extent, the time delay of the output and the maximum speed of response of the module. See Figures 8 and 9. Additional input pulse characteristics and module responses are given in Figures 10 and 11. It should be noted that Figures 9 and 11 differ in types of loads on the module.

The applicable temperature range is -55 to +125 C. The rate of heat dissipation should be less than 0.26 watt. This figure is the maximum heat dissipated by the prototype circuit.

OUTPUT CHARACTERISTICS

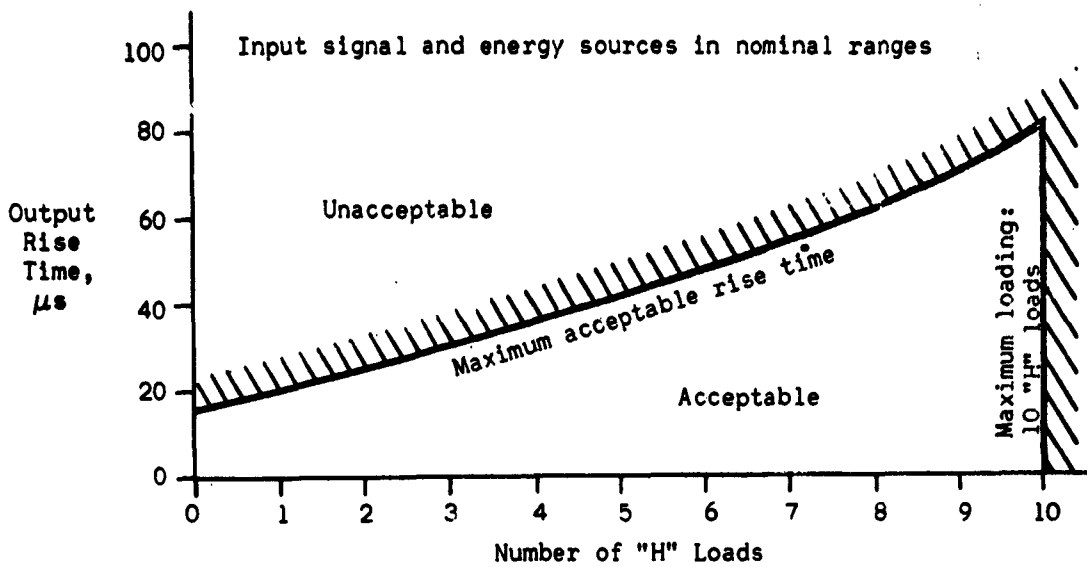



FIGURE 2. RISE TIME OF OUTPUT WAVEFORM

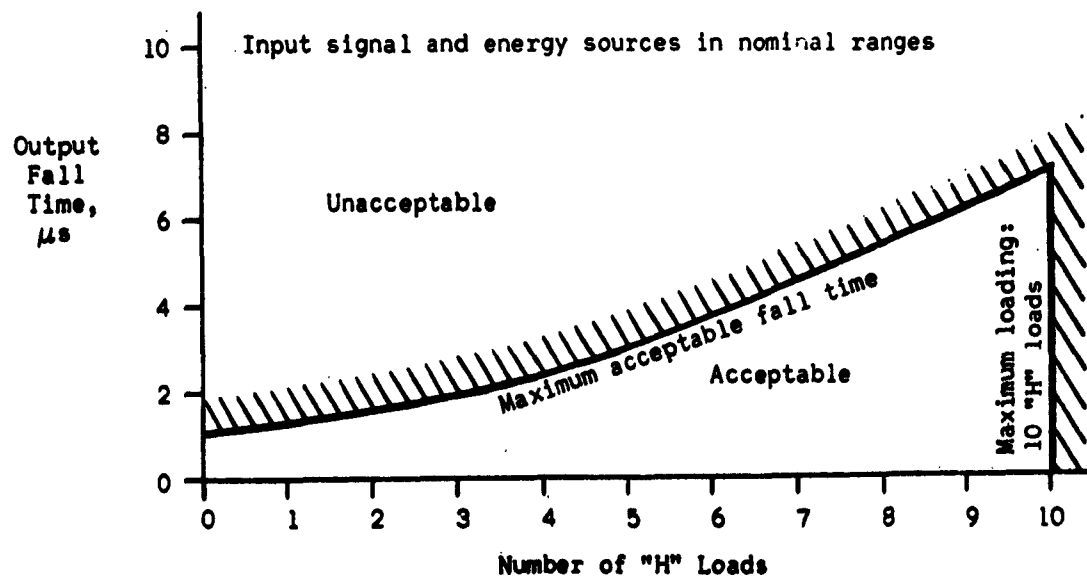



FIGURE 3. FALL TIME OF OUTPUT WAVEFORM

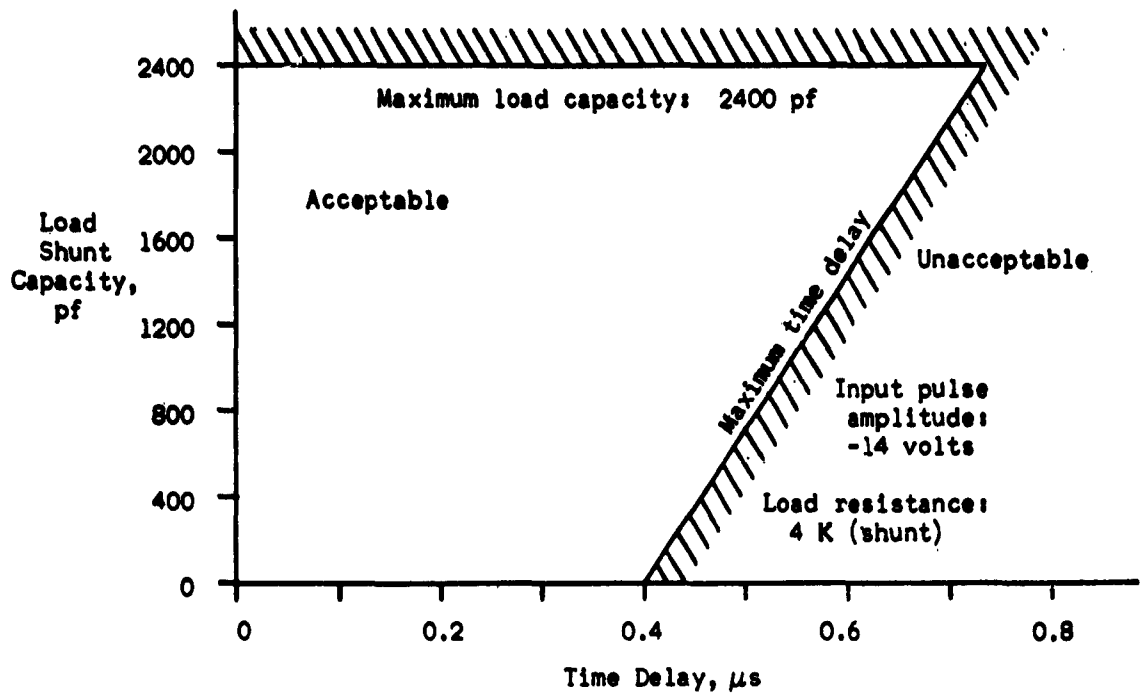



FIGURE 4. TIME DELAY, INPUT TO OUTPUT, VERSUS LOAD SHUNT CAPACITY

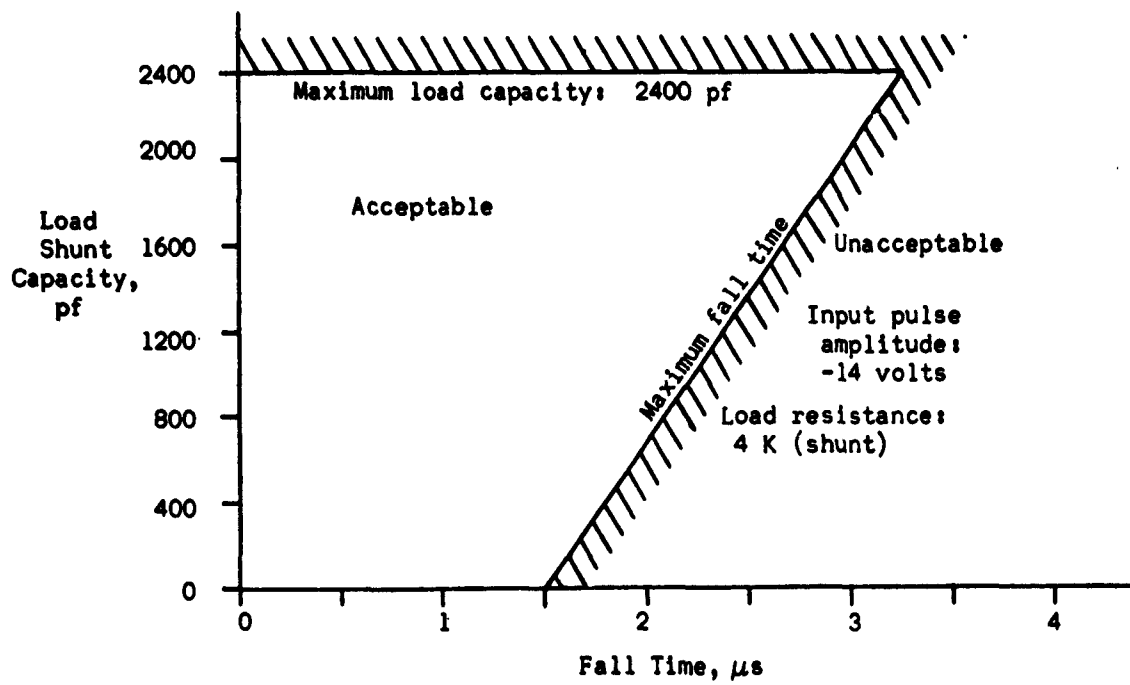



FIGURE 5. FALL TIME OF OUTPUT VERSUS LOAD SHUNT CAPACITY

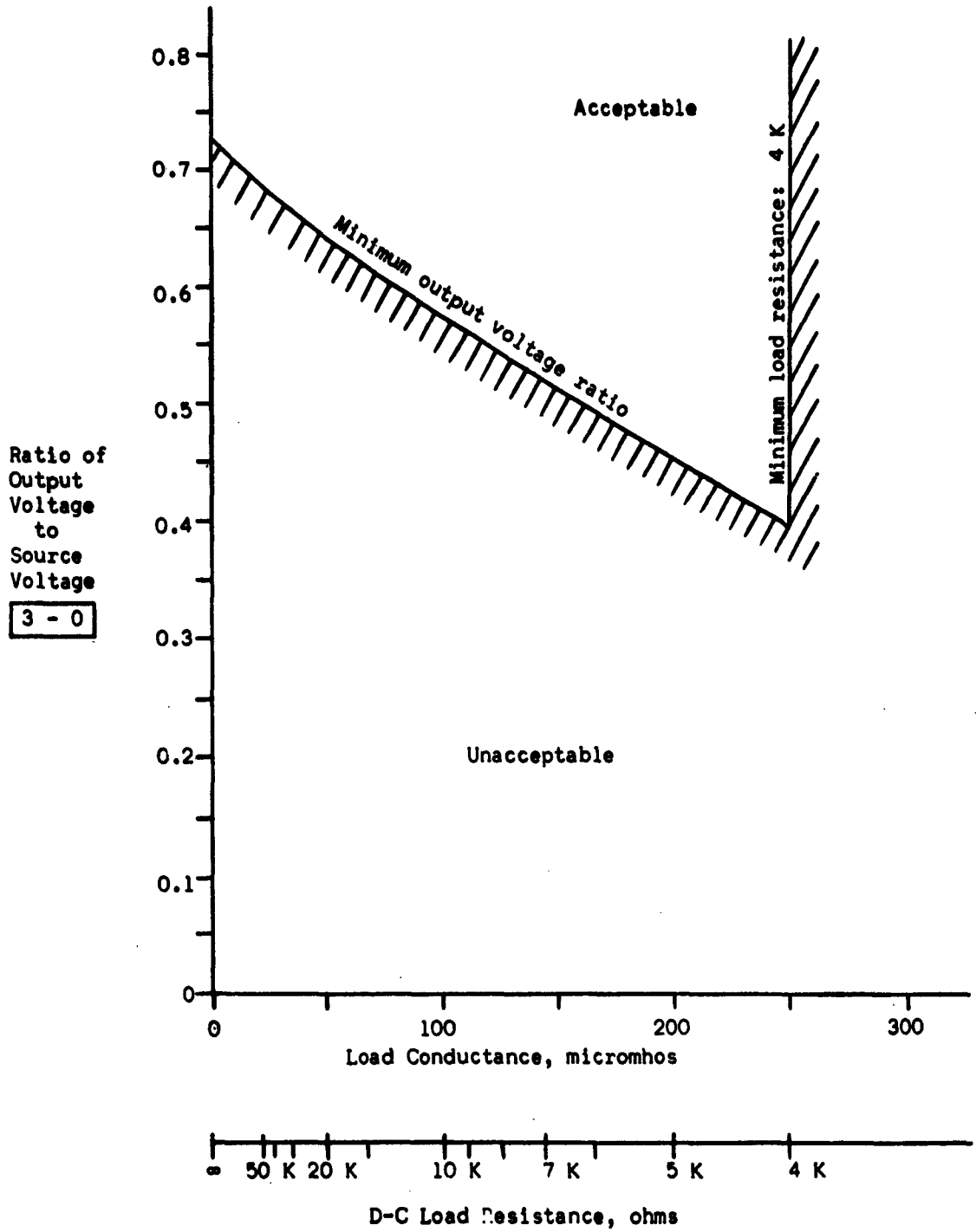



FIGURE 6. VARIATION OF OUTPUT AMPLITUDE WITH D-C LOAD

TRANSFER CHARACTERISTICS

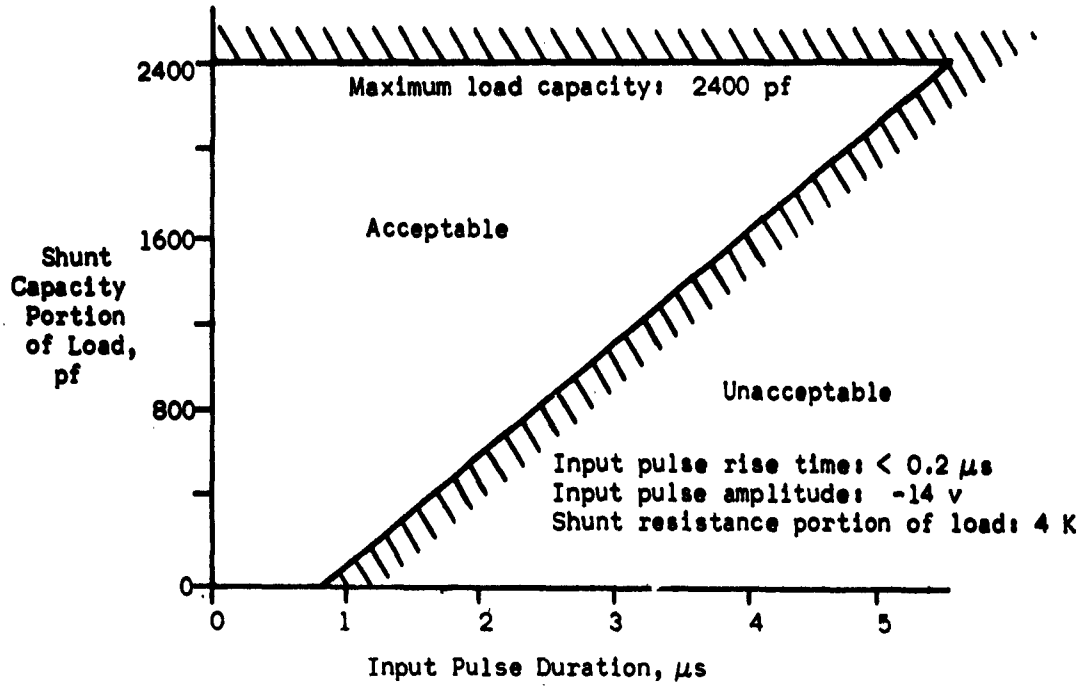



FIGURE 7. PERFORMANCE PROFILE, SHUNT LOAD CAPACITY AND INPUT PULSE DURATION REQUIRED FOR RELIABLE OPERATION

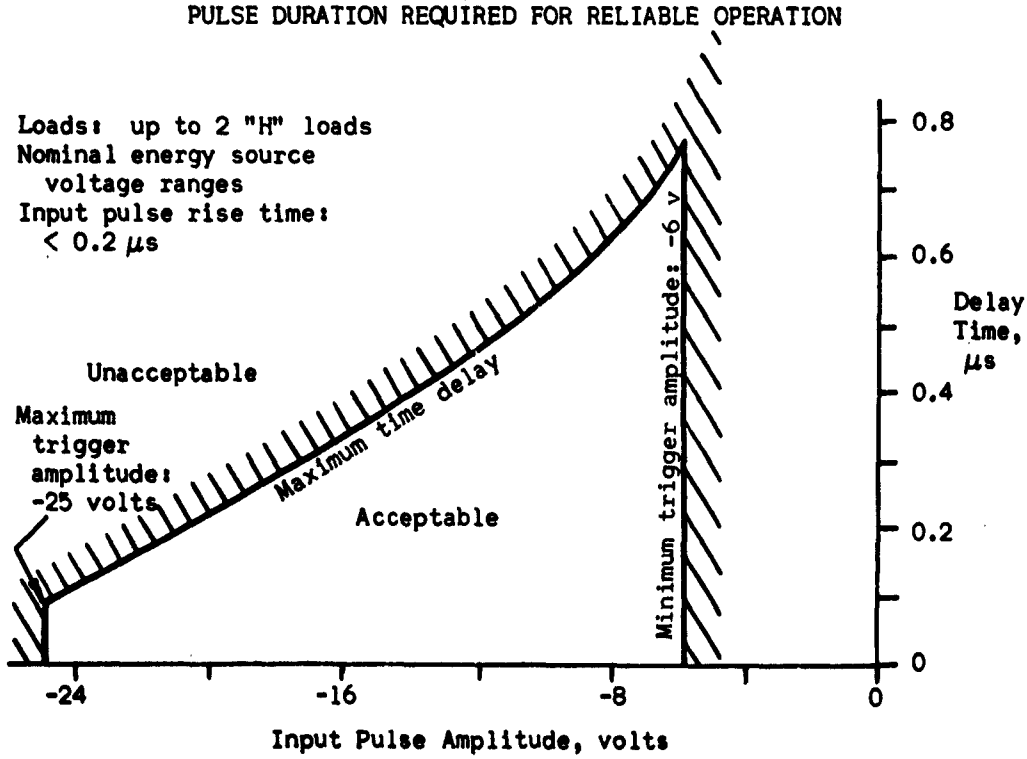



FIGURE 8. PERFORMANCE PROFILE, FUNCTION DELAY TIME AND INPUT PULSE AMPLITUDE

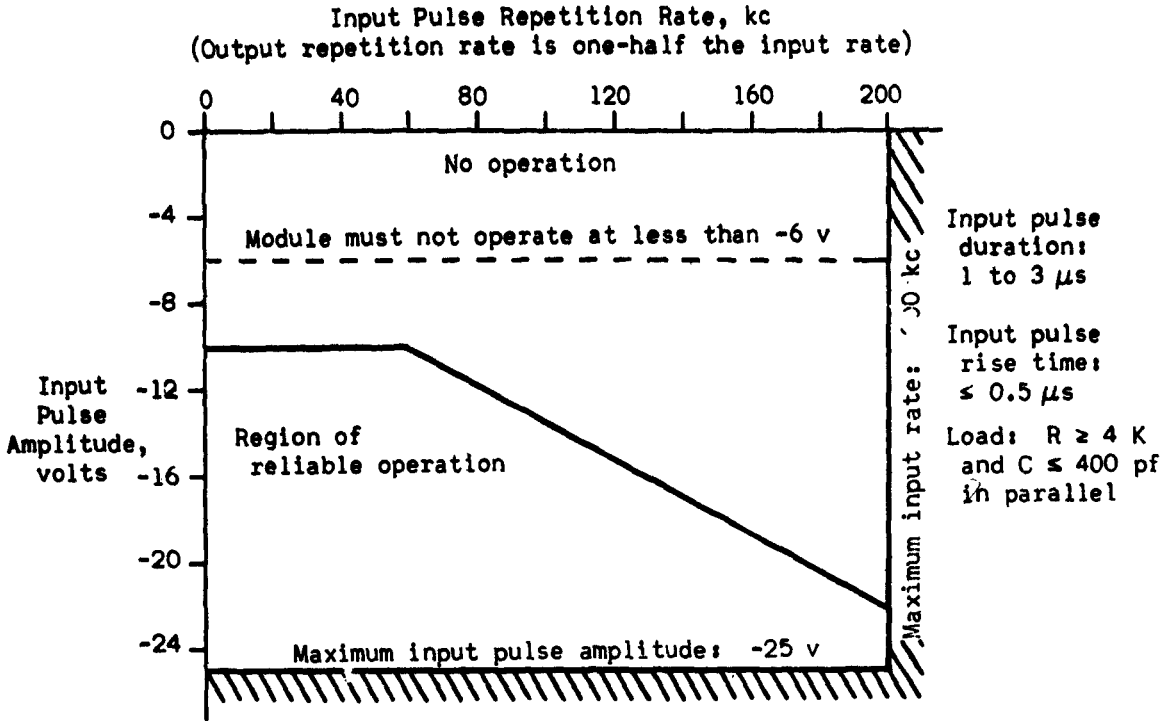



FIGURE 9. PERFORMANCE PROFILE, INPUT PULSE AMPLITUDE AND OPERATION SPEED

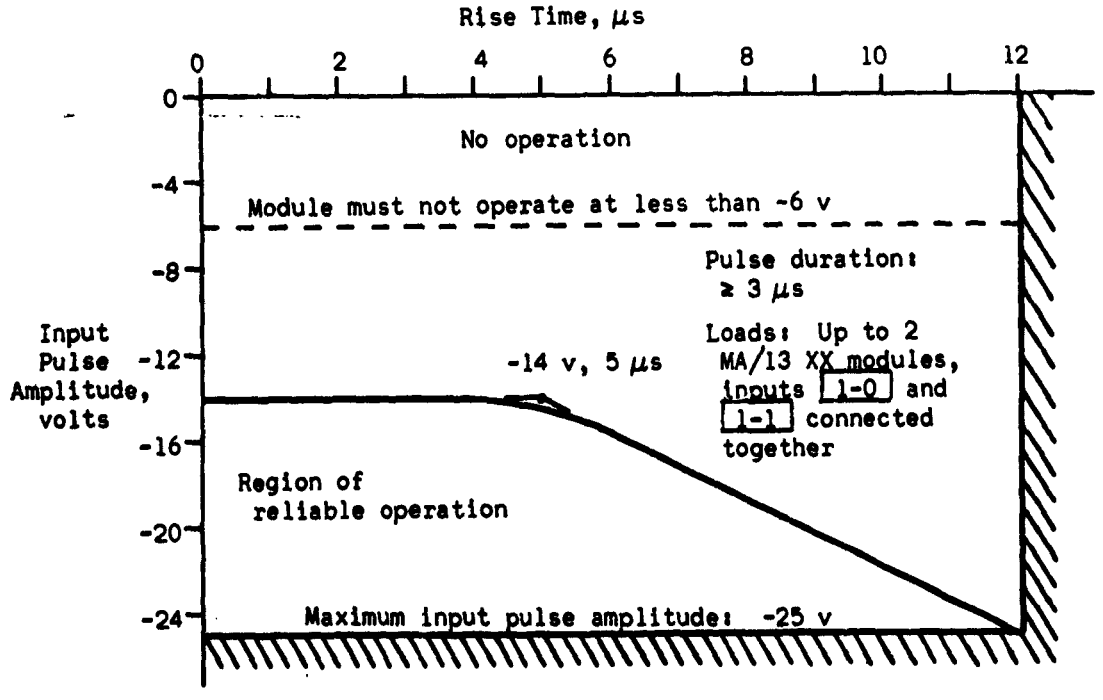



FIGURE 10. PERFORMANCE PROFILE, INPUT PULSE CHARACTERISTICS

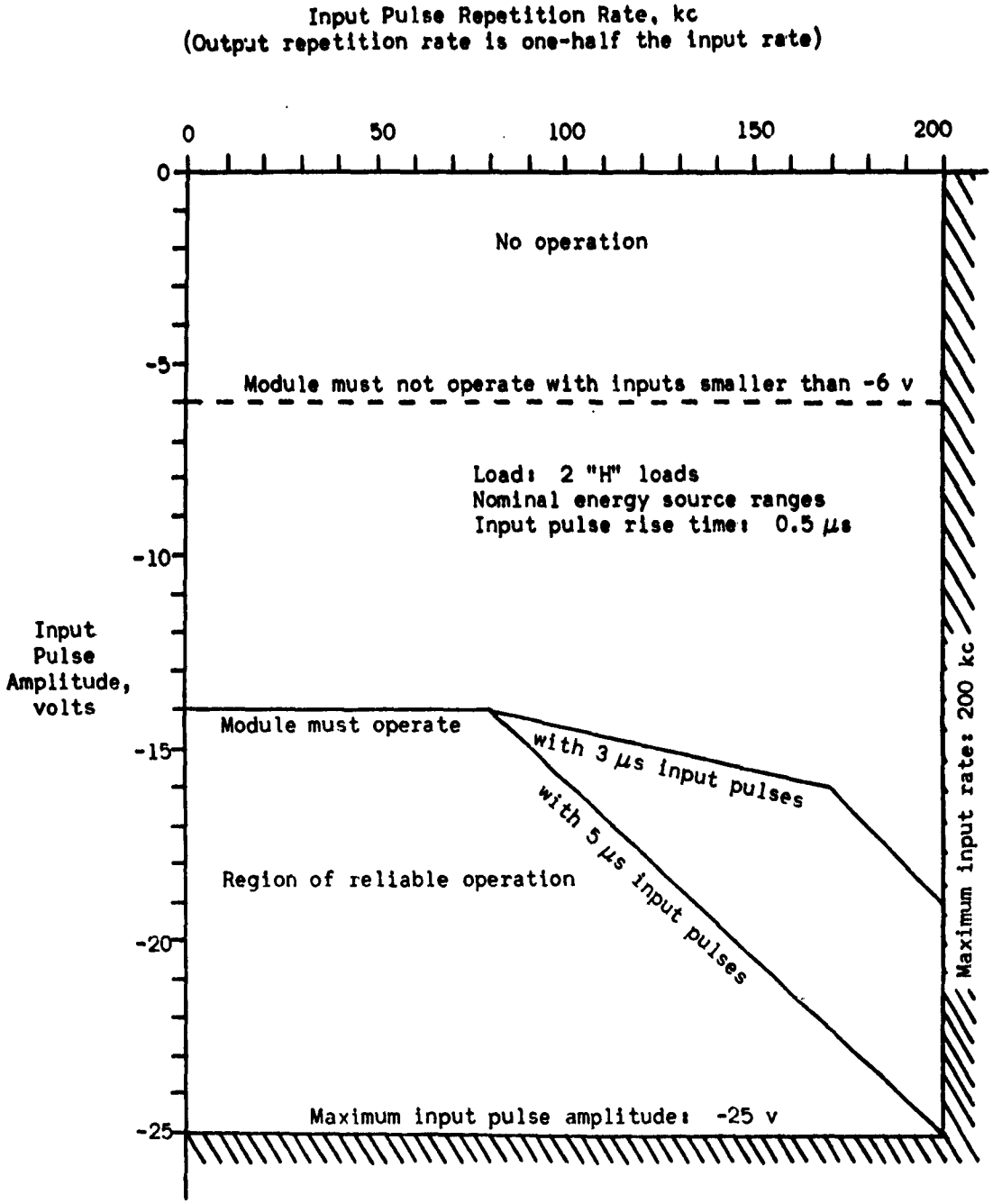



FIGURE 11. PERFORMANCE PROFILE, INPUT PULSE CHARACTERISTICS AND OPERATION SPEED

## 4. DESIGN CONSIDERATIONS

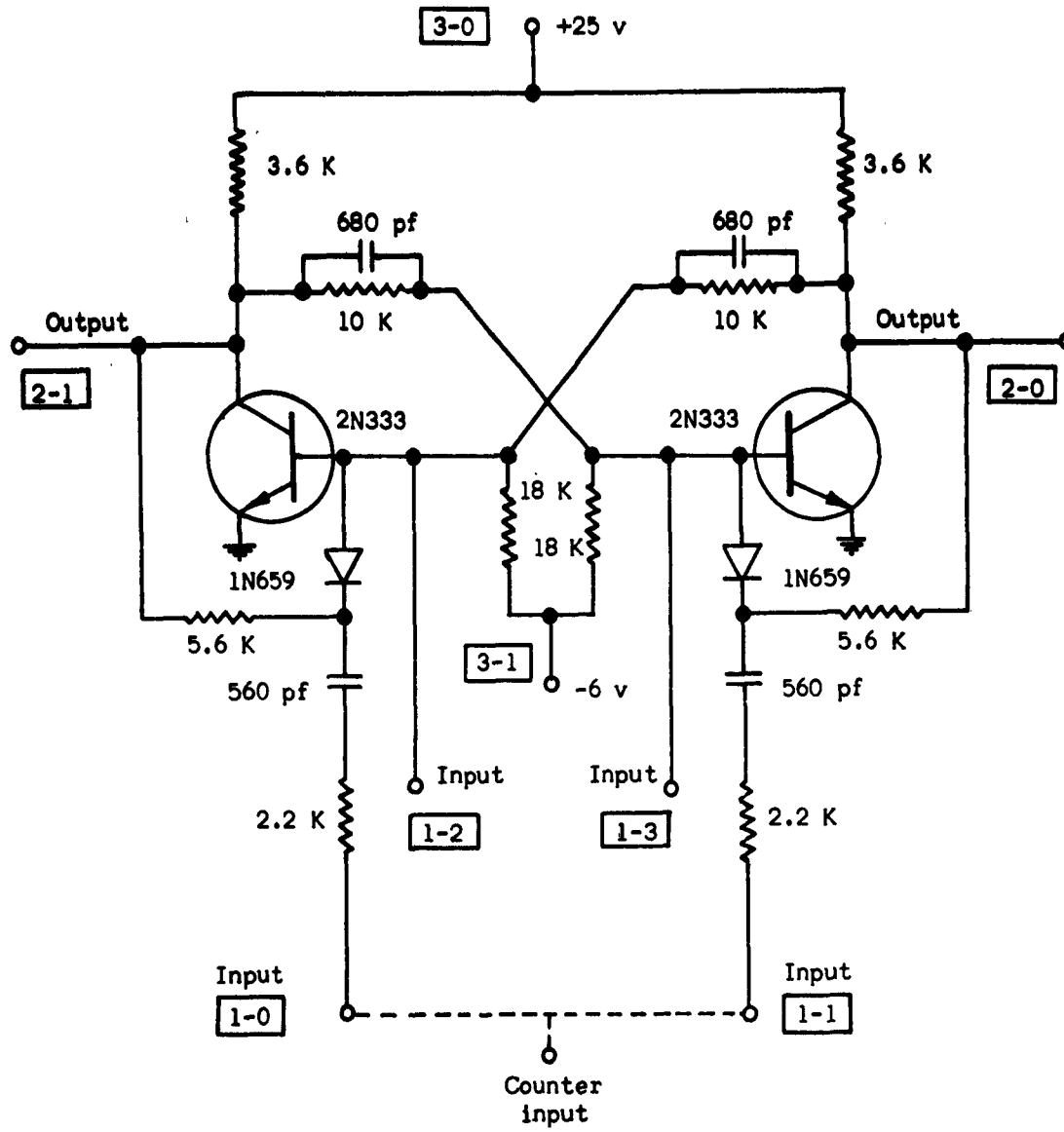
The prototype can be adjusted for changes in load, and input and output characteristics by adjusting various resistors and capacitors. Module MA/13 XX is fixed for one set of conditions equivalent to that of the basic form of Adaption 3 of the prototype. This form includes the counting function.

Should MA/13 XX be used with other than nominal energy source voltage at terminal 3 - 1, the input impedance, and required input pulse amplitudes, would be affected and if the voltage tends toward zero, the function may cease to be bistable.

## 5. PROTOTYPE CIRCUIT

PREFERRED SEMICONDUCTOR CIRCUIT NO. 14, ADAPTION NO. 3

(Bistable Multivibrator)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

ADDENDUM

COMPLETE TRUTH TABLE

| Output State Before Input Pulse, volts | | Inputs (a) | | | | Output State After Input Pulse, volts | |
|---|---|---|---|---|---|---|---|
| | | Pulse | | Direct | | | |
| 2-0 | 2-1 | 1-0 | 1-1 | 1-2 | 1-3 | 2-0 | 2-1 |
| 1 | 18 | 0 | 0 | 0 | 0 | No change | |
| 18 | 1 | 0 | 0 | 0 | 0 | No change | |
| 1 | 18 | 1 | 0 | 0 | 0 | No change | |
| 18 | 1 | 1 | 0 | 0 | 0 | 1 | 18 |
| 1 | 18 | 0 | 1 | 0 | 0 | 18 | 1 |
| 18 | 1 | 0 | 1 | 0 | 0 | No change | |
| 1 | 18 | 1 | 1 | 0 | 0 | 18 | 1 |
| 18 | 1 | 1 | 1 | 0 | 0 | 1 | 18 |
| 1 | 18 | 0 | 0 | 1 | 0 | No change | |
| 18 | 1 | 0 | 0 | 1 | 0 | 1 | 18 |
| 1 | 18 | 1 | 0 | 1 | 0 | No change | |
| 18 | 1 | 1 | 0 | 1 | 0 | 1 | 18 |
| 1 | 18 | 0 | 1 | 1 | 0 | 1(b) | 18 |
| 18 | 1 | 0 | 1 | 1 | 0 | 1(c) | 18 |
| 1 | 18 | 1 | 1 | 1 | 0 | 1(b) | 18 |
| 18 | 1 | 1 | 1 | 1 | 0 | 1(a) | 18 |
| 1 | 18 | 0 | 0 | 2 | 0 | 18 | 1 |
| 18 | 1 | 0 | 0 | 2 | 0 | No change | |
| 1 | 18 | 1 | 0 | 2 | 0 | 18(d) | 1 |
| 18 | 1 | 1 | 0 | 2 | 0 | 18(d) | 1 |
| 1 | 18 | 0 | 1 | 2 | 0 | 18 | 1 |
| 18 | 1 | 0 | 1 | 2 | 0 | No change | |
| 1 | 18 | 1 | 1 | 2 | 0 | 18(d) | 1 |
| 18 | 1 | 1 | 1 | 2 | 0 | 18(d) | 1 |
| 1 | 18 | 0 | 0 | 0 | 1 | 18 | 1 |
| 18 | 1 | 0 | 0 | 0 | 1 | No change | |
| 1 | 18 | 1 | 0 | 0 | 1 | 18 | 1(e) |
| 18 | 1 | 1 | 0 | 0 | 1 | 18 | 1(f) |
| 1 | 18 | 0 | 1 | 0 | 1 | 18 | 1 |
| 18 | 1 | 0 | 1 | 0 | 1 | No change | |
| 1 | 18 | 1 | 1 | 0 | 1 | 18 | 1(e) |
| 18 | 1 | 1 | 1 | 0 | 1 | 18 | 1(f) |

COMPLETE TRUTH TABLE
(CONT.)

| Output State Before Input Pulse, volts | | Inputs (a) | | | | Output State After Input Pulse, volts | |
|---|---|---|---|---|---|---|---|
| | | Pulse | | Direct | | | |
| 2-0 | 2-1 | 1-0 | 1-1 | 1-2 | 1-3 | 2-0 | 2-1 |
| 1 | 18 | 0 | 0 | 1 | 1 | Indeterminate | |
| 18 | 1 | 0 | 0 | 1 | 1 | Indeterminate | |
| 1 | 18 | 1 | 0 | 1 | 1 | Indeterminate | |
| 18 | 1 | 1 | 0 | 1 | 1 | Indeterminate | |
| 1 | 18 | 0 | 1 | 1 | 1 | Indeterminate | |
| 18 | 1 | 0 | 1 | 1 | 1 | Indeterminate | |
| 1 | 18 | 1 | 1 | 1 | 1 | Indeterminate | |
| 18 | 1 | 1 | 1 | 1 | 1 | Indeterminate | |
| 1 | 18 | 0 | 0 | 2 | 1 | 18 | 1 |
| 18 | 1 | 0 | 0 | 2 | 1 | No change (e) | |
| 1 | 18 | 1 | 0 | 2 | 1 | 18 | 1 (f) |
| 18 | 1 | 1 | 0 | 2 | 1 | 18 | 1 |
| 1 | 18 | 0 | 1 | 2 | 1 | 18 | 1 |
| 18 | 1 | 0 | 1 | 2 | 1 | No change (e) | |
| 1 | 18 | 1 | 1 | 2 | 1 | 18 | 1 (f) |
| 18 | 1 | 1 | 1 | 2 | 1 | 18 | 1 |
| 1 | 18 | 0 | 0 | 0 | 2 | No change | |
| 18 | 1 | 0 | 0 | 0 | 2 | 1 | 18 |
| 1 | 18 | 1 | 0 | 0 | 2 | No change | |
| 18 | 1 | 1 | 0 | 0 | 2 | 1 | 18 |
| 1 | 18 | 0 | 1 | 0 | 2 | 1 (b) | 18 |
| 18 | 1 | 0 | 1 | 0 | 2 | 1 (c) | 18 |
| 1 | 18 | 1 | 1 | 0 | 2 | 1 (b) | 18 |
| 18 | 1 | 1 | 1 | 0 | 2 | 1 (c) | 18 |
| 1 | 18 | 0 | 0 | 1 | 2 | No change | |
| 18 | 1 | 0 | 0 | 1 | 2 | 1 | 18 |
| 1 | 18 | 1 | 0 | 1 | 2 | No change | |
| 18 | 1 | 1 | 0 | 1 | 2 | 1 | 18 |
| 1 | 18 | 0 | 1 | 1 | 2 | 1 (b) | 18 |
| 18 | 1 | 0 | 1 | 1 | 2 | 1 (c) | 18 |
| 1 | 18 | 1 | 1 | 1 | 2 | 1 (b) | 18 |
| 18 | 1 | 1 | 1 | 1 | 2 | 1 (c) | 18 |
| 1 | 18 | 0 | 0 | 2 | 2 | Indeterminate | |
| 18 | 1 | 0 | 0 | 2 | 2 | Indeterminate | |
| 1 | 18 | 1 | 0 | 2 | 2 | Indeterminate | |
| 18 | 1 | 1 | 0 | 2 | 2 | Indeterminate | |

COMPLETE TRUTH TABLE
(CONT.)

| Output State Before Input Pulse, volts | | Inputs (a) | | | | Output State After Input Pulse, volts | |
|---|---|---|---|---|---|---|---|
| | | Pulse | | Direct | | | |
| 2-0 | 2-1 | 1-0 | 1-1 | 1-2 | 1-3 | 2-0 | 2-1 |
| 1 | 18 | 0 | 1 | 2 | 2 | Indeterminate | |
| 18 | 1 | 0 | 1 | 2 | 2 | Indeterminate | |
| 1 | 18 | 1 | 1 | 2 | 2 | Indeterminate | |
| 18 | 1 | 1 | 1 | 2 | 2 | Indeterminate | |

(a) Inputs are defined as follows:
For 1-0 and 1-1: 0 is equivalent to no input.
1 is equivalent to a -14-volt pulse, duration of 3 to 5 $\mu$s.

For 1-2 and 1-3: 0 is equivalent to no input (not grounded).
1 is equivalent to -4 ma for 5 $\mu$s or more.
2 is equivalent to +1 ma for 10 $\mu$s or more.

(b) Output 2-0 is turned off momentarily during the pulse input at 1-1..

(c) Output 2-0 may be delayed or develop a spurious pulse depending upon the timing of the inputs.

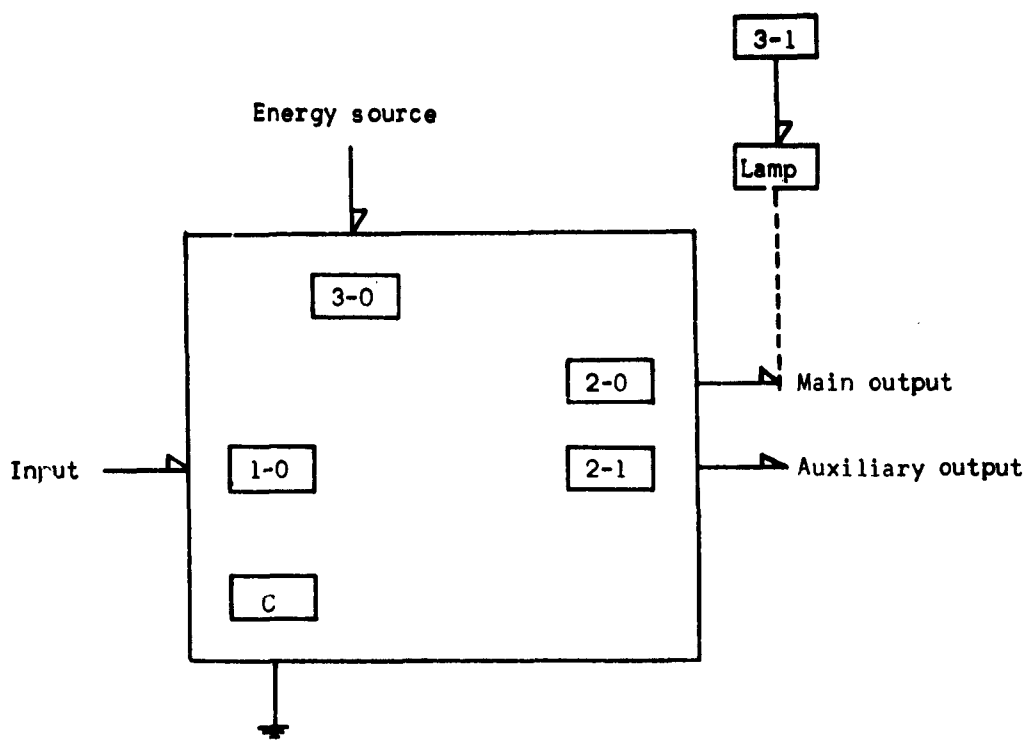
(d) The operation is indeterminate during the pulse input at 1-0 and/or 1-1.

(e) Output 2-1 may be delayed or develop a spurious pulse depending upon the timing of the inputs.

(f) Output 2-1 is turned off momentarily during the pulse input at 1-1.

PREFERRED MICROELECTRONIC FUNCTION MA/27 XX

(Driver)




Prototype: Preferred Semiconductor Circuit No. 13 (NAVWEPS 16-1-519-2)
Formerly Preferred Circuit No. 216 (NAVWEPS 16-1-519).
(See Section 5)

## 1. GENERAL

MA/27 XX is a driver designed to control the state of the Type 344 lamp under conservative operating conditions. It can be used to drive other devices which operate within the specified loading criteria.

The preferrred energy sources are one or more of the following:

[3 - 0], + 6 volts ± 10 per cent at 0.16 ma max

[3 - 1], -18 volts ± 10 per cent at 15 ma max.

In addition, any of the standard voltages in Section 3.5.1 of Specification NAVAIRDEVCEN EL5-13A are acceptable. However, a maximum voltage limitation of +6.6 and -24 volts is specified for energy sources [3 - 0] and [3 - 1], respectively.

## 2. APPLICATION

MA/27 XX is a driver which, by the electrical state of its input terminal [1 - 0], controls the electrical state of an output load element. The module has two output terminals: terminal [2 - 0] is the main output; terminal [2 - 1] is the auxiliary output. The main output is designed for a nominal load of 15 ma at 10 volts when operating the Type 344 lamp. In addition, this output connection may be used to drive other load elements, as determined by the characteristics shown in Figure 1.

The auxiliary output terminal is provided to give a greater flexibility in load-element driving capability. The Type 344 lamp may be driven from this connection with the addition of an external series resistance of 470 ohms ±20 per cent. Should any other lamp be used than Type 344, caution should be observed so that the series resistance used with the lamp will limit the surge current to a safe value. In other cases, the auxiliary output will drive load elements as determined by the characteristics of Figure 2. The two output terminals may not be used concurrently to drive their specified load elements.

The input logic governing the operation of either output is displayed in Table 1.

TABLE 1. INPUT LOGIC FOR MA 27 XX

| Input Signal Voltage[(a)] | Output State |
|---|---|
| Ground | Open Circuit |
| Negative | On |

(a) See Table 2 for voltage ranges.

3. PERFORMANCE

TABLE 2. BASIC FUNCTION PERFORMANCE RANGES

| Parameter | Minimum | Fifth Percentile | Design Center | Ninety-fifth Percentile | Maximum |
|---|---|---|---|---|---|
| Input signal voltage, ground | -0.5 v | | 0.0 | | +12 v(a) |
| Input signal voltage, negative(b) | -5.6 v | | -6.2 v | | -6.8 v |
| Input resistance (grounded input)(c) | 33 KΩ | 36 KΩ | 39 KΩ | | |
| Input resistance (negative input) | 5.5 KΩ | 5.7 KΩ | 6.0 KΩ | | |
| Load current (grounded input) | | | | -90 μa | -105 μa |
| Load impedance, main connection. (resistance)(d) | 130 Ω | | 665 Ω | | >18.0 KΩ |
| Load impedance, auxiliary connection (resistance)(d) | 505 Ω | | 1135 Ω | | >18.0 KΩ |
| Peak voltage, main or auxiliary connection to ground | | | | | -24 v |

(a) The +12 volt specification is the maximum voltage limit for the active element in the prototype circuit.

(b) See Figure 4 for negative input signal limitations.

(c) Resistance measured with application of small positive voltage.

(d) Minimum applies over temperature range from -55 C to +25 C. See Figure 3 for minimum at temperatures above 25 C.

The electrical characteristics of the main and auxiliary output connections are given in Figures 1 and 2, respectively. These plots may be used for the determination of appropriate loading elements for MA/27 XX in those cases where the module is not utilized for driving the Type 344 lamp.

A performance profile displaying output load-element impedance against the operating ambient temperature is given in Figure 3. Any coordinate combination of output load impedance and ambient temperature that falls within the indicated failure region is not a permissible set. The maximum load-element impedance is not shown. It is assumed that the module will not be used to drive a load with greater impedance than three times its own input impedance under driving conditions.

In any case, internal heat dissipation is limited to 165 mw when using the main connection, or 15 mw when using the auxiliary connection. The temperature range is limited to between -55 C and +125 C, and may be subject to additional limitations as in Figure 3.

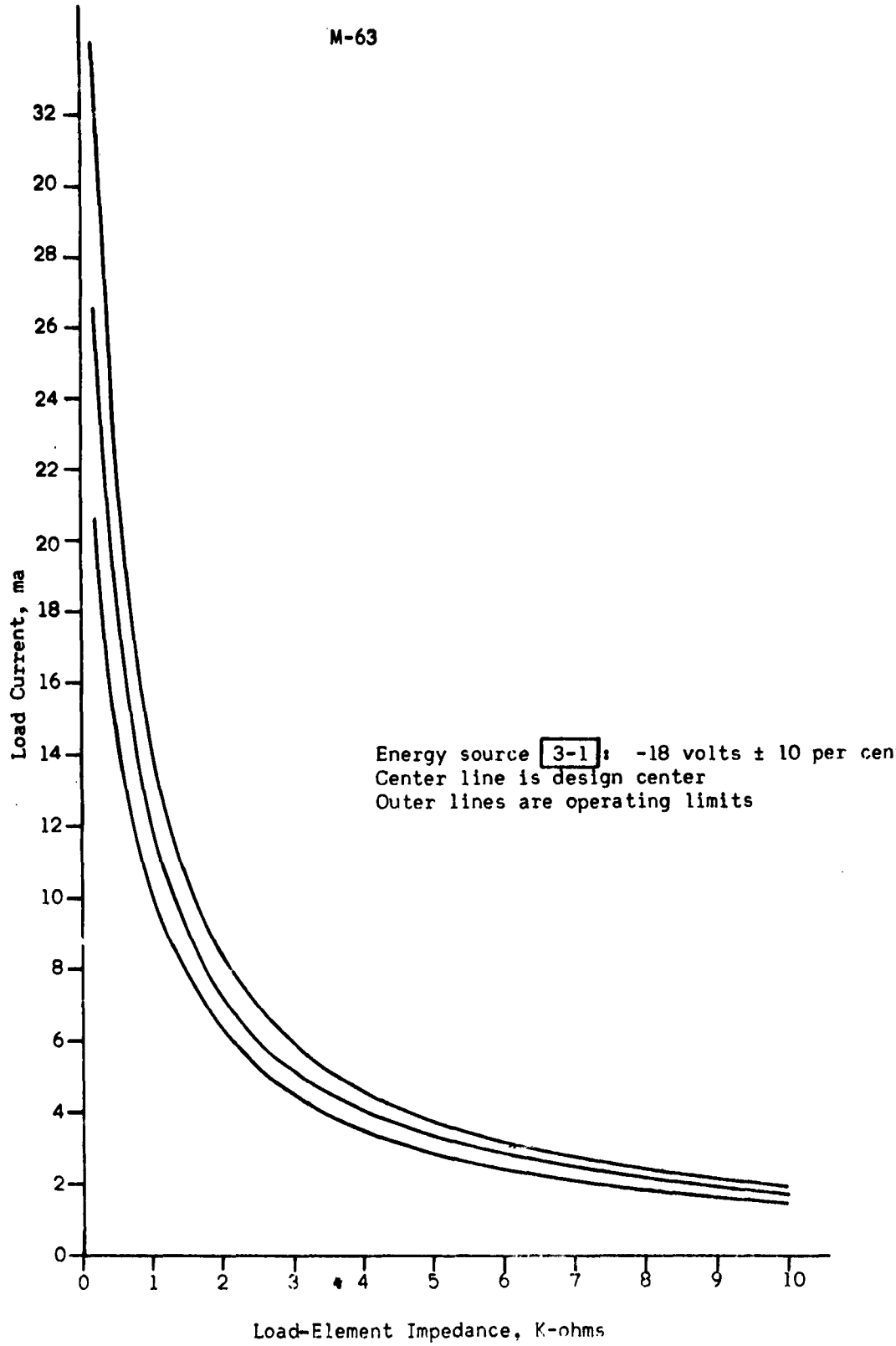



FIGURE 1. ELECTRICAL CHARACTERISTICS OF MAIN OUTPUT CONNECTION

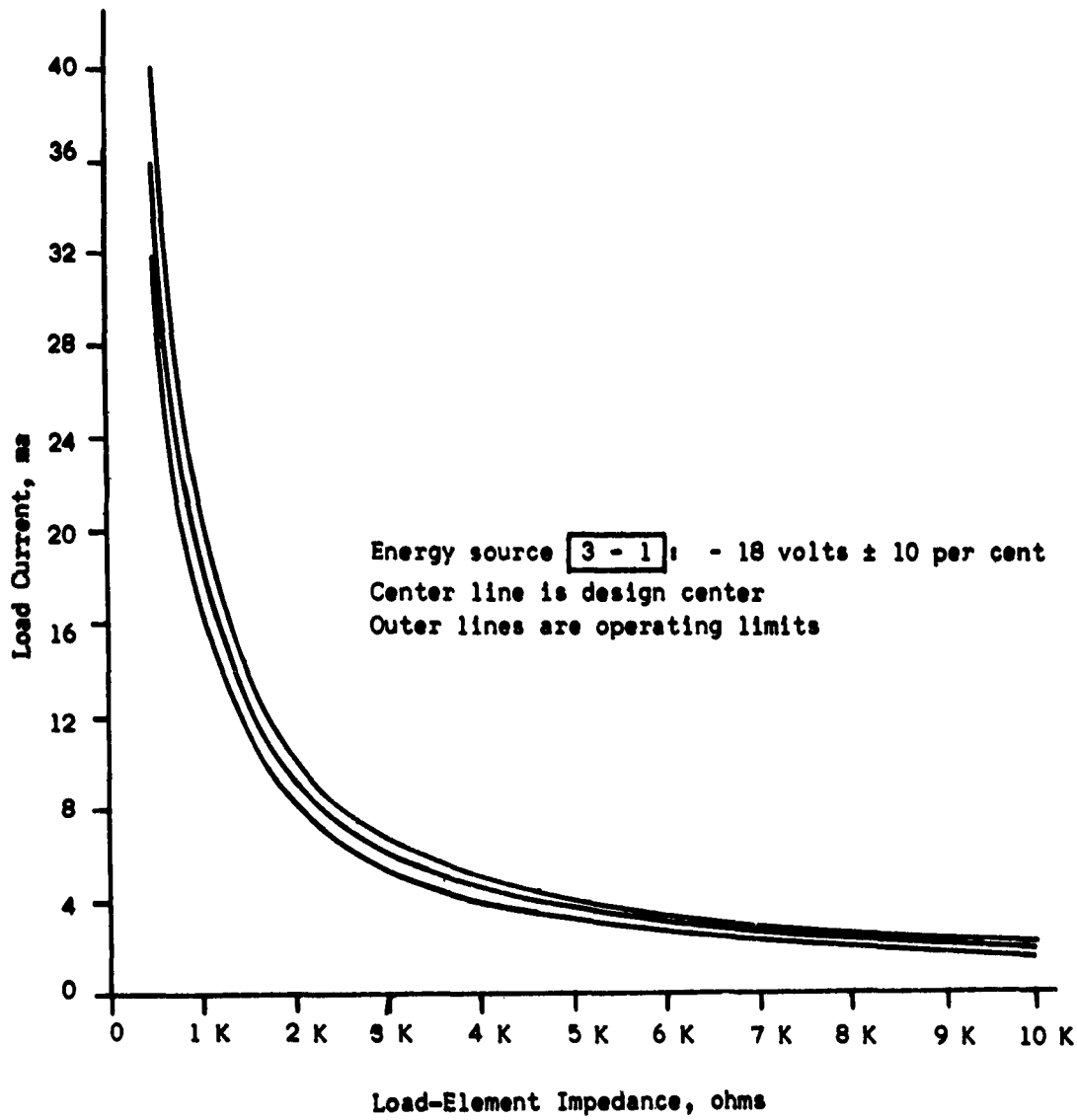
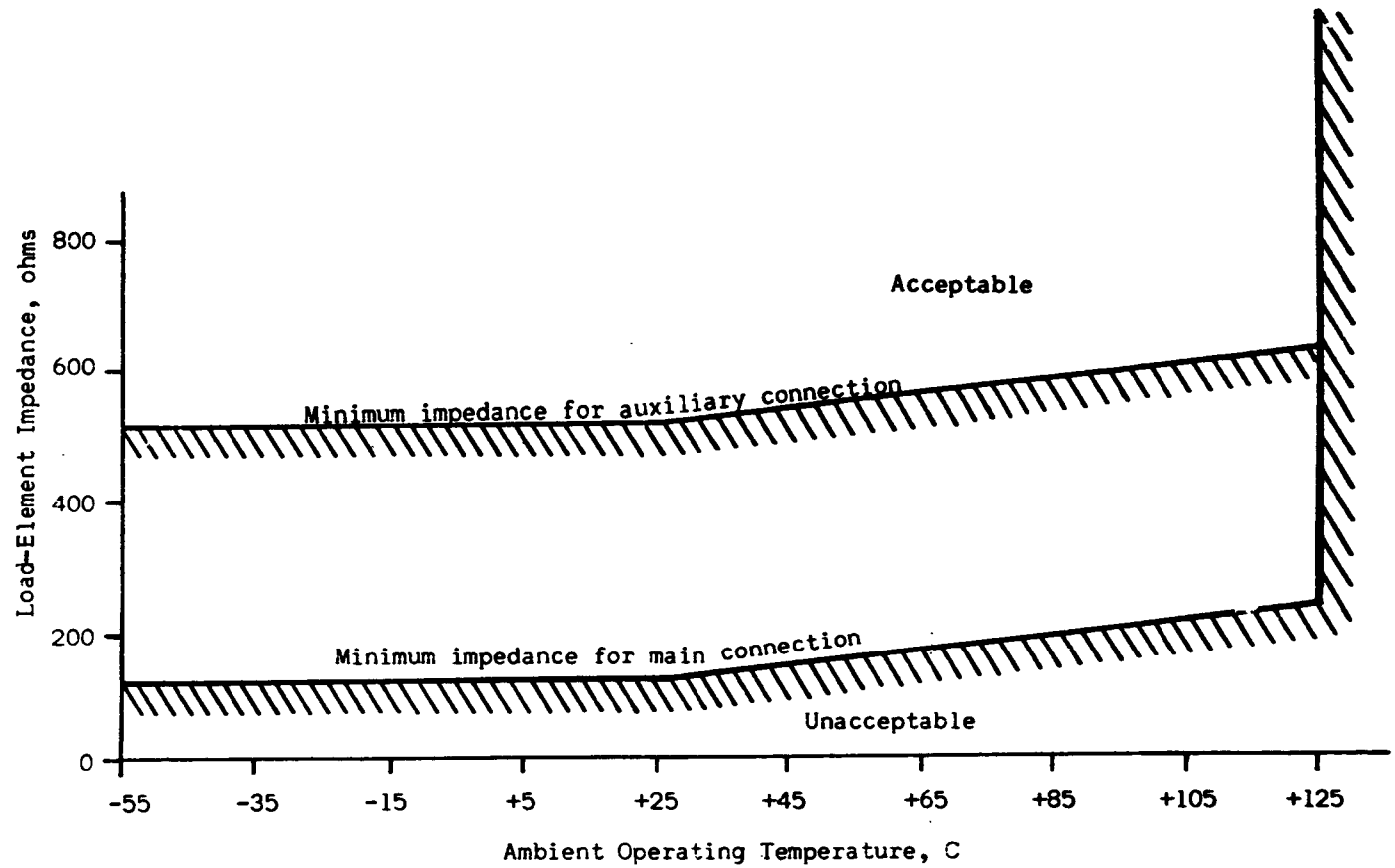



FIGURE 2. ELECTRICAL CHARACTERISTICS OF AUXILIARY OUTPUT CONNECTION




M-65

FIGURE 3. PERFORMANCE PROFILE - LOAD-ELEMENT IMPEDANCE VERSUS AMBIENT OPERATING TEMPERATURE

## 4. DESIGN CONSIDERATIONS

Should MA/27 XX be used at other than the preferred energy source voltage [3 - 1] or other than the specified negative input signal voltage [1 - 0], certain limitations are placed on the permissible load-element impedance. These limitations are displayed in the performance profiles of Figures 4 and 5. Figure 4 is a performance profile of the load-element impedance against the negative input signal voltage. Combinations of negative signal voltage and load-element impedance that yield coordinate points in the indicated failure region are not permissible. Similarly, Figure 5 is a performance profile of the load-element impedance against the energy source voltage [3 - 1]. In Figures 4 and 5, the maximum load-element impedance is not shown. It is assumed that the module will not be used to drive a load with greater impedance than three times its own input impedance under driving conditions.

Figures 3, 4, and 5 are based in part on limitations of the transistor in the prototype. Microminiaturized functions may not have as restrictive a set of limitations, and the profiles may be improved upon if such is the case.

If a function module is operated at maximum limits, this will naturally reduce reliability. This should be taken into consideration by the manufacturer.

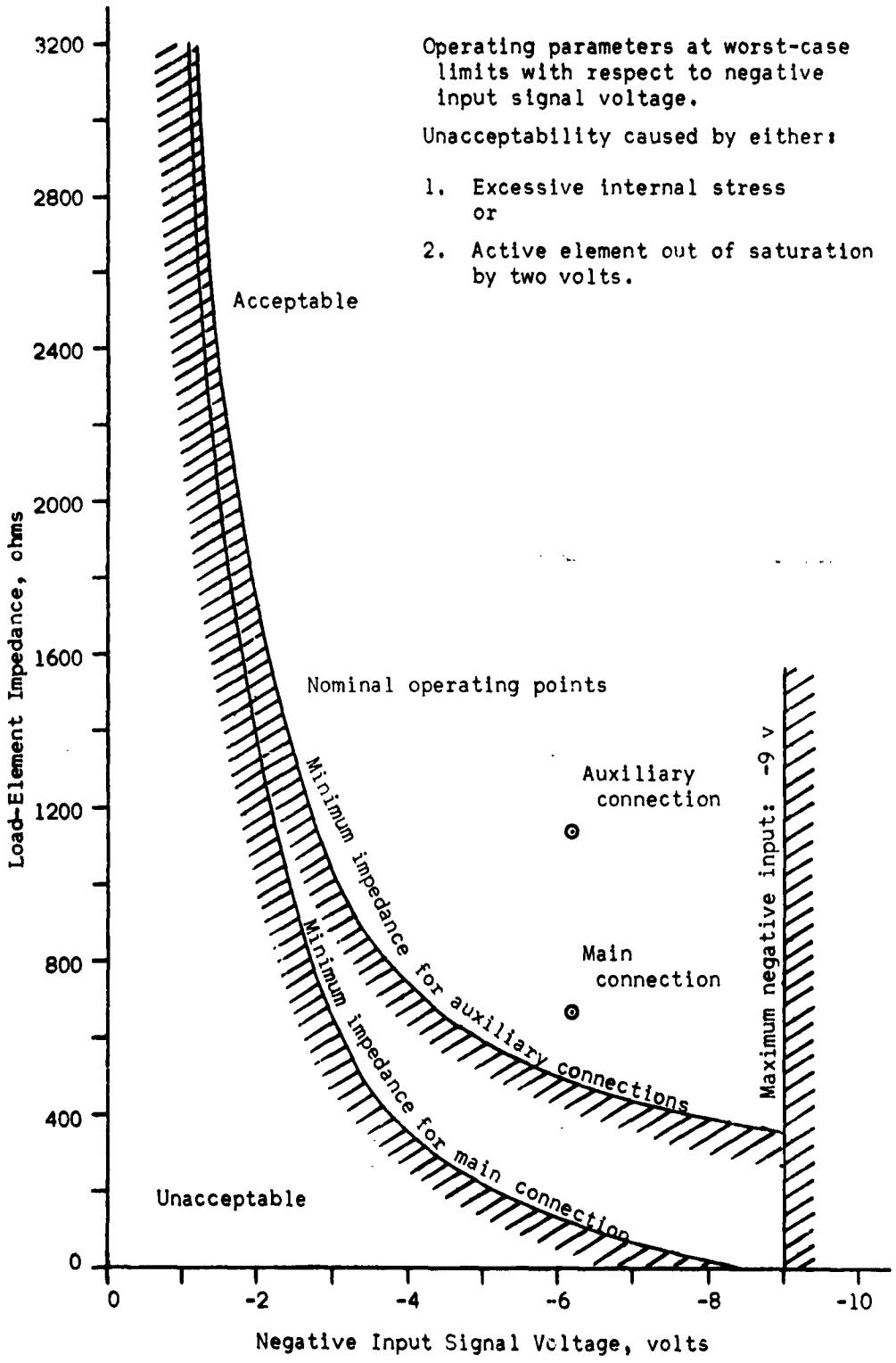



FIGURE 4. PERFORMANCE PROFILE - LOAD-ELEMENT IMPEDANCE VERSUS NEGATIVE INPUT SIGNAL VOLTAGE

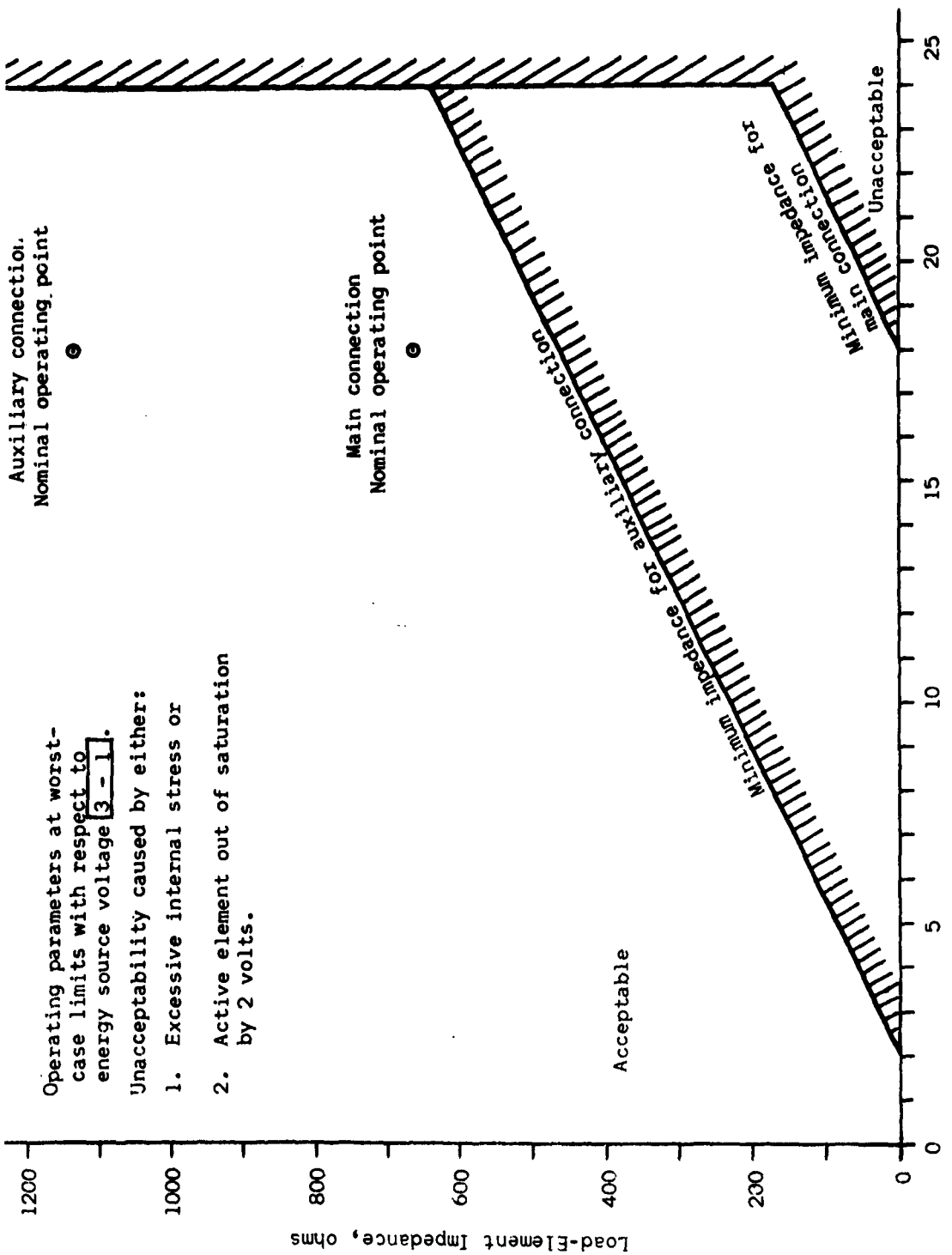
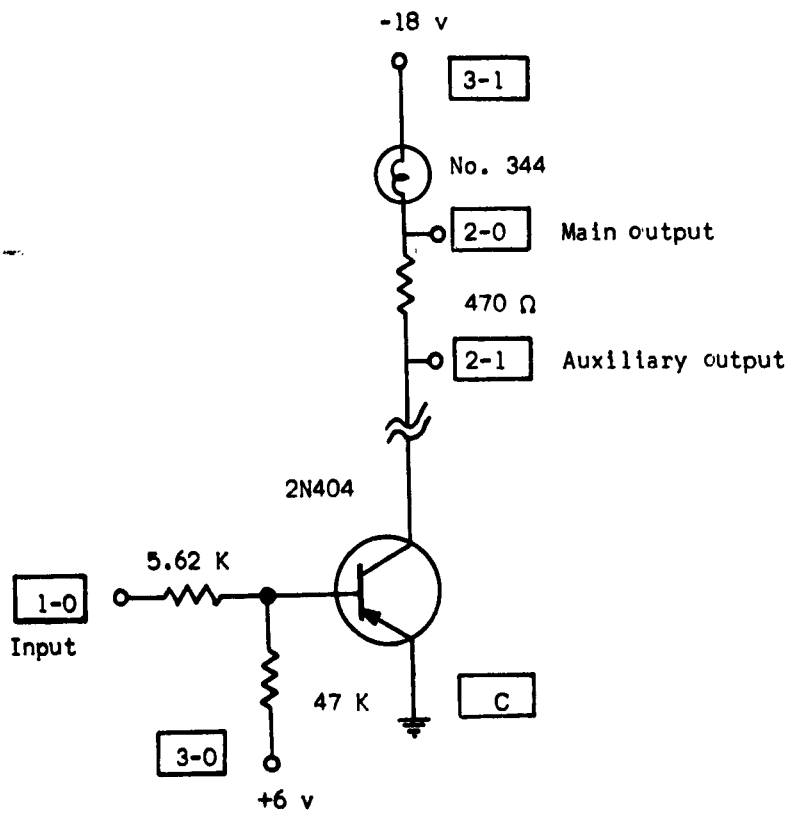



FIGURE 5. PERFORMANCE PROFILE - LOAD-ELEMENT IMPEDANCE VERSUS ENERGY SOURCE VOLTAGE 3 - 1

## 5. PROTOTYPE CIRCUIT

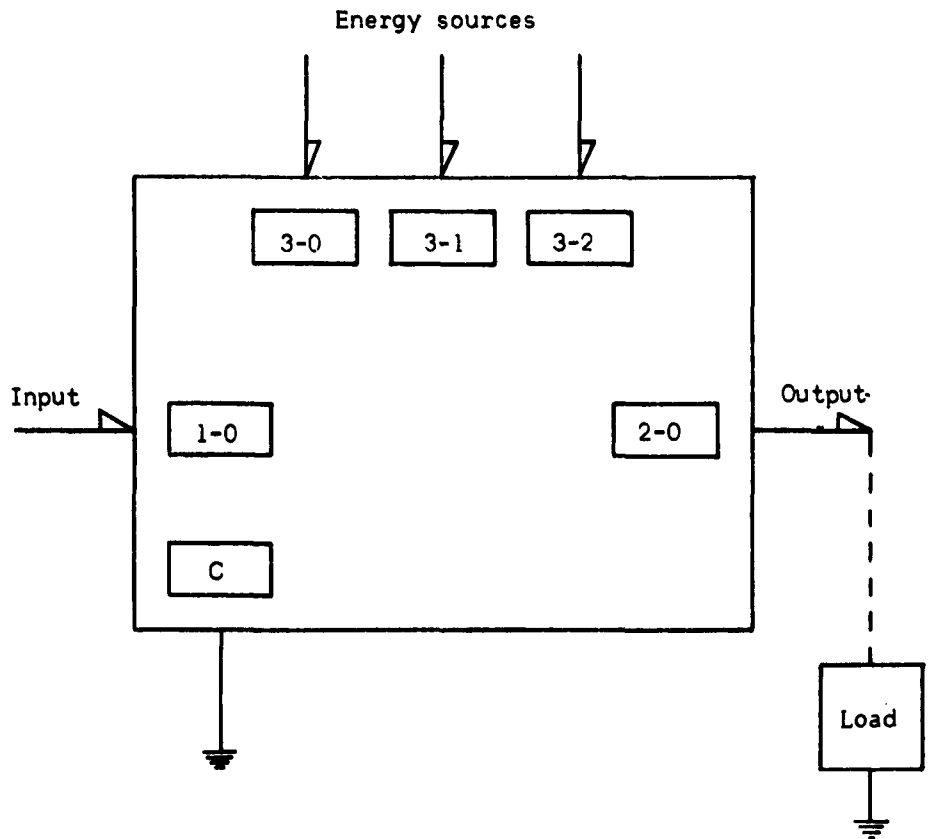
PREFERRED SEMICONDUCTOR CIRCUIT NO. 13
(Indicator)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

PREFERRED MICROELECTRONIC FUNCTION MA/29 XX

(Pulse Power Amplifier)




Prctotype: Preferred Semiconductor Circuit No. 12 (NAVWEPS 16-1-519-2)
Formerly Preferred Circuit No. 215 (NAVWEPS 16-1-519)
(See Section 5)

## 1. GENERAL

MA/29 XX is intended for use as a pulse power amplifier. Suitable inputs are nominal zero and -6-volt levels or pulses between these levels. Outputs are at nominal zero and -6-volt levels and are inverted with respect to the input. The function may be described in more detail as a controlled variable resistance which will effectively connect a load terminal at [2 - 0] to an energy source at [3 - 0] or to ground [C]. Figure 1 shows permitted input signal ranges.

The preferred energy sources are one or more of the following:

[3 - 0], -6 volts ±10% at 50 ma max

[3 - 1], -18 volts ±10% at 10 ma max

[3 - 2], +6 volts ±10% at 0.9 ma max.

In addition, any of the standard voltages in Specification NAVAIRDEVCEN E15-13A are acceptable. However, the +6-volt input at [3 - 2] in the prototype circuit is in the nature of a reference. If this voltage is changed, the input impedance and voltage ranges will be affected.

## 2. APPLICATION

MA/29 XX can be used as a level or pulse amplifier to drive low impedance loads. Suitable inputs for the function are zero and -6-volt levels and transitions between these in the form of step functions, negative 6-volt pulses, or positive 6-volt pulses with -6-volt base line. Minimum input pulse duration is 0.8 μs. Maximum transition time is 0.2 μs over the region shown in Figure 1. Input rise time longer than 0.2 μs may degrade the output response.

The controlled low resistance state is less than 10 ohms and the high resistance is greater than 60,000 ohms for all ambient temperatures between -55 and +125 C. The input voltage and controlled resistance relationship is shown in Table 1.

TABLE 1. INPUT LOGIC FOR MA/29 XX

| Input Signal Voltage[(a)] | Output State | Terminal Pairs 3 - 0 to 2 - 0 | Terminal Pairs 2 - 0 to C |
|---|---|---|---|
| Ground | On | Low resistance | High resistance |
| Negative | Open circuit | High resistance | Low resistance |

(a) See Figure 1 for input voltage ranges.

## 3. PERFORMANCE

Parameter limits under nominal operating conditions are summarized in Table 2. For this table, the energy source voltage [3 - 0] is -6 volts.

TABLE 2. PARAMETER LIMITS

| Parameter | Minimum | Fifth Percentile | Design Center | Ninety-fifth Percentile | Maximum |
|---|---|---|---|---|---|
| Input levels at [1 - 0]:(a) | | | | | |
| Nominal zero | -0.5 v | | -0.15 v | | +1? v |
| Nominal -6 v | -5.6 v | | -6.2 v | | -6.8 v |
| Input pulse duration: (Measured at half amplitude) | 0.8 μs | | | | |
| Input impedance(b) (pulse input) | | | 4 "G" loads(c) | | |
| Controlled resistance between terminals [3 - 0] and [2 - 0]: | | | | | |
| Input = -6 v | 60 KΩ | 100 KΩ | 250 KΩ | | |
| Input = 0 v | | | 5 Ω | 10 Ω | 15 Ω |
| Controlled resistance between terminals [2 - 0] and [C]: | | | | | |
| Input = -6 v | | | 5 Ω | 10 Ω | 15 Ω |
| Input = 0 v | 60 KΩ | 100 KΩ | 250 KΩ | | |
| Output transition turn-on time(d) | | | | | 0.4 μs |
| Output transition turn-on time(d) | | | | | 0.7 μs |

(a) See Figure 1.

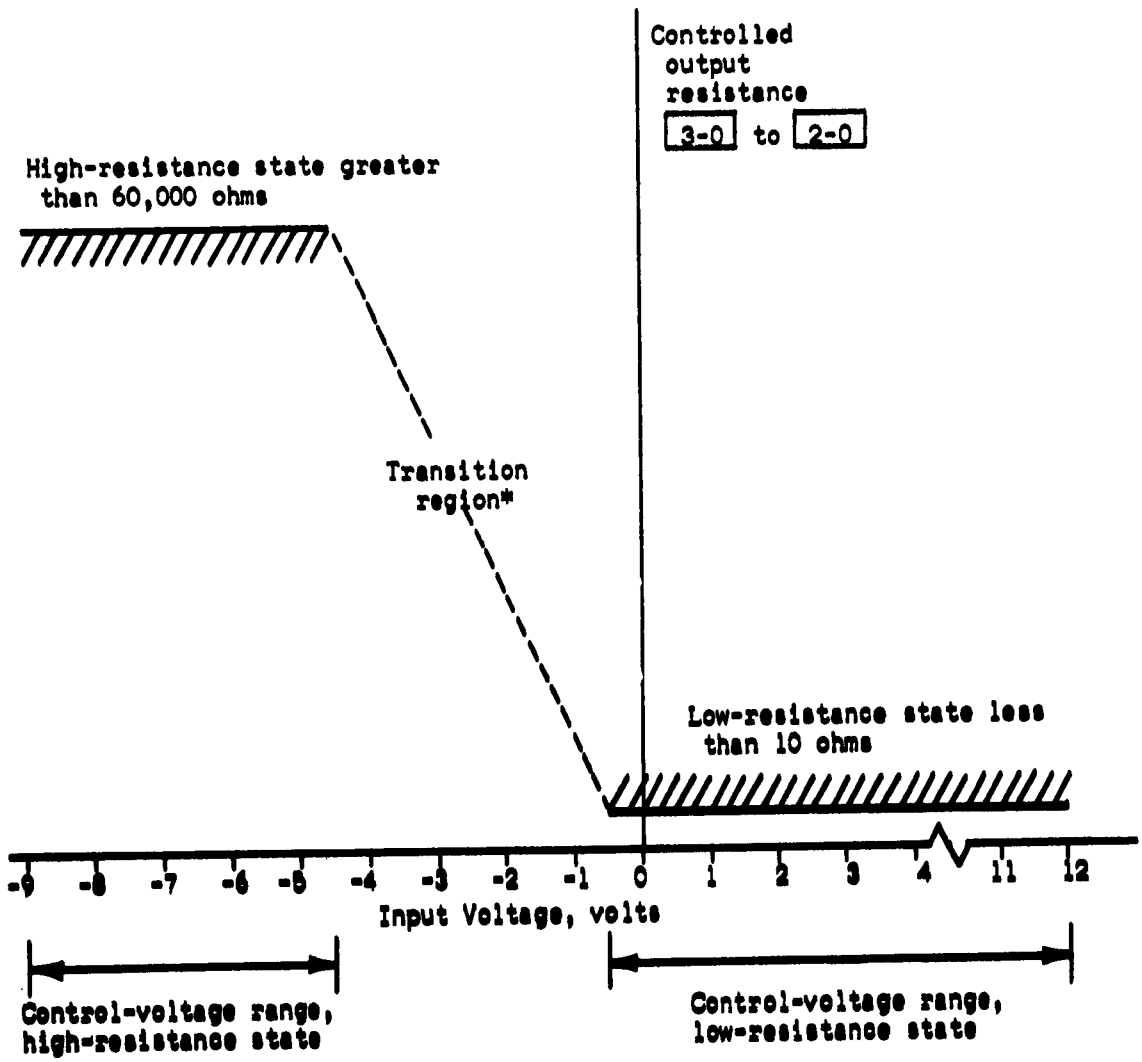
(b) See Figure 4 for d-c input characteristics.

(c) One "G" load is defined as 5,620 ohms paralleled with 180 pf.

(d) Output transition times are functions of output loading and input rise times. Input rise times used here are less than 0.3 μs. See Figures 5 to 8 for transition times under varying loads.

Figure 2 shows maximum permitted voltage across, maximum permitted current through, and maximum permitted power in the controlled resistance, as well as high- and low-resistance operating regions. Figure 1 indicates module transfer characteristics with input voltage ranges indicated. D-C input characteristics are shown in Figure 4. Transition time variation with loading is given in Figures 5 to 8. The energy source at terminal [3 - 0] is maintained at -6 volts for these figures.

The maximum heat dissipation in the controlled resistance (terminals [3 - 0] to [2 - 0]) at 25 C is 120 mw, and 50 mw at 125 C. The total heat dissipation in the module is 220 mw and 120 mw, respectively.




* Input voltage transition times in excess of 0.2 μs may degrade output transition times.

FIGURE 1. TRANSFER CHARACTERISTICS

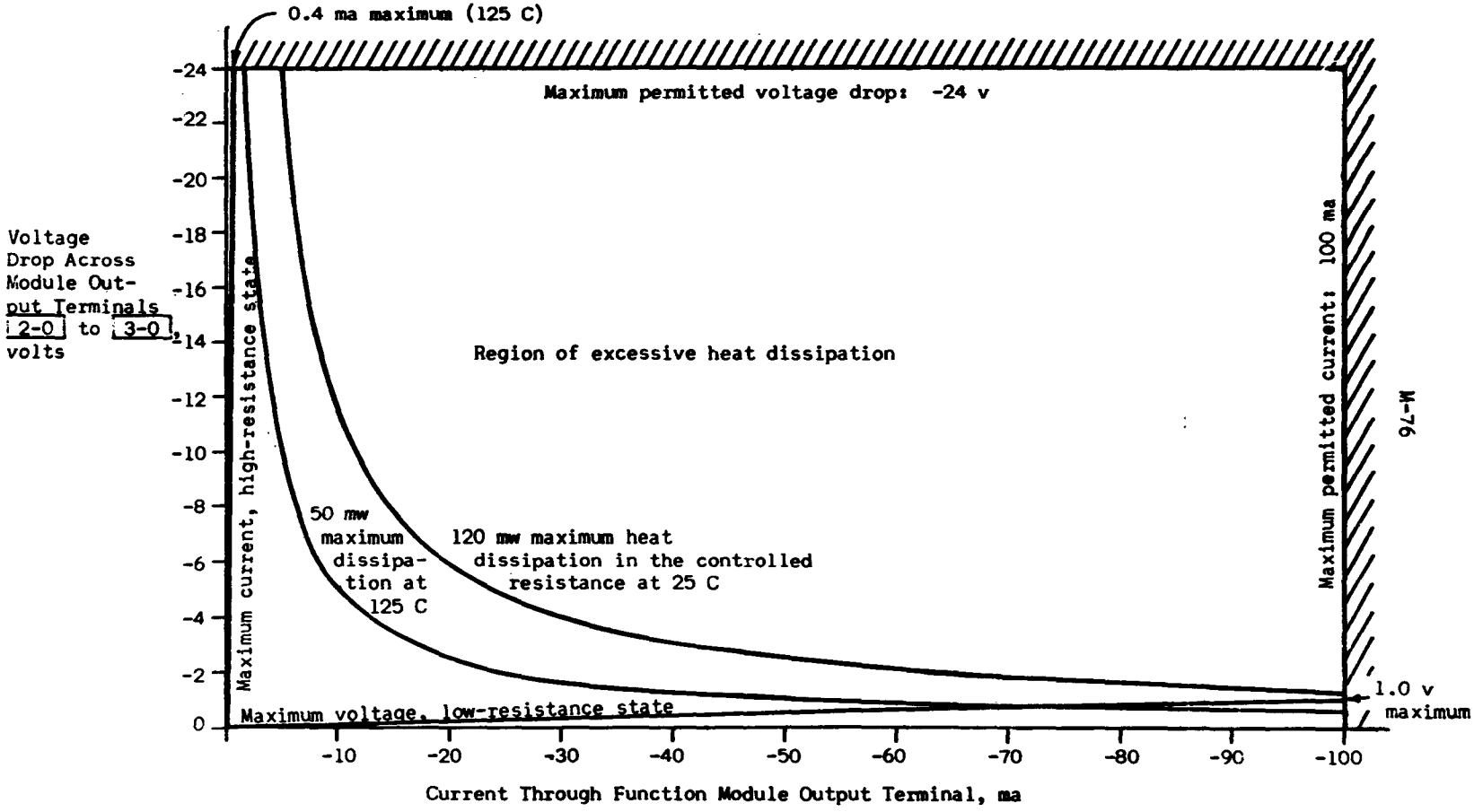



FIGURE 2. OUTPUT CHARACTERISTICS, TERMINALS 3 - 0 to 2 - 0

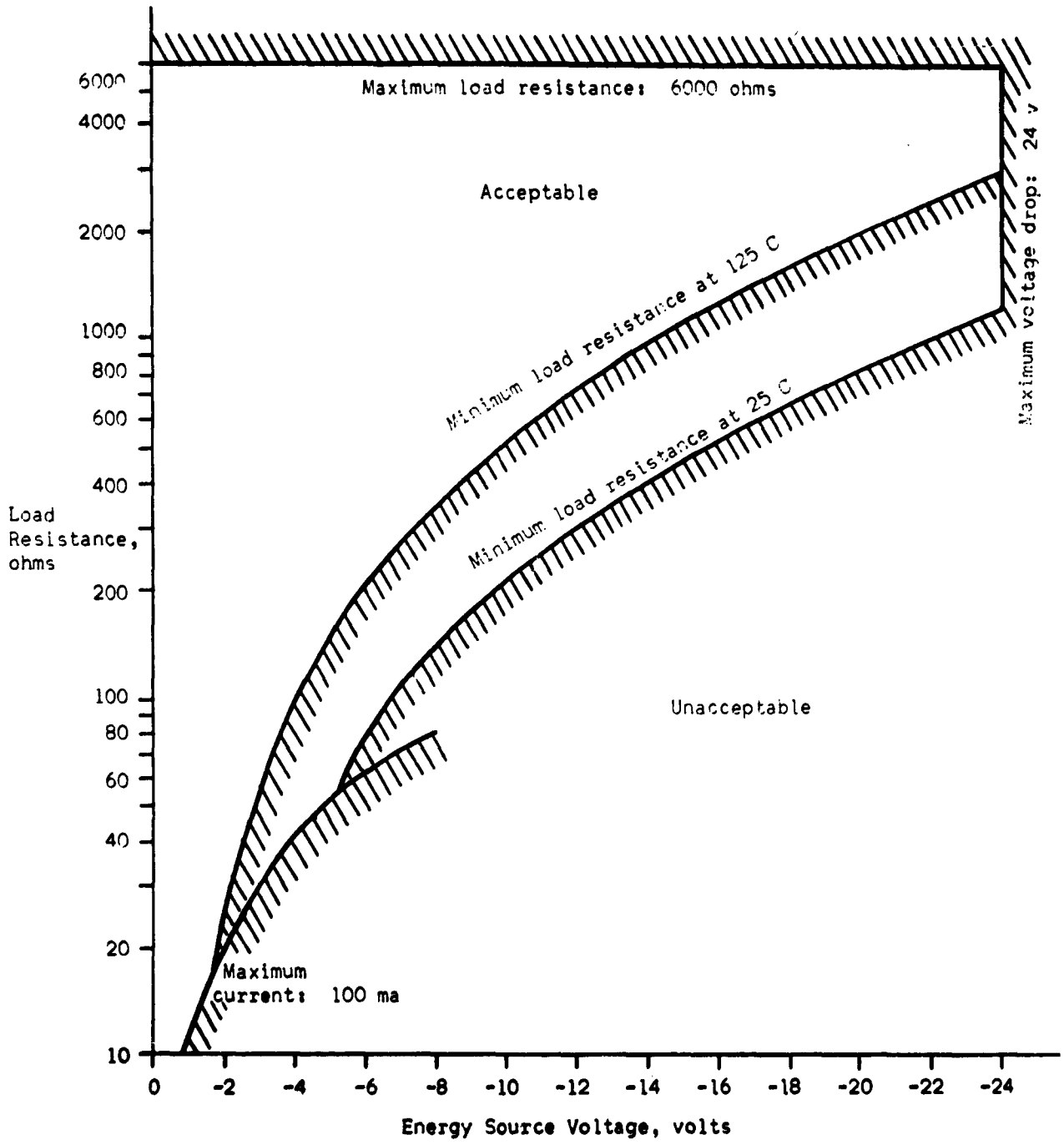



FIGURE 3. LOAD RESISTANCE PERFORMANCE PROFILE

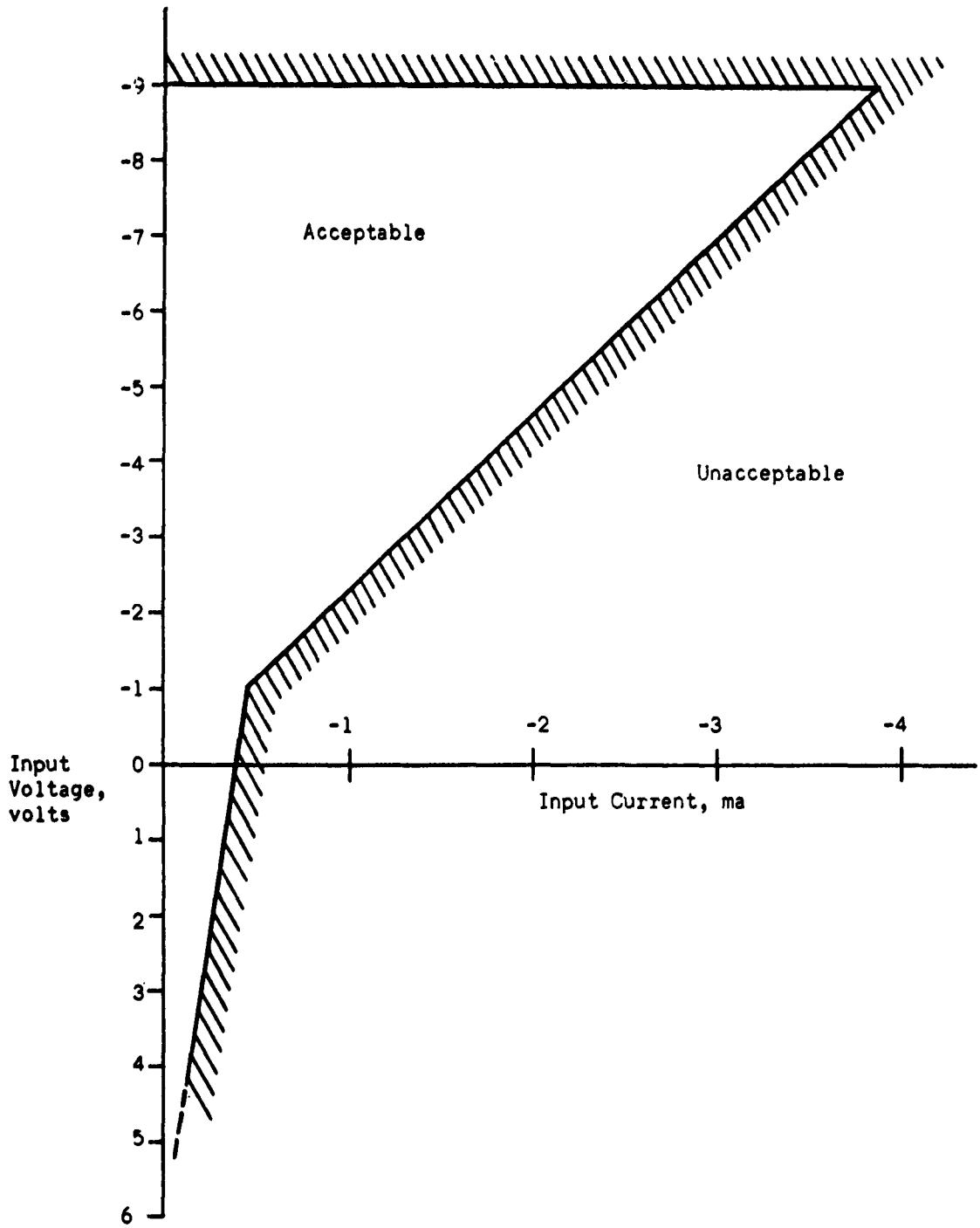



FIGURE 4. INPUT RESISTANCE CHART

OUTPUT WAVEFORM TIMING

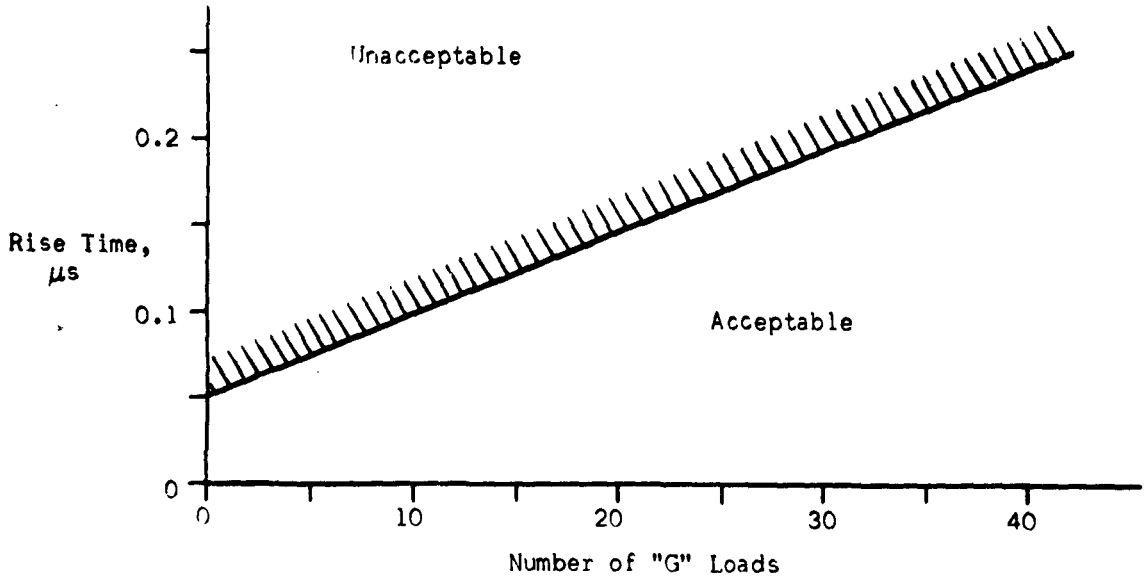



FIGURE 5. RISE TIME VERSUS LOADING (negative going waveform)

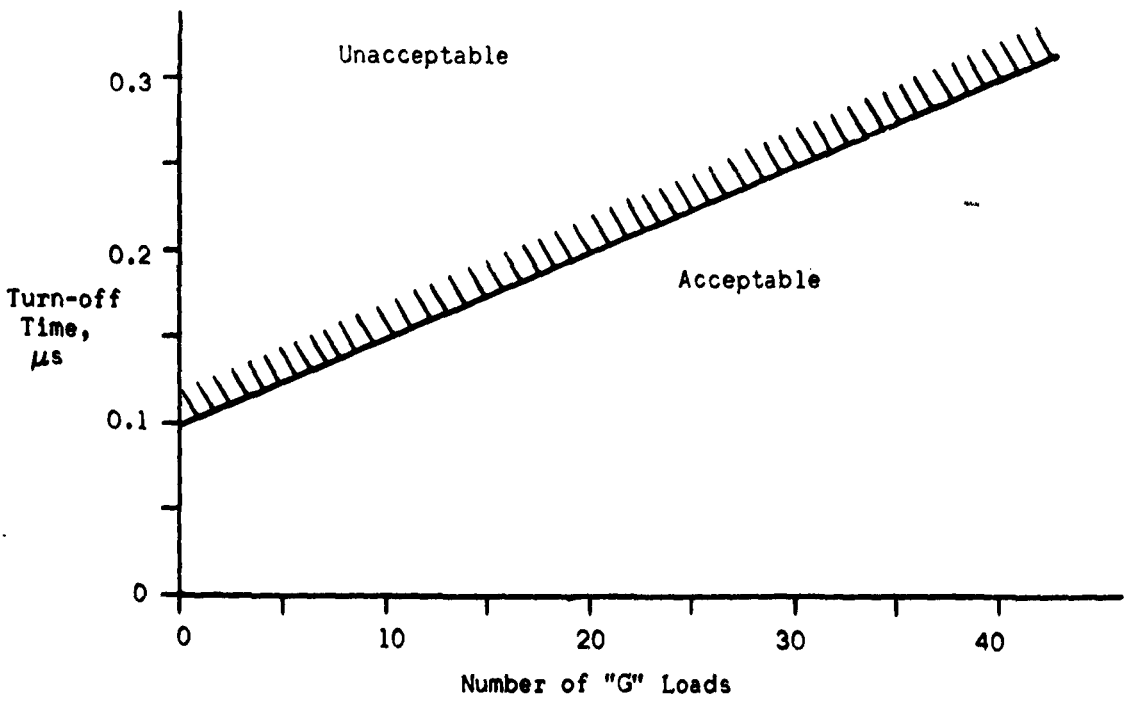



FIGURE 6. TURN-OFF TIME VERSUS LOADING (negative going waveform)

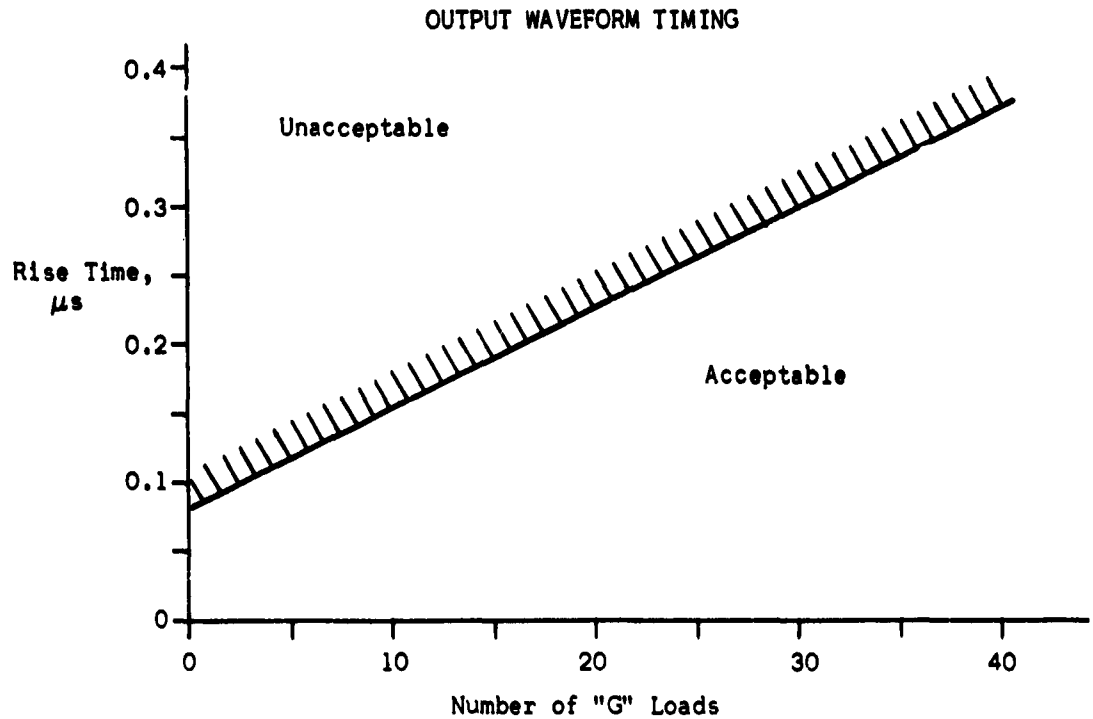



FIGURE 7. RISE TIME VERSUS LOADING (positive going waveform)

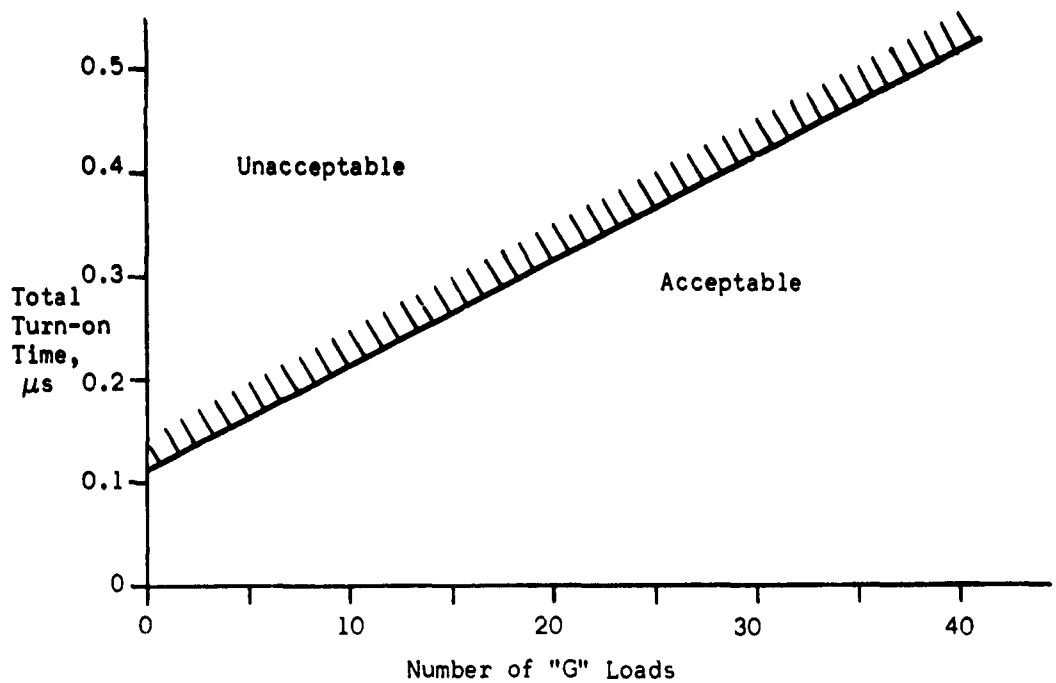



FIGURE 8. TURN-ON TIME VERSUS LOADING (positive going waveform)

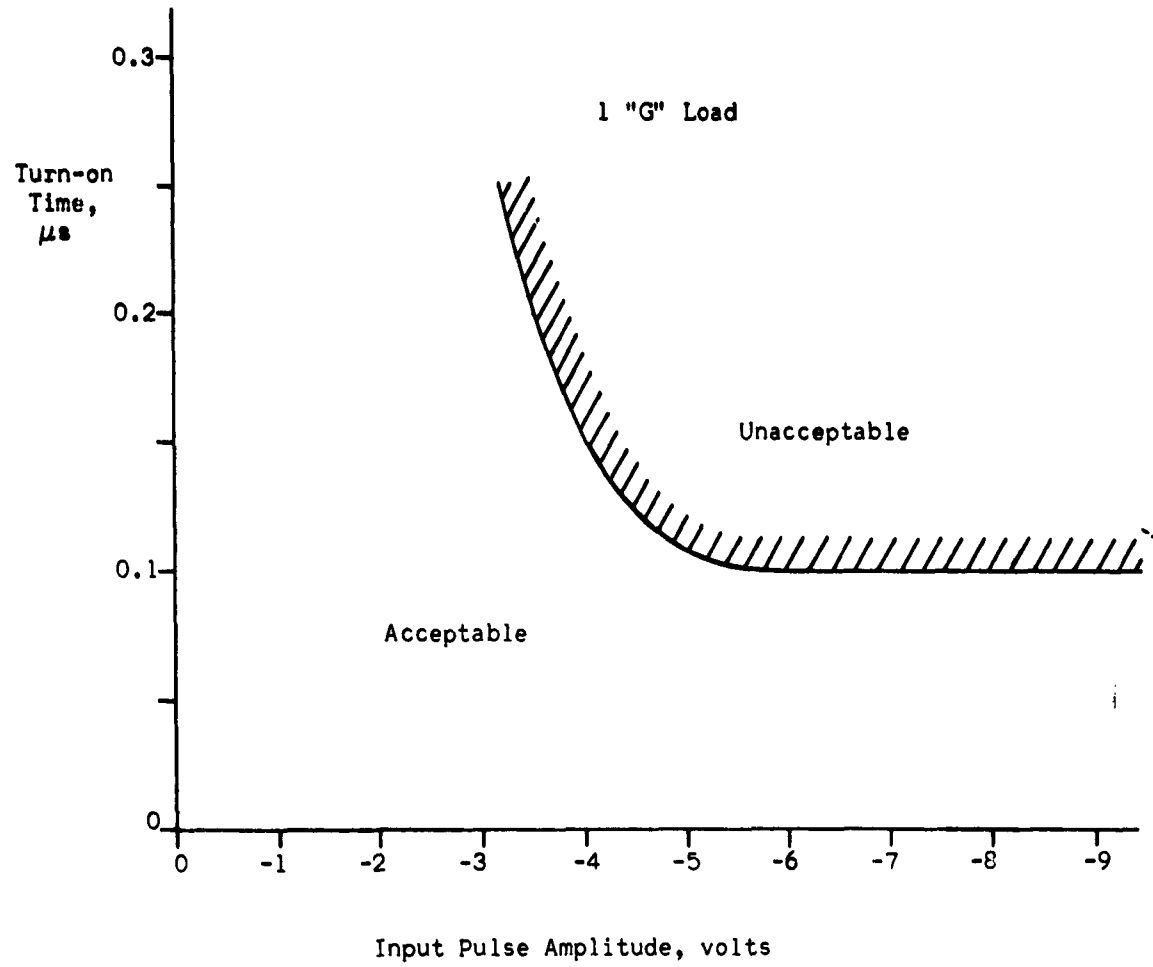



FIGURE 9. TURN-ON TIME VERSUS INPUT VOLTAGE

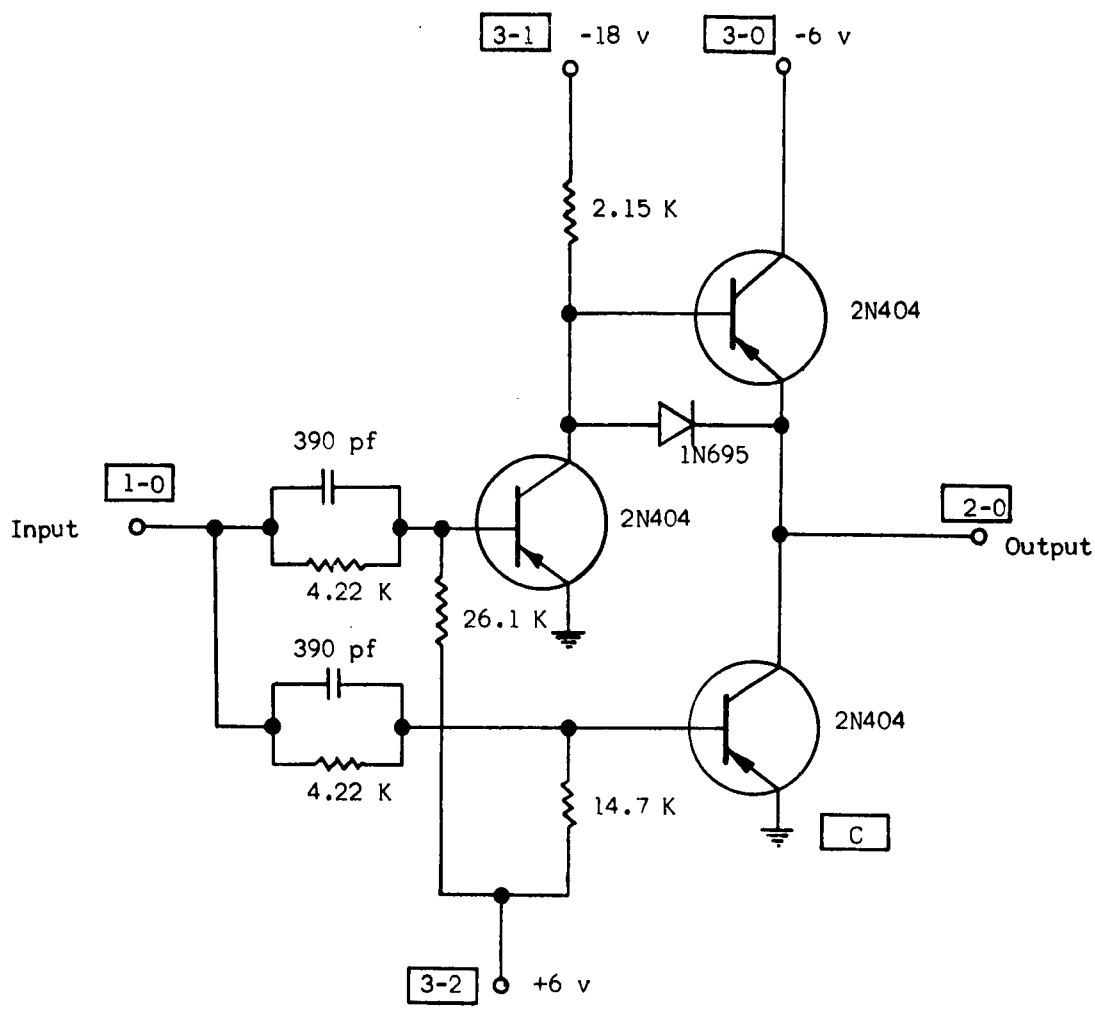
## 4. DESIGN CONSIDERATIONS

When MA/29 XX is used with other than nominal energy source voltage at terminal [3 - 0], Figures 2 and 3 show performance and limitations. Figure 2 shows MA/29 XX output characteristics and permissible voltages and current loads. Performance with resistive loads can be obtained from this graph. For any d-c load resistance, a conventional load line can be drawn terminating on the axes of the graph. The intersection of the load line with the high-resistance state line and with the low-resistance state line will show worst case off and on conditions, respectively. If the load line happens to pass through the region of excessive heat dissipation, switching transition times must be restricted and the frequency of transitions must be limited. Note also that operation at a temperature of 125 C will place a limit of 73 ma on the load current.

## 5. PROTOTYPE CIRCUIT

PREFERRED SEMICONDUCTOR CIRCUIT NO. 12

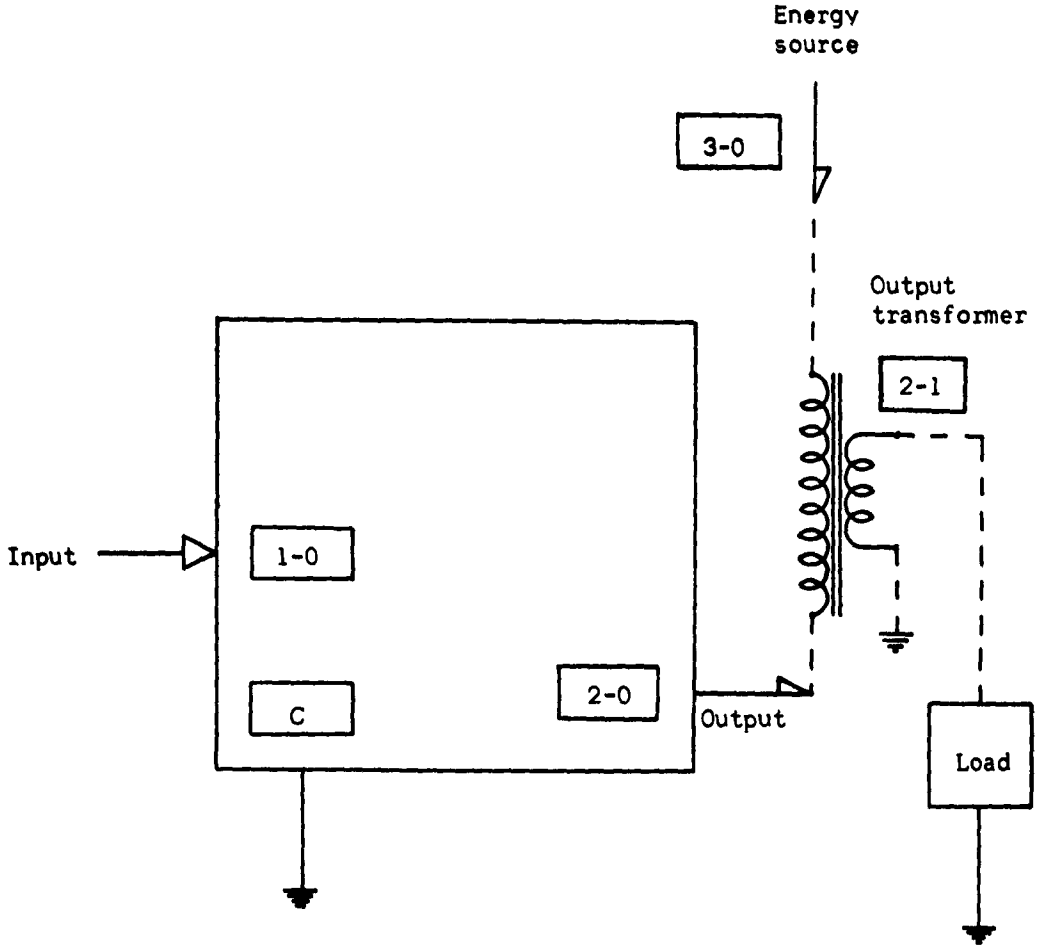
(Pulse Power Amplifier)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

PREFERRED MICROELECTRONIC FUNCTION MA/29 XXX

(Audio Driver, 150 mw)




**Prototype:** Preferred Semiconductor Circuit No. 24 (NAVWEPS 16-1-519-2) (See Section 5)

1. GENERAL

MA/29 XXX is a medium-power audio amplifier intended to deliver 150 mw of audio signal. It can be used with the preamplifier MA/03 XX (PSC 23). With a suitable output transformer, it can be used to drive a push-pull power amplifier, earphones, loudspeaker, or a similar load.

The preferred energy source is:

3 - 0, +25 volts ± 10 per cent at 35 ma max.

In addition, any of the standard voltages in Specification NAVAIRDEVCEN EL5-13A are acceptable.

## 2. APPLICATION

MA/29 XXX will provide a nominal 18 db of power gain in the audio-frequency region from 60 to 30,000 cycles per second, with inputs up to 1 vac rms. Inputs with a d-c component will reduce the usable range of undistorted output. Normally an output transformer such as the UTC H-27 will be required for d-c isolation and to match the module output impedance of 500 to 1000 ohms to a load impedance.

## 3. PERFORMANCE

Some parameter limits are summarized in Table 1. Unless otherwise noted, the operating conditions are: temperature range, -55 to +125 C; frequency range, 60 to 30,000 cycles; output transformer, UTC H-27. These parameter limits are modified and extended by Figures 1 to 6. Figure 7 shows the frequency response for a constant 1 vac input signal.

TABLE 1. BASIC FUNCTION PERFORMANCE RANGES

| Parameter | Minimum | Fifth Percentile | Design Center | Maximum |
|---|---|---|---|---|
| Input impedance | 500 ohms | 550 ohms | 650 ohms | - |
| Power gain | 18 db(a) | - | 20 db(a) | - |
| Output distortion for 0.8-volt a-c rms input(b) | - | - | - | 2% |
| Output distortion for 1.0-volt a-c rms input(b) | - | - | - | 5% |
| Output distortion for 1.2-volt a-c rms input(b) | - | - | - | 10% |
| Load impedance(c) | - | - | 16 ohms | - |

(a) Modification of this figure may be necessary according to the characteristics of the transformer used and the ambient temperature range expected. Then Figures 1 and 2 apply.

(b) See Figures 3 to 5 for permissible modifications under extreme conditions.

(c) Load impedance is specified as 16 ohms using the UTC H-27 transformer. If a higher impedance load is used, the permissible input-voltage range must be reduced in direct proportion to avoid a corresponding increase in distortion. If a lower impedance load is used, there is a corresponding reduction in available power output.

Minimum power gain for MA/29 XXX is 18 db with less than 2 per cent distortion between 60 cycles and 30 kc, with a 16 ohm load, and for the temperature range -55 to +125 C except as shown by Figures 1 and 2. Limiting input signals for Figures 1 and 2 can be obtained from the corresponding distortion lines in Figure 3.

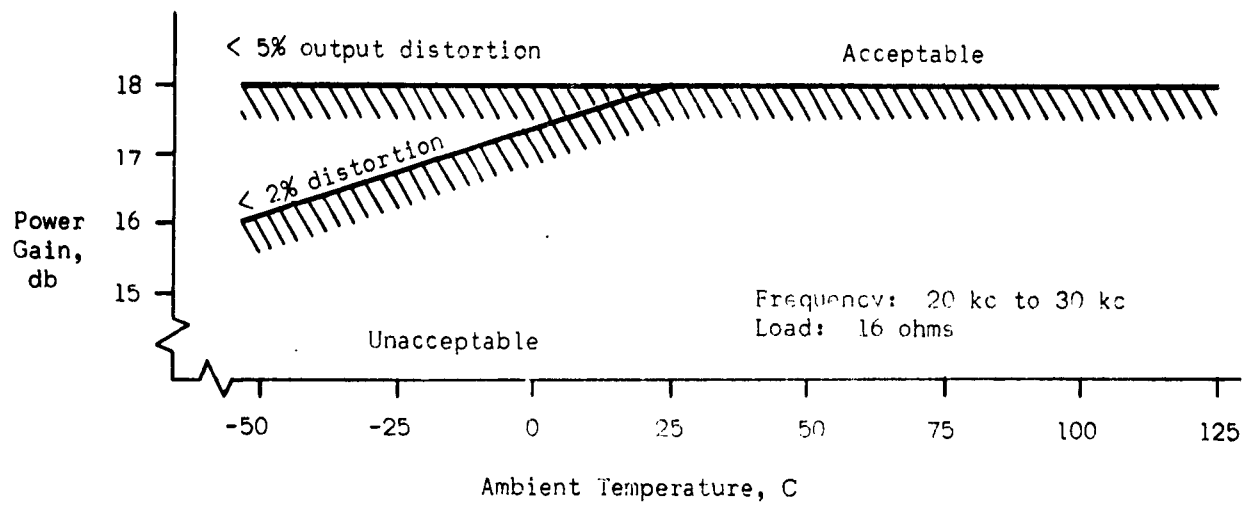



FIGURE 1. MINIMUM POWER GAIN

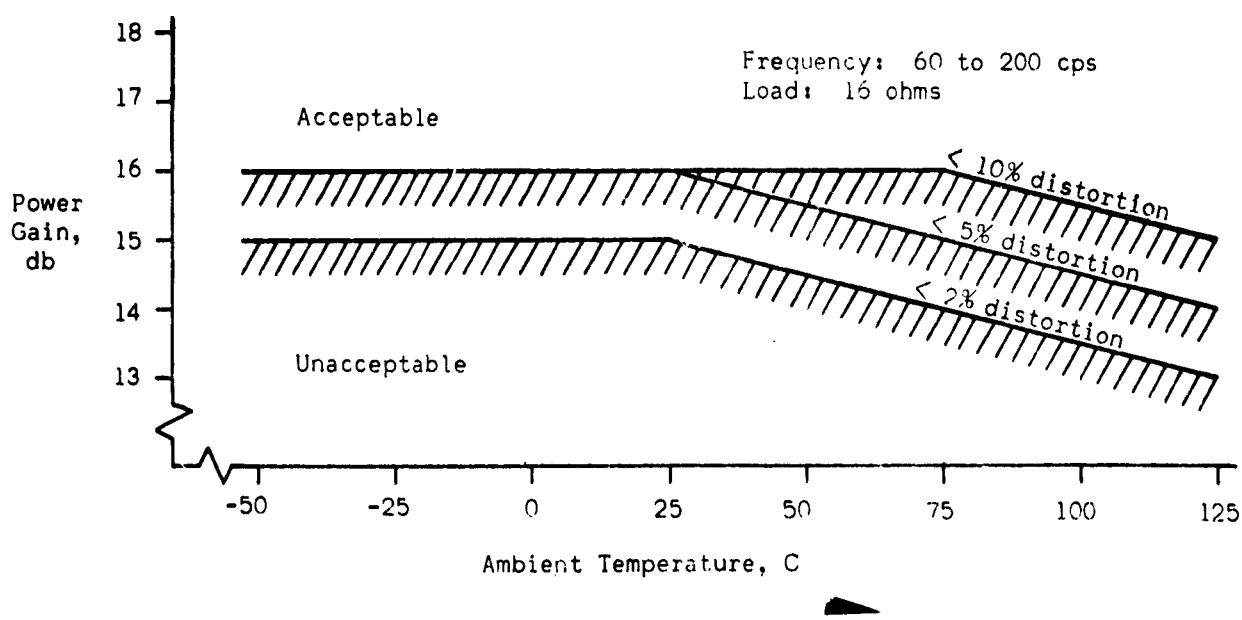



FIGURE 2. MINIMUM POWER GAI

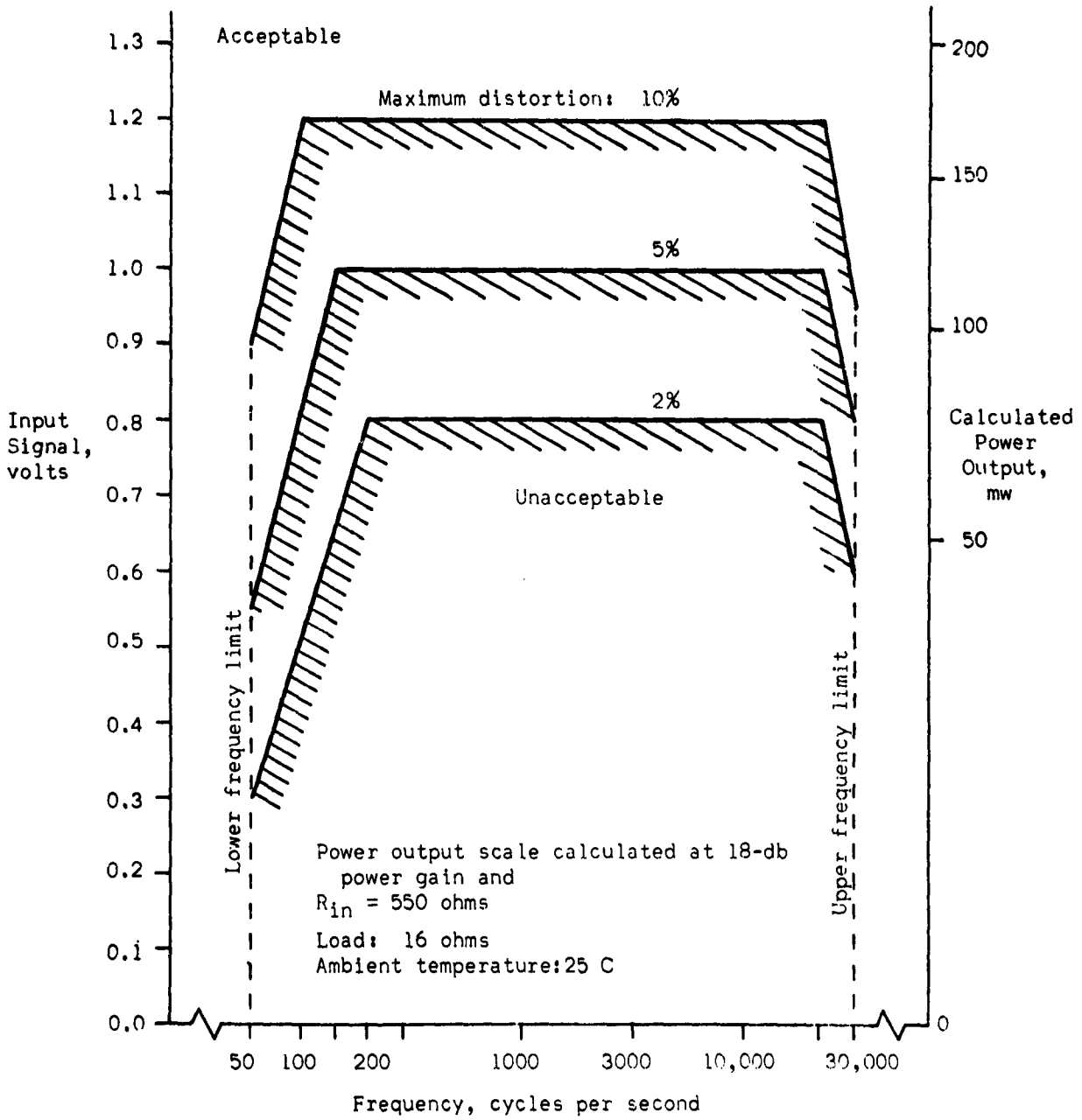



FIGURE 3. PERFORMANCE PROFILE--MINIMUM INPUT SIGNAL LEVEL VERSUS FREQUENCY FOR CERTAIN OUTPUT DISTORTION LEVELS

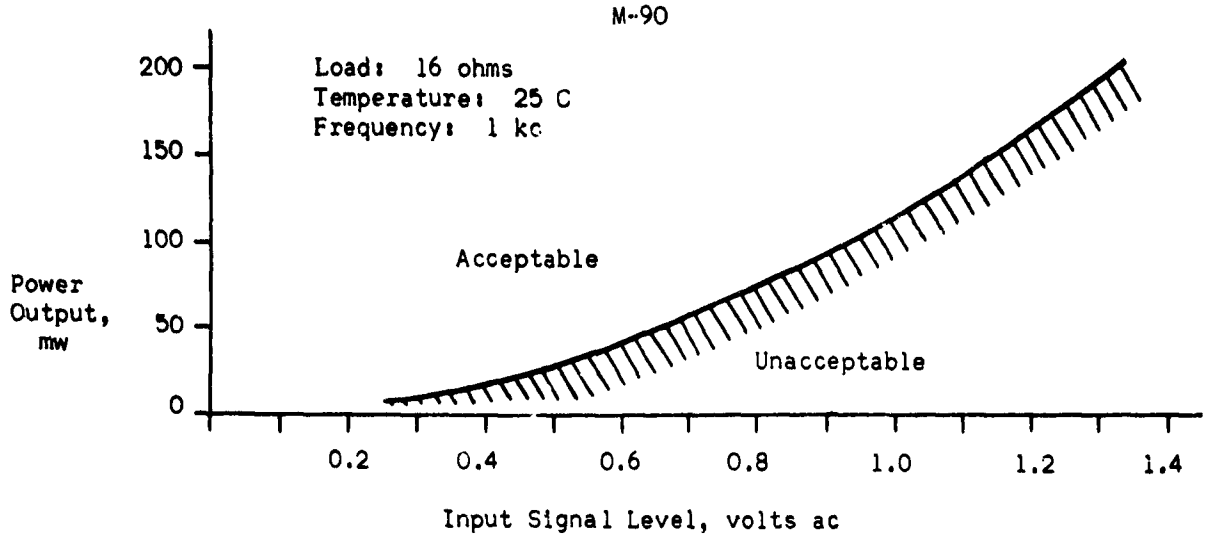



FIGURE 4. MINIMUM ACCEPTABLE POWER OUTPUT VERSUS INPUT SIGNAL LEVEL

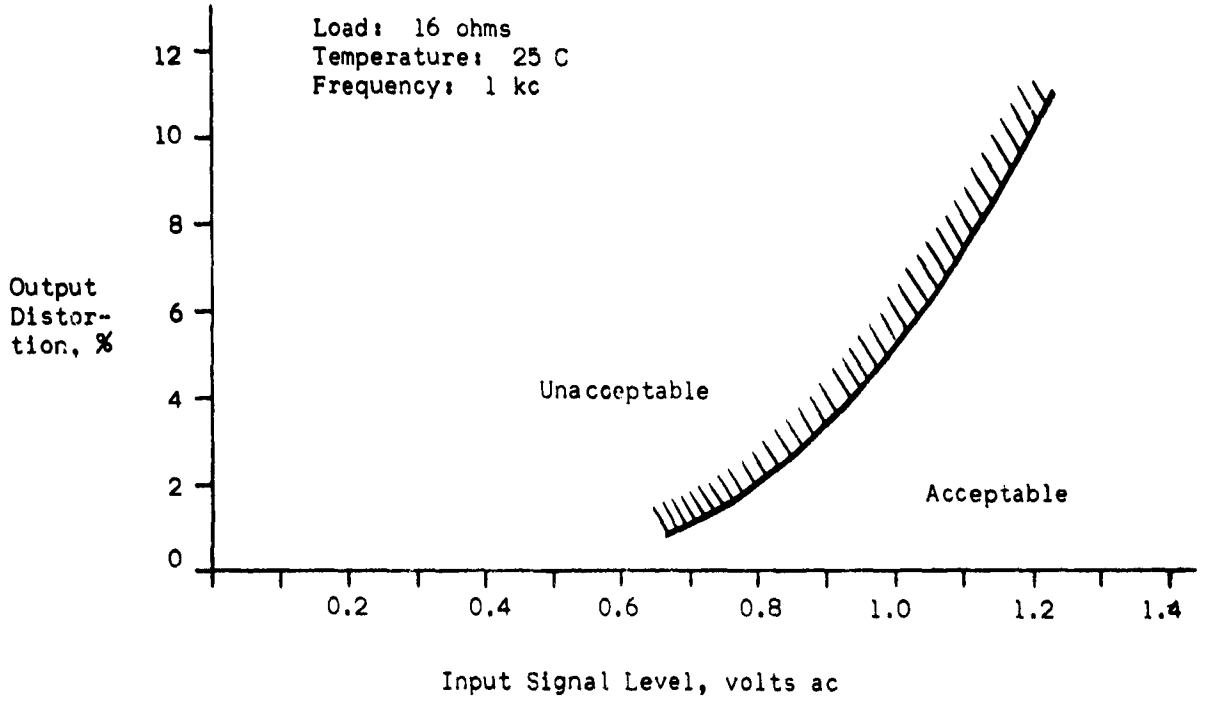



FIGURE 5. MAXIMUM ACCEPTABLE OUTPUT DISTORTION VERSUS INPUT SIGNAL LEVEL

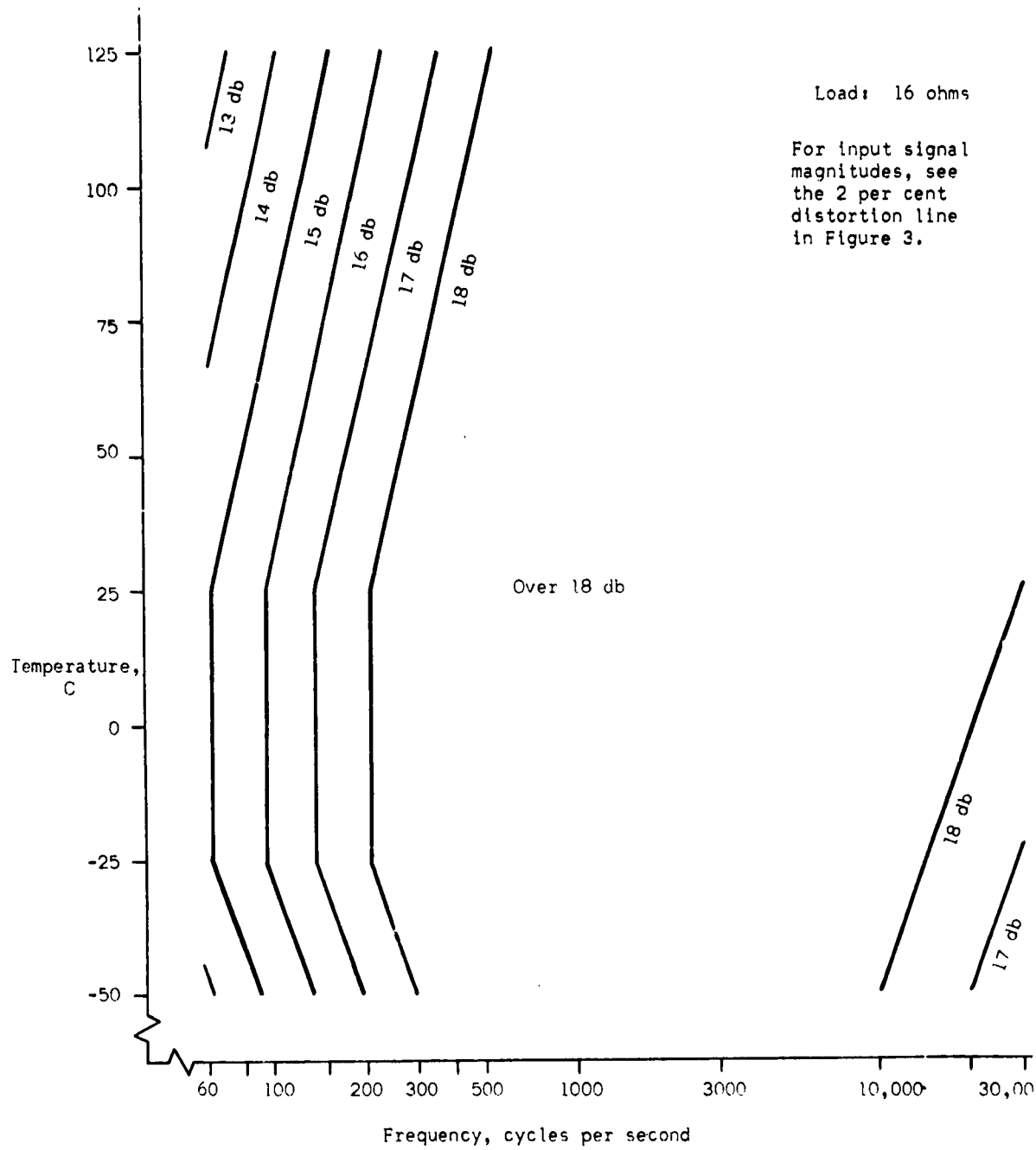



FIGURE 6. PERFORMANCE PROFILE--MINIMUM ACCEPTABLE POWER GAIN AS A FUNCTION OF TEMPERATURE AND FREQUENCY

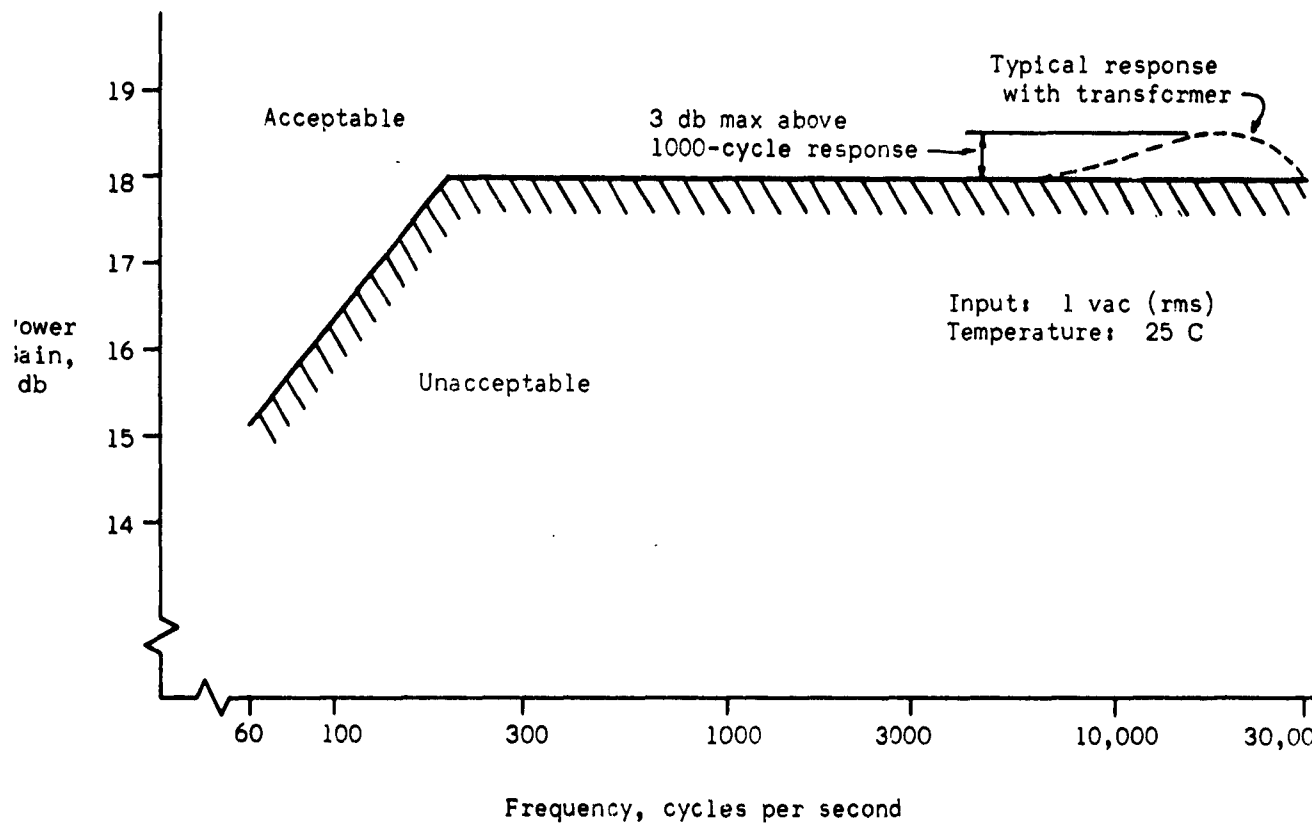



FIGURE 7. MINIMUM FREQUENCY RESPONSE

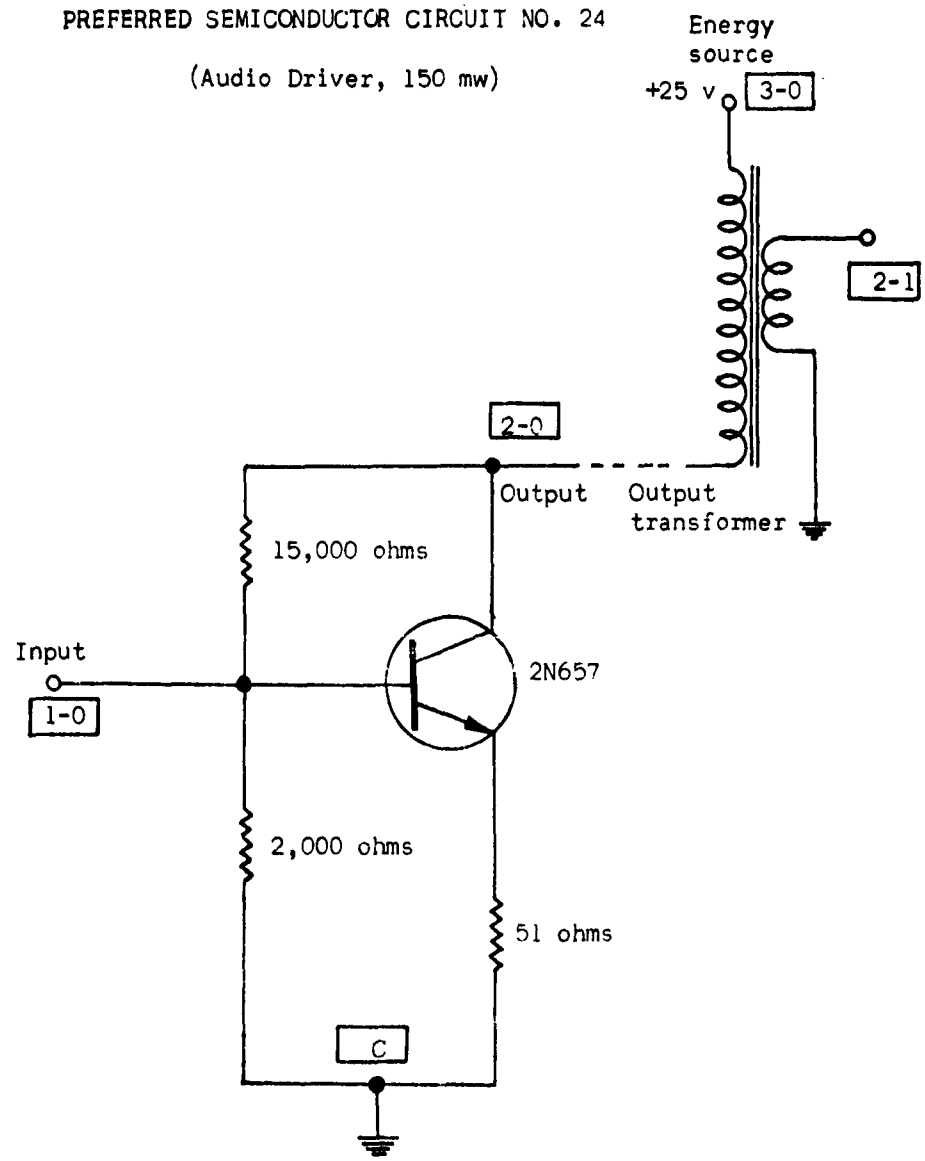
## 4. DESIGN CONSIDERATIONS

Microminiaturization of the prototype POC 24 is severely handicapped by the output transformer. A module based on a redesign of the circuit to eliminate the transformer would be desirable. The characteristics outlined in this module description are largely a function of the transformer chosen, and must be modified with other transformers. The size and weight of the transformer can be reduced with some sacrifice in bandwidth. The acceptability of this will depend upon the end use.

## 5. PROTOTYPE CIRCUIT

PREFERRED SEMICONDUCTOR CIRCUIT NO. 24

(Audio Driver, 150 mw)




Note: The prototype circuit is included for reference purposes and should not be considered restrictive as to design approach.

U.S. Naval Air Development Center, Johnsville, Pa. Aeronautical Electronic and Electrical Laboratory

μ-NOTES NO. 3; INFORMATION ON MICROELECTRONICS FOR NAVY AVIONICS EQUIPMENT; by H. B. Martin; 5 Jun 1963; 125 pp and appendix A; Report No. NADC-EL-6319; WEPTASK No. RAV03J002/2021/R008-03-01, Problem No. 14.

This μ-NOTES details the evaluation of Signetics Corporation microelectronic units SE100T, SE120T, SE130T, SE140T, and SE200T; Pacific Semiconductors, Incorporated, units PCF-101, PCG-101, PCH-101, and PCR-101; and the Radio Corporation of America DMC-100 unit. The initial effort of the contractor (Battelle Memorial Institute) in the preparation of functional descriptions for microelectronic assemblies is included as appendix A.

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I. Martin, H. B.

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REPORT NO. NADC-EL-6319

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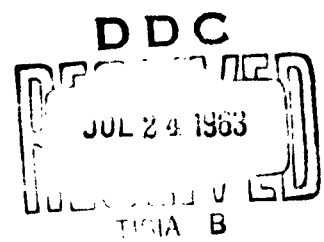
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