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LANSDALE DIVISION
Lansdale, Pennsylvania

PHILCO CORPORATION
LANSDALE DIVISION
Lansdale, Pennsylvania

PEM for
TRANSISTOR MANUFACTURING
PROCESS IMPROVEMENT
Fourth Quarterly Progress Report
1 February 1963 to 30 April 1963
Contract No. DA-36-039-SC-86720
Placed by USAEMA, Philadelphia, Pa.

Philco Project No. R-232.1

**PHILCO CORPORATION
LANSDALE DIVISION
Lansdale, Pennsylvania**

**PEM for
TRANSISTOR MANUFACTURING
PROCESS IMPROVEMENT**

Fourth Quarterly Progress Report

Period Covered:

1 February 1963 to 30 April 1963

Contract No. DA-36-039-SC-86720

Placed by: USAEMA, Philadelphia, Pa.

Object of Study:

**Production Engineering Measure (PEM)
in accordance with Step 1 of Signal
Corps Industrial Preparedness Pro-
curement Requirements (SCIPPR) No.15,
dated 1 October 1958, for improvement
of production techniques to increase
the reliability for the Jet Etch
Transistor type 2N501A, with a maximum
operating failure rate of 0.01% per
1000 hours at a 90% confidence level
at 25°C as an objective.**

Philco Project No. R-232.1

Report Prepared by J. Sanders

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SECTION I - ABSTRACT

Data is submitted on the operating and storage life tests and environmental tests performed on two groups of pilot line transistors. The failure rates demonstrated by the tests are higher than the specified goal. The test results are not consistent with evaluation of units of the same type fabricated in the factory, or of units manufactured earlier on the pilot line. Failed units are being analyzed to define the failure mechanisms.

Installation of the hot sealing oven in a factory drybox is complete and units are being processed through it for accumulation of 2500 units for evaluation. The helium leak test equipment is in the process of being installed in the factory line area. While awaiting completion of the installation, units are being helium leak tested on existing laboratory equipment. The Reliability and Quality Control Department is sampling the production line output to qualify the device for general sale.

Additional work is reported in connection with production line process control inspections. An over-all process control specification has been completed and will be implemented in the next quarter. The specification is included in this report.

Further work on thermal resistance determination is described. The work centered on the d-c β method. Procedures of the method are described and its advantages and anticipated usefulness are indicated. Production line transistor failure rates continue to have a close fit with the proposed acceleration curve.

SECTION II - PURPOSE

The purpose of this contract is to improve production techniques to increase the reliability of transistor type 2N501A (or of additional or substitute transistors as specifically authorized by the Contracting Officer). An objective is a maximum operating failure rate of 0.01% per 1000 hours at a 90% confidence level at 25°C. This failure rate is an objective and as a minimum, all process improvements listed below will be performed toward attaining or exceeding it.

Processes to Be Improved

- a. Plating Edge Definition
- b. Higher Temperature Alloys
- c. Lead Attachments (includes collector attachments)
- d. Gettering Techniques for Encapsulating and Sealing
- e. Thermal Dissipation of Package
- f. Leak Determination.

The process improvements will be incorporated in a production run for final test, and the data obtained will be consolidated and presented in accordance with Part 1 of the ASTM Manual on Quality Control of Materials, January 1951.

Performance of the contract also calls for the delivery of the following items:

1. Engineering Samples (48 each)
2. Quarterly Reports (75 copies/qtr)
3. Final Engineering Report (75 copies)
4. Bills of Materials and Parts (2 copies)
(Forms DD 346 and DD 347)
5. General Report on Step II (6 copies)
(Twice the maximum rate attainable with existing facilities).

SECTION III - NARRATIVE AND DATA

3.1 Evaluation of Pilot Line Transistor (A. McKelvey)

An evaluation of the final design of the pilot line transistor was conducted during this quarter. The evaluation comprised operating life, storage life and environmental testing, and was conducted on two groups of transistors drawn from the pilot line. One group (designated as Construction N) included all process improvements, while the other group (designated as Construction M) included all process improvements except hot sealing. The results of this evaluation are contained in Tables 3-1 and 3-2. Endpoint criteria used to determine failures are:

I_{CBO} at $V_{CB} = -6v$ ----- $-6\mu A$ max.

V_{CBO} at $I_C = -100 \mu A$ ----- $-12v$ min.

h_{FE} at $V_{CE} = -0.3v$ and

$I_C = -10 mA$ ----- 20 min.

To these endpoints, the computed combined failure rates established by the data of Table 3-1 are listed below.

<u>Test Condition</u>	<u>Transistor Hours</u>	<u>Total Failures</u>	<u>Failure Rate %/1000 hours</u>
250 mw	347,000	78	22.5
150 mw	150,000	5	3.3
175°C	262,500	84	32.0
125°C	225,000	1	0.5

In all cases, except the 125°C storage life tests, these failure rates are significantly higher than that required to attain the desired goal of 0.01%/1000 hours at 60 mw at 25°C to a 90% confidence.

It should be noted that these results are not consistent with the results obtained on the same unit manufactured in the factory and are also at variance with earlier units manufactured on the pilot line. An example of this is shown in Table 3-3. From this data it can be seen that earlier pilot line units (L-1103 and L-1165) had a 175°C storage failure rate of 2.1%/1000 hours and that a recent group of factory manufactured units is currently running at a 175°C storage failure rate of 2.7%/1000 hours. These are both well within the desired failure rate at this temperature to attain the desired goal.

Of the 175°C storage tests shown in Table 3-1, failure analysis work has been partially completed on 7 of the 84 hFE failures. This work has verified the seven as hFE failures to the designated end-point. Helium leak tests have shown the packages to be tight. Electrical tests on the units have shown severe degradation of the

emitter-base diode with some of the units, with typical initial BV_{EBO} of 7 v, degrading to near shorts (0.4 v). Further data will be required for a decision regarding the failure mechanism.

The three drop failures and one centrifuge failure shown in the environmental summary, Table 3-2, have been determined to be broken blanks with the break occurring along the forward edge of the tab. This type of failure has also been seen on the factory unit and has been corrected by extending the organic junction coating back so that it overlaps the tab-to-blank solder joint on both sides of the transistor. Factory units of this construction have survived both the 9-foot drop test and the 20K "G" centrifuge test without failure.

3.2 Incorporation of Process Improvements in Production Line (J. Javes)

With the exceptions of hot sealing and helium leak testing, both reported below, all process improvements were previously incorporated in the production line as described in the Third Quarterly Report.

3.2.1 Hot Sealing Oven (E. Lobko)

Operation of the pilot line was terminated March 31, 1963 and at that time the prototype hot sealing oven was moved from the laboratory to the production floor and installed in the factory drybox. At the

present time, 300 transistors per day are being diverted from the production line to be processed through the hot sealing oven. These transistors are being processed according to the specification for the reliable transistor and are being accumulated into one lot of approximately 2500 transistors for evaluation.

3.2.2 Helium Leak Test (A. McKelvey)

The helium leak test equipment has been received and is in the process of being installed on the production floor. During the interim, all transistors for the reliability program manufactured on the production line are being helium leak tested on the existing laboratory equipment. During this quarter, a total of 4811 transistors were bombed and tested; 6 helium leakers and 3 wet bomb leakers were found for a combined leak failure rate of 0.2%.

3.3 Production Line Operation

3.3.1 Operating and Storage Life Data (J. Sanders)

As was reported in the Third Quarterly Progress Report, the Reliability and Quality Control Department is currently sampling the output of the production line as part of a standard procedure of qualifying the device for general sale. Additional data has become

available this quarter as the result of this testing and is presented in Table 3-4. The endpoint criteria used to determine failures are the same as those listed in subsection 3.1 of this report. From this data, the following observed failure rates are computed.

<u>Test Condition</u>	<u>Transistor Hours</u>	<u>No. of Failures</u>	<u>Failure Rate %/1000 hours</u>
150 mw	567,000	2	0.35
190 mw	13,600	0	----
200 mw	200,000	5	2.50
225 mw	6,800	0	----
250 mw	200,000	13	6.50
100°C	577,000	1	0.17
125°C	226,800	0	----
150°C	323,400	0	----
175°C	75,000	2	2.67

A plot of the operating failure rate data is contained in Figure 3-1. In addition, points for the observed failure rates for storage life tests at 100°C and 175°C are plotted. The 100°C point fits the curve with reasonable accuracy and has been used in obtaining the curve shown. This curve has a slope equivalent to an activation energy of 17.4 kcal/mole, which is somewhat less than the value of 19.6 kcal/mole which was originally proposed for a thermally induced reaction of this type.

3.3.2 In-Process Control (A. McKelvey)

During this quarter the standard production line process control inspections were reviewed. Additions and revisions to the standard

procedure were made where required and an in-process control commensurate with a high reliability transistor was developed. An over-all process control specification was prepared and is included in this report as Figures 3-2 and 3-3. This plan will be implemented during the early part of the next quarter so that full and effective control of the line will be realized for the production run.

3.4 Supporting Programs

3.4.1 Inspection and Quality Control Plan (E. Wojcik)

A draft copy of the Inspection and Quality Control Plan has been prepared and was submitted to USAEMA this quarter. The plan was reviewed and found not acceptable by USAEMA, due primarily to insufficient detail in the narrative portion of the plan. The plan is being revised and will be resubmitted in the near future.

3.4.2 Chemical Control Program and Specifications (T.Manns, E.Cocozza)

During this quarter specifications relating to the manufacture and testing of transistors on the production line were written and issued as listed below.

PS 022-4004	Process Quality Mount Inspection
PS 80-020	Overall Fabrication Outline -T2820 (L-5465)
PS 80-311	Processing Flow Chart - T2820 (L-5465)

PS 80-310 Filled Epoxy Coating of Electrochemical Transistors

PS 80-315 Leak Testing Sealed Electrochemical Transistors.

3.4.3 Thermal Resistance Program (D. Rizzetto)

Work on thermal resistance during the fourth quarter has consisted mostly of work on a variation of the d-c β method which eliminates much of the error caused by the variation of d-c β with voltage and is usable over a wider range of currents. Essentially, the base current of a grounded-emitter transistor is measured at a high temperature and suitably chosen point on one of the V_C - I_C characteristic curves. It is assumed that for this value of base current there is only one curve which represents a given junction temperature. At the measuring point on the V_C - I_C curve, the slope of the curve is measured using a General Radio impedance bridge. If it is assumed that the slope of the V_C - I_C curve is fixed over the voltage range covered for the succeeding measurements (a reasonable assumption for voltages between the saturation voltage and avalanche voltage), a collector characteristic curve can be drawn to represent the particular junction temperature at the chosen value of constant base current.

The temperature is then lowered to a new value and V_C is varied (with I_B held constant) until I_C has a value near that originally chosen. At this new point, another slope measurement is made. This new point must also lie on a new curve of constant temperature for

the same value of I_B as the original point. A number of such points are obtained and graphically used to locate the V_C - I_C coordinate lying on the curve postulated from the initial high temperature measurement.

In essence, the foregoing measurements provide enough information to allow a reasonably accurate prediction of a family of collector characteristic curves for constant junction temperature at a particular value of base current. All that is required to obtain the thermal resistance is to match the curve obtained by the application of power to the one obtained by the elevated case temperature measurement. Graphic illustration of such a family of curves is shown in Figure 3-4 for a typical L-5465.

The measurement of the slope or impedance at each of the secondary points provides more complete knowledge of the originally assumed curve as well as assurance that the transistor is not being operated in the avalanche region. With this additional information, high order corrections are possible. The variation in calculating thermal resistance will vary somewhat with the output impedance of the transistor at the secondary measurement. This variation, however, is relatively minor and the degree of variation for various assumed slopes can be seen in Figure 3-5. The complicated nature of the

method described above should not be misleading, since many simplifications of the procedure are possible.

By the modified d-c β method described above, the problem of the variation of d-c β with voltage is practically eliminated. Also, since the output impedance of the transistor is being constantly monitored, there is immediate awareness of collector voltage extension into the avalanche region. Because of these two desirable features, very little variation has been experienced in thermal resistance with current over a fairly wide range of currents (Figure 3-6). In a preliminary check using the same equipment and the same operator, the repeatability of thermal resistance measurements has been within $\pm 4\%$ (Figure 3-7). The distribution of thermal resistance on the twenty units which have been measured has been normal. The method has been tried only on the L-5465.

A number of these same units tested by the modified d-c β method have also been read by the original d-c β (grounded-base, uncorrected for h_{FE} variation with voltage) method, both on the original equipment and on an independent set-up, as well as on equipment using the d-c V_{EB} method. The new grounded-emitter d-c β method produces numbers for thermal resistance in the same order of magnitude as those obtained from measurements by the d-c V_{EB} and pulsed V_{EB} methods, but the original grounded-base d-c β method yields numbers about twice as high

as those secured from any other method of thermal resistance measurement. If, however, the voltage correction factor used in the new method is ignored, the new d-c β method produces results very similar to the original d-c β method. A comparison of results obtained by various methods of thermal resistance measurement on L-5465 transistors is given below.

Comparison of Methods of Thermal Resistance Measurement
(Values for L-5465 Transistors - °C/mw)

<u>Unit No.</u>	<u>D-C VBE Method</u>	<u>Grounded-Emitter hFE with Vc Corr.</u>	<u>Grounded-Emitter hFE, no Vc Corr.</u>	<u>Grounded-Base hFE Original</u>	<u>Repeat</u>
1	0.207	0.190	0.37	0.329	0.403
4	0.246	0.223	0.49	0.483	0.510
5	0.264	0.261	0.45	0.461	0.470
7	0.242	0.217	0.43	0.413	0.427

Several alternatives which could be pursued in further thermal resistance work are summarized below.

1. Concentrate on measuring large quantities of L-5465 transistors for thermal resistance by all of the present methods, placing the units on life, and comparing the measured thermal resistance with the thermal resistance derived from the life test results. The outcome of this could be misleading in that absolute correlation between thermal resistance measurements and life test results is only assumed and has never been substantiated.

2. Perform an intensive engineering analysis of all of the methods available for measuring thermal resistance in an effort to find the method most sensitive to variations in construction. This approach assumes that the selected method would then successfully predict life test performance, providing a relative (but not necessarily absolute) estimate of life test performance.
3. Concentrate work on all the methods in an effort to select the most repeatable method, least sensitive to variations in measurement techniques, and usable over the widest possible variety of transistor types. This might allow independent measurements of thermal resistance on all types of transistors by various manufacturers and show similar results without particular regard for correlation with life test results.

Pursuit of the first of the above alternatives would be extremely expensive and time consuming, since correlation of thermal resistance and life test results is presupposed, but has never been actually verified in practice. The second alternative is recommended, since it offers the possibility of a relative degree of correlation between thermal resistance values and life test performance. If a degree of correlation can be obtained, it would be desirable to follow up with

the third alternative in an effort to standardize readings throughout the semiconductor industry; however, such standardization of readings would be relatively valueless on a thermal resistance measurement which showed no correlation whatsoever with life test performance.

3.5 Incorporation of Process Improvements in Additional Production Line (J. Sanders)

During the latter part of this quarter, an additional production line utilizing some of the process improvements developed under this contract was set up at Philco. This line is currently manufacturing an amplifier transistor for UHF television application. The process improvements included in this line are:

- a. Diffused collector structure (MADE*)
- b. High conductivity-high temperature electrode systems
- c. Reinforced junction
- d. High conductivity encapsulant
- e. High temperature vacuum bake
- f. High temperature stabilization bake.

3.6 Engineering Schedule (J. Sanders)

A review of the engineering schedule for this program, Figure 3-8, shows that process improvements 1, 2, 3, 5 and 6 are complete. Process

* Trademark of Philco Corporation for Micro Alloy Diffused Electrode Transistor.

(improvement number 7, leak determination, will be completed next quarter when the new leak detection equipment, presently on the production floor, has been set up and put into operation. Process improvement number 4, controlled formation of surface oxides for surface stabilization, has been deleted as a result of process improvements implemented in accordance with USAEMA Approval of Technical Action Request No. PL-1, dated 8 October 1962.

Incorporation of process improvements on a factory production line has been completed with the one exception of helium leak testing. This has been covered in subsection 3.2.2 of this report.

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SECTION IV - CONCLUSIONS

1. Evaluation of the final design of the pilot line transistor has shown failure rates higher than required to attain the goal of the contract. For reasons unknown at this writing, these failure rates are higher than previously obtained, both on pilot line transistors and transistors manufactured on the production line.
2. All process improvements except helium leak detection have been installed on the production line and the line is currently manufacturing devices.
3. Failure rates obtained on production line transistors continue to fit, with reasonable accuracy, the acceleration curve proposed for this device.

SECTION V - PROGRAM FOR THE NEXT INTERVAL

1. Complete evaluation of pilot line transistor and explore cause of failures.
2. Complete installation of helium leak test equipment.
3. Implement in-process control inspections for production run.
4. Complete revision of Inspection and Quality Control Plan and submit to USAEMA for review and approval.
5. Continue the thermal resistance measurement program.
6. Begin production run and production run testing.

SECTION VI - PUBLICATIONS, REPORTS AND CONFERENCES

No publications, lectures, or reports pertaining to work developed on this contract were issued or given during the period covered by this report.

SECTION VII - IDENTIFICATION OF PERSONNEL

The key technical personnel who have taken part in the work covered by this reported are listed below and the approximate hours of work performed by each is given. Total approximate man-hour figures are also given for three general categories of technical assistance furnished to the key personnel during the quarter. Background resumes are included for two key individuals added to the program during the quarter.

<u>Name</u>	<u>Approx. Man-Hours</u>
Cocozza, E.	58
Javes, J.	196
Lobko, E.	61
Manns, T.	82
McKelvey, A.	456
Rizzetto, D.	21
Sanders, J.	213
Wojcik, E.	<u>26</u>
Total	1113
Misc. Engineering	1245
Technicians and Operators	2568

LOBKO, EDWARD R. - Engineer

Mr. Lobko graduated from Villanova University in 1948 with two B.S. degrees - one in Naval Science with engineering electives, and the other in Marketing. While serving for three years as an enlisted man in the Navy, working on aircraft electronics, he had taken the seven-months Navy Electrical Course. Later, as a lieutenant, j.g., he served for a year and a half in the Navy Supply Corps.

Prior to joining the Lansdale Division of Philco Corporation in 1955, he had had a year's experience with U.S. Gauge Co. in liaison engineering, and two years with IBM on field servicing of equipment. At Philco he has worked on many types of equipment and processing apparatus for the fabrication and testing of semiconductor devices and cathode ray tubes. Among these have been a thermal fatigue test set for diodes, automatic dispenser for the cathode ray tube settling process, process control for epitaxial furnaces, automatic vacuum aluminizer, KOH etch unit, dual probe solderer, automatic diode assembler, gold spot plating machine, and transistor stem machines. On this contract he has devoted effort to the hot sealing oven.

RIZZETTO, DARWIN J. - Senior Engineer

Mr. Rizzetto received his B.S.E.E. from Lehigh University in 1959 and has done graduate work in Electrical Engineering at the Pennsylvania State University. He joined Philco Corporation in 1959 as a semiconductor evaluation engineer, specializing in high frequency transistor evaluation and characterization. He has designed and employed numerous UHF coaxial test equipments. He contributed to the development of the first 5Kmc f_{max} transistor, the Philco T2351, and has been active in establishing definitions and methods for high frequency transistor measurements, such as f_T , r_b' , C_c , power gain, and noise figure. He has applied for two patents, entitled "Distributed Parameter f_T Test System," and "Transistorized Ignition System." He is a member of the IRE and its Professional Group on Microwave Theory and Techniques.

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APPENDIX - TABLES AND FIGURES

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Table 3-1

OPERATING AND STORAGE LIFE DATA

ON PILOT LINE TRANSISTOR

Group No.	Test Cond.	No. Units	Test Hours	Const.	Failures		
					ICBO	VCR	hFE
					VCR=-6v	IC=-100μA	VCE=-0.3v IC=-10mA
R9221	250mw	43	2000	M	3	3	16
R9225	250mw	57	1500	M	8	16	5
R9224	150mw	100	1500	M	1	4	0
R9228	250mw	50	1500	M	1	3	6
R9234	250mw	75	670	N	1	6	0
R9235	250mw	75	670	N	1	7	2
R8250	175°C	100	1500	M	0	0	39
R8251	125°C	100	1500	M	0	1	0
R8256	125°C	75	1000	N	0	0	0
R8255	175°C	75	1500	N	0	0	45

TABLE 3-3

175°C STORAGE LIFE DATA ON EARLIER PILOT LINE TRANSISTORS
AND ON RECENT FACTORY MANUFACTURED TRANSISTORS

Group No.	Test Condition	No. Units	Test Hours	Construc- tion	Failures		
					ICBO	VCE	hFE
					VCE=-6V	IC=-100μA	VCE=-0.3V IC=-10mA
L-1103	175°C	20	1700	I	0	0	0
L-1165	175°C	15	1000	K	0	1	0
R-8263	175°C	75	1000	Factory	1	0	1

TABLE 3-4

OPERATING AND STORAGE LIFE DATA
ON UNITS FROM PRODUCTION LINE

Group No.	Test Condition	No. Units	Test Hours	Failures		
				ICBO	VCB	h _{FE}
				VCB=-6V	IC=-100 μ A	VCE=-0.3V IC=-10mA
Q3009A	150 mW	40	2000	0	0	0
Q3009B	150 mW	20	2000	0	0	0
Q3009C	150 mW	140	2000	1	1	0
Q3010A	200 mW	35	2000	0	1	0
Q3010B	200 mW	50	2000	1	1	1
Q3010C	200 mW	15	2000	0	1	0
Q3011A	250 mW	35	2000	0	3	1
Q3011B	250 mW	45	2000	0	4	3
Q3011C	250 mW	20	2000	0	2	0
Q3015A	150 mW	50	2000	0	0	0
Q2007A	125°C	20	2000	0	0	0
Q2007B	125°C	35	2000	0	0	0
Q2007C	125°C	45	2000	0	0	0
Q2008A	100°C	40	2000	0	0	0
Q2008B	100°C	160	2000	0	0	0
Q2009A	150°C	35	2000	0	0	0
Q2009B	150°C	50	2000	0	0	0
Q2009C	150°C	15	2000	0	0	0
Q2011	150°C	55	2000	0	0	0
Q2012A	100°C	55	2000	0	0	0
Q2026	100°C	100	670	0	0	1
Q2027	125°C	40	670	0	0	0
Q2028	150°C	20	670	0	0	0
R8263	175°C	75	1000	1	0	1
Q3035	150 mW	100	670	0	0	0
Q3036	190 mW	40	340	0	0	0
Q3037	225 mW	20	340	0	0	0

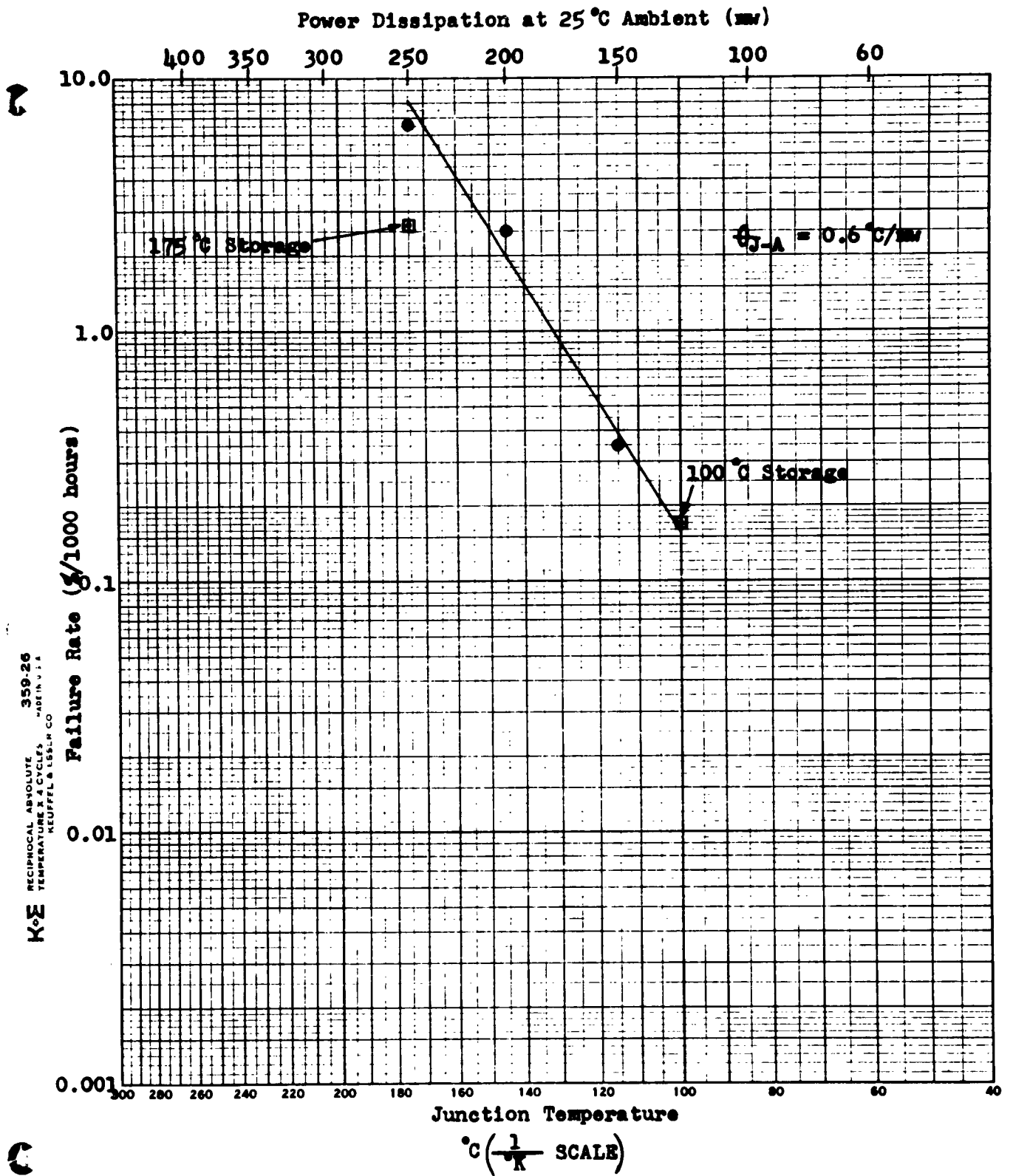


Figure 3-1. Observed Failure Rate Curve for Production Transistors

Figure 3-2.

PRODUCTION LINE OVERALL PROC
HIGH RELIABILITY TRANSISTOR

Part of Quality Assurance Specification No. 2008
Plant 40

Line: Fat Line #4 & 5 Location: Green Room Basic Type: L-5465

Flow Chart Ref. No.	Check	Performed By:	Print No.	Additional Specs. No.	Frequency of Check	Sample Size	Deci
1	Profile of Diffused Material	Process Control Inspector	2008-1217	PS 80-316	Each lot	One (1) unit per lot.	Distance ≥ .03 mi Peak V. Peak V. VEB > 7V
2	Dual Probe Solder Tab-Blank Solder strength and alignment	Process Control Inspector	2008-1200		Two (2) times per shift.	Three (3) units from each soldering station in operation	Visually print #: failure force =
3	Dual Probe Solder Tab-Blank Solder Connection	Process Control Inspection	2008-1201	PS 80-140	One (1) time weekly, day shift only	"	Reject lapping evidence
4	Jet Etching Base width	Process Control Inspection	2008-1202	PS 80-010	Four (4) times per shift.	Five (5) units.	Record
5	Emitter Diode Breakdown Test	Process Control Inspection	2008-1218		Two (2) times per shift.	Five (5) units.	VEB ≥
6	Jet Etching Collector pit Contour	Process Control Inspection	2008-1203	PS 80-010	Two (2) times per shift.	One (1) unit.	Collect dia. 13 deviati
7	Collector and Emitter Electr- ode Diameters	Process Control Inspection	2008-1219		Two (2) times per shift.	Five (5) units.	Emitter 5.0 - 5 Emitter = 2.8 - Collect = 6.0 - Collect attach Emitter attach A-6

Figure 3-2.

OVERALL PROCESS CONTROL PRINT # 2008-107

STABILITY TRANSISTOR

Date:

Revision:

Page 1 of 2

APPROVALS: Originator

In Process

THIS SPECIFICATION WAS NOT
ISSUED THROUGH REGULAR CHANNELS
AND WILL NOT BE SERVICED.

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of	Sample Size	Decision making criteria	Information		Corrective action
			Recording	Notify	
	One (1) unit per lot.	Distance between 7V to peak V. $\geq .03$ mils. Peak V. to cross over $\leq .05$ mils Peak V. depth is .18 to .26 mils VEB $> 7V$	Record results in Inspector's log book.	Engineer Supervisor	Engineer & Supervisor ascertain cause of and institute corrections. Refer to QAS 2008 Sec. 3, Para. 3-1-1 for resumption of production prior to resampling by Process Control Inspector.
times	Three (3) units from each soldering station in operation	Visually inspect as per Page 2 print #2008-1200 and reject for failure to withstand applied force ≤ 40 gm.	Record results in Inspector's log book.	Supervisor	Use of any station in which rejects occur is discontinued. Mechanic repairs station. Refer to QAS 2008 Sec. 3, Para. 3-1-1 for resumption of production prior to resampling by Process Control Inspector.
times	"	Reject with $< 2/3$ of blank overlapping tab failing to show evidence of soldering.	Record results in Inspector's log book.	Supervisor	Same as reference #2.
times	Five (5) units.	Record for information only.	Record W_b		
times	Five (5) units.	VEB $\geq 7V$.	Record results in Inspector's log book.	Engineer Supervisor	Same as reference #1.
times	One (1) unit.	Collector etch pit flat bottomed dia. 13 mils ± 1 mil with flatness deviation not to exceed .05 mils.	Record minimum of 9 readings at .002" intervals in each of two directions front-back and left-right. Plot readings on 10x10 div/in graph paper. Post on Line Control Board.	Supervisor Engineer	Etch plate technician adjust jets, lights, reflectors, etc. until desired pit is obtained. Resume production as in reference #1.
times	Five (5) units.	Emitter pit dia. at etchplate = 5.0 - 5.5 mils. Emitter plating dia. at etchplate = 2.8 - 3.2 mils. Collector dot dia. at etchplate = 6.0 - 6.2 mils. Collector Electrode dia. at lead attach = 6.0 - 7.0" Emitter Electrode dia. at lead attach = 2.8 - 3.2" A-6	Record results on control chart.	Supervisor Engineer	Same as reference #1.

PRODUCTION LINE OVERALL PROCHIGH RELIABILITY TRANSISTOR

Part of Quality Assurance Specification No. 2008

Plant 40

Line: Fat Line #4 & 5Location: Green RoomBasic Type: L-5465

Flow Chart Ref. No.	Check	Performed By:	Print No.	Additional Specs. No.	Frequency of Check	Sample Size	Decision
8	Metallographic Sectioning	Process Control Inspector	2008-1220		One (1) time per day.	One (1) unit.	For engin
9	Dust Shield Sample Physical Inspection	Process Control Inspector	2008-1204	Mount Insp. Chart 022-4004	Five (5) times per shift.	Five (5) units per whisker welder.	Visually according #022-4004
10	Top Cap Fill	Process Control Inspector	2008-1216	PS 80-305	One (1) time per shift.	10 units	Weight of weight of equal 49
11	Radiograph	Process Control Inspector	2008-1018	Mount Insp. Chart 022-4004	One (1) time per shift.	10 units	Refer to 022-4004 Check Pr:
12	Dry Box	Process Control Inspector	2008-1208	PS 80-010	Hourly		Moisture ≤ 10 pp
13	Vacuum Bake Ovens	Process Control Inspector	2008-1012	PS 80-010	One (1) time per shift.		Oven tem Vacuum =
14	Hermetic Seal Testing - Helium Leak Check	Process Control Inspector	2008-1050		Two (2) times per shift.	Ten (10) units	Leak rat unit.
15	Hermetic Seal Testing - Detergent Bomb	Process Control Inspector	2008-1051		Two (2) times per shift.		Pressure
16	Black Paint	Process Control Inspector	2008-1055	PS 80-257	Each lot that is painted at the same time.	Double Sampling N1 = 32 N2 = 64	Refer to Dwg. No. Use A.N. Use A.N.



Figure 3-3.

OVERALL PROCESS CONTROL PRINT #2008-107

LIABILITY TRANSISTOR

Date:

Revision:

Page 2 of 2

APPROVALS: Originator

In Process O.C.

THIS SPECIFICATION WAS NOT
ISSUED THRU REGULAR CHANNELS
AND WILL NOT BE SERVICED.

L-5465

cy of k	Sample Size	Decision making criteria	Information Recording	Notify	Corrective action
time	One (1) unit.	For engineering evaluation.	Record in log book.	Engineer, Supervisor	Same as reference #1.
times t.	Five (5) units per whisker welder.	Visually inspect and reject according to Mount Insp. Chart #022-4004	Record results in Inspector's log book.	Supervisor, Engineer	Mechanic and/or Machine attendants adjust equipment to correct defects. Units in Process to be treated as per MIC 022-4004. Resume production as in ref. #1.
time t.	10 units	Weight of filled top cap minus weight of empty top cap must equal 49 ± 3 mg.	Record in log book.	Engineer, Supervisor	Mechanic checks fill mechanism, pressure, etc.
time t.	10 units	Refer to Mount Inspection Chart 022-4004 and Process Control Check Print #2008-1018.	Circle the indiv- idual faulty units on the negative with china marker. Record inform- ation in log book.	Engineer, Supervisor	Check tab and whisker welding operations. Resume production as in reference #1.
		Moisture content of Dry box ≥ 10 ppm water.	Moisture content readings plotted on control chart for line.	Supervisor, Engineer	Mechanic repairs dryers to reduce moisture content of air into Dry Box. Dry Box cannot be used if out of Spec. Units in Dry Box must be re-baked. See ref. #2.
time t.		Oven temperature $190^{\circ}\text{C} \pm 5^{\circ}$ Vacuum ≥ 10 microns	Record on control chart for line.	Supervisor, Engineer	Mechanic checks oven heaters or vacuum pumps and repairs. Units must be rebaked if conditions are not met. See ref. #1.
times t.	Ten (10) units	Leak rate $< 5 \times 10^{-10}$ cc/sec per unit.	Record in log book. Stamp route ticket.	Engineer, Supervisor	Same as reference #1.
times t.		Pressure = 80 ± 5 psi.	Record in log book. Stamp route ticket.	Engineer, Supervisor	Same as reference #1.
that ed at time.	Double Sampling N1 = 32 N2 = 64	Refer to QAS T-6. Dwg. No. 961-6822 Use A.N. = 1 for N1 Use A.N. = 3 for N2	Record in log book. Stamp route ticket.	Engineer, Supervisor	Same as reference #1.
A-7					

- ① Initial measurement and supposed characteristic curve for
 $T_J = \theta_{J-C} \times 40 + T_C(\text{High})$
- ② Locus of secondary measurement points
 $T_J = \theta_{J-C} \times 169 + T_C(\text{Low})$
 $= \theta_{J-C} \times 40 + T_C(\text{High})$
- ③ Intersection of locus with initial curve where

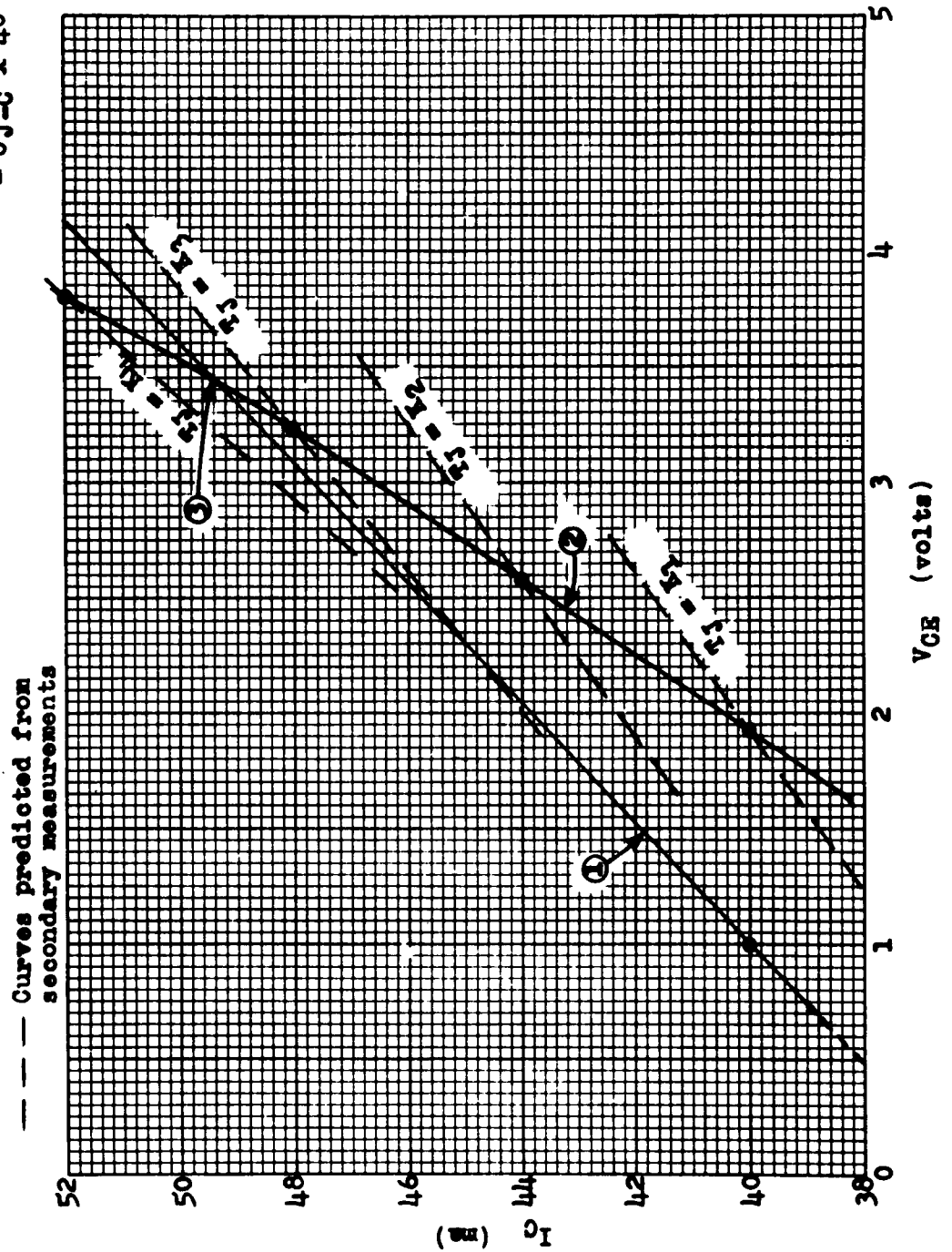


Figure 3-4. Collector Characteristic Family of Constant Junction Temperature Curves for $I_B = \text{Constant}$.

L-5465 Typical Unit #1 $I_C = 70 \text{ mA}$ $V_{CE} = 1.0 \text{ V}$ $\Delta T = 27.2^\circ\text{C}$

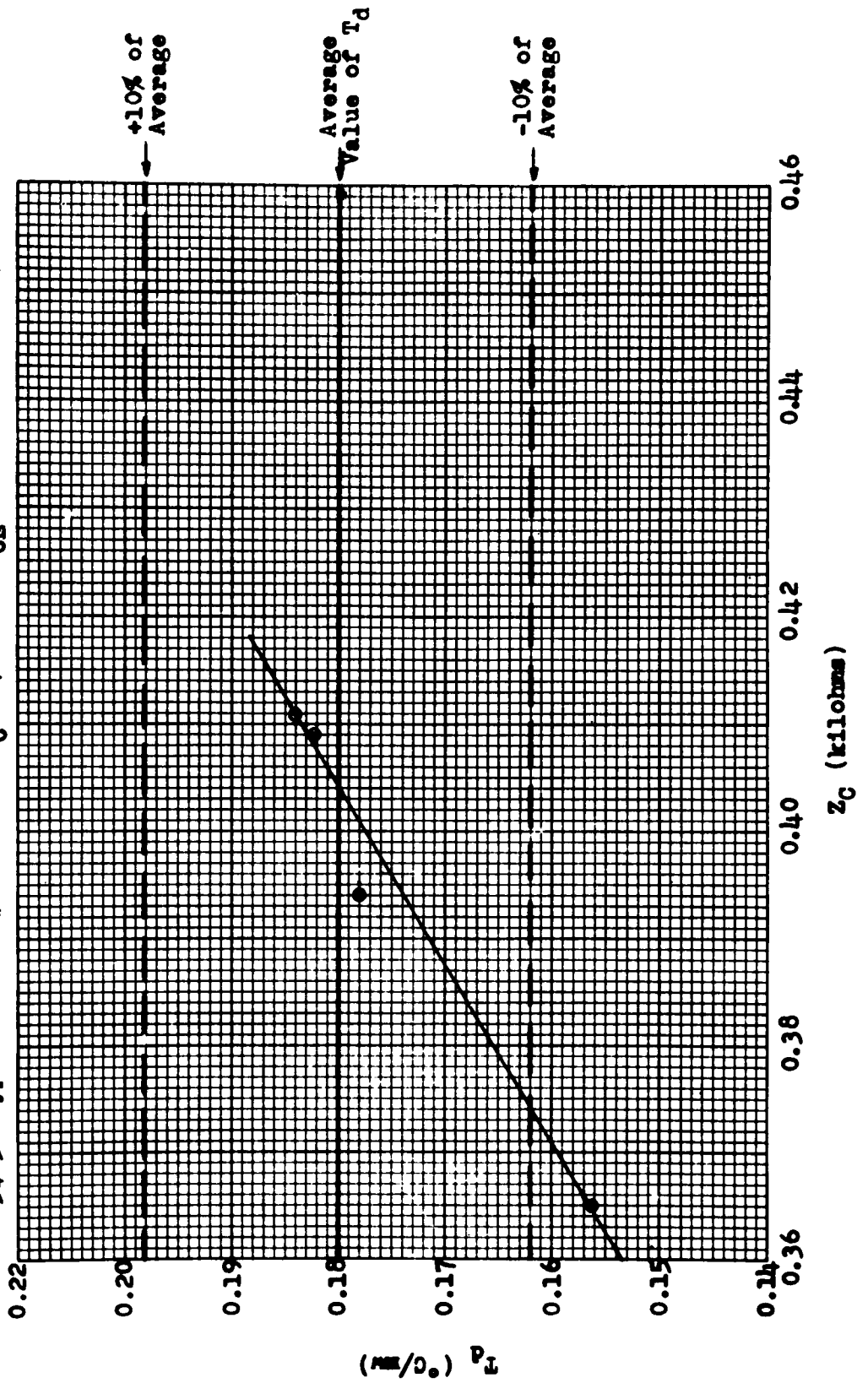


Figure 3-5. Thermal Drop vs. Collector Impedance

10 X 10
HEUFFEL & SONS CO. 300-45
NEW YORK 1, N. Y.

L-5465 Typical Unit #2

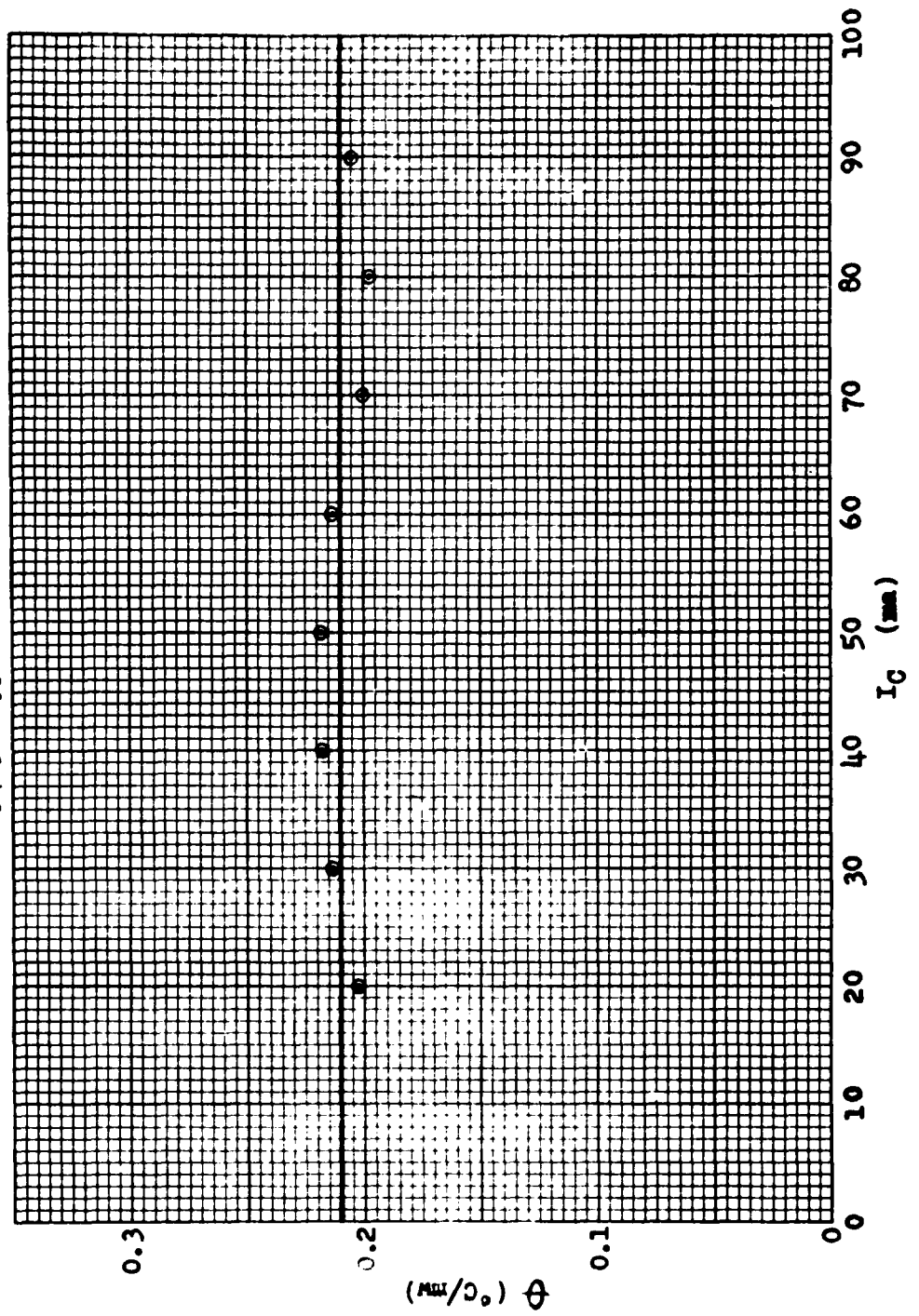


Figure 3-6. Thermal Resistance vs. Collector Current

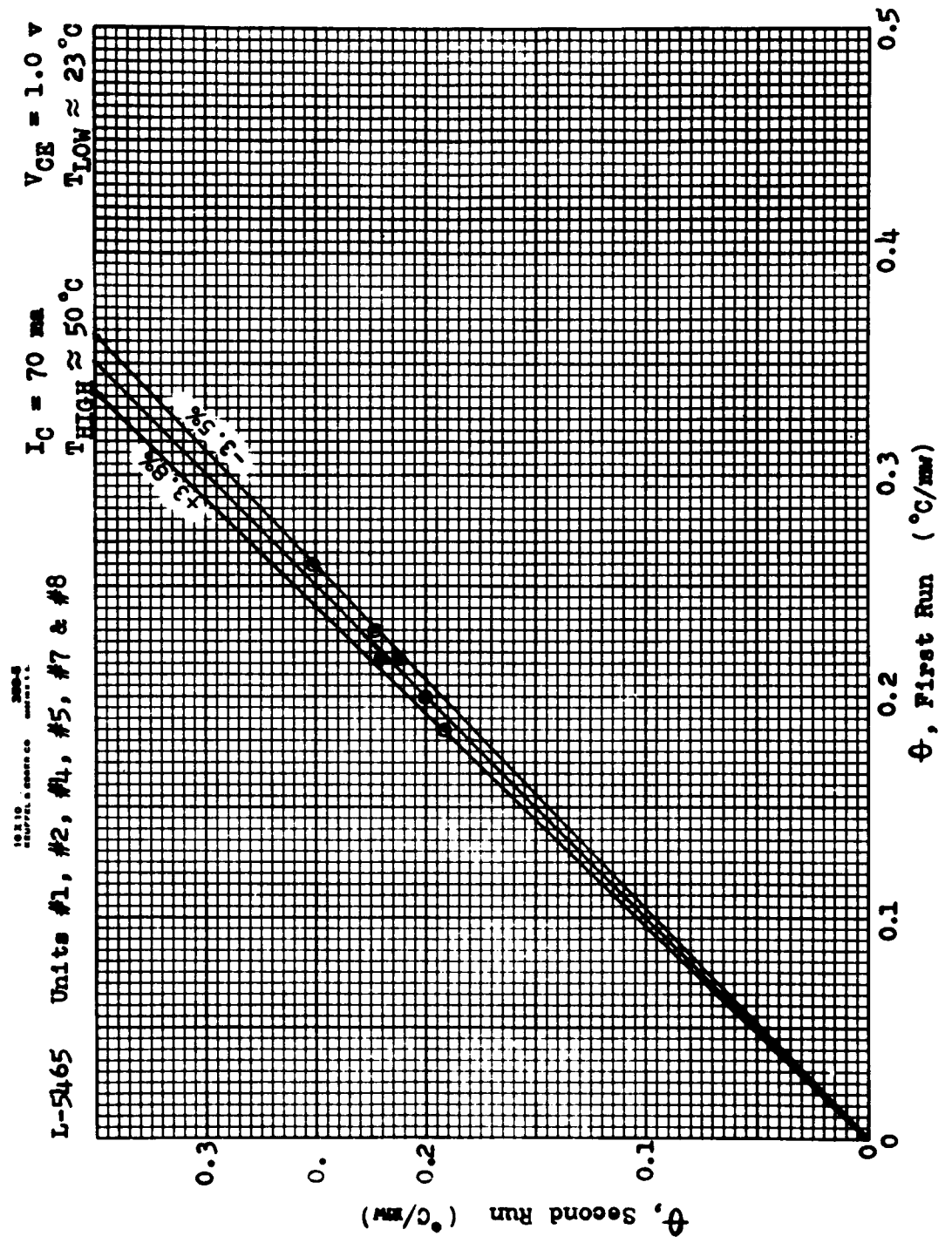


Figure 3-7. Repeatability Data

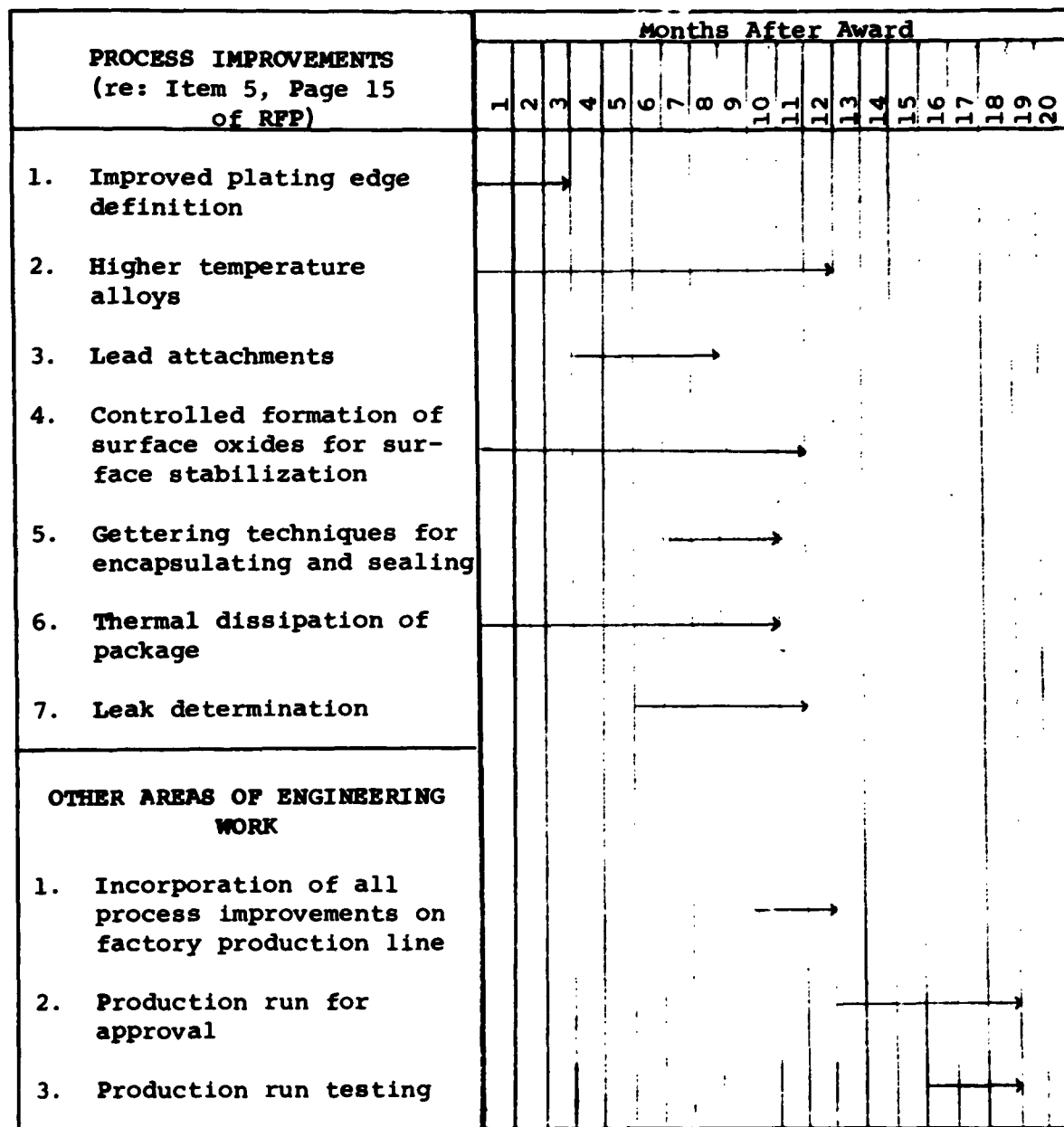


Figure 3-8. Engineering Schedule