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**DATA TRANSMISSION INVESTIGATION  
REPORT NO. 7**

**THIRD QUARTERLY PROGRESS REPORT**

**11 March 1963 to 10 June 1963**

**DA PROJECT NO. 3B31-07-001**

**CONTRACT NO. DA 36-039-SC-90728**

**(Continuation of Contract No. DA 36-039-SC-87343)**

U.S. ARMY SIGNAL RESEARCH  
AND DEVELOPMENT LABORATORY.  
FORT MONMOUTH NEW JERSEY

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**MOTOROLA INC.**

**Communications Division**

4545 W. AUGUSTA BLVD. CHICAGO 51, ILL.

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The objective of this program is to determine the characteristics and distribution of errors in digital data communications systems of the tactical army.

**SIGNAL CORPS TECHNICAL REQUIREMENT**

**SCL-4276, Dated 13 October 1960  
and**

**Amendment No. 1 dated 15 November 1961  
Amendment No. 2 dated 9 October 1962**

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**MOTOROLA INC.**

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## SECTION I

### PURPOSE

The purpose of this project is to investigate the performance of data transmission terminals over tactical military communications systems. Testing of the data terminals and communications systems will take place in the vicinity of Fort Monmouth, New Jersey.

A family of communications systems has been developed for the Army. These systems, designed primarily for voice communications, are to provide the circuits for digital data transmission. The limitations of these systems when functioning as digital data transmission links are to be determined.

Error statistics of the data transmission terminals obtained while operating over these communications systems are to be evaluated and reported upon. Included in this study is an investigation of the transmission of digital data in the presence of random and impulse noise. Error correction and/or detection will be investigated from the results of the error statistics. Encoding and decoding equipments will be constructed for testing with the modems over the various communication links.

## SECTION II

### ABSTRACT

Field test results of various modems operating over the AN/VRC-12 radio set are presented. Map profiles of each data link are shown and the average error rates are given for digital data transmission at rates from 300 to 4800 bps. Bit error rates vary from  $10^{-3}$  to  $10^{-6}$  depending upon the site and bit rate. The errors are analyzed for multiple error characteristics and the probability of receiving a message error free as a function of message length.

Photographs of the frequency spectra generated by each modem at their various bit rates are presented and used to discuss the relative bandwidth requirements of the modems. The performance of the FSK (AN/TYC-1, XC-2), Di-Phase and Quad-phase modems in the presence of a controlled impulse noise test while operating at 1200 bps is shown in graphical form.

A multi-frequency modem is being constructed for the HF data transmission study phase of the contract. The modem will have the capability of 18 bit rates and will be used in the investigation of the short range HF data transmission. System block diagrams of the multi-frequency modem are presented, and the performance of the clock generator and clock recovery circuits is discussed. Progress on the coding phase of the program is discussed, and results of a computer study performed on the (15,7) code is presented. The limits of the code's error correcting and detecting capability are shown, and the code's performance when these capabilities are exceeded is discussed.

### SECTION III

#### CONFERENCES

On April 22, 1963 a meeting was held between USAELRDL and Motorola personnel. The USAELRDL representatives were J. Buegler, J. Duffy, J. Tucker, and A. Gillette; the Motorola representatives were R. Salava and N. Thomas. The computer analysis to be performed on the data gathered from the AN/VRC-12 field tests was discussed. It was decided to analyze the data for (1) long term error rates, (2) distribution of errors (1, 2, . . . . or 8 bit errors), (3) percent of multiple errors, (4) distribution of error free intervals, (5) message reliability as a function of message length, and (6) the distribution of consecutive one second error intervals. The contract modification was also discussed, and it was decided to make report number 8 a summary report of the work performed during the first two years of the study program.

A second meeting was held between the aforementioned USAELRDL and Motorola personnel on June 11, 1963. The project status and test program for the next quarter were discussed. It was decided that the data gathered from the AN/VRC-12 tests was not sufficient at this date and the next quarter should be devoted mainly toward further AN/VRC-12 tests. The computer results from these tests show that the one second interval of analysis is not small enough to provide satisfactory information on consecutive error intervals and error free intervals. The decision was made to omit these two statistics (number 4 and 6) from the present analysis.

## SECTION IV

### FACTUAL DATA

#### 4.1 AN/VRC-12 TESTS

Field testing of the modems over the AN/VRC-12 radio set was continued during the last quarter. The characteristics of the radio set and the field test system are discussed in Quarterly Report Number 6. The equipments tested over this system were the FSK (AN/TYC-1, XC-2), Di-phase, and Quad-phase modems. Only a limited amount of testing was conducted with the Quad-phase modem since trouble was encountered with one of the terminals. All the test results given in this report were obtained with the AN/VRC-12 transmitter operating at 41.5 mc and a RF output power of approximately 35 watts.

Various transmission links were used in the AN/VRC-12 field tests and ground profile maps for each link were constructed to help evaluate the results properly. Figures 1 and 2 show the map profiles of the eight transmission links with the ground elevation as the ordinate and the distance (statute miles) scaled on the abscissa. The "dashed" line connects the transmitting and receiving antennas on a line-of-sight basis. Note that the receiving station is always at the left of the graph and the antenna is actually about 80 feet above the ground level. The radio links were chosen to present both line-of-sight and rough terrain transmission paths.

Most of the data gathered during the quarter was from site 10. This site presents a line-of-sight transmission path with the only obstacle being a hill approximately one mile from the transmitter. Since the transmission path skims over the hill, this obstacle did not present any major problem.

Data transmission links were established over all the transmission paths shown in Figures 1 and 2 although only a few tests were conducted at several of the sites. The average error rates for these tests are given in Figure 3. These error rates are an average of all the tests conducted at each site for a particular bit rate. The results from site 10 are the most significant since most of the testing was performed from this site. The right hand column in Figure 3 gives the number of tests conducted with each test approximately 200 seconds long. Each test was performed on a different day thus the effects of weather and noise are averaged into the results.

A comparison of the bit error rates and the character error rates given in Figure 3 show that the character error rate is approximately 8 times the bit error rate. This is especially true when observing the results of the FSK (AN/TYC-1, XC-2) modem. The Fielddata character used in these tests consisted of 8 bits and if each character has only one bit in error then the two error rates would differ exactly by a factor of eight.

The distribution of errors in the AN/VRC-12 field tests conducted during the quarter is shown in Figure 4. The results in Figure 4-A are a tabulation of single (N=1) and multiple (N>1) errors obtained from the "characters in error" column of the logging circuits and the "characters with multiple errors" column. The data for Figure 4-B were obtained from the "bit errors in the first character in error" column in the logging circuits and is only a sample of the multiple error distribution.

The results given in Figure 4-A show an increase in multiple errors with an increase in bit rate. Also shown is that the Di-phase modem produced a greater number of multiple errors than the FSK modem. It must be pointed out that these results are probably due to the specific implementation of the modem and not the modulation technique. It is believed that this result is mostly due to the different methods of clock recovery employed by each modem.

The AN/TYC-1, XC-2 (FSK) employs a stable clock from which it derives its receiver timing. The phase of the clock is corrected by examining the axis crossings of the incoming data signal which is either at 1200 cps (space) or 2400 cps (mark) assuming that no frequency translation occurs during the transmission of the data. The phase of the clock is corrected a few microseconds at a time; thus if a large impulse degrades the signal by a substantial amount, only a few erroneous corrections are made but not enough to seriously affect the timing in the receiver. This results in errors due to the actual degradation of the data signal and not a result of incorrect timing in the receiver.

The Di-phase modem recovers its receiver timing by an entirely different method. The timing for the demodulator is derived from the data signal through the use of tuned circuits. The output of the tuned circuit, which is the recovered clock, plus the data signal is applied to the demodulator. The effect of an impulse is noted in the data signal itself plus the recovered clock. A large impulse will affect the recovered clock phase but not in an instantaneous manner since the tuned circuit is present. This may lead to errors not only due to the degraded data signal but also due to an improper phase relationship in the recovered clock. The latter effect will be slightly delayed and may cause errors while the actual data signal is no longer degraded; thus the result will be a greater number of multiple errors. This may be the cause of the large

number of multiple error recorded in the tests of the modem operating over the AN/VRC-12, since it is known that almost all of the errors recorded in these tests have been caused by impulse noise.

Referring back to Figure 3 and examining the error rates of each modem at their various bit rates yields an interesting characteristic. As the bit rate is increased in the FSK modem the bit error rate also increases while with the Di-phase modem the opposite is true. This result is not easily explained, and it again refers back to the construction of each modem. The Di-phase modem has been designed to operate most efficiently at 1200 bps with all of its filtering designed for this bit rate. Report Number 5 analyzed the Di-phase modem with respect to its performance in white noise. The results in that report showed that the S/N improvement was less for each step in decreasing the bit rate. While approximately a 3 db improvement was noted between the 1200 bps and 600 bps rates, less than a 1 db improvement was noted when reducing the bit rate from 600 bps to 300 bps. This, in conjunction with the modem's performance in impulse noise is regarded as the cause of the reverse trend in error rates as compared to the FSK modem.

In general the performance of a modem should improve with a reduction in the bit rate if advantage is taken of the longer bit time and the possibility of reducing the bandwidth of the receiver input filter. It should be noted that the time distribution of impulse noise may also help determine the behavior of the error rate as a function of the bit rate. Since most of the errors in the AN/VRC-12 tests are caused by impulse noise, an increase in the bit rate may result in a greater number of multiple errors because each impulse extends over a larger number of bits. However, it is also true that during the error free time a larger number of error free bits are transmitted that may tend to balance the effect of the multiple errors. With the aforementioned areas of question plus the internal design of each modem, it is difficult to predict the performance of each modem without further testing. All these areas will be investigated to a further extent to help define the error characteristics obtained in this program.

The error results given in Figure 4 show that the use of a single bit error correcting code would reduce the error rates of both modems by a substantial amount. An exact distribution of errors is necessary to calculate the actual improvement in error rate by using multiple error correcting codes, but the present error logging system yields only an estimate of the error distribution.

The effect of single error correcting codes such as the Hamming (8, 4) code which consists of 4 information bit and 4 check bits can be evaluated from the results given in Figure 4. In the case of the FSK modem all the errors

recorded at 300 bps were single bit errors. At 600 bps only 3.1 percent of the errors were not single bit errors, while at 1200 bps only 2.9 percent fit into the multiple error category. If the 1200 bps case is taken as an example and if the (8, 4) code is used, the actual information rate would be 50% of 1200 bps. The character error rate would then become approximately 2.9% of the character error rate recorded at 1200 bps without coding, which becomes:

$$(0.029) (3.6 \times 10^{-3}) = 1.04 \times 10^{-4}$$

With the bit rate decreased to 600 bps without coding, an error rate of  $6.53 \times 10^{-4}$  was measured; thus if coding is utilized an improvement by a factor of greater than 6 is obtainable. This is only one example of the effect of coding, and this effect may be regarded as small in the case shown. However, if the 300 bps case is used as an example, it is found that while the effective data rate is reduced to 150 bps using the (8, 4) code, the transmission would have been error free since all the errors were single bit errors. Various codes are available with more powerful correcting capabilities, some of which are discussed in the last paragraph of this report.

Since digital data transmission systems consisting of a modem and the AN/VRC-12 radio set may be used to transmit messages in a tactical situation, it is desirable to know the probability of receiving a message free from errors. This probability is, of course, dependent upon the transmission link and the length of the message. To obtain an estimate of the accuracy that can be expected in a typical data link, the results obtained from site 10 were analyzed for message reliability vs. messages of various lengths. Figure 5 shows these results for messages of 1 second to 50 seconds in length. The results were compiled on the Burroughs 220 computer at Fort Monmouth by using the statistical transmission results recorded by the logging system. A computation was made of all possible positions in time that each message could have been transmitted, and each was checked for errors. The error free messages were divided by the total number of messages to obtain the probability of receiving an error-free message.

The probability of receiving a message free from errors is not only a function of the error rate but also a function of the error distribution, since an error burst will have a different effect than if the same number of errors were randomly dispersed. The results shown in Figure 5 give a probability factor for each bit rate, and both the bit rate and message length must be considered when using the table to decide what bit rate will give the most reliable transmission. If a message 10 seconds in length at 1200 bps is transmitted, it must be remembered that at 600 bps the time to transmit the same

message would be 20 seconds. Using the FSK modem it is seen that the 600 bps rate would result in more reliable transmission of the message than at 1200 bps, while the opposite is true for the Di-phase modem.

This opposite result is again due to the reverse trend in the error rate as a function of the bit rate as was previously discussed. The results here should be regarded only as a sample, since the number of tests were small and additional tests are required before the results should be considered as significant.

#### 4.2 SPECTRA ANALYSIS

Analysis of the spectrum generated by each modem is deemed necessary in order to determine the channel bandwidth requirements of each modem at their various bit rates. The spectrum generated by phase shift keying with discrete changes in phase is shown in Figure 6-A with  $f_c$  being the carrier and  $f_m$  equal to the modulating frequency. The spectrum is of the form  $\sin x/x$  displaced from the origin by  $f_c$ . It must be noted that this is the basic form, and deviation from this form will be dependent upon the various approaches used to obtain the phase modulated signal. Only the upper or lower sideband of the carrier is transmitted if single sideband or vestigial sideband techniques are employed, but the modems under study in this program generate both sidebands. Therefore, no further mention is made of single or vestigial sideband techniques. The spectrum generated by frequency shift keying with the modulating signal  $f_m$  is shown in Figure 6-B. The  $\sin x/x$  form is now centered about the two space and mark frequencies  $f_1$  and  $f_2$ .

Using the above brief discussion of phase and frequency modulation the spectra generated by each modem will be discussed. Each modem was connected back-to-back and a spectrum analyzer was placed on the line connecting the two modems. The data generator was set for the pseudo-random mode of operation in which the pattern was 2047 bits long. For the maximum bit rate of 4800 bps the repetition rate of the data was less than 3 cps, thus this effect was not noticed on the analyzer. Photographs were taken of each modem operating at all bit rates, and the results are presented in Figures 7, 8, and 9.

The spectra generated by the FSK (AN/TYC-1, XC-2) modem is shown in Figure 7. Two peaks are shown at the space and mark frequencies of 1200 cps and 2400 cps respectively. At the 1200 bps rate the space carrier frequency of 1200 cps and the modulating frequency  $f_m$  equal to 1200 cps results in nulls at zero and 2400 cps. With the mark carrier of 2400 cps, nulls occur at 1200 and 3600 cps; thus entire band of interest from zero to 3600 cps is

utilized at the high bit rate. The spectra photographs shown in the report have a db amplitude scale and a log frequency scale. The decibel amplitude scale tends to emphasize the lower level signals, and with the log frequency scale the upper sidebands appear not to be completely present, as is observed in Figure 7. Because of this scale the analysis is conducted using the lower sidebands in most cases.

At the 600 bps rate Figure 7 shows nulls at 600 cps and zero as would be expected. A null also appears at 1800 cps, which is the common null point for both carrier sidebands. At 300 bps the null points are less defined but appear to be at the expected points of 900, 600 and 300 cps. Because of the log scale, the nulls between the carriers cannot be readily seen, but they should also appear at 1500, 1800 and 2100 cps.

The results of the Di-phase modem are presented in Figure 8 for all four bit rates. In the Di-phase modem, a filter with its 3-db point at 800 cps shapes the data just before modulation; hence the sidebands generated by the modulator are limited. The modem adds a synchronization bit to each 8 data bits; therefore the actual transmission bit rate is  $9/8$  the data bit rate. For the maximum data rate of 1200 bps the actual modulating frequency  $f_m$  is 1350 cps.

The results given in Figure 8 show the obvious effect of the filter used for shaping the data before modulation. The carrier is at 2025 cps and the bandwidth at the 1200 bps data rate is observed to be between 1000 cps and 3000 cps. This is approximately 1000 cps above and below the carrier, so the first null points expected at 1350 cps above and below the carrier are not present because of the data shaping filter. The spectrum generated at the lower portion of the band is most likely due to switching transients in the modem.

At 600 bps a null point is observed to occur at approximately 1350 cps as expected, and the upper null points are present but are not readily seen in the photograph. Similar results are observed in at the remaining bit rates, with more of the null points being shown as the bit rate is reduced. At the lowest bit rate of 150 bps a null occurs every 168.5 cps on either side of the carrier.

The spectra generated by the Quad-phase modem are shown in Figure 9. The results here are similar to those of the Di-phase modem except the data in this modem is not band limited before modulation. Therefore, the spectrum generated in each case is observed to extend over the entire band of interest. The carrier at the 4800 bps rate is 2400 cps, while at the remaining rates it is 1920 cps. Since the modem utilizes four-phase modulation, the actual modulation rate is one-half the bit rate.

At the highest bit rate the resultant spectrum extends from almost zero to 4800 cps as expected. At the 2400 bps rate null points are observed to occur every 1200 cps on either side of the 1920 cps carrier. Note that while the spectrum in the lower portion of the band appears to be quite large, it is at least 20 db down from the carrier. Similar results are shown at the remaining bit rates. The null points in some cases are not easily observed because switching transients in the modem tend to obscure these points.

The results presented in the spectra study may be used as a guide in determining the expected performance of each modem over a particular channel. In the Di-phase and Quad-phase modems it is apparent that the modems were designed to operate over a channel with its characteristics centered near 2 kc. The FSK (AN/TYC-1, XC-2) modem with its carrier frequencies at 1200 cps and 2400 cps would operate best over channels with characteristics centered around 1800 cps.

It is interesting to compare the spectrum generated by each modem at the highest common bit rate of 1200 cps, since each modem employs a different modulation technique. The spectrum between the first null points on either side of the carrier (or carriers) will be used as the criterion of comparison. The FSK modem with its two carriers generates a band extending from zero to 3600 cps. If the synchronization bit in the Di-phase modem is omitted, this modem utilizes the band from 825 cps to 3225. With the Quad-phase modem the bandwidth is half that generated by the Di-phase modem, and in the case with the carrier at 1920 the spectrum between first null points extends between 1320 cps and 2520. Thus if conservation of bandwidth is desired, the modem best suited for this purpose (of the three discussed in this report) is the Quad-phase modem.

#### 4.3 IMPULSE NOISE TESTS

The performance of a modem in the presence of white noise does not give an indication of how the modem will perform when the noise is impulsive in nature. Since modems operating over both radio and telephone links experience many errors caused by impulse noise, tests have been included in this program to examine the performance of the modems under these conditions.

Report Number 3 describes the method used to generate the impulse that was used to test each modem. Photographs of the impulse and its spectrum were included in the third report. This impulse at a rate of 27 pps was used to test the Quad-phase, Di-phase, and FSK modems and the results are shown in Figure 10.

The results shown in Figure 10 are given as the error rate of each modem vs. RMS signal to peak-to-peak noise voltage ratio. The relative performance of the three modems at 600 bps is observed to be almost identical, showing a sharp improvement in error rate for a very small increase in signal-to-noise ratio. As the bit rate of the Quad-phase modem is increased, the slope of the curve decreases.

The results of these tests must be viewed carefully since this is only one of many types of controlled impulse noise tests that may be performed. The curves shown in Figure 10 give the performance of each modem for the particular impulse used in the tests. A different impulse would no doubt produce a variation in these results, and since the level of the noise is set to obtain error rates in the vicinity of  $10^{-5}$ , this does not necessarily simulate the actual conditions present in field operation.

#### 4.4 AN/TRC-24 FIELD TESTS

The modem field tests over the AN/TRC-24 radio system were initiated over the new link set up during the last quarter. A line-of-sight link approximately 7 miles long was established with a transmitter power capability of 15 to 70 watts. A block diagram and description of the system is given in Report Number 4 which differs only in the distance of transmission. The results were again very good, with all the modems performing virtually error free during the 150 hours of testing over the system. These tests were performed with both transmitters operating at the minimum power of 15 watts.

Since the AN/TRC-24 is designed for operation over links of approximately 30 miles (which is about the limit of line-of-sight operation), the link under test at this time does not present the typical situation that will usually be encountered under a tactical military operation. The only characteristic that can now be measured is the effect of storm activity, which presents only a limited amount of information.

#### 4.5 DATA LOGGING SYSTEM

The data logging system described in Report Number 6 was modified to permit easier processing of the data in the computer analysis phase. In the previous system 19 characters of information were automatically punched on the paper tape each time an error in transmission occurred. At the end of each test this information was transferred to cards, and additional information of the test such as the modem and bit rate were added to each card. This proved to be quite cumbersome. With the present modification, 32 characters (shown in Figure 11) are now used to describe the test, and these characters

are punched on the tape each second during which an error in transmission has occurred. Characters 20 through 31 are selected by the operator before the test is conducted by setting selector switches to their desired positions. This format reduces the chance of error in processing the data and also greatly reduces the work involved in inserting additional information in the tape-to-card conversion phase.

#### 4.6 MULTI-FREQUENCY MODEM

A multi-frequency data transmitter and receiver system will be constructed and used in determining optimum data transmission rates over HF radio data links. The system block diagram is shown in Figure 12. The system will consist of two Bell Data-phones (Model 202B), and multi-frequency clock generator and clock recovery circuits.

The Data-phone is an asynchronous FSK modem designed to operate up to 1600 bps, while the clock generator and recovery circuits will operate up to 19.2 K bps. The design of the clock-generator and clock recovery circuits have been completed. The clock generator is shown in block diagram form in Figure 13. The clock rates possible using the two selector switches are shown in the table below the block diagram. The B band provides all Fielddata rates from 37.5 to 19,200 bps.

A block diagram of the clock recovery circuits is shown in Figure 14. The clock recovery scheme is completely digital, hence the S'pac series of circuits are used throughout for standardization. The basic frequency selection is the same as in the clock generator, with the band switch selecting between the divide by 3, 4 or 5 and the frequency switch dividing in binary form between 0 and 256.

The last divide circuit in the clock recovery normally divides by 31 if no correcting information is available. The information used for correcting the phase of the recovered clock is derived from data transitions in the baseband signal. For each data transition a narrow pulse is generated by the "one shot" multivibrator. These pulses are compared with the recovered clock in gate circuits, and depending upon where the pulses occur with respect to the phase of the recovered clock, a decision is made to divide by 30 or 32. The pulses are made very narrow (approximately 0.5  $\mu$ sec), hence a correction will be made every time a transition in the baseband signal occurs. This results in an inherent jitter in the recovered clock of approximately  $\pm 3$  percent, but with this technique the system should perform equally well at all bit rates since there are no frequency selective circuits. Also note that the phase correction circuits (+30, 31, 32) are placed after the frequency selection; thus the correction is a constant value (approximately 3%) for all clock frequencies.

Operation of the clock generator and clock recovery circuits with the Data-phones was checked on a preliminary basis and found satisfactory. Further tests will be performed to determine the relative performance of the modem at the various bit rates in the presence of white noise. In addition, the minimum signal-to-noise ratio over which the clock recovery system will remain in synchronization will be determined in order to predict the system's operation over the HF radio link.

#### 4.7 ENCODER/DECODER

A transmitter coder and receiver decoder will be constructed and tested to help determine the effectiveness of error-correcting techniques in data transmission systems. This equipment will be basically designed to handle the (23, 12) Golay code and the (15, 7) Bose-Chaudhuri code, but if the method of implementation permits other codes will also be provided. A coding study of implementing these and other codes is presently being performed.

The coding study has been confined to cyclic codes which are fairly simple to implement. Cyclic codes are a form of block codes which consist of code words  $n$  bits in length, made up of  $k$  information bits plus  $n-k$  check bits. Data are transmitted in blocks of  $n$  bits which leads to the possibility of receiving  $2^n$  words. For each combination of  $k$  information bits there exists a combination of check bits, hence out of the encoder there are only  $2^k$  possible code words. It is the function of the decoder to decode these  $2^k$  code words and make a decision on the remaining  $(2^n - 2^k)$  words that are present if errors occur. The decision is made on a "maximum likelihood" basis which is briefly described in the following example. A (7, 4) code consists of 4 information bits and 3 check bit. The 16 possible code words (each consisting of the information bits plus check bits) are given below with the 4 information bits being at the right of each code word.

000000	1101000
1010001	0111001
1110010	0011010
0100011	1001011
0110100	1011100
1100101	0001101
1000110	0101110
0010111	1111111

If one of the code words is compared to all the remaining code words, it is observed that each word differs in at least three positions. For example, if the code word (000000) is compared to the code word (1010001) they are found to differ in the first, third and last bits. The number of positions in

which code words differ is called the Hamming distance. Thus a single error results in a Hamming distance of 1 between the transmitted and received word. In the example above, a single error while transmitting the all zero code word may result in the word 0000001, and if decoded using the "maximum-likelihood" criterion the corrected word would again be the all zero code word, since it is only one Hamming distance away while all other code words are at least two Hamming distances away.

The minimum Hamming distance of a code is defined as the minimum distance between all code words generated by the encoding scheme. The minimum distance of a code defines the capabilities of the code from both the error detection and correction viewpoints. If a code is used to detect all patterns of  $e_d$  or fewer errors, it is necessary and sufficient for the minimum distance between code words to be  $e_d+1$ . In a similar manner, it is possible to correct all patterns of  $e_c$  or fewer errors if and only if the minimum distance between code words is at least  $2e_c+1$ . Then if any received word has  $e_c$  or fewer errors it is possible to correct these errors.

The above performance of coding schemes is dependent upon the method of coding and the implementation of the encoder and decoder. The minimum distance defines only the limit in performance of a code, while the actual performance is dependent upon the implementation of the code.

The (15, 7) Bose-Chaudhuri code has a minimum distance of 5; thus it is capable of correcting all single and double bit errors in each 15 bit word. It also has the capability of detecting 4 bit errors, but it must be pointed out that the code may not be used simultaneously for correcting 2 bit errors and detecting 4 bit errors. Since all the code words are separated by at least 5 positions, error detection of up to 4 bits is obvious. When error correction is utilized, a word with 3 bits in error may be decoded into another word since its distance from another word may only be 2, the decoder believing it has corrected properly and assumes that no error is present. This characteristic limits the detection capability of the code. If the (15, 7) code is used for only 1 bit error correction it is then capable of using the code to simultaneously detect up to 3 bits in error. A rule to follow for combined error detection and correction is:

$$e_d + e_c < \text{minimum distance}$$

Hence, if a code is used for  $e_c$  bit error correction and  $e_d$  bit error detection, their sum must be less than the minimum distance of the code. When using the above rule it must be remembered that the error correction capability of the code must not be exceeded; thus:

$$2e_c + 1 \leq \text{minimum distance}$$

The Golay (23, 12) code has a minimum distance of 7 and may be used for 3 bit error correction or 6 bit error detection, or a combination of the two, using the aforementioned rule. Since the amount of circuitry increases quite rapidly with the degree of error correction, it may be desirable to use a more powerful code for its error detection capability than for its correction capability. Also a combination of error correction and detection may be desirable, such as correction of all single bit errors. This is fairly easy to accomplish while using the remaining capability of the code for error detection.

Predicting the performance of a code when its maximum error correcting capability is not exceeded is fairly easy using the minimum distance of the code. What happens when the maximum error correcting capability of the code is exceeded is not easily determined, but certainly is of great interest since in many cases this indeed will happen. An example of this is when a large error burst occurs. The encoder and decoder designed for the (15, 7) code were simulated on the IBM 1620 computer and its performance was evaluated. Errors in transmission were introduced in all possible positions of the transmitted word and the  $k$  information bits after error correction were checked for errors. All possible 1, 2, 3, and 4 bit error combinations were introduced and the results are tabulated in Figure 15 and 16.

The results given in Figure 15-A were obtained by introducing all single bit error combinations into the 15 bit word. Since a single error could exist in any one of the 15 bits there were 15 different error patterns. The table shows that before correction there were 8 words (each 15 bits in length) that did not contain any errors in the information bits since the errors were introduced into the check bits. The remaining 7 words had errors in the information bits. Since the desired message is the  $k$  information bits and not the check bits, only these information bits are checked for errors. Figure 15-A shows that all the errors in the information bits were corrected by the decoder.

All double bit error combinations were introduced into the 15 bit word with the results given in Figure 15-B. The results are similar to the single error case, with the decoder detecting and correcting all errors introduced into the 7 information bits. The results in Figure 15 show that the design of the (15, 7) code simulated on the computer was sound, and all single and double bit error combinations will be corrected by the decoder.

The results tabulated in Figure 16 show that all messages with 3 and 4 bit error combinations were detected as in error, but in trying to correct the errors, more errors were introduced than if the messages were accepted without correction. For an example, examine the number of messages received error free for all the 3 bit error combinations. It is observed that if

no error correction was performed 56 of the 455 messages would have been received as error free, while when correction was performed only 31 were decoded as error free. Similar results are seen with the 4 bit error combinations. Computation time on the IBM 1620 computer prevented carrying this investigation further, but the results show that the code actually makes conditions worse when the error correcting capability of the code is exceeded.

Various methods of implementing the codes are possible and they are being investigated from two viewpoints. First, the complexity of the implementation is considered as the prime factor, since if these correction devices are to be used in data transmission as practical methods of error control they must not be unwieldy to implement. Secondly, a method of implementation is desired that will easily permit the change of the code structure, such as changing from the (15, 7) code to the (23, 12) code. This factor is important since the equipment is to be used primarily in a laboratory test program.

## SECTION V

### CONCLUSIONS

Digital data transmission at bit rates from 300 to 4800 bps over the AN/VRC-12 radio set was conducted with error rates varying from  $10^{-6}$  to  $10^{-3}$  depending upon the bit rate and transmission link. The accuracy of transmission continues to be limited by impulse noise which causes a majority of the errors. It is recommended that a continuing effort be applied to find the source of these impulses in order to determine if the impulses are due to the particular locality or if some other cause is present. The tests conducted during the last quarter were mostly performed at one site. Since this has resulted in the accumulation of a limited amount of information, tests will be conducted during the next quarter to accumulate an equal amount of information from each site.

The spectra analysis conducted on the three modems presently being studied compares the three modulation techniques. The effect of pre-shaping the data before modulation is shown in the results of the Di-phase modem and has the advantage of bandlimiting the data before final amplification; thus the power applied to the line is concentrated in the spectrum used for detection. A comparison of the spectrum generated by each modem shows that for a common bit rate the Quad-phase modem generates the smallest spectrum. The Di-phase modem is next, requiring approximately twice the bandwidth of the Quad-phase modem. The FSK (AN/TYC-1, XC-2) modem is seen to require approximately 1.5 times the bandwidth compared to the Di-phase modem. It is observed that if a narrow channel is the limiting factor in a data transmission link the Quad-phase modem will permit the highest speed of transmission of the three modems discussed in this report.

The design employed in the clock recovery circuits of the multi-frequency modem utilizes completely digital techniques and standard circuits. Its advantage is that the performance of the clock recovery is not dependent upon the bit rate, since its characteristics are independent of the rate of operation. Its inherent jitter in most cases is not objectional, but it may be reduced by increasing the number of divide stages in the phase correction circuits.

The coding study has shown that error correction in many cases is the answer in improved transmission accuracy, but in most cases this is accomplished only a sacrifice of transmission rate. Since multiple error correction at this time greatly increases the circuit complexity, a combination of error detection and/or correction with the additional capability of retransmission may be the answer to obtaining very good accuracy for a minimum amount of circuitry.

SECTION VI  
PROGRAM FOR NEXT INTERVAL

Continuation of the AN/VRC-12 field tests will take place during the next quarter. Additional tests will be conducted over the selected sites in order to gain more significant results. Qualitative field tests will be initiated which will include mobile data transmission plus a study to help establish a relationship between voice and data transmission over the AN/VRC-12. Also, a study of the impulse noise that is causing a majority of the errors will be conducted.

The construction of the multi-frequency modem will be completed during the next quarter. It will be tested both at Motorola and with the error logging system at Fort Monmouth, and its performance will be included in the next Quarterly Report. The encoder and decoder will be designed, and construction of the equipments will be initiated. Both equipments will be designed using the standard logic circuits already employed in the logging circuits and modem equipment.

**SECTION VII**  
**IDENTIFICATION OF KEY PERSONNEL**

Dr. J. Cohn	Chief Engineer
W. Borman	Assistant Chief Engineer
J. Tsimbidis	Program Advisor
R. Salava	Project Engineer
N. Thomas	Field Engineer

**Summary of Man-Hours**

	11 March 1963 to 10 June 1963	Total to Date
N. Thomas	512	788
R. Salava	356	1217
J. Tsimbidis	30	272
J. Gabalis	36	36
D. Bouchard	2	2

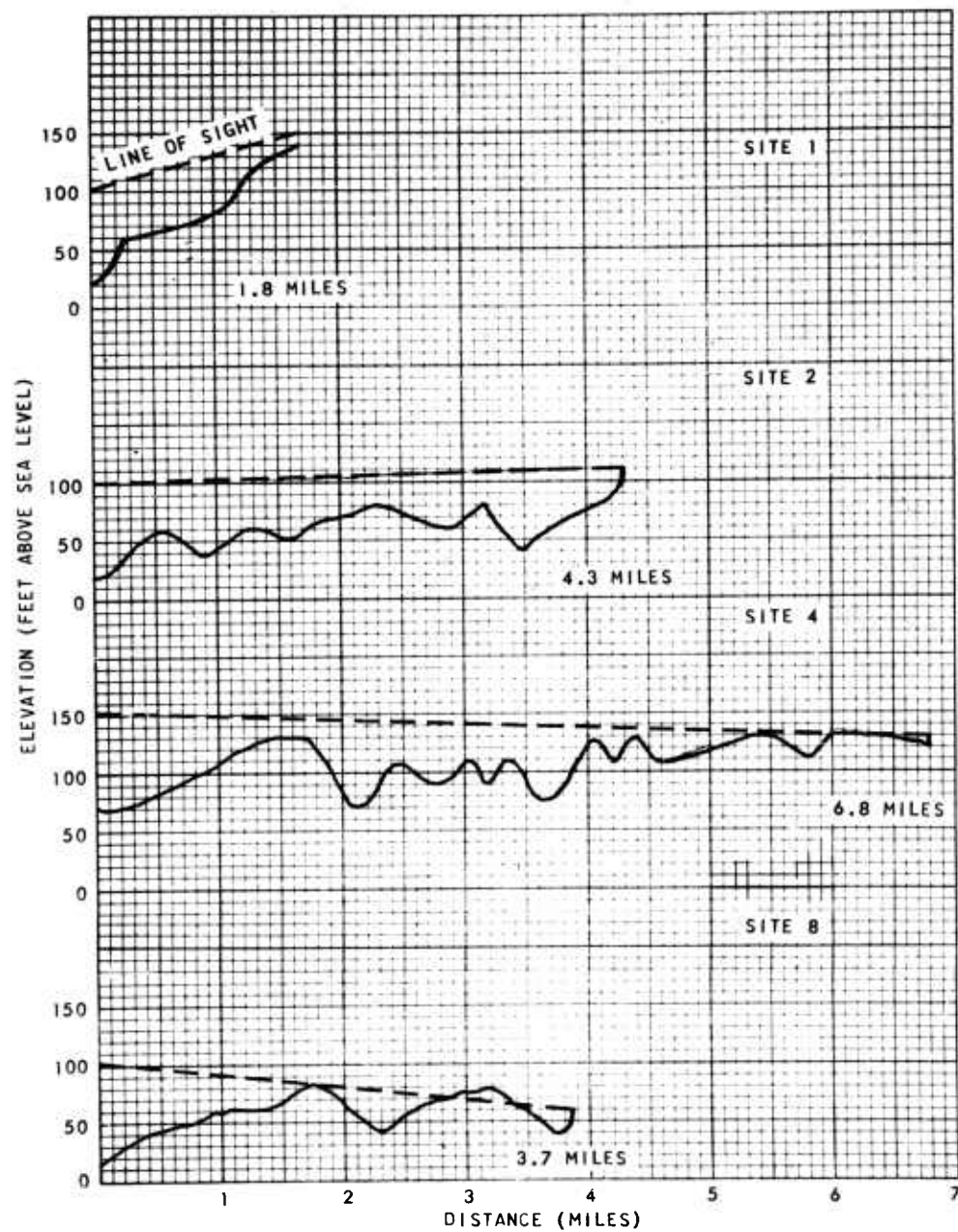


Figure 1. Transmission Map Profiles (Sites 1 to 8).

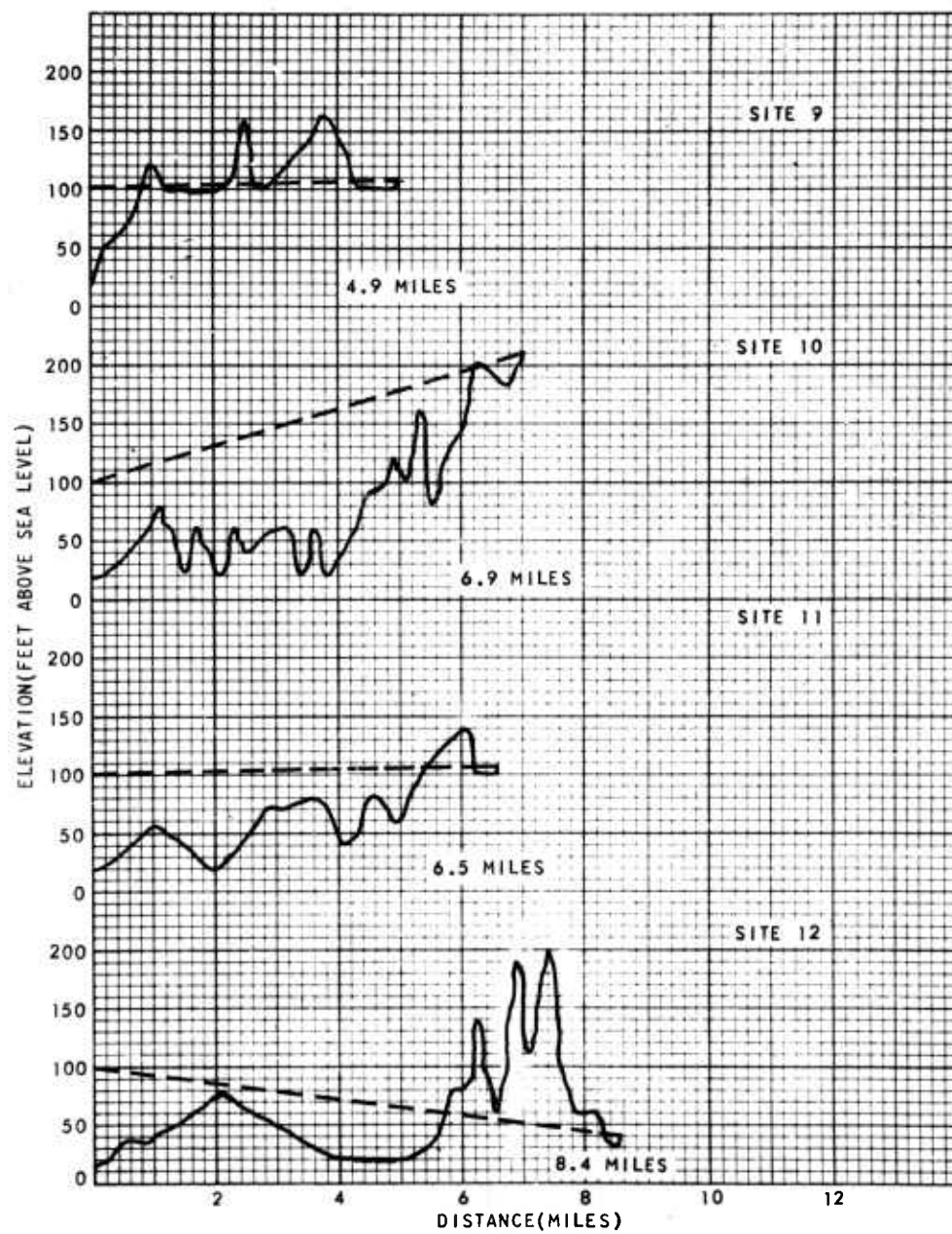


Figure 2. Transmission Map Profiles (Sites 9 to 12).

Site	Modem	Bit Rate	Bit Error Rate	Character Error Rate	No. Tests * at Site
4	Di-phase	300	$1.7 \times 10^{-3}$	$1.25 \times 10^{-2}$	2
		600	$9.49 \times 10^{-4}$	$6.53 \times 10^{-3}$	2
		1200	$6.98 \times 10^{-4}$	$3.92 \times 10^{-3}$	2
2	FSK	300	$8.33 \times 10^{-6}$	$6.67 \times 10^{-5}$	2
		600	$1.67 \times 10^{-5}$	$1.33 \times 10^{-4}$	2
		1200	$2.71 \times 10^{-5}$	$2.17 \times 10^{-4}$	2
	Di-phase	300	$1.5 \times 10^{-4}$	$1.13 \times 10^{-3}$	2
		600	$4.58 \times 10^{-5}$	$3.2 \times 10^{-4}$	3
		1200	$5.21 \times 10^{-5}$	$3.0 \times 10^{-4}$	2
10	FSK	300	$3.33 \times 10^{-5}$	$2.67 \times 10^{-4}$	10
		600	$8.42 \times 10^{-5}$	$6.53 \times 10^{-4}$	10
		1200	$4.64 \times 10^{-4}$	$3.6 \times 10^{-3}$	12
	Di-phase	300	$5.57 \times 10^{-3}$	$3.33 \times 10^{-2}$	11
		600	$9.99 \times 10^{-4}$	$4.0 \times 10^{-3}$	12
		1200	$1.48 \times 10^{-4}$	$6.85 \times 10^{-4}$	9
9	Quad-phase	4800	$3.25 \times 10^{-4}$	$6.85 \times 10^{-4}$	1
12	Quad-phase	4800	$1.94 \times 10^{-3}$	$8.38 \times 10^{-3}$	1
1	Quad-phase	4800	$1.99 \times 10^{-4}$	$8.59 \times 10^{-4}$	1
11	FSK	300	$6.12 \times 10^{-5}$	$4.9 \times 10^{-4}$	1
		600	$3.02 \times 10^{-4}$	$2.16 \times 10^{-3}$	1
	Quad-phase	4800	$6.45 \times 10^{-4}$	$2.68 \times 10^{-3}$	1
8	Quad-phase	1200	$1.62 \times 10^{-4}$	$7.89 \times 10^{-4}$	2
		2400	$1.06 \times 10^{-3}$	$5.83 \times 10^{-3}$	1
		4800	$9.41 \times 10^{-5}$	$4.3 \times 10^{-4}$	1

\* Test duration = 200 seconds

Figure 3. Average Error Rates (AN/VRC-12 Field Tests)

Modem	Bit Rate	Percent of characters in error with N bits in error	
		N = 1	N > 1
FSK	300	100.0	0
	600	96.9	3.1
	1200	97.1	2.9
Di-phase	300	85.0	15.0
	600	65.5	34.5
	1200	60.4	39.6

Figure 4-A. Distribution of Errors (AN/VRC-12 Field Tests)

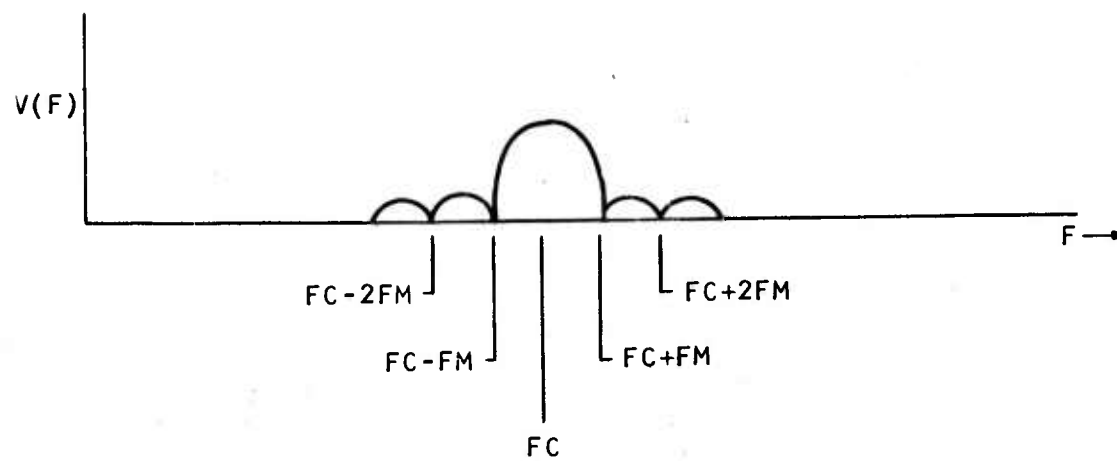
Modem	Bit Rate	Percent of Multiple errors with N bits in error						
		N =						
		2	3	4	5	6	7	8
FSK	300	0	0	0	0	0	0	0
	600	100.0	0	0	0	0	0	0
	1200	100.0	0	0	0	0	0	0
Di-phase	300	88.5	7.7	1.9	0	1.9	0	0
	600	60.0	8.0	8.0	16.0	8.0	0	0
	1200	92.8	2.4	2.4	2.4	0	0	0

Figure 4-B. Sample Distribution of Multiple Errors (AN/VRC-12 Field Tests)

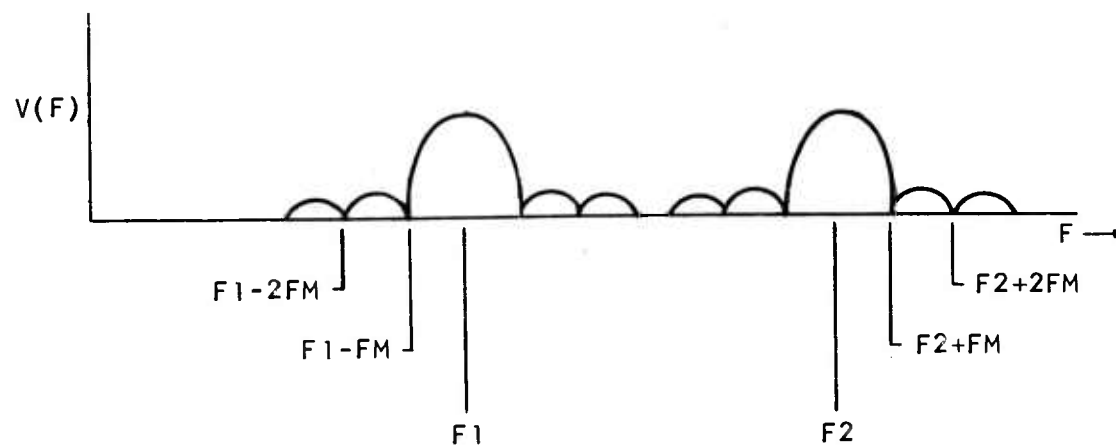
Modem	Bit Rate	Probability of Receiving a Message of Length M Error Free									
		M (seconds)									
		1	2	3	4	5	10	20	30	40	50
AN/TYC-1	300	.99	.98	.97	.96	.95	.90	.81	.74	.67	.61
	600	.96	.93	.90	.87	.85	.76	.65	.58	.52	.48
	1200	.68	.60	.51	.45	.41	.26	.13	.08	.06	.04
Di-phase	300	.69	.64	.59	.56	.53	.42	.28	.21	.16	.12
	600	.90	.87	.83	.81	.78	.68	.52	.40	.32	.24
	1200	.94	.90	.86	.82	.79	.63	.39	.22	.12	.06

Results obtained from tests conducted at site number 10

Figure 5. Probability of Receiving Error Free Message (AN/VRC-12 Field Tests)



(A) PHASE SHIFT KEYING



(B) FREQUENCY SHIFT KEYING

Figure 6. Frequency Spectra of PSK and FSK Models.

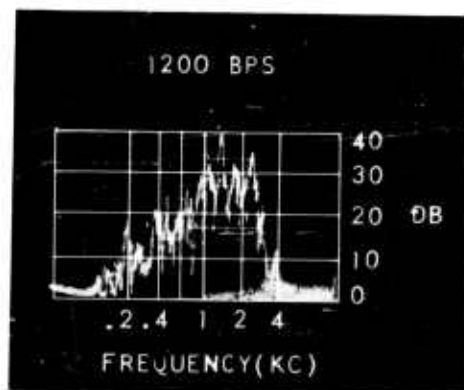
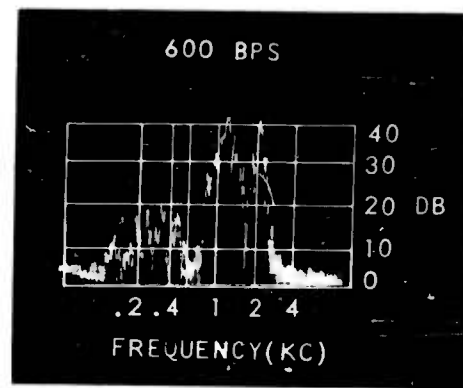
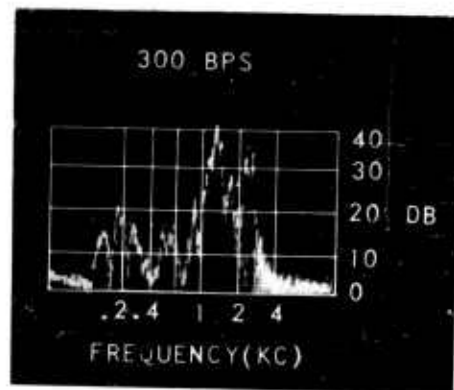


Figure 7. Frequency Spectra of the FSK Modem

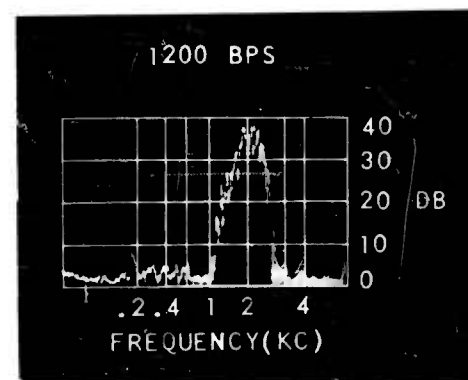
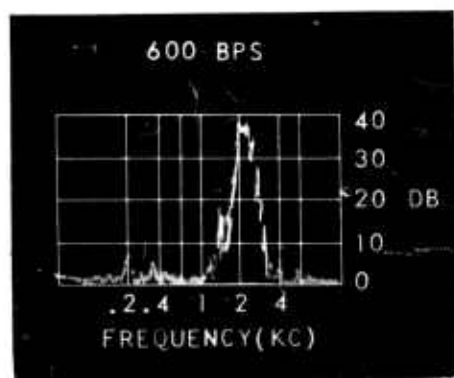
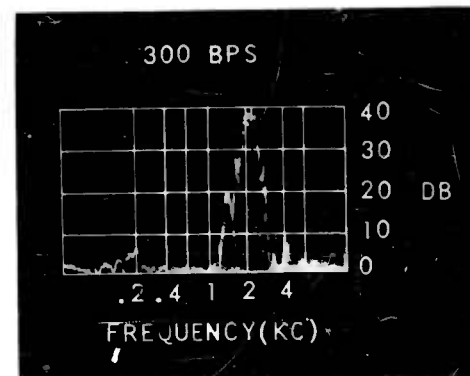
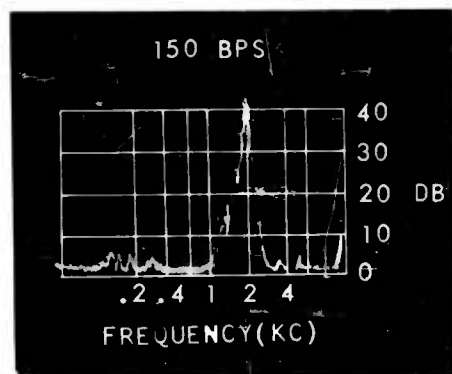


Figure 8. Frequency Spectra of the Di-Phase Modem

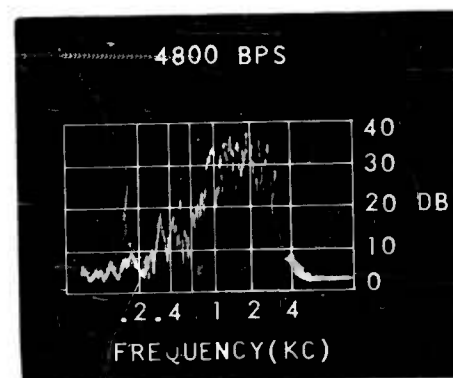
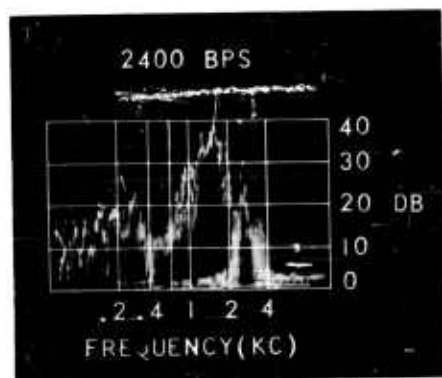
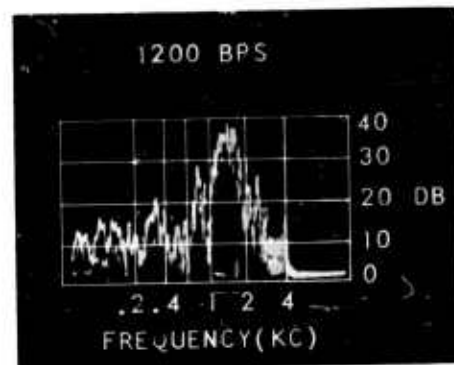
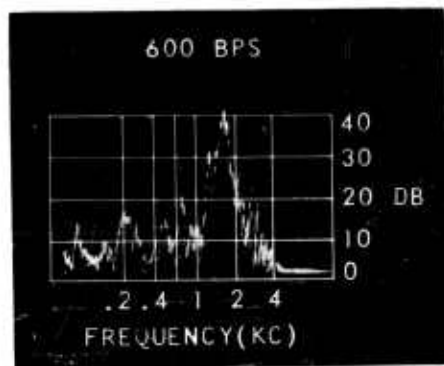


Figure 9. Frequency Spectra of the Quad-Phase Modem

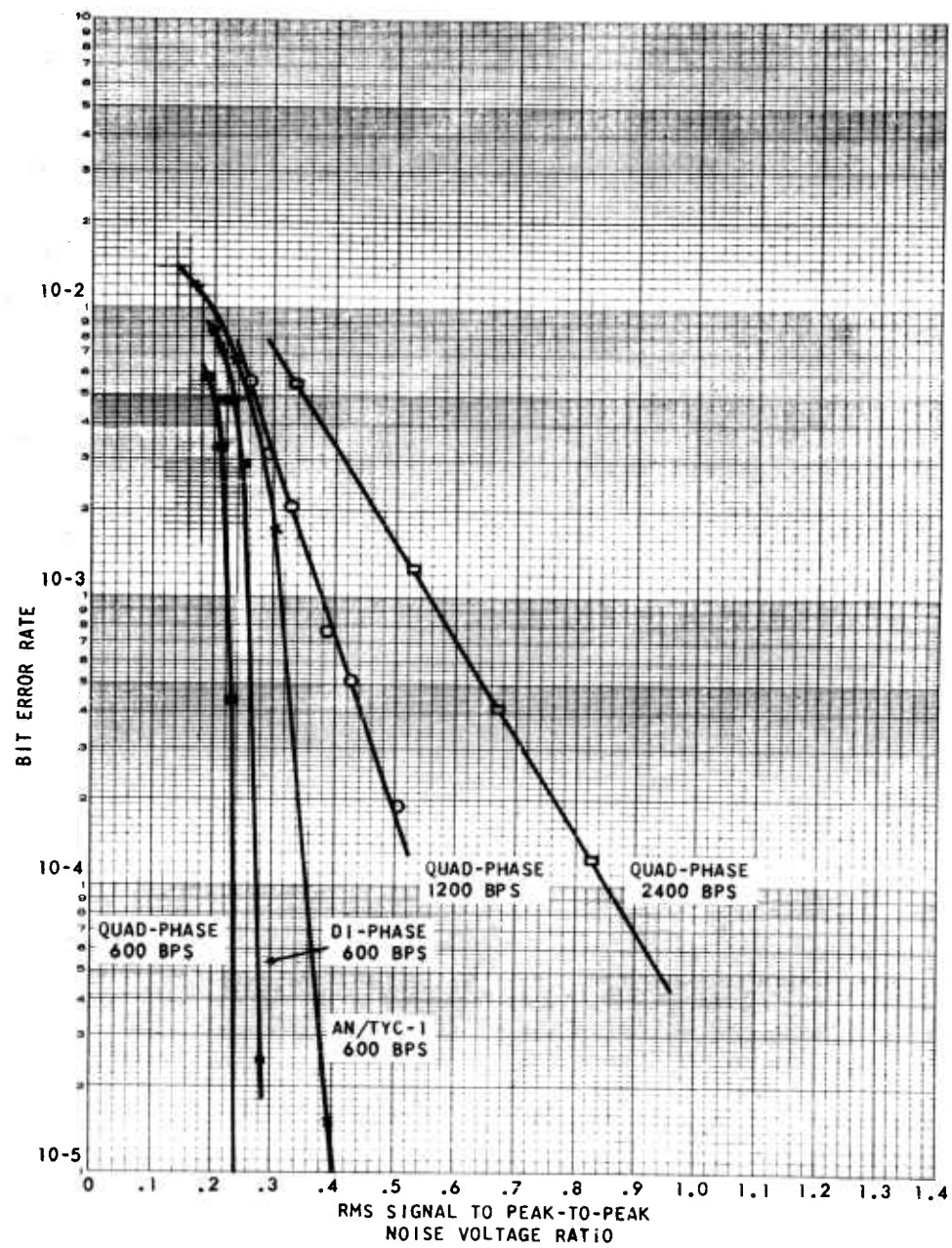


Figure 10. Impulse Noise Tests (Impulse Rate = 27 pps).

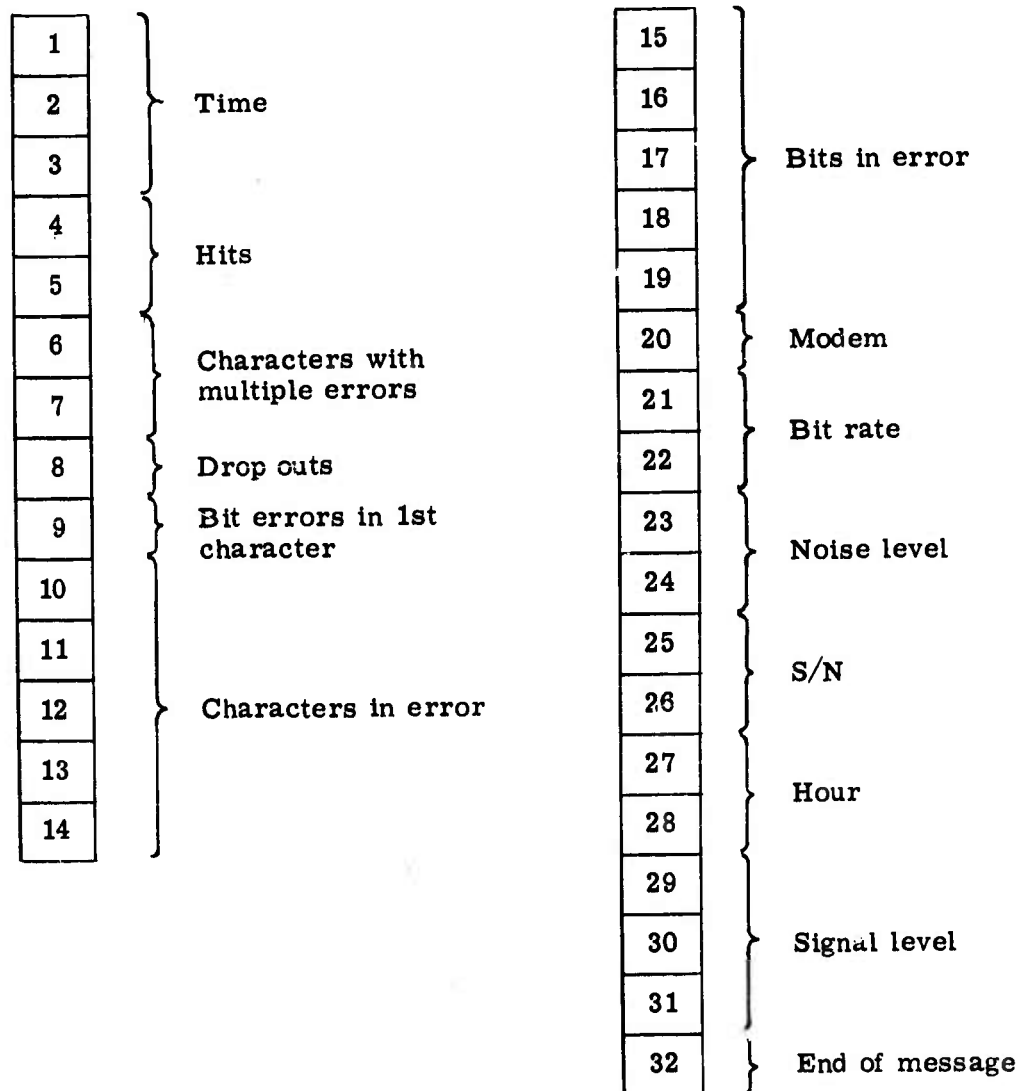


Figure 11. Paper Tape Format

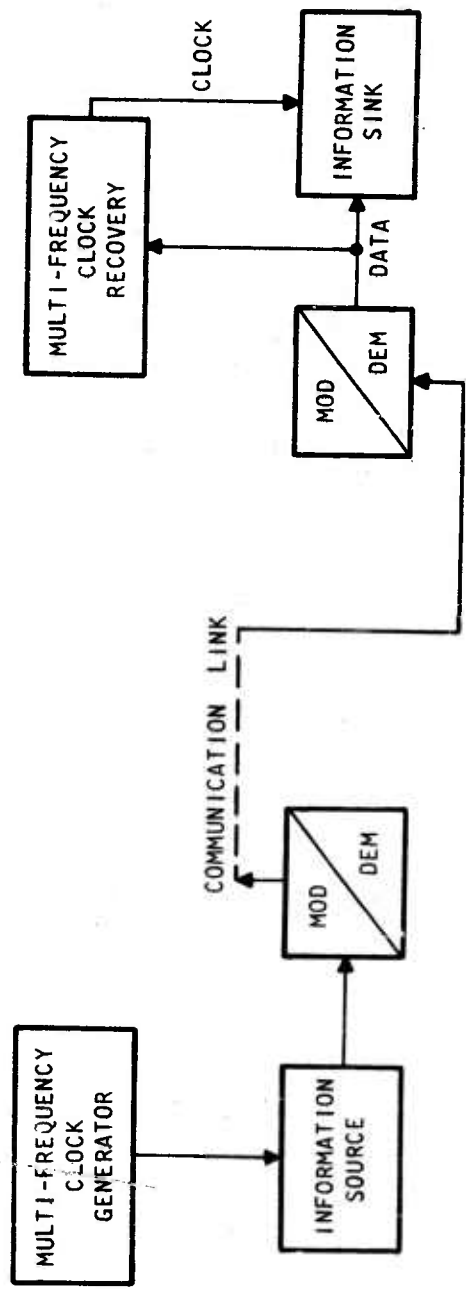
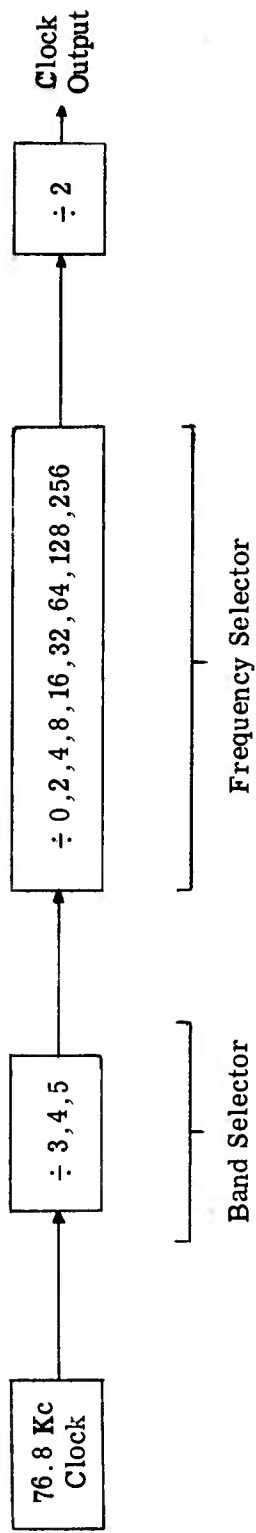


Figure 12. Multi-Frequency Modem System Block Diagram.



Band Selector	Frequency Selector									
	1 (÷256)	2 (÷128)	3 (÷64)	4 (÷32)	5 (÷16)	6 (÷8)	7 (÷4)	8 (÷2)	9 (÷0)	10*
A (÷5)	30	60	120	240	480	960	1920	3840	7680	--
B (÷4)	37.5	75	150	300	600	1200	2400	4800	9600	19.2K
C (÷3)	50	100	200	400	800	1600	3200	6400	12.8K	--

\*19.2K obtained from clock and ÷4 circuit.

Figure 13. Clock Generator

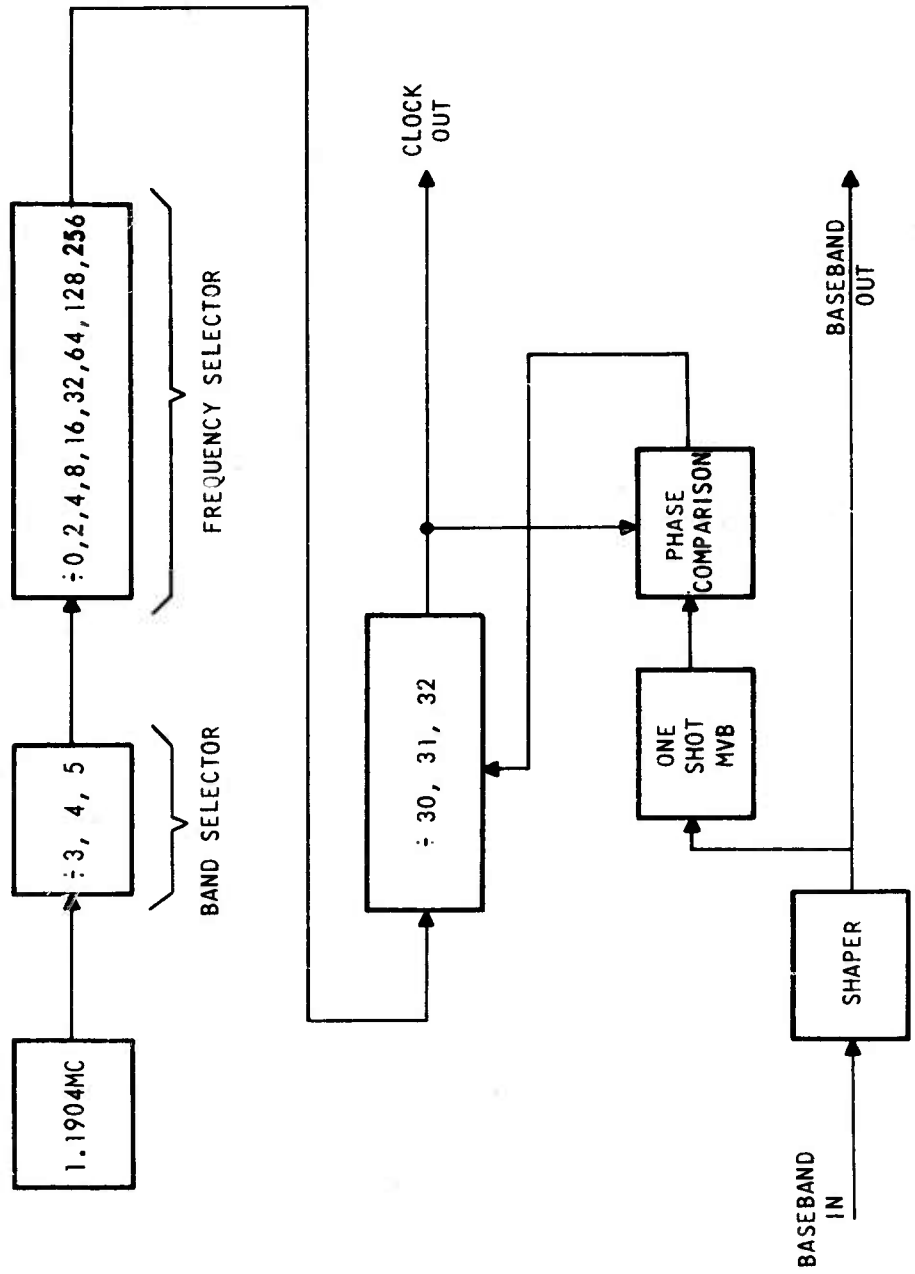


Figure 14. Clock Recovery.

		Words with j information bits in error							
j =	0	1	2	3	4	5	6	7	
Before Correction	8	7	0	0	0	0	0	0	
After Correction	15	0	0	0	0	0	0	0	

Total Error Combinations = 15

Total Error Combinations = 15

(A) All single bit error combinations introduced into the 15 bit word.

		Words with j information bits in error							
j =	0	1	2	3	4	5	6	7	
Before Correction	28	56	21	0	0	0	0	0	
After Correction	105	0	0	0	0	0	0	0	

Total Error Combinations = 105

Total Error Combinations = 105

(B) All double bit error combinations introduced into the 15 bit word.

Figure 15. Performance of 15,7 Code (Single and Double Bit Errors)

j =	Words with j information bits in error							
	0	1	2	3	4	5	6	7
Before Correction	56	196	168	35	0	0	0	0
After Correction	31	171	155	68	30	0	0	0

Total Error Combinations = 445

Total Error Combinations Detected = 455

(A) All 3 bit error combinations introduced into the 15 bit word.

j =	Words with j information bits in error							
	0	1	2	3	4	5	6	7
Before Correction	70	392	588	280	35	0	0	0
After Correction	46	286	517	389	112	15	0	0

Total Error Combinations = 1365

Total Error Combinations Detected = 1365

(B) All 4 bit error combinations introduced into the 15 bit word.

Figure 16. Performance of 15, 7 Code (3 and 4 bit errors)

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