TR-1154

DESIGN PROCEDURE FOR A TRANSISTOR RING COUNTER

Ira R. Marcus

15 October 1963

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CONTENTS

ABSTRACT 5

1. INTRODUCTION 5

2. THE RING COUNTER 5

3. DERIVATION OF DESIGN PROCEDURE 8
   3.1 Voltage Required to Shift 11
   3.2 Voltage Requirements for Turning an ON Stage OFF when Driven on Both Buses Symmetrically 12
   3.3 Design Condition to Eliminate Two Stages from Being ON at One Time 13
      3.3.1 Case I - z Resistors Have Infinite Resistance . . 14
      3.3.2 Case II - z Is Finite. 15
   3.4 High-Frequency Considerations 15
   3.5 Design Procedure. 16
      3.5.1 Design Example 1: A Low-Power, Low-Frequency, Counter 18
      3.5.2 Design Example 2: A High-Speed Counter 19

ABSTRACT

A design procedure for the transistor ring counter is derived. Using this procedure a 30-μw decade ring counter and a 500-kc decade ring counter were built. Both operated satisfactorily.

1. INTRODUCTION

Digital electronic timers and programmers require countdown circuits to accumulate time base pulses. When the countdown circuits are in the proper state, logic circuits give out output signals. Transistor ring counters are one type of countdown circuit. Reference 1 describes a particular type of transistor ring counter circuit that appears to be useful in many applications. No design procedure is known to be published that would enable the circuit to be adapted for use under various conditions. The purpose of this report is to derive a design procedure for this circuit and to analyze it so that its performance is predictable.

A transistor ring counter is a series of identical stages connected in a ring. A stage of the ring counter to be analyzed is shown in figure 1. The chief advantage of this circuit for ordnance applications is its low power capability. In one of the examples demonstrating the design procedure, a 10-stage ring counter was built that required only 30 μw for operation from -55^{o} to $+75^{o}$C. Another advantage of the ring counter is that no matrix is required to read out the information in the counter. A disadvantage, compared with binary counting, is that the ring counter requires more components to divide by a given number. When extensive counting or division is required, one of the stages of the ring is used as an output to feed another ring. This cascading may be repeated as many times as required. In some cases a simple buffer driver is required between rings.

2. THE RING COUNTER

Figure 1 shows a single stage of the ring counter being considered. When both transistors are not conducting, the circuit is stable since the base-emitter junction of both the NPN and PNP transistors are not forward biased. When both transistors are conducting, both base-emitter junctions are forward biased and the circuit is stable. Partial conduction is not a stable condition, and the stage is either ON or OFF; therefore the stage is a two-stage device. The z resistors are used to provide low-resistance base-to-emitter paths for transistors that require this condition to suppress excessive leakage at elevated temperatures.

Figure 2 shows how the single stages may be connected to form a ring counter. The emitters of all the NPN transistors share a common emitter resistor p_1. Similarly, the emitters of all the PNP transistors share a common resistor of identical value p_2. The purpose of these resistors is to insure that only one stage is ON at any one time. When one stage is ON, the voltage drop across these resistors back-biases all the junctions of the remaining transistors and holds them all OFF. A

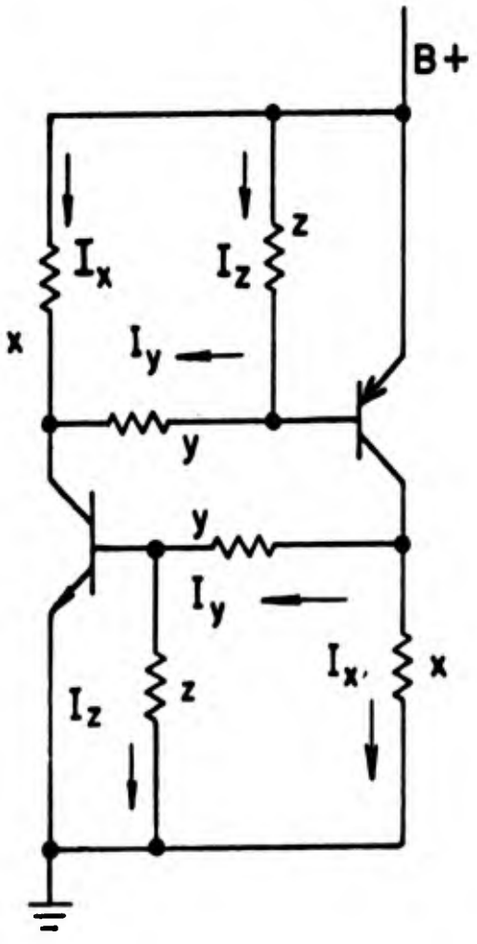


Figure 1. Ring counter stage.

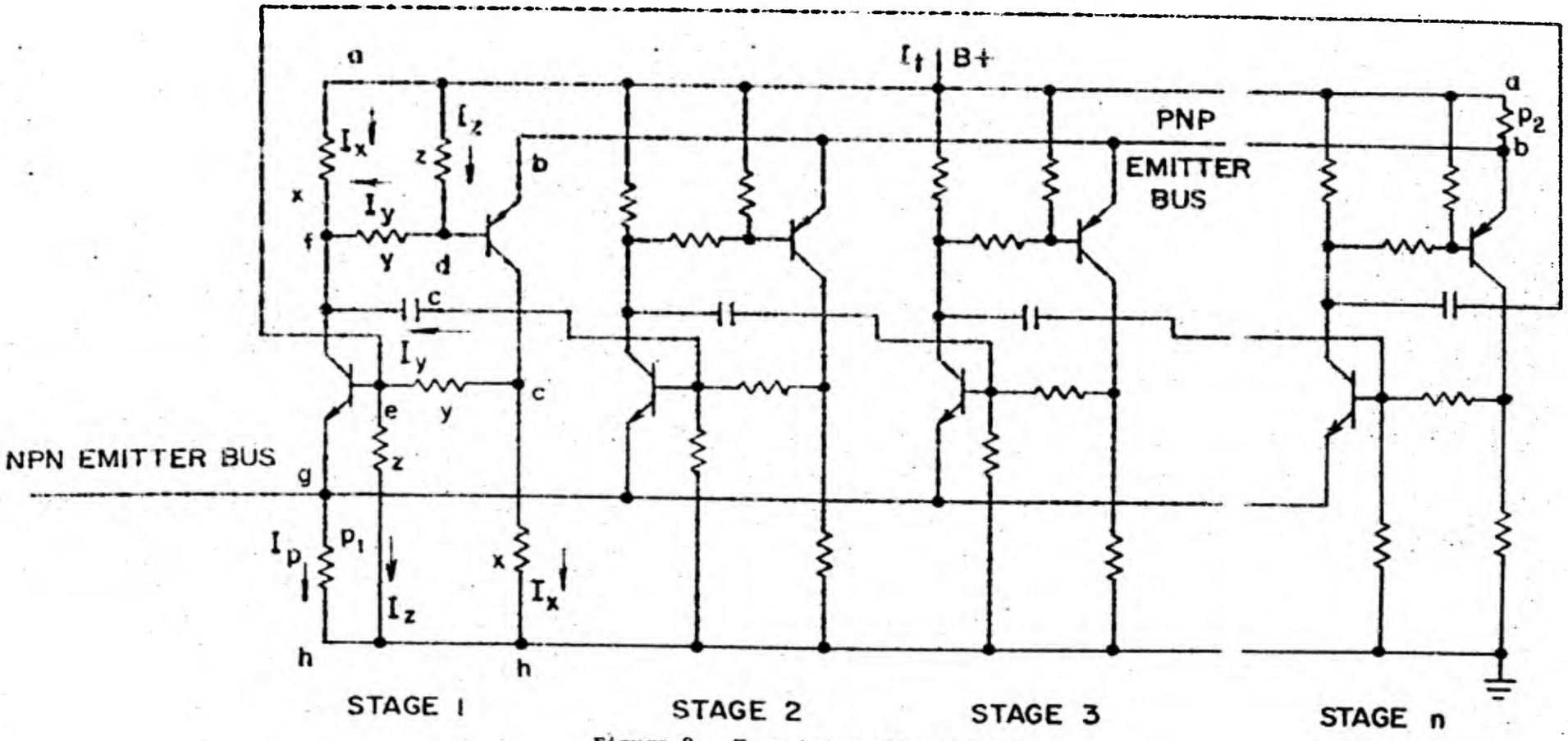


Figure 2. Transistor ring counter.

shift register may be made by deleting both resistors and allowing more than one stage to be ON at one time. The stages are coupled by a capacitor between either collector of stage r and the base of the corresponding transistor of stage r + 1. Moving the position of the ON stage within the ring is accomplished by turning the ON stage OFF and allowing the next stage to be pulsed ON by the coupling capacitor. This may be done by putting a positive shift pulse on the emitter bus line of the NPN transistors, or a negative pulse on the emitter bus line of the PNP transistors, or both simultaneously. The only restriction is that the coupling pulse be longer than the shift pulse. If the coupling pulse is not longer than the shift pulse, all stages are turned OFF and remain OFF.

The stage to be set ON may be turned ON by either grounding the collector of the NPN transistor or applying B+ to the collector of the PNP transistor. Figure 3 shows simple circuits to accomplish this.

3. DERIVATION OF DESIGN PROCEDURE

Only one stage of the transistor ring counter (fig. 2) is ON. Values I_x, I_y, I_z, and I_p are solved in terms of I_t, where I_t is the total counter current. Due to symmetry, the following equations apply to both the NPN and PNP transistors.

$$I_c = I_x + I_y \tag{1}$$

$$I_b = I_y - I_z \tag{2}$$

$$B = \frac{I_c}{I_b} \tag{3}$$

where

I_c = collector current

I_b = base current

B = the minimum value of H_{FE} of the transistor under all operating conditions.

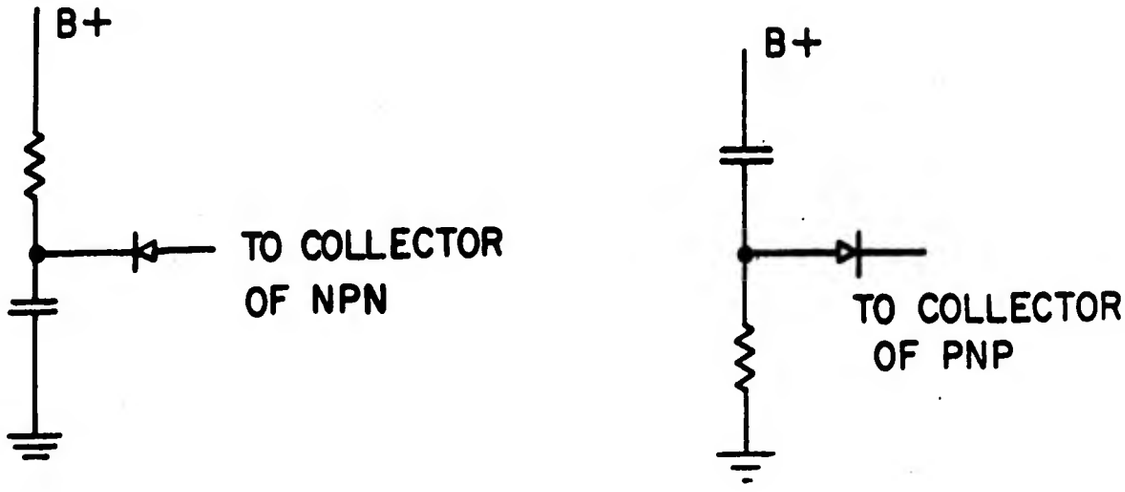
From equations (1), (2), and (3)

$$B = \frac{I_x + I_y}{I_y - I_z} \tag{4}$$

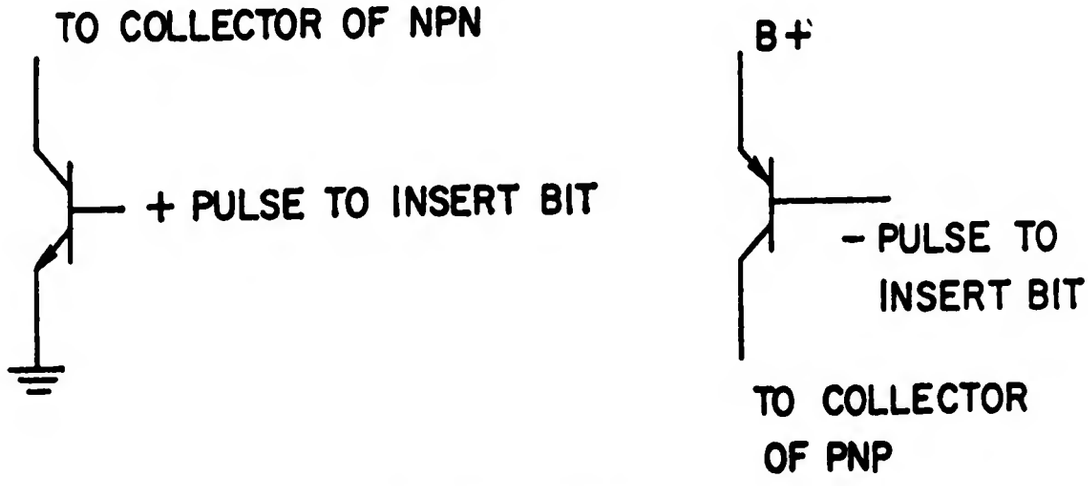
$$I_p = I_c + I_b$$

$$I_p = I_x + 2I_y - I_z \tag{5}$$

$$I_t = I_x + I_z + I_p \tag{6}$$



ACTIVATED WHEN B+ IS APPLIED



ACTIVATED ON PULSE COMMAND

Figure 3. Some methods of bit insertion.

If

$$A = \frac{I_z}{I_y} \tag{7}$$

then from equations (4) and (7)

$$B = \frac{I_x + I_y}{I_y(1 - A)} \tag{8}$$

From equations (5) and (7)

$$I_p = I_x + I_y(2 - A) \tag{9}$$

From equations (6) and (7) solving for I_p

$$I_p = I_t - I_x - AI_y \tag{10}$$

Equating equations (9) and (10)

$$I_x + I_y(2 - A) = I_t - I_x - AI_y$$

$$I_x = \frac{I_t}{2} - I_y \tag{11}$$

Solving for I_x, I_y, I_z and I_p in terms of B, I_t, and A, we obtain from equations (4), (7), and (11)

$$I_y = \frac{I_t}{2(1-A)B} \tag{12}$$

From equations (11) and (12)

$$I_x = \frac{I_t\,(B-BA-1)}{2B(1-A)} = \frac{I_t}{2}\left[1 - \frac{1}{B(1-A)}\right] \tag{13}$$

From equations (9), (12), and (13)

$$I_p = \frac{I_t\,(1+B)}{2B} = \frac{I_t}{2}\quad 1 + \frac{1}{B} \tag{14}$$

From equations (7) and (12)

$$I_z = \frac{AI_t}{2B(1-A)} \tag{15}$$

Thus by choosing I_t, B, and A, we determine I_x, I_y, I_z and I_p.

3.1 Voltage Required to Shift

Consider the condition when V_{gh} is raised by an external driver to V_T (fig. 2) so that the NPN transistor is on the threshold of going OFF, and the base current of the NPN transistor is close to the minimum value that will keep the NPN transistor in saturation. The PNP transistor is still ON. In this condition, all voltages that have substantially changed from the normally ON condition are indicated by the use of the letter E.

$$V_{ah} - E_{ab} - V_{bc} - E_{ch} = 0 \tag{16}$$

$$E_{ch} = E_{ce} + E_{eh} \tag{17}$$

$$E_{eh} = V_{eg} + V_T \tag{18}$$

From equations (16), (17), and (18)

$$V_{ah} - E_{ab} - V_{bc} - E_{ce} - V_{eg} = V_T \tag{19}$$

If V_T is raised to $V_{ah} - V_{bc} - V_{eg}$ so that

$$V_T = V_{ah} - V_{bc} - V_{eg} \tag{20}$$

then E_{ce} and E_{ab} equal zero, and the stage is turned OFF.

If the drive pulse is capacitively coupled to point g then

$$V_T = V_{gh} + V_{drive} \tag{21}$$

From equations (20) and (21)

$$V_{ah} - V_{bc} - V_{eg} - V_{gh} = V_{drive} \tag{22}$$

Since

$$V_{ah} - V_{ab} - V_{bc} - V_{ce} - V_{eg} - V_{gh} = 0 \tag{23}$$

when the stage is normally ON and $V_{ab} = V_{gh}$, then rearranging equation (23) we obtain

$$V_{ah} - V_{bc} - V_{eg} - V_{gh} = V_{ce} + V_{gh} \tag{24}$$

Equating (22) and (24)

$$V_{drive} = V_{ce} + V_{gh} \tag{25}$$

V_{drive} is the voltage required at point g to shift the "one" (ON equals "one") from one stage to the next. We now show that V_{drive} can be obtained from a prior ring. If point C is the takeoff point from one ring and is capacitively coupled to a second ring for driving, then V_{ch} is the driving voltage. V_{ch} is always greater than $V_{ce} + V_{gh}$, the required driving voltage, and thus one ring can always supply the required voltage to drive another ring.

3.2 Voltage Requirements for Turning an ON Stage OFF when Driven on Both Buses Symmetrically

When a single stage is ON (fig. 2) the potential at point b is

$$V_{bh} = V_{ah} - V_{ab} \tag{26}$$

The potential at point f is

$$V_{fh} = V_{fg} + V_{gh} \tag{27}$$

The ring counter is driven on both the NPN and the PNP emitter buses. The potential at point g rises, and the potential at point b falls. The change in potential at point f is the same as that at point g. If the potential at point b is lowered and the potential at point f is raised simultaneously by the same amount Q, and if E represents the voltage at a point that has changed substantially from the normally ON condition then

$$E_{bh} = V_{ah} - V_{ab} - Q \tag{28}$$

and

$$E_{fh} = V_{fg} + V_{gh} + Q \tag{29}$$

If Q is raised so that the stage is turned OFF then

$$E_{fh} + V_{bd} \geq E_{bh} \tag{30}$$

since the PNP transistor has its base-to-emitter junction back-biased. Substituting equations (28) and (29) into equation (30)

$$V_{fg} + V_{gh} + Q + V_{bd} \geq V_{ah} - V_{ab} - Q \tag{31}$$

Thus

$$2Q \geq V_{ah} - V_{ab} - V_{fg} - V_{gh} - V_{bd} \tag{32}$$

V_{fg} equals V_{bc} and V_{bd} equals V_{eg} for most NPN and PNP transistors when operated under similar conditions. Equation (32) becomes

$$2Q \geq V_{ah} - V_{ab} - V_{bc} - V_{gh} - V_{eg} \tag{33}$$

However,

$$V_{ah} - V_{ab} - V_{bc} - V_{eg} - V_{gh} = V_{ce}$$

Thus equation (33) becomes

$$Q \geq \frac{V_{ce}}{2}$$

Now, if both points g and b are pulsed by an external driver and the pulse is capacitively coupled to these points, then the minimum voltage required to shift is $V_{ce}/2$.

3.3 Design Condition to Eliminate Two Stages from Being ON at One Time

Assume two stages are ON simultaneously (fig. 2). Voltages and currents which have substantially changed from the single ON stage condition are indicated by the letters E and i respectively. Let the emitter resistor p_1 equal resistor p_2. Then

$$V_{ah} = E_{ab} + V_{bc} + E_{ch} \tag{34}$$

$$E_{ch} = E_{ce} + E_{eh} \tag{35}$$

and

$$E_{eh} = V_{eg} + E_{gh} \tag{36}$$

From equations (34), (35), and (36)

$$V_{ah} = E_{ab} + V_{bc} + E_{ce} + V_{eg} + E_{gh} \tag{37}$$

and since E_{ab} equals E_{gh} by symmetry, then

$$E_{gh} = \frac{V_{ah} - V_{bc} - E_{ce} - V_{eg}}{2} \tag{38}$$

i_p is the sum of the currents at point g when two stages are ON simultaneously. By symmetry i_p is also the sum of the currents at point b when two stages are ON.

By inspection

$$i_p = 2i_x + 4i_y - 2i_z \tag{39}$$

Substituting equation (47) into (46), we obtain

$$I_x = \frac{I_x(V_{ah} - V_{bc} + V_{eg})}{2(V_{ah} - V_{bc} - pI_p)} \tag{48}$$

Substituting equation (42) into equation (48) and solving for p, we obtain

$$p = \frac{(V_{ah} - V_{bc} - V_{eg})(V_{ah} - V_{bc})}{2I_x(V_{ah} - V_{bc} + V_{eg}) + I_p(V_{ah} - V_{bc} - V_{eg}} \tag{49}$$

p is determined in terms of B+, the transistor parameters V_{bc} and V_{eg} and the currents previously determined I_x and I_p. This value of p or greater will prevent two stages from being ON simultaneously.

3.3.2 Case II - z Is Finite

If z is finite, the value for p derived in case I is higher than that required to keep two stages from being ON at one time, because the added z shunts base current and lowers the base voltage tending to shut the transistors off. In general, z is high compared with y. (A is low, below 0.2.) In this case the value for p derived in case I is adequate. The case where z is comparable to y is not considered because (a) low-leakage transistors are presently available and therefore do not require low values of z, (b) a high value of A is poor design practice since a high percentage of available base current is shunted to ground, and (c) a precise analytic expression for p is not easily derived. If for any reason a large value of A is desired, p is best determined by experiment, using transistors having the highest gain normally expected of the transistor type.

3.4 High-Frequency Considerations

The choice of the maximum value for the coupling capacitor depends upon the highest operating frequency, since the base of stage r + 1 is pulsed negative when stage r is turned ON (fig. 5). The coupling capacitor between these two stages discharges through the NPN transistor of stage r and p_1, and through the series-parallel combination of x, y, and z resistors of stage r + 1, yielding a combined resistance of

$$\frac{(x + y)z}{x + y + z} + p \tag{50}$$

This negative pulse must decay before the next drive pulse occurs. The minimum period should be greater than one time constant; therefore

$$\frac{1}{f} > \left[\frac{(x + y)z}{x + y + z} + p\right] c \tag{51}$$

$$i_p p = E_{gh} = p(2i_x + 4i_y - 2i_z) \tag{40}$$

Equating equations (38) and (40) yields

$$V_{ah} - V_{bc} - E_{ce} - V_{eg} = p(4i_x + 8i_y - 4i_z) \tag{41}$$

All the circuit components are fixed except both p resistors, which are increased until the base currents are close to zero, but the transistors are still saturated. Any further increase in p will allow only one stage to be ON at a given time. We have thus determined the value of p that prevents two stages from being ON simultaneously.

3.3.1 Case I - z Resistors Have Infinite Resistance

If z becomes infinite, i_z equals zero; i_y equals zero and E_{ce} equals zero, since p has been increased to the maximum value that will allow two stages to be ON simultaneously. Equation (41) becomes

$$p = \frac{V_{ah} - V_{bc} - V_{eg}}{4i_x} \tag{42}$$

The value of the x resistors is determined when only a single stage is ON and by inspection

$$x = \frac{V_{ah} - pI_p - V_{bc}}{I_x} \tag{43}$$

When both stages are ON

$$i_x = \frac{E_{ch}}{x} \tag{44}$$

and

$$E_{ch} = V_{ah} - E_{ab} - V_{bc} \tag{45}$$

Substituting equations (43) and (45) into (44)

$$I_x = \frac{I_x(V_{ah} - E_{ab} - V_{bc})}{(V_{ah} - V_{bc} - pI_p)} \tag{46}$$

Since E_{ab} equals E_{gh} by symmetry and E_{ce} equals 0, equation (38) becomes

$$E_{ab} = \frac{V_{ah} - V_{bc} - V_{eg}}{2} \tag{47}$$

and if z is infinite

$$\frac{1}{f} > (x + y + p)c \qquad (52)$$

When high-frequency operation is required, the stage shown in figure 1 is modified to that shown in figure 4. D1 shorts out the x, y, and z resistors, thus reducing the discharge time of the coupling capacitor. R allows C to discharge to ground beyond the threshold value of D1. D2 is used to isolate the base of the NPN transistor of the following stage from the loading effects of R. The time constant is now approximately Cp. The transistor parameters also determine the upper frequency limit of operation. Factors such as the turnon time, the turnoff time, and the storage time are the primary limiting parameters. High-speed operation is aided by driving on both emitter buses simultaneously. It may be possible to further increase speed by adding PNP to PNP coupling capacitors and speedup networks.

3.5 Design Procedure

(1) Compute I_x, I_y, I_z and I_p from

$$I_x = \frac{I_t}{2}\left[1 - \frac{1}{B(1 - A)}\right]$$

$$I_y = \frac{I_t}{2(1-A)B}$$

$$I_z = \frac{AI_t}{2B(1 - A)}$$

$$I_p = \frac{I_t}{2}\left[1 + \frac{1}{B}\right]$$

I_t is the total current. B is the minimum expected value of the d-c gain of the transistor under all operating conditions. A is the ratio of I_z to I_y and is a function of transistor leakage.

(2) Compute the minimum value of p; p may be made equal to zero if the requirement that only one stage be ON at one time is not necessary.

$$p = \frac{(V_{ah} - V_{bc} - V_{eg})(V_{ah} - V_{bc})}{2I_x(V_{ah} - V_{bc} + V_{eg}) + (I_p(V_{ah} - V_{bc} - V_{eg})}$$

V_{bc} and V_{eg} are transistor parameters.

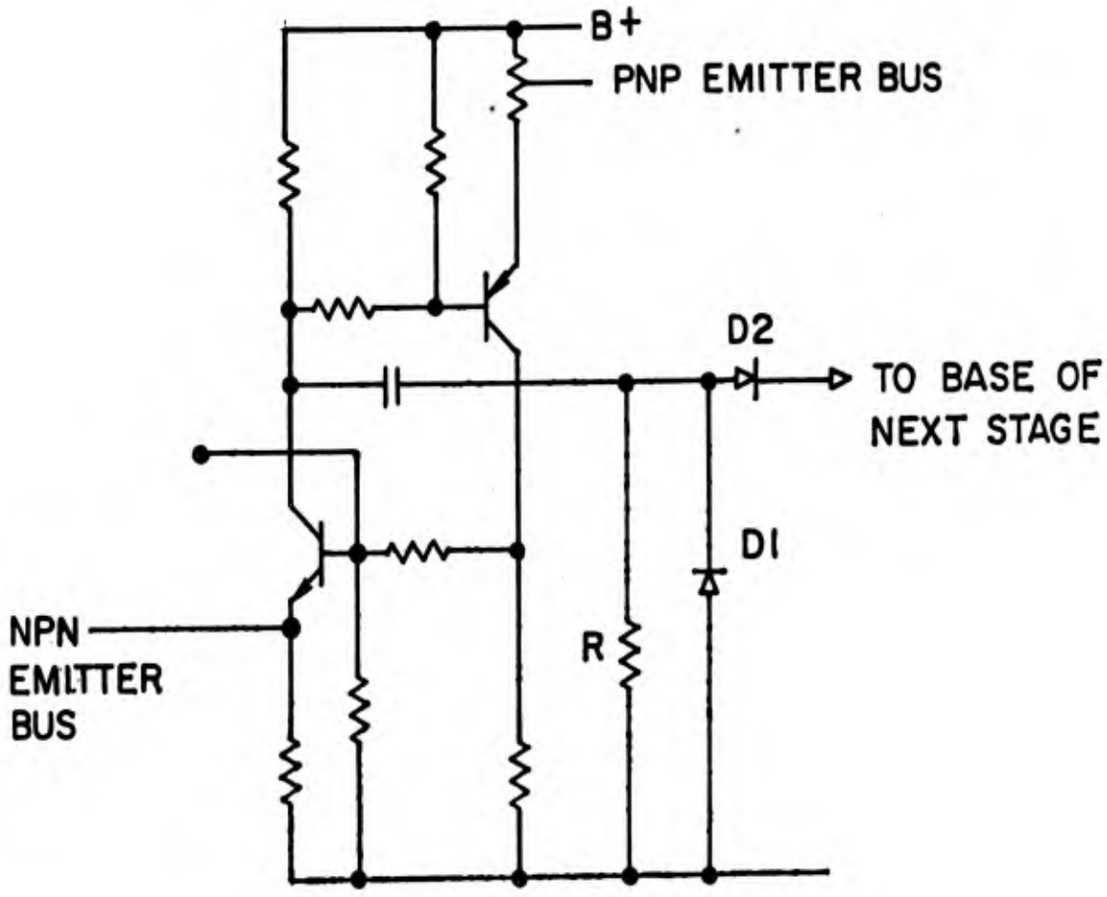


Figure 4. High-frequency stage.

(3) Compute V_{ab} from

$$V_{ab} = pI_p$$

(4) Compute x from

$$x = \frac{V_{ah} - V_{ab} - V_{bc}}{I_x}$$

(5) Compute y from

$$y = \frac{xI_x - V_{eg} - V_{gh}}{I_y}$$

using the value computed for V_{ab} in steps 3 for V_{gh}, since V_{ab} equals V_{gh}.

(6) Compute z, if required, from

$$z = \frac{V_{eg} + V_{gh}}{I_z}$$

(7) Choose the highest operating frequency and determine the maximum value of c from

$$c = \frac{1}{f\left[\frac{(x + y)\, y}{x + y + z} + p\right]}$$

if z is finite or

$$c = \frac{1}{f(x + y + p)}$$

if z is infinite.

3.5.1 Design Example 1: A Low-Power, Low-Frequency, Counter

(1) Transistors 2N2523 (NPN) and 2N2604 (PNP) were selected because of their low leakage and high gain at low collector currents. An I_t of 10 μa was chosen. From the properties of the transistors, B was determined to be 10 and A to be zero. The values of I_x, I_y, I_z and I_p were then computed to be 4.5, 0.5, 0.0, and 5.5 μa, respectively.

(2) It was required that no two stages be ON at any one time. Therefore the minimum permitted value of p was to be computed. A supply voltage of 3 v was chosen and from the

transistor specifications, V_{bc} was determined to be 0.1 v and V_{eg} to be 0.6 v. The minimum value of p was computed to be 150,000.

(3) V_{ab} was computed to be 0.825 v.

(4) The value of x was computed to be 460,000 ohms but 470,000 ohms was selected since that is the nearest standard value available.

(5) The value of y was computed to be 1.38 meg but 1.5 meg was selected -- again the nearest standard value available.

(6) Since I_z equals zero, the z resistor is not required.

(7) A maximum operating frequency of 100 cps was chosen and the maximum value of c was computed to be equal to 0.0047 μf. A value of 0.002 μf was selected.

Table I shows the performance of this design, and figure 5 displays various waveforms of this ring counter.

3.5.2 Design Example 2: A High-Speed Counter

(1) Transistors 2N2523 (NPN) and 2N2604 (PNP) were selected because of their high switching speeds. An I_t of 20 ma was chosen, and from the properties of the transistors, B was determined to be 10 and A to be zero. The values of I_t, I_y, I_z, and I_p were computed to be 9, 1, 0, and 11 ma.

(2) It was required that no two stages be ON at any one time. Therefore, the minimum permitted value of p was to be computed. A supply voltage of 6 v was chosen, and from the transistor specifications V_{bc} was determined to be 0.3 v and V_{eg} to be 0.6 v. The minimum value of p was computed to be 173 ohms; 180 ohms was used in the model.

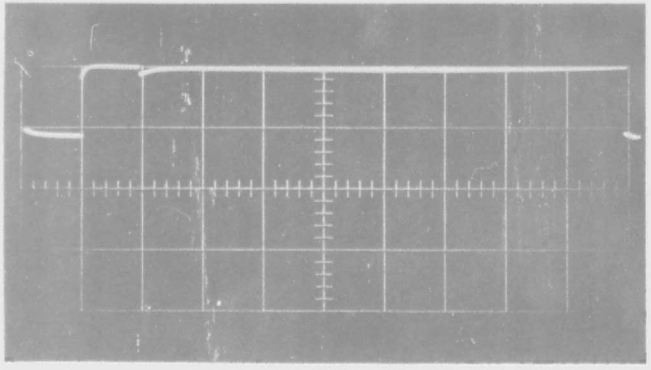
(3) V_{ab} was computed to be 2.0 v.

(4) The value of x was computed to be 410 ohms but 430 ohms was selected since that is the nearest available value.

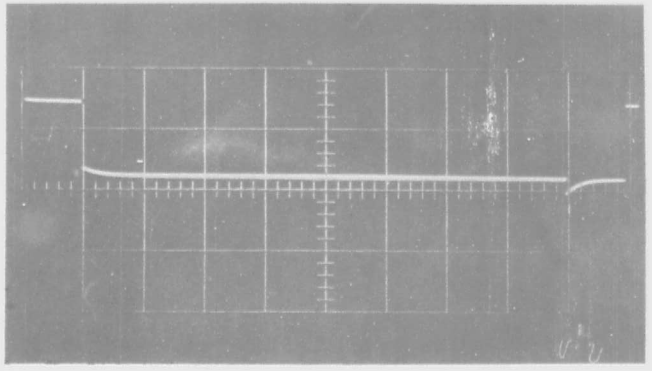
(5) The value of y was computed to be 1270 ohms but 1500 ohms was selected (the nearest value available).

(6) Since I_z equals zero, the z resistor is not required.

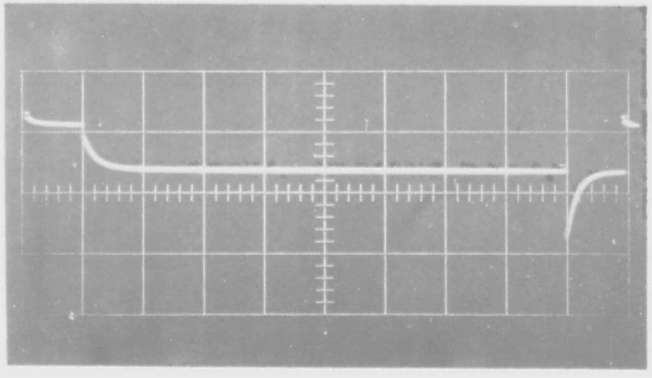
(7) A maximum operating frequency of 500 kc was desired. The speedup network shown in figure 4 was used. D1 and D2 are computer diodes, type GMD-1. The value of R is five to ten times the value of y. The value chosen for R is 10,000 ohms.



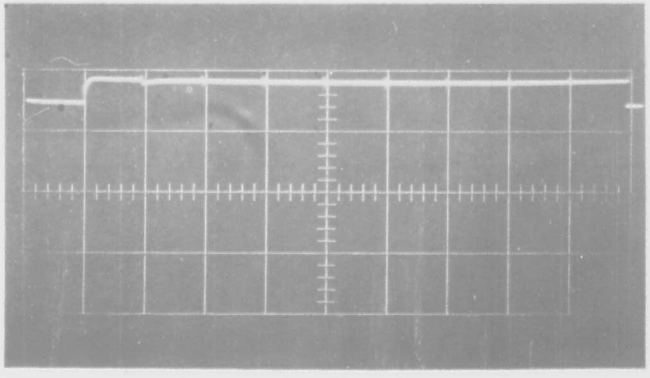
Collector NPN



Collector PNP



Base NPN



Base PNP

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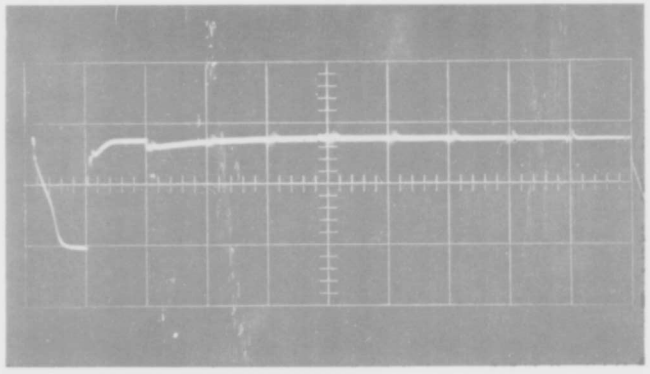
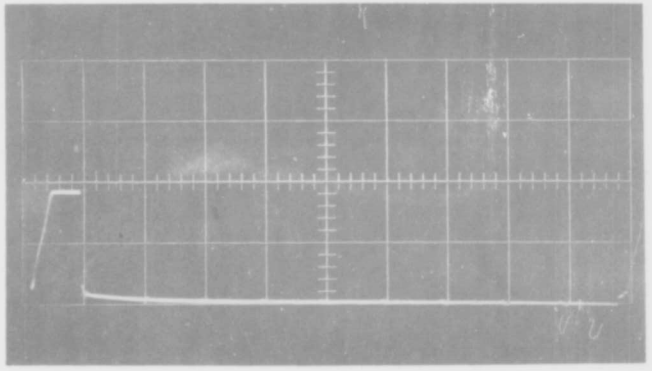
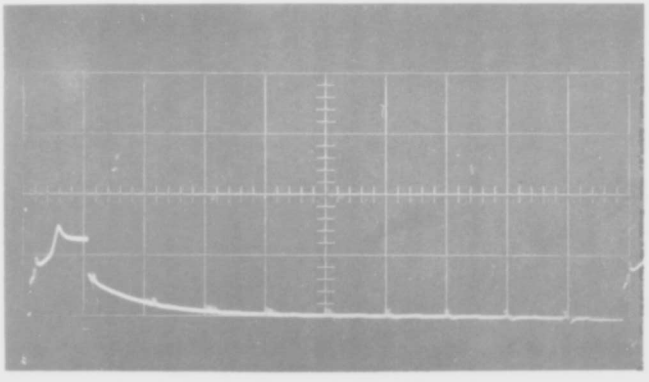
Figure 5. Waveforms of low-power ring counter.
(Horizontal, 0.01 sec/cm; vertical, 2 v/cm)



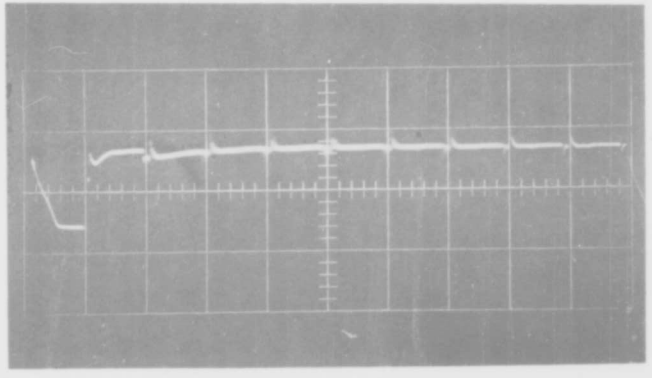
Collector NPN



Collector PNP



Base NPN



Base PNP

554-63

Figure 6. Waveforms of high-speed ring counter.
(Horizontal, 2 μs/cm; vertical, 2 v/cm)

Since cp equals 2 μsec, c equals 0.011 μf. The value selected for the model is 0.001 μf. Figure 6 shows waveforms of this decade ring counter at 500 kc. Drive pulses were supplied to both buses simultaneously.

TABLE I. PERFORMANCE OF LOW-POWER RING COUNTER

(All measurements at 100 cps)

	B+		
	2.5 v	3 v	4.5 v
At room temperature			
Min width of drive (μs)	110	64	50
Max width of drive (μs)	1200	1800	800
Current (μa)	7.5	10	13.5
Min drive voltage (v)	0.25	0.4	0.5
Max drive voltage (v)	2	2	3
At 75°C			
Min width of drive (μs)	120	70	65
Max width of drive (μs)	450	0	480
Current (μa)	7.5	9	13.5
Min drive voltage (v)	0.25	0.40	0.75
Max drive voltage (v)	0.8	3	3
At -55°C			
Min width of drive (μs)	*	40	140
Max width of drive (μs)	*	425	1000
Current (μa)	*	9	11.5
Min drive voltage (v)	*	0.25	0.3
Max drive voltage (v)	*	2.5	3

*Transistors did not have required gain of 10, and therefore, the ring counter did not operate reliably.

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TR-1154, 15 October 1963, 12 pp text, 6 illus., Department of the Army Proj 1P523801A300, AMCMS Code 5523.11.624, HDL proj 46345, UNCLASSIFIED Report

A design procedure for a transistor ring counter is derived. Using this procedure a 30-μw decade ring counter and a 500-kc decade ring counter were built. Both operated satisfactorily.

Low-power counters

Ring counters

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