TR-1185

THE APPLICATION OF PULSE SEQUENTIAL CIRCUITRY TO CONTROL DEVICES

Ira R. Marcus

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FOR THE COMMANDER:
Approved by

Robert S. Hoff

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CONTENTS

ILLUSTRATIONS

Figure

ABSTRACT

This report describes the application of pulse sequential circuitry theory to the design of an all solid-state electronic control circuit. In pulse sequential circuits, an output program occurs only upon receiving a unique input sequence. A prototype model was built and its performance was satisfactory. It demonstrated the ease with which pulse sequential circuitry theory can be applied to the solution of pulse sequential problems.

1. INTRODUCTION

In many applications, it is required that before an output control signal can occur, a unique set of inputs must first take place. In combinational circuits, these inputs occur simultaneously. In sequential circuits, the inputs occur one after the other. This report is concerned with sequential circuits. A mechanical analogy would be a mechanical "combination" lock where the inputs, the combination numbers, are put into the system one after the other.

Pulse sequential theory offers solutions to problems that appear in ordnance devices, e.g., in programmers, proximity fuze systems, security systems, and computers. The inputs to the sequential circuits may be remotely inserted through a wire or radio link as might be desired in remote initiation of a nuclear explosive.

In sequential circuits, the inputs may be a series of pulses, step functions, or both. The output may be a single pulse or step function or a complex program of either or both. The design procedure for sequential circuits using flow tables and Boolean algebra is explained in reference 1. Other procedures may be found in references 2, 3, and 4.

2. APPLICATION OF PULSE SEQUENTIAL CIRCUITRY THEORY

The following problem was arbitrarily selected to illustrate the power of sequential circuitry when applied to control circuits.

(a) The input circuit will be composed of three input lines.

(b) The input sequence, which will control a single output, will be composed of seven pulses.

(c) If the input lines are numbered X_1, X_2, and X_3, the unique input sequence that enables an output to occur will be X_2, X_3, X_1, X_3, X_2, X_3, X_2.

(d) The output will be a positive-going voltage step-function and will manifest itself by turning on an incandescent lamp. (A relay or a squib could, of course, be substituted for control purposes.)

(e) Any deviation from the proper input sequence will immediately lock out the device so that no further inputs can cause an output. A lockout indicator will indicate that an incorrect input has been applied.

It is clear that there are 2186 (3^7 - 1) incorrect sequences and only one correct sequence.

The design procedure given in reference 1 is applied. The correct sequence is X_2, X_3, X_1, X_3, X_2, X_3, X_2. The output is to occur upon the application of the last X_2 input.

A flow table is developed.

State	X_1	X_2	X_3
1	8	2	8
2	8	8	3
3	4	8	8
4	8	8	5
5	8	6	8
6	8	8	7
7	8	$\underline{8}$	8
8	8	$\underline{8}$	8

The flow table describes the states of the memory circuits when the circuits are stable (not in transition). In addition it describes the state to which the memory circuits will go when they receive an input. For example,we start out in state 1, and upon application of an X_1 input (X_1 column), we go to state 8. Similarly an X_3 input will cause the circuits to go to state 8. However, an input of X_2 will cause the circuits to go to state 2. If the circuits are in state 2 and receive an input of X_1 or X_2, they will go to state 8; however, if the input is X_3, they will go to state 3. We thus see that the table describes the desired operation of the circuits. It is also clear that the circuits follow the required response; i.e., any input sequence other than the correct one, leads to state 8, and once in state 8, they cannot change state no matter what the input. The correct six inputs lead the circuits to state 7. The seventh correct input causes the circuitry to yield an output, underlined, and then they go to state 8 and are locked in. Figure 1 is a state diagram and is another way of describing the responses of the system to input pulses.

We note that the system has eight states and that if it is composed of three binary devices, the eight possible states of these devices could describe the eight required states of the circuits. The three binary devices are labeled Y_1, Y_2, and Y_3. We use flip-flops as the binary memory elements.

We can label the outputs of the flip-flop Y_1 to be y_1 and $\bar{y}_1$. The outputs of flip-flops Y_2 and Y_3 are labeled similarly. In addition, we describe the state of the flip-flop to be either in the 0 or the 1 state. The flow table now becomes

State	Secondary Assignment			Primary Inputs		
	y_1	y_2	y_3	X_1	X_2	X_3
1	0	0	0	8	2	8
2	0	0	1	8	8	3
3	0	1	0	4	8	8
4	0	1	1	8	8	5
5	1	0	0	8	6	8
6	1	0	1	8	8	7
7	1	1	0	8	$\overline{8}$	8
8	1	1	1	8	$\overline{8}$	8

where y_1 y_2 y_3 describe the eight possible states. This is called secondary assignment. We can now describe what each flip-flop must do upon application of an input pulse. For example, if the circuits are in state 1, the three binaries Y_1 Y_2 Y_3 are in states 000. Upon receiving an X_1 or an X_3 input, the system goes to state 8, and the flip-flops must assume the 111 condition defined by state 8. If an X_2 input is received and the system is in state 1, then the system must assume state 2 or 001. We can now make a table describing the changes that the binaries must undergo when going from one system state to another system state.

State	Secondary Assignment			Primary Inputs			Flip-flop State-changes		
	y_1	y_2	y_3	X_1	X_2	X_3	X_1	X_2	X_3
1	0	0	0	8	2	8	111	001	111
2	0	0	1	8	8	3	110	110	011
3	0	1	0	4	8	8	001	101	101
4	0	1	1	8	8	5	100	100	111
5	1	0	0	8	6	8	011	001	011
6	1	0	1	8	8	7	010	010	011
7	1	1	0	8	$\overline{8}$	8	001	001	001
8	1	1	1	8	$\overline{8}$	8	000	000	000

When the system is in state 1 and is directed to go to state 8 by either an X_1 or an X_3 input, the secondary assignment must change from 000 to 111. If a flip-flop state-change is indicated by a "1", and no change is indicated by a "0", then going from state 1 to state 8 is denoted by 111. If the system is in state 1 and receives an X_2 input, it must go to state 2, and change its secondary state from 000 to 001, and the change is denoted by 001. If the system is in state 6, 101, and receives an X_3 input directing it to go to state 7, or 110, then the change is denoted by 011 and is so listed in the table. The following equations describe the desired behavior of the three binaries and are derived from the flip-flop change columns. C_1 represents conditions for which binary Y_1 is to change state. C_2 and C_3 are similarly defined for binaries Y_2 and Y_3.

$$C_1 = X_1 [\bar{y}_1\bar{y}_2 + \bar{y}_1 y_3] + X_2 [\bar{y}_1 y_2 + \bar{y}_1 y_3] + X_3 [\bar{y}_1 y_2 + \bar{y}_1\bar{y}_3]$$

$$C_2 = X_1\bar{y}_2 + X_2 [\bar{y}_2 y_3] + X_3 [\bar{y}_2 + \bar{y}_1 y_3]$$

$$C_3 = X_1\bar{y}_3 + X_2\bar{y}_3 + X_3 [\bar{y}_3 + \bar{y}_1 + \bar{y}_2]$$

$$\text{OUTPUT } L_z = X_2 y_1 y_2 \bar{y}_3$$

L_z is the input to a latching circuit. Once latched, the circuit will remain latched until reset. The output of the latching circuit is Z.

These equations are derived from the flip-flop change table and have been reduced using standard minimization techniques derived in Boolean algebra (ref 1). It should now be noted that the original pulse sequential problem has its solution expressed in combinational equations.

The incorrect-input indicator is to be activated when the system is in state 8 and when the correct input has not been applied. This is expressed by

$$\text{Incorrect input } (Q) = y_1 y_2 y_3 \bar{Z}$$

Figures 2, 3, and 4 show the logic block diagrams for converting the equations for C_1, C_2, and C_3 into circuitry. It may be noted that the third level logic NOR's are included for logic purposes but are omitted in the circuitry, because the logic calls for the flip-flops to change state when the input to the flip-flop goes from a "0" to a "1". However, the circuits in figure 6 change state when the input goes from "1" to "0". Figure 5 shows the logic block diagram for the output circuit and for the incorrect-input indicator. Figure 6 is a schematic of the flip-flop. It changes state when the input C goes from +6 v, a "1", to ground, a "0". Both collectors of the flip-flop transistors have emitter-follower outputs due to the large fan-out of NOR circuits that have to be driven by the flip-flop. In addition, a 1N792 diode, a 680-ohm resistor, and a 1-μf capacitor form a clamping circuit, so that the flip-flop comes up to the "0" state when power is applied. This eliminates the possibility of false outputs such as the three flip-flops initially coming up to the 110 condition, state 7, and yielding a correct sequence output when X_2 is the first input. The emitter-follower output circuitry of the flip-flops has filter networks composed of a 100-ohm resistor and a 1-μf capacitor. The purpose of the filters is to prolong the rise and fall times. The filter networks are required to prevent hazards. For example, if the system was in state 1 and received an X_2 input, it would proceed to state 2. If the X_2 input was still present after the system went into state 2, then flip-flops Y_1 and Y_2 would change if their inputs were step-functions. The system would again change state, to state 8, and be locked in. In addition, the filter networks prevent another type of hazard from causing false

outputs. For example, if the system was in the 001 state and received an X_3 input directing a change to the 010 state, the system could possibly assume the 000 state before going into the 010 state. During this transition we could get a false output if the filter networks did not decrease the slopes of the pulses to the input of the flip-flops and the latching output circuit and indicator.

Figure 7 shows the schematic diagrams of the NOR circuits and the $\bar{X}$ generators. The 10-ohm resistor and the 22-μf capacitor in the $\bar{X}$ generator prevent switch bounce from disturbing the circuits. Figure 8 shows the schematic diagram of the output circuit and the incorrect-input indicator. In a field application, it is not expected that an incorrect-input indicator would be used. The flip-flops and the output circuit have provisions to be reset by a single push-button.

3. CONCLUSION

It has been shown that pulse sequential circuitry theory can easily be applied to pulse sequential problems. It converts sequential input problems to simple combinational problems. It can be used wherever it is required that a specific input sequence take place before an output program can be obtained. The solutions use simple logic circuits readily available in microelectronics and thus can be packaged in small volumes.

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(2) Huffman, D. A., "The Synthesis of Sequential Circuits," Journal of Franklin Institute, Vol 257, No. 3, pp 161-190, March 1954, No. 4,pp 275-303, April 1954.

(3) Mealy, G. H., "A Method for Synthesizing Sequential Circuits," Bell System Tech J, Vol 34, No. 5, pp 1045-1079, Sept 1955.

(4) Marcus, M. P., "Switching Circuits for Engineers," Prentice Hall 1962, Englewood Cliffs, N. J.

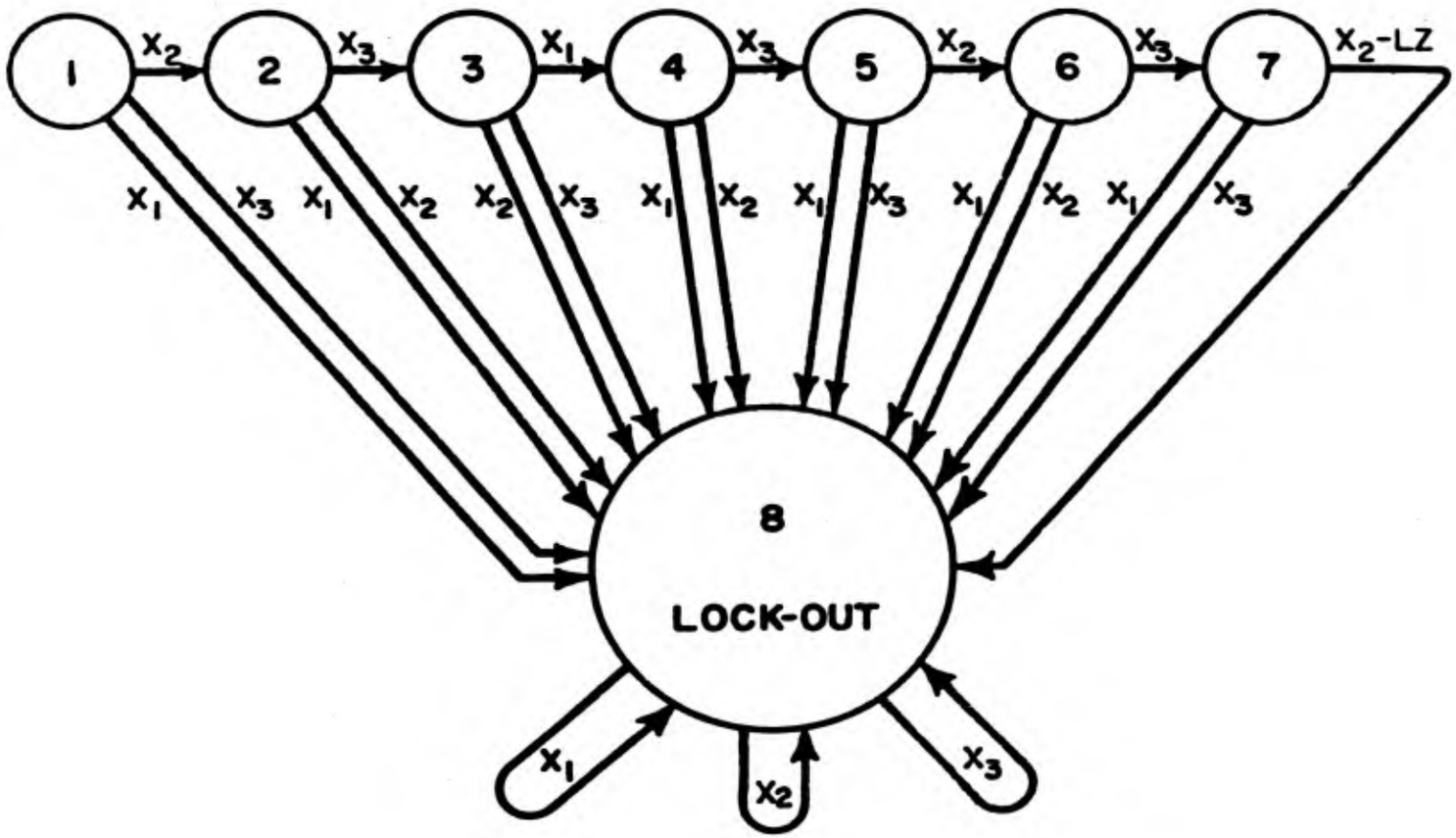


Figure 1. State diagram.

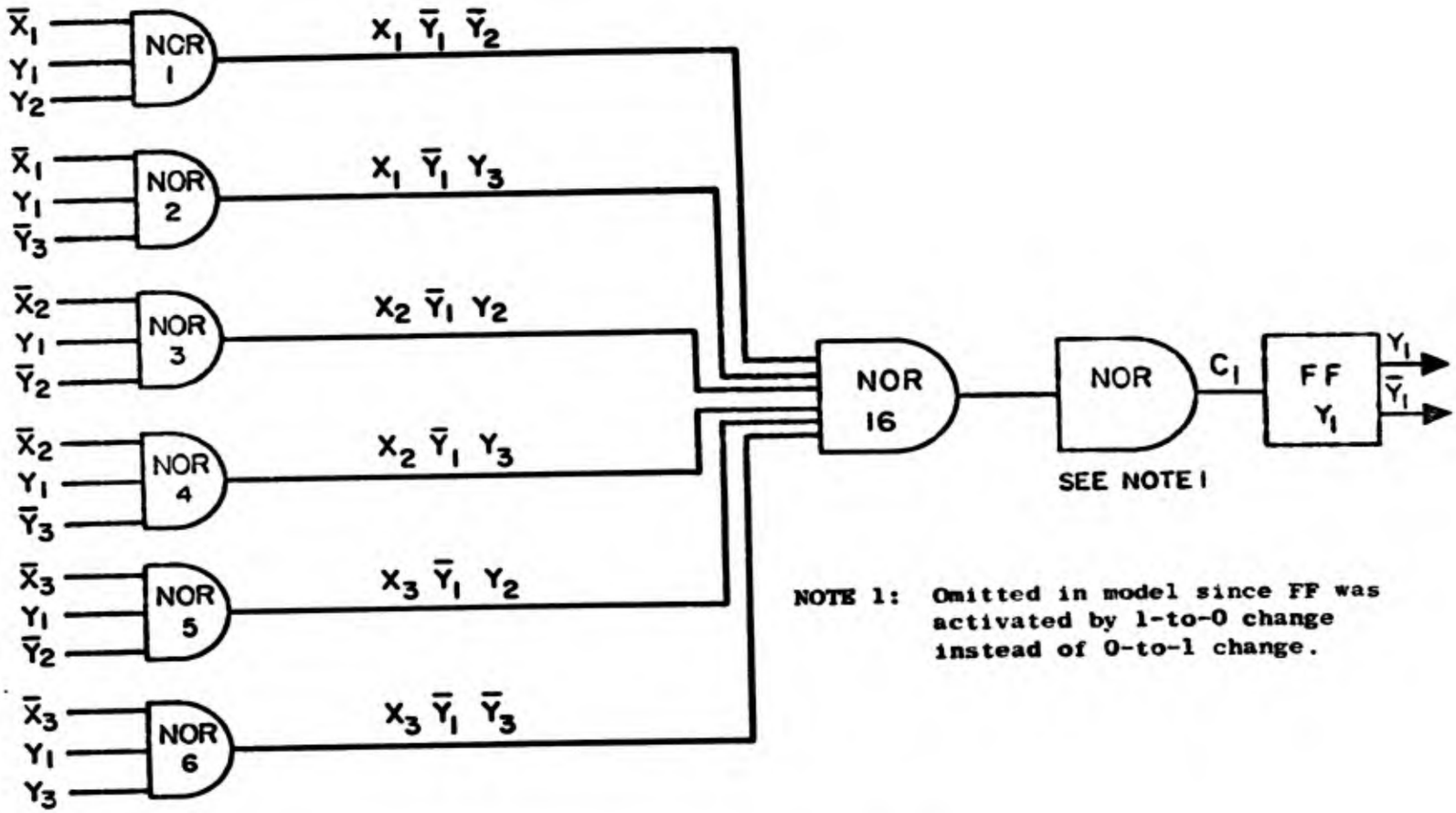
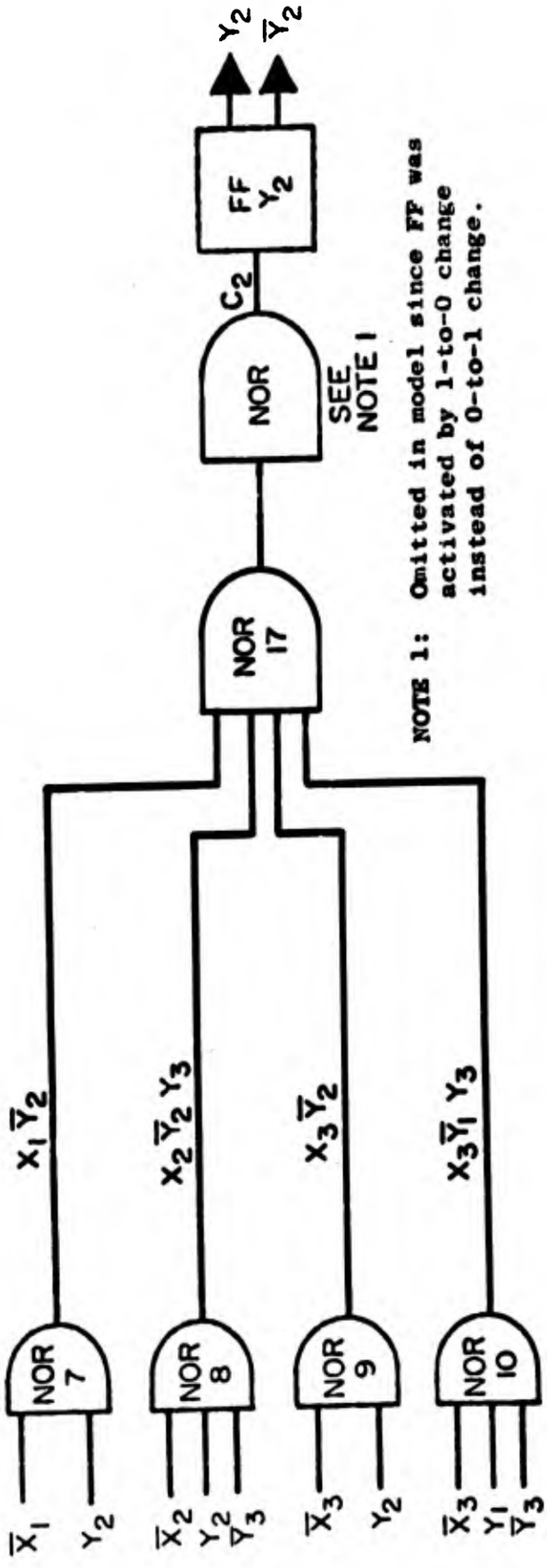


Figure 2. Logic block diagram for C_1.



NOTE 1: Omitted in model since FF was activated by 1-to-0 change instead of 0-to-1 change.

Figure 3. Logic block diagram for C_2.

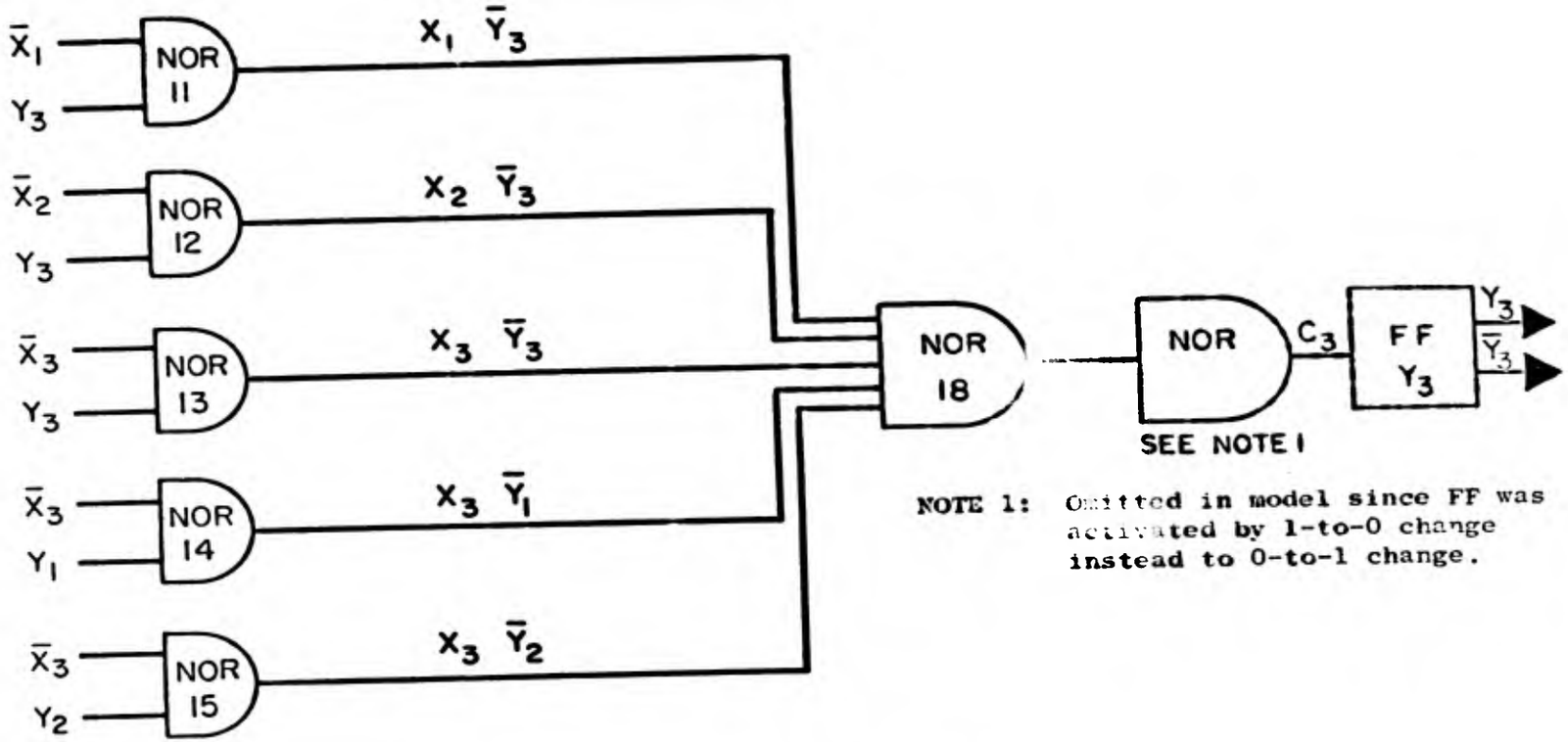


Figure 4. Logic block diagram for C_3.

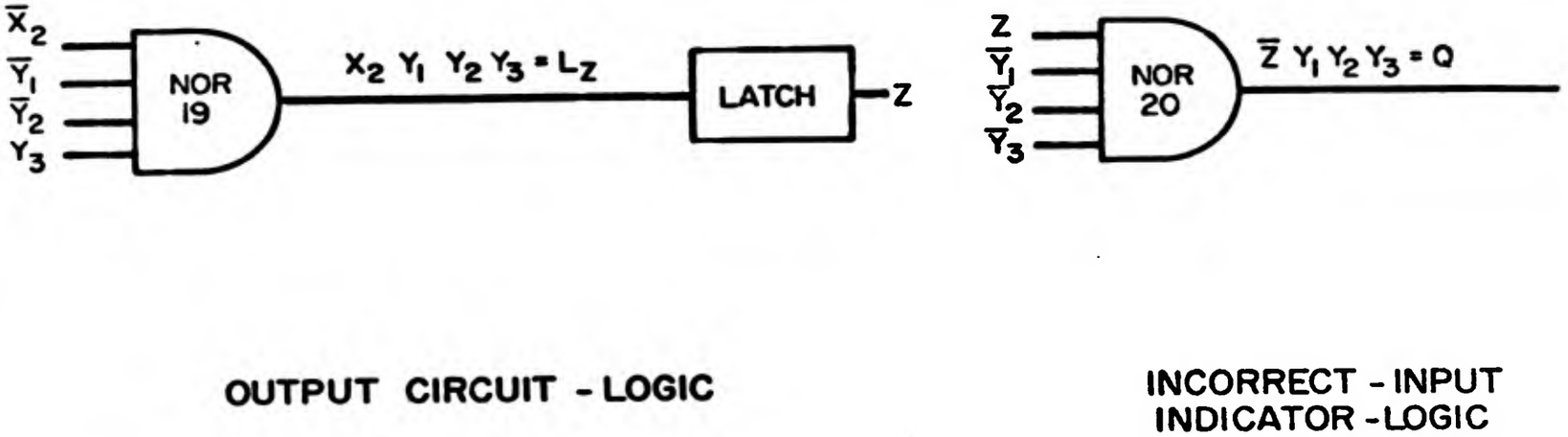


Figure 5. Block diagram for output circuit logic and incorrect-input indicator logic.

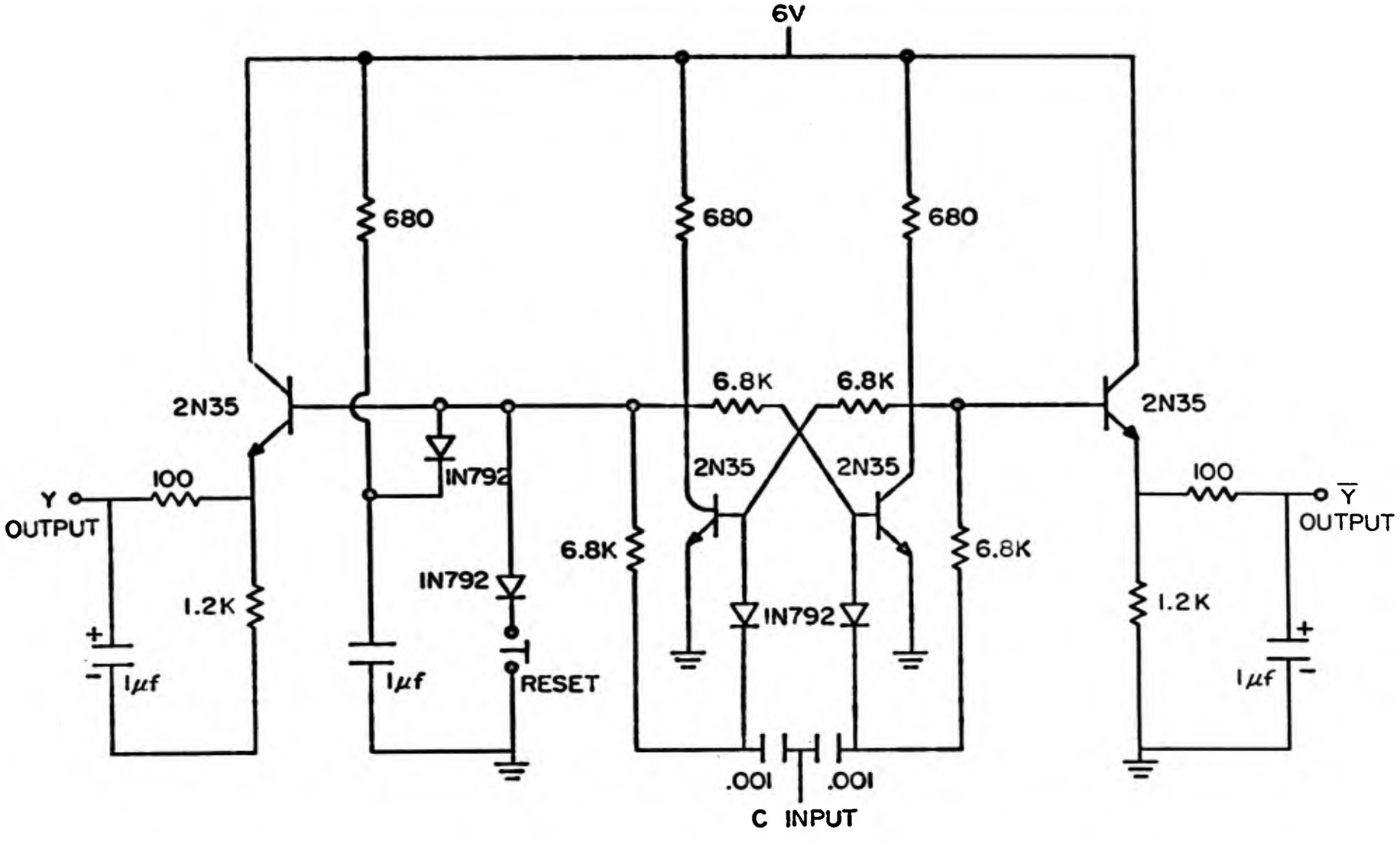


Figure 6. Logic circuits, memory element, flip-flop Y

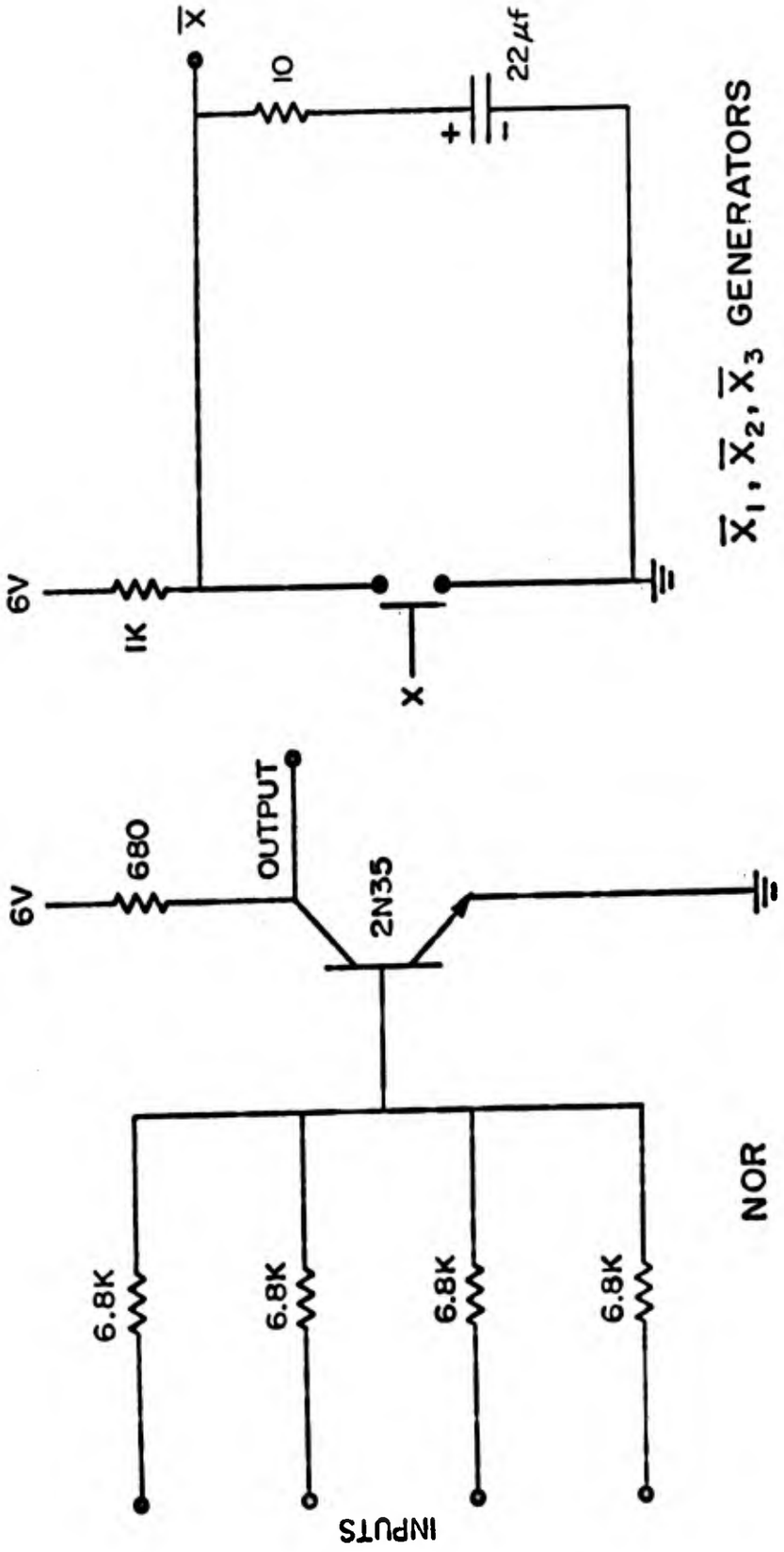
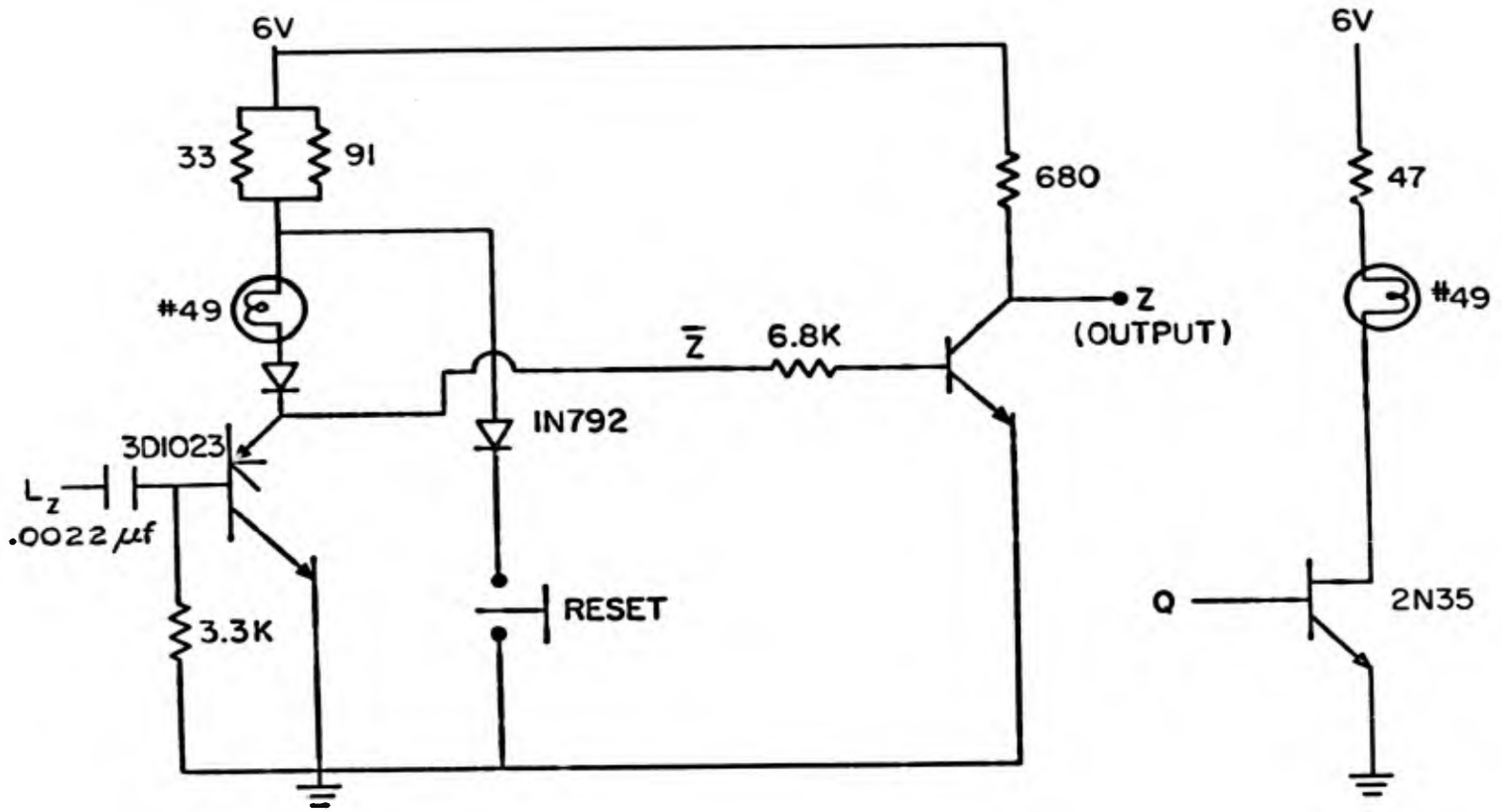


Figure 7. Logic circuits.



CORRECT - INPUT INDICATOR

INCORRECT - INPUT INDICATOR

Figure 8. Logic circuits.

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