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INTERIM REPORT

Contract No. FAA/ARDS-444

TASK 2: LABORATORY EVALUATION OF BREADBOARD EQUIPMENT

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EXPERIMENTAL EVALUATION OF COMPATIBLE PWI/CAS INTERROGATOR - TRANSPONDER TECHNIQUES

VOLUME 2 OF 2

September 1963

This report has been approved for general distribution.

Prepared for

AVIATION RESEARCH AND DEVELOPMENT SERVICE
FEDERAL AVIATION AGENCY
WASHINGTON 25, D.C.

By

SPERRY GYROSCOPE COMPANY
DIVISION OF SPERRY RAND CORPORATION
GREAT NECK, NEW YORK

426908

Sperry Report No. EB-5261-0341-2

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JAN 17 1964

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**EXPERIMENTAL EVALUATION
OF COMPATIBLE PWI/CAS
INTERROGATOR - TRANSPONDER TECHNIQUES**

VOLUME 2 OF 2

September 1963

This report has been prepared by Sperry Gyroscope Company Division of Sperry Rand Corporation for the Aviation Research and Development Service, Federal Aviation Agency, under Contract No. FAA/ARDS-444. The contents of this report reflect the views of the contractor, who is responsible for the facts and the accuracy of the data presented herein, and do not necessarily reflect the official views or policy of the FAA.

By

SPERRY GYROSCOPE COMPANY

DIVISION OF SPERRY RAND CORPORATION

GREAT NECK, NEW YORK

Sperry Report No. EB-5261-0341-2

Copy No. 1

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SECTION V

BREADBOARD IMPLEMENTATION

A. DESCRIPTION

This section contains descriptions of the components which make up the CAS and PWI interrogators and the transponder equipment. The components consist of coders, decoders, and computers. Six sections are included, each one corresponding to a particular system component. The operation of the coding and decoding units is described with the aid of detailed block diagrams (figure 5-1 thru 5-4) where the blocks represent standard video and logic circuits. The operation of the computing units is described with the aid of signal schematics (figures 5-5 and 5-6) considered more appropriate for describing the flow of analog data. These block diagrams and signal schematics are contained at the end of this volume. They are followed by other interconnection information in the form of

- interconnection diagrams for the coders and decoders (figures 5-7 through 5-10)
- power schematics and schematics of chassis-mounted transformers for the computing units, which have self-contained power supplies (figures 5-11 through 5-15).

Following the interconnection information are schematic diagrams of the components which comprise these major units (figures 5-16 through 5-62). Component diagrams are identified by the same titles and numeric or alpha-numeric designations employed in the block diagrams and signal schematics to aid in identification. Following the component schematics are schematics of multiple-use elements, saturated flip-flop and chopper stabilized d-c operational amplifiers (figures 5-63 and 5-64).

1. Interrogator Encoder

The basic system repetition rate of 200 cps is generated by an astable multivibrator driving a bistable multivibrator (see figure 5-1).

The gate generated by the bistable multivibrator is used as a system sampling gate. Its duration is one-half of the period between cycles or 2.5 milliseconds.

The gate is also differentiated to form positive and negative spikes at leading and trailing edges, respectively.

The control coder employs a delay line with taps corresponding to desired time delay spacings between pulses 1 and 2 and pulses 2 and 3. Delay between pulse no. 1 and pulse no. 2 is 12 microseconds. A delayed pulse (pulse no. 2) is amplified and shaped and coupled to the mixer-amplifier. The delay between pulse no. 2 and pulse no. 3 is determined by the coarse altitude code wheel selecting a ground for a pickup amplifier on the control coder corresponding to the coarse altitude band in which the present or projected altitude is located. A delayed pulse (pulse no. 3) is amplified and shaped and coupled to the mixer-amplifier and the vernier coder.

The vernier coder uses a linear sweep generator to produce a pair of pulses delayed in time with respect to pulse no. 3, proportional to the altitude vernier d-c input voltage.

The gate generator is a simple flip-flop triggered on by pulse no. 3 and reset by pulse no. 5.

The sweep generator produces a linear sweep voltage proportional to time for the duration of the gate.

Isolation amplifiers decouple the sweep generator from the following circuits to prevent interaction which might cause sweep non-linearities. Clamping of sweeps to a d-c level permits vernier adjustments of delays to compensate for sweep generator delay irregularities and to provide a fixed time delay in addition to the continuously variable delay.

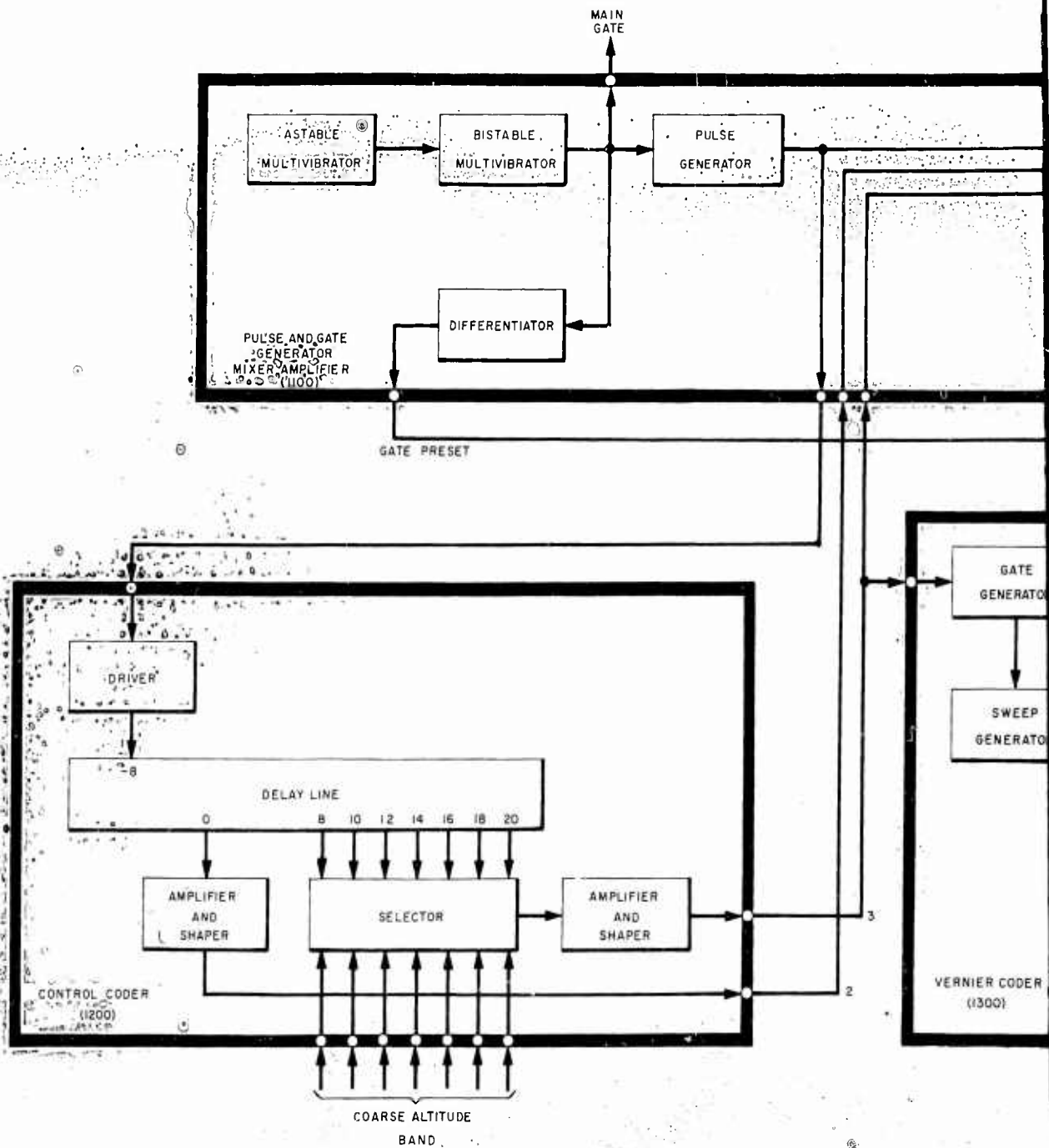
Comparators and pulse generators compare the sweep with the d-c reference voltage, generating pulses at the times the sweep voltages exceed the reference voltage.

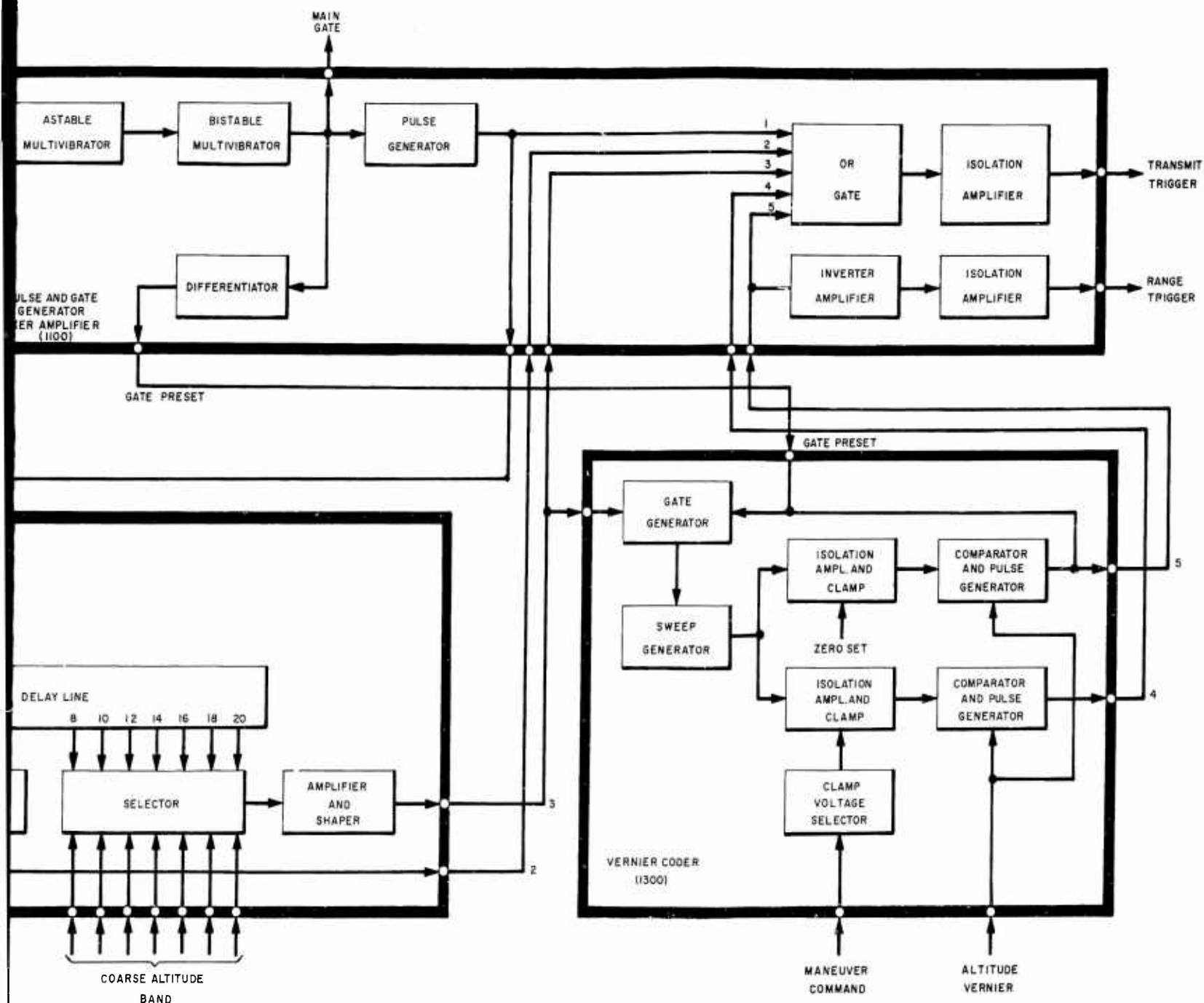
The clamp voltage selector selects one of two clamp voltages to provide two positions for pulse no. 4 with respect to pulse no. 5. Both pulse no. 4 and pulse no. 5 are coupled to the mixer-amplifier.

The mixer-amplifier accepts all five input pulses and combines them in a five-pulse train. Isolation amplifiers decouple the amplifiers from the following circuits.

2. Interrogator Decoder

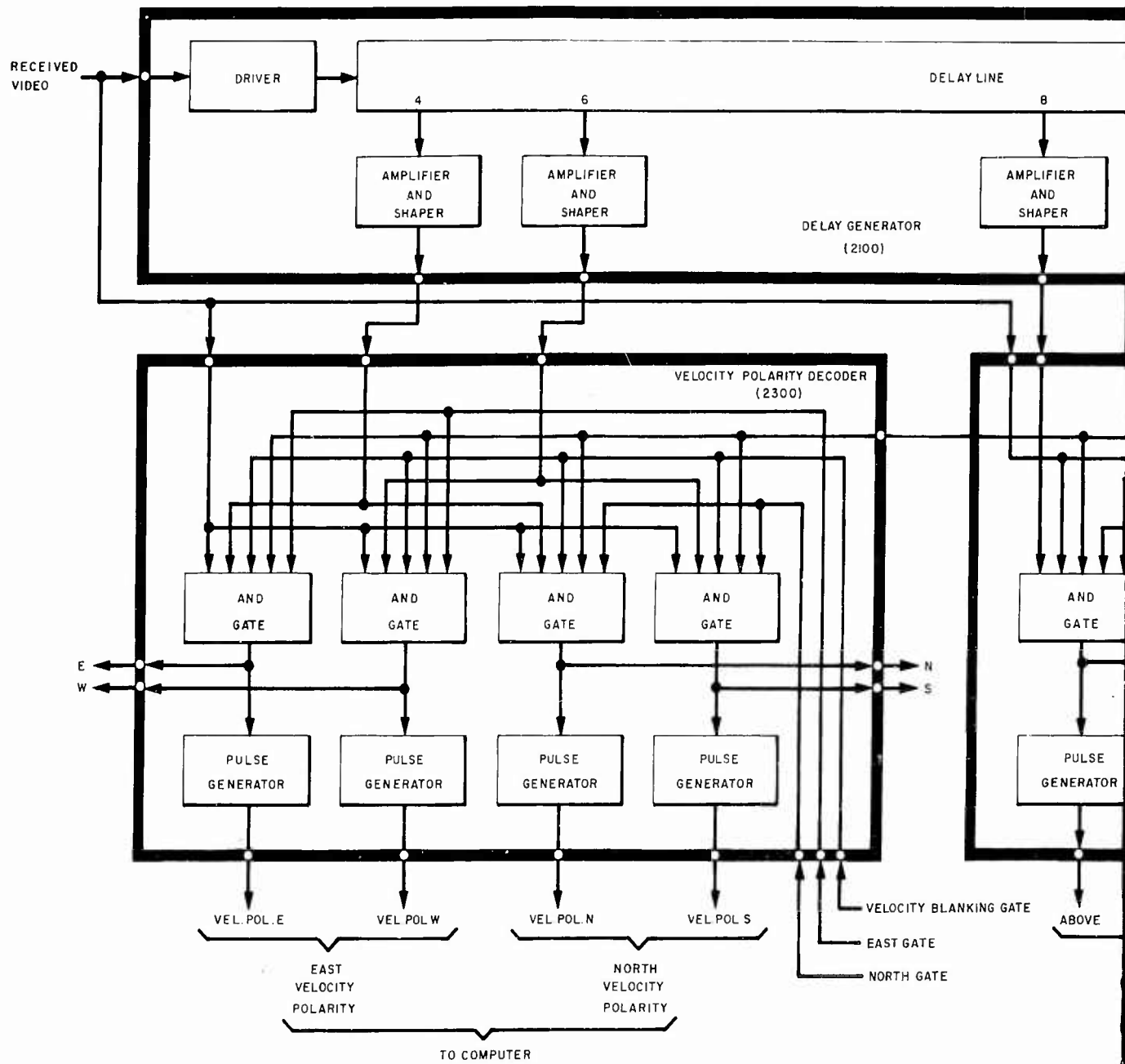
In the interrogator decoder block diagram, shown in figure 5-2 received video pulses are applied to the delay generator where they are delayed, amplified, and shaped into square pulses. Output signals correspond to delays of 4, 6, 8, 10, 12 and 20 microseconds.



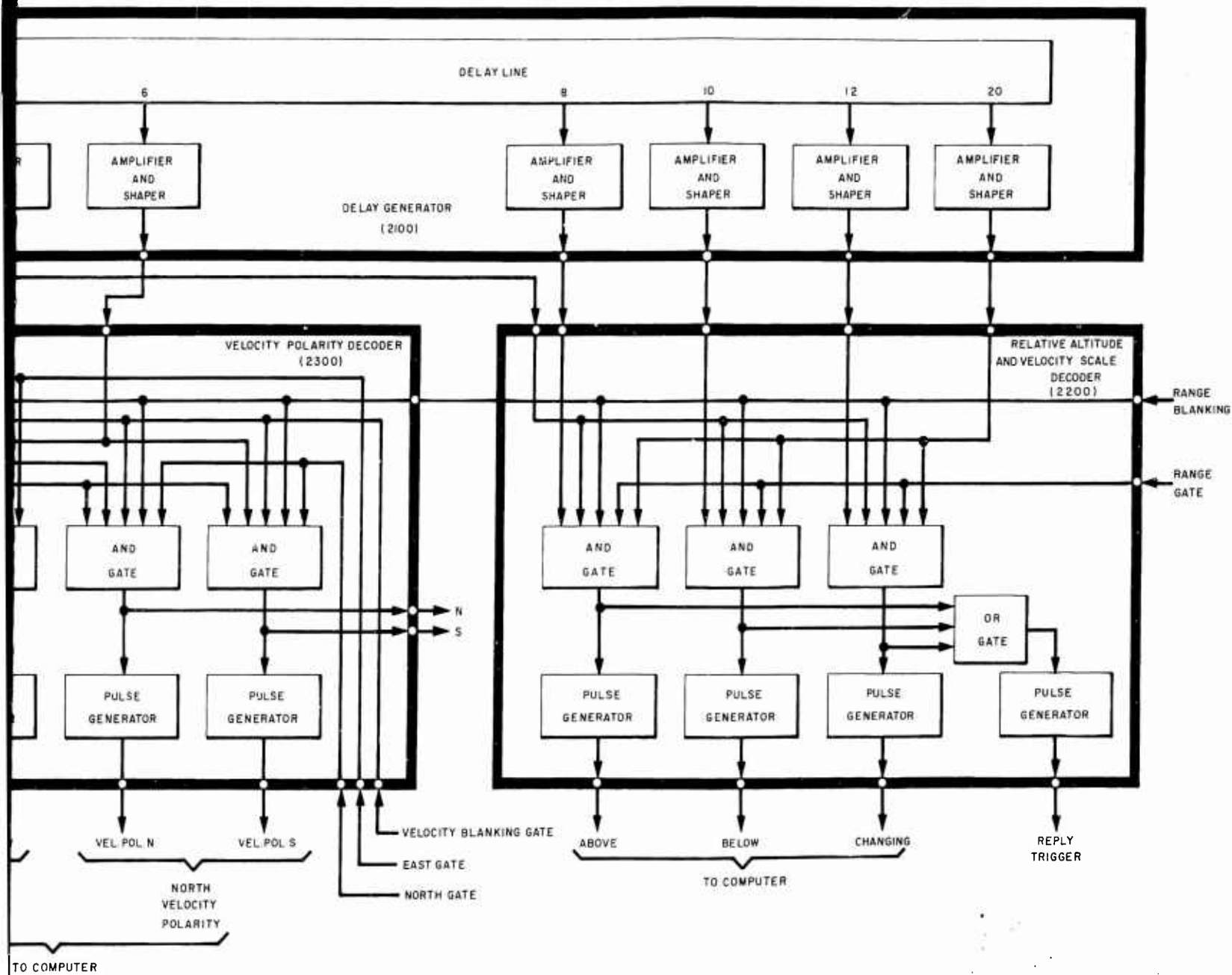


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FIGURE 5-1
INTERROGATOR ENCODER (1000)

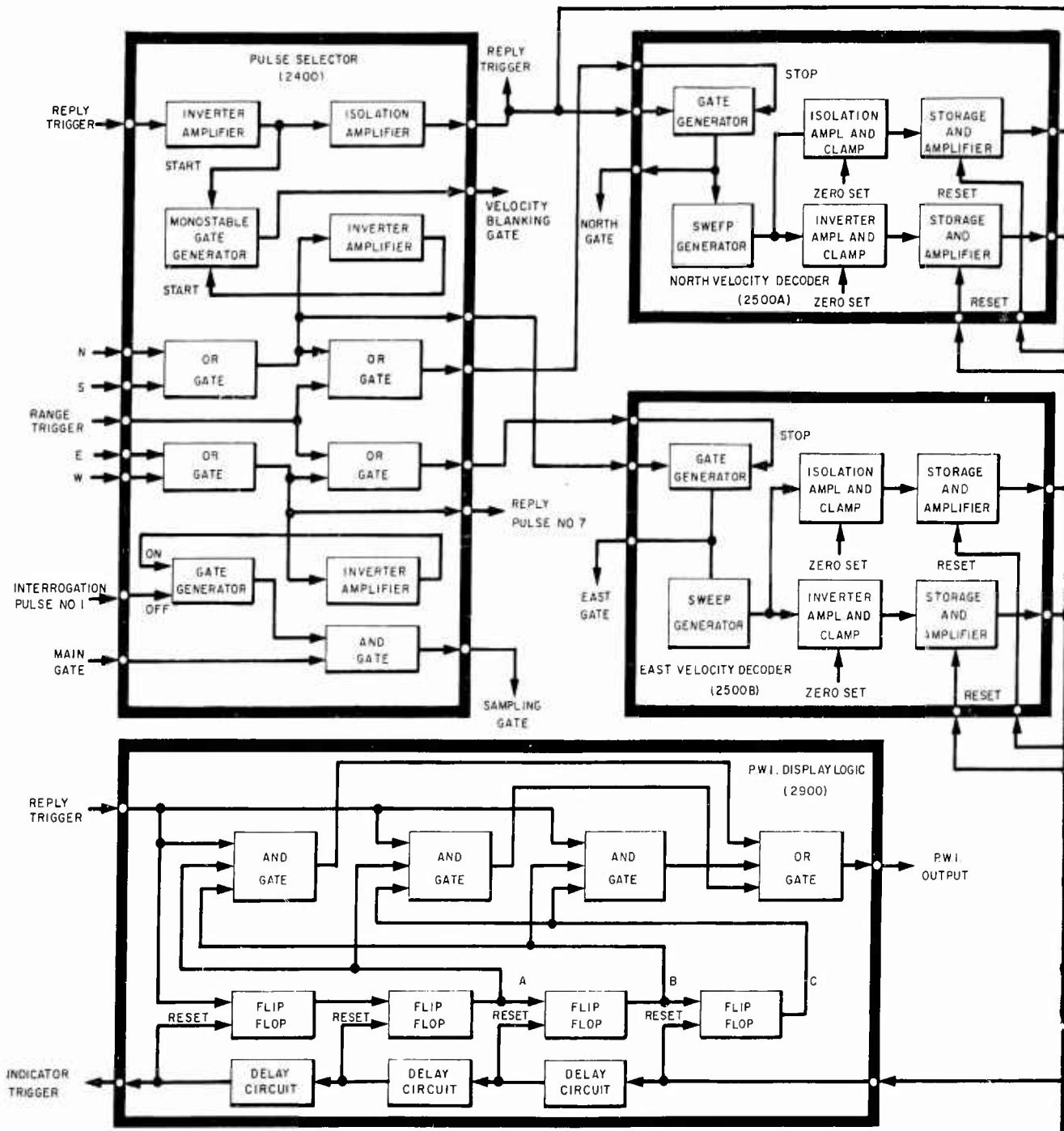


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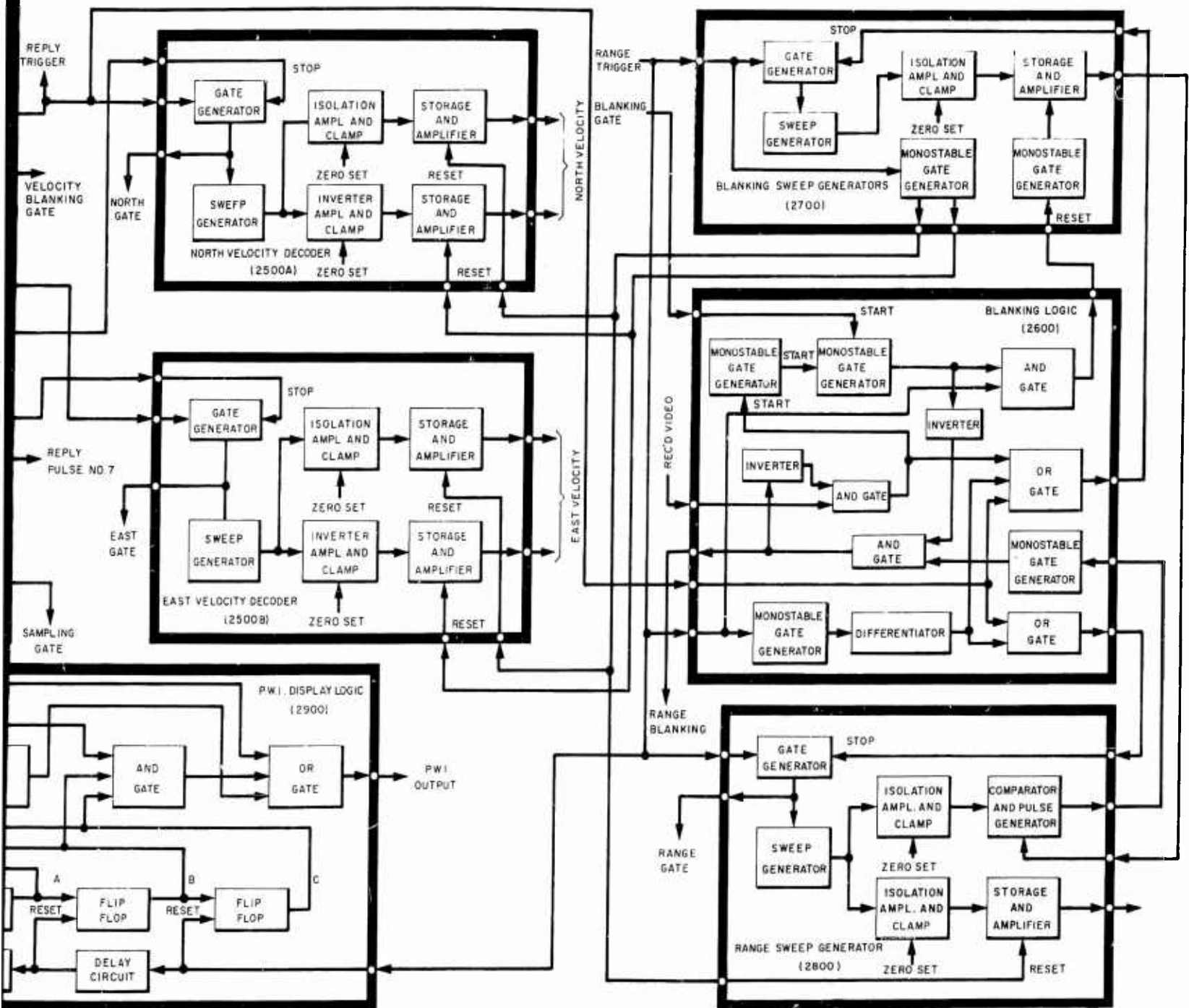


2

FIGURE 5-2
INTERROGATOR DECODER (2000) (SHEET 1 OF 2)



1



2

FIGURE 5-2.
INTERROGATOR DECODER (2000) (SHEET 2 OF 2)

The 8, 10, 12 and 20-microsecond delayed pulses are compared with the undelayed video pulses in the relative altitude decoder. If coincidence occurs in any of these three AND gates, a pulse appears at the corresponding output terminals. This reply trigger pulse is generated to start the velocity decoding, and complete the ranging measurements.

In the velocity polarity decoder the four- and six-microsecond delayed pulses are compared with the received video signal. In addition, gates are applied to separate the north and east polarity signals from each other, and to blank improper decoding of north or east components near or at zero magnitude. When video coincidence occurs between the four- or six-microsecond delayed signal and the undelayed video, an output pulse is generated provided that the appropriate north or east velocity gate is also present. The velocity polarity pulses are then coupled to the computer and to the north and east velocity decoders.

The north velocity decoder accepts a reply trigger pulse to start a linear velocity voltage sweep. The sweep is terminated when a north/south velocity polarity signal is received which resets the velocity gate generator. The sweep is also inverted, and both positive and negative sweep voltages are stored and peak detected to provide a bipolar north velocity voltage on two wires which is maintained until reset by the next range trigger pulse.

The east velocity decoder is identical to the north velocity decoder except that it is triggered on by the north/south velocity polarity signal and off by the east-west velocity polarity signal.

A sampling gate generator is also in the pulse selector. A flip-flop is triggered on by the east/west velocity polarity signal of a received pulse train; the off trigger is the next following interrogation pulse no. 1. Thus, when a correctly coded reply signal is received, a long gate is generated which is used to accept the main gate signal for use as a sampling gate in the computer. If no correctly coded reply signal is received no sampling gate is sent to the computer.

The range blanking signal is applied to the relative altitude decoder, velocity scale decoder, and the velocity polarity decoder.

The range measurement circuits consist of a range sweep generator, a blanking sweep generator, and a blanking logic circuit.

The range trigger pulse starts the voltage sweep of the range sweep generator. This sweep is stopped by a reset pulse from the blanking logic unit. The peak voltage reached by the sweep is stored in the voltage storage circuit and coupled to the computer as a range voltage. The voltage storage circuit is reset by the next following range trigger. A range gate is extracted from the gate generator to gate the relative altitude decoder and velocity scale decoder to accept only reply signals from transponders within a predetermined range.

The range trigger pulse also starts the blanking sweep generator voltage sweep which continues until reset by either the gated video (third pulse of a non-threatening transponder) or the coincidence trigger pulse. The peak voltage reached by this sweep is stored and applied to the comparator of the range sweep generator. By means of the zero set adjustments the blanking sweep generator voltage output is caused to produce a pulse output from the range sweep generator which precedes the coincidence trigger of the next cycle by a small time interval. This pulse is used for range blanking.

The blanking logic unit accepts the range trigger pulse and generates a monostable gate having a time duration equivalent to the range of the interrogator system. The gate is differentiated to produce a pulse at its trailing edge. This pulse is combined with the reply trigger pulse in an OR gate, such that the earlier of the two pulses resets the range sweep generator gate.

The gated video (third pulse of a non-threatening transponder) also starts a monostable gate generator which sets another monostable gate generator. The second gate generator output is coupled to an AND gate to inhibit the blanking sweep storage reset pulse. The duration of the sum of the two gates is slightly longer than one system cycle. A blanking gate from the computer, indicating that the earliest coincidence trigger is from a non-threatening aircraft and should be blanked also starts the second gate generator. Therefore, if a blanking gate is present or if the reply trigger is inhibited, then the range trigger is prevented from resetting the blanking sweep storage by means of an AND gate.

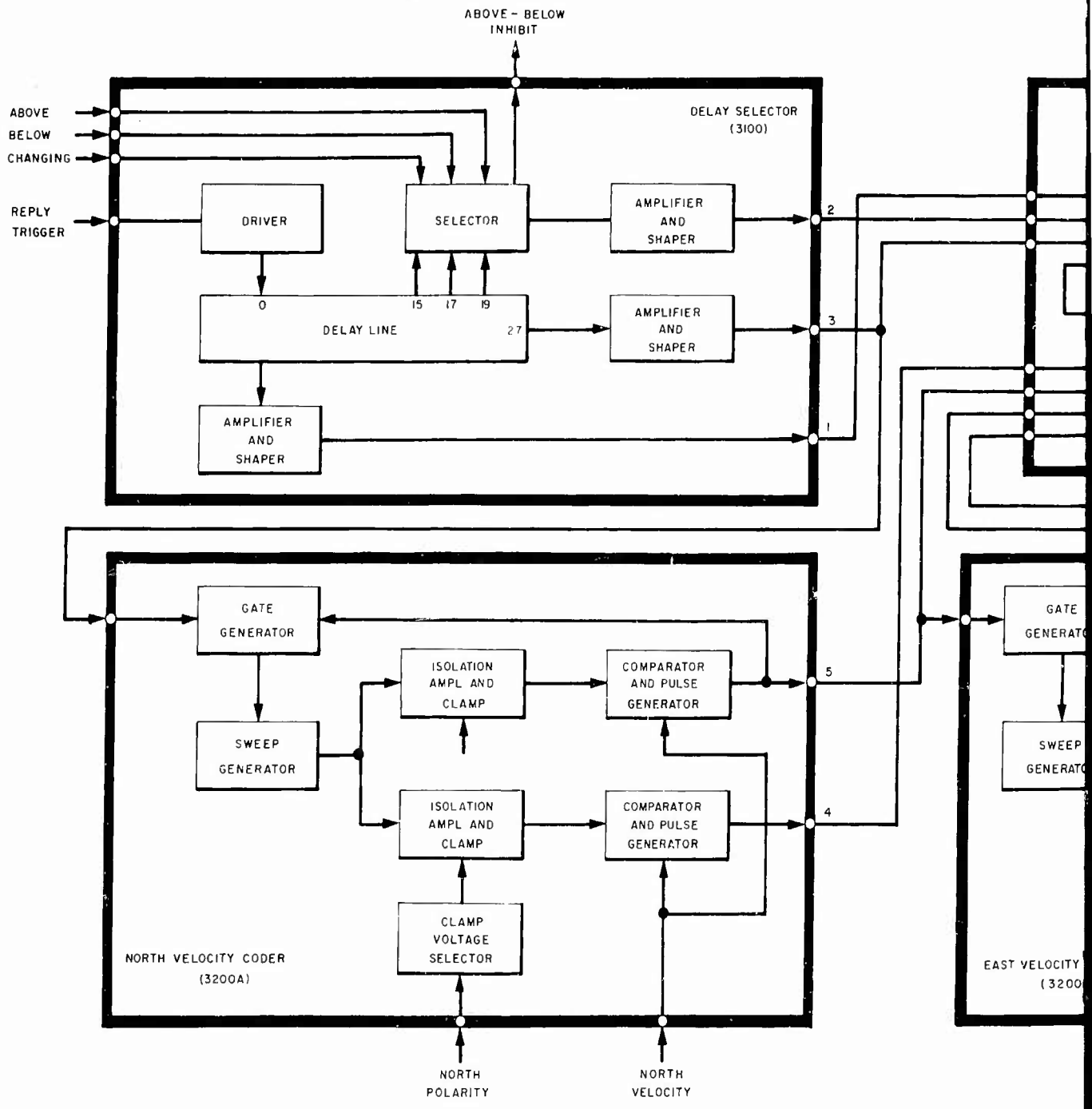
The storage reset inhibiting gate is also used to accept the range blanking pulse generated by the range sweep generator, passing through a monostable gate generator and thence to an AND gate. The resultant signal is the range blanking signal.

3. Transponder Encoder

The transponder encoder is driven by the reply trigger and modulates the transmit trigger and suppressor output signal with information concerning the vector velocity of the transponder aircraft. A block diagram of the transponder encoder is shown in figure 5-3.

The reply trigger is coupled into the delay selector of the transponder encoder where it drives a delay line. The following three pulses are tapped from this delay line:

- pulse no. 1 is chosen according to the velocity scale factor and is placed in a fixed time prior to pulse no. 3.
- pulse no. 2 is chosen according to the relative altitude of the interrogator input signal and is likewise placed in one of three positions. A climbing signal, if present, selects one position. If no climbing signal exists, an early trigger, if present, selects a second position. If neither a climbing signal nor any early trigger signal is present the third position is chosen.



1

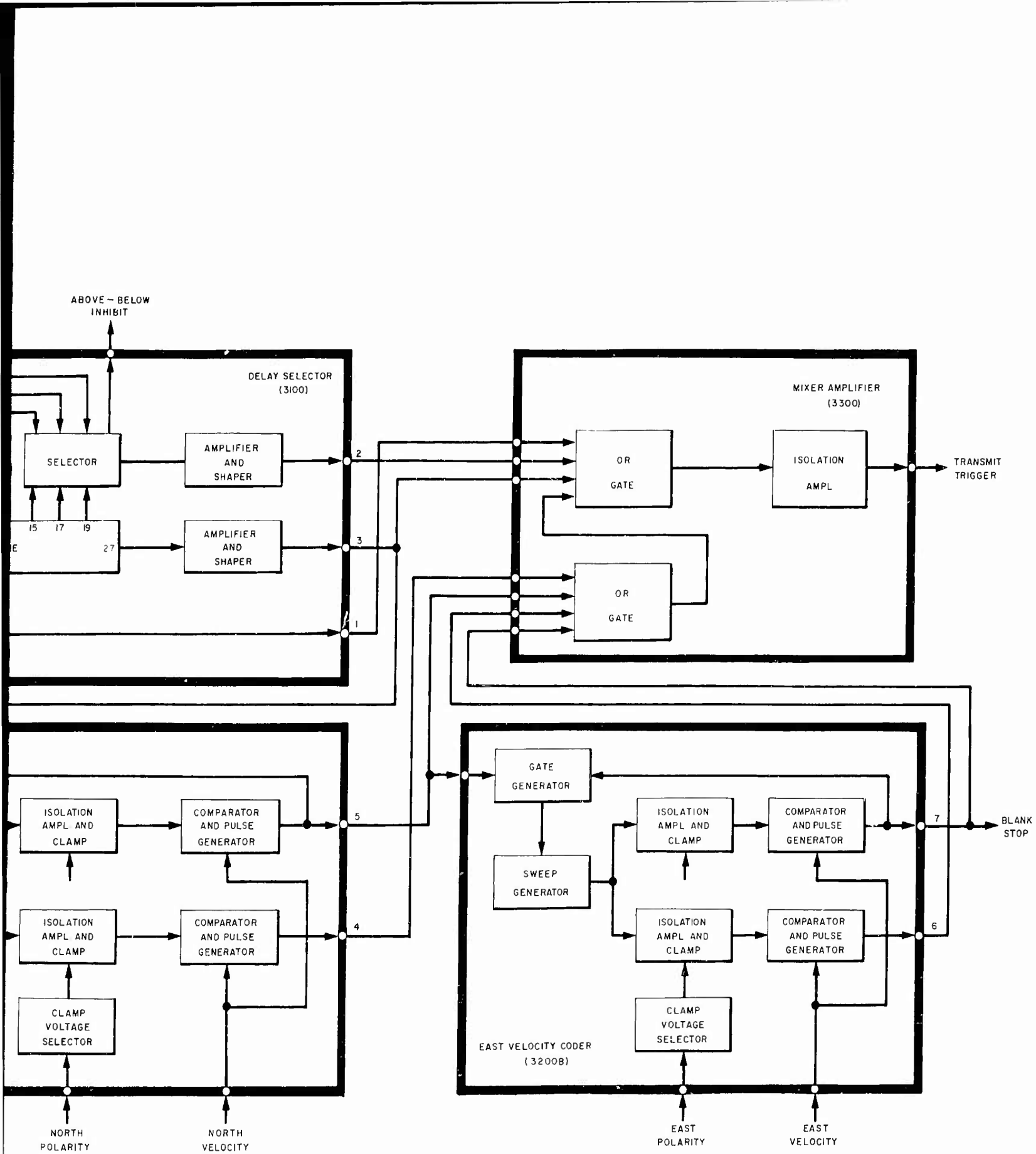


FIGURE 5-3
TRANSPONDER ENCODER (3000)

- pulse no. 3 is delayed by a fixed time from the reply trigger pulse and is coupled to the north velocity coder where it triggers a flip-flop gate generator which activates a linear sweep generator.

The voltage sweep of the linear sweep generator is coupled to two isolation amplifiers which prevent interaction of the pulse generating circuits with the sweep.

Pulse no. 5 is generated from a comparison between the linear sweep and a voltage proportional to the north velocity component of the aircraft. This pulse is initiated when the sawtooth sweep voltage exceeds the north velocity voltage and thus the delay of pulse no. 5 is proportional to the north velocity of the aircraft.

Pulse no. 4 is generated in a manner similar to pulse no. 5 except that the sweep signal is clamped to a different voltage level in accordance with the north polarity input. One of two clamp voltages is selected. Clamping of the sweep to a preset level provides an artificial sweep starting time and therefore a different delay period for any given velocity reference voltage. The clamp voltage selector can be set such that pulse no. 4 precedes pulse no. 5 by either four or six microseconds.

Pulse no. 5 is coupled to the flip-flop gate generator to reset the circuit and thus terminate the gate and sweep voltage. It is also coupled to the east velocity coder which acts in the same manner as the north velocity coder just described. Pulses no. 6 and 7 are generated in this unit in the same way that pulses 4 and 5 were generated in the north velocity coder.

Pulses 1 through 7 are coupled to the mixer-amplifier and combined into a single signal consisting of all seven pulses in time sequence. An isolation amplifier is used to provide a low impedance driving source of the 7-inch train.

Pulse no. 5 is generated from a comparison between the linear sweep and a voltage proportional to the north velocity component of the aircraft. This pulse is initiated when the sawtooth sweep voltage exceeds the north velocity voltage and thus the delay of pulse no. 5 is proportional to the north velocity of the aircraft.

Pulse no. 4 is generated in a manner similar to pulse no. 5 except that the sweep signal is clamped to a different voltage level in accordance with the north polarity input. One of two clamp voltages is selected. Clamping of the sweep to a preset level provides an artificial sweep starting time and therefore a different delay period for any given velocity reference voltage. The clamp voltage selector can be set such that pulse no. 4 precedes pulse no. 5 by either four or six microseconds.

Pulse no. 5 is coupled to the flip-flop gate generator to reset the circuit and thus terminate the gate and sweep voltage. It is also coupled to the east velocity coder which acts in the same manner as the north velocity coder just

described. Pulses 6 and 7 are generated in this unit in the same way that pulses 4 and 5 were generated in the north velocity coder.

Pulses 1 through 7 are coupled to the mixer-amplifier and combined into a single signal consisting of all seven pulses in time sequence. The 7-pulse train is shaped for use as a suppressor output signal.

The 7-pulse train is also delayed by a 0.8-microsecond delay line to provide the specified pretriggering time for the suppressor signal. This output is the transmit trigger.

4. Transponder Decoder

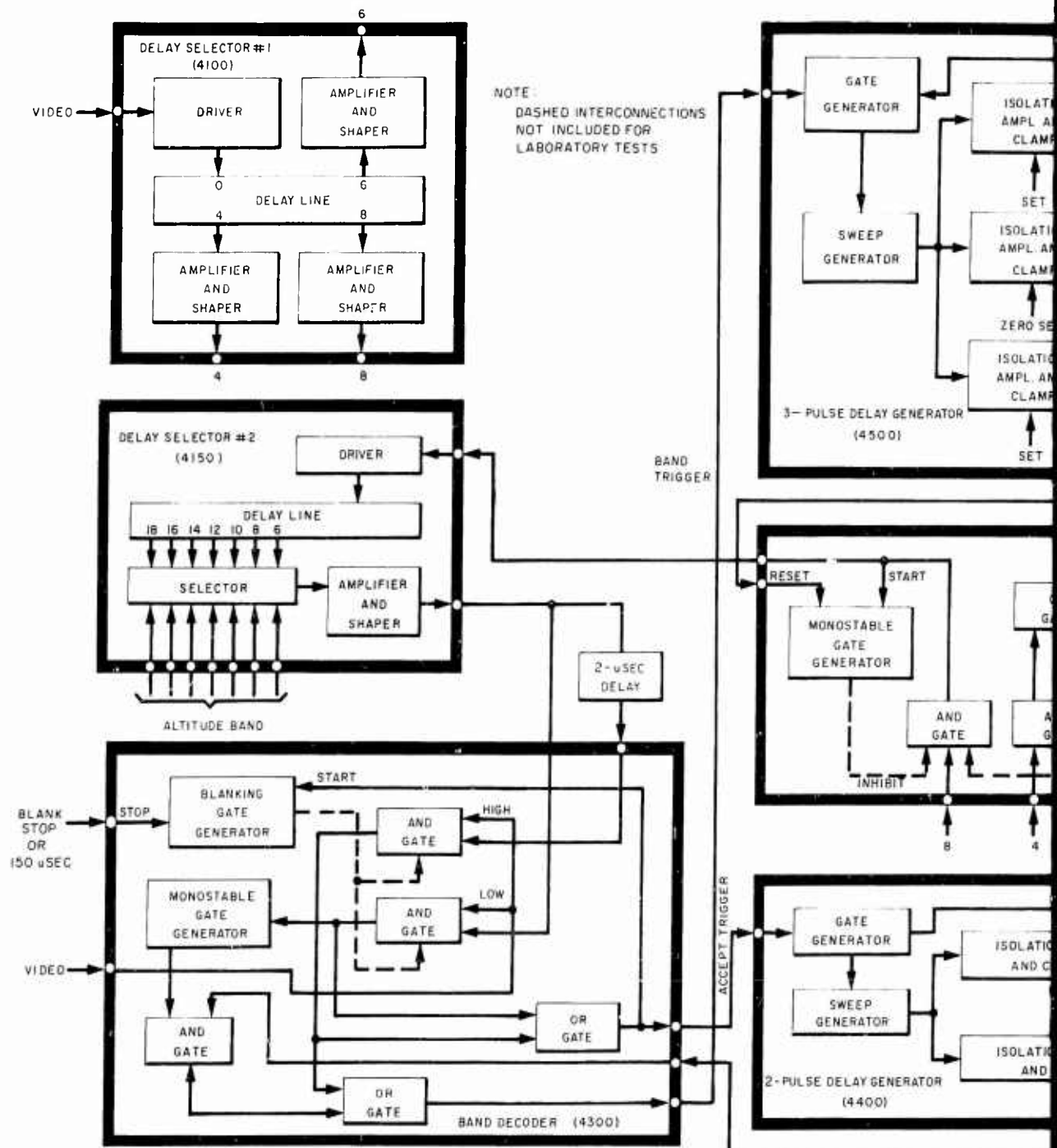
As shown in the block diagram, figure 5-4, the video pulse train is applied to the delay selector no. 1 where the entire signal is delayed by fixed times of 4, 6, and 8 microseconds. Separate outputs are provided for each delay time.

All three of these outputs are applied to the command decoder. Input no. 8 is compared with the undelayed video signal and if coincidence occurs between the undelayed video and the 8-microsecond delayed signal an output pulse is generated.

This coincidence output (coincident with interrogation pulse no. 2) is routed to the delay selector no. 2 where it is delayed an amount corresponding to the coarse altitude band of the transponder aircraft, as selected by the coarse altitude code wheel of the transponder aircraft. The delayed pulse is amplified, shaped, and coupled to the band decoder.

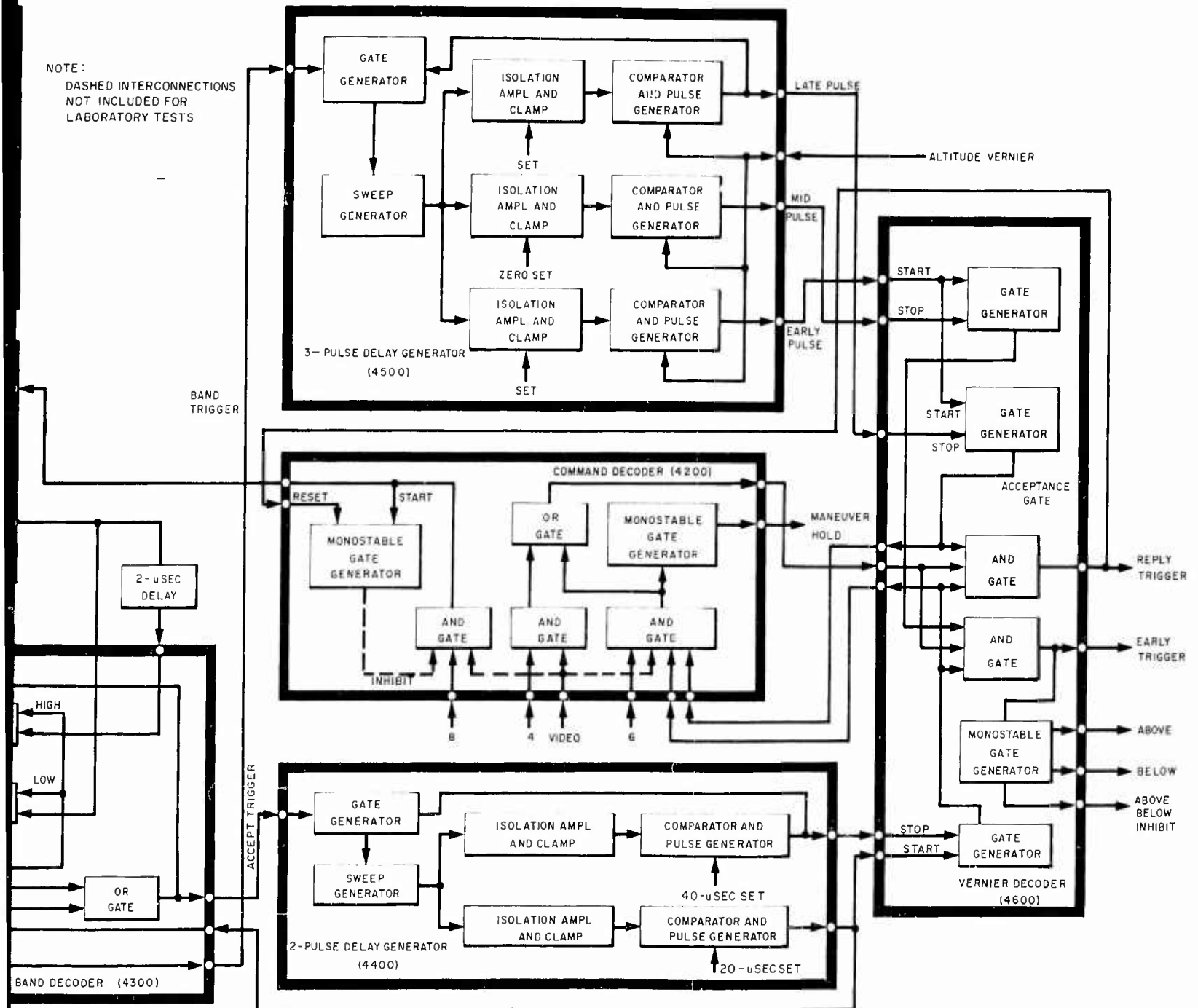
The band decoder unit compares the delayed output signal with the video pulses to determine if the video signal corresponds to either the selected altitude band or the band above. Comparison for the selected altitude band is performed in an AND gate which produces a low band output trigger pulse. For the band above the selected band, the delayed input signal is delayed an additional two microseconds and compared with video in another AND gate to produce a high band output trigger pulse. Both low band and high band output triggers are applied to an OR gate to produce the accept trigger signal. Both of these AND gates are blanked by a signal from the blanking gate generator.

The output trigger from the low band AND gate also triggers a 30-microsecond monostable multivibrator. A pulse delayed by 20 microseconds (from the two-pulse delay generator) is compared with this gate in an AND gate. The output of this AND gate is coupled to an OR gate in addition to the high band output trigger, to generate a band trigger pulse for triggering the three-pulse delay generator. With this technique the trigger for the three-pulse delay generator occurs at the time of the third input video pulse if the input code corresponds to the higher altitude band, and at 20 microseconds later than the third input video pulse if the input code corresponds to the same altitude band as that selected by the sensor.



1

NOTE:
DASHED INTERCONNECTIONS
NOT INCLUDED FOR
LABORATORY TESTS



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FIGURE 5 4
TRANSPONDER DECODER (4000)

The two-pulse delay generator is triggered by the accept trigger from the band decoder. This unit generates two pulses delayed 20 microseconds and 40 microseconds from the accept trigger. The generator is reset by the 40-microsecond delayed pulse.

The three-pulse delay generator is triggered by the band trigger pulse and generates three delayed pulses by means of a linear sweep generator. The altitude vernier control voltage from the altitude sensor is coupled to the three comparator circuits and controls the time delay of the three pulses. Delay of the middle pulse is proportional to the altitude vernier voltage. Delay of the early and late pulses is controlled by the clamp voltages set to obtain the required guard band.

The vernier decoder contains gating circuits for accepting or rejecting the altitude vernier pulse signal. An early gate is initiated by the early pulse and terminated by the middle pulse. An acceptance gate is also started by the early pulse, but terminated by the late pulse. These gates are coupled to two AND gates which are also gated by a 20-microsecond video gate. The video gate is positioned to accept only signals which occur within the altitude vernier code time interval. The vernier trigger pulse is also applied to the two AND gates. If coincidence with the acceptance gate occurs, a reply trigger is generated, and if coincidence with the early gate occurs an early trigger is generated. If an early trigger is generated, a monostable gate generator is set, indicating an above state to the transponder encoder. An absence of early trigger denotes below similarly.

The acceptance and video gates are also applied to an AND gate in the command decoder to determine if a maneuver command exists. Coincidence of the fifth interrogation pulse with a fourth pulse delayed six microseconds by the delay selector no. 1 in the presence of the acceptance and video gates sets the maneuver command monostable gate generator.

5. Interrogator Computer

The interrogator computer evaluates collision threats based on decoded and locally derived data and, if a risk exists, provides the intelligence to activate the appropriate maneuver display. A signal schematic of the computer is shown in figure 5-5.

The airspeed of the interrogating aircraft is resolved with respect to relative antenna bearing in the relative bearing servo. Inputs to the relative bearing motor amplifier, in addition to the bearing error signal, include:

- a heading error signal from the local transponder heading servo which cancels high frequency components of aircraft motion, resulting in data referenced to the average heading of the aircraft
- a fixed bias to compensate for the steady state velocity lag in the servo due to the 30-rpm antenna scan speed.

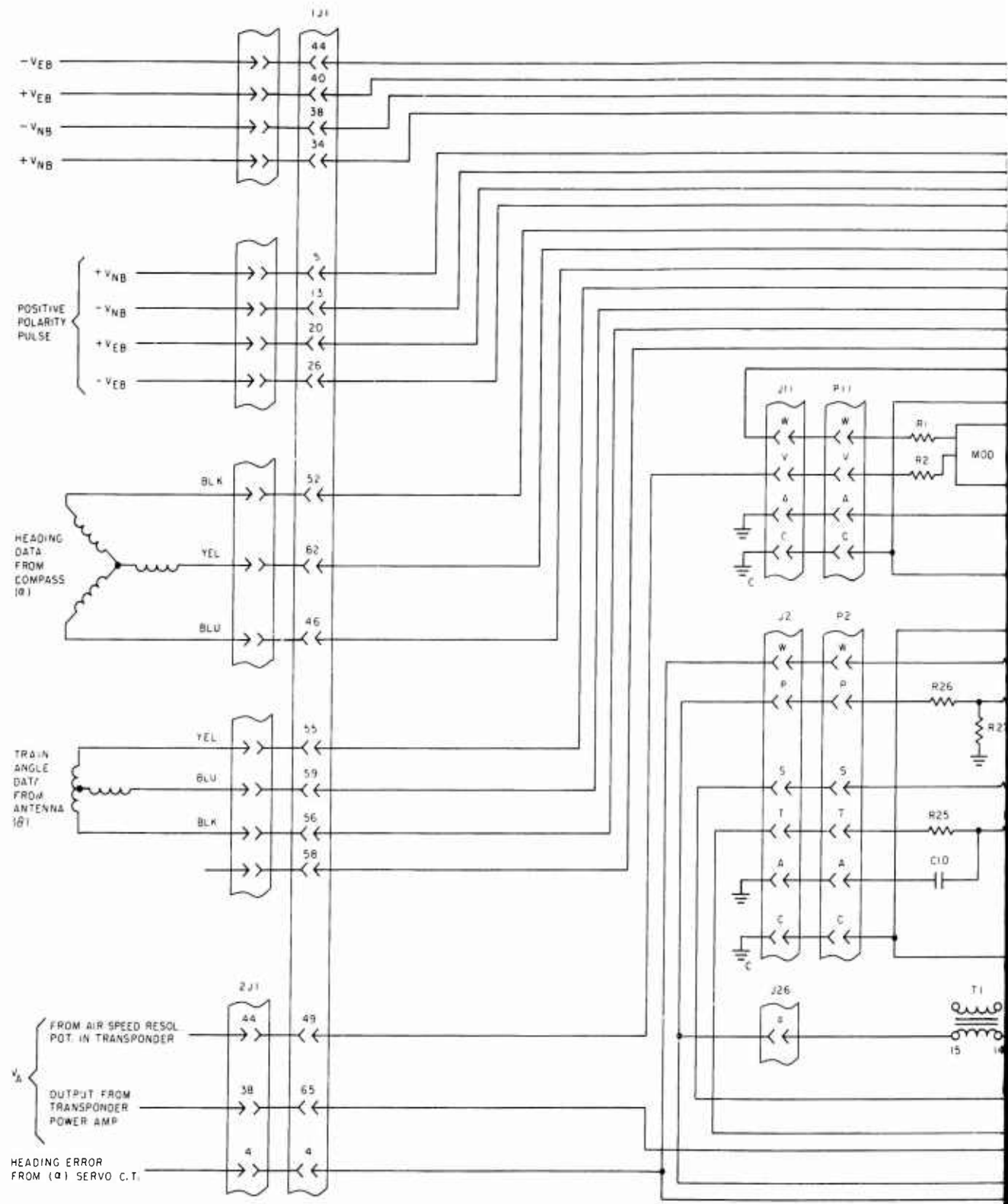
The decoded components of the transponding aircraft's airspeed are resolved with respect to antenna magnetic bearing in the magnetic bearing servo. The polarity of the airspeed components applied to the resolver is selected in the polarity control amplifier based on decoded reply data. The heading error signal from the local transponder is applied to this motor amplifier in reversed sense to recover the high frequency components, resulting in instantaneous data with respect to the external reference (magnetic north). The fixed bias is also applied as an input here to compensate for steady state velocity lag.

The resolver outputs constitute components of both aircraft's velocities normal to and parallel to the antenna bearing. The normal and radial components are summed with proper polarities in the normal velocity and radial velocity adders, respectively, to yield the corresponding components of the relative velocity between aircraft. Normal velocity signals are scaled so that the adder limits velocity samples to about 133 knots. This limit will not effect valid data in a collision or near collision case, but will minimize the effect of a single large error in the subsequent averaging process.

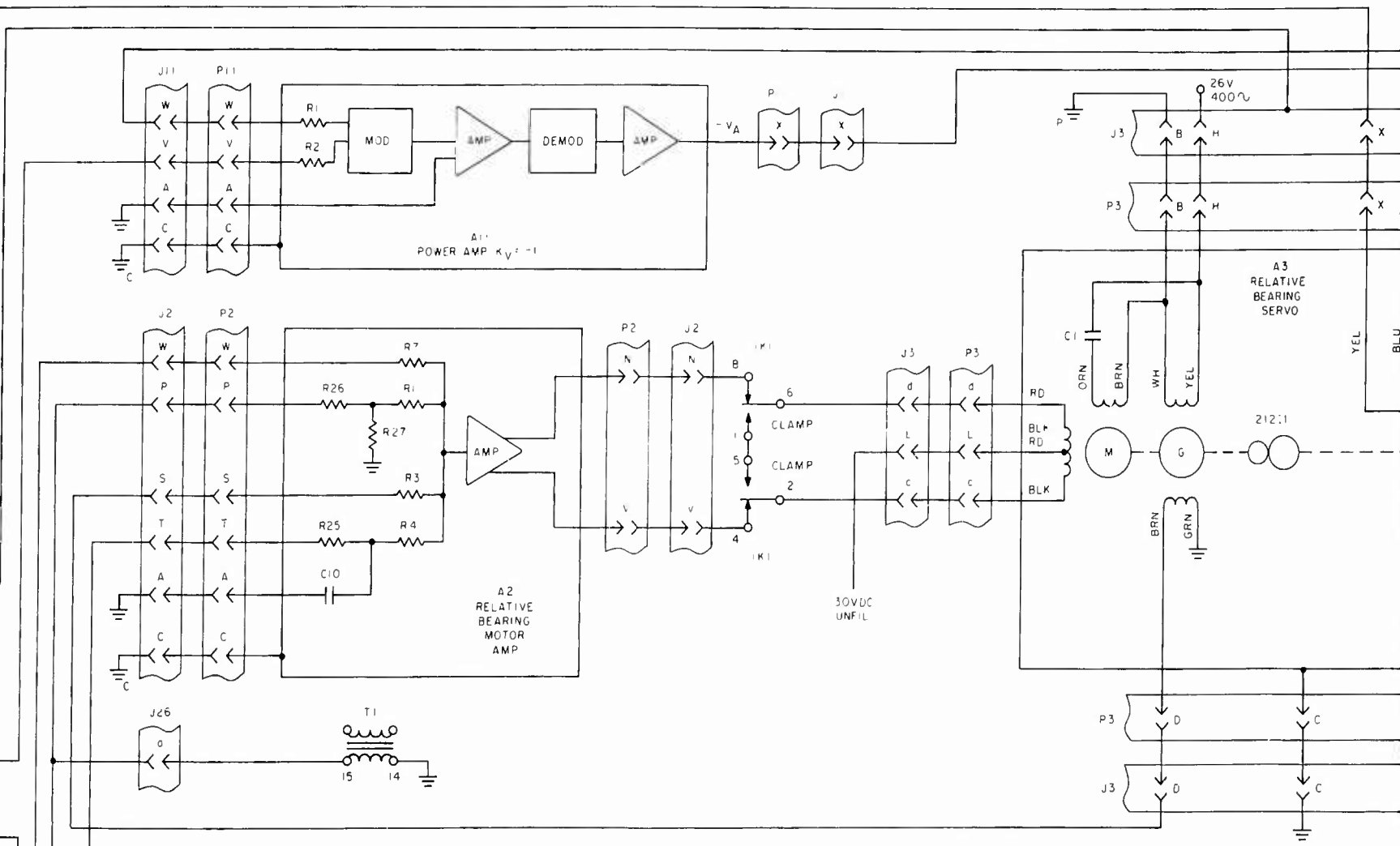
The radial component of relative velocity is scaled by a voltage divider in the range criterion comparator to analogs of the ranges which would be covered in 27 and 40 seconds. These range analogs are compared with the analog of actual range to determine the increment in which time-to-go lies. Actual range is also compared with a fixed 1/3 nautical mile bias to determine whether the minimum range limit has been violated. The results of these comparisons are the decisions on time-to-go and minimum range used in the Maneuver Logic.

Successive samples of the normal velocity and the velocity threshold (45 knots) analogs are summed in the normal velocity and velocity threshold integrators, respectively. The samples are gated in by the sample gate controller each time a complete reply is received, as indicated by the sample gate signal. The sums are read out and the integrators reset on leaving a given target, as indicated by the occurrence of two consecutive misses or a range change of more than 0.36 nautical miles. The derivation of the reset control signals is described below.

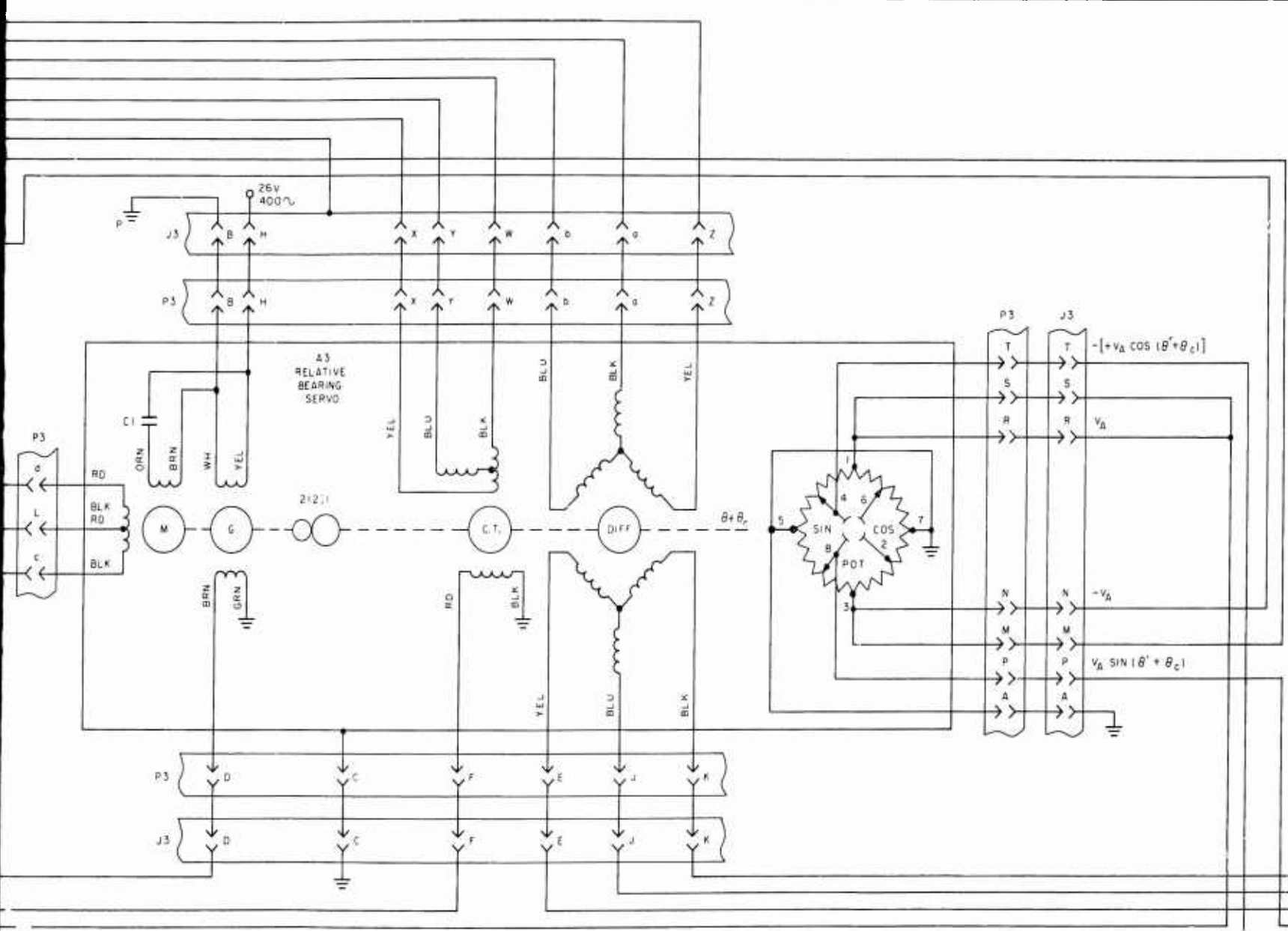
The sums of the normal velocity samples and the velocity threshold samples are compared in the normal velocity criterion comparator to evaluate the collision threat. This comparison is equivalent to comparing the normal velocity sample closest to the beam center with the velocity threshold, and this effectively locates the antenna beam centerline. It also has the added advantage of averaging out errors in the received velocity data. The result of this comparison is a decision on whether or not a collision threat exists, used in the Maneuver Logic. The output of the velocity threshold integrator is also compared with a fixed bias corresponding to more than two samples (about 100 knots). The result of this comparison is used to inhibit collision decision outputs based on one or two samples only.



1

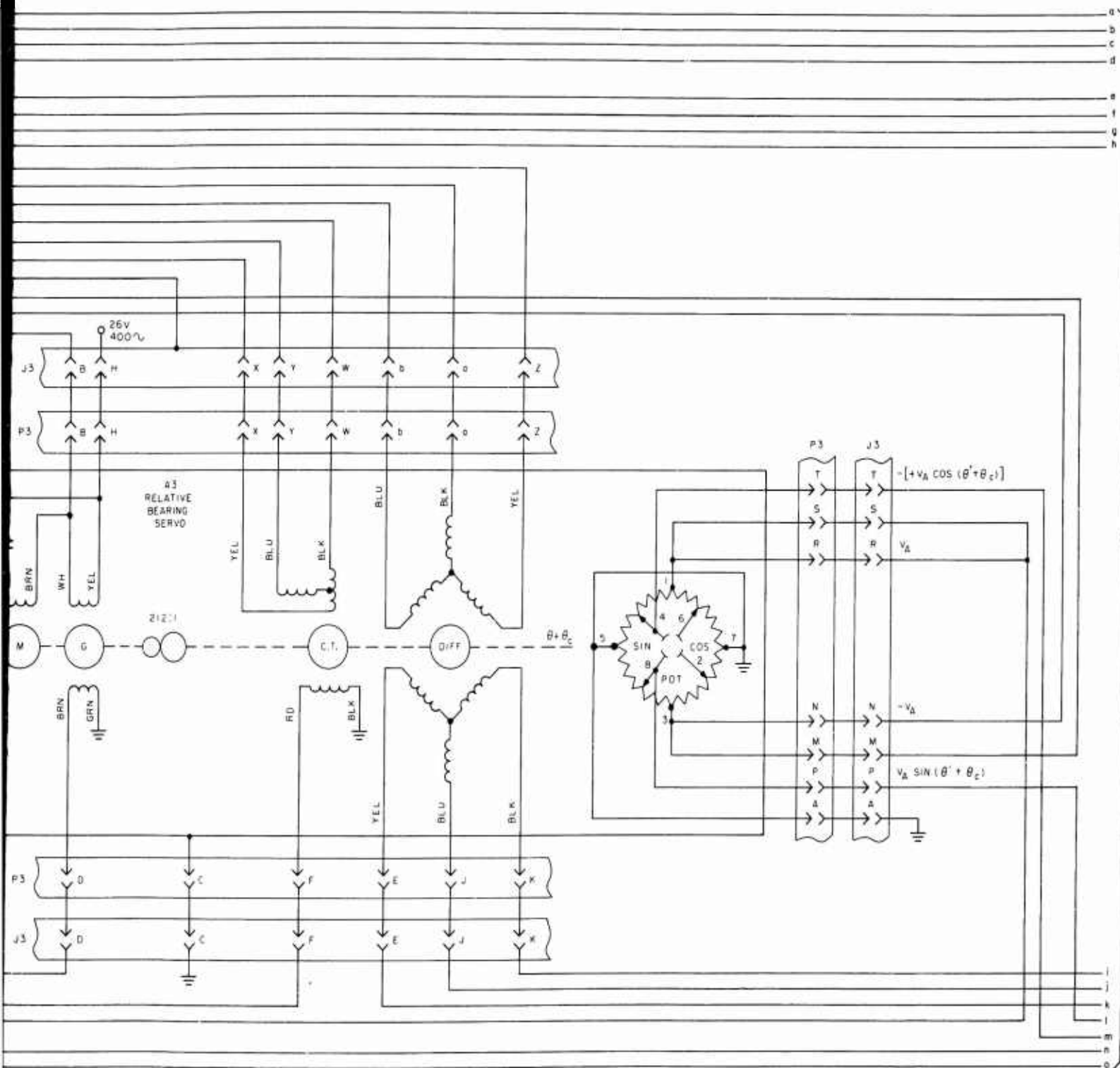


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FIGURE 5-5
INTERROGATOR COMPUTER SIGNAL SC
(SHEET 1 OF 4)

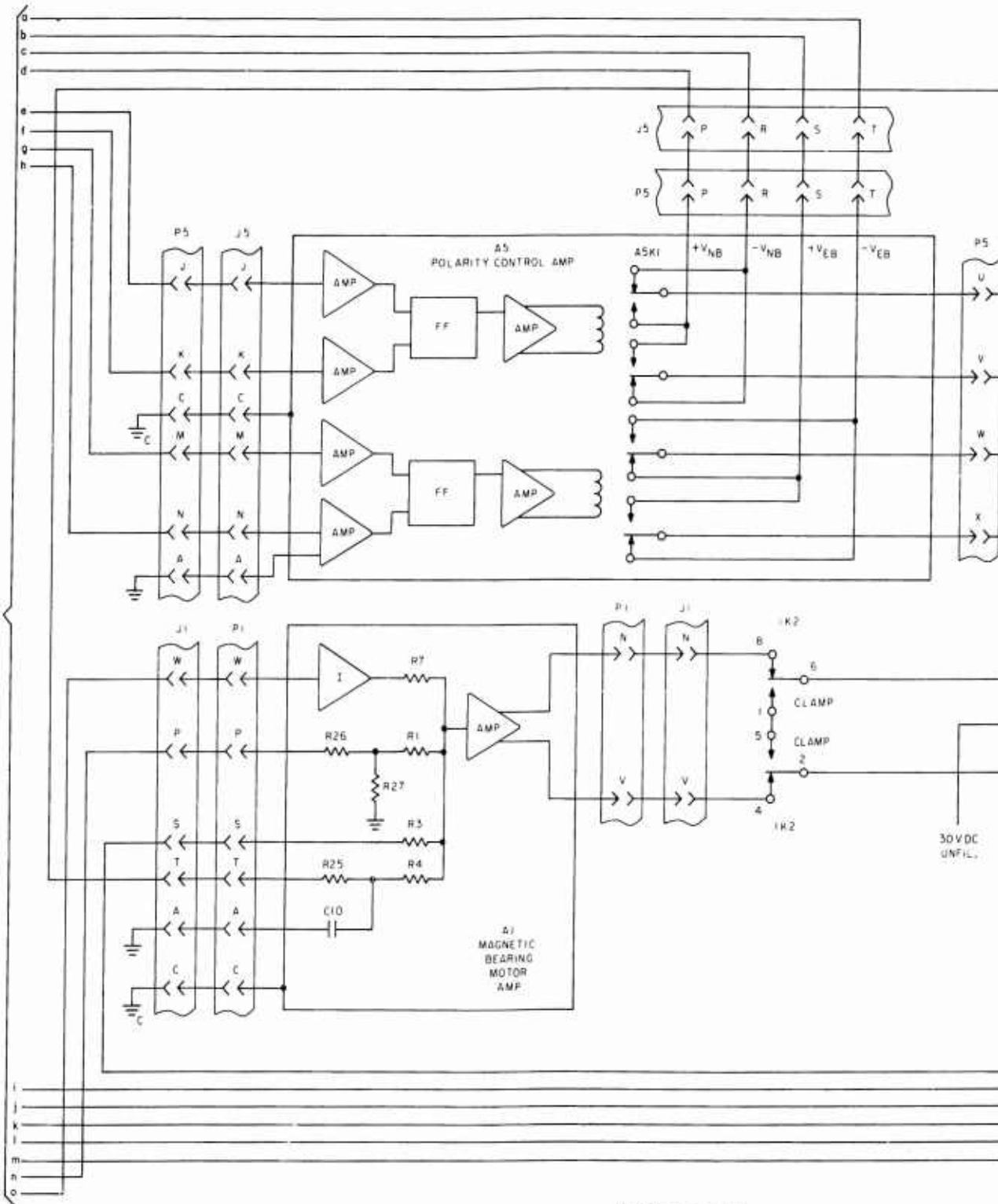


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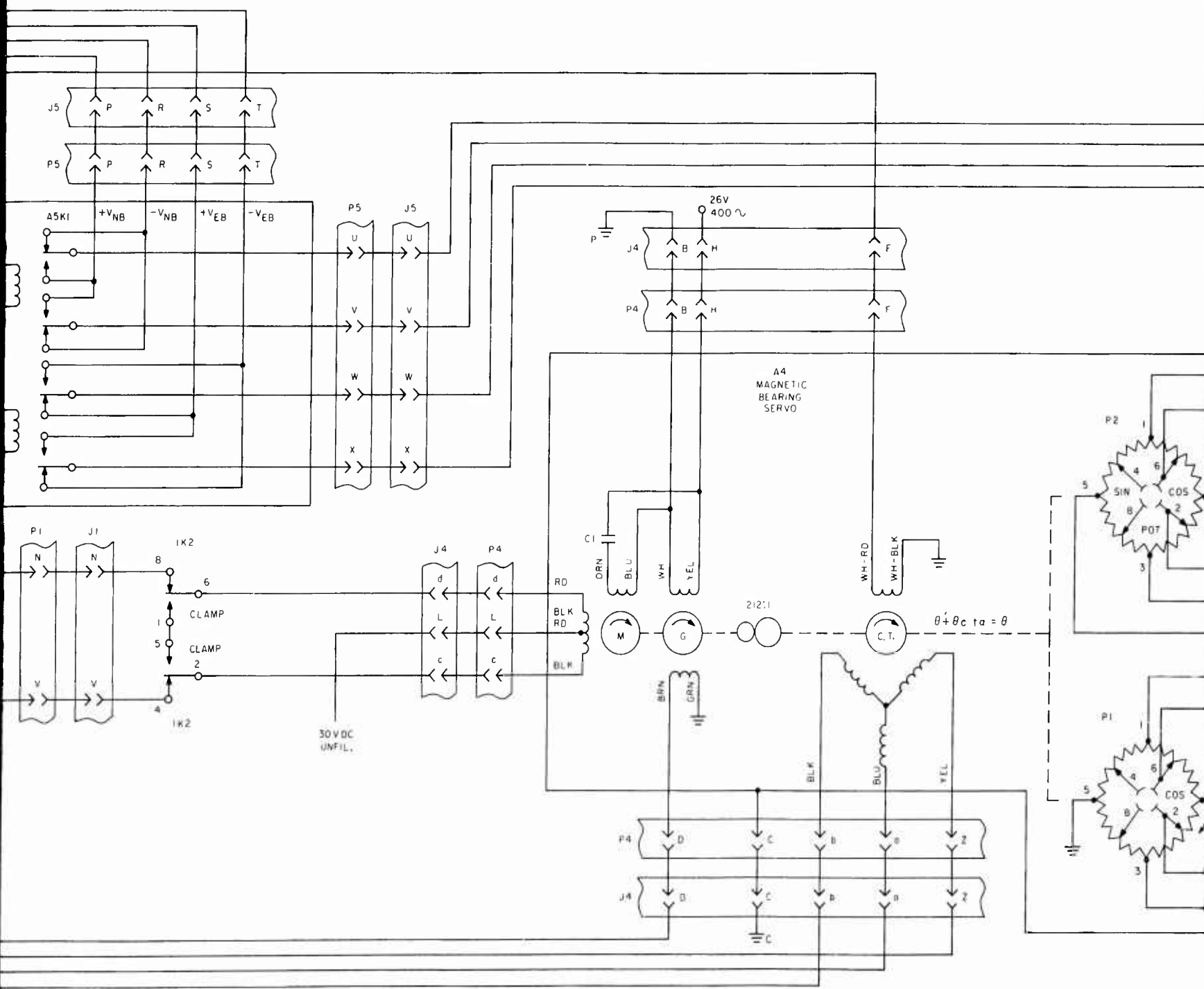
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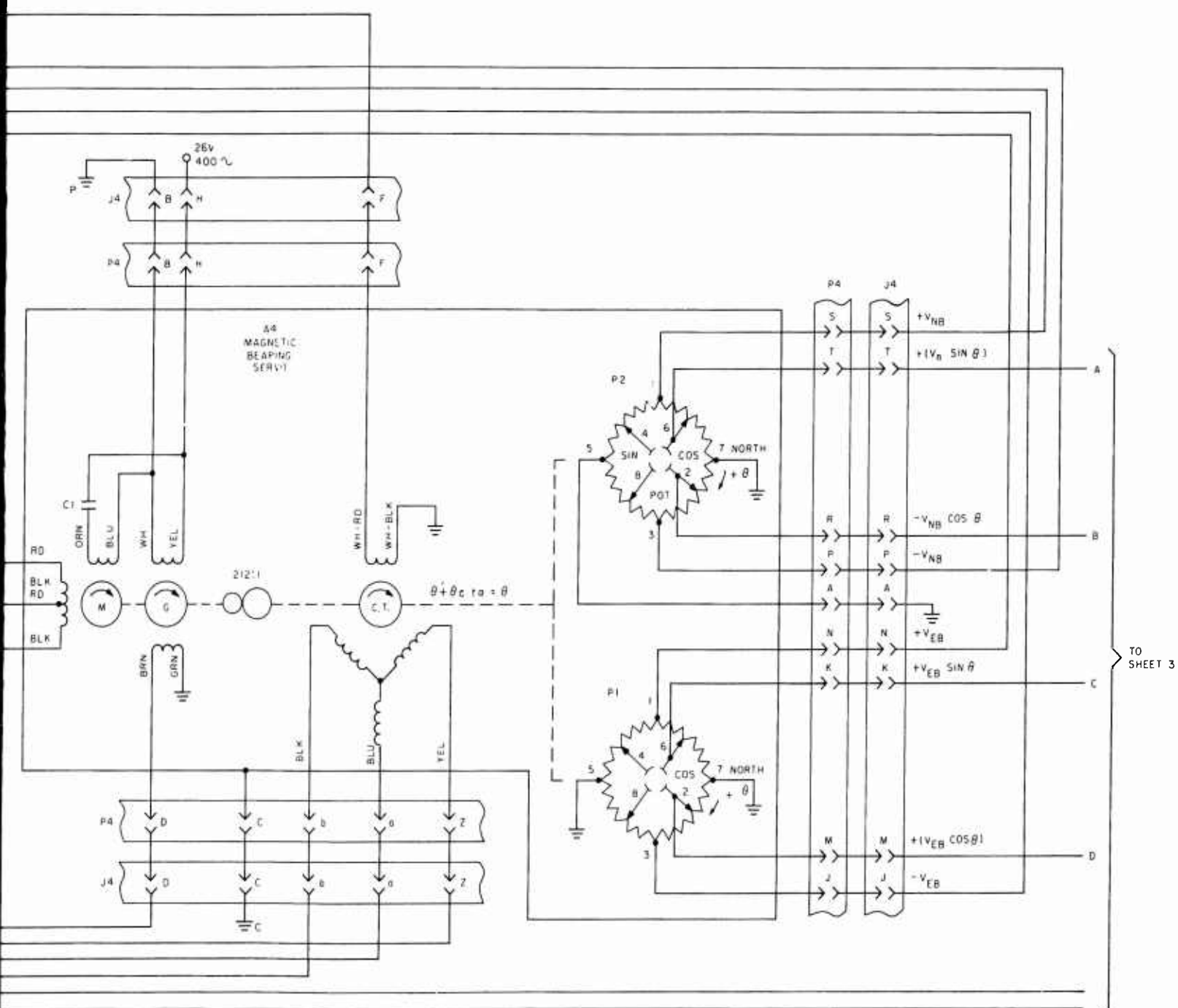
FIGURE 5-5
INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 1 OF 4)

CONTINUED FROM SHEET 1



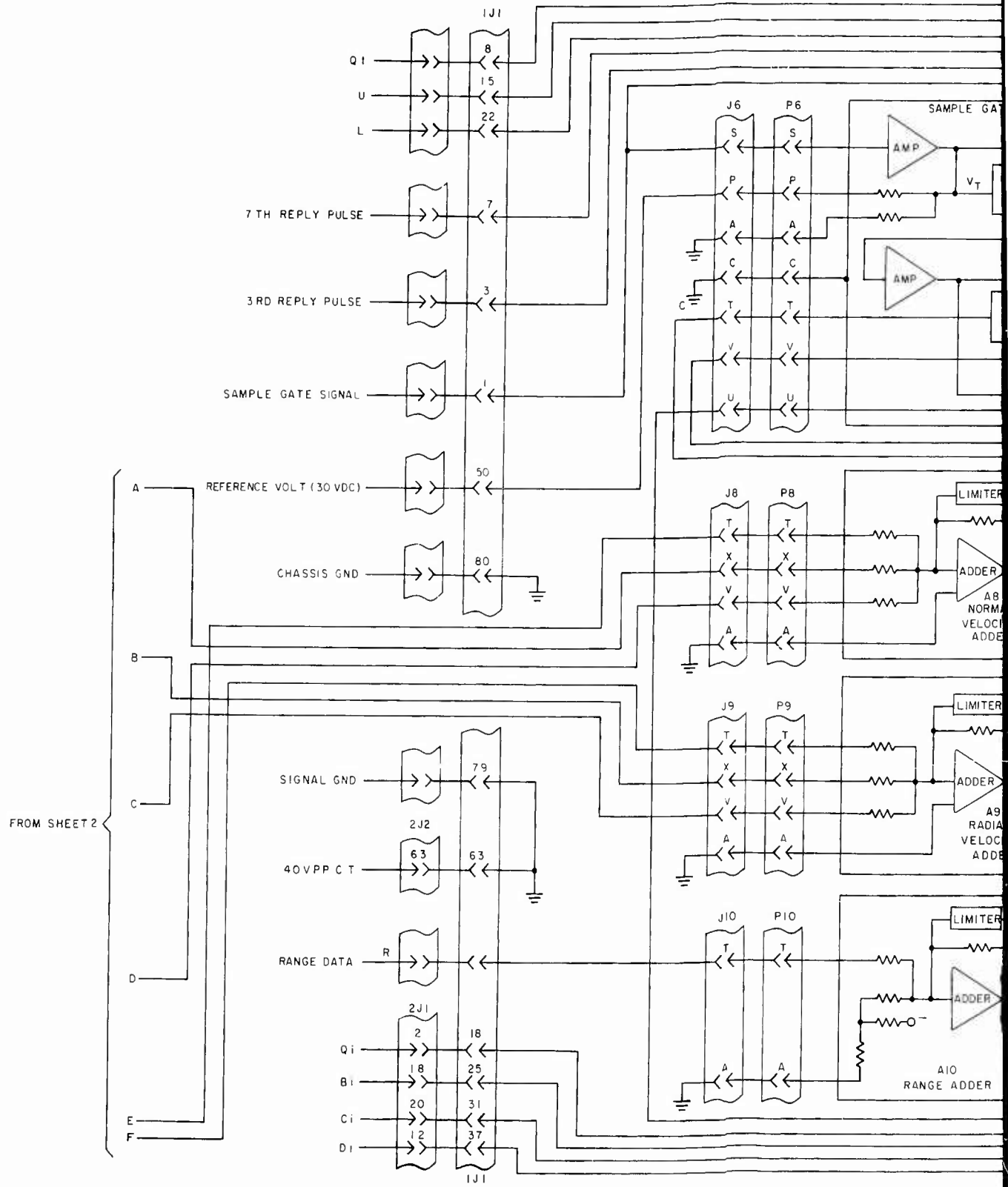
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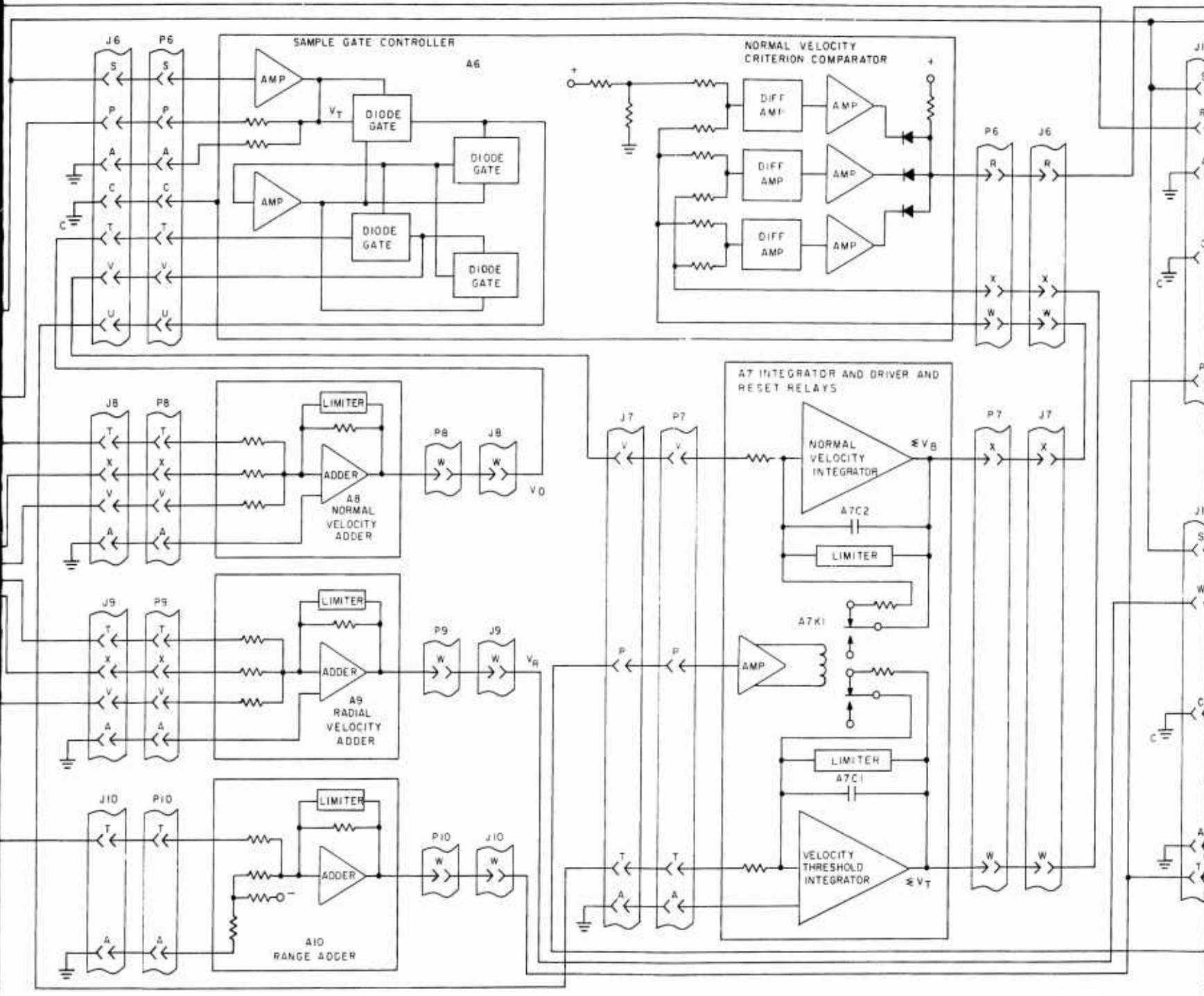


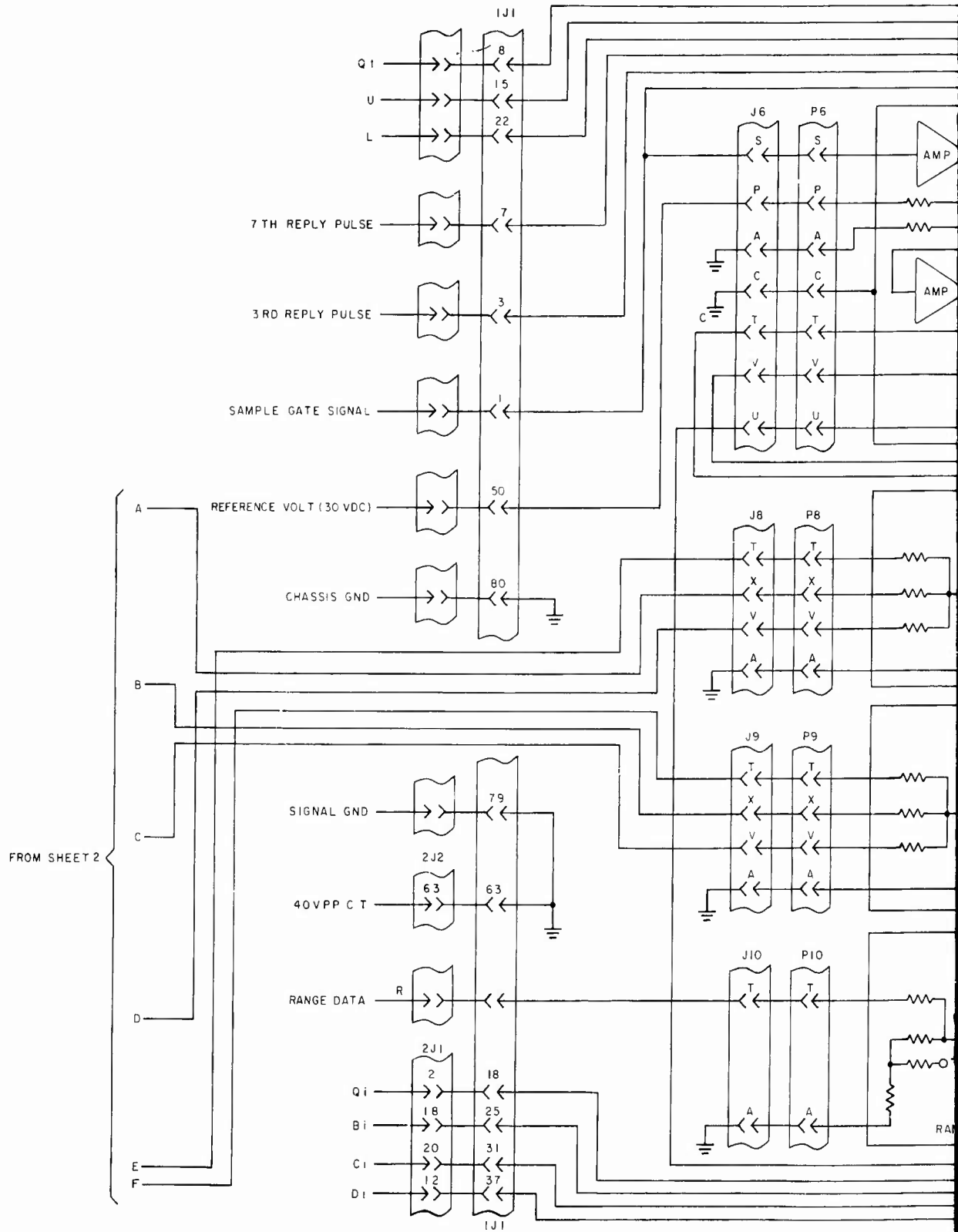
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FIGURE 5-5
 INTERROGATOR COMPUTER SIGNAL SCHEMATIC
 (SHEET 2 OF 4)

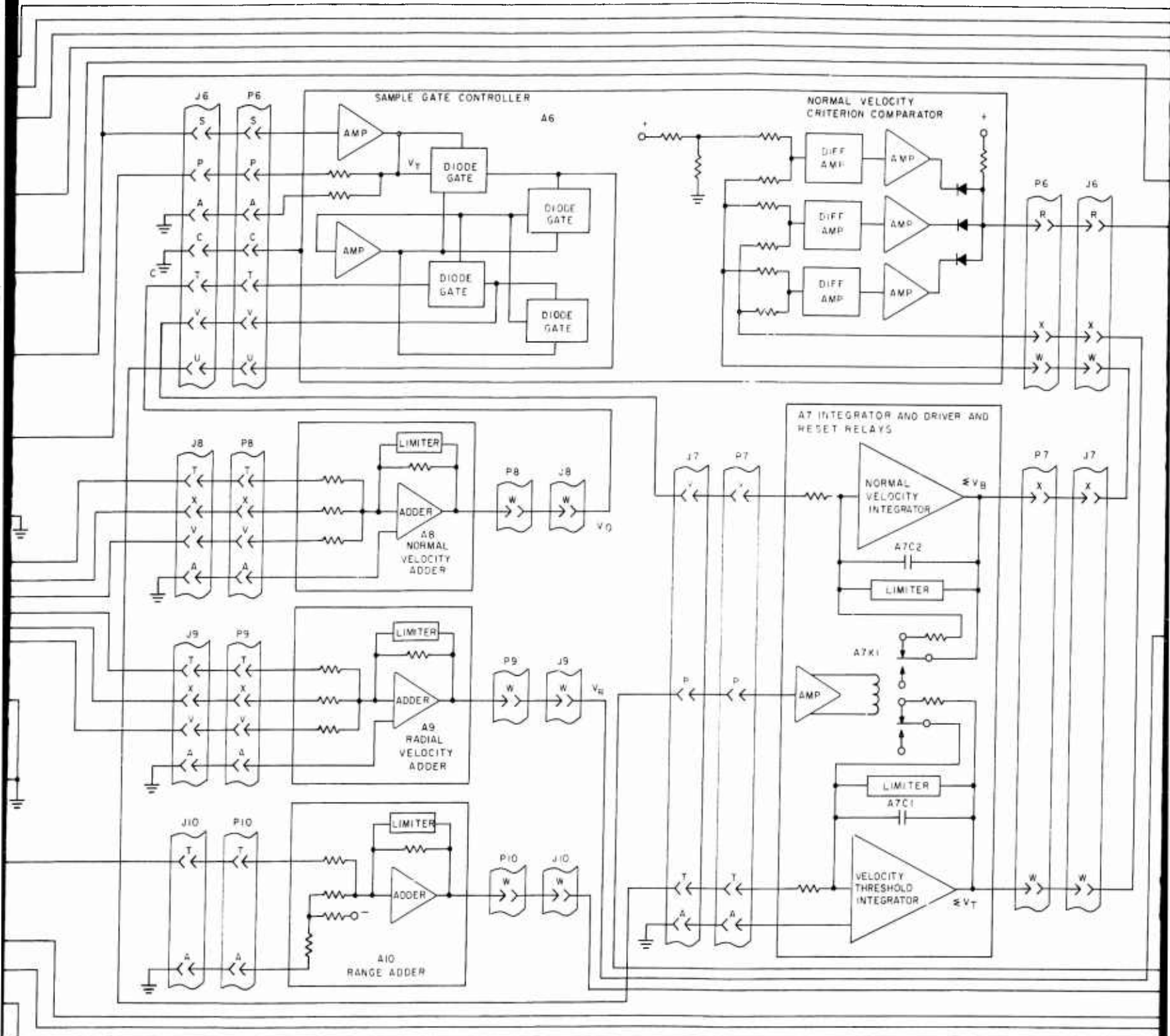


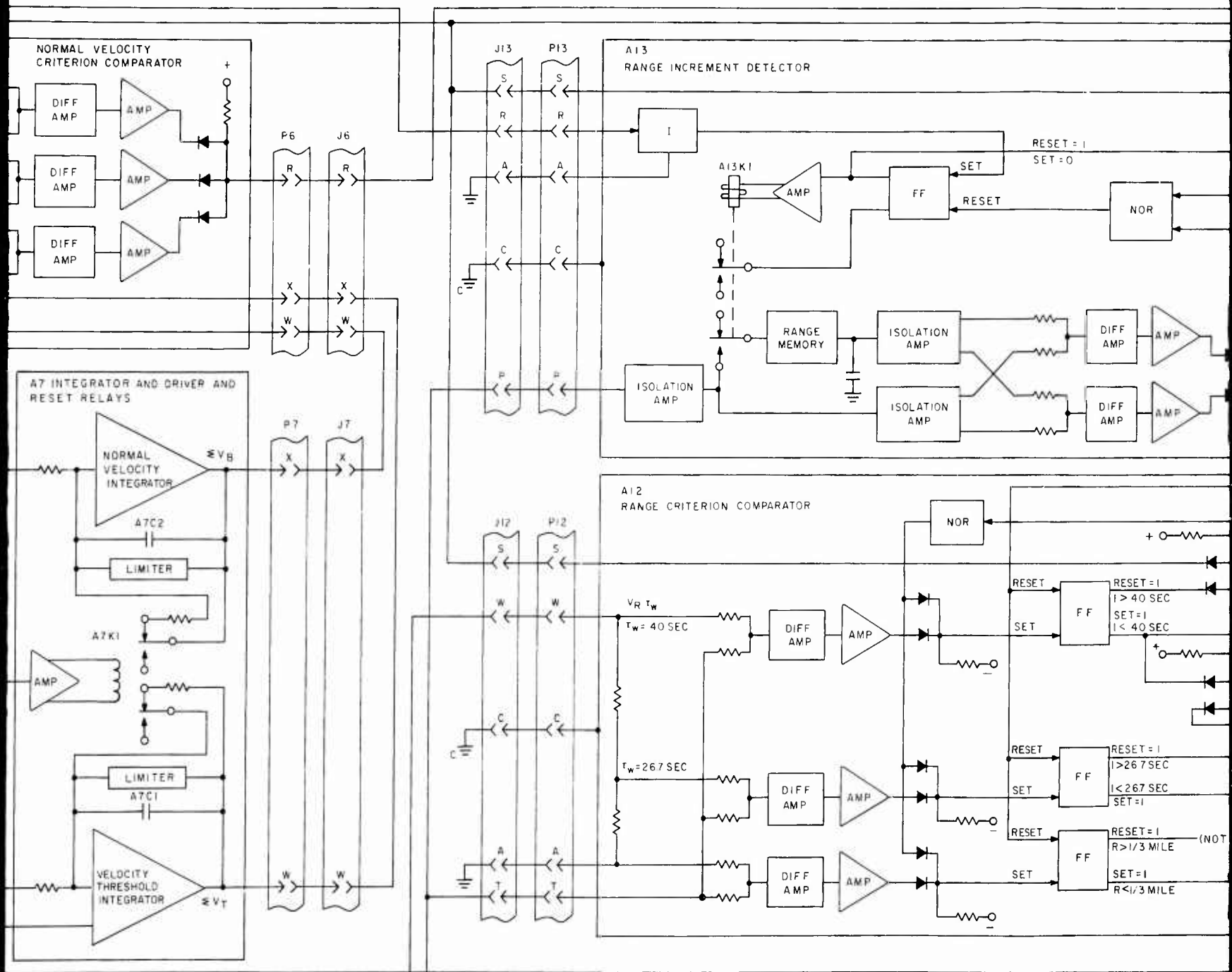
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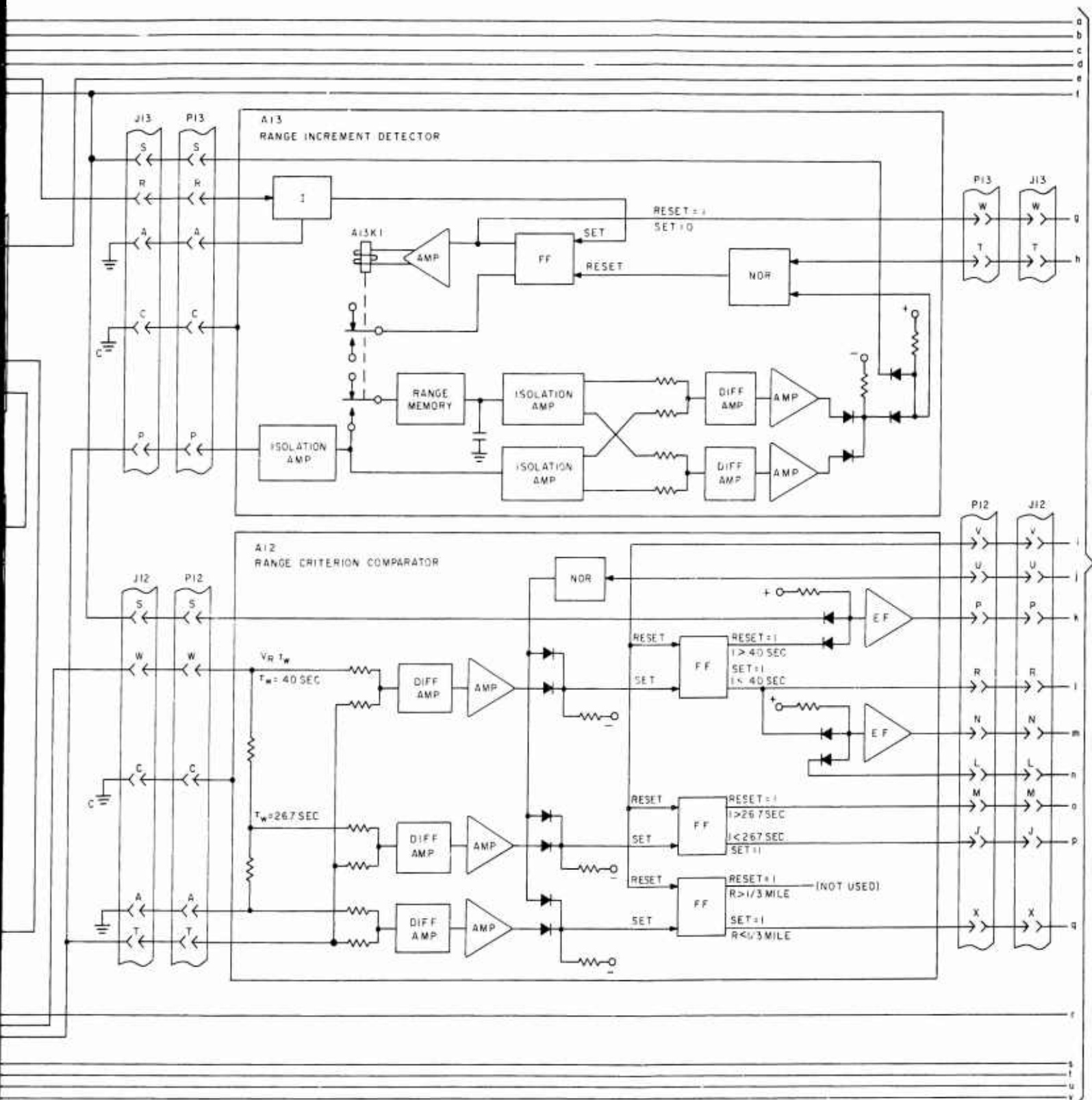




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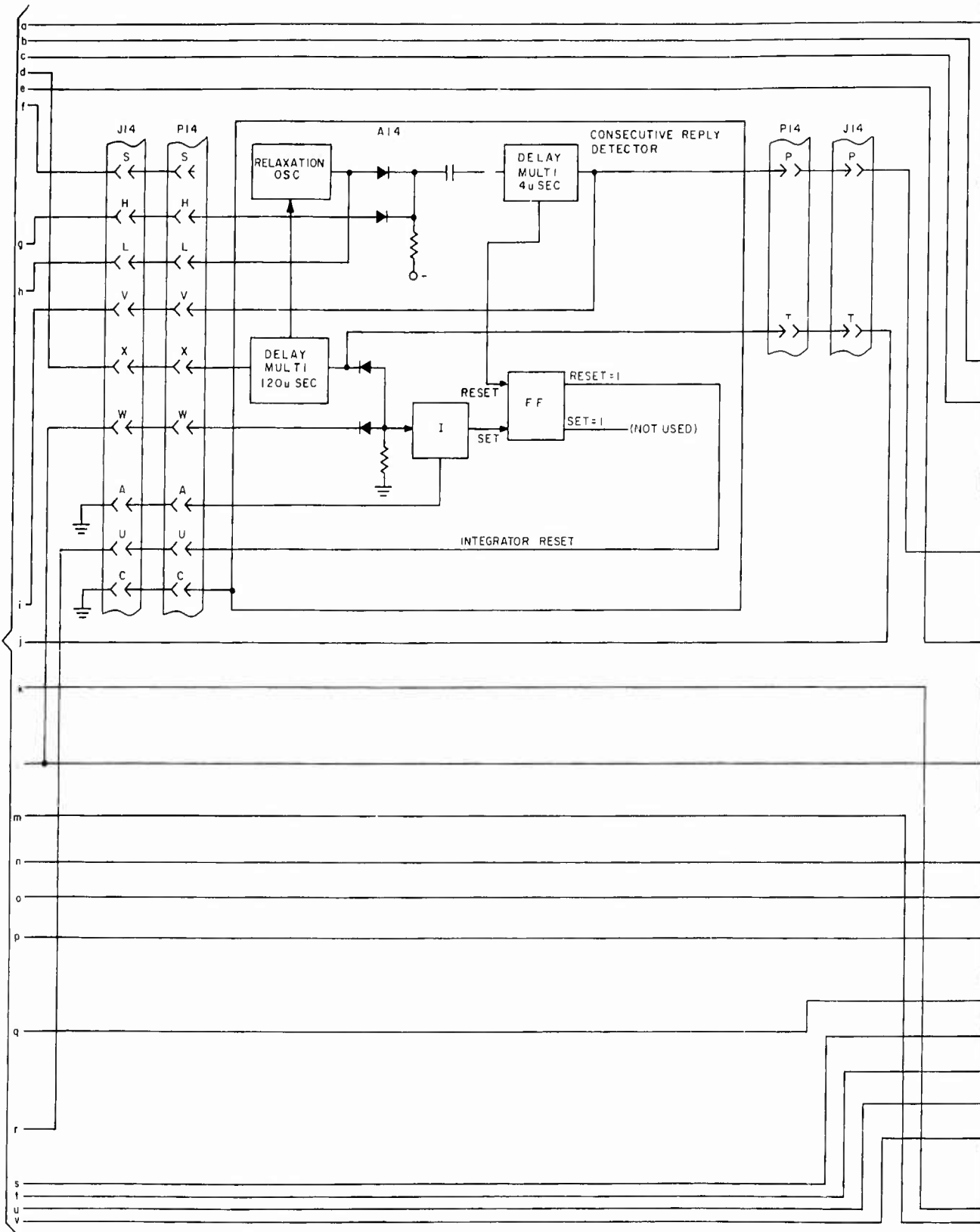


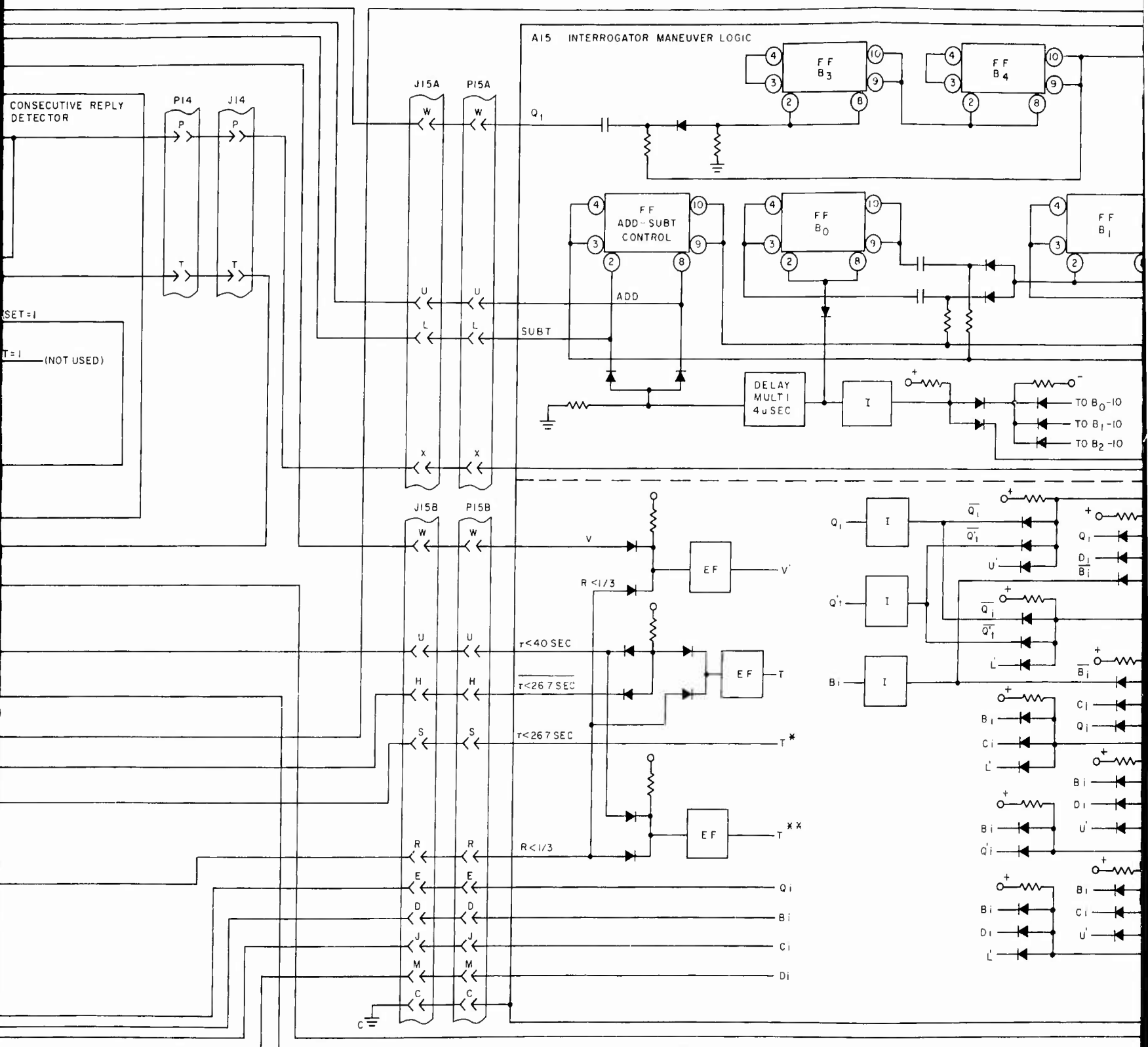
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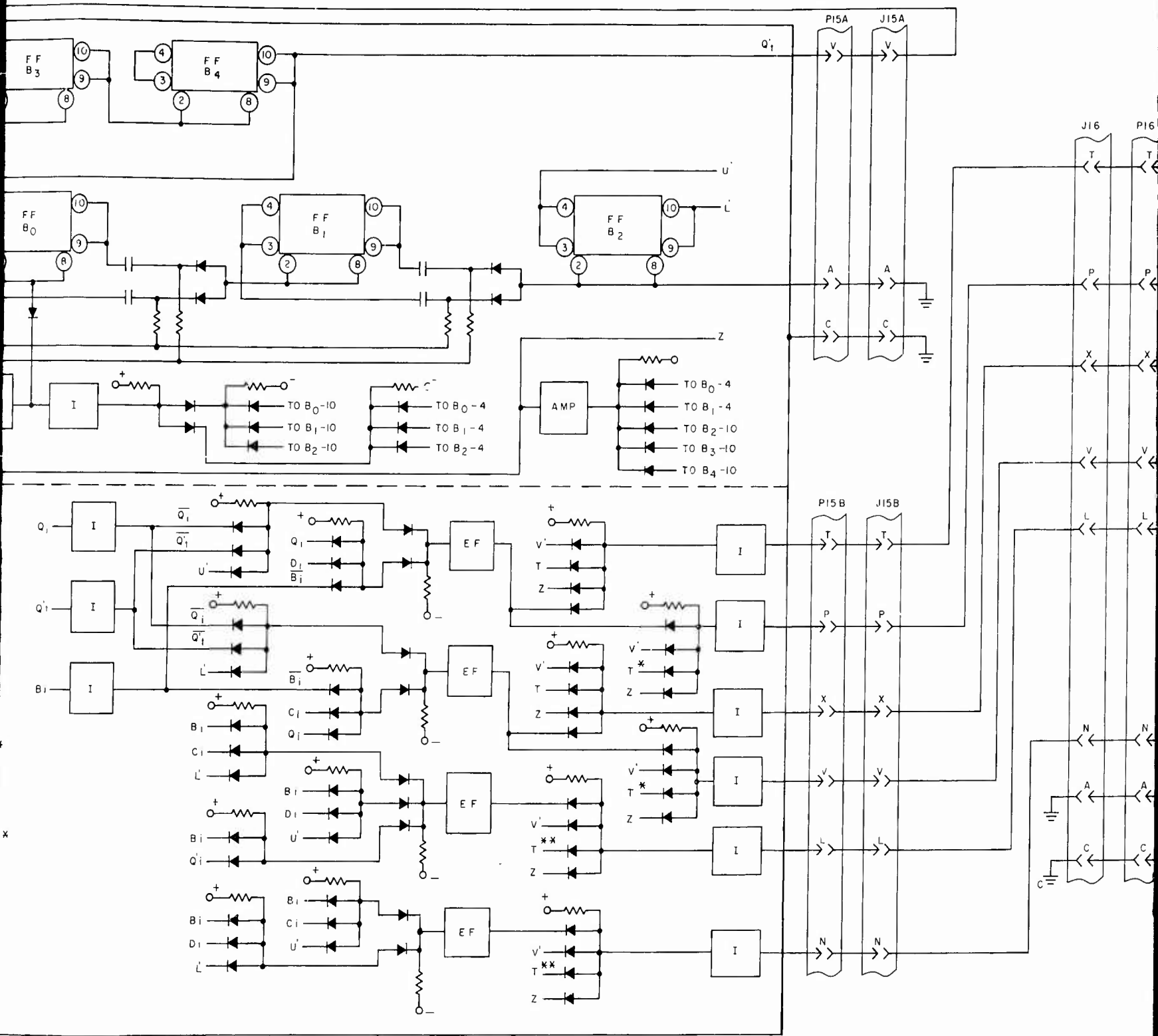
FIGURE 5-5

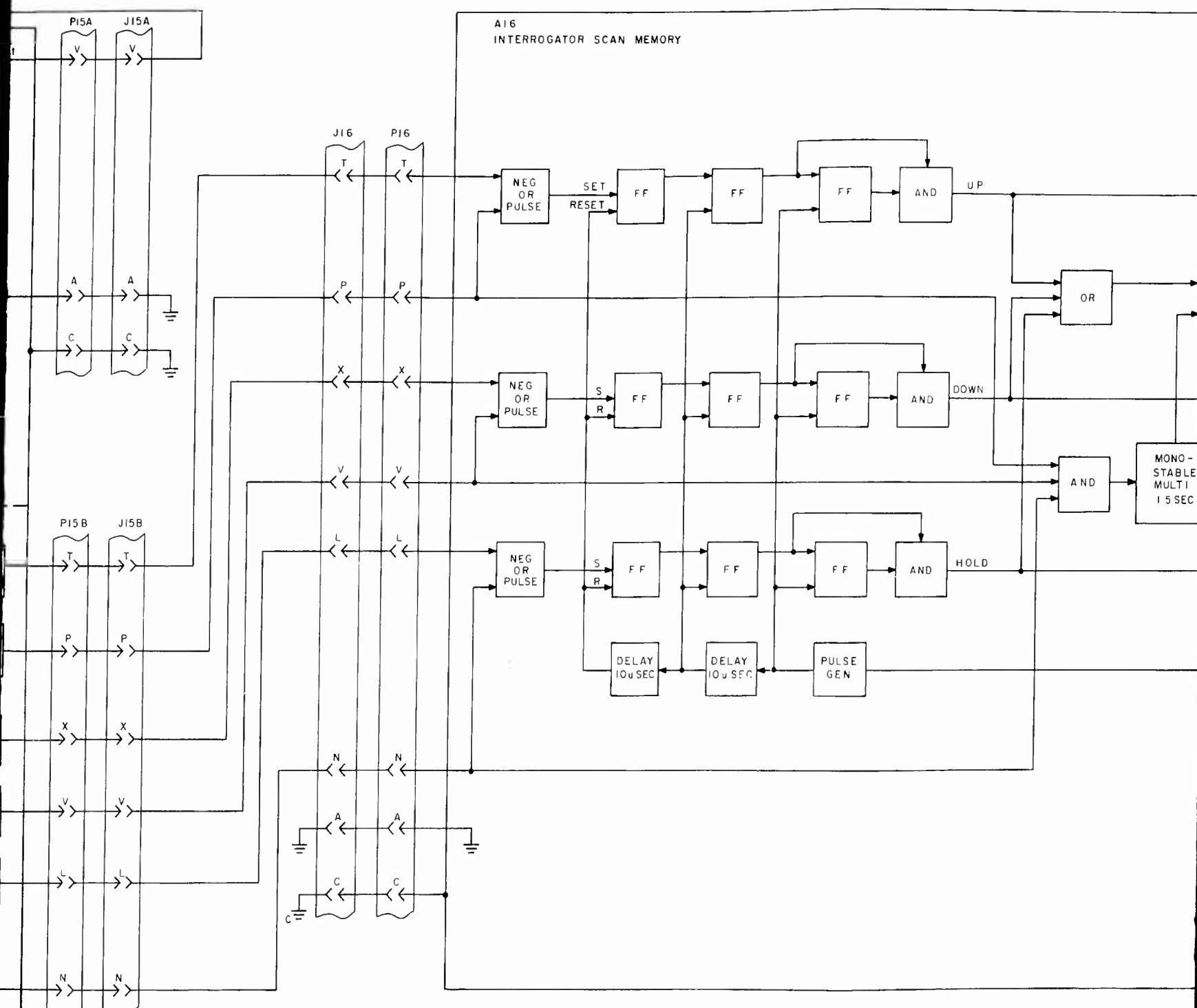
INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 3 OF 4)

CONTINUED FROM SHEET 3









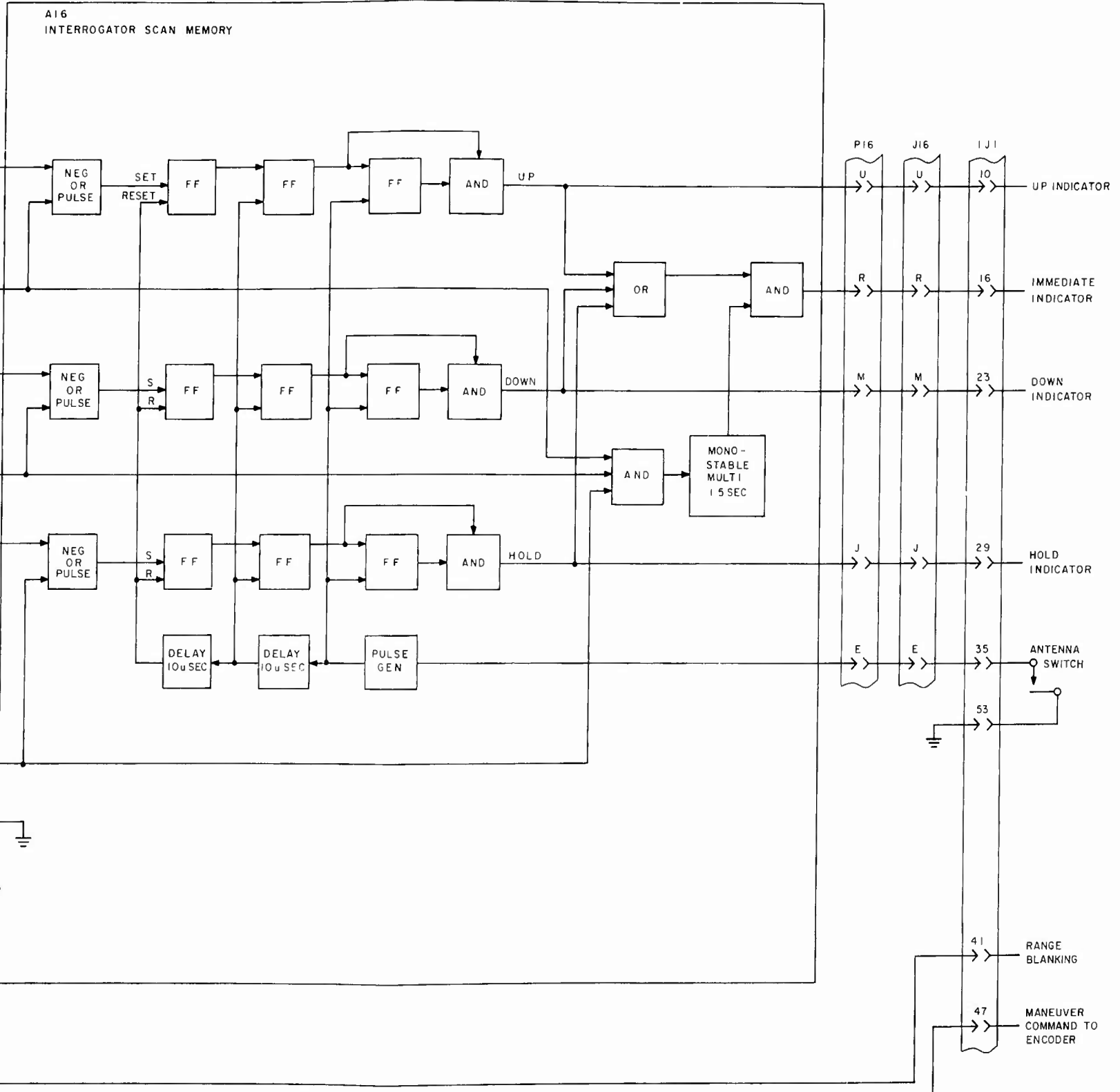


FIGURE 5-5
INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 4 OF 4)

Reset of the velocity integrators is controlled by the flip-flop in the integrator reset circuits which is set whenever a reply is received for which the derived time-to-close is less than 40 seconds. This input is inhibited until 120 microseconds after the receipt of the last reply pulse to assure that derived time-to-close has reached steady state. Reset stimuli are obtained from the range increment detector and the consecutive reply detector, described below.

The consecutive reply detector contains a relaxation oscillator having a period of more than two interrogation intervals (more than 10 milliseconds). Completion of the relaxation cycle produces an integrator reset output. The oscillator is recycled by each sample gate, thus inhibiting an output unless two consecutive sample gates are missing.

In the range increment detector, the range derived from the first reply from an intruder is stored in a range memory. Further inputs to the memory are inhibited about one millisecond after the receipt of the third reply pulse, the delay being inherent in the relay which does the switching. The circuit is reset either by an output from the consecutive reply detector or an output from the differential amplifiers in the range increment detector, indicating the receipt of a range sample which differs by more than 0.36 nautical miles from the stored sample. Resetting the range increment circuits also produces an integrator reset output.

The function of the Maneuver Logic is to determine the type of avoidance maneuver to be made by the interrogator aircraft based on the specified maneuver rules. These rules are defined in paragraph 8.0 of the interrogator characteristics.⁶ The output of the maneuver logic elements consists of a pulse appearing on one of six wires indicating one of the six possible maneuvers. The logic equations, that must be satisfied to provide each of the six outputs are as follows:

$$\begin{aligned}
 P_{up} &= 2TV (\bar{Q}_i \bar{Q}_t U + A_i D_i) \\
 I_{up} &= 2T*V (\bar{Q}_i \bar{Q}_t U + A_i D_i) \\
 R_{down} &= 2TV (\bar{Q}_i \bar{Q}_t L + A_i C_i) \\
 I_{down} &= 2T*V (\bar{Q}_i \bar{Q}_t L + A_i C_i) \\
 R_{hold} &= 2T**V (B_i C_i L + B_i D_i U + B_i Q_t) \\
 I_{hold} &= 2T**V (B_i C_i U + B_i D_i L)
 \end{aligned}$$

⁶ Design Study Report - Experimental Evaluation of Compatible PWI/CAS Interrogator-Transponder Techniques, Volume II, furnished by Sperry Gyroscope Company to the Federal Aviation Agency under Contract No. FAA/ARDS-444.

The symbol definitions for the preceding equations are as follows:

V = normal velocity criterion satisfied

T = $27.6 \text{ sec} \leq \tau \leq 40 \text{ sec}$, where τ = time to closest approach

T* = $\tau < 26.7 \text{ sec}$

T** = $\tau < 40 \text{ sec}$ R < 1 nautical mile

Q = absolute altitude rate is greater than 1350 ft/min

C = climbing

D = descending

U = interrogator is in transponder's upper altitude guard band

L = interrogator is in transponder's lower altitude guard band

R = maneuver

I = immediate maneuver

A = absolute value of altitude rate greater than 1350 ft/min., less than 3000 ft/min

B = absolute value of altitude rate greater than 3000 ft/min

Z = read in data to scan memory (computation completed).

NOTE: The suffix t or i affixed to the preceding literal terms indicates that the logical term applies to the transponder or to the interrogator respectively.

The logic operations performed in the Maneuver Logic are self-explanatory upon study of figure 5-5. The only part of the Maneuver Logic section requiring any amplification is the averaging circuit. The function of this circuit is to satisfy the requirement that the indicated direction of an up or down maneuver be based on an instantaneous average of the decoded relative altitude data. A second function is to inhibit a transponder climbing or descending conclusion unless two or more samples of this code have been received. The method used is to provide an up-down counter (add-subtract) to derive the instantaneous average and a counter of two (with suitable gating logic) to provide recognition of the presence of two or more transponder climbing or descending codes.

The scan memory provides the following functions:

- inhibits warnings unless collision decisions are made on two successive scans
- serves as a "data hold" to provide a continuous rather than intermittent display.

Each command channel (up, down, or hold) of the memory is identical and consists of a shift register which is advanced once each scan by shift pulses from the antenna switch. A command is indicated if both of the last two stages are in the set condition. If any input on a scan has an immediate label, a monostable multivibrator with a period of 1.5 seconds is also triggered. Its output is gated out as an "immediate" indication concurrently with the maneuver command. Because the multivibrator period is shorter than the scan cycle, an intermittent "immediate" indication is produced.

6. Transponder Computer

The transponder computer converts heading, altitude, and altitude rate data to a form suitable for coding and decoding and contains the logic necessary to provide the intelligence for the limited transponder maneuver display. A signal schematic is shown in figure 5-6.

The heading servo resolves the transponding aircraft's airspeed into north and east components and contains a quadrant switch to produce binary data on their polarities. A lag network has been included in the error sensor to make the servo an effective low-pass filter, resulting in a shaft position proportional to the average heading. The control transformer output voltage, however, will contain the high-frequency variation. This signal is used in the relative bearing servo (in the interrogator collision computer) to cancel the high frequency component of train angle. The limiting diode in the generator feedback circuit is used to allow faster slewing than would be otherwise possible for large errors in heading. This feature permits quicker recovery from the effects of turns.

The Transponder Maneuver Logic contains the logic elements necessary to determine the type of maneuver (hold or immediate hold), the data holds necessary to provide continuous displays, and provisions to establish precedence for "immediate" commands. The operation of the basic logic elements is self-explanatory. Data holds consist of flip-flops which are set by the commands and reset by relaxation oscillators having periods in excess of the antenna scan period. Each received command recycles the relaxation oscillators, thus inhibiting reset signals as long as maneuver commands continue to be received. A set condition of the "immediate" data hold inhibits further set inputs to the normal data hold, achieving the precedence function.

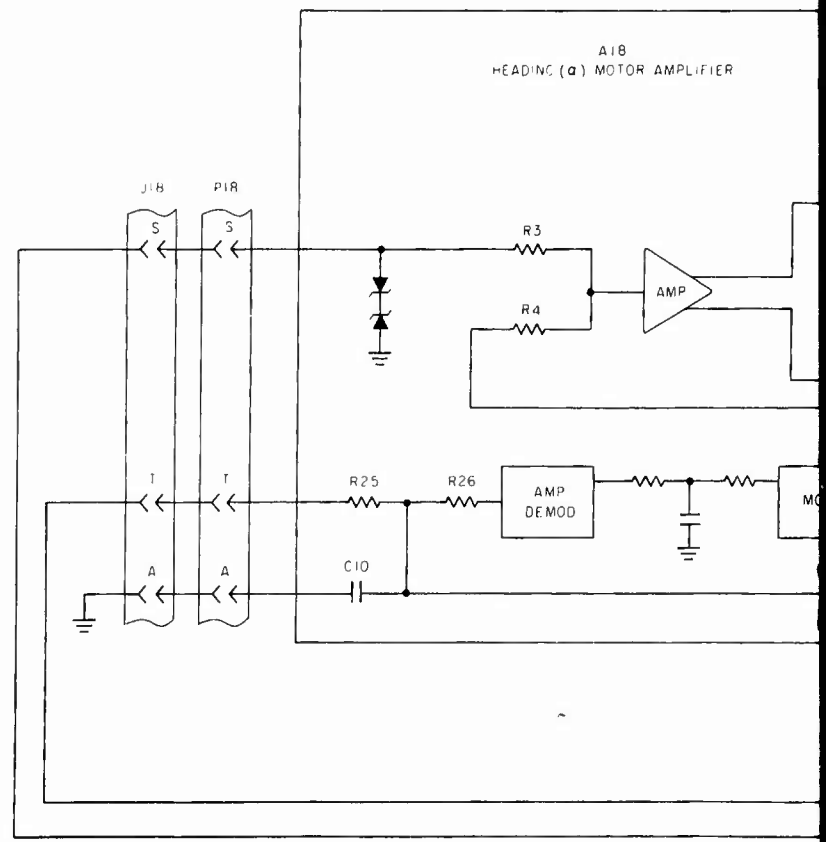
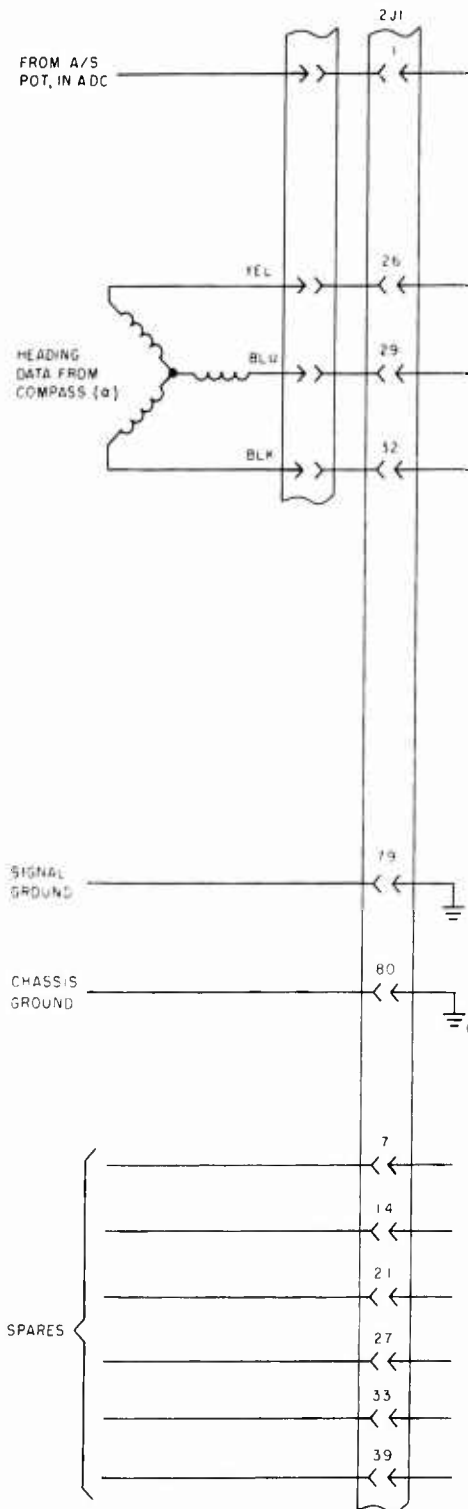
B. SUGGESTED MODIFICATIONS

In the course of the evaluation program, circuit modifications suggested themselves. These modifications have the potential of improving system performance or of achieving satisfactory performance more economically. Because of the experimental nature of the program, these changes were not implemented or even explored in detail. However, the nature of these suggested changes is given for completeness.

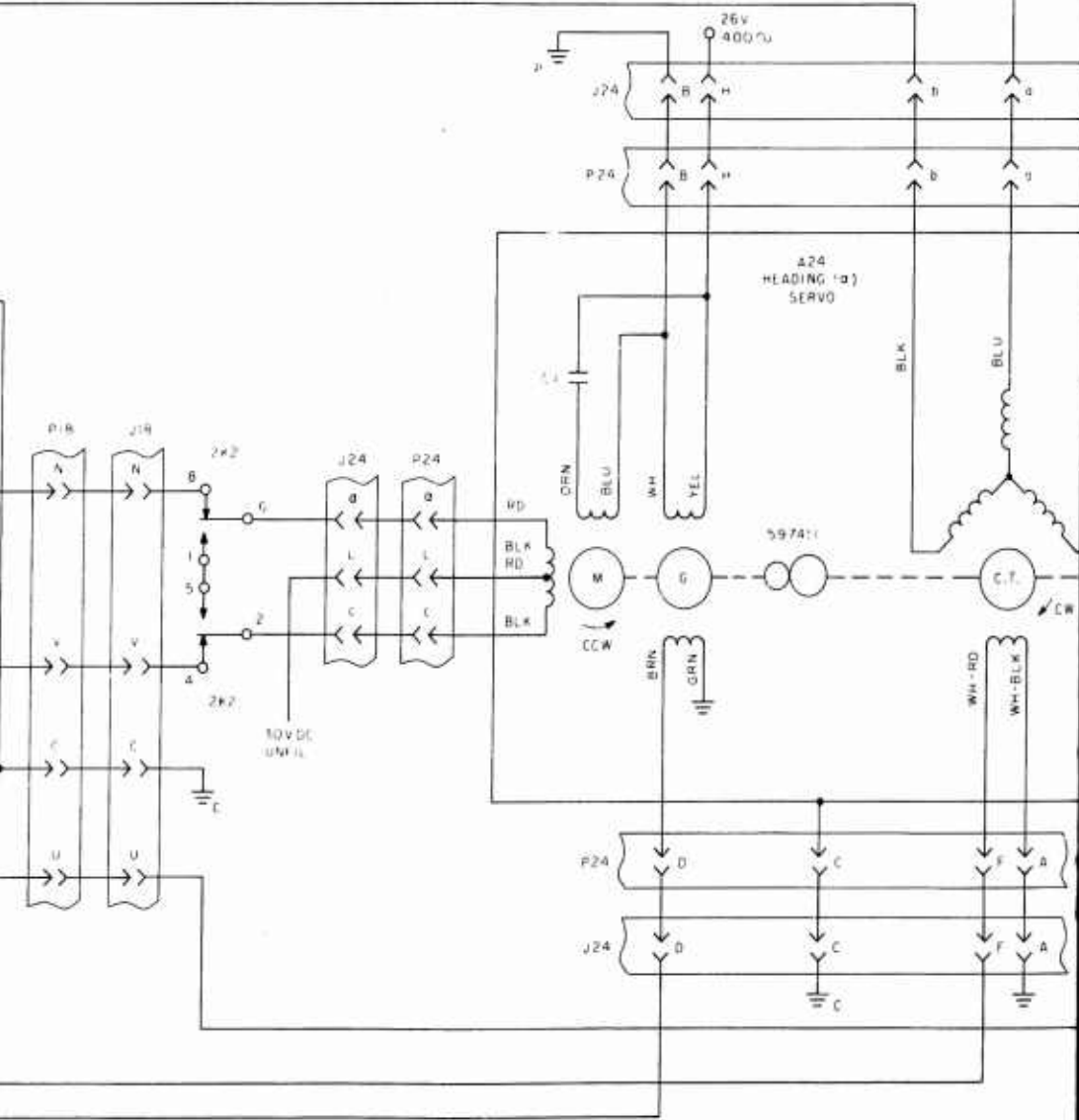
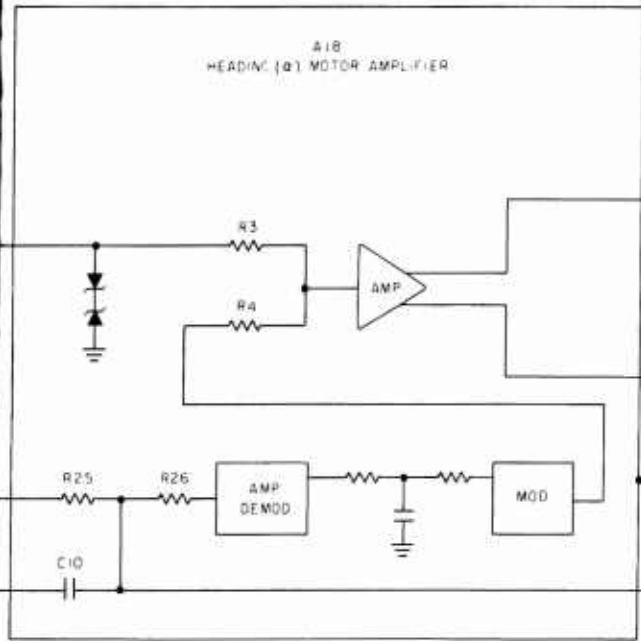
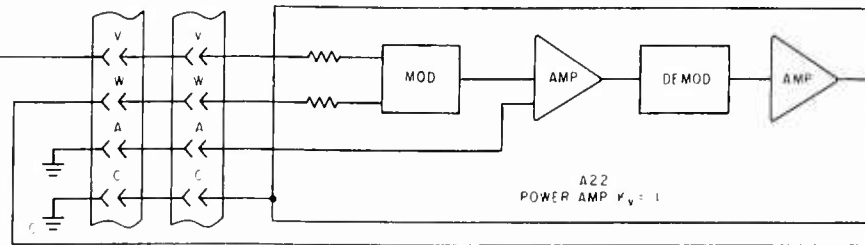
In general, an effort devoted to defining the simplest circuit to accomplish the present functions would be beneficial. For instance, the number of elements employed in logic circuits could generally be reduced, by rearrangement. A net gain might also be realized by sharing elements, such as delay lines, between functions. No effort has been devoted to such simplification beyond that intuitively done in normal engineering practices.

The sonic delay lines and associated circuits employed for encoding and, in some cases, for decoding are marginal in performance for the application. The primary deficiencies are limited bandwidth, high reflection levels, and excessive pulse generator recovery times. Improved reliability could be achieved by substituting electromagnetic delay lines. This substitution would also facilitate the sharing of elements.

The linearity of the linear sweep circuits and associated memory circuits, where employed, could be improved. The most obvious approach is to employ an operational amplifier as an integrator, as in the interrogator computer. Such an integrator could serve as both the sweep generator and memory, where required. An alternate approach would be to employ digital techniques, by counting clock pulses and converting the count to an analog output. The counter could also double as a memory where required.



1



2

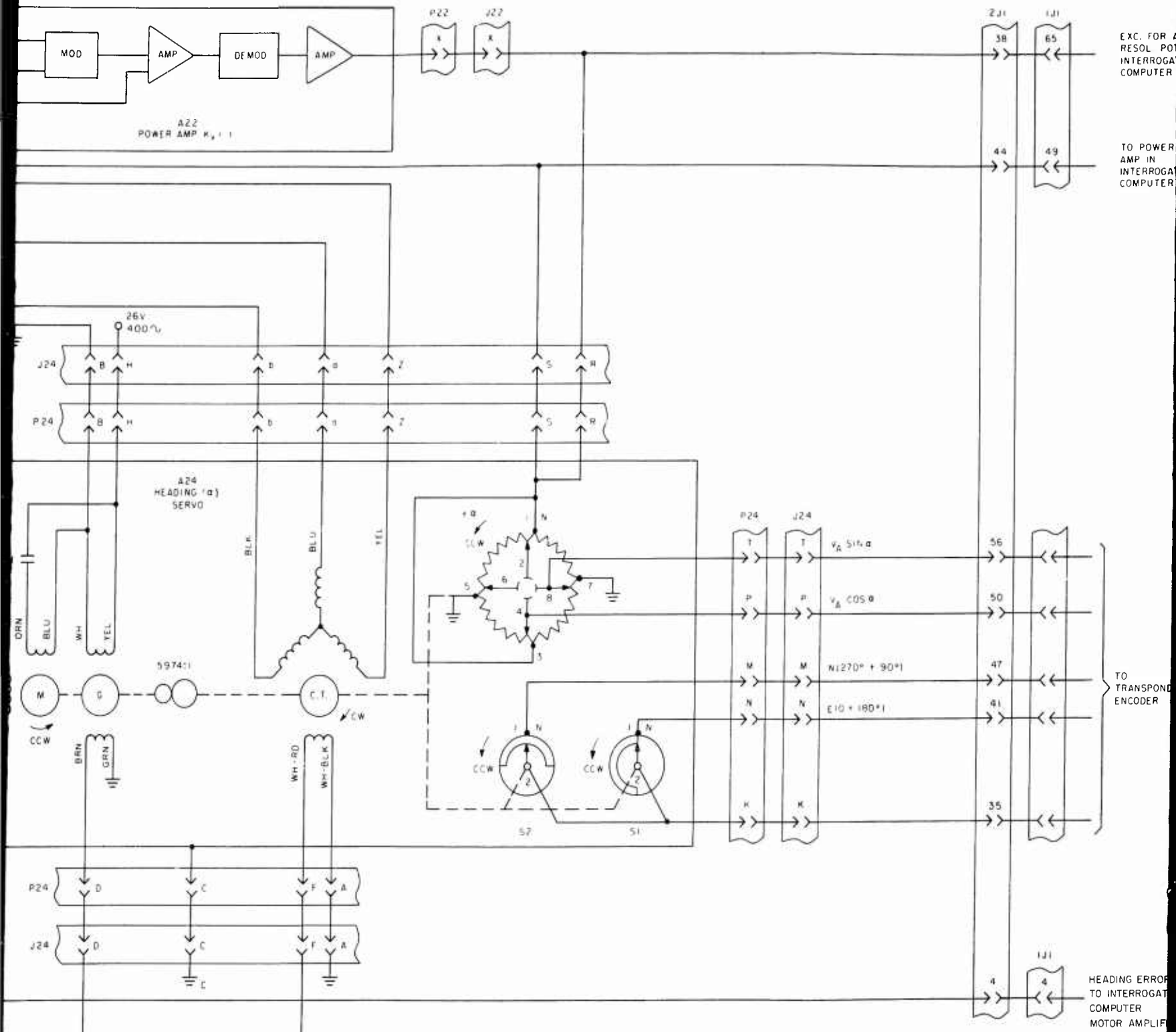


FIGURE 5-6. TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 1 OF 2)

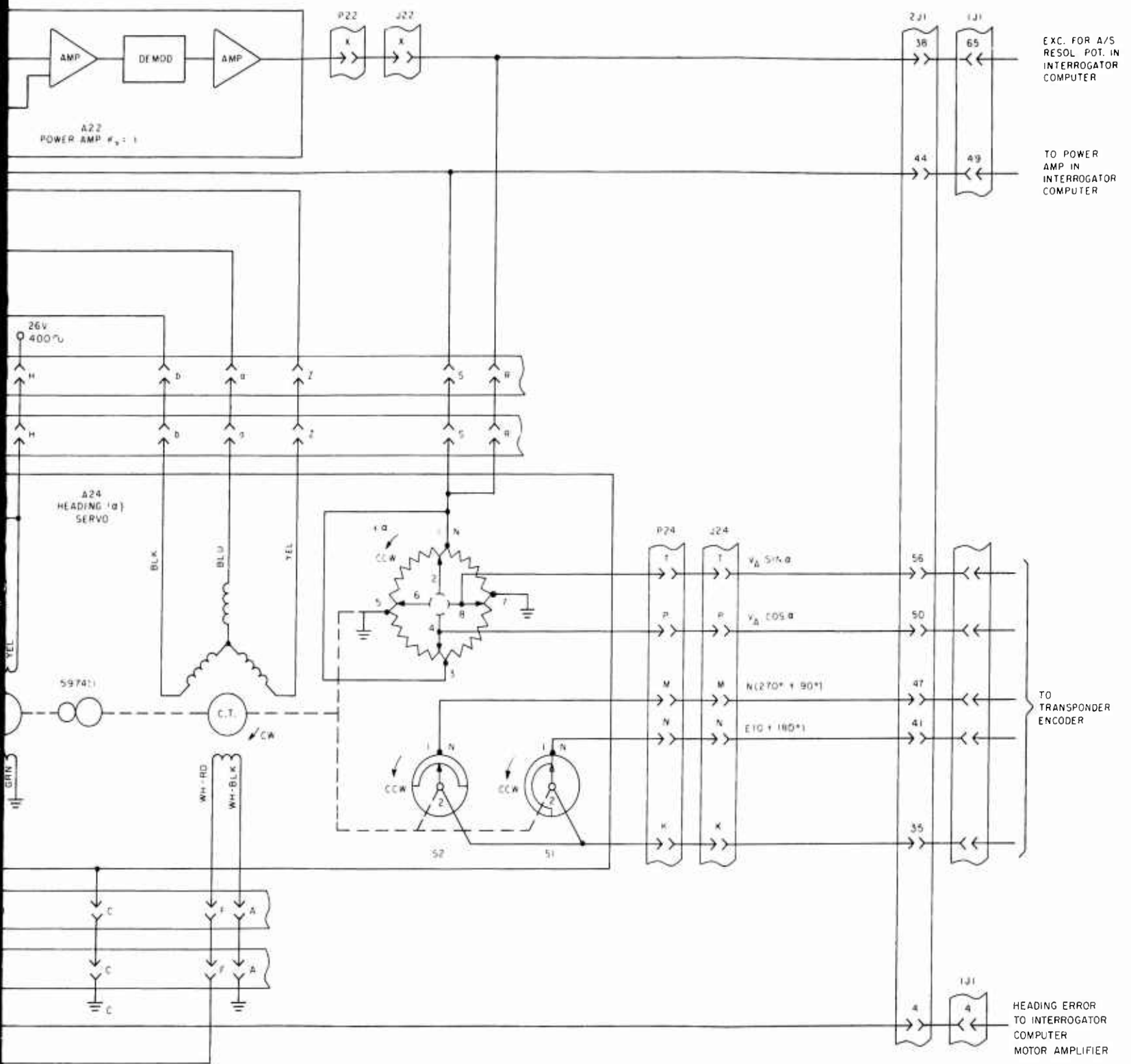
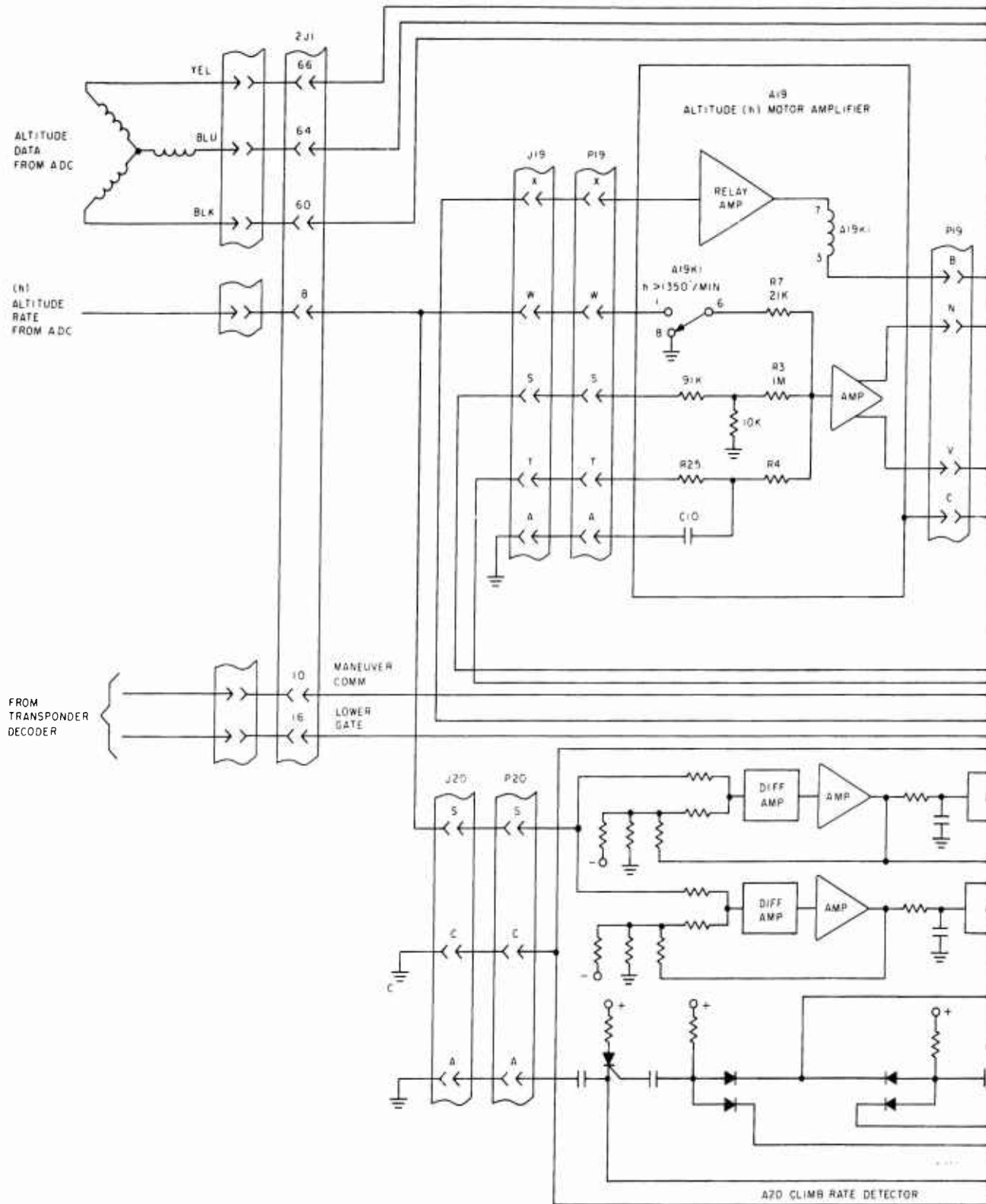
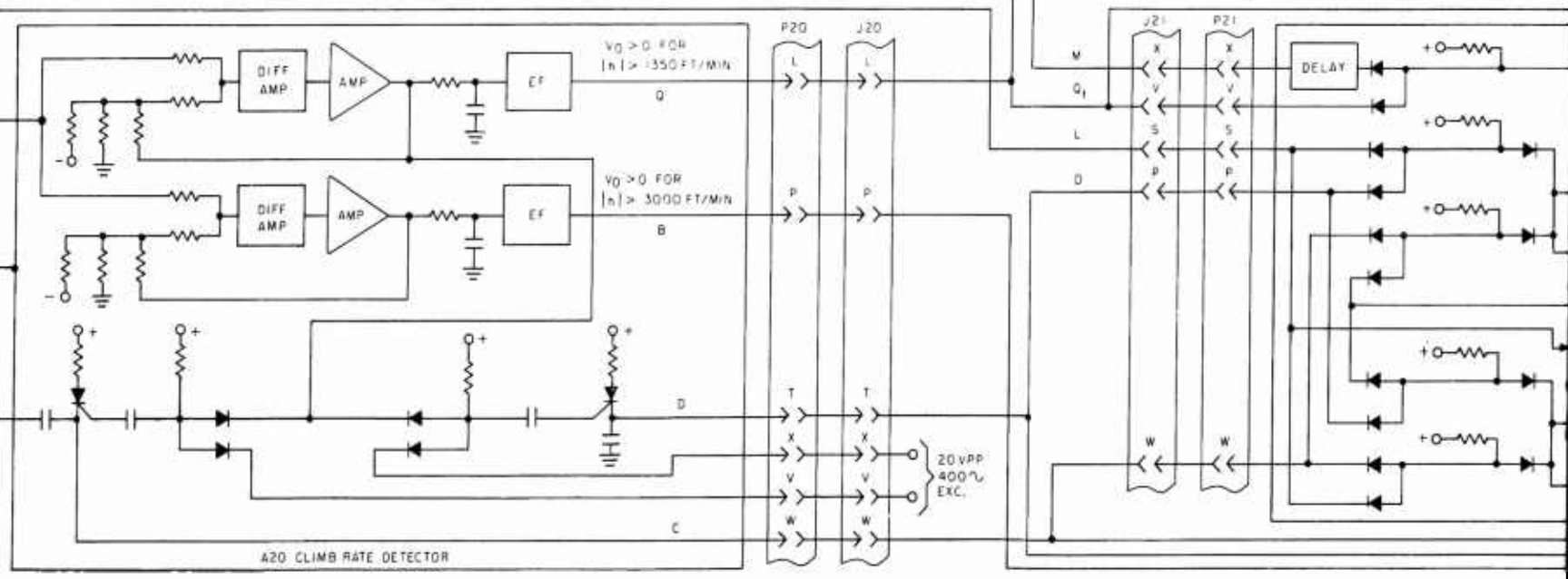
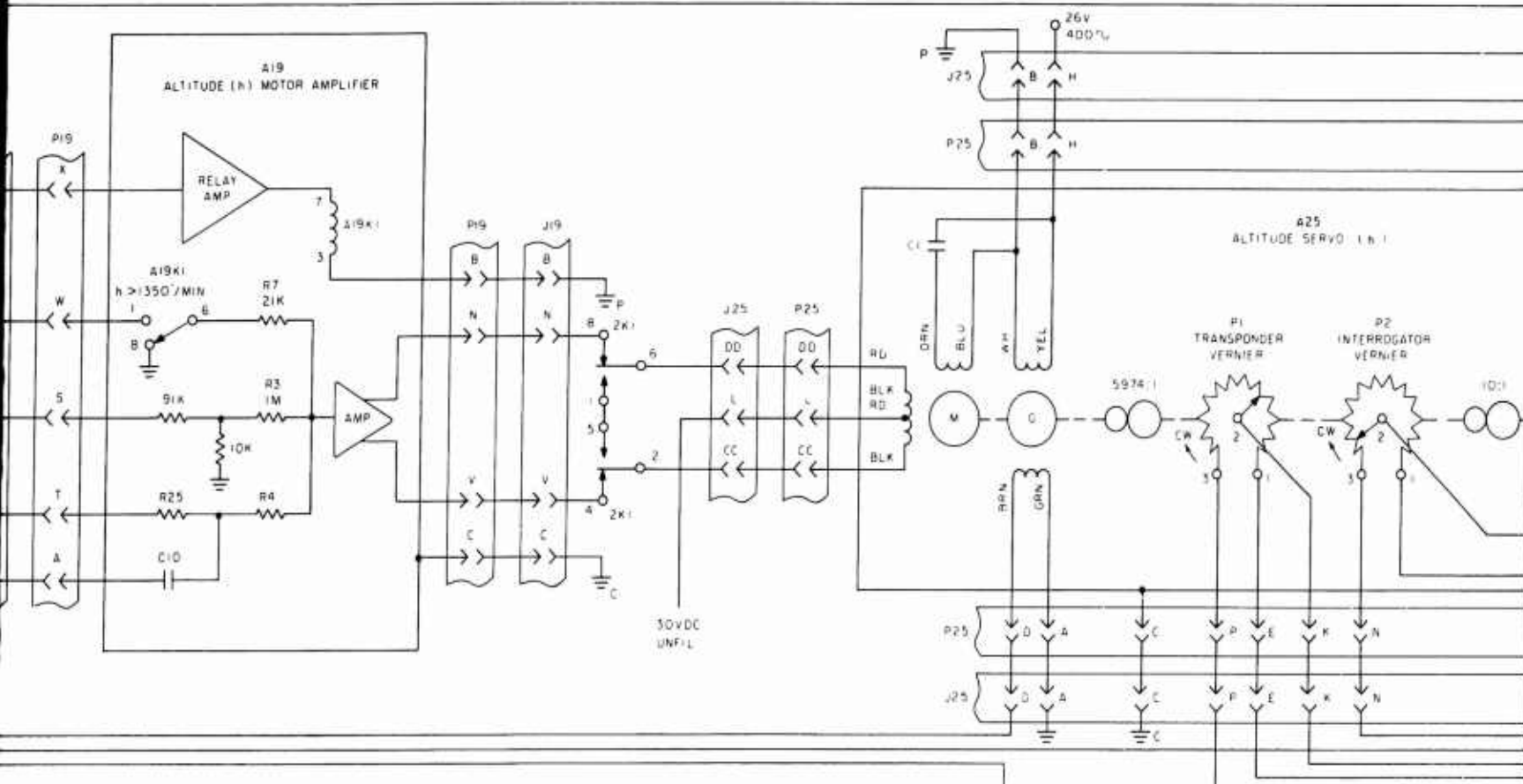
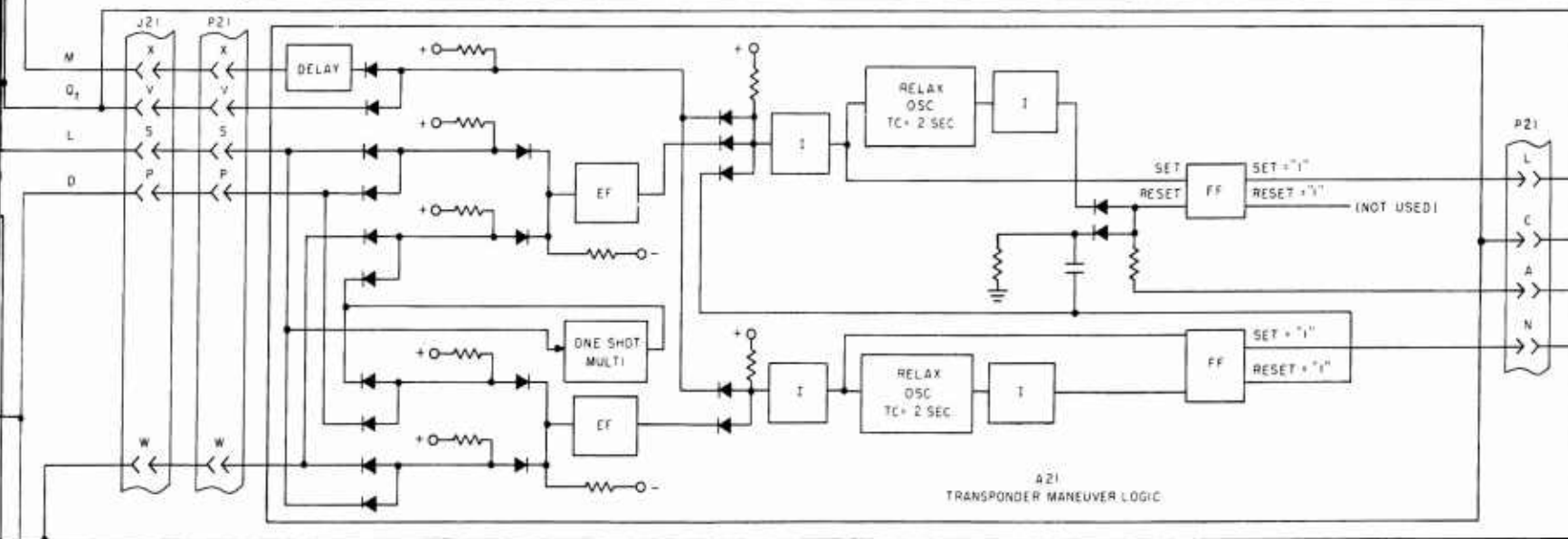
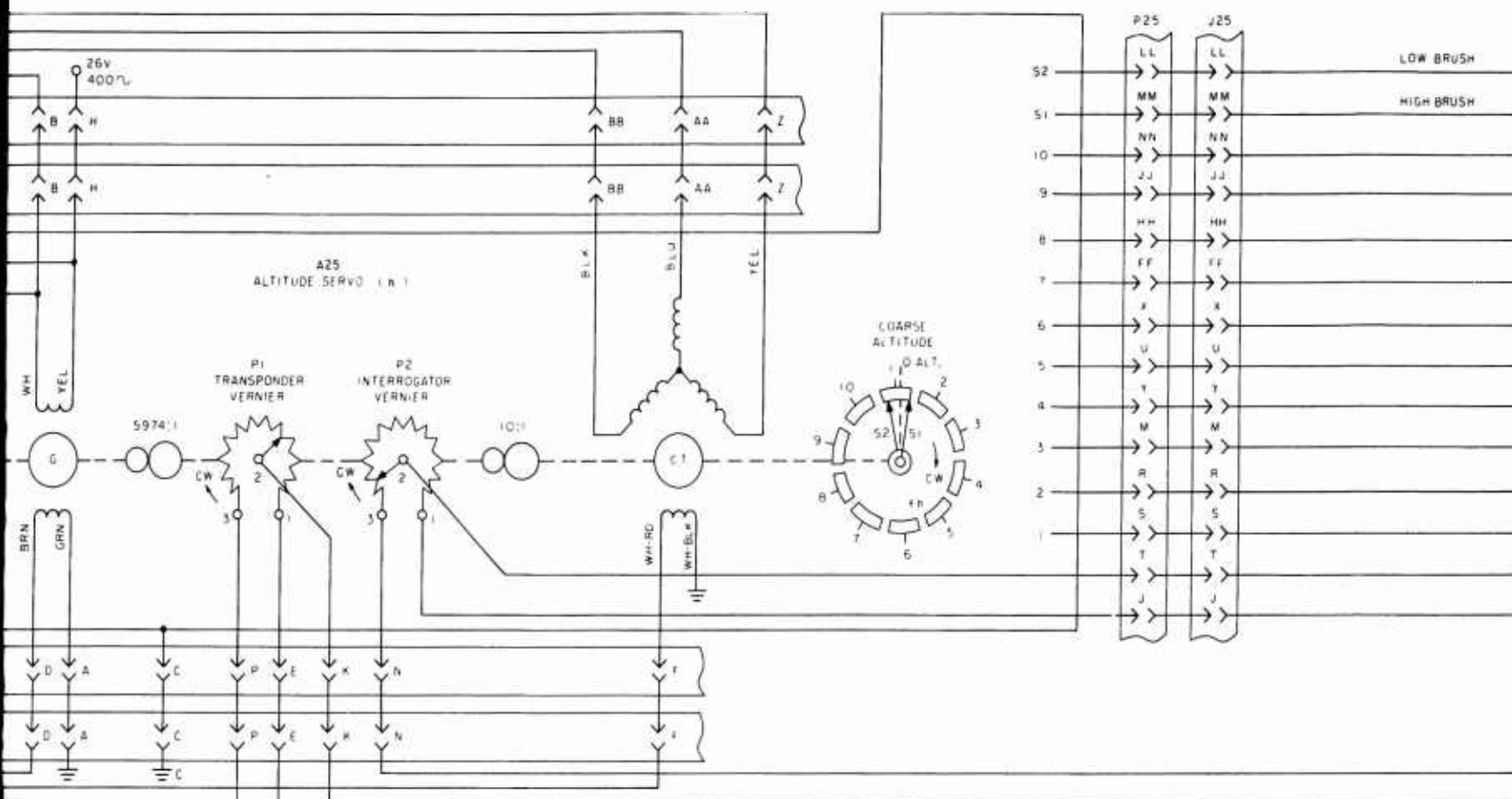


FIGURE 5-6.
 TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 1 OF 2)



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3

TRANS

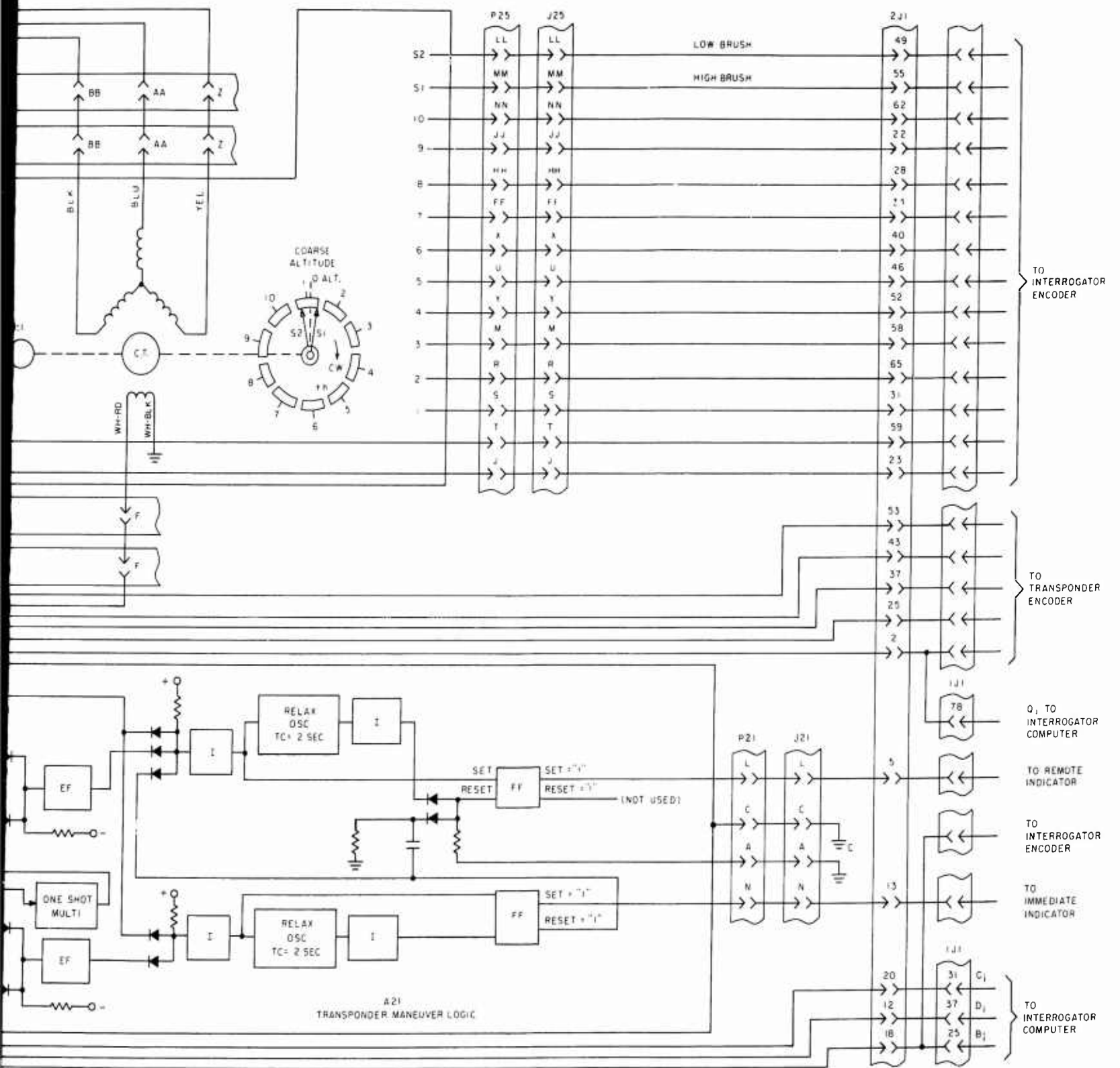
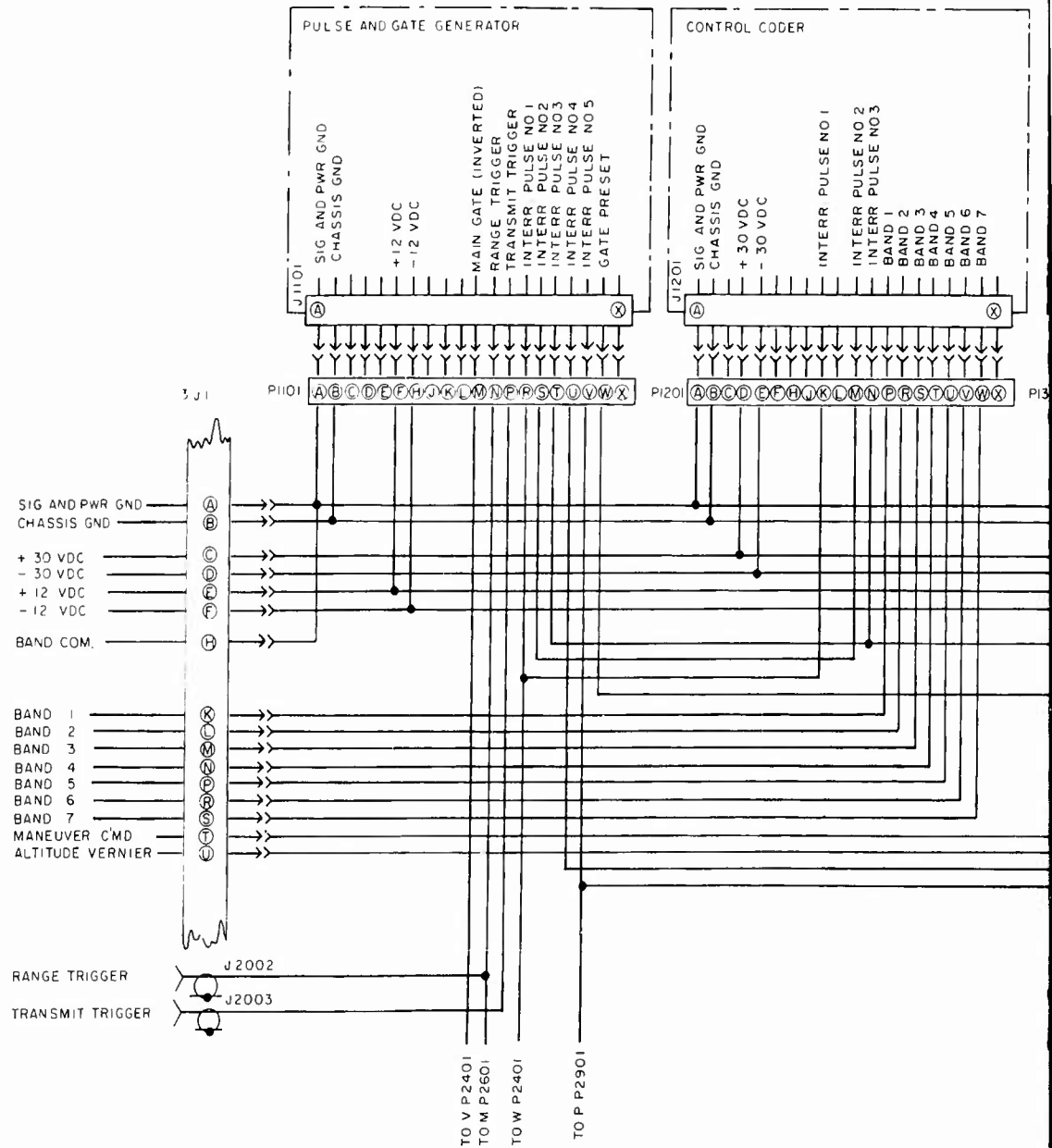


FIGURE 5-6.
TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 2 OF 2)



1

INTERRO
(UNIT S

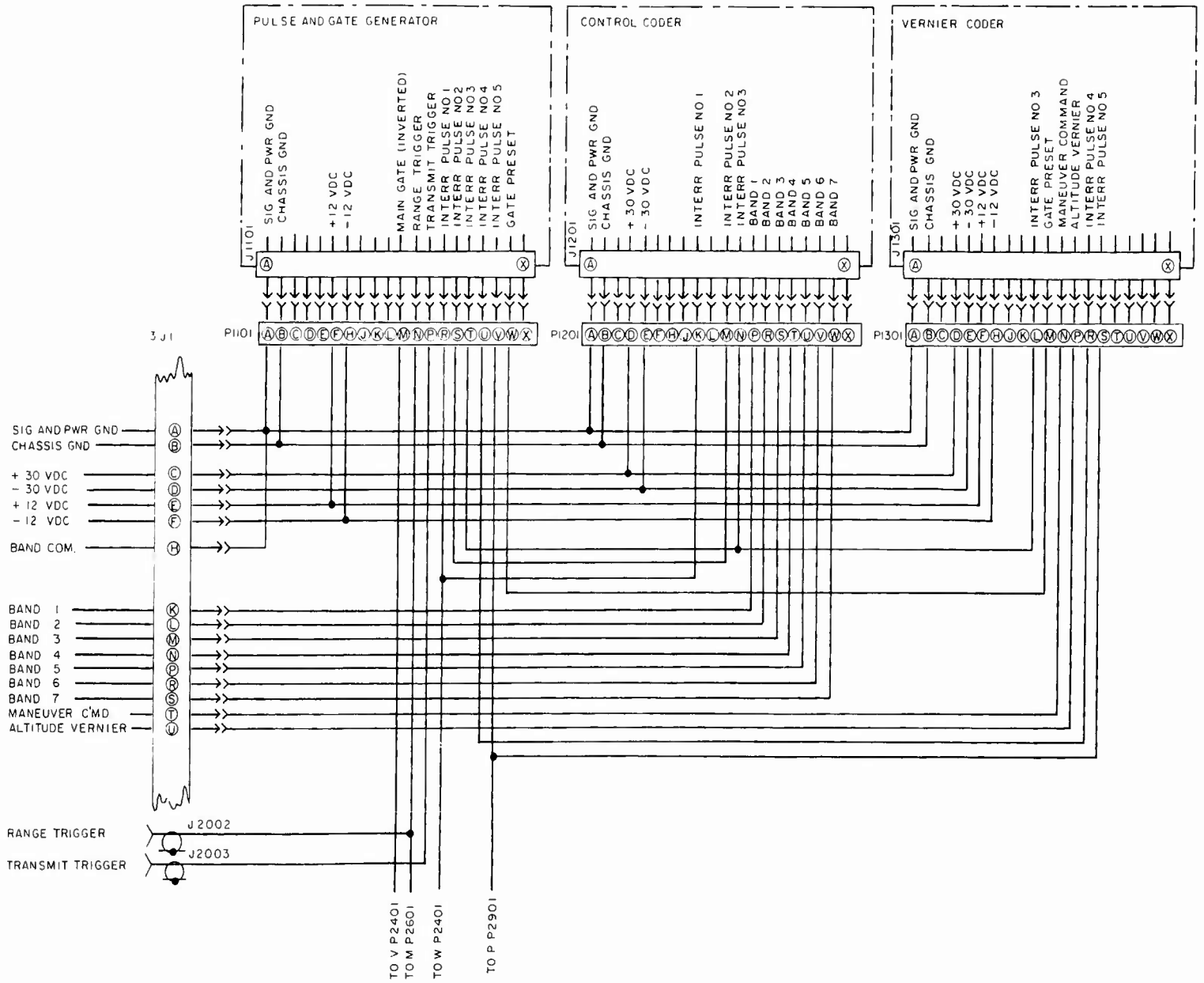


FIGURE 5-7.

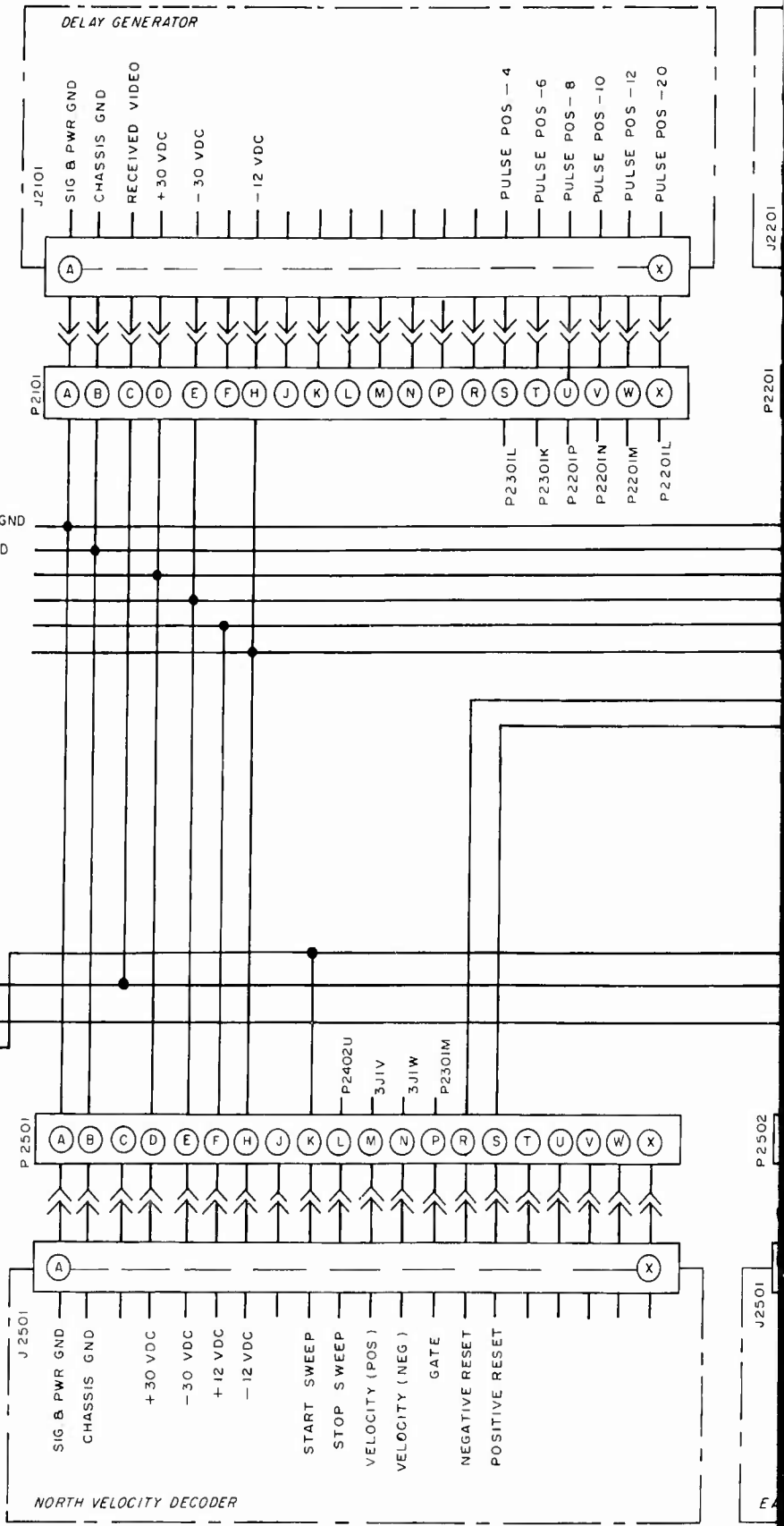
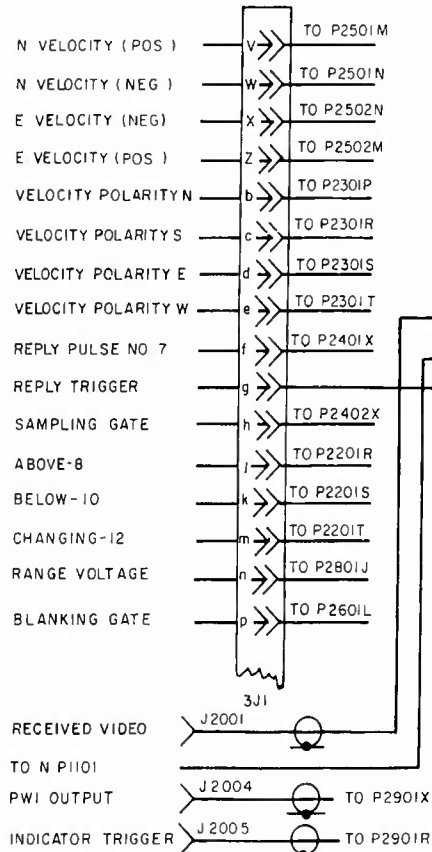
INTERROGATOR ENCODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 1000)

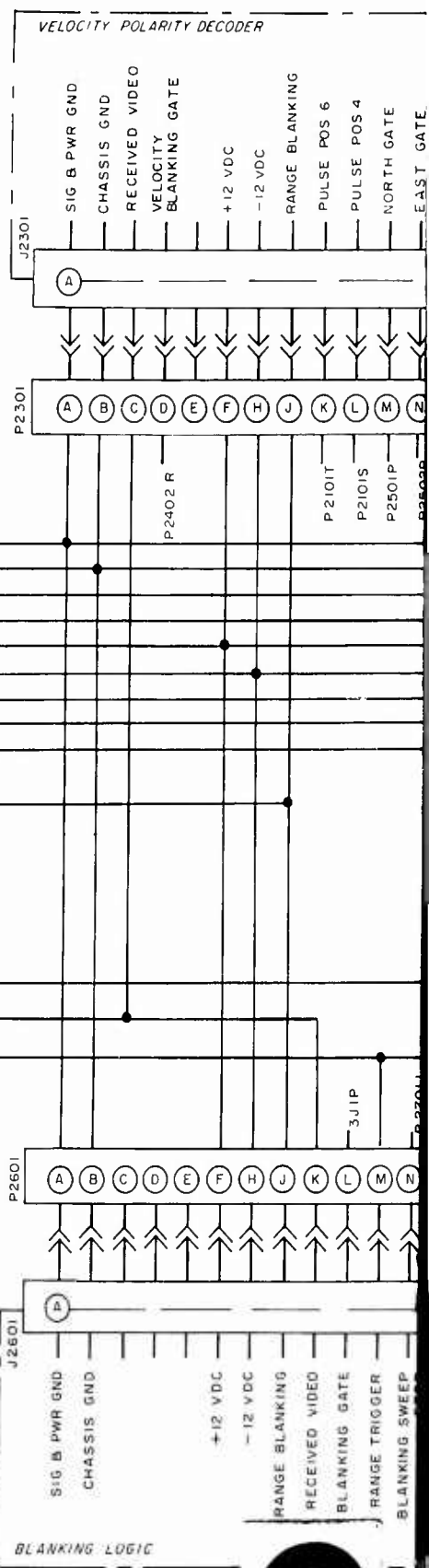
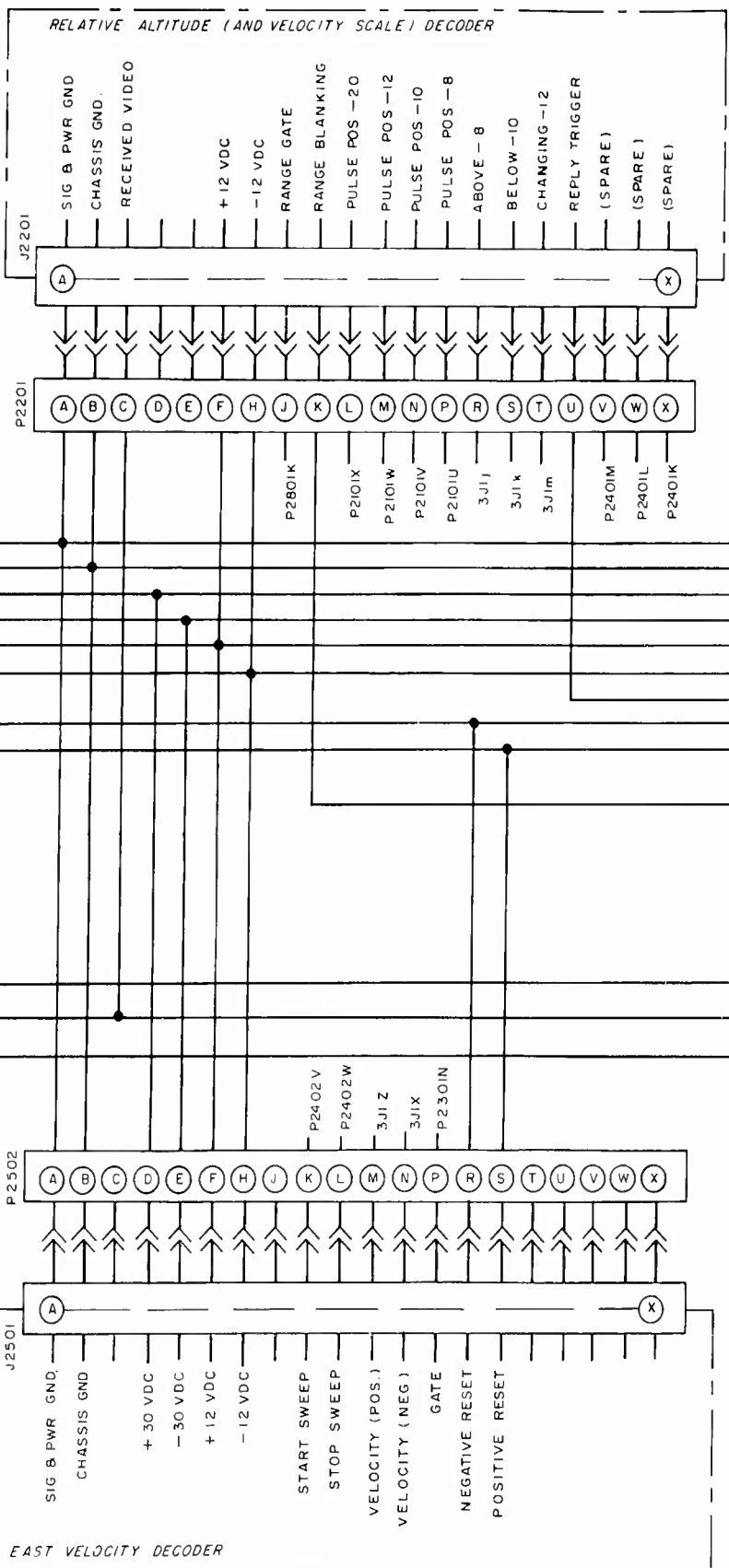
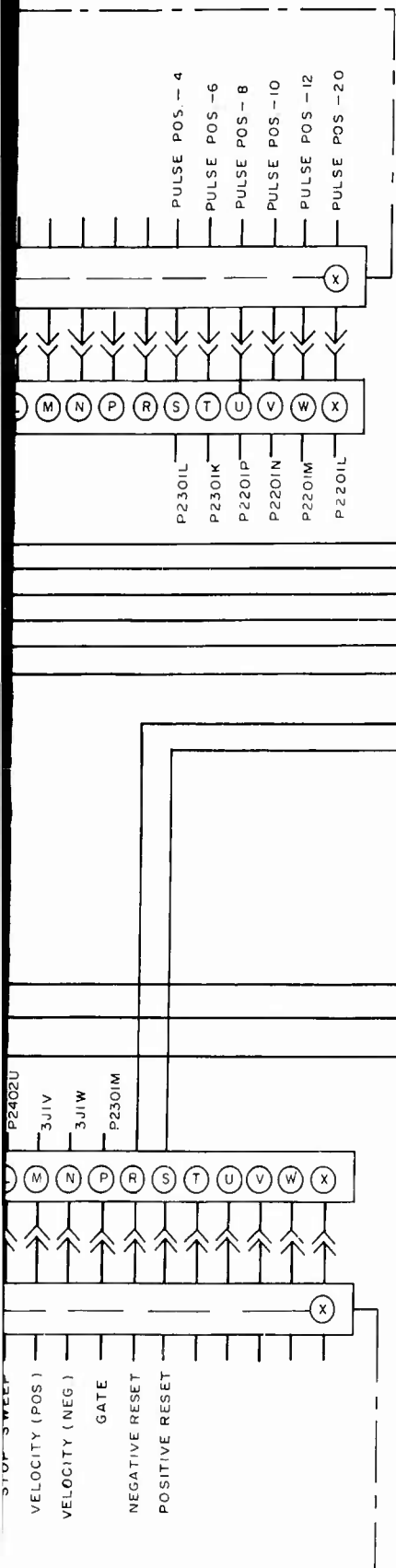
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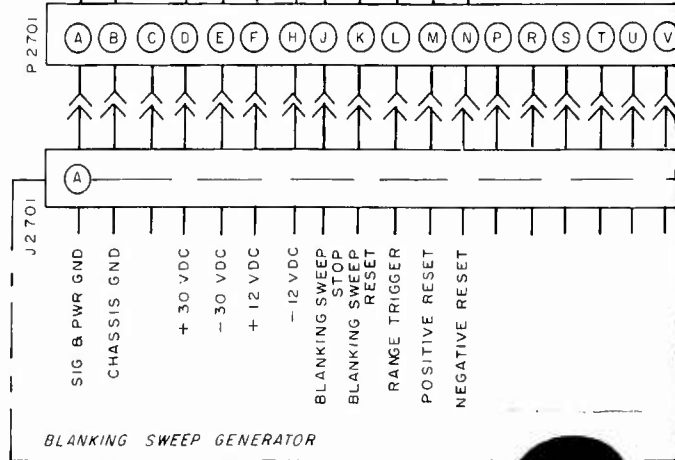
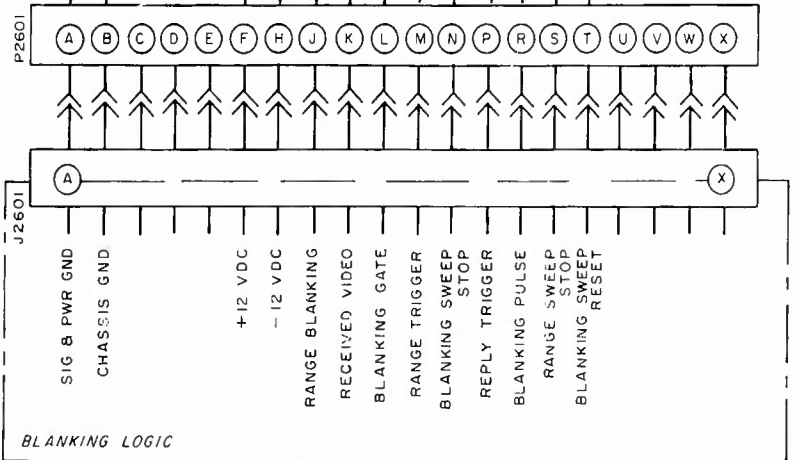
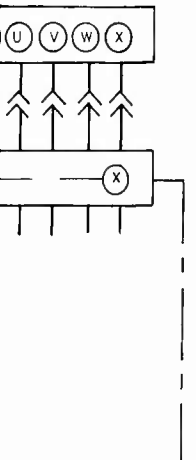
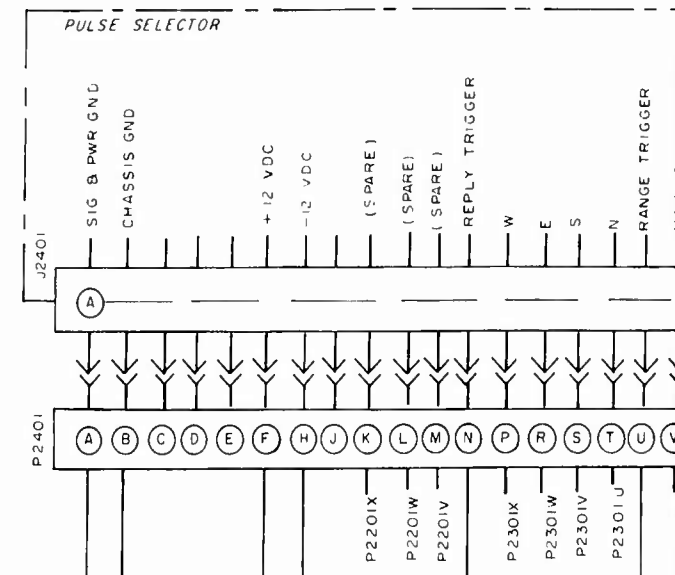
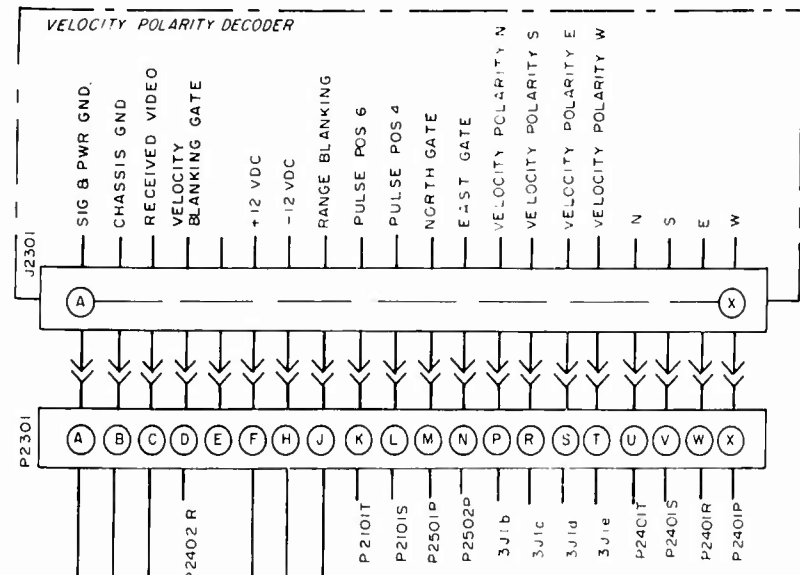
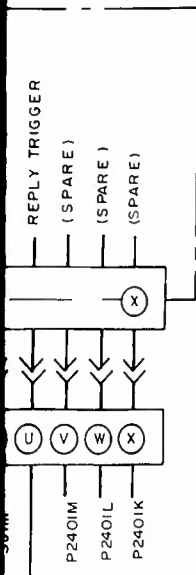
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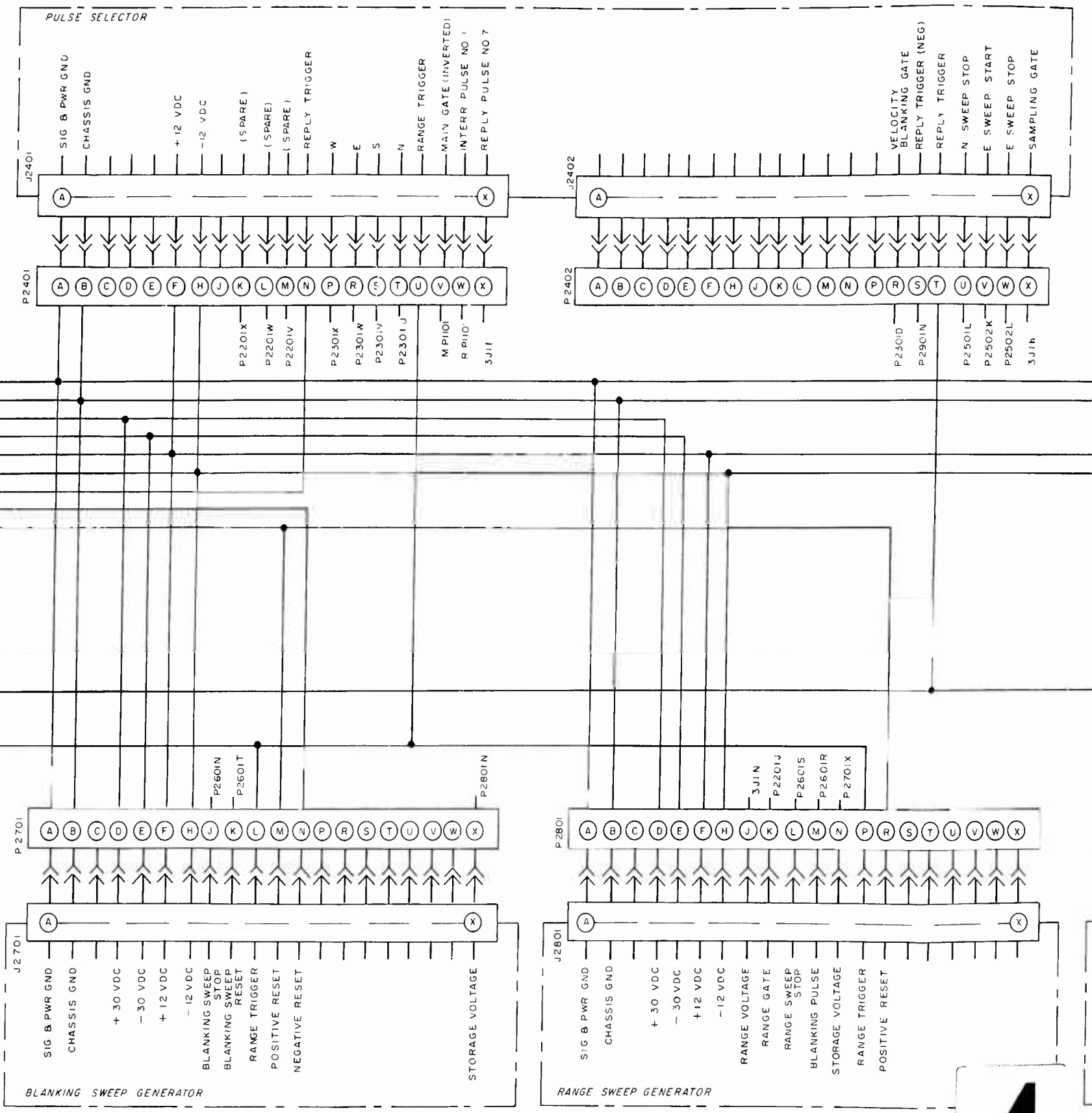
THESE WIRES ARE TIED TO THEIR PROPER BUSSES INSIDE THE CHASSIS THE 3JI TERMINATIONS ARE SHOWN ON EN - DECODER DIAGRAM

- PWR & SIG GND
- CHASSIS GND
- + 30 VDC
- 30 VDC
- + 12 VDC
- 12 VDC









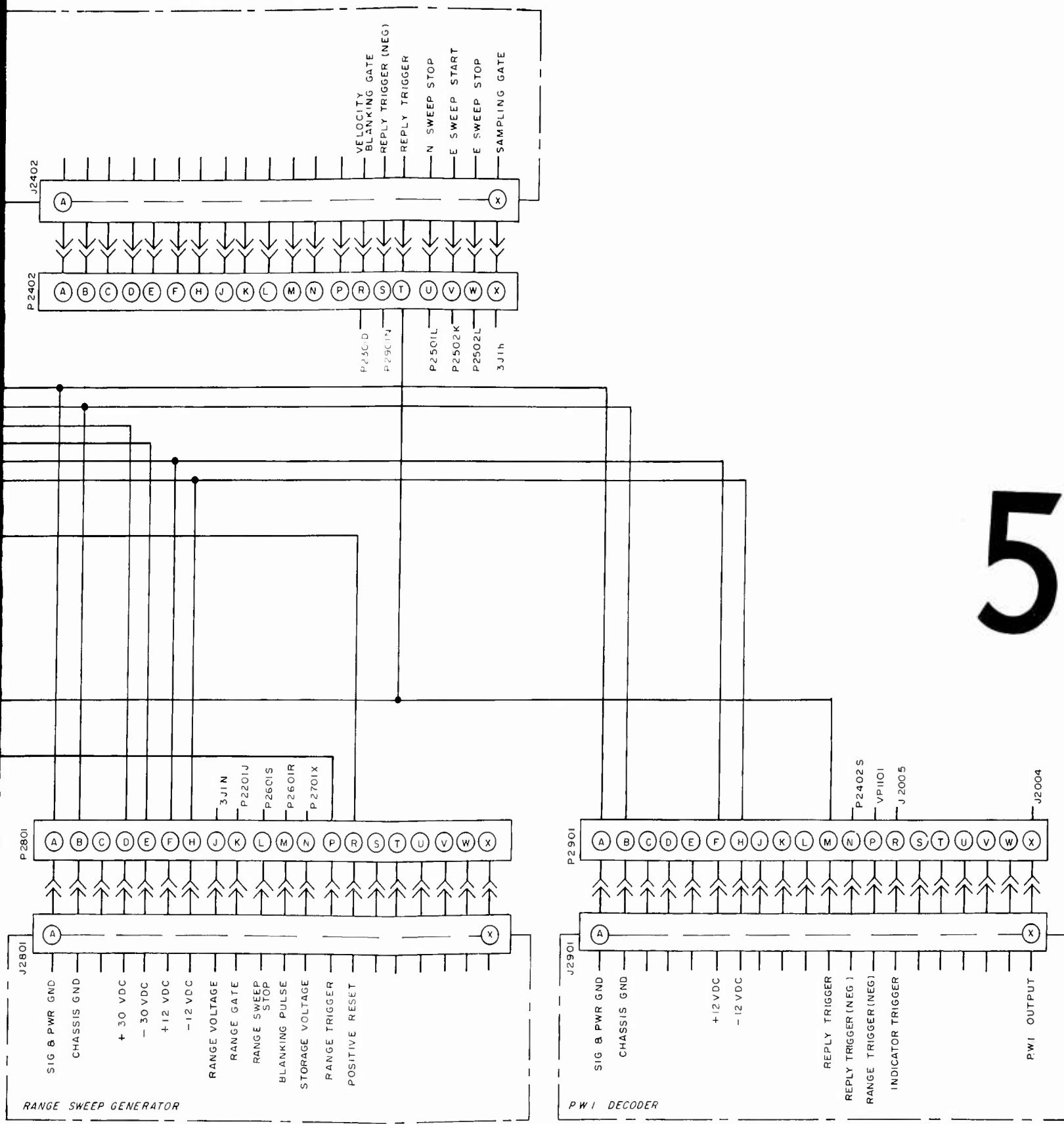
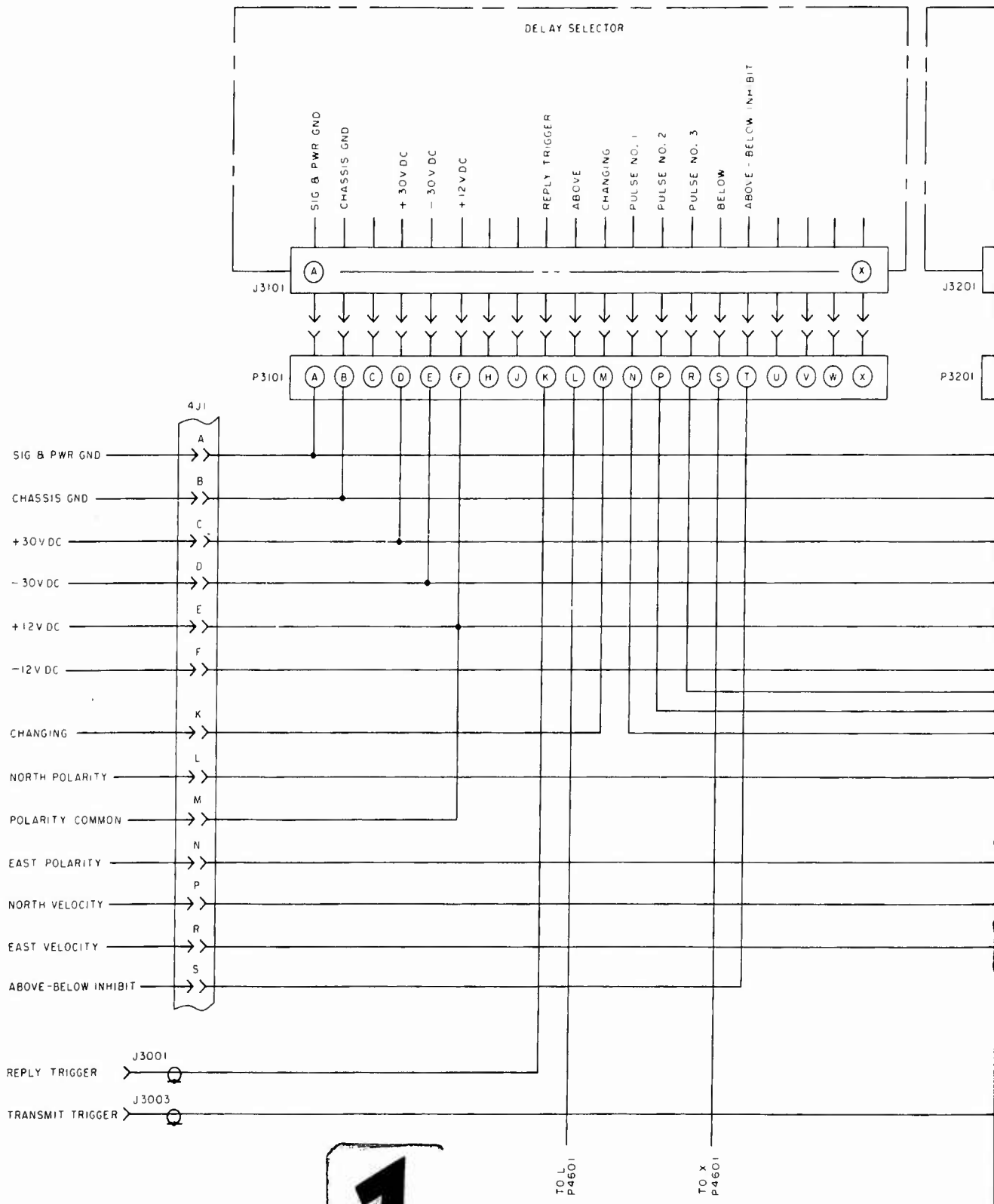


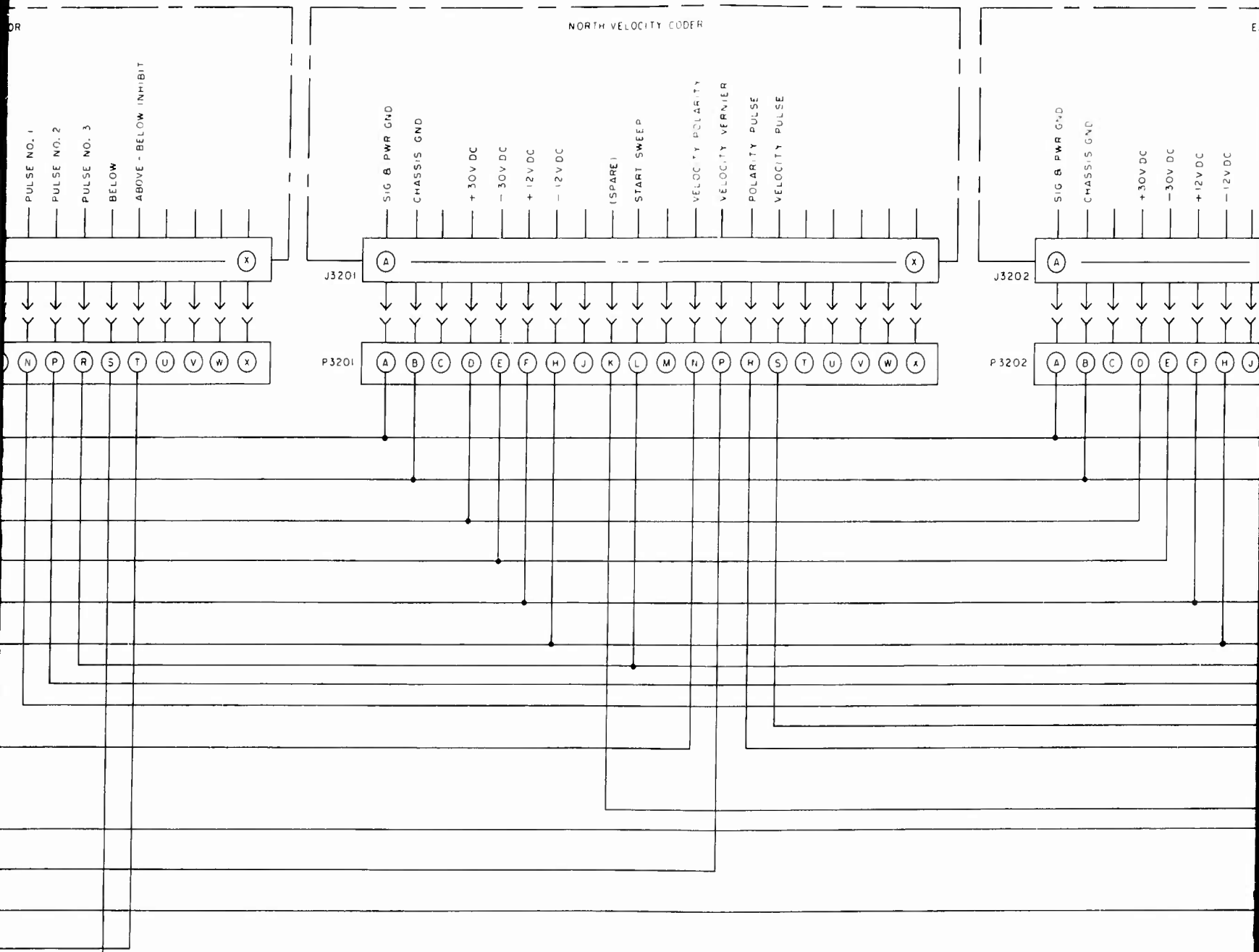
FIGURE 5-8
INTERROGATOR DECODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 2000)



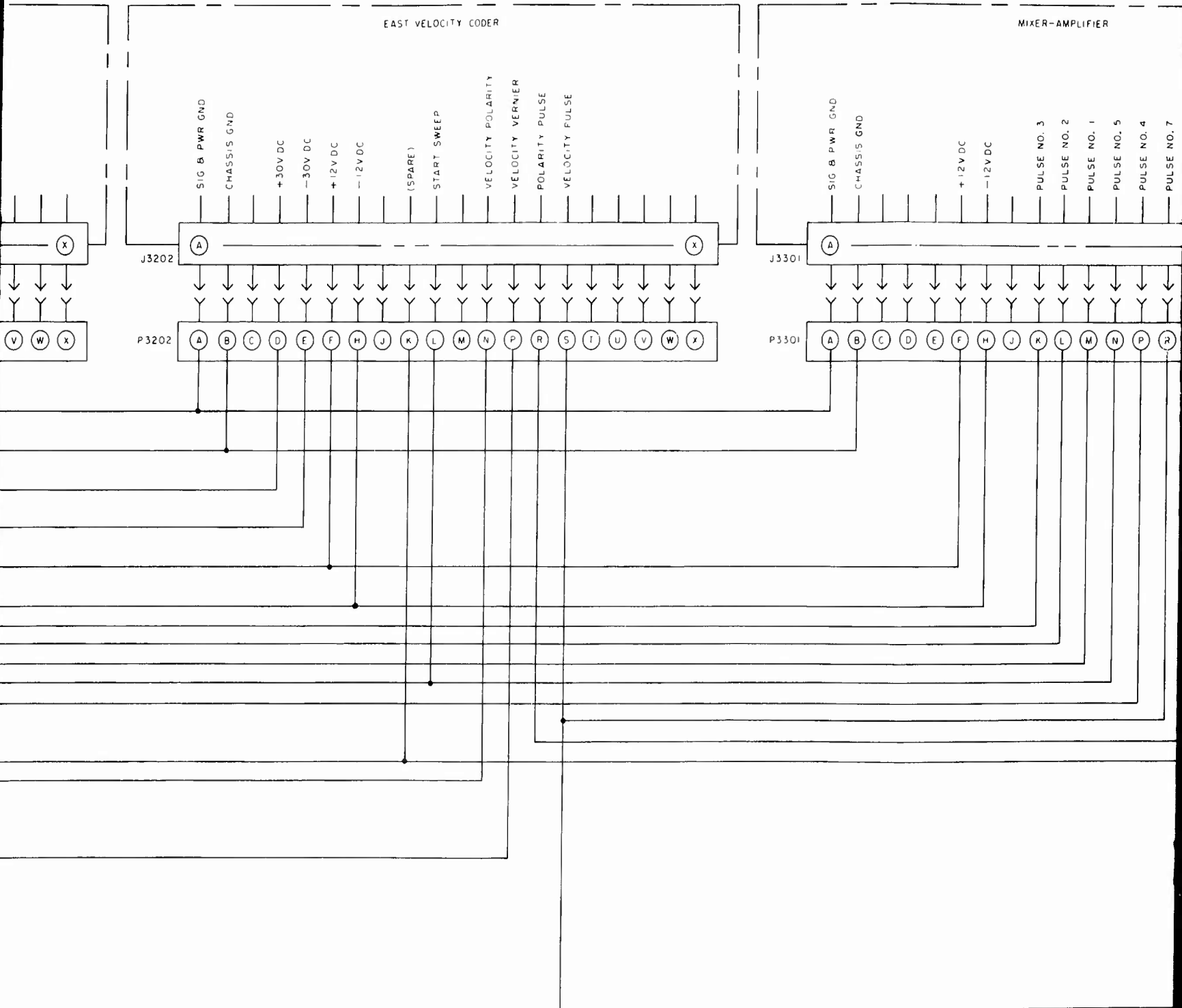
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3

TRANSPONDER ENCODER
(UNIT SERIAL)

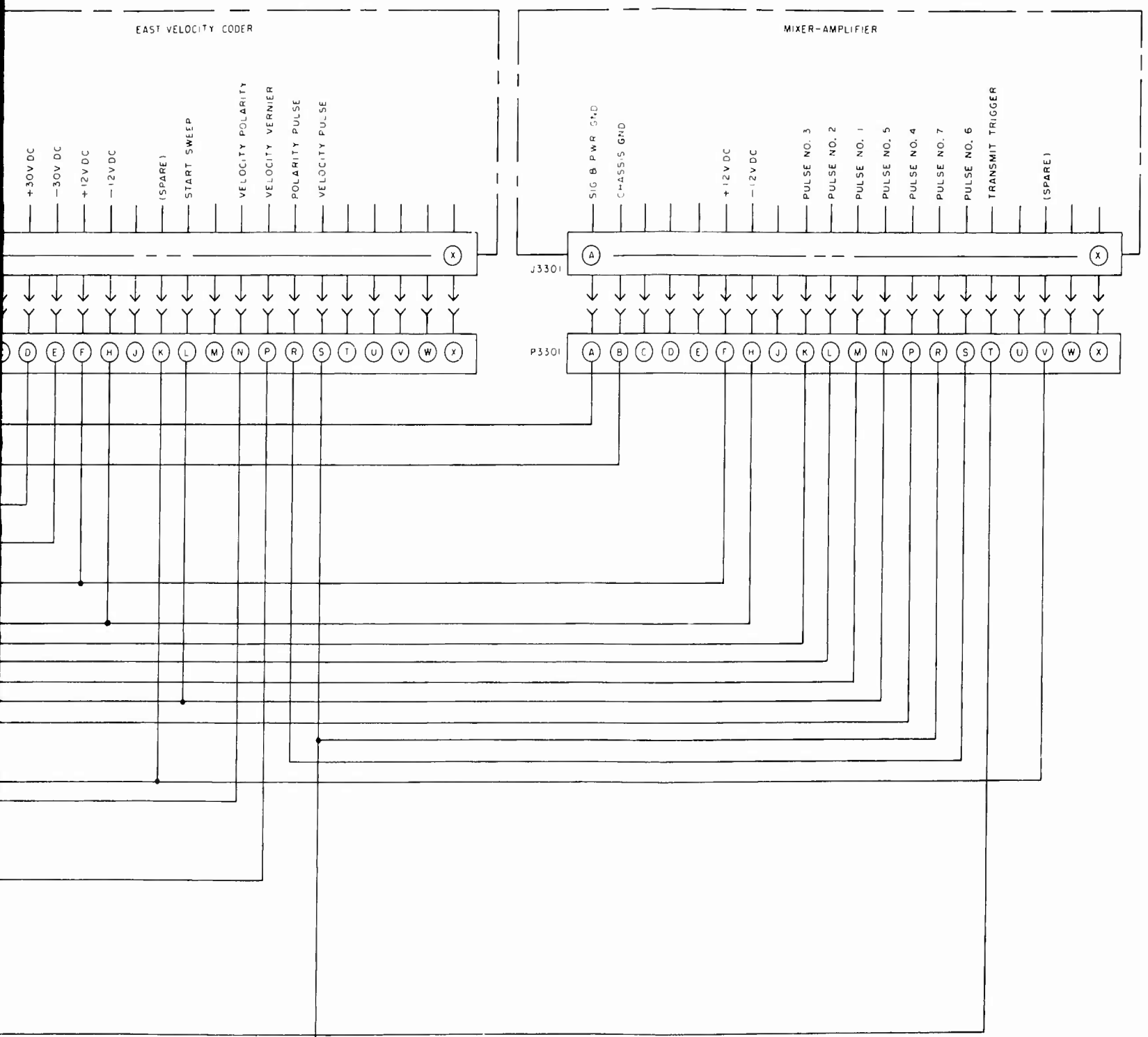
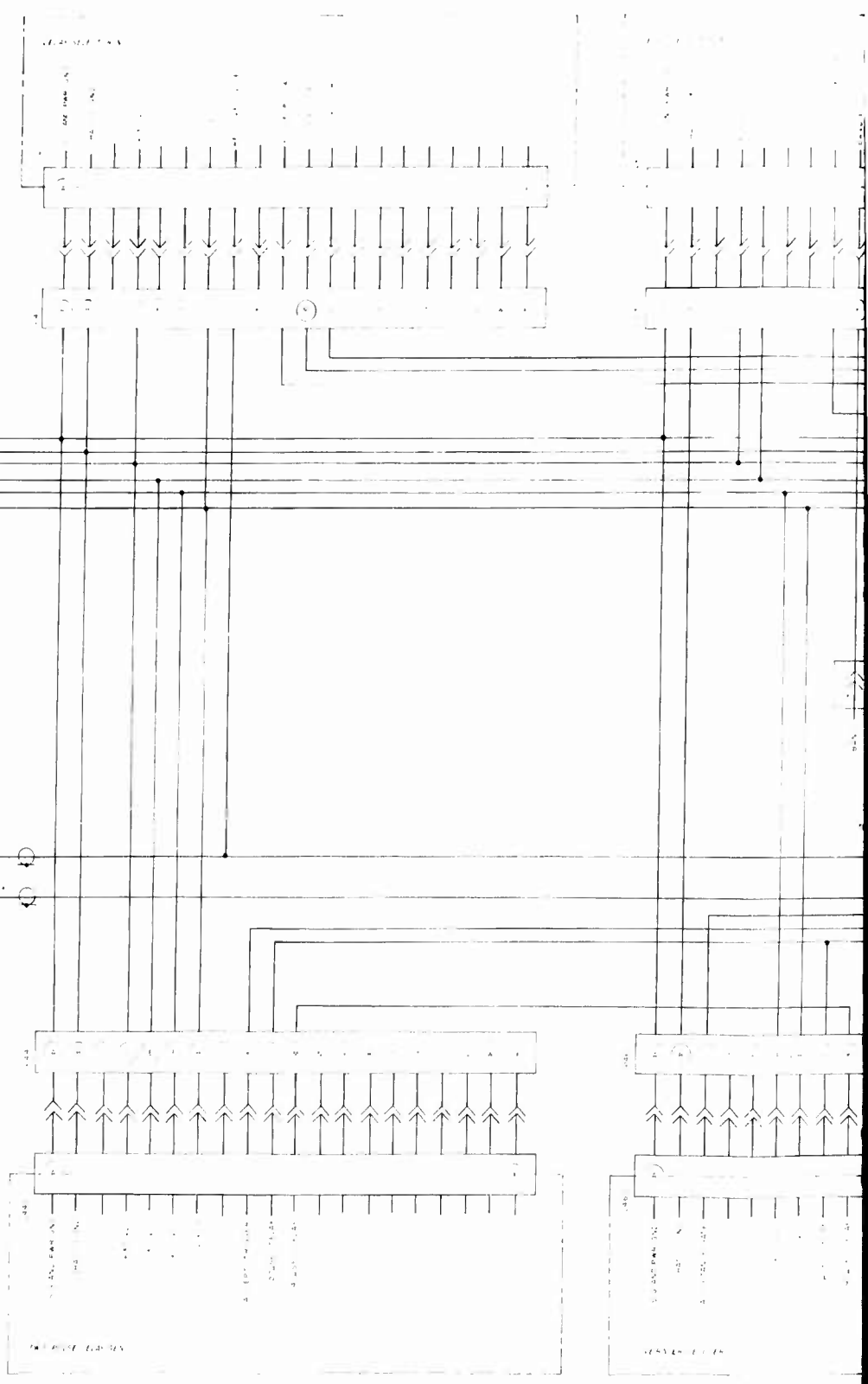


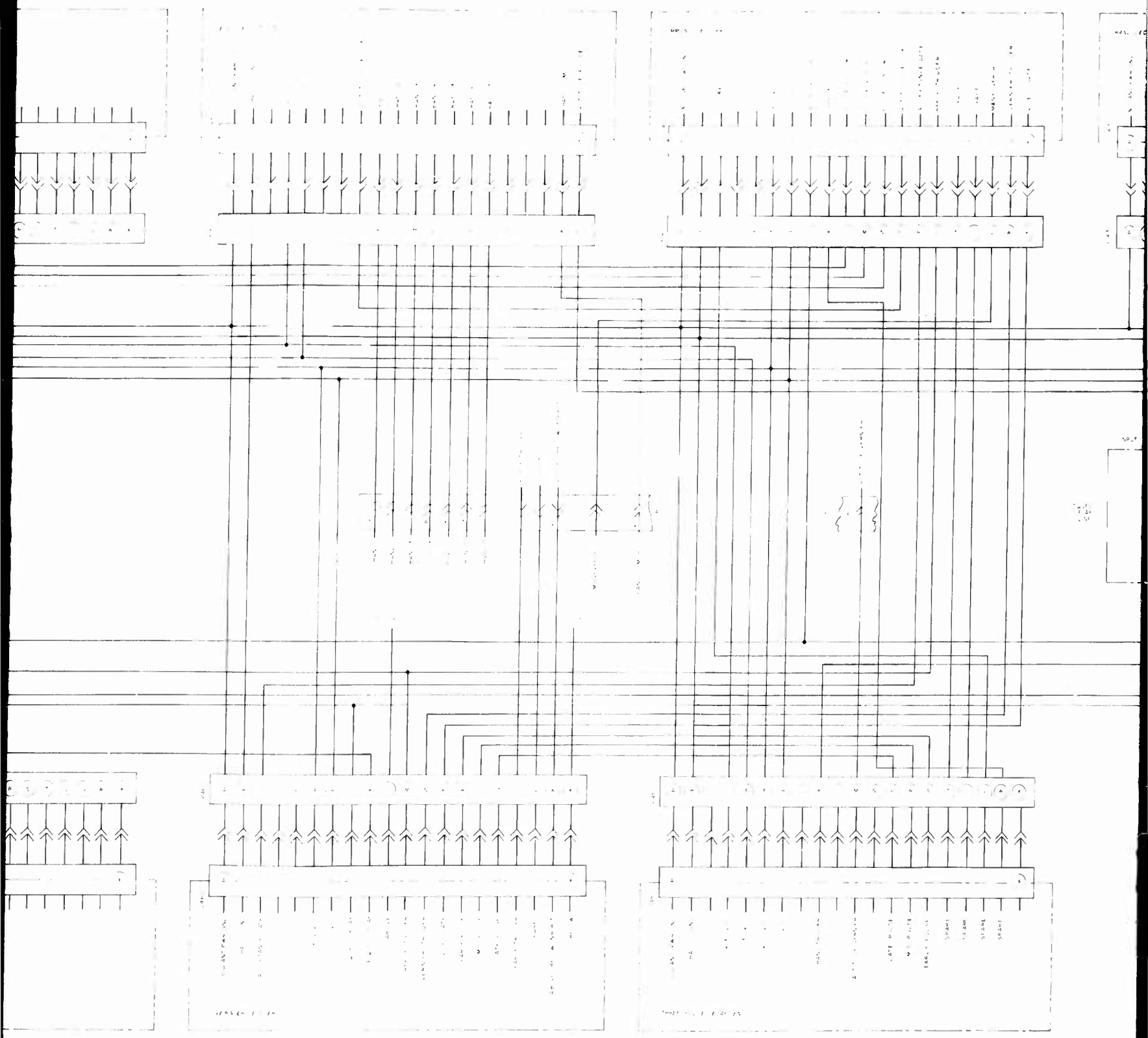
FIGURE 5-9
 TRANSPONDER ENCODER INTERCONNECTION DIAGRAM
 (UNIT SERIES DESIGNATION 3000)

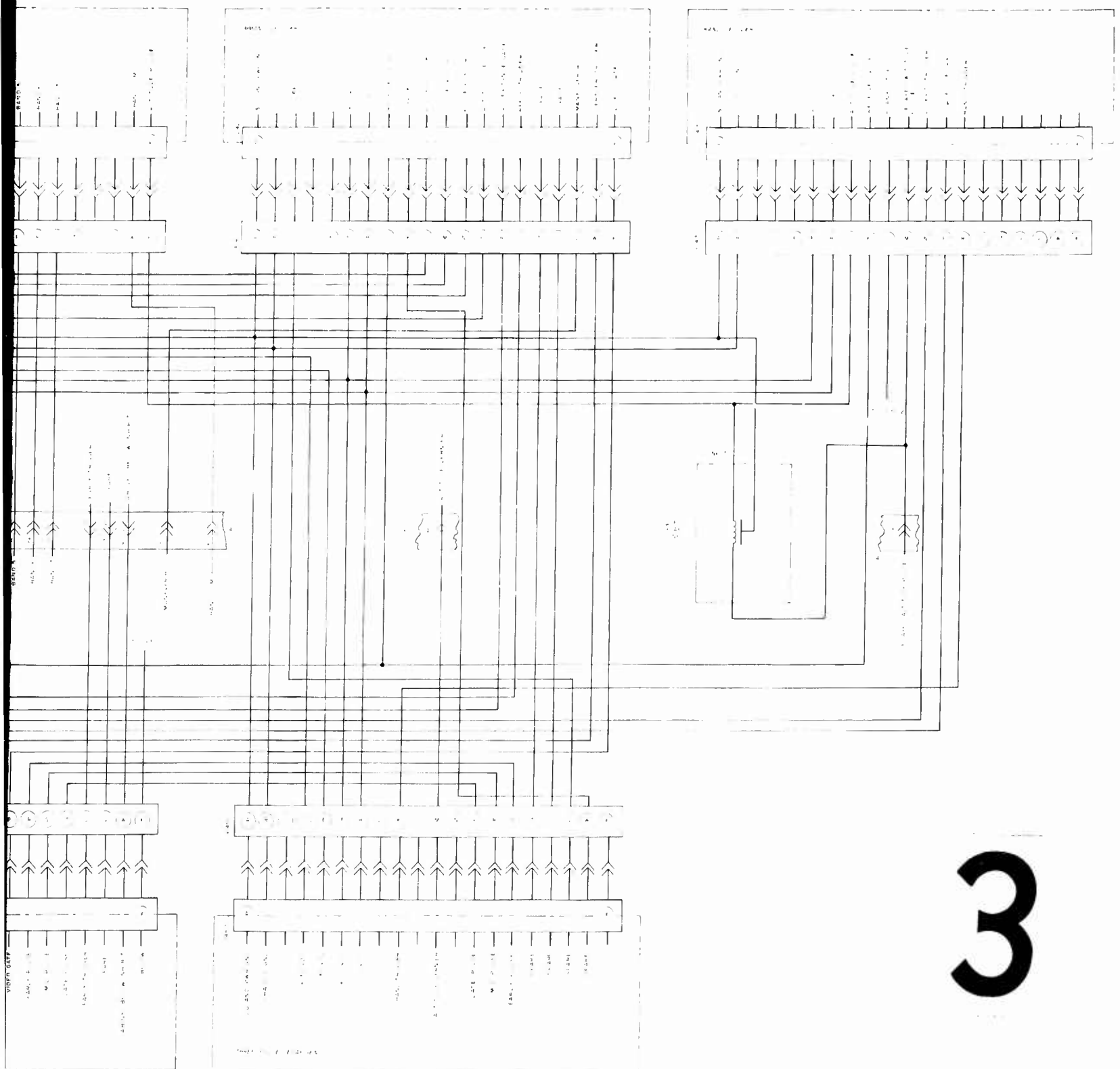
THESE WERE TO BE THE
MAIN SENSORS FOR THE
THEIR TERMINAL IN THE
CIVILIAN

MULTI-...
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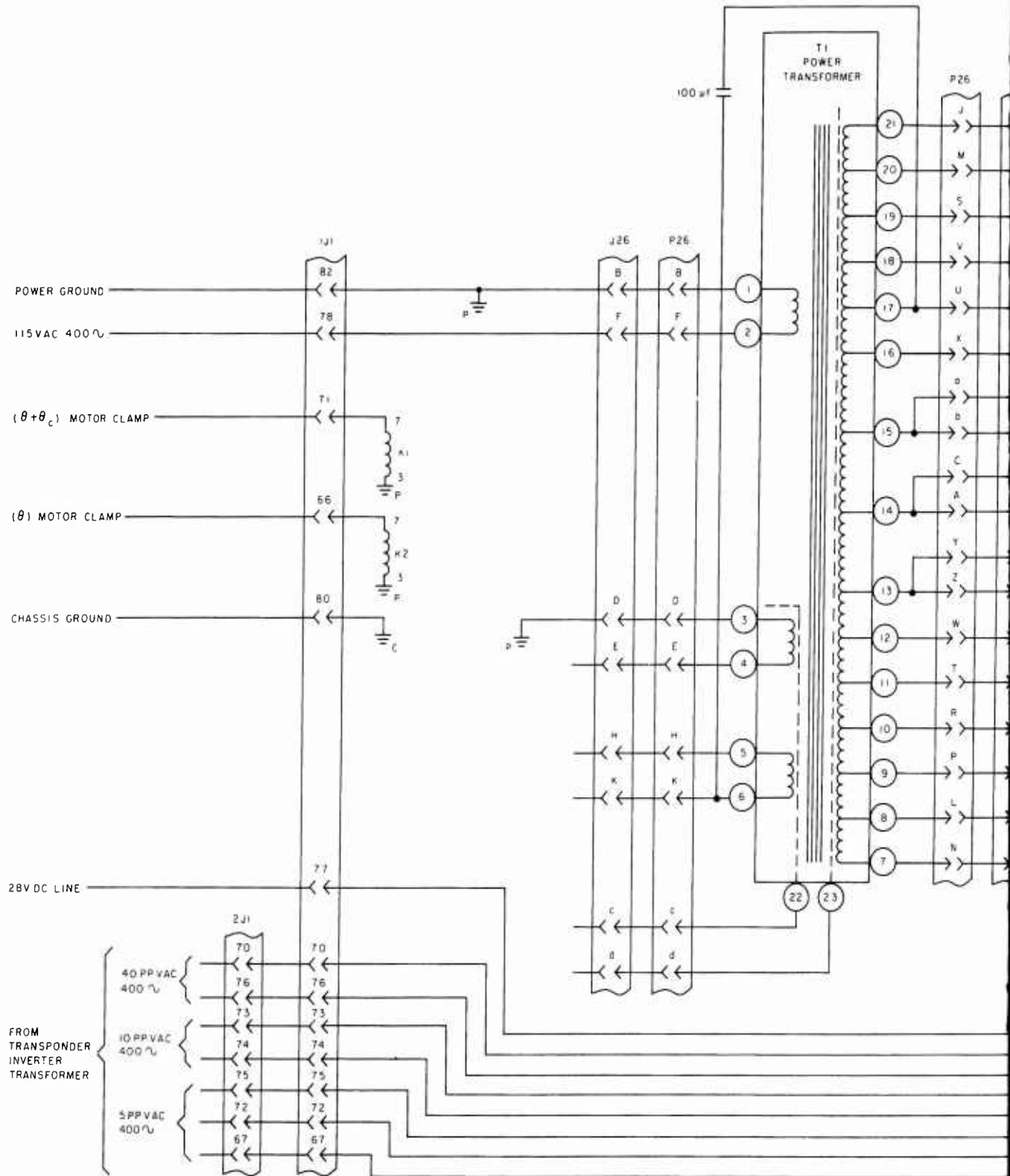
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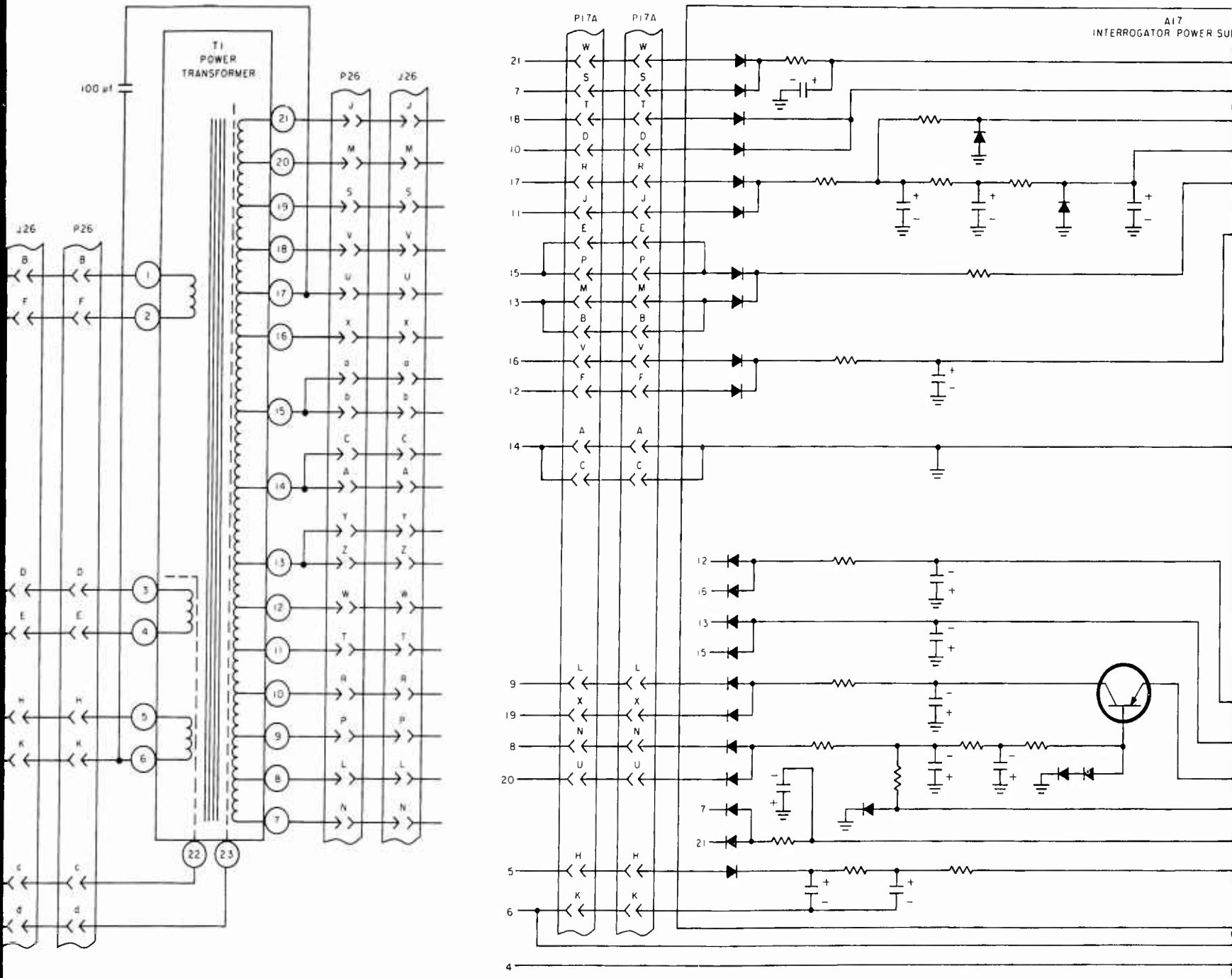


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FIGURE 5-10.
 TRANSPONDER DECODER INTERCONNECTION DIAGRAM
 (UNIT SERIES DESIGNATION 4000)



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A17
INTERROGATOR POWER SUPPLY (FOR DETAILS SEE FIGURE 5-54)

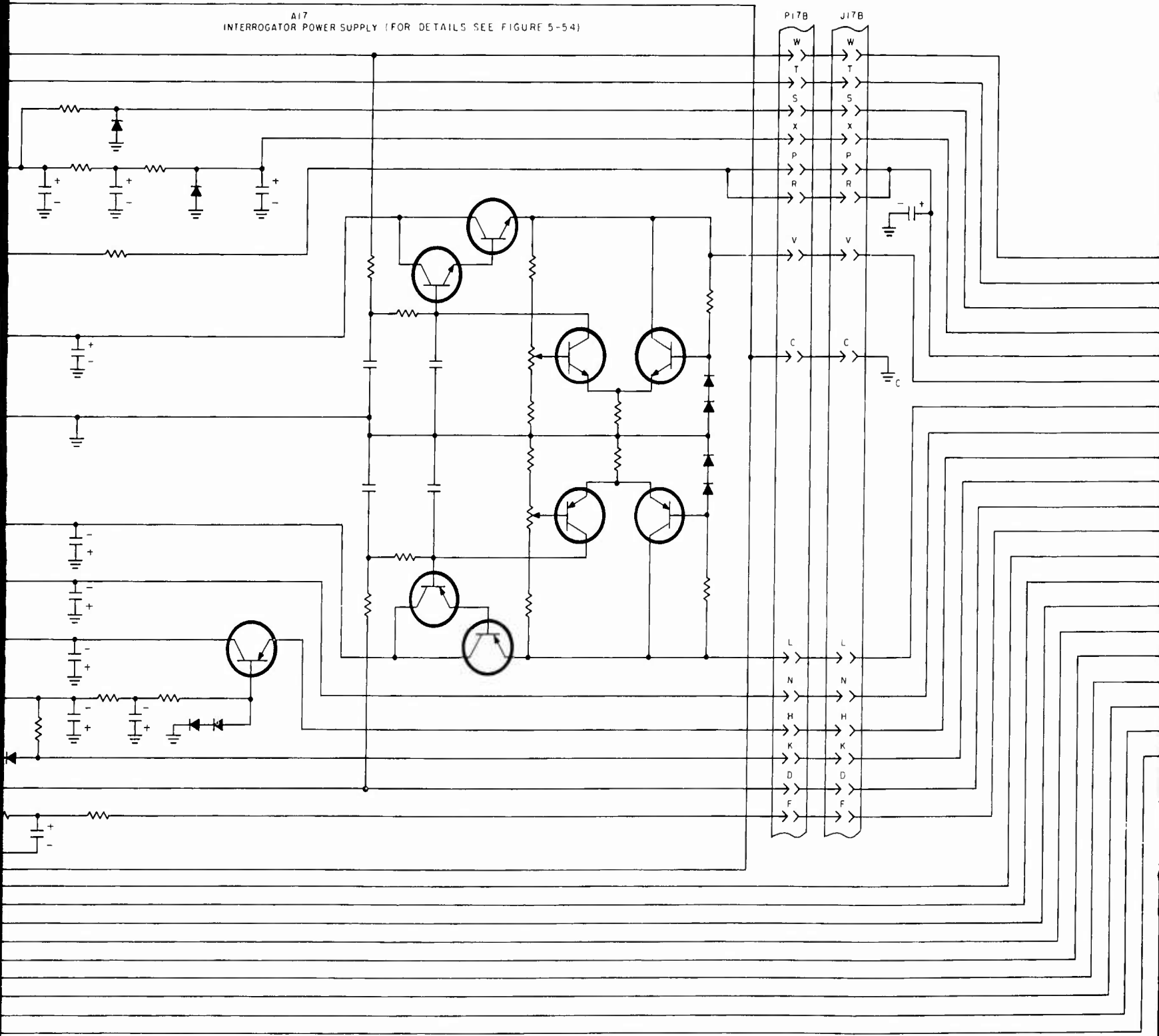
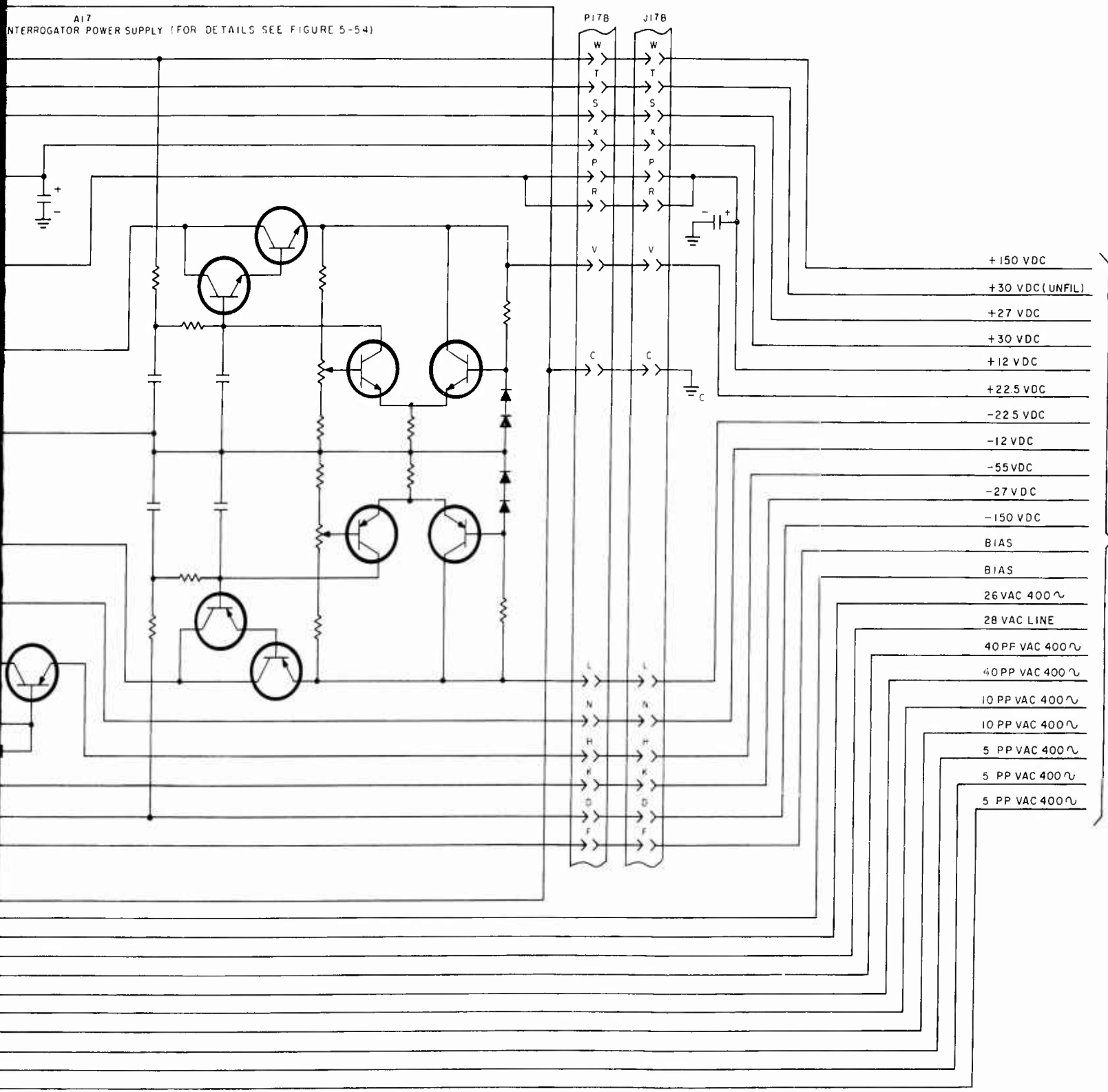


FIGURE 5-1

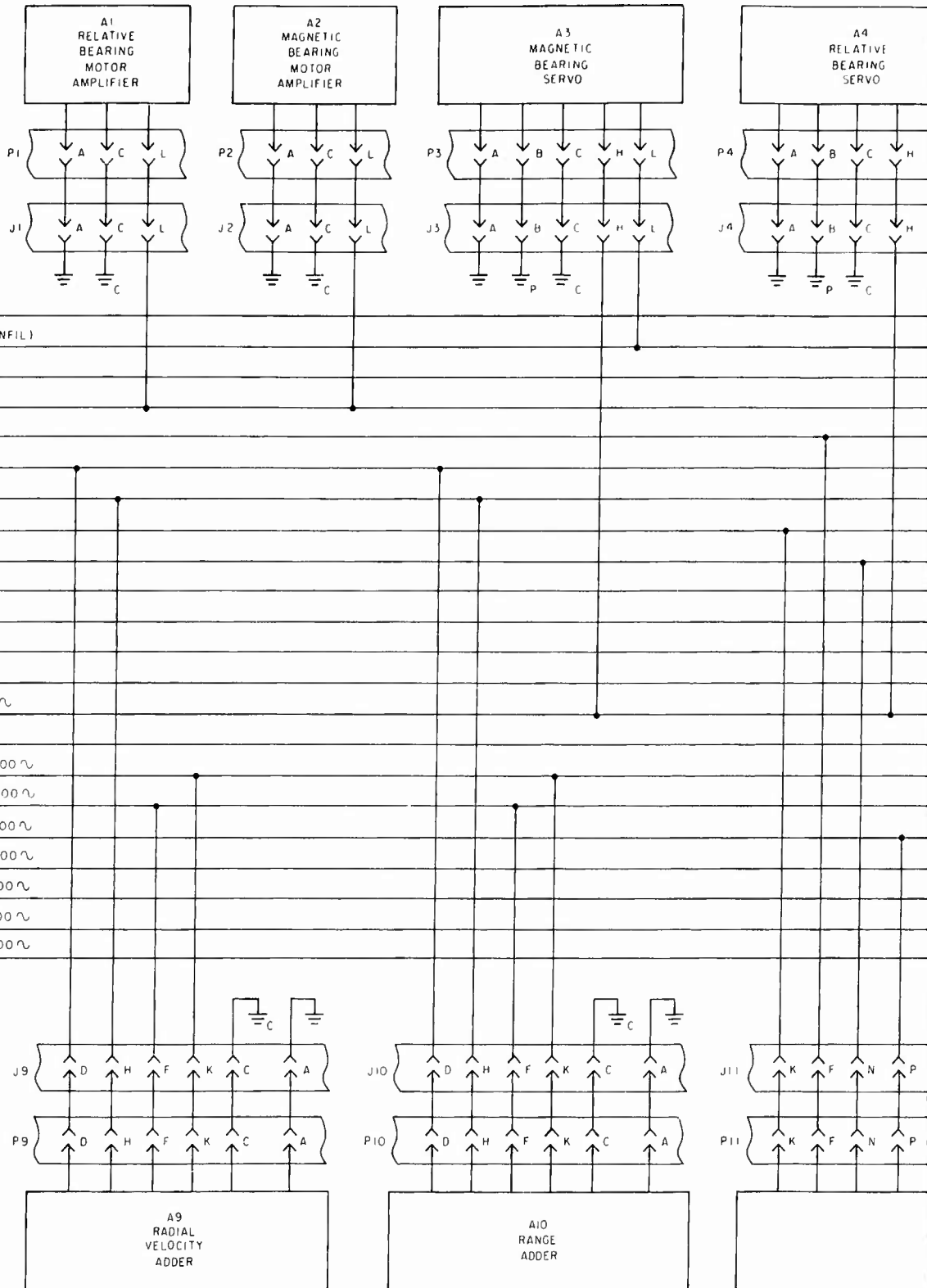
INTERROGATOR COMPUTER POWER SUPPLY

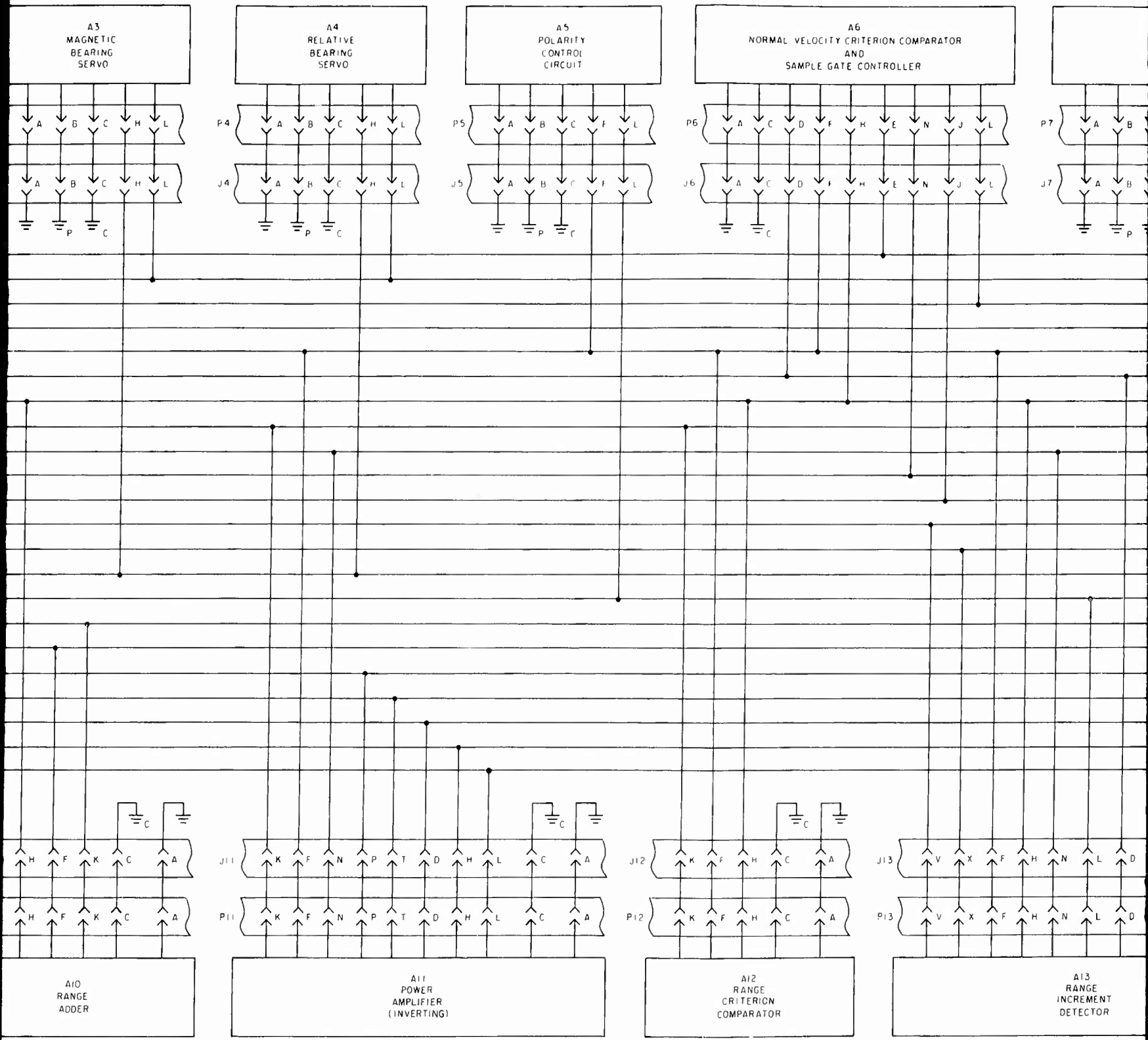


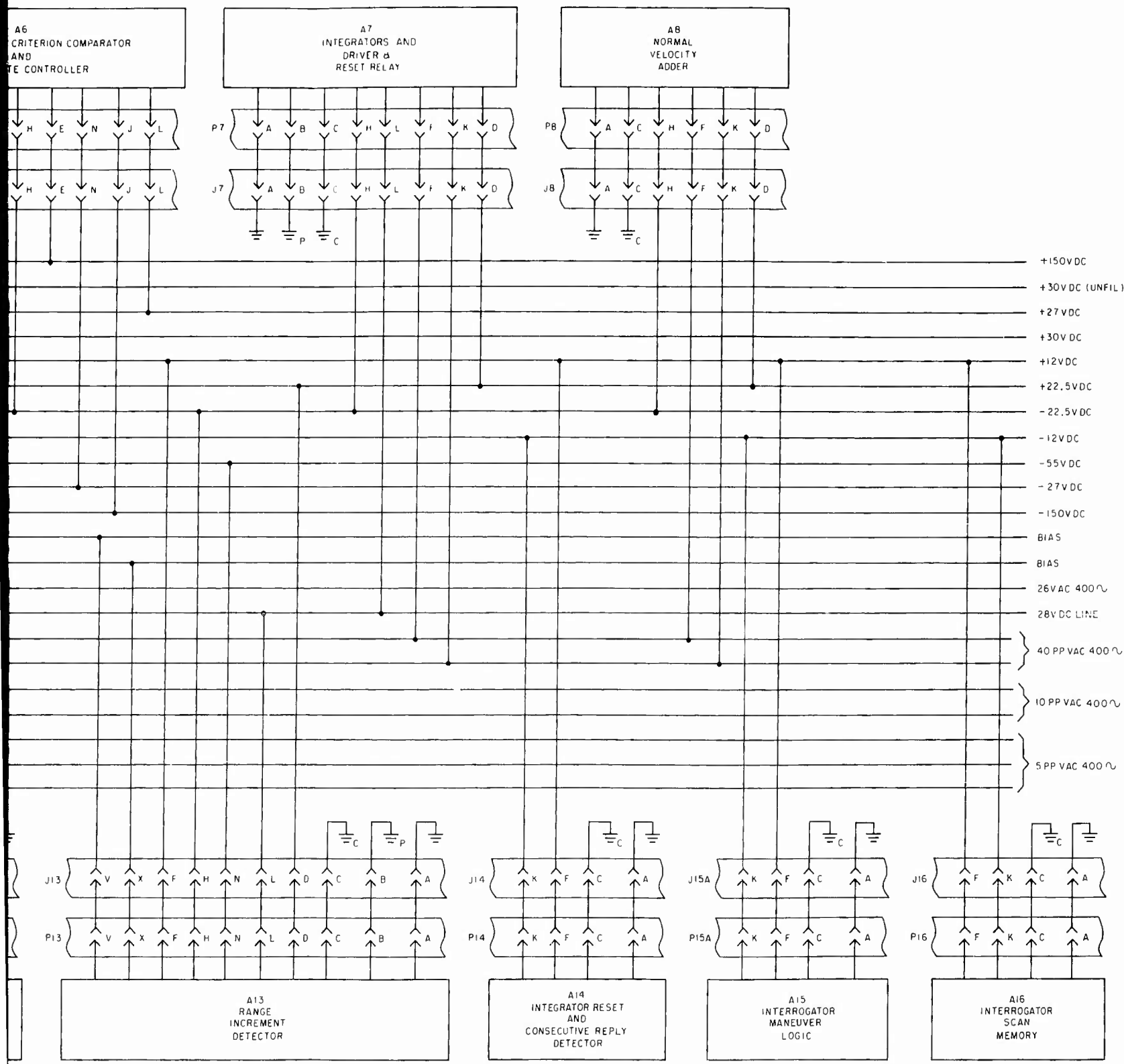
4

FIGURE 5-11.
INTERROGATOR COMPUTER POWER SCHEMATIC (SHEET 1 OF 2)

CONTINUED FROM SHEET 1







3

FIGURE 5-11.
INTERROGATOR COMPUTER POWER SCHEMATIC (SHEET 2 OF 2)

CORE - E1-12 STACK 10"
 SECONDARY BIFILAR WOUND
 ALL WINDINGS NO 26 SWG

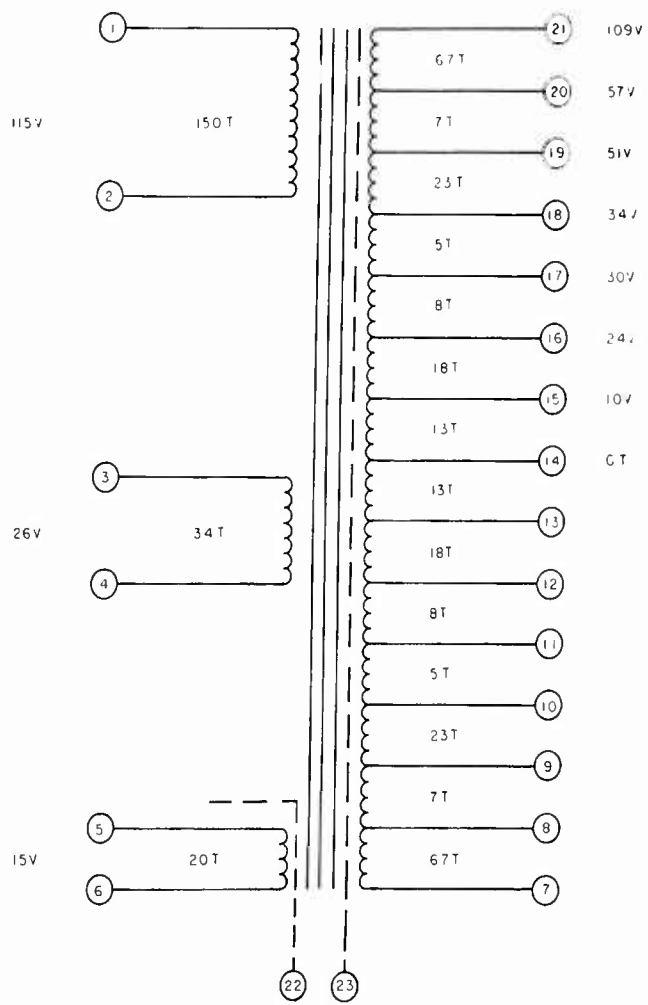
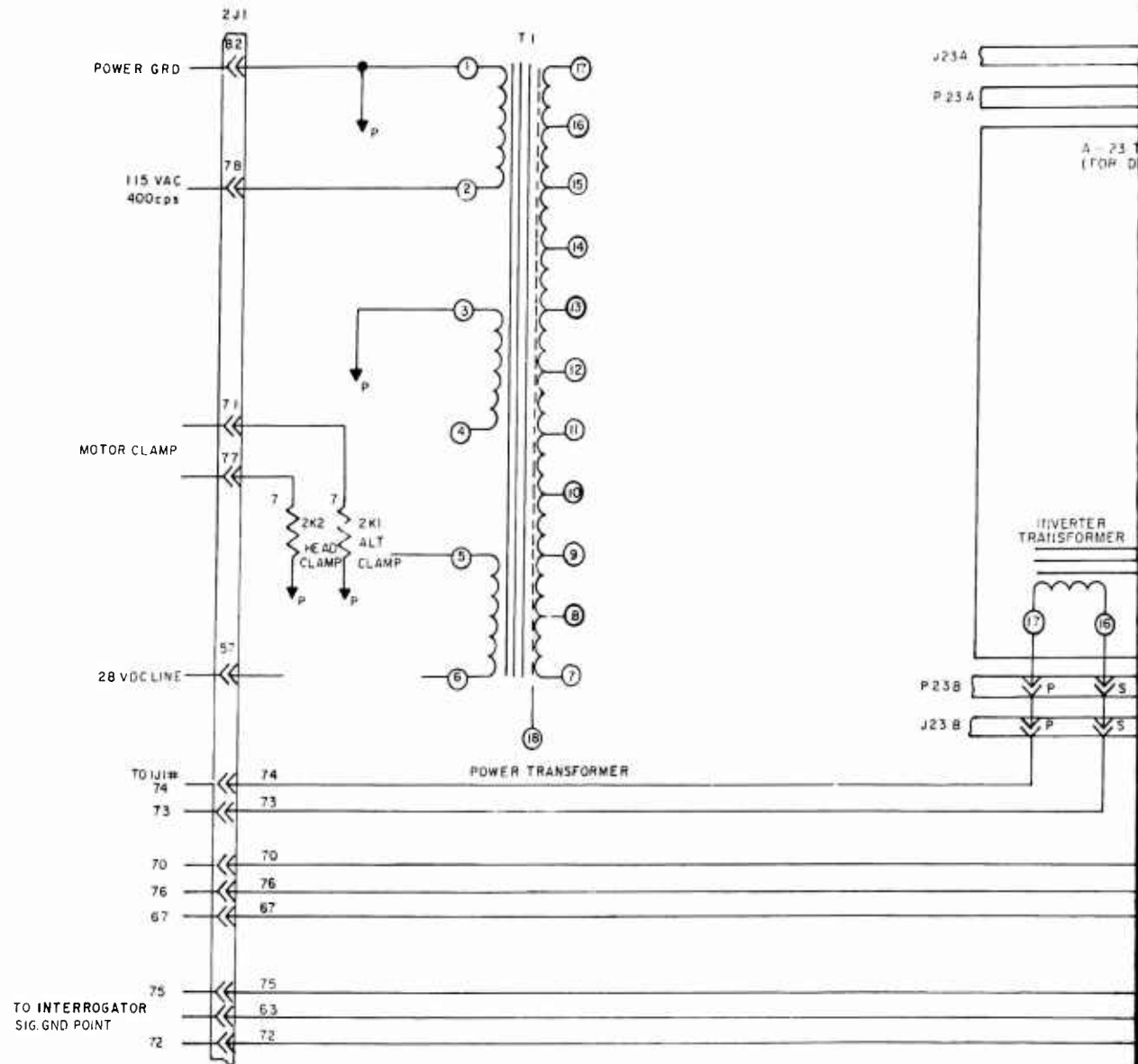
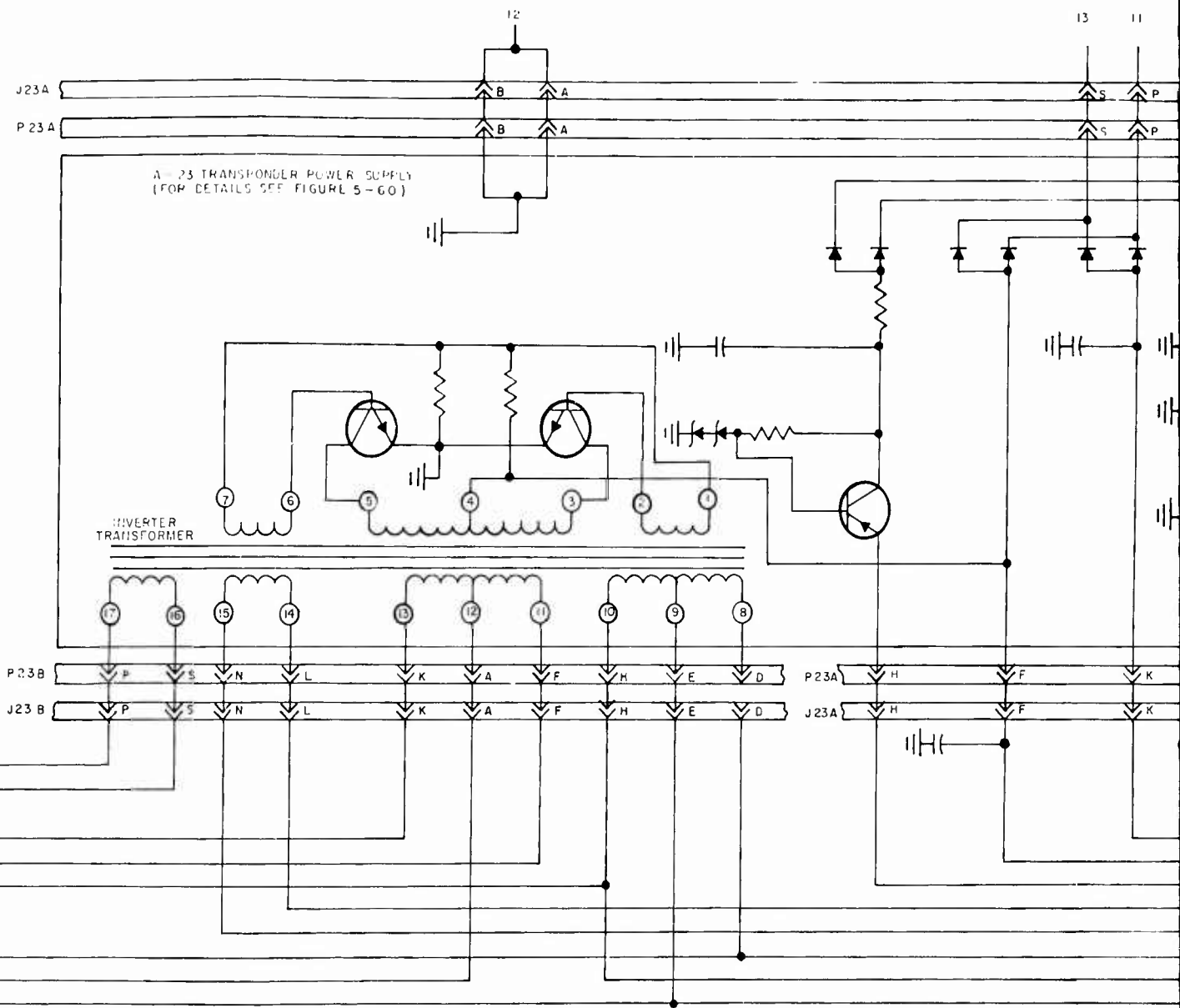


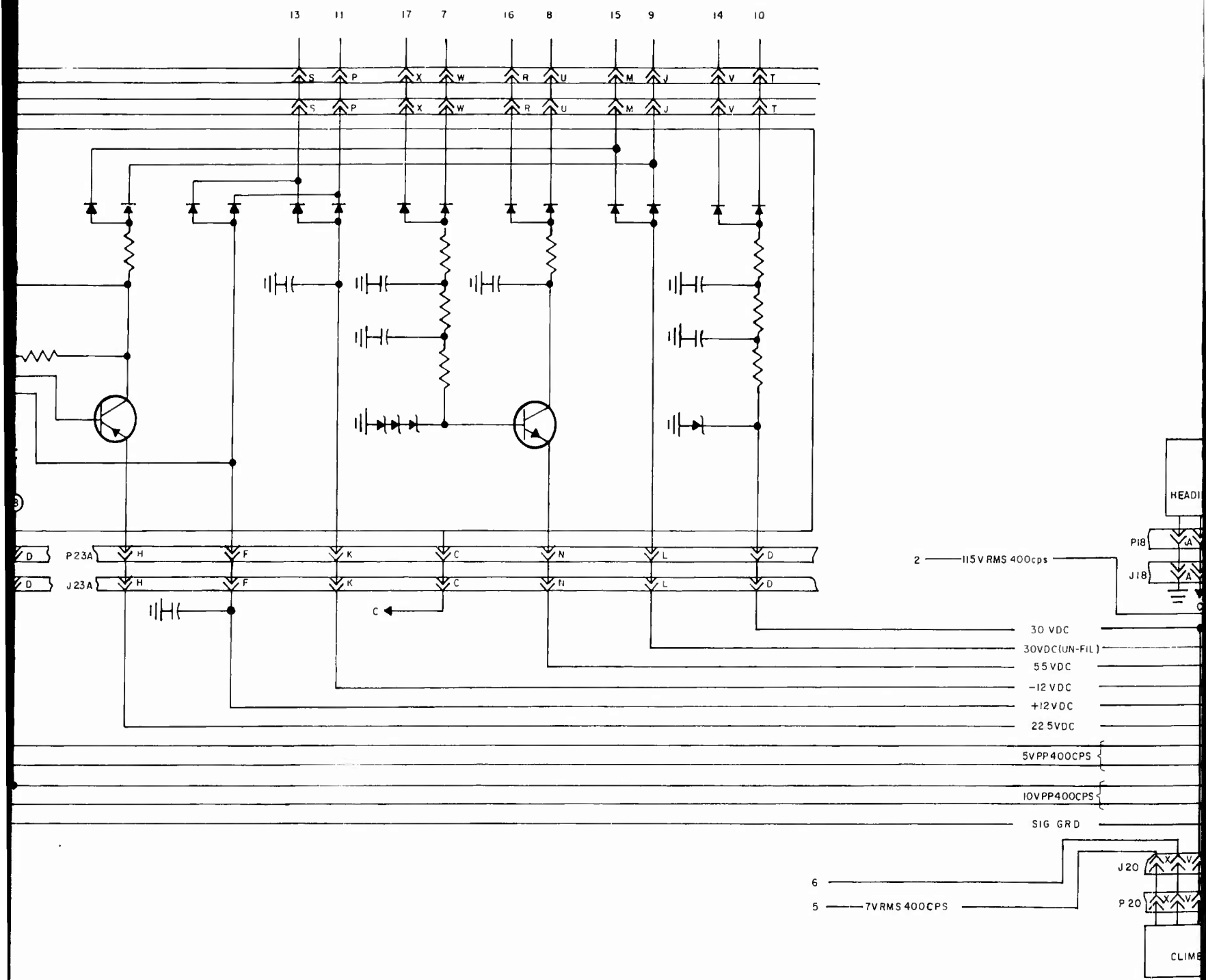
FIGURE 5-12. INTERROGATOR POWER TRANSFORMER



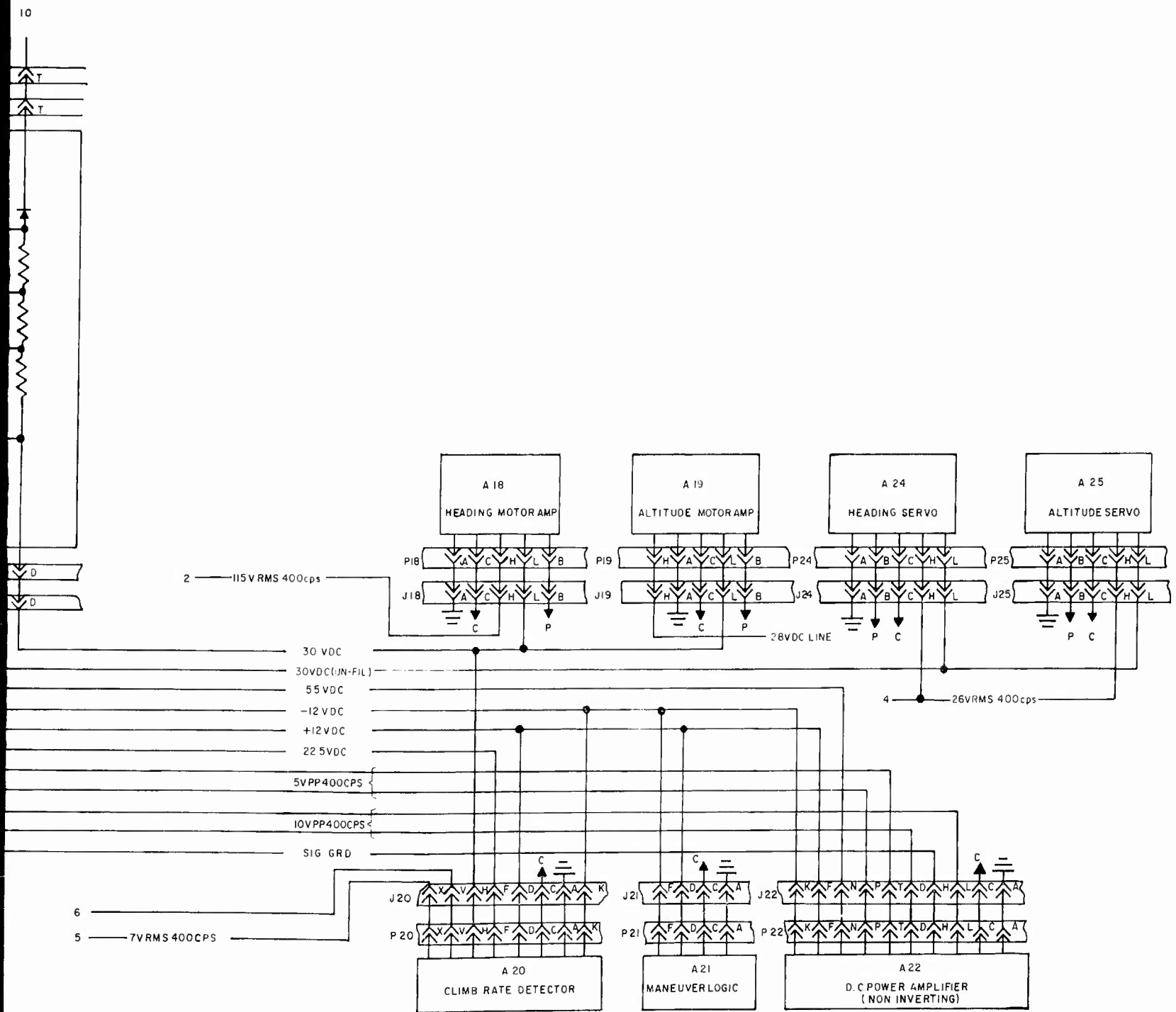
1



2



3



4

FIGURE 5 13
TRANSPONDER COMPUTER POWER SCHEMATIC

CORE E1 — 625 STACK 65" ALL
WINDINGS NO 26 SWG SECONDARY —
BIFILAR WOUND

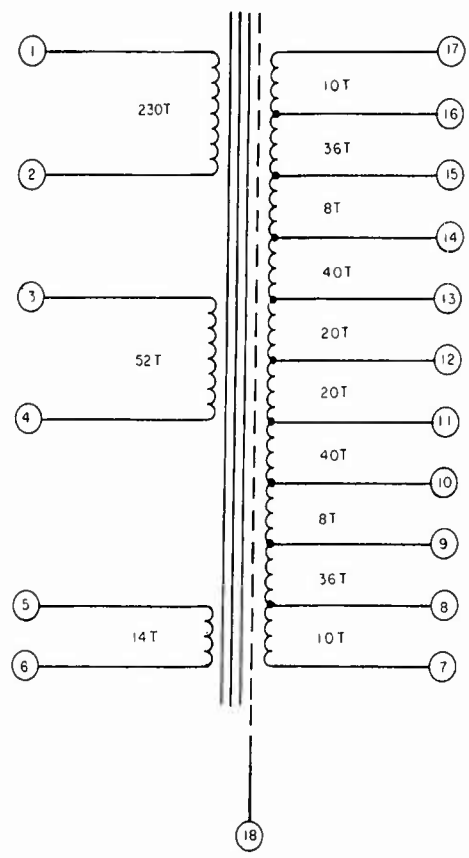
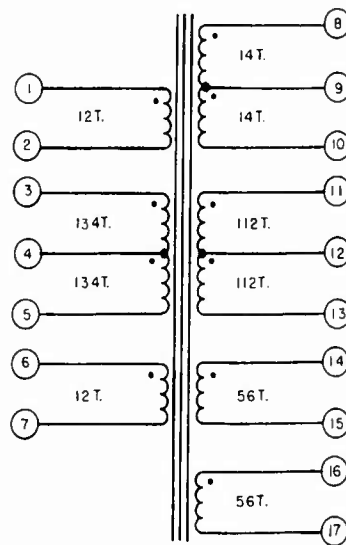


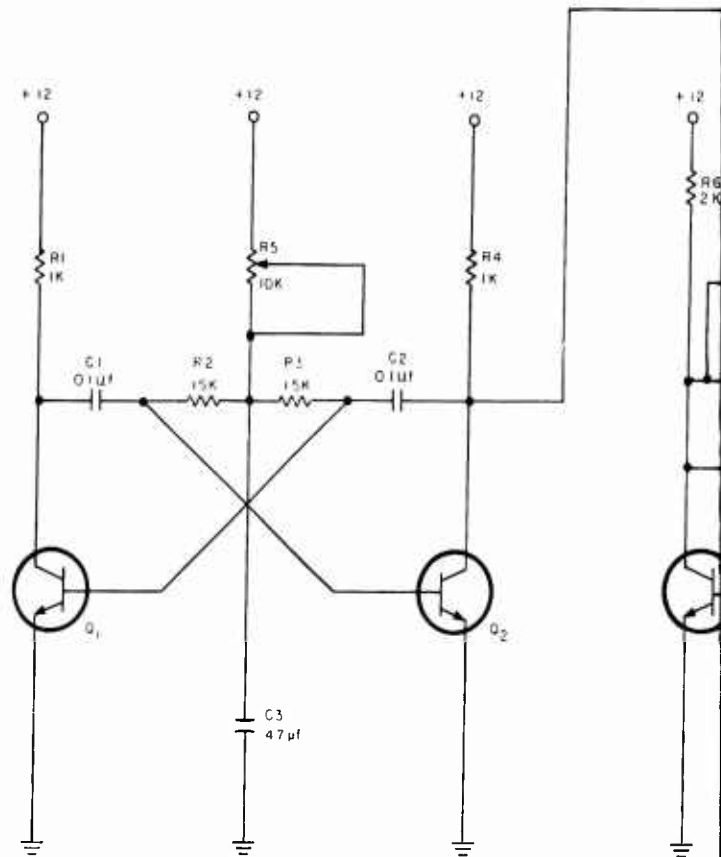
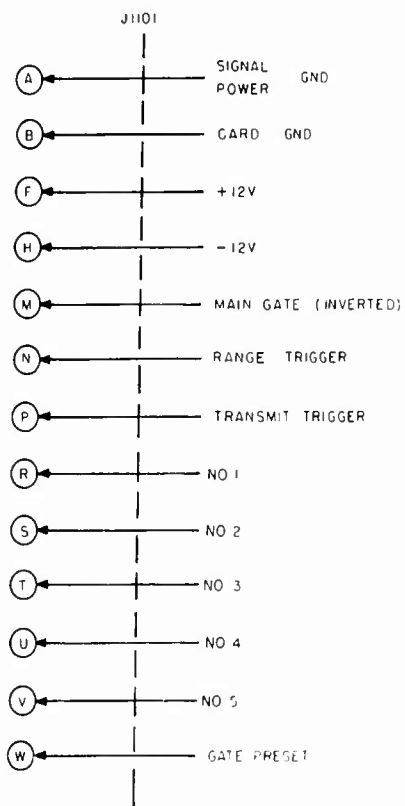
FIGURE 5-14. TRANSPONDER POWER TRANSFORMER



TR - T 100

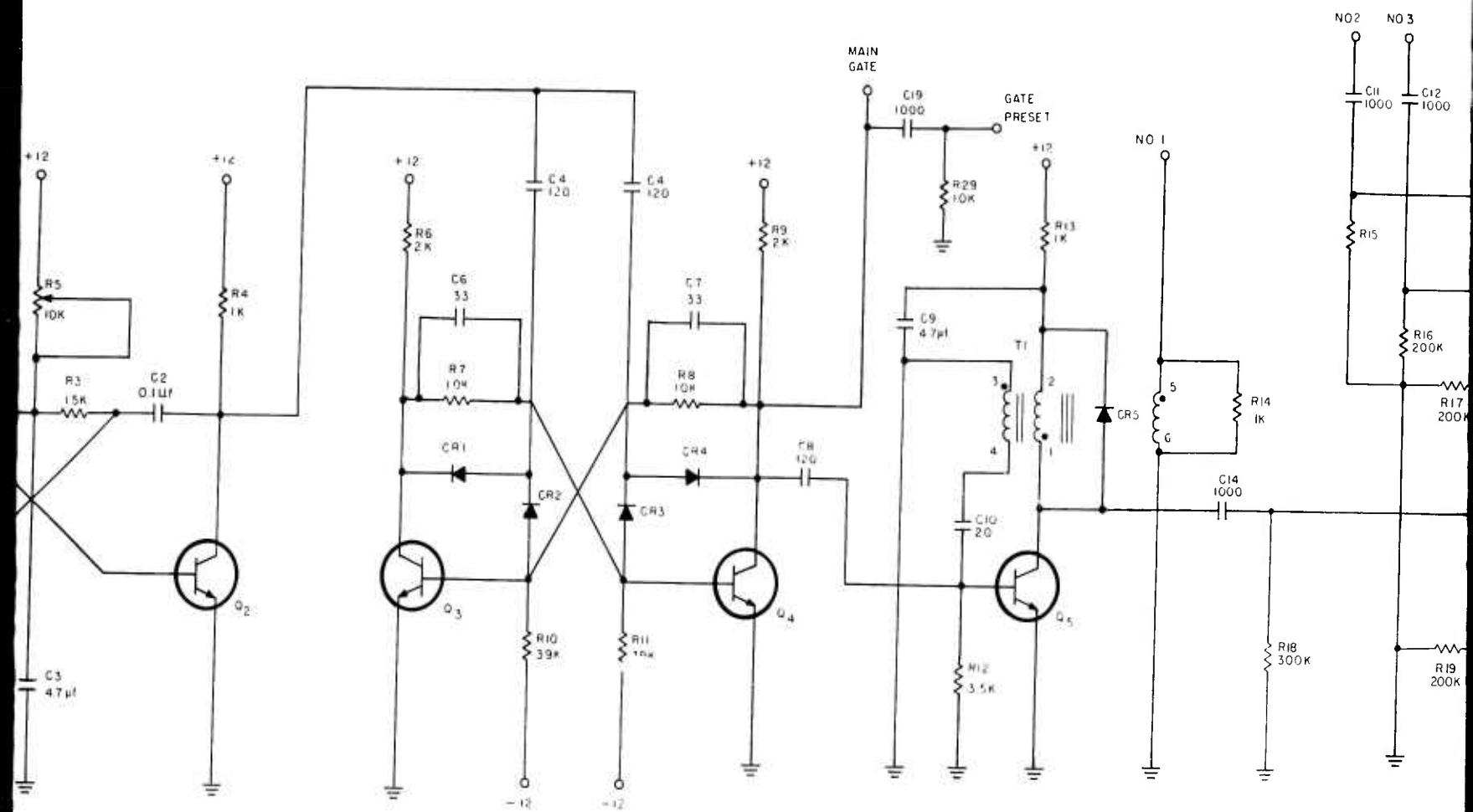
ALL WINDINGS NO.30 SWG
 CORE - MAGNETICS INC. ORTHONOL NO.50034, 1 MIL TAPE
 TAPPED WINDINGS ARE BIFILAR WOUND

FIGURE 5-15. INVERTER TRANSFORMER



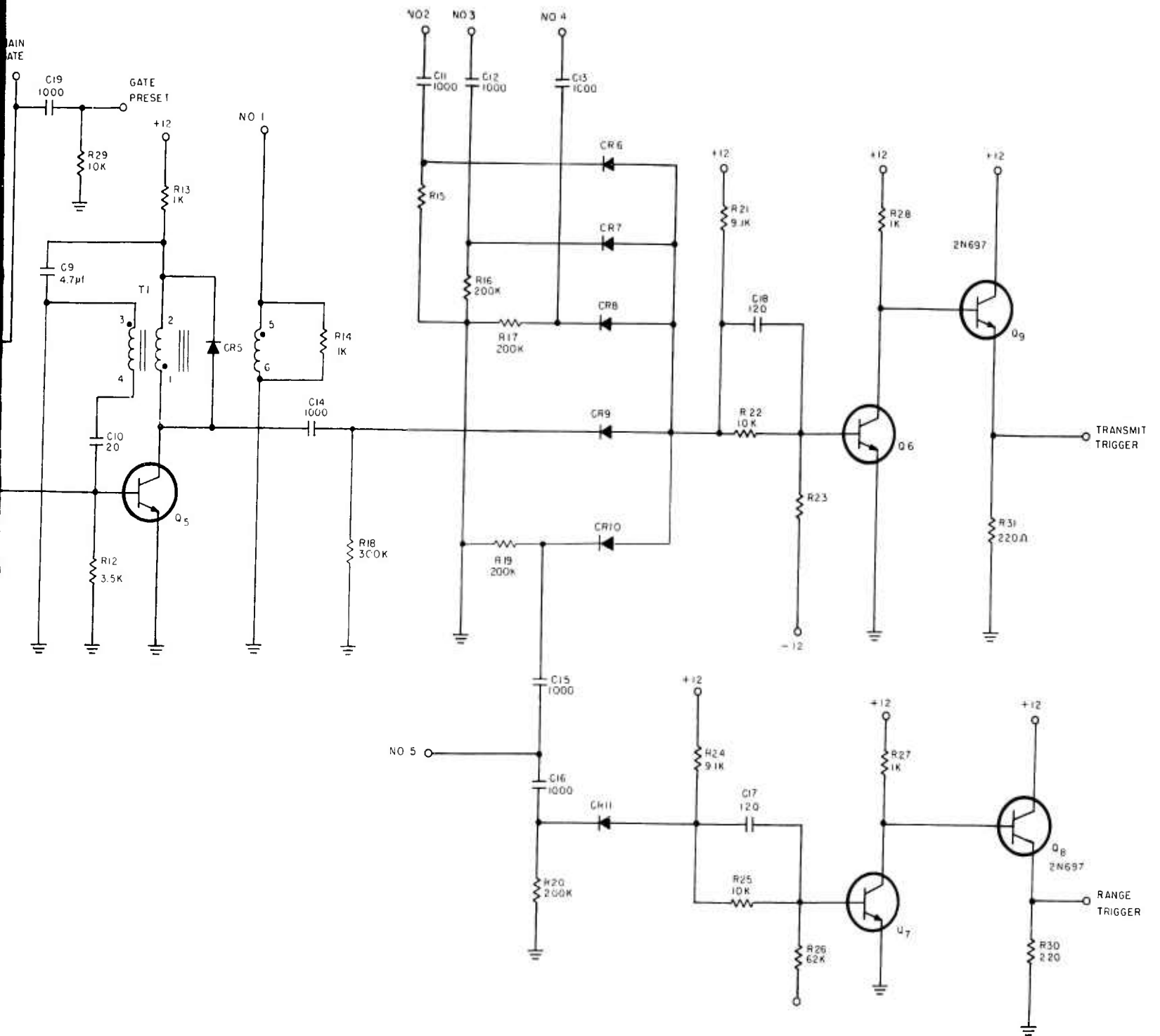
NOTE 1 ALL RESISTORS IN OHMS
 2 ALL CAPACITORS IN P.F.
 3 ALL DIODES TYPE 1N4001
 4 ALL TRANSISTORS TYPE 2N3055

1



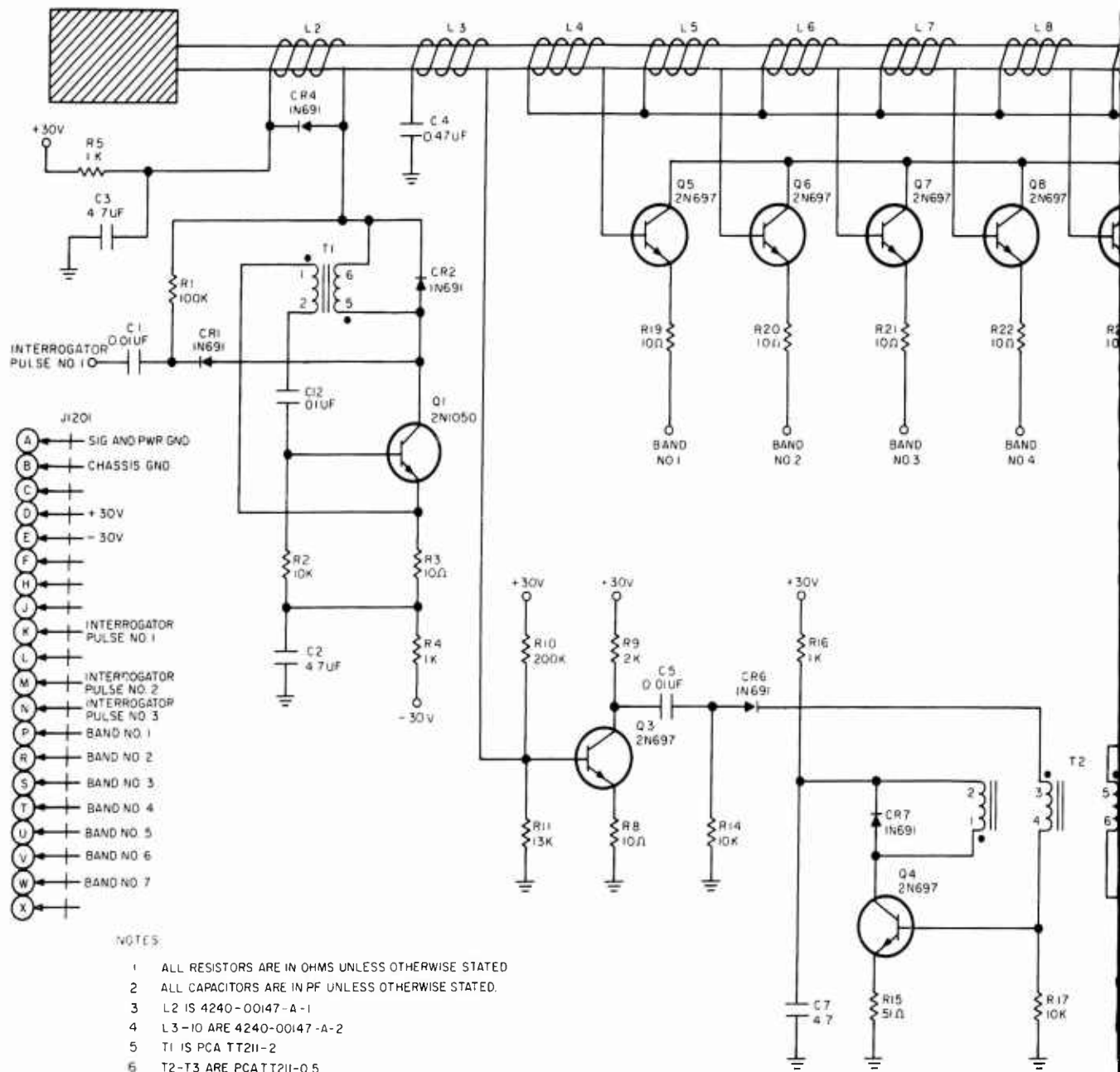
- NOTE 1 ALL RESISTORS IN OHMS
 2 ALL CAPACITORS IN pF UNLESS OTHERWISE SPECIFIED
 3 ALL DIODES TYPE 1N691
 4 ALL TRANSISTORS TYPE 2N709 UNLESS OTHERWISE NOTED

2

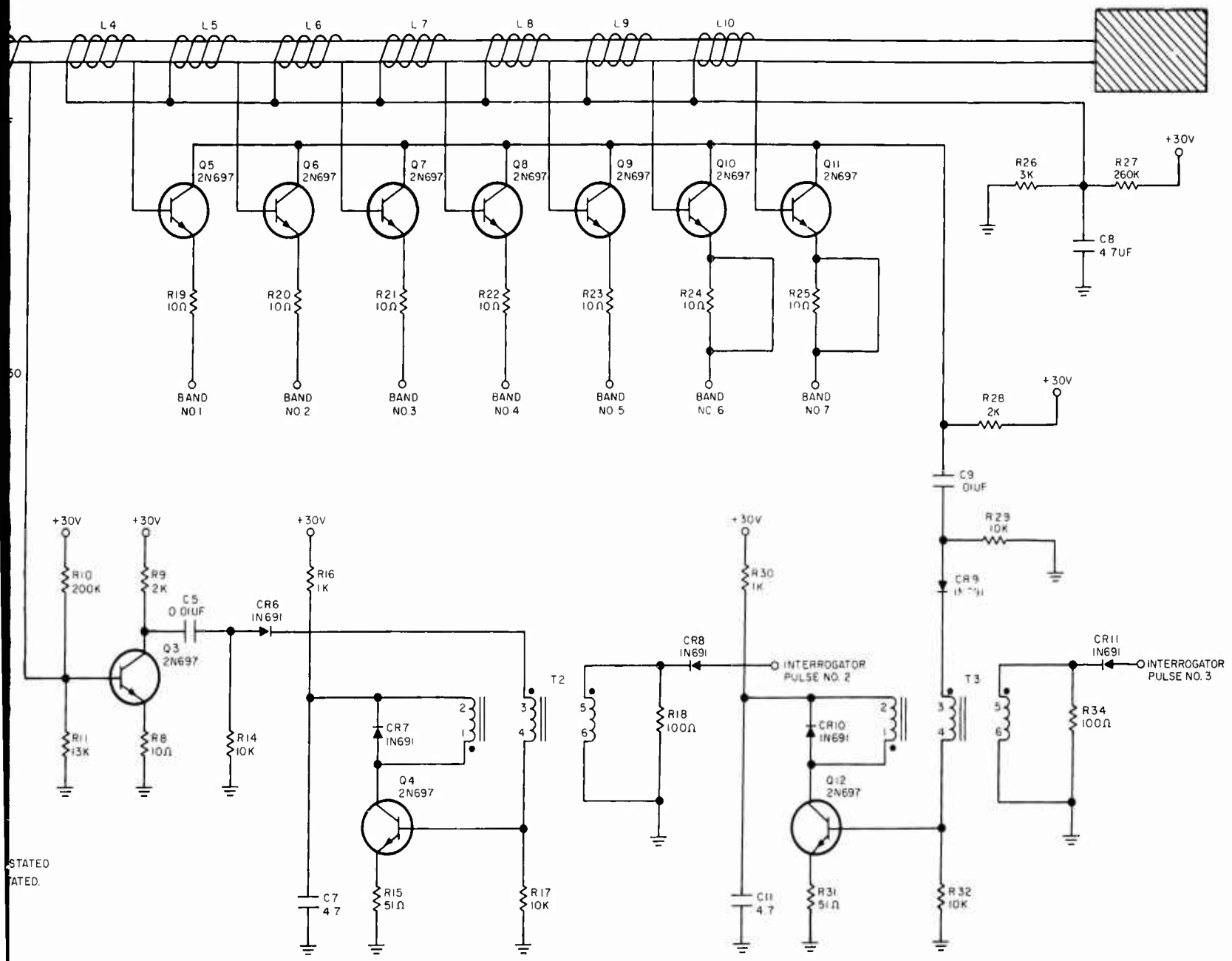


3

FIGURE 5-16
PULSE AND GATE GENERATOR MIXER AMPLIFIER 1100
CAS SCHEMATIC



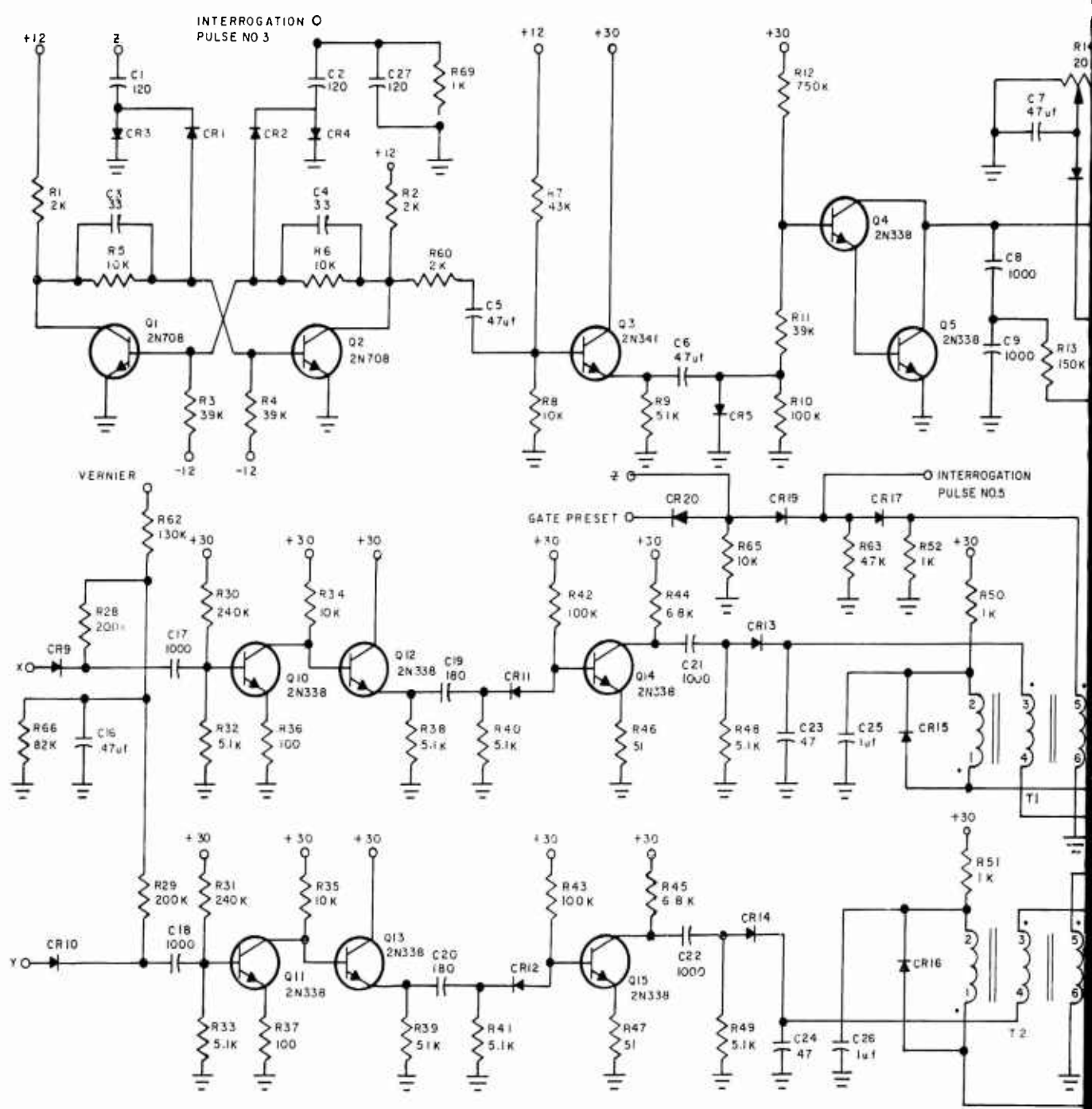
1



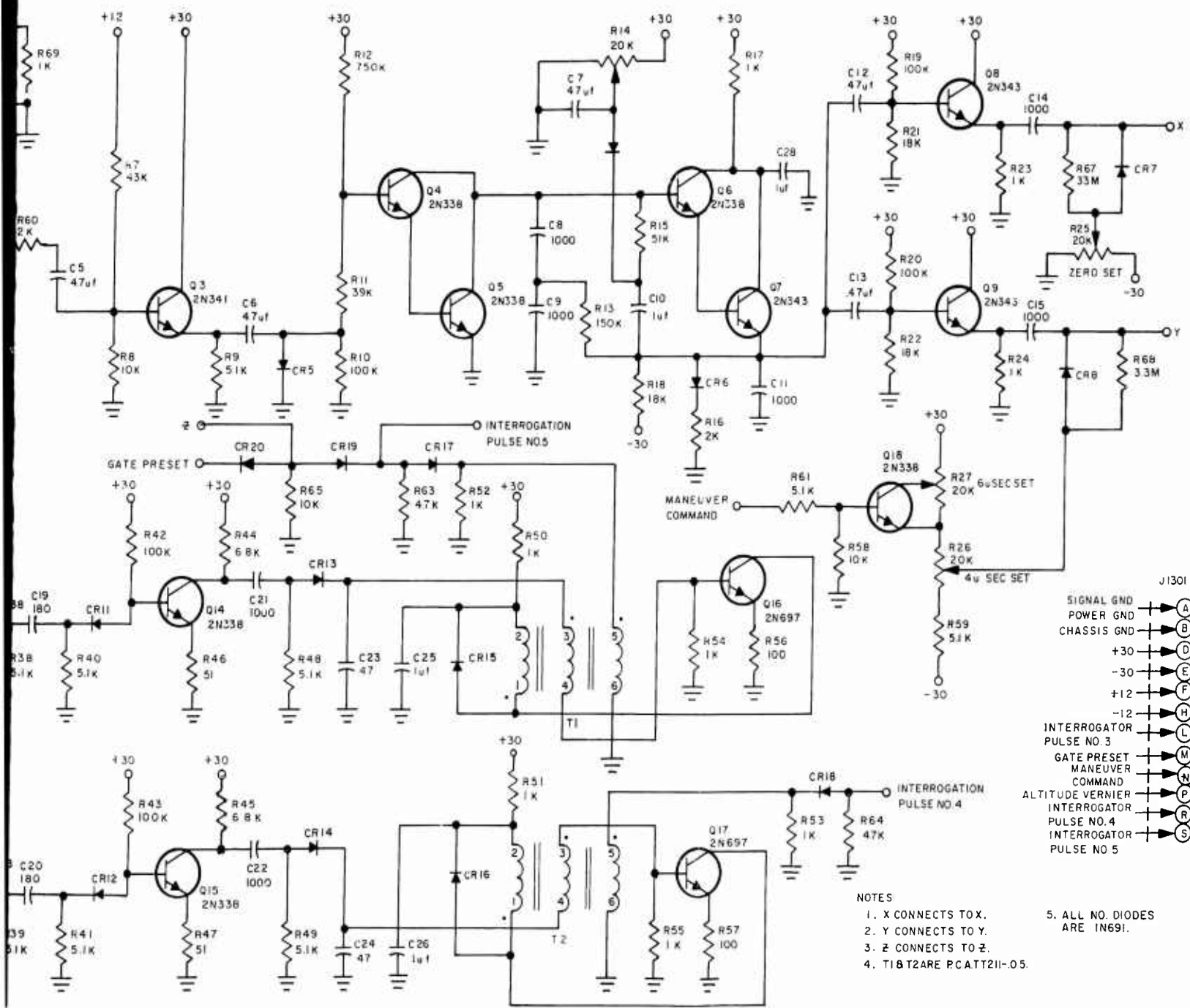
STATED
ATED.

2

FIGURE 5 17
INTERROGATOR ENCODER CONTROL CODER (1200)



1

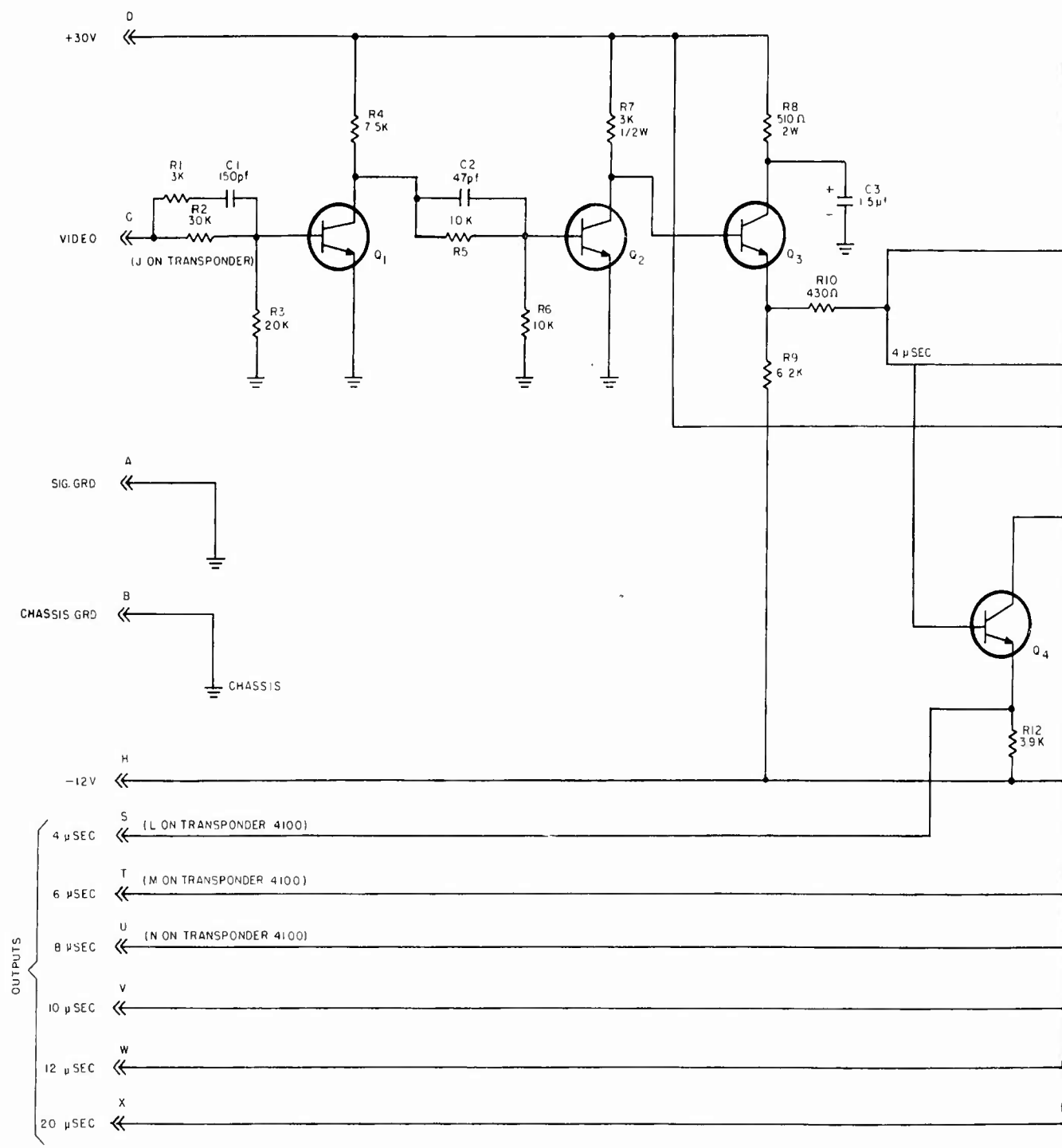


- J1301
- SIGNAL GND → (A)
 - POWER GND → (B)
 - CHASSIS GND → (C)
 - +30 → (D)
 - 30 → (E)
 - +12 → (F)
 - 12 → (H)
 - INTERROGATOR PULSE NO 3 → (L)
 - GATE PRESET → (M)
 - MANEUVER COMMAND → (N)
 - ALTITUDE VERNIER → (P)
 - INTERROGATOR PULSE NO 4 → (R)
 - INTERROGATOR PULSE NO 5 → (S)

- NOTES
1. X CONNECTS TO X.
 2. Y CONNECTS TO Y.
 3. Z CONNECTS TO Z.
 4. T1 & T2 ARE PCATT211-05.
 5. ALL NO. DIODES ARE 1N691.

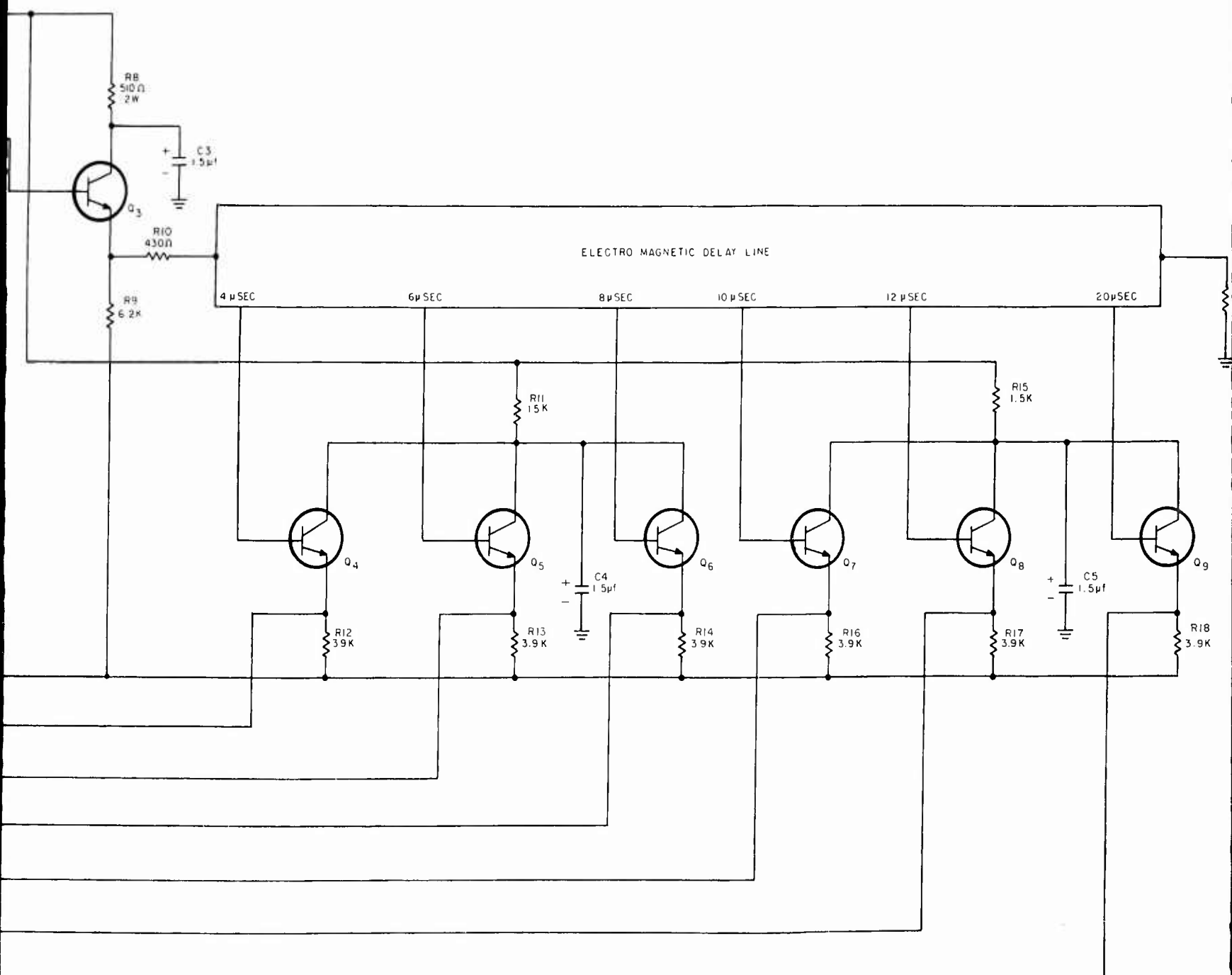
2

FIGURE 5-18
VERNIER CODER (1300)



NOTE: Q_7 , Q_8 , Q_9 , AND OUTPUTS (10 μSEC, 12 μSEC, 20 μSEC) DO NOT EXIST ON TRANSPONDER DELAY L



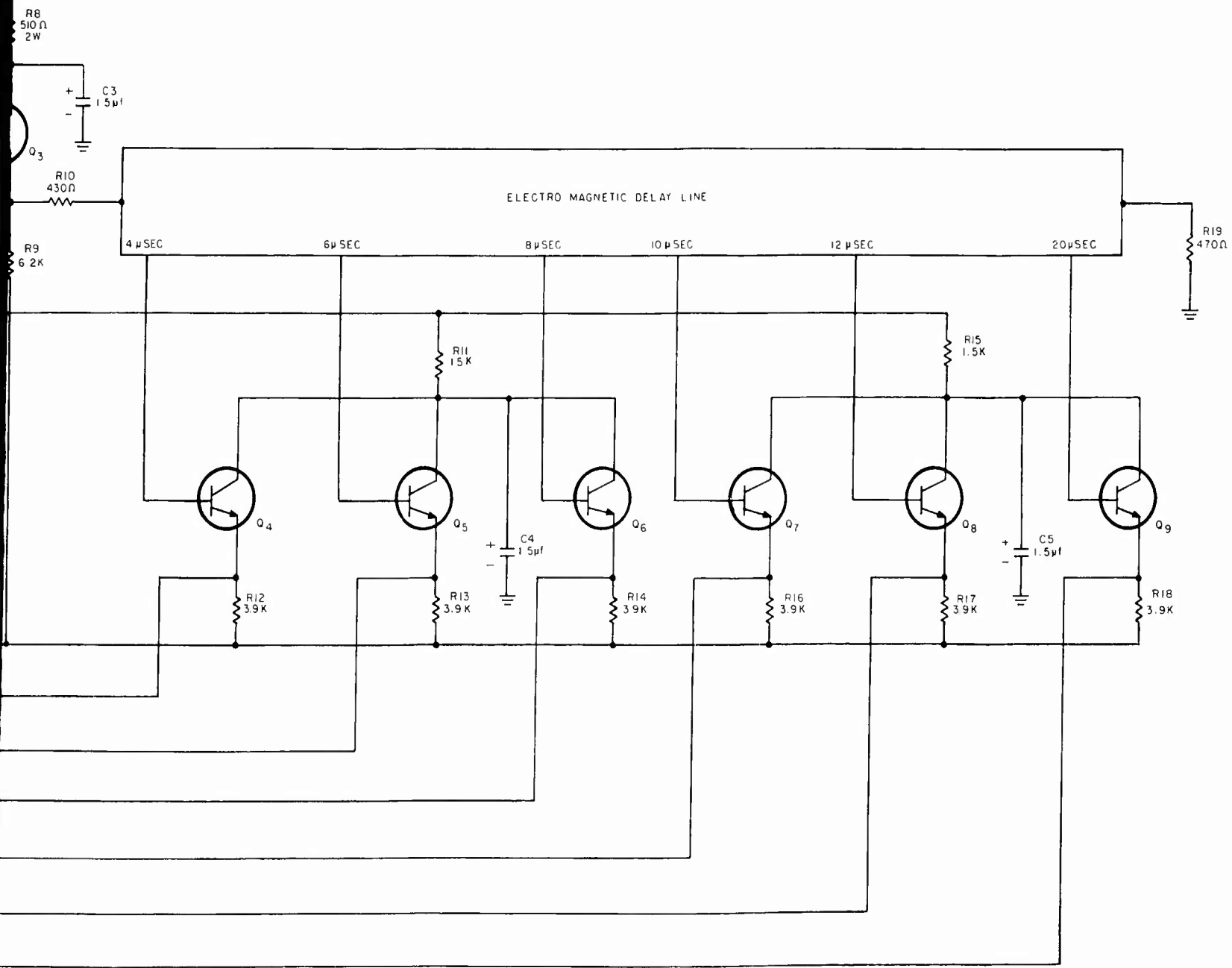


20 μSEC) DO NOT EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

- Q₁ Q₄ ——— Q₉ ——— 2N1104 OR 2N338
- Q₂ ——— 2N708
- Q₃ ——— 2N699

FIGURE 5-19
DECODER DELAY LINE AND DRIVER (INTERROGATOR
TRANSPONDER) (2100 AND 4100)

2

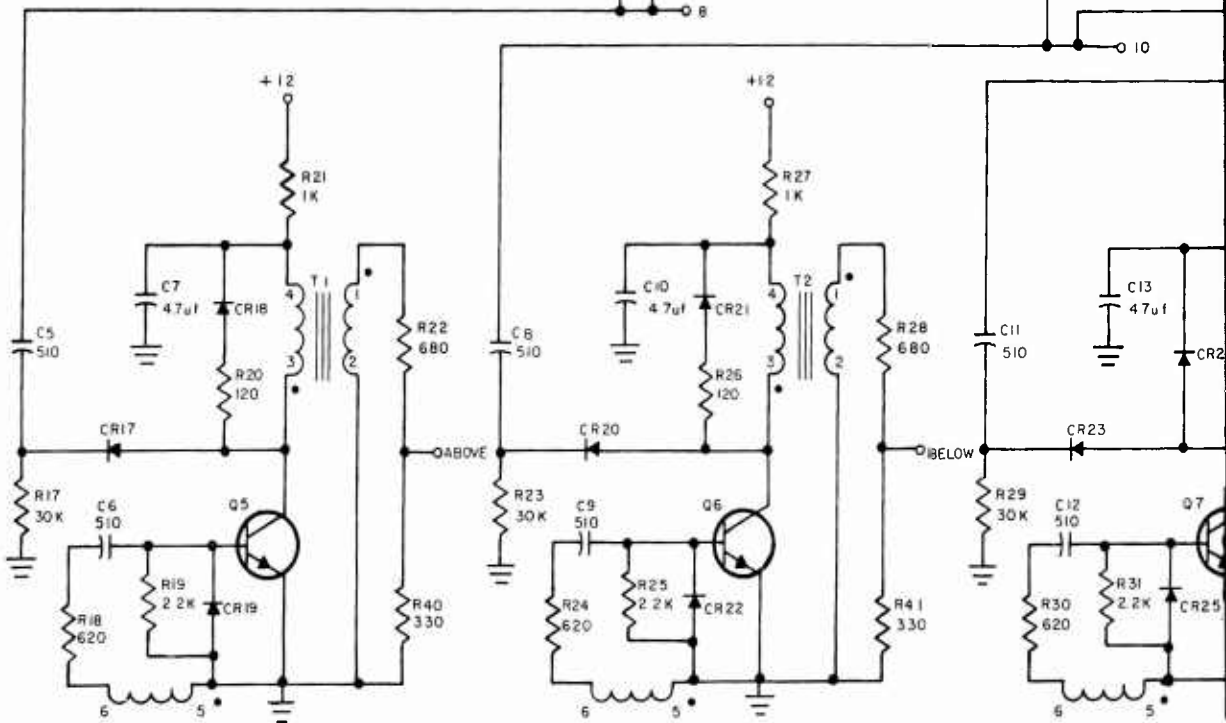
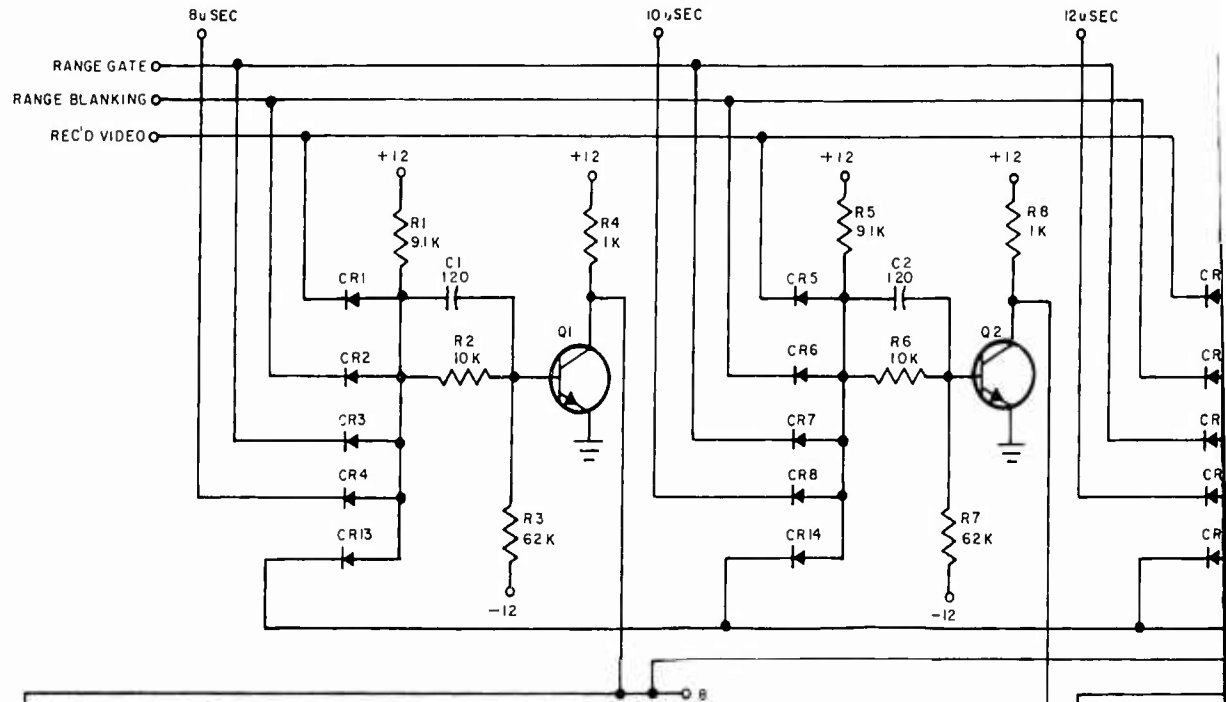


NOT EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

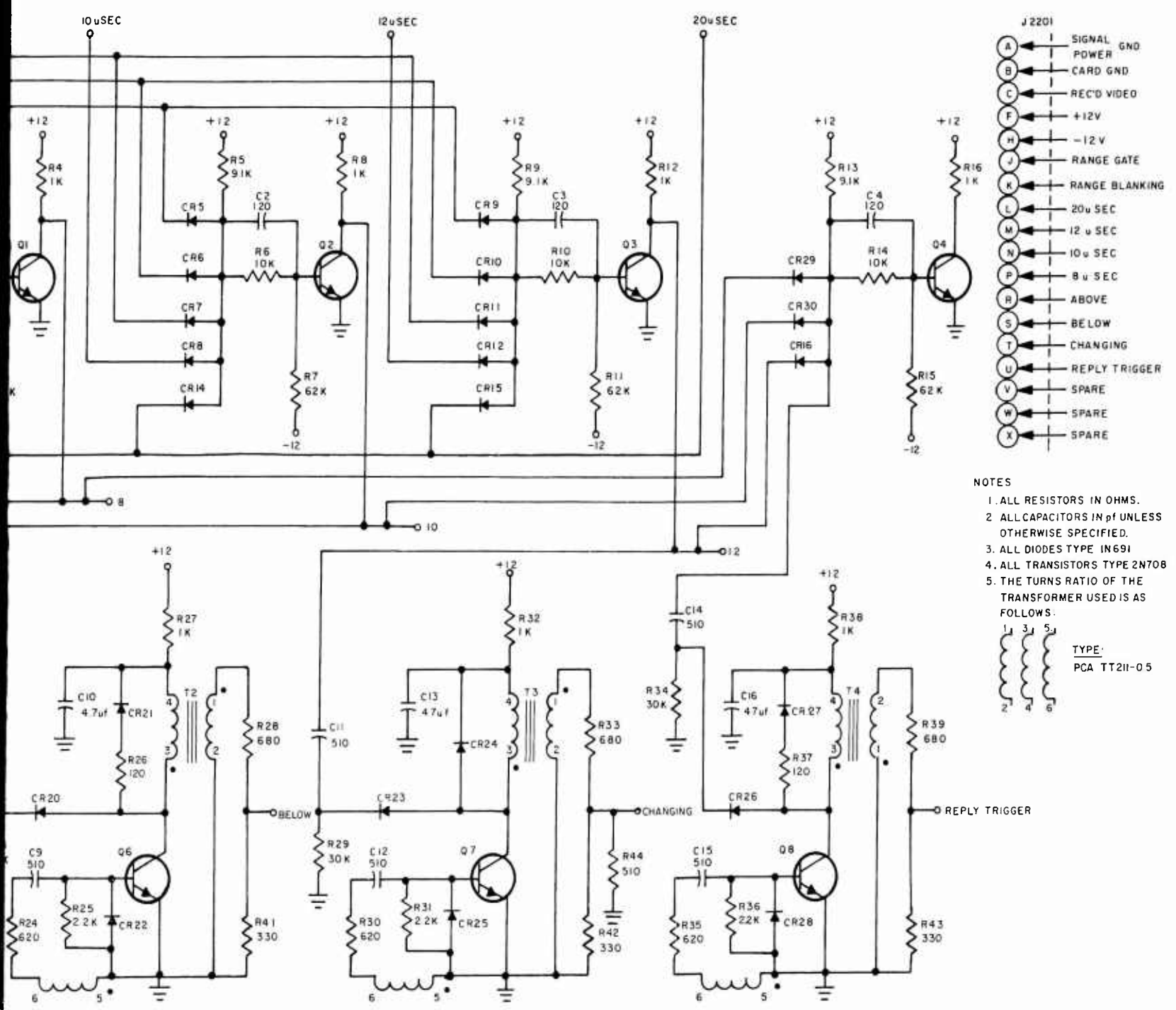
- Q₁ Q₄ ——— Q₉ ——— 2N1104 OR 2N338
- Q₂ ——— 2N708
- Q₃ ——— 2N699

3

FIGURE 5-19
 DECODER DELAY LINE AND DRIVER (INTERROGATOR-
 TRANSPONDER) (2100 AND 4100)



1



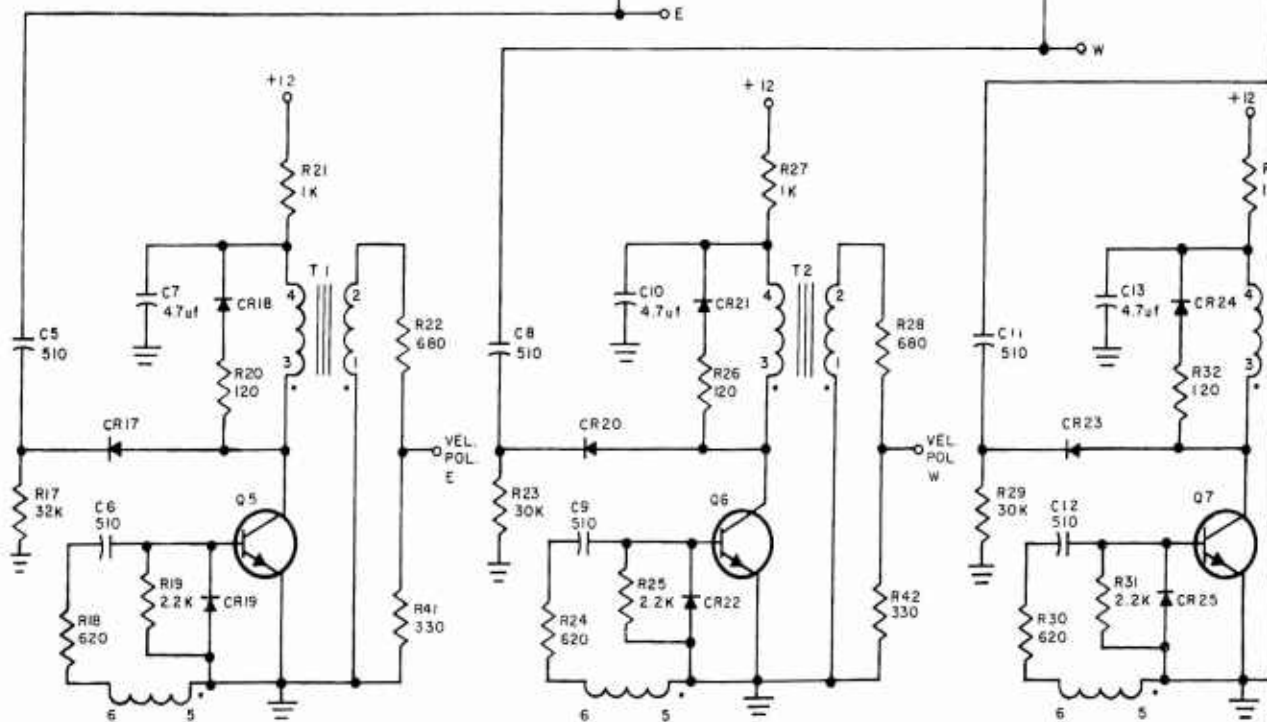
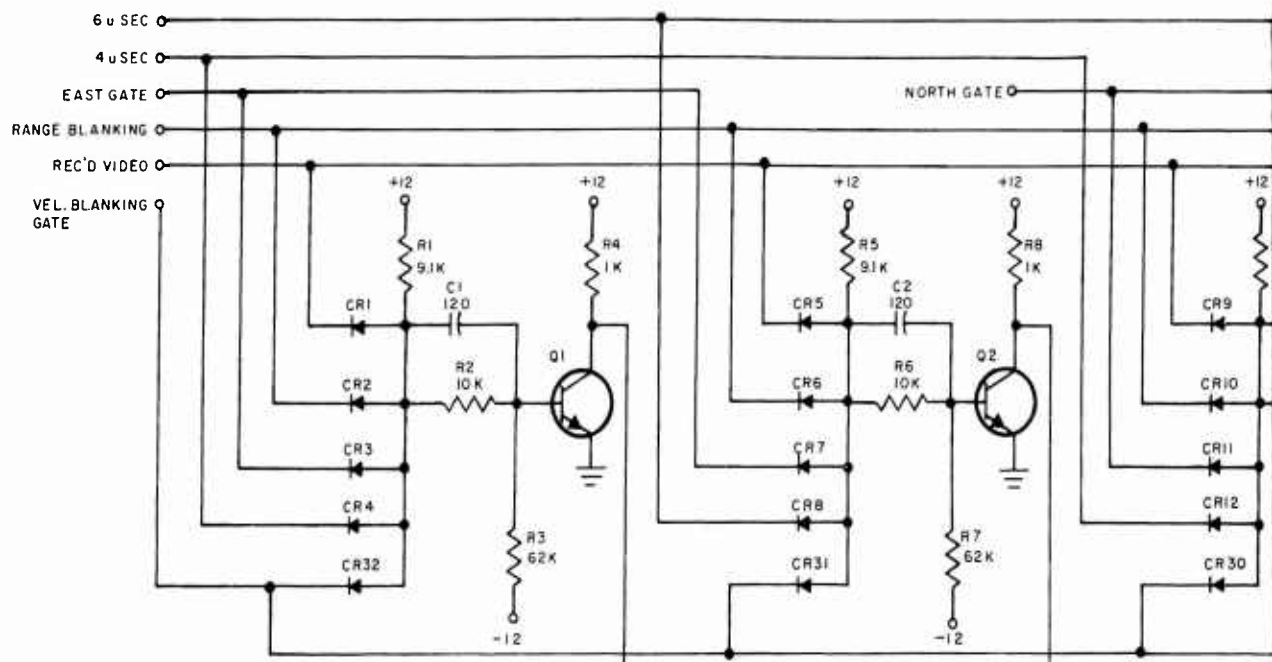
J 2201

A	SIGNAL
B	POWER GND
C	CARD GND
D	REC'D VIDEO
E	+12V
F	-12V
G	RANGE GATE
H	RANGE BLANKING
I	20μ SEC
J	12 μ SEC
K	10 μ SEC
L	8 μ SEC
M	ABOVE
N	BELOW
O	CHANGING
P	REPLY TRIGGER
Q	SPARE
R	SPARE
S	SPARE
T	SPARE
U	SPARE
V	SPARE
W	SPARE
X	SPARE

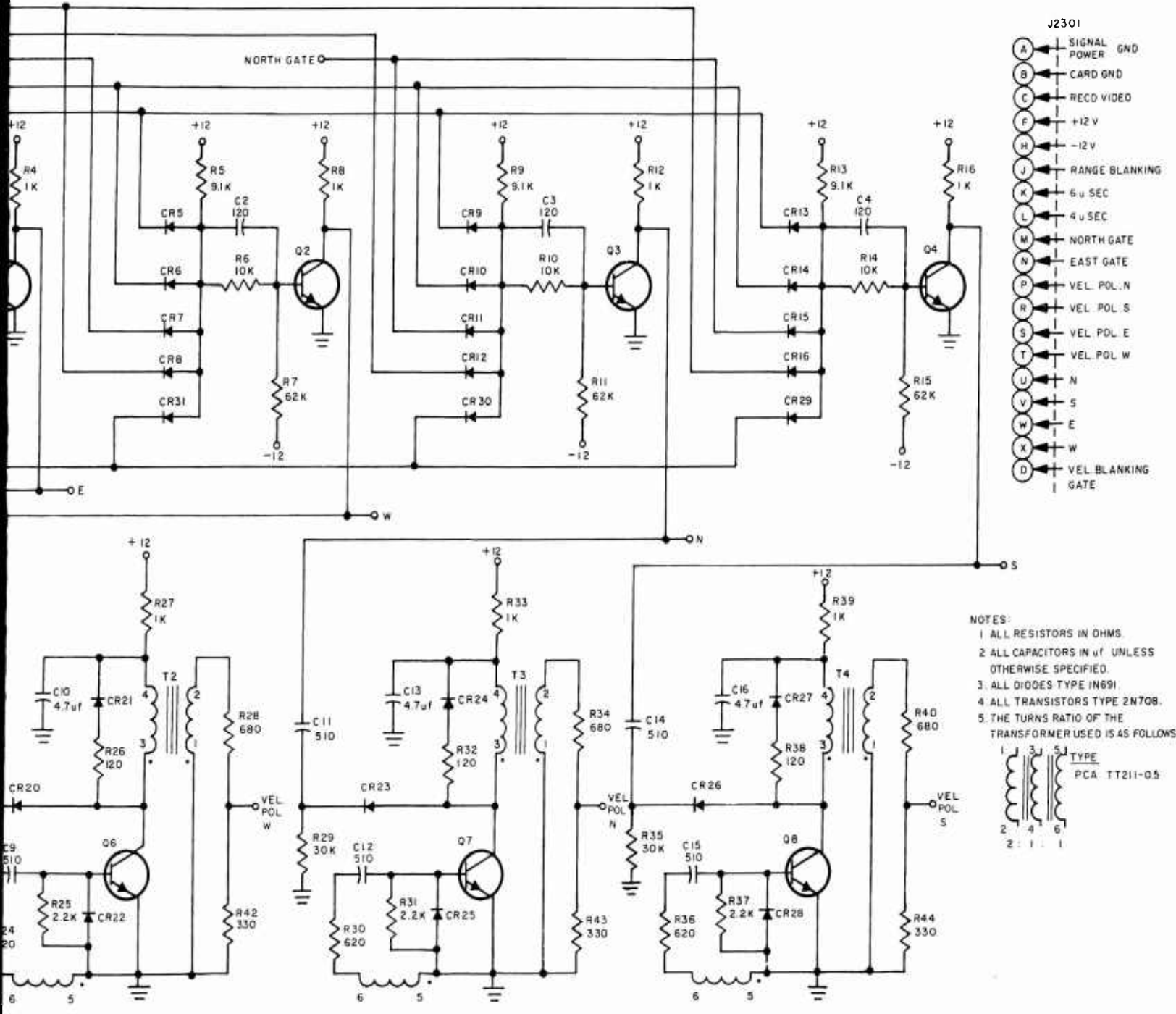
- NOTES
1. ALL RESISTORS IN OHMS.
 2. ALL CAPACITORS IN pf UNLESS OTHERWISE SPECIFIED.
 3. ALL DIODES TYPE IN691
 4. ALL TRANSISTORS TYPE 2N708
 5. THE TURNS RATIO OF THE TRANSFORMER USED IS AS FOLLOWS:



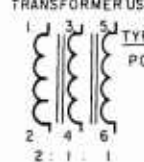
FIGURE 5-20.
RELATIVE ALTITUDE VELOCITY SCALE DECODER (2200)



1

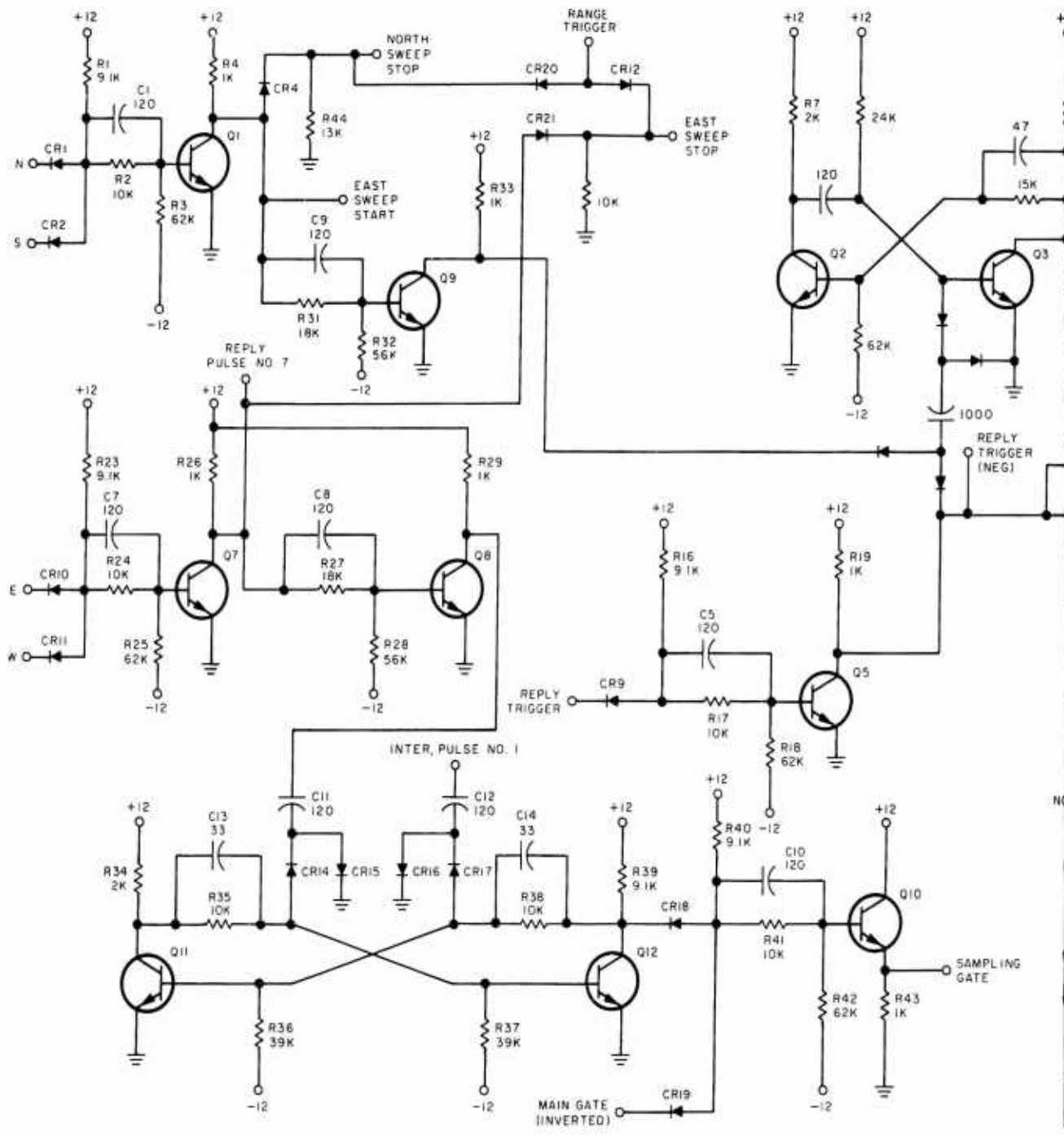


- NOTES:
- 1 ALL RESISTORS IN OHMS.
 - 2 ALL CAPACITORS IN μ F UNLESS OTHERWISE SPECIFIED.
 - 3 ALL DIODES TYPE IN691.
 - 4 ALL TRANSISTORS TYPE 2N708.
 - 5 THE TURNS RATIO OF THE TRANSFORMER USED IS AS FOLLOWS

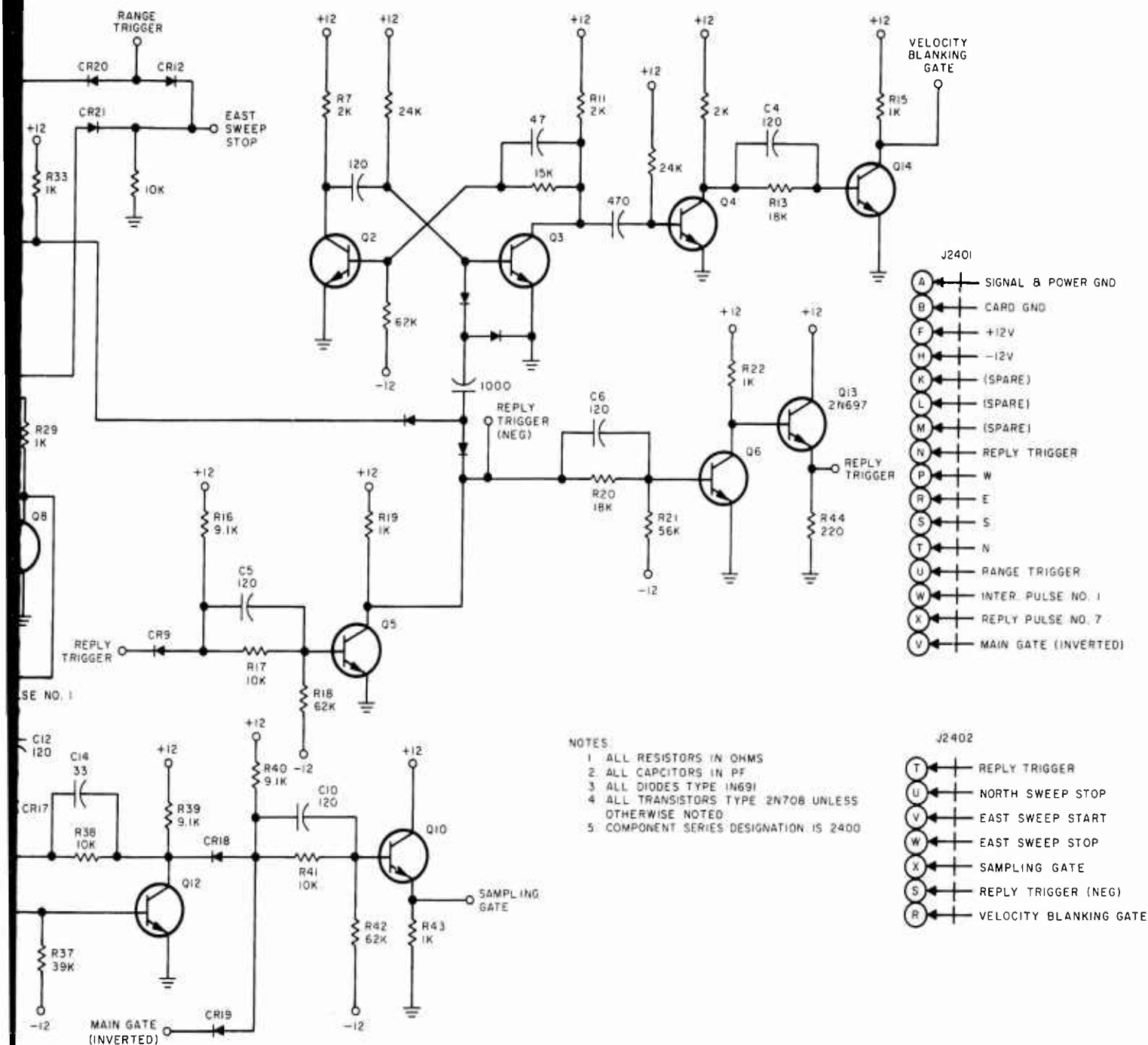


2

FIGURE 5-21
VELOCITY POLARITY DECODER (2300)

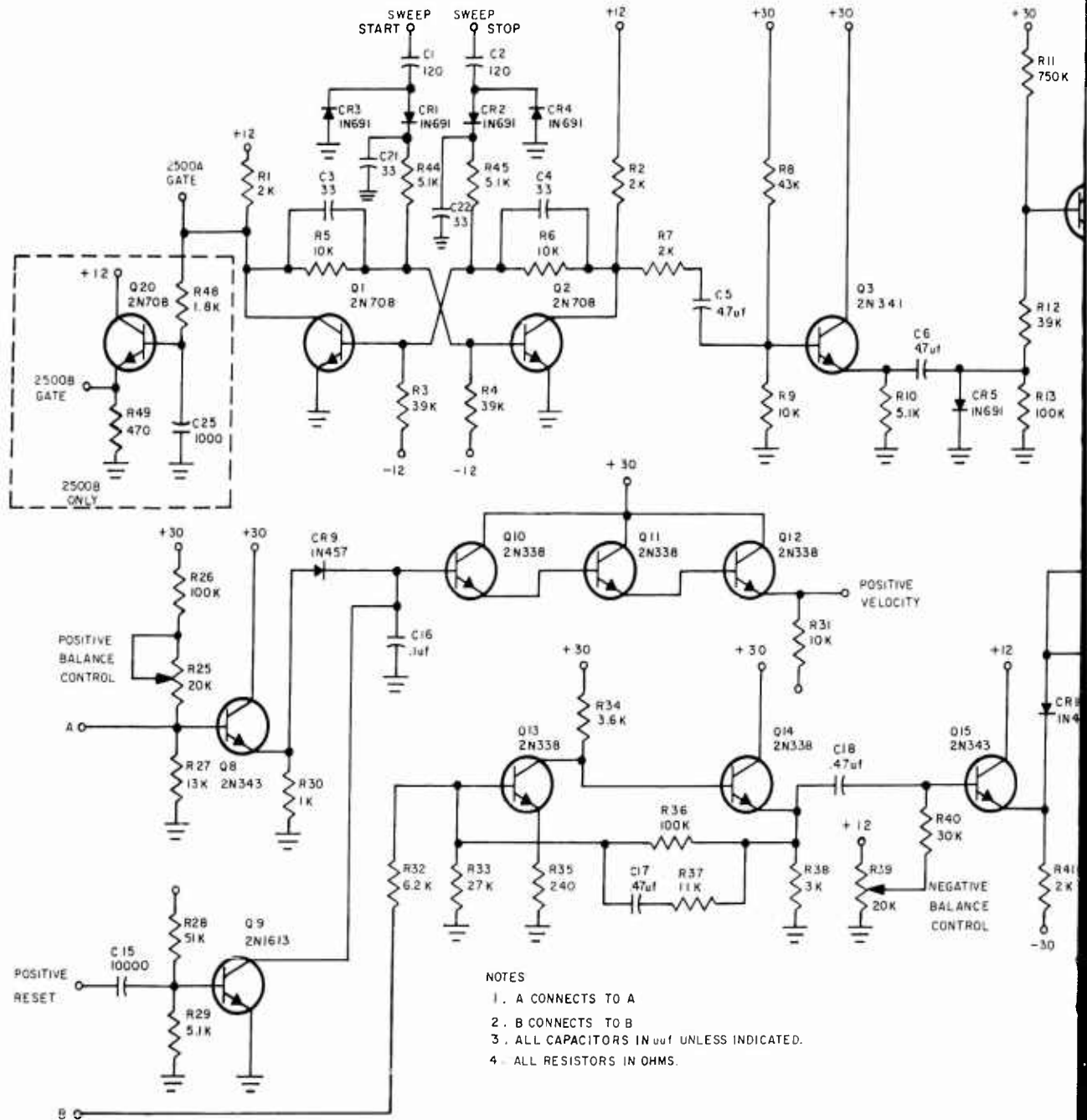


1

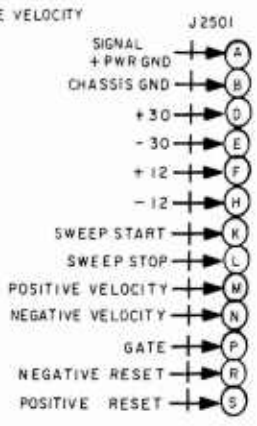
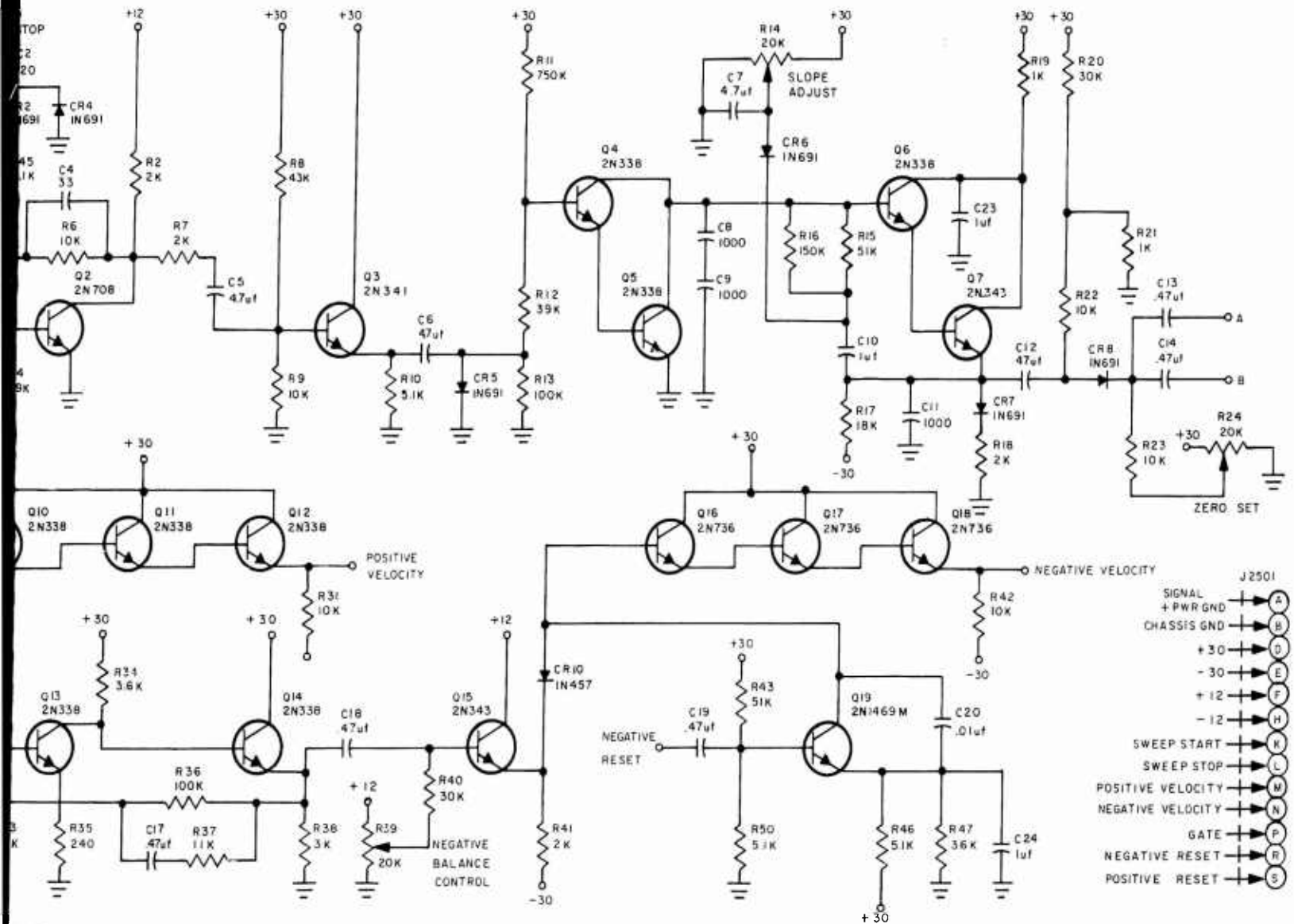


2

FIGURE 5 22
PULSE SELECTOR (2400)



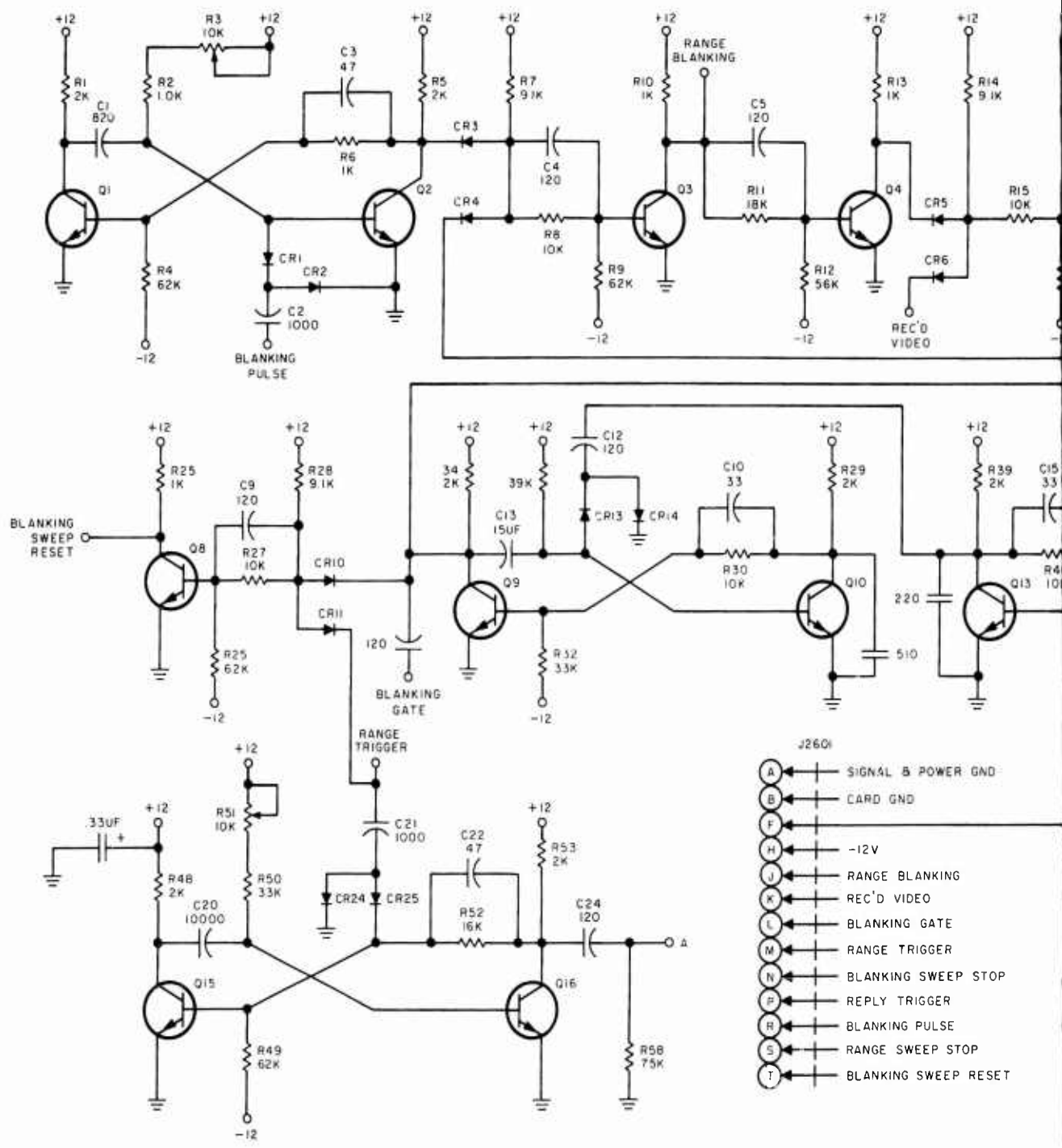
1



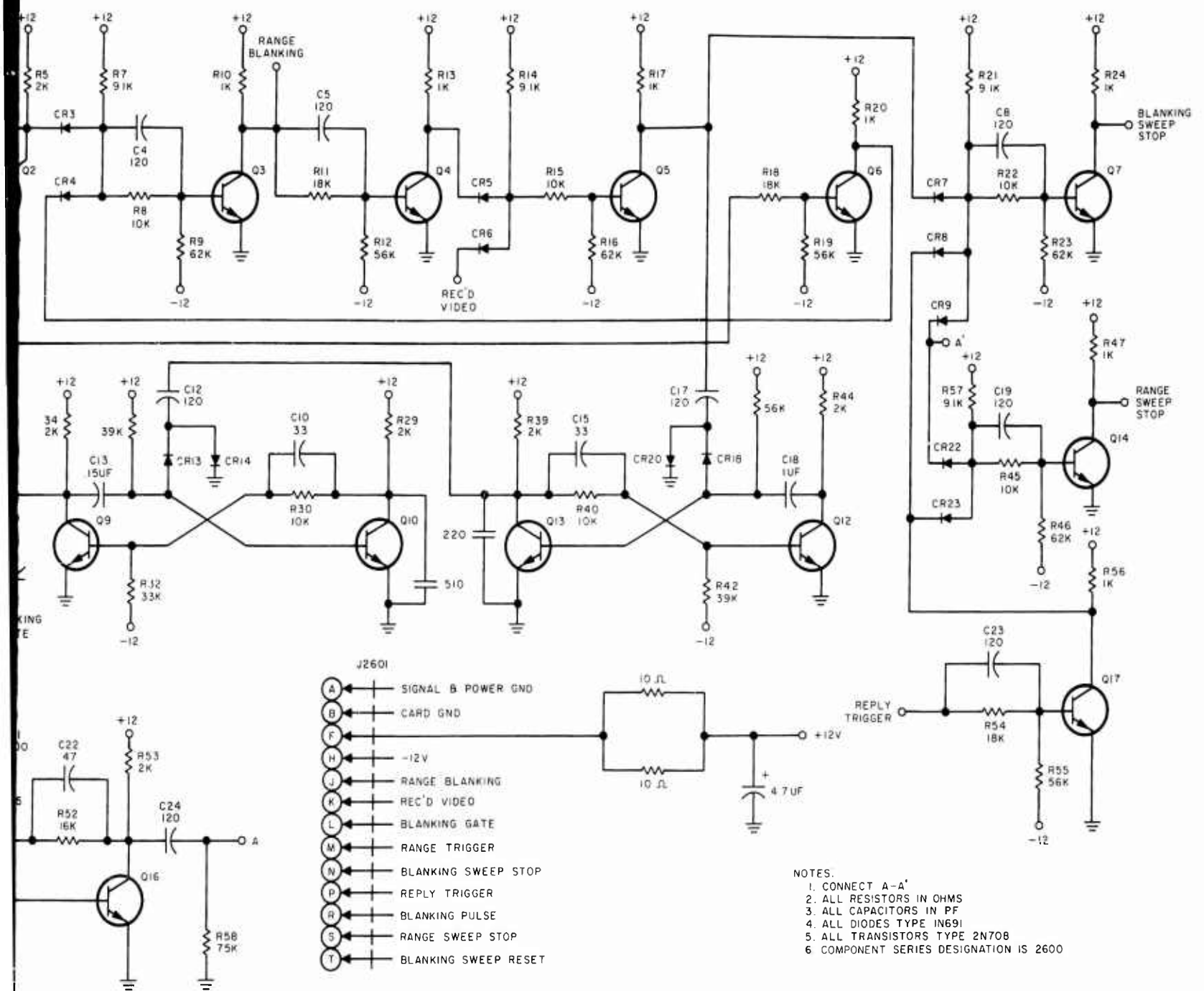
- NOTES
1. A CONNECTS TO A
 2. B CONNECTS TO B
 3. ALL CAPACITORS IN μf UNLESS INDICATED.
 4. ALL RESISTORS IN OHMS.

2

FIGURE 5-23
NORTH EAST VELOCITY DECODER (2500)



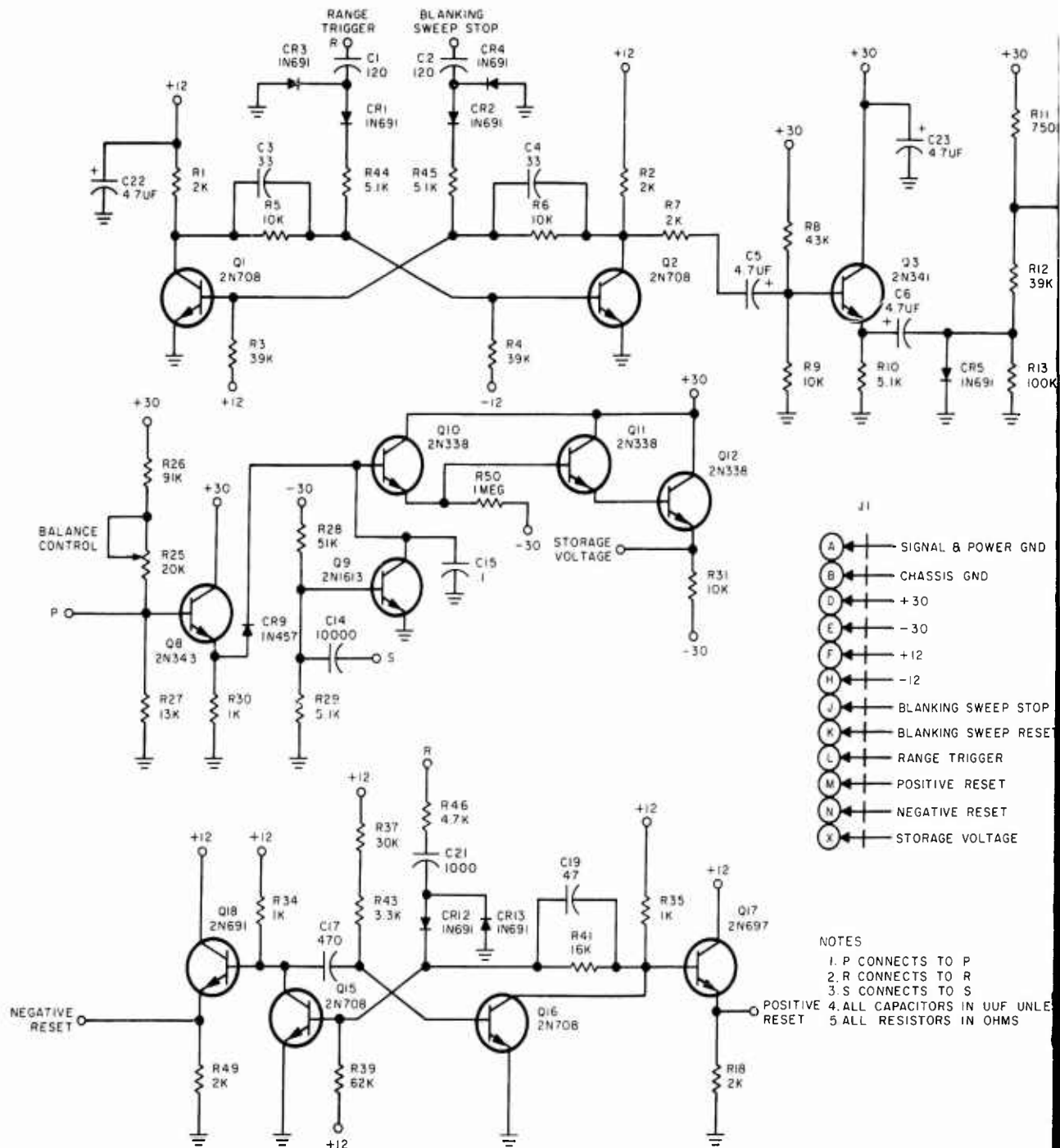
1



- NOTES.
1. CONNECT A-A'
 2. ALL RESISTORS IN OHMS
 3. ALL CAPACITORS IN PF
 4. ALL DIODES TYPE IN691
 5. ALL TRANSISTORS TYPE 2N708
 6. COMPONENT SERIES DESIGNATION IS 2600

2

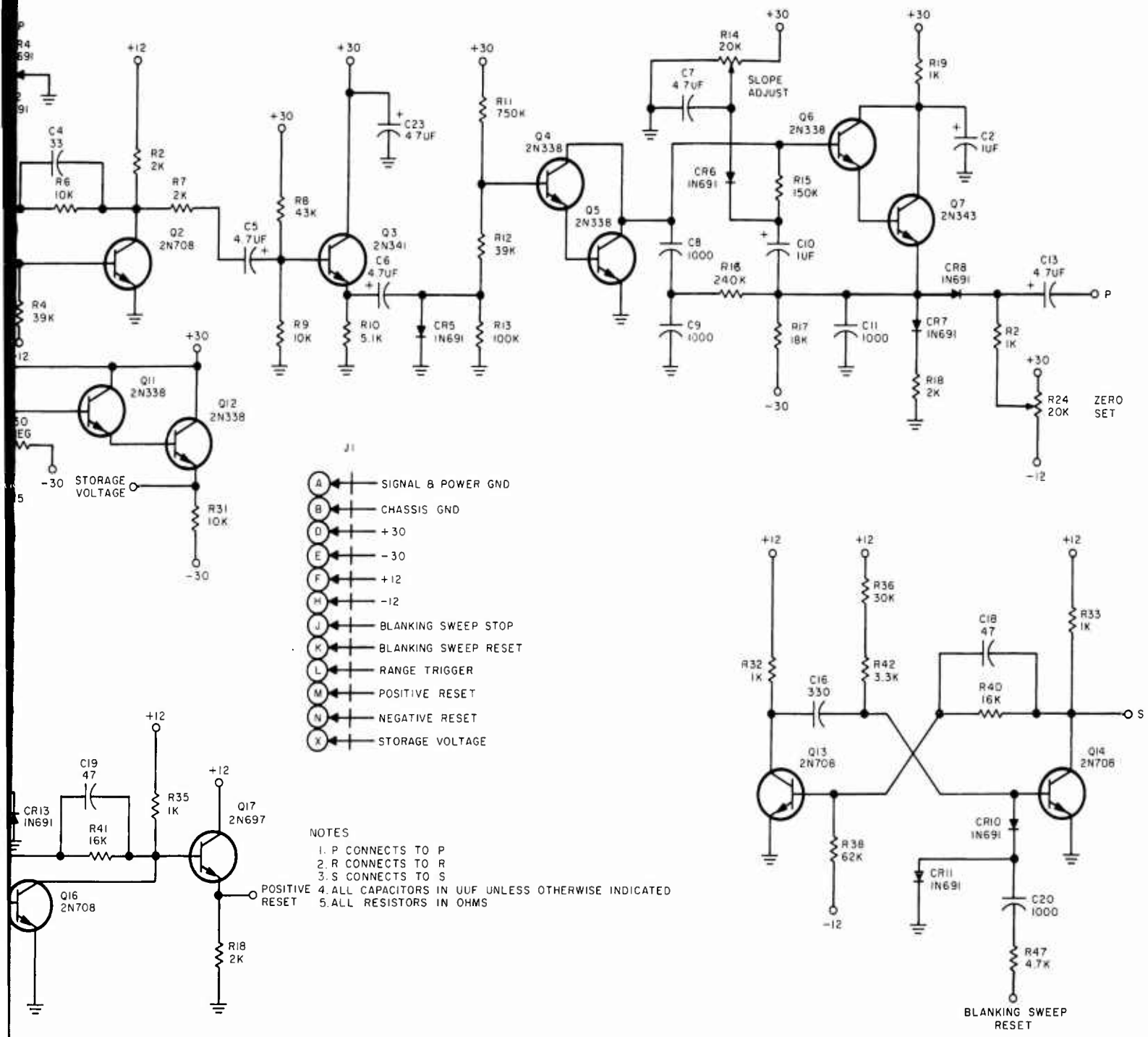
FIGURE 5-24
BLANKING LOGIC (2600)



- J1
- A — SIGNAL & POWER GND
 - B — CHASSIS GND
 - D — +30
 - E — -30
 - F — +12
 - H — -12
 - J — BLANKING SWEEP STOP
 - K — BLANKING SWEEP RESET
 - L — RANGE TRIGGER
 - M — POSITIVE RESET
 - N — NEGATIVE RESET
 - X — STORAGE VOLTAGE

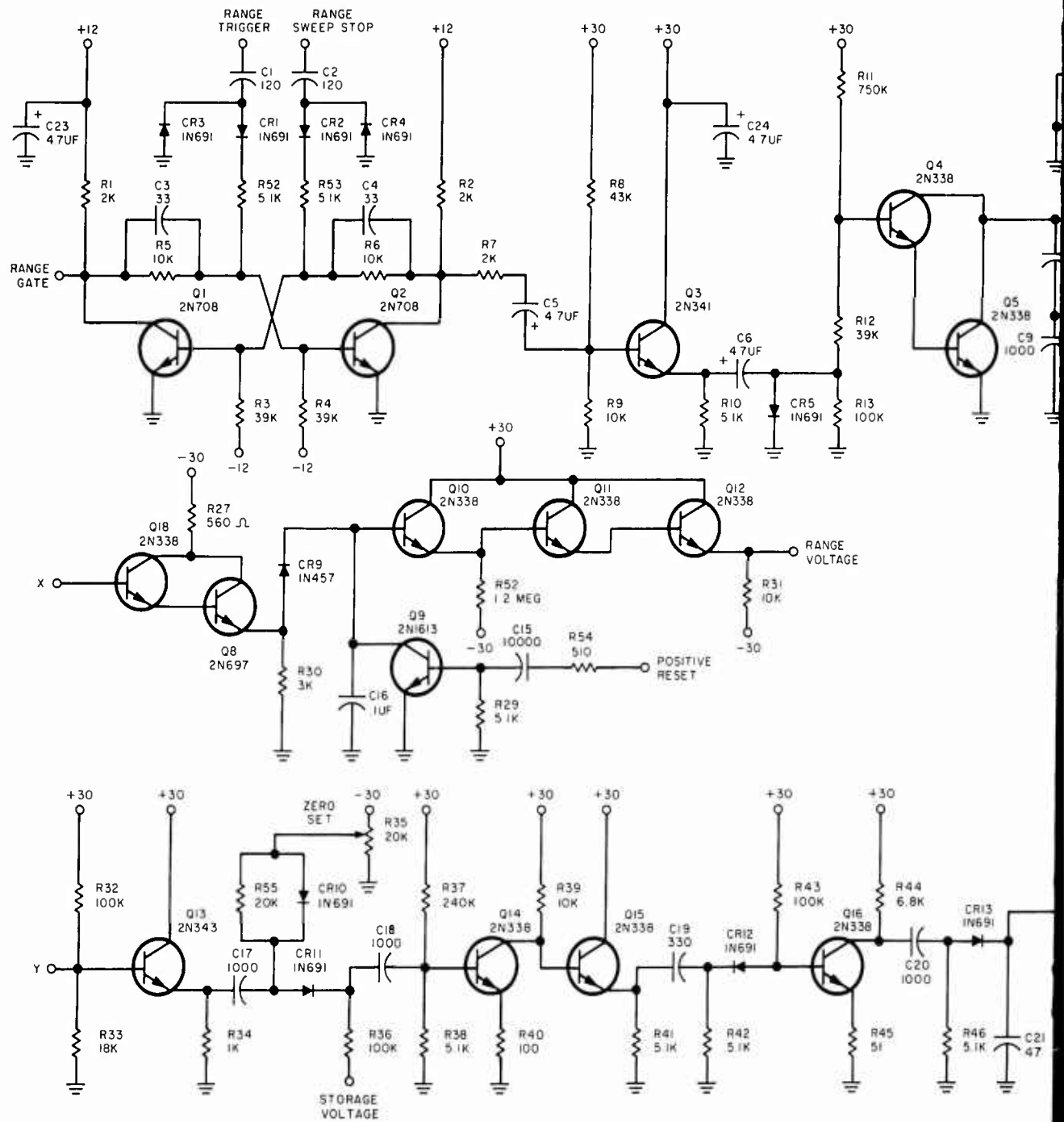
- NOTES
1. P CONNECTS TO P
 2. R CONNECTS TO R
 3. S CONNECTS TO S
 4. ALL CAPACITORS IN UUF UNLESS OTHERWISE SPECIFIED
 5. ALL RESISTORS IN OHMS



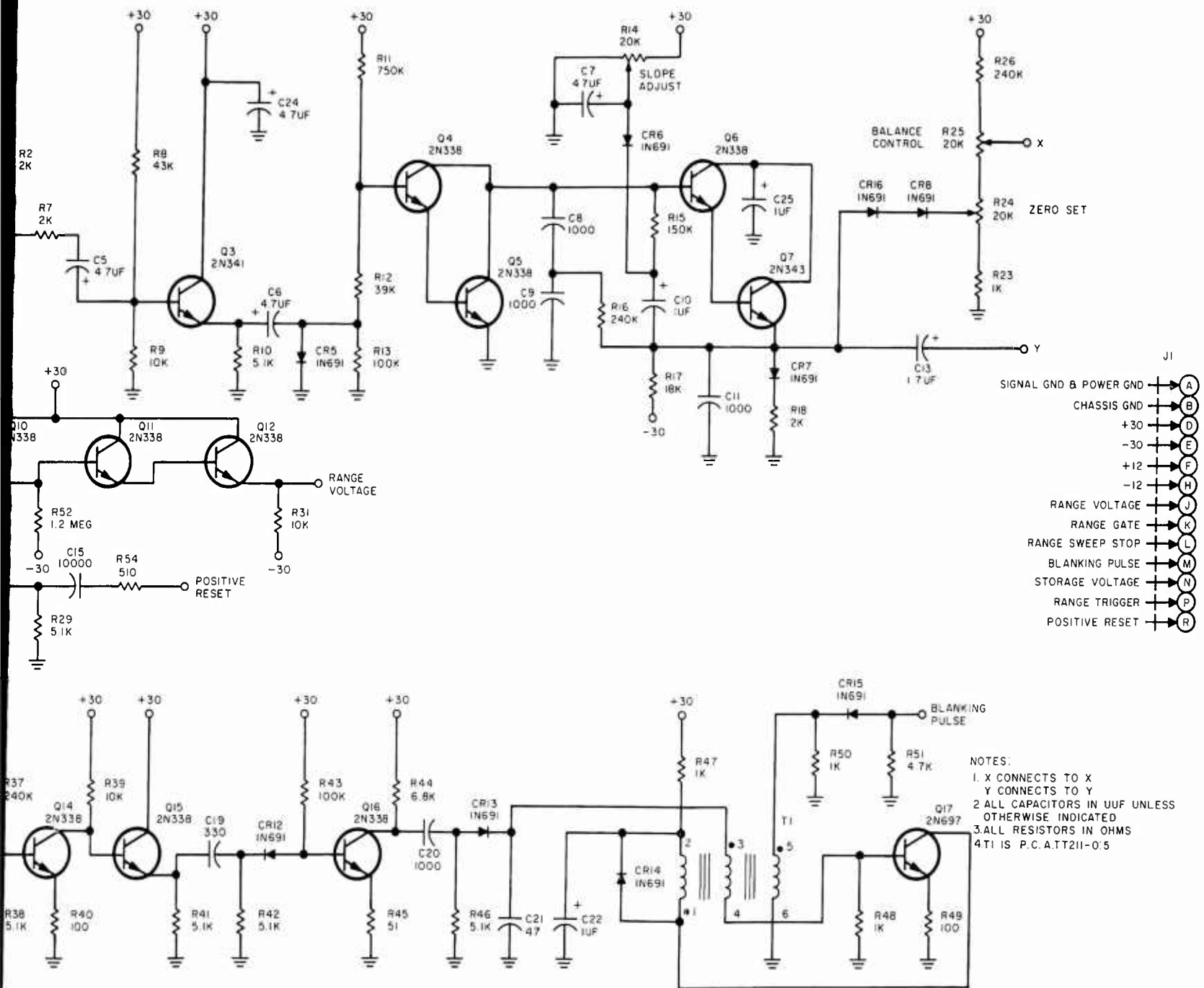


2

FIGURE 5-25
BLANKING SWEEP GENERATOR (2700)



1



NOTES:
 1. X CONNECTS TO X
 Y CONNECTS TO Y
 2. ALL CAPACITORS IN UUF UNLESS OTHERWISE INDICATED
 3. ALL RESISTORS IN OHMS
 4. T1 IS P.C.ATT211-0.5

2

FIGURE 5-26
 RANGE SWEEP GENERATOR (2800)

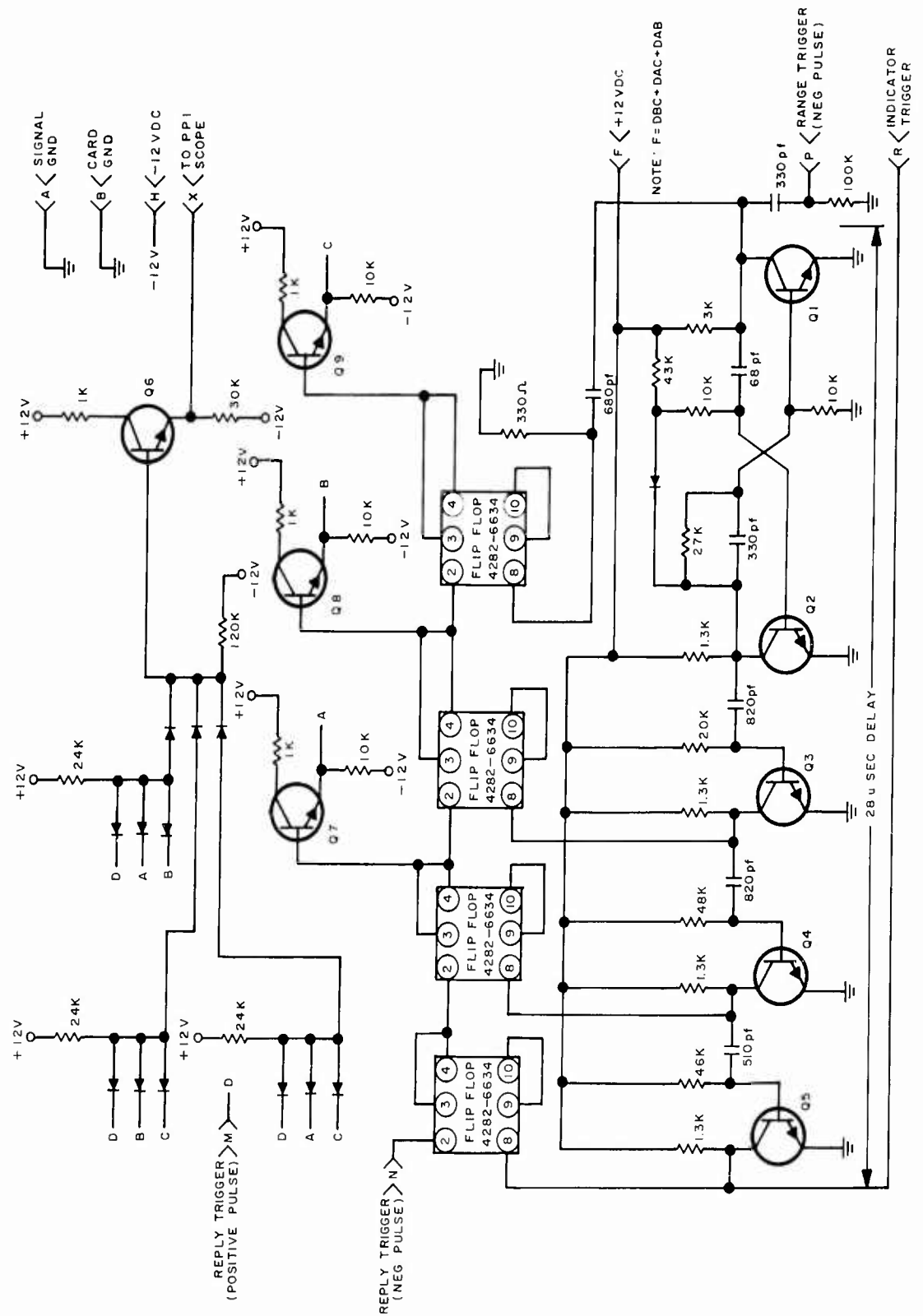
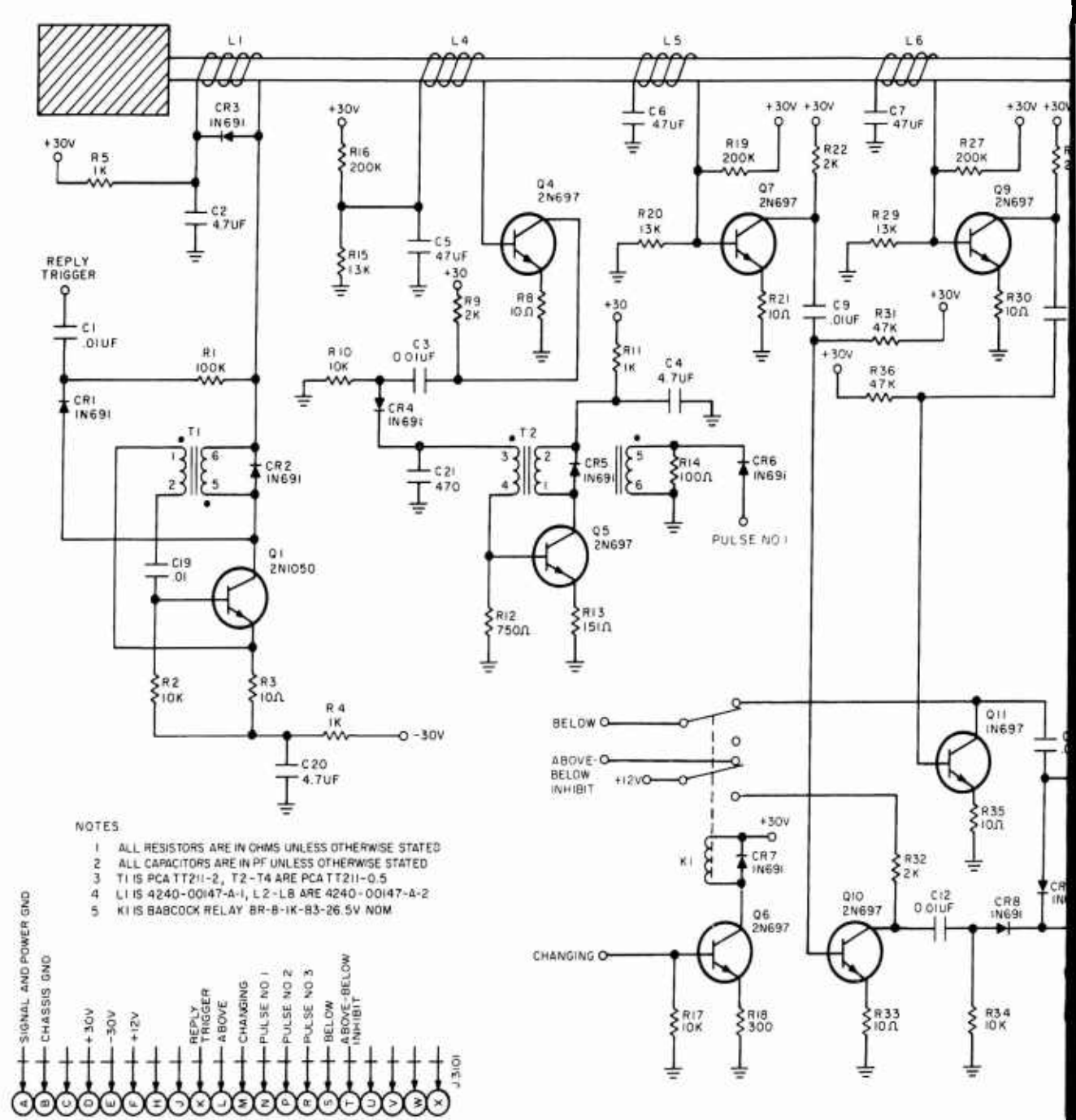
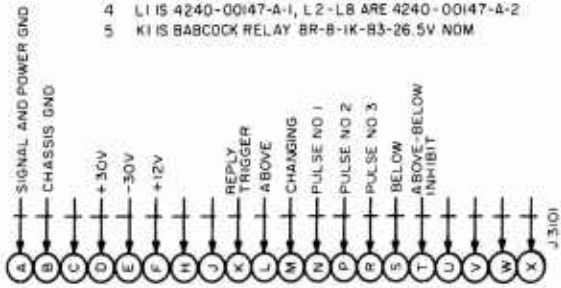


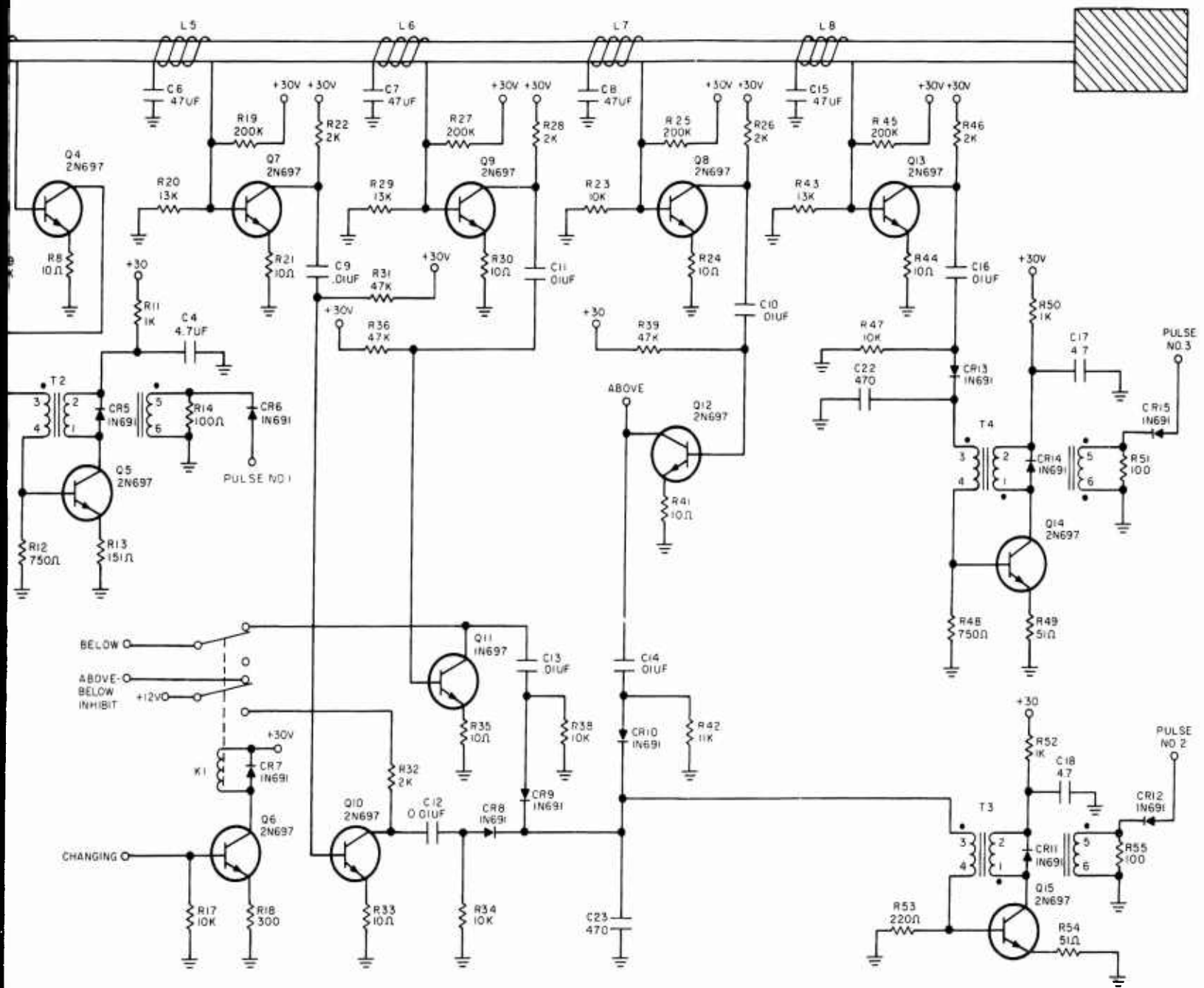
FIGURE 5 27. PWI DISPLAY LOGIC (2900)



- NOTES
- 1 ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED
 - 2 ALL CAPACITORS ARE IN PF UNLESS OTHERWISE STATED
 - 3 T1 IS PCA TT211-2, T2-T4 ARE PCA TT211-0.5
 - 4 L1 IS 4240-00147-A-1, L2-L6 ARE 4240-00147-A-2
 - 5 K1 IS BABCOCK RELAY BR-B-1K-B3-26.5V NDM

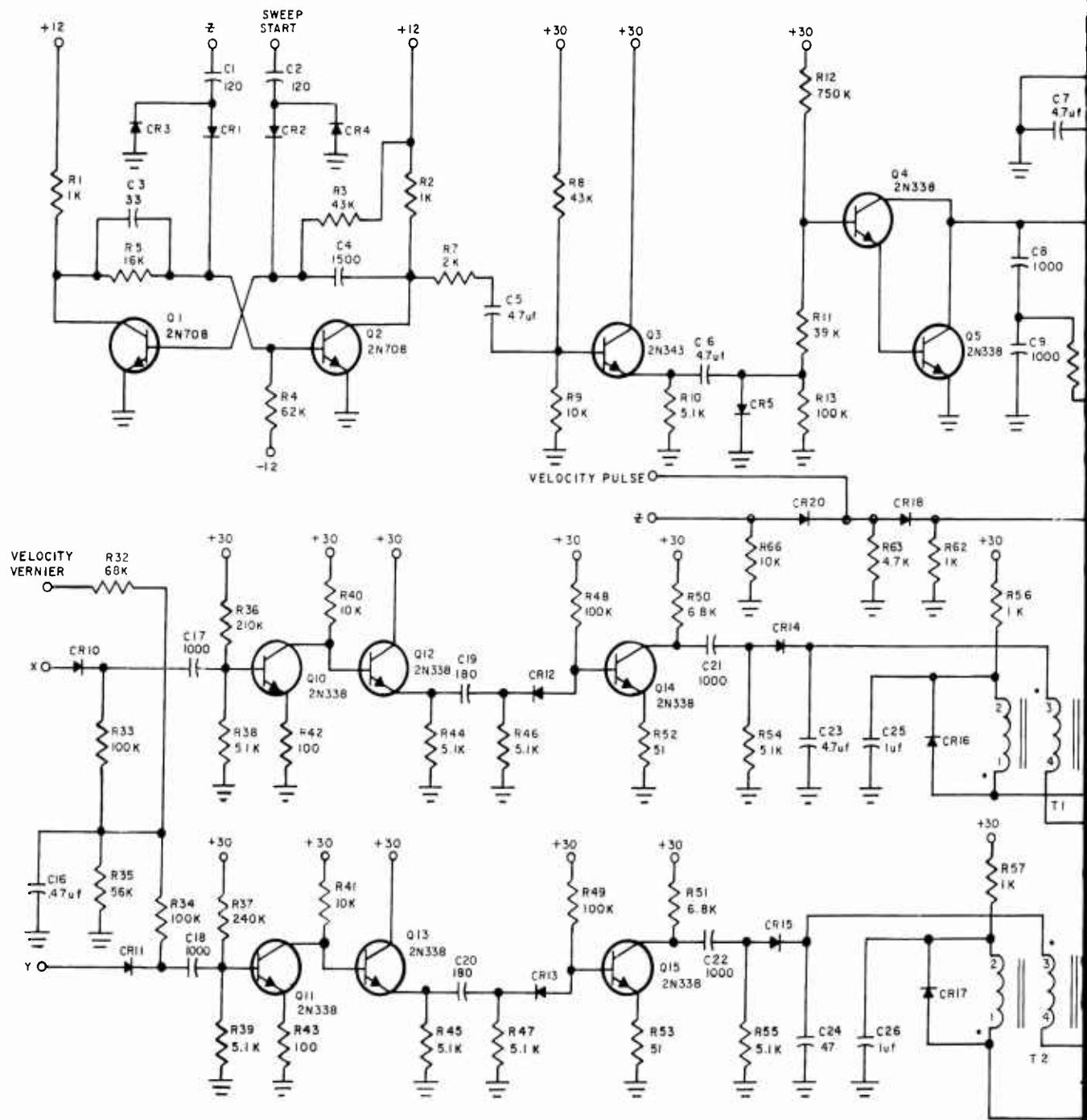


1

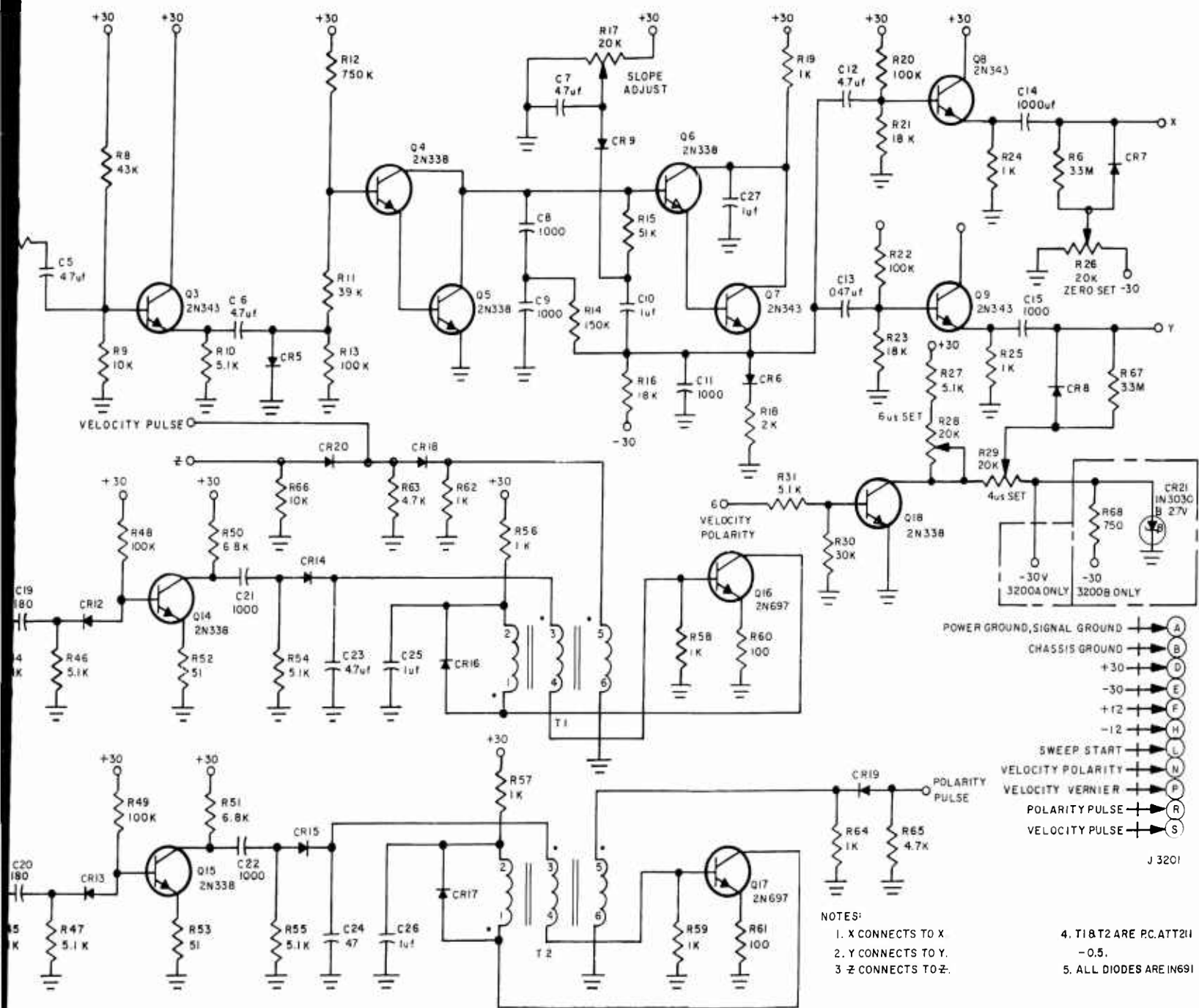


2

FIGURE 5-20
TRANSPONDER ENCODER DELAY SELECTOR (3100)



1

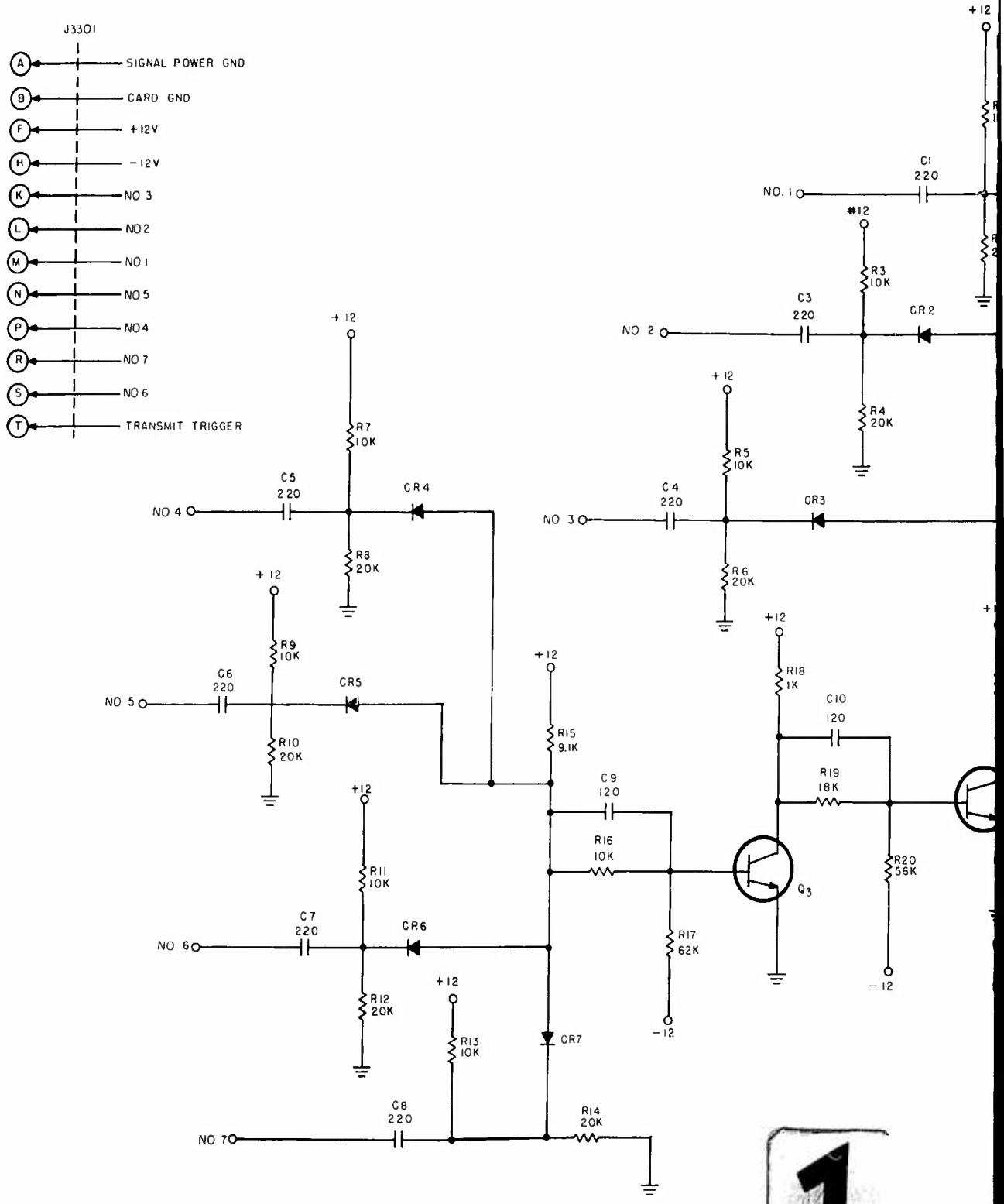


J 3201

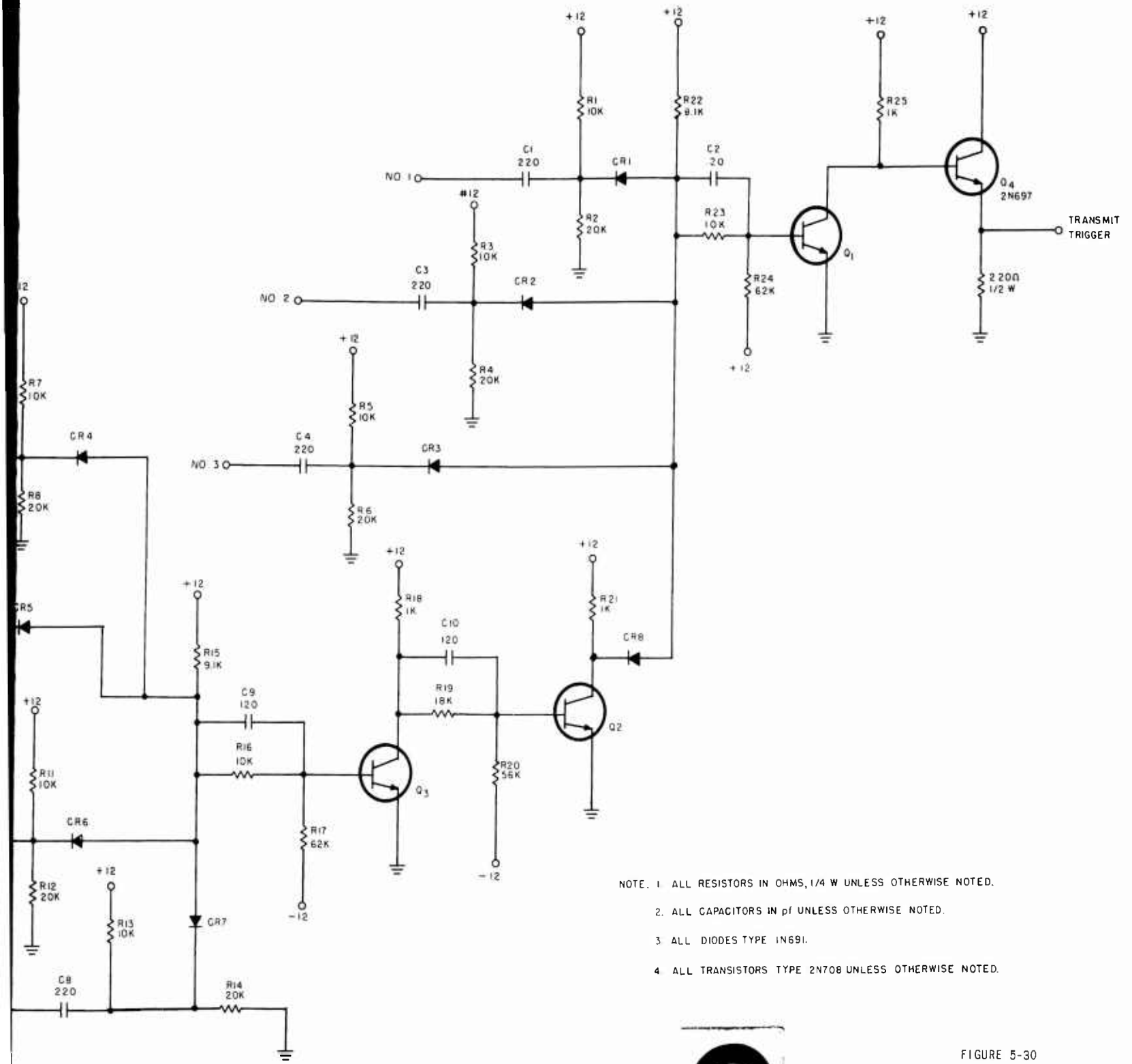
- NOTES:
1. X CONNECTS TO X.
 2. Y CONNECTS TO Y.
 3. Z CONNECTS TO Z.
 4. T1 & T2 ARE PC.ATT2H
-05.
 5. ALL DIODES ARE IN691

2

FIGURE 5-29
NORTH-EAST VELOCITY CODER (3200)



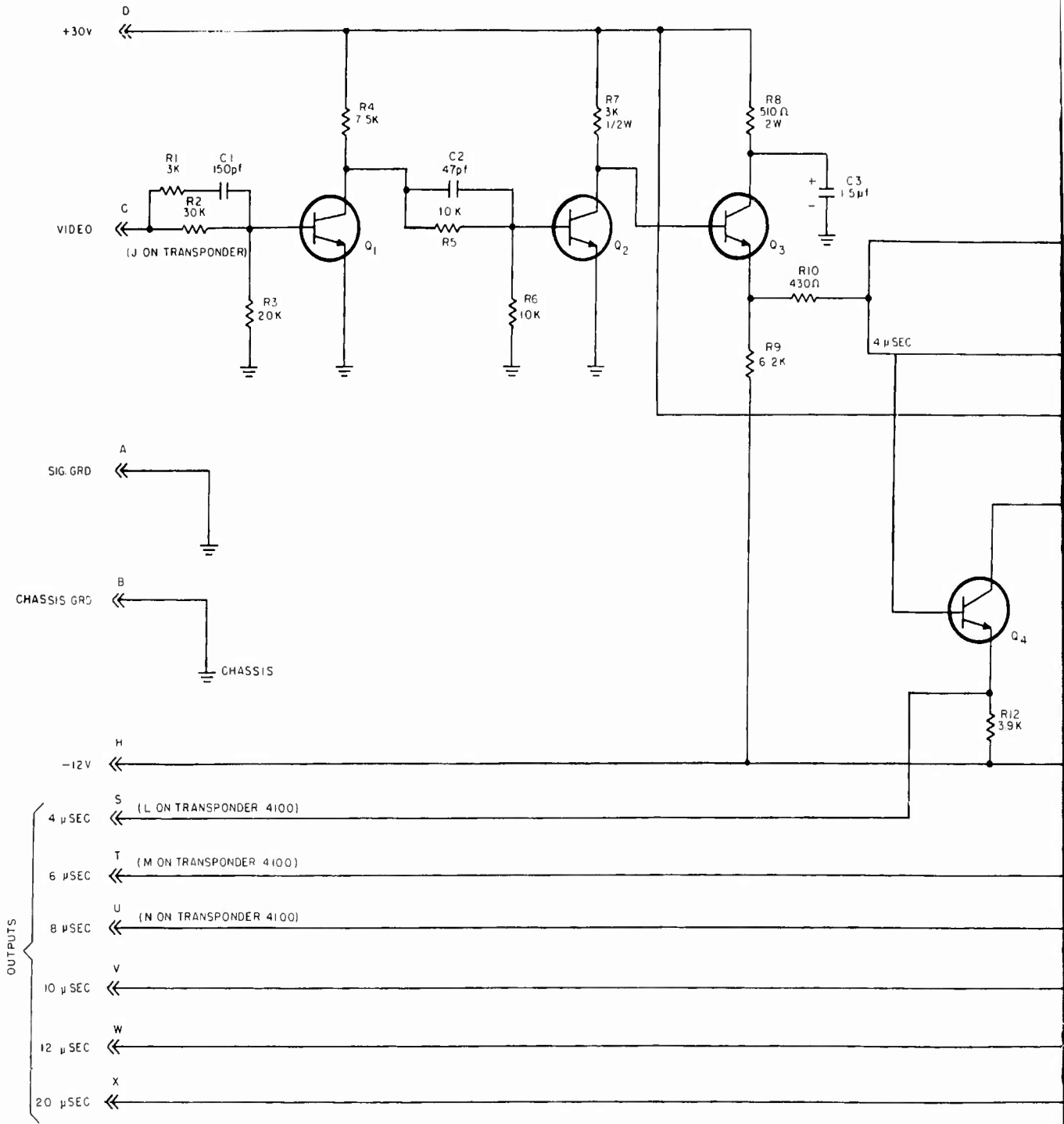
1



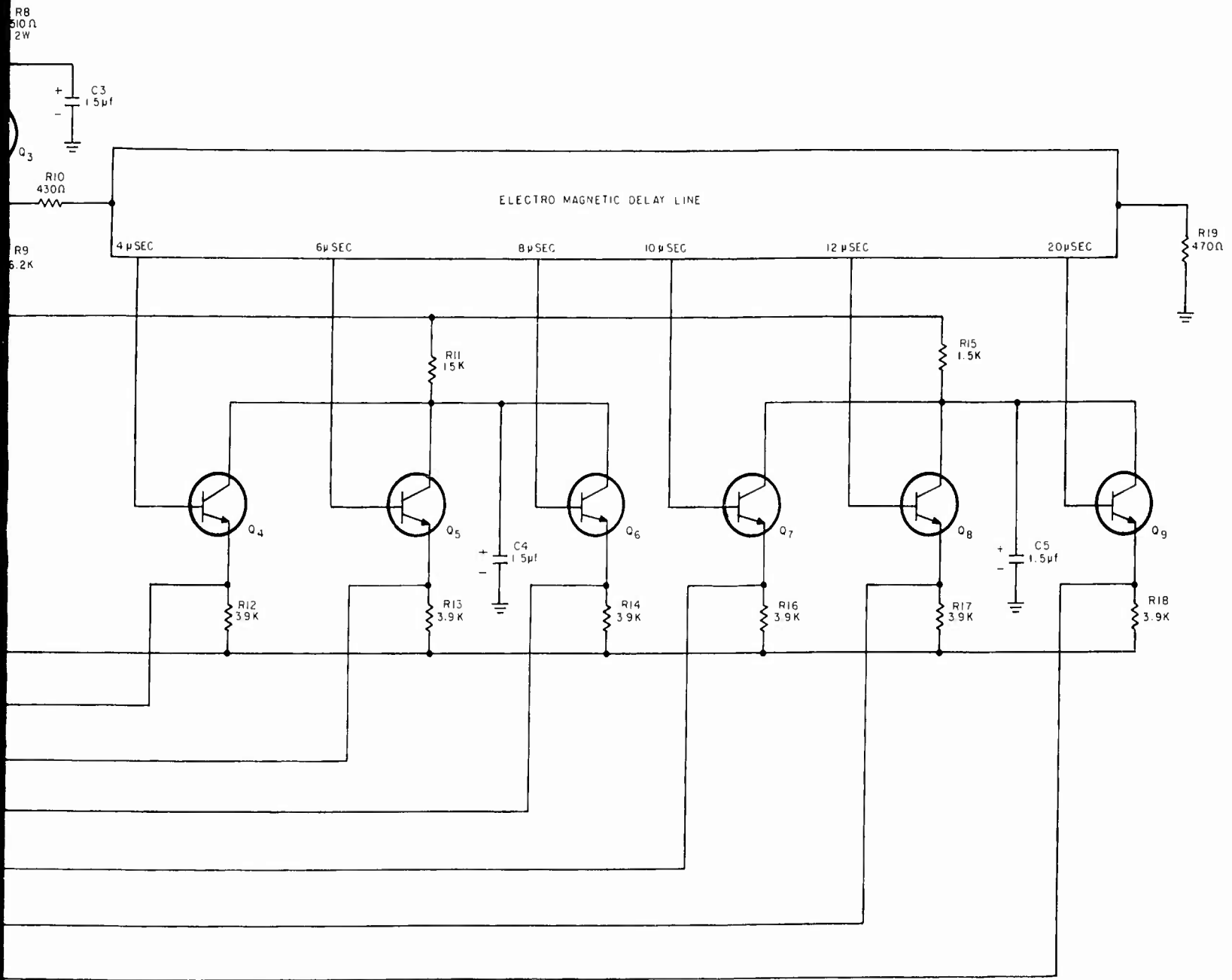
- NOTE. 1. ALL RESISTORS IN OHMS, 1/4 W UNLESS OTHERWISE NOTED.
 2. ALL CAPACITORS IN pF UNLESS OTHERWISE NOTED.
 3. ALL DIODES TYPE 1N691.
 4. ALL TRANSISTORS TYPE 2N708 UNLESS OTHERWISE NOTED.

2

FIGURE 5-30
 MIXER AMPLIFIER 3300 CAS SCHEMATIC



1

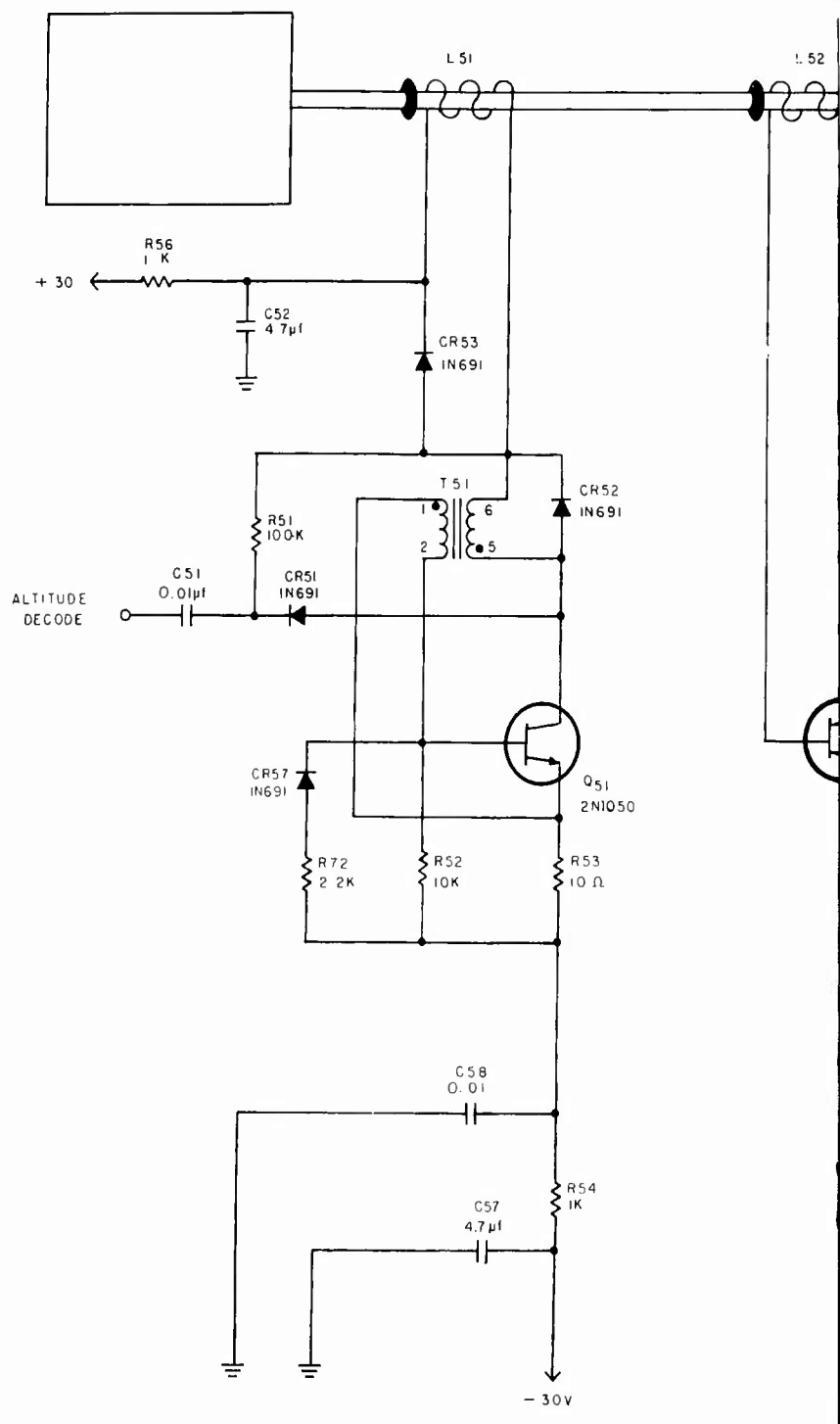
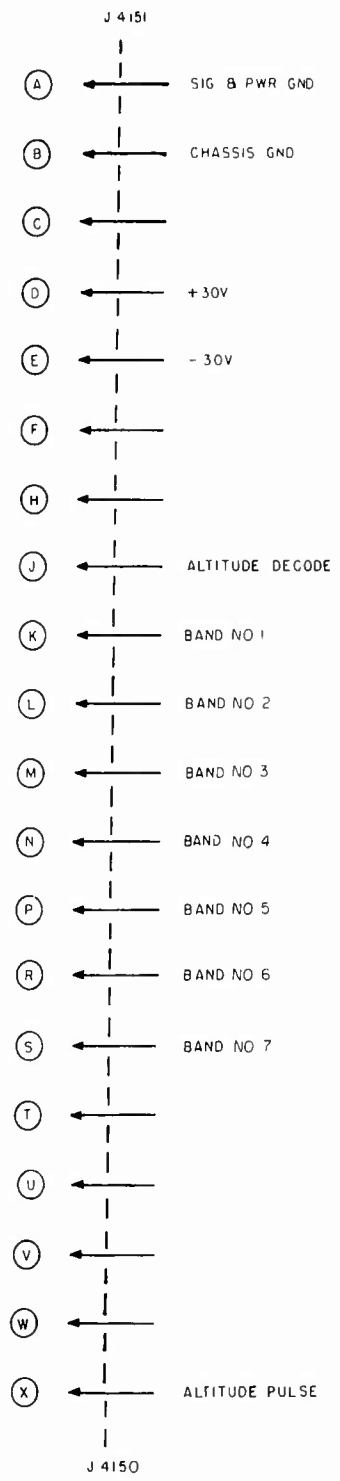


EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

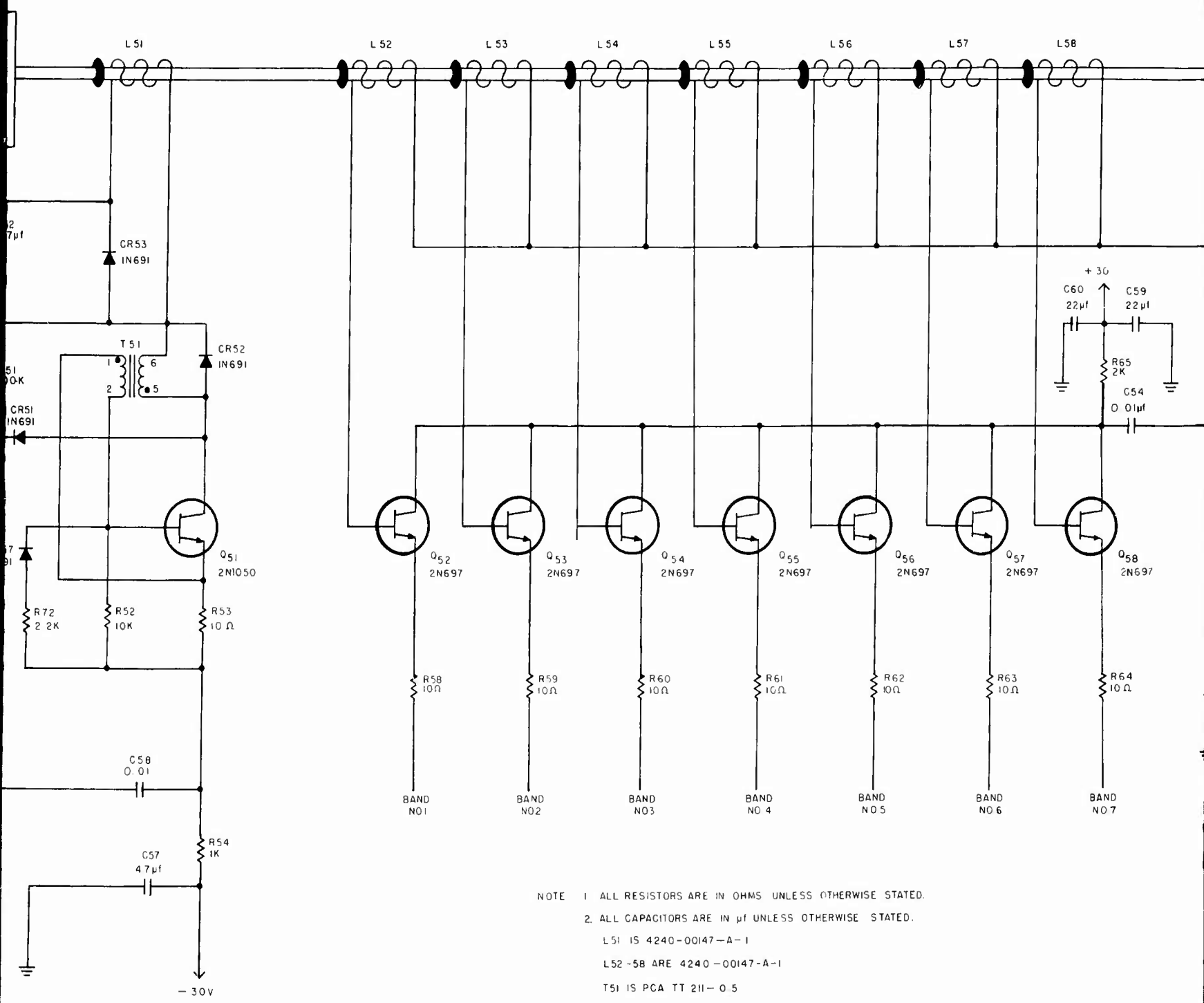
- Q₁ Q₄ — — — — — 2N1104 OR 2N338
- Q₂ — — — — — 2N708
- Q₃ — — — — — 2N699

3

FIGURE 5-31
TRANSPONDER DECODER DELAY SELECTOR NO. 1 (4100)

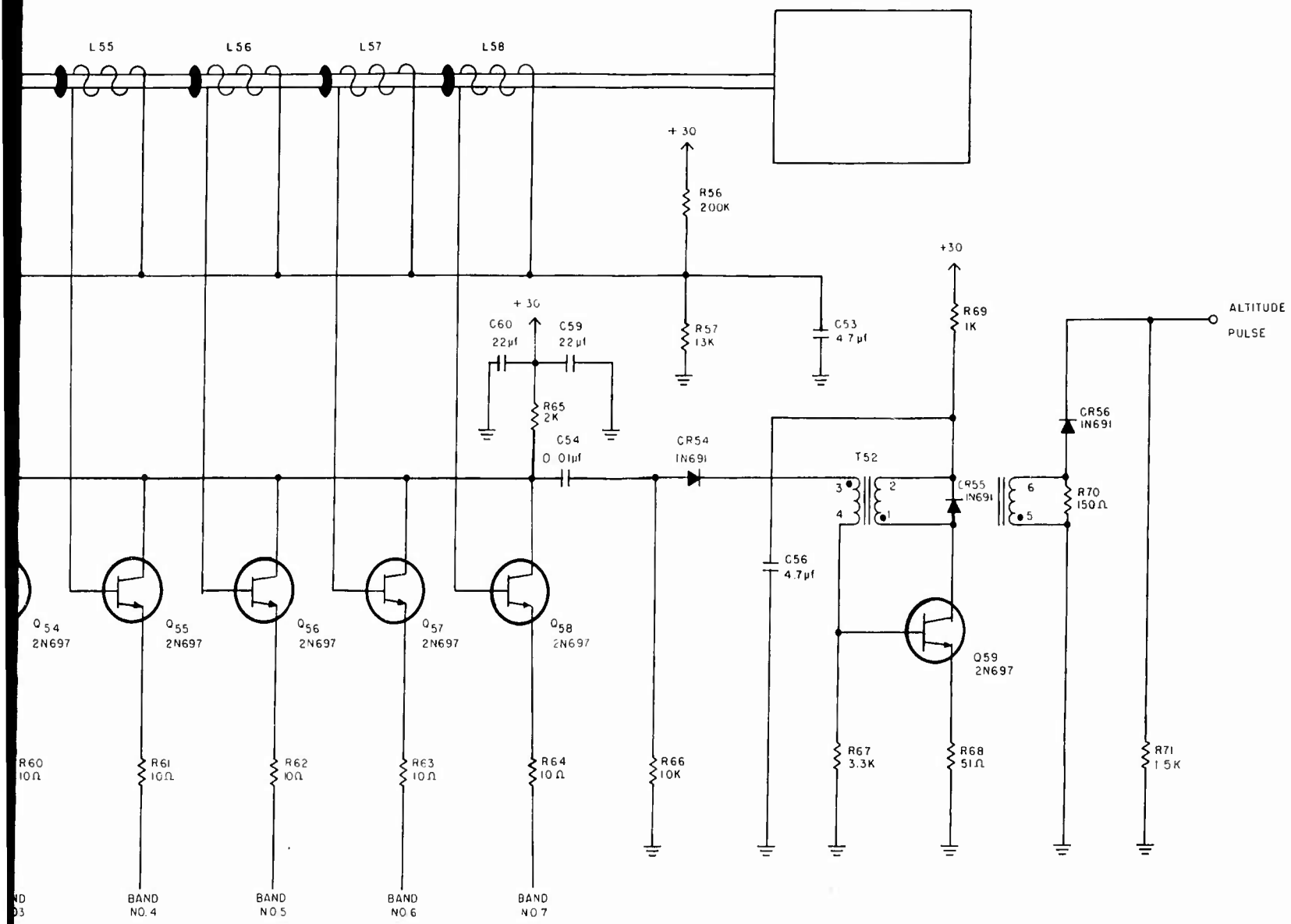


1



NOTE 1 ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED.
 2. ALL CAPACITORS ARE IN μf UNLESS OTHERWISE STATED.
 L51 IS 4240-00147-A-1
 L52-58 ARE 4240-00147-A-1
 T51 IS PCA TT 211-0.5
 T52 IS PCA TT 1111-1

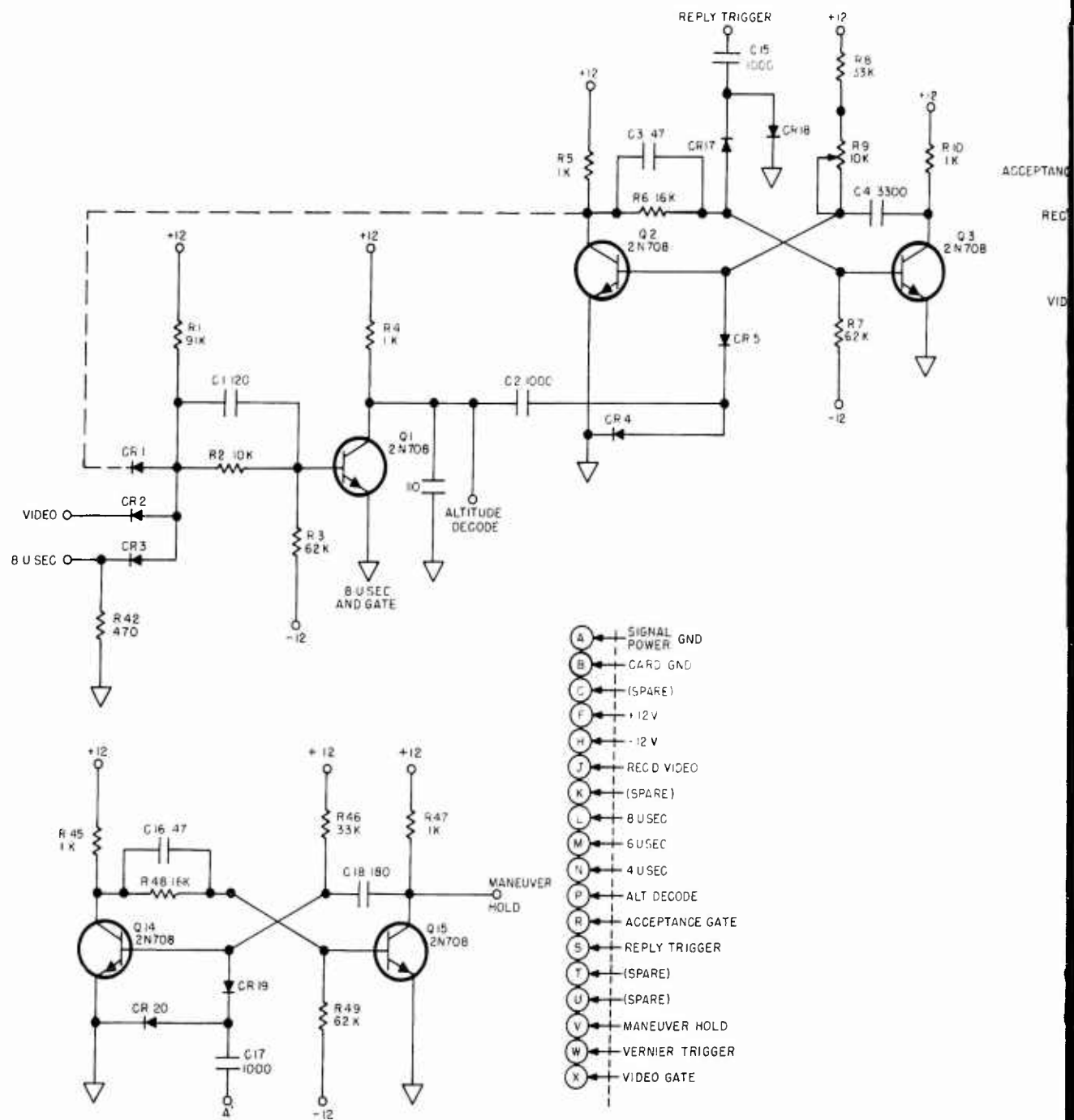
2



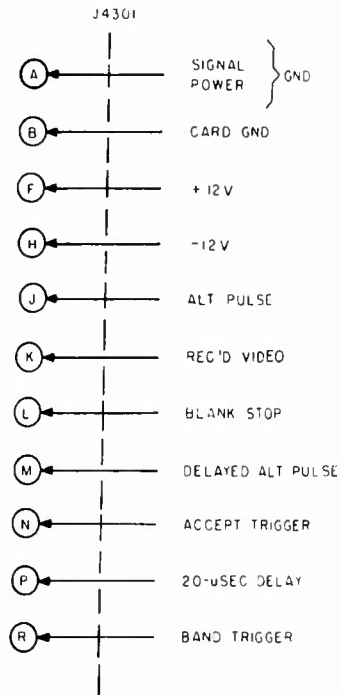
RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED.
 CAPACITORS ARE IN μf UNLESS OTHERWISE STATED.
 4240-00147-A-1
 PARTS ARE 4240-00147-A-1
 PCA TT 211-0.5
 PCA TT 111-1

3

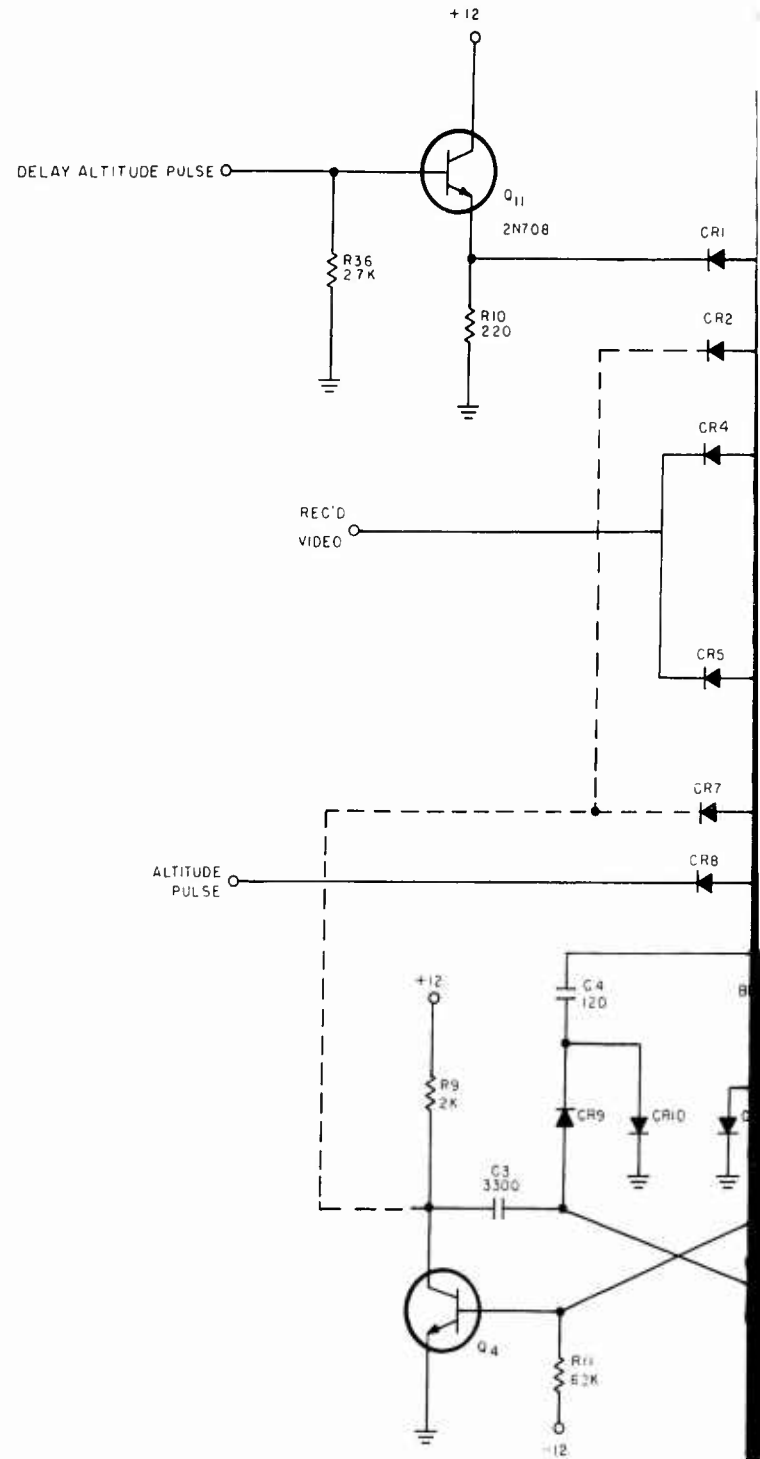
FIGURE 5-32.
 TRANSPONDER DECODER DELAY SELECTOR NO. 2 (4150)



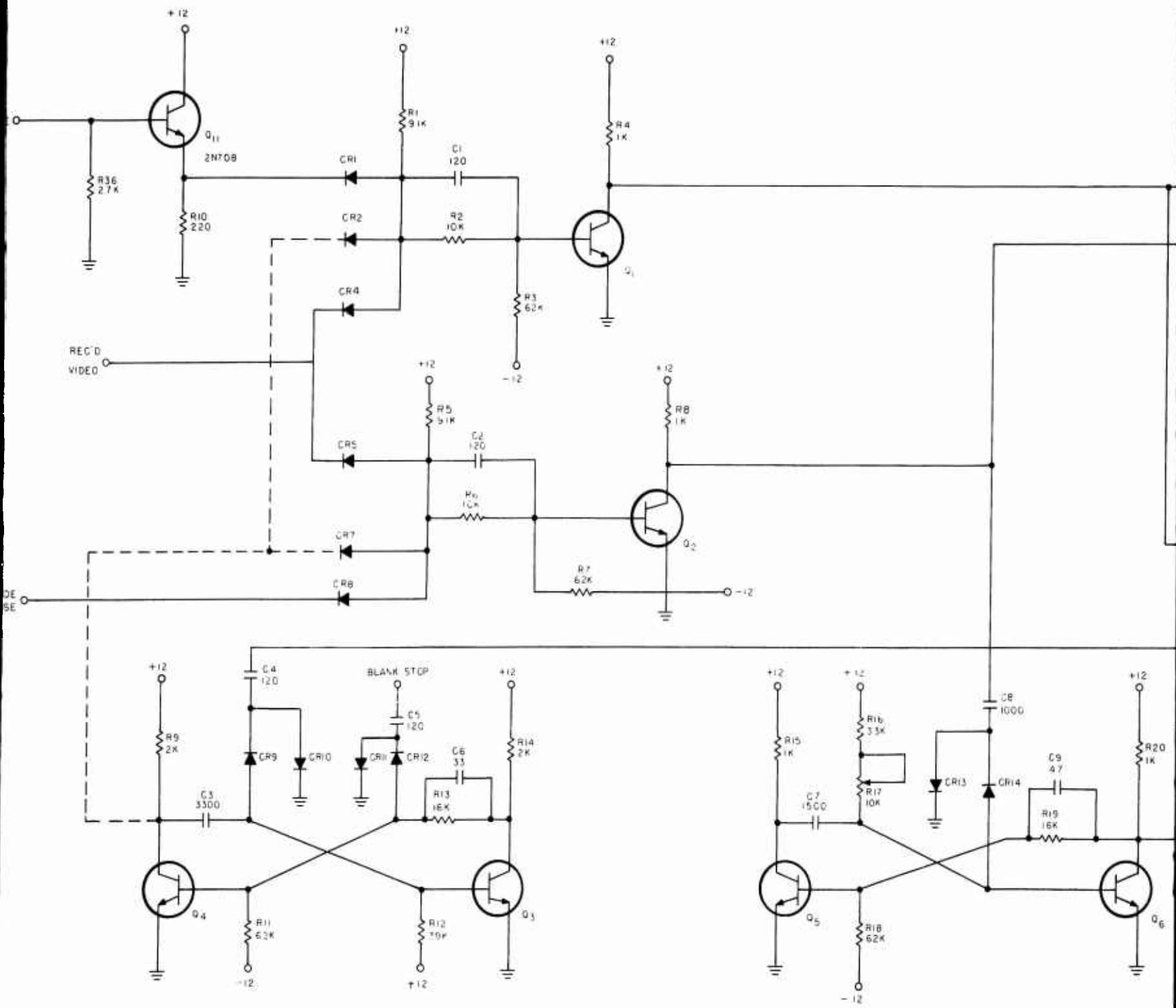
1

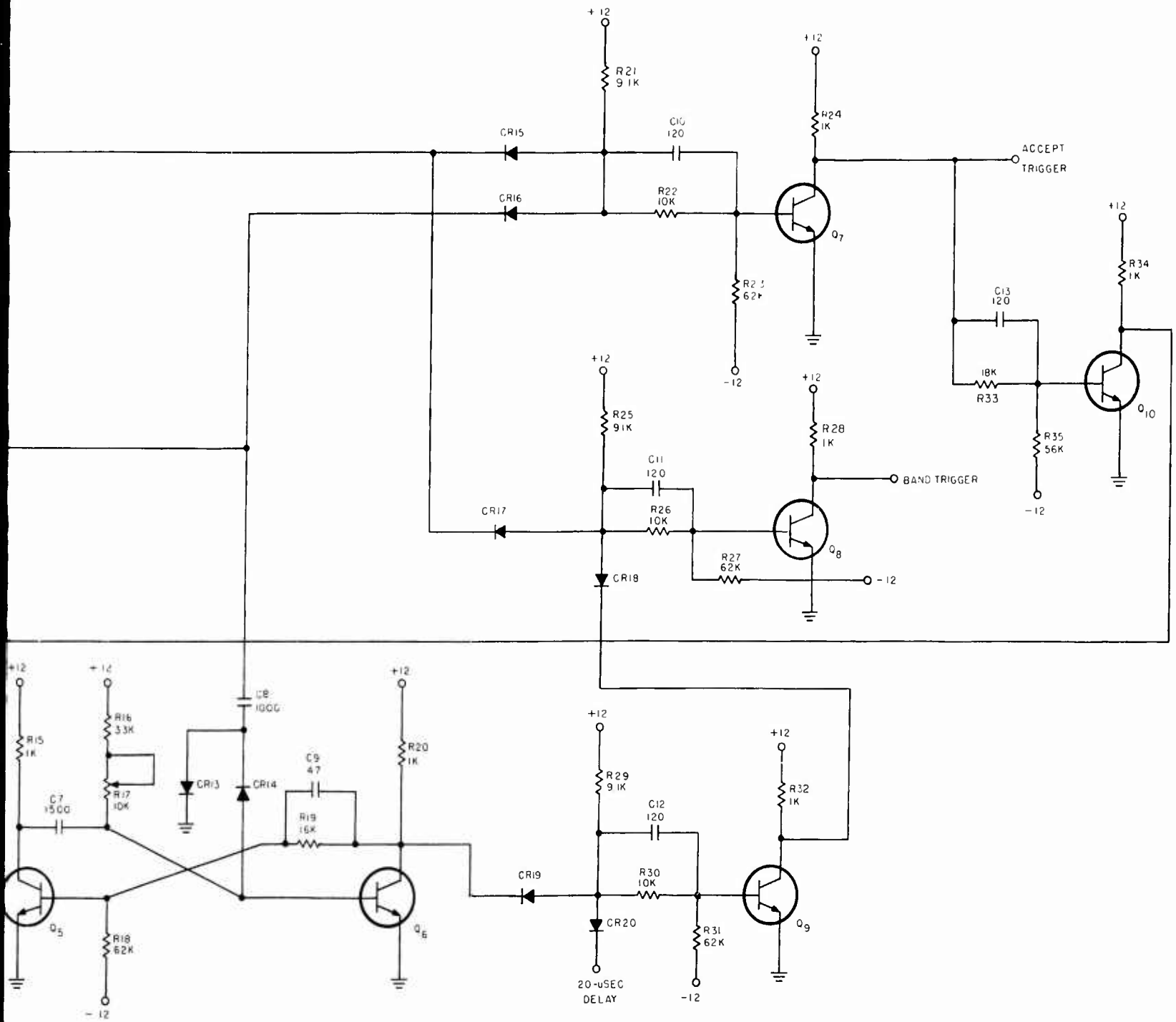


- NOTE
- 1 ALL RESISTORS IN OHMS
 - 2 ALL CAPACITORS IN PF
 - 3 ALL DIODES TYPE IN691
 - 4 ALL TRANSISTORS TYPE 2N708
 5. DASHED INTERCONNECTION REMOVED FOR LAB TEST



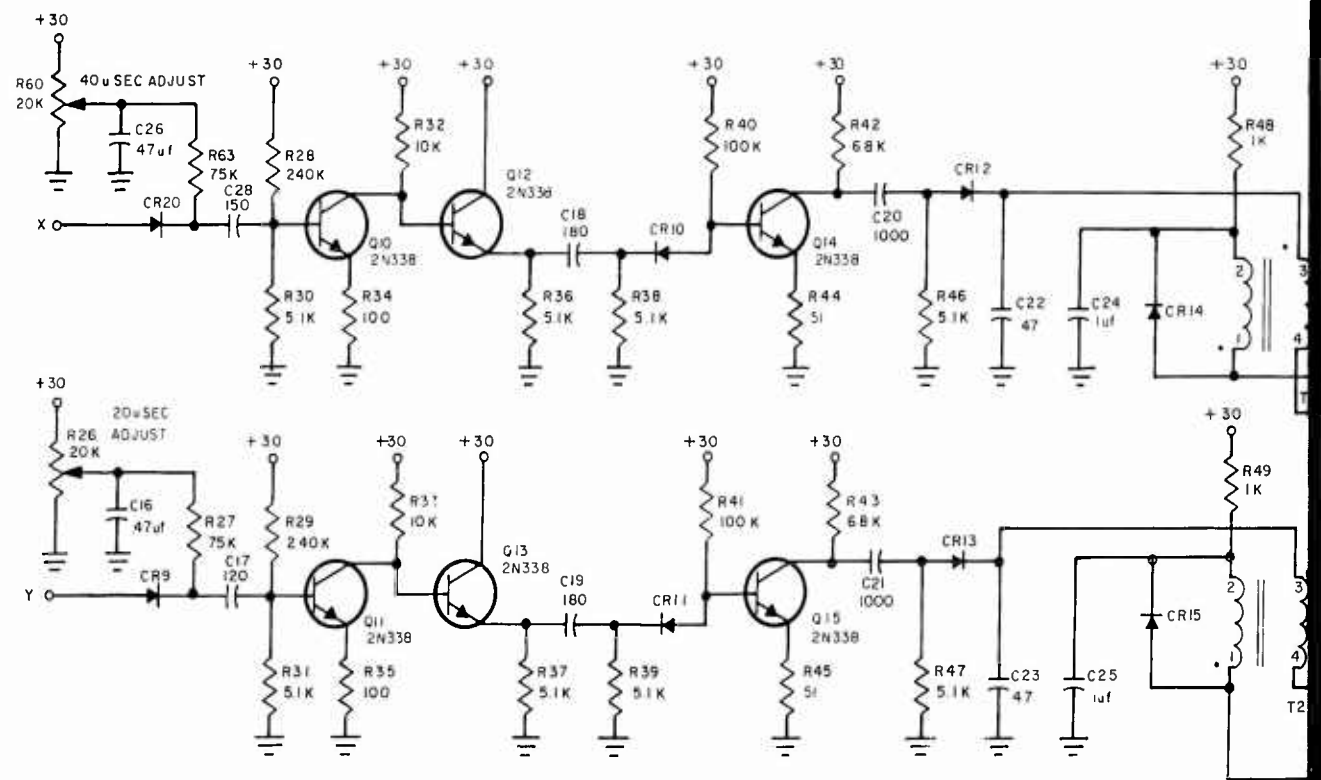
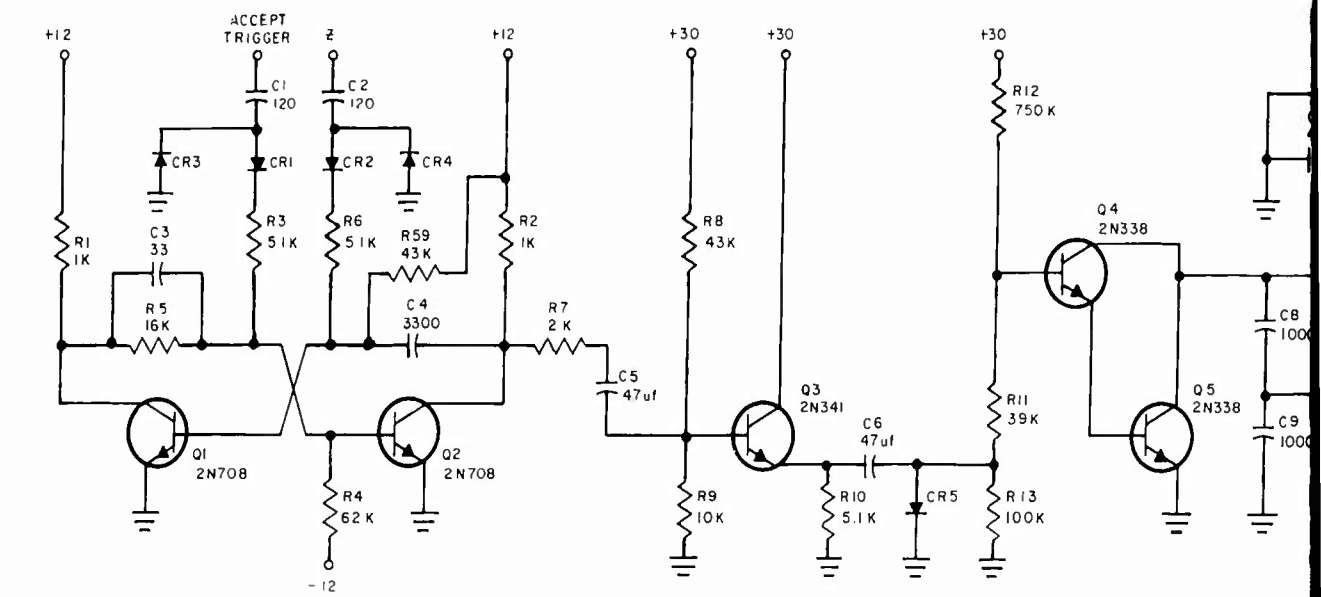
1





3

FIGURE 5-34
BAND DECODER (4300)



1

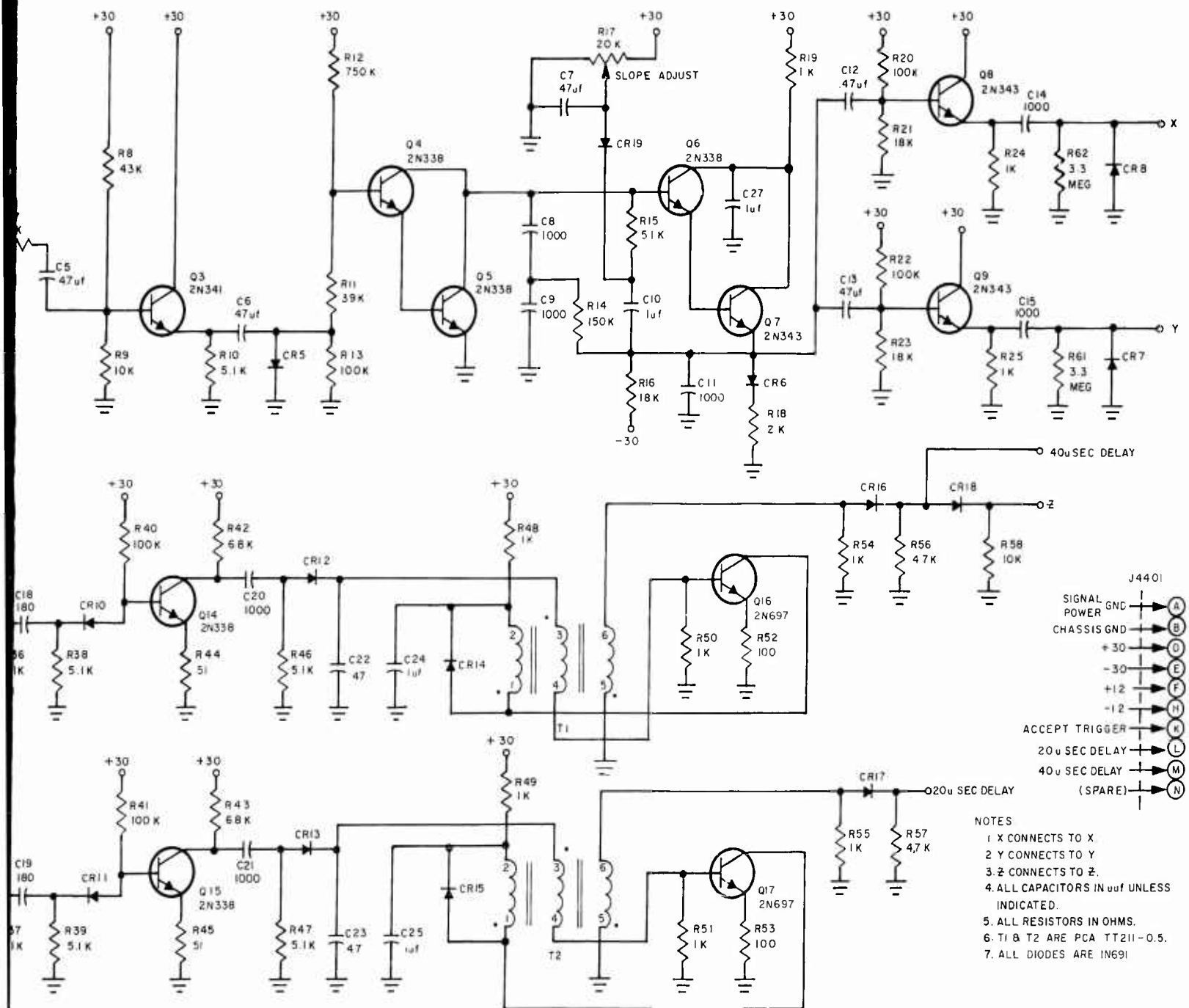
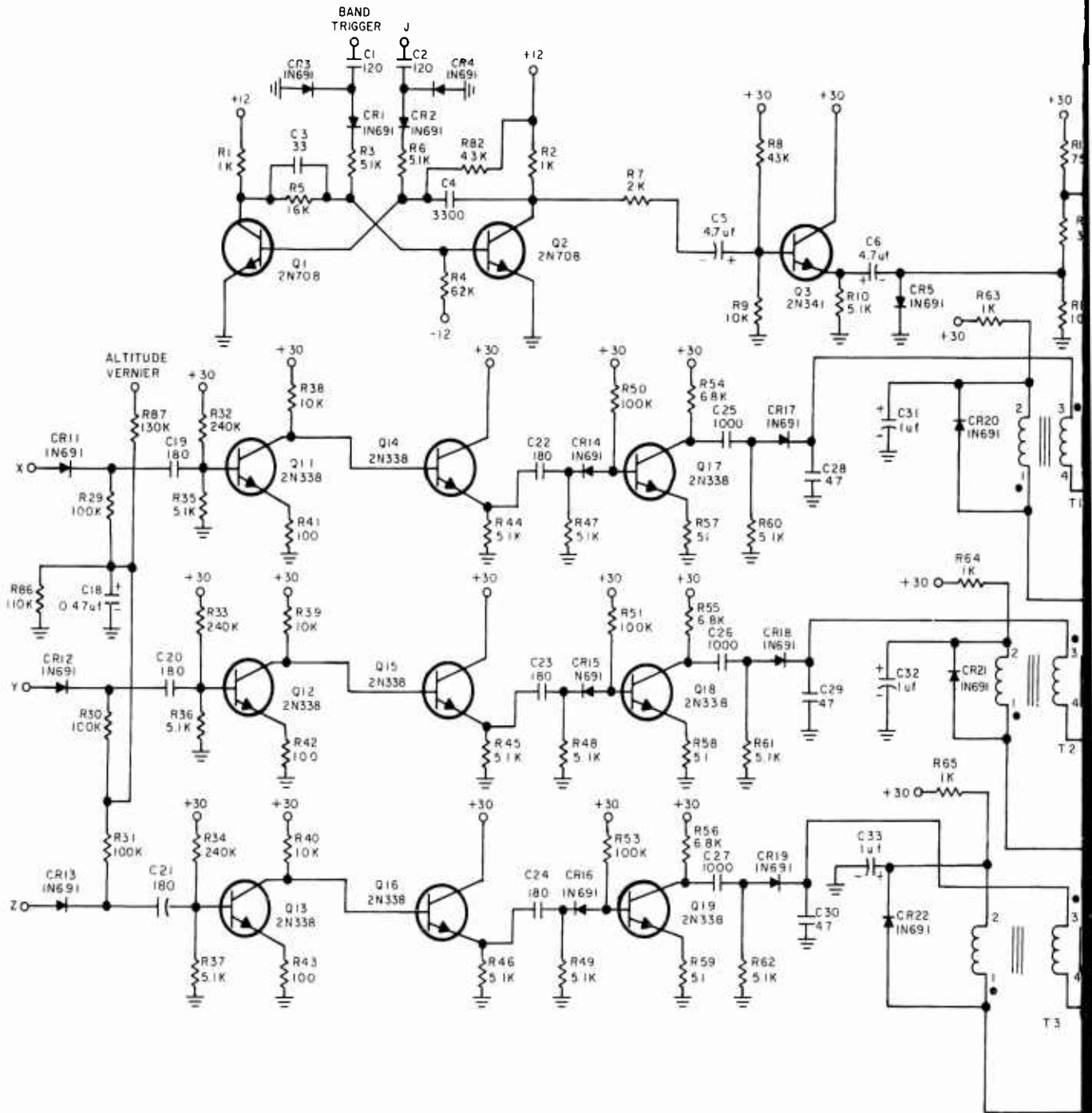


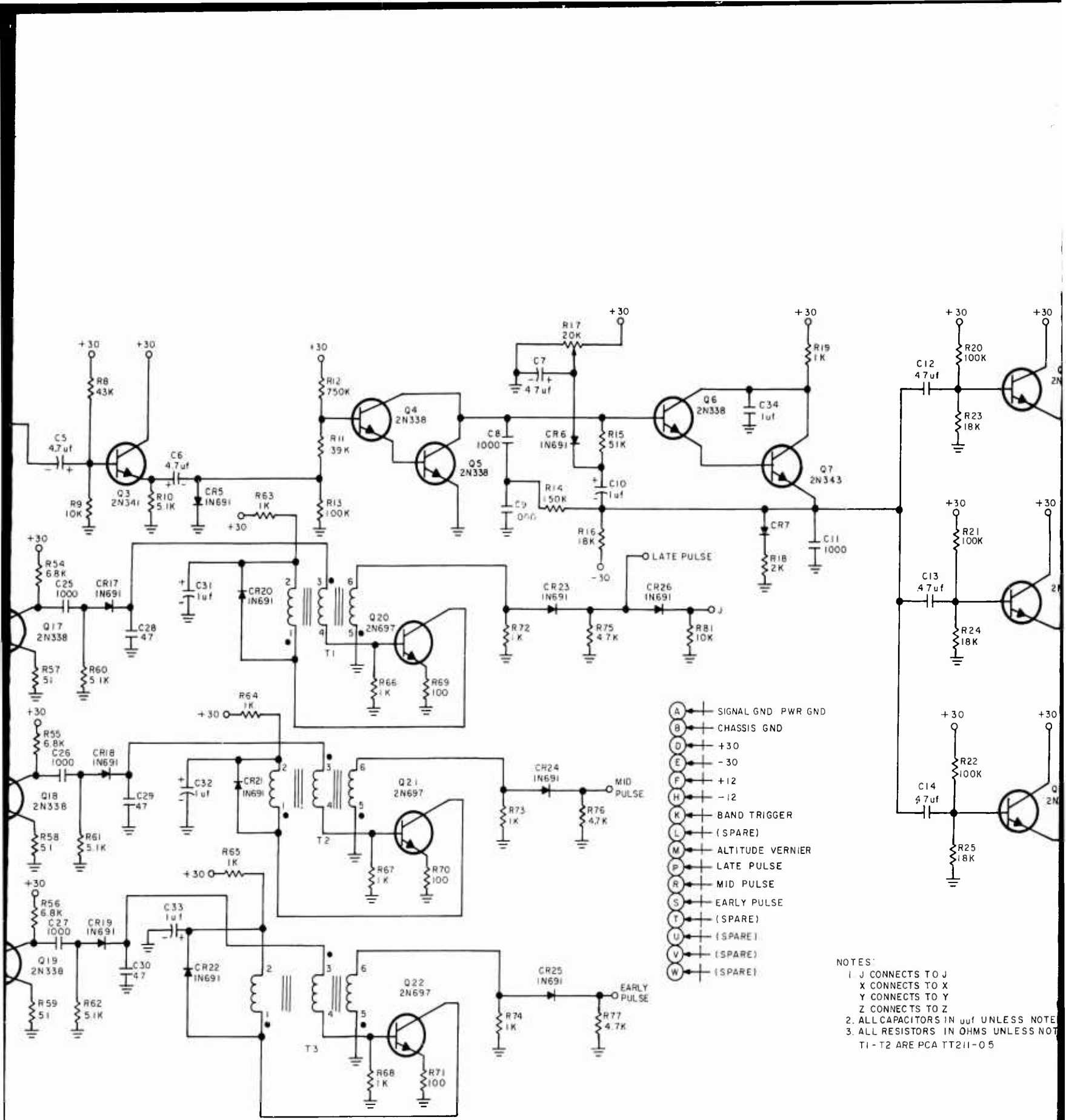
FIGURE 5-35

TWO-PULSE DELAY GENERATOR (4400)

2



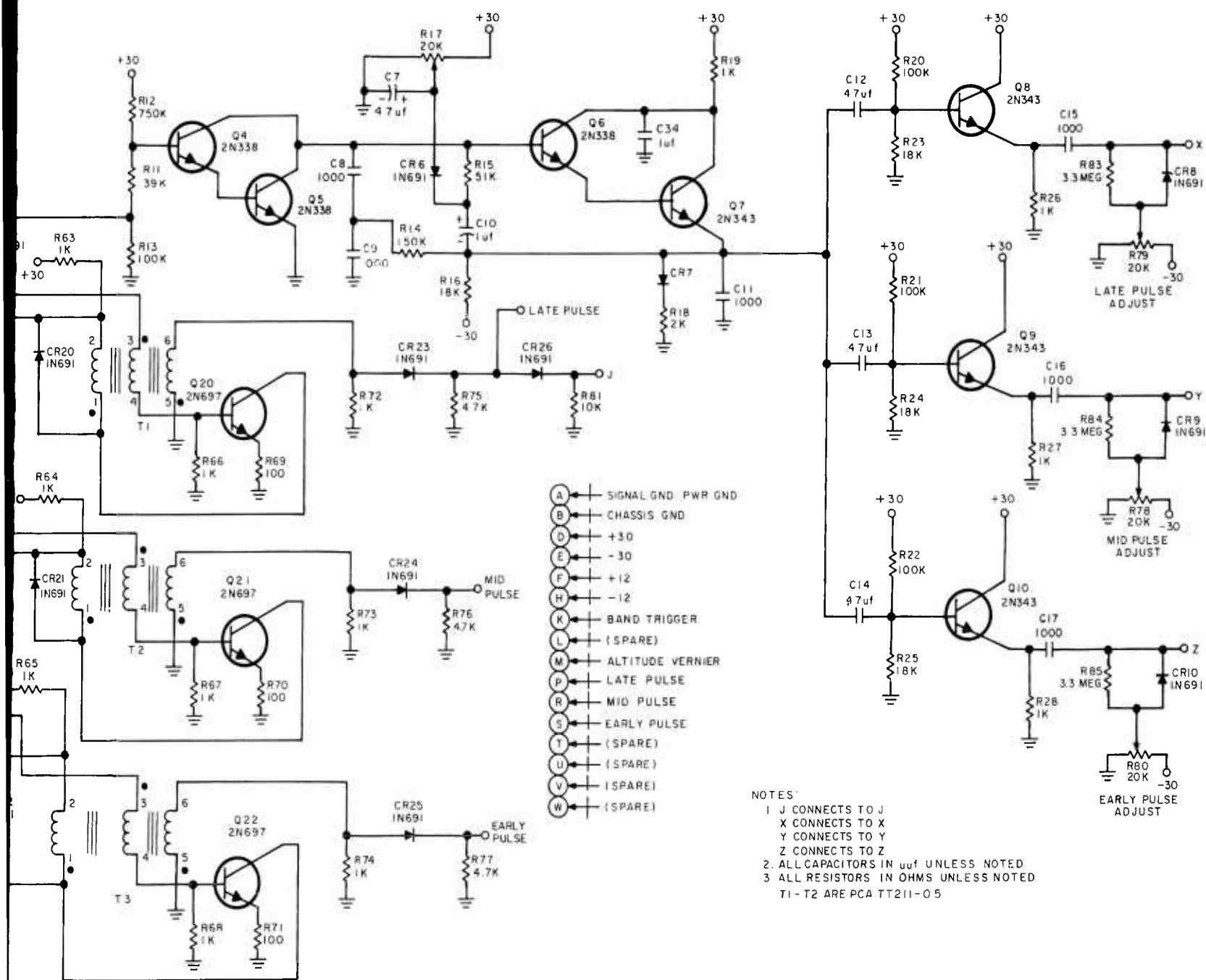
1



- A ← SIGNAL GND PWR GND
- B ← CHASSIS GND
- C ← +30
- D ← -30
- E ← +12
- F ← -12
- G ← BAND TRIGGER
- H ← (SPARE)
- I ← ALTITUDE VERNIER
- J ← LATE PULSE
- K ← MID PULSE
- L ← EARLY PULSE
- M ← (SPARE)
- N ← (SPARE)
- O ← (SPARE)
- P ← (SPARE)
- Q ← (SPARE)
- R ← (SPARE)
- S ← (SPARE)
- T ← (SPARE)
- U ← (SPARE)
- V ← (SPARE)
- W ← (SPARE)

NOTES:
 1. J CONNECTS TO J
 X CONNECTS TO X
 Y CONNECTS TO Y
 Z CONNECTS TO Z
 2. ALL CAPACITORS IN μf UNLESS NOTE
 3. ALL RESISTORS IN OHMS UNLESS NOTED
 T1 - T2 ARE PCA TT211-05

2

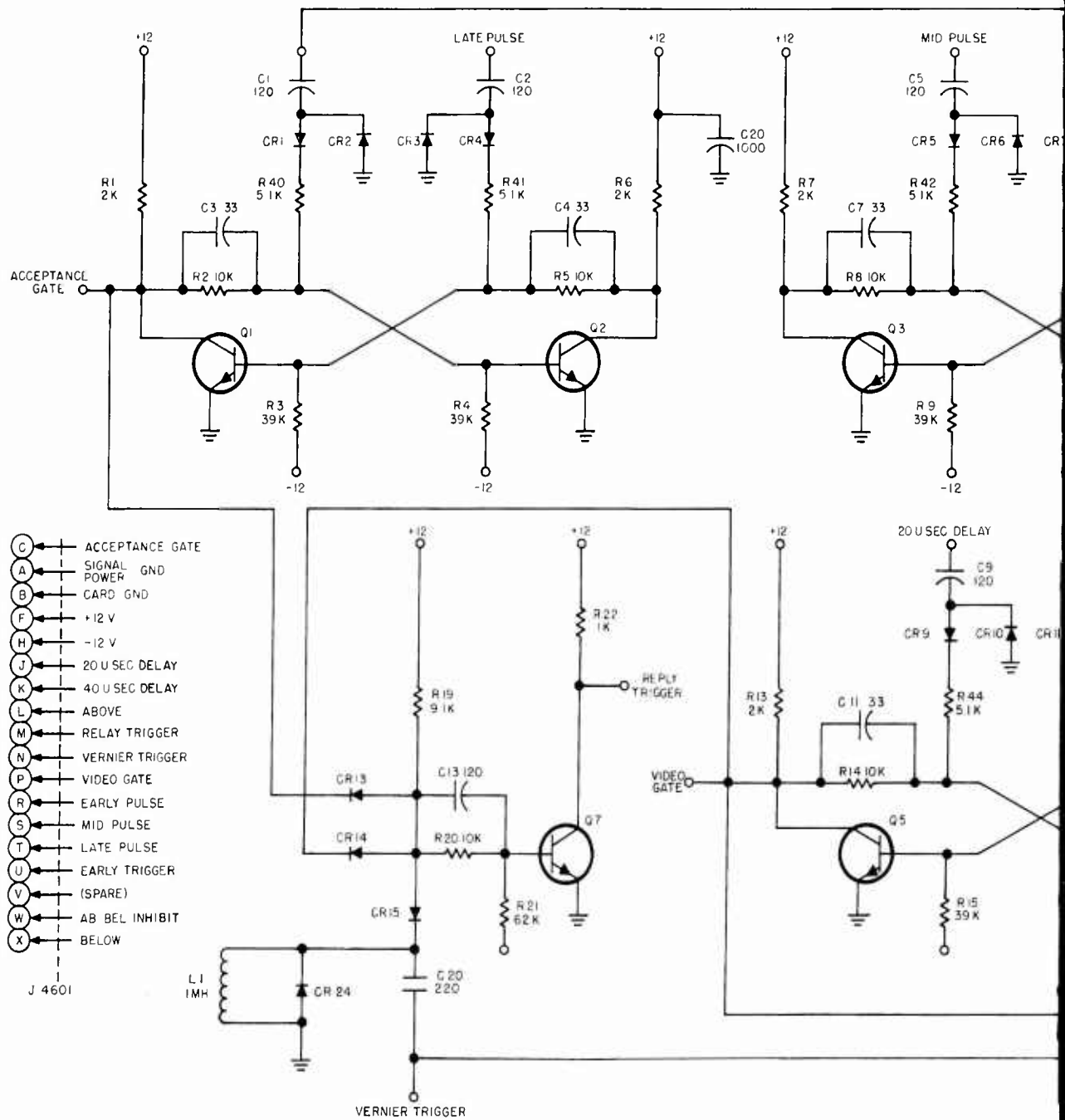


- A — SIGNAL GND PWR GND
- B — CHASSIS GND
- C — +30
- D — -30
- E — +12
- F — -12
- G — BAND TRIGGER
- H — (SPARE)
- I — ALTITUDE VERNIER
- J — LATE PULSE
- K — MID PULSE
- L — EARLY PULSE
- M — (SPARE)
- N — (SPARE)
- O — (SPARE)
- P — (SPARE)
- Q — (SPARE)
- R — (SPARE)
- S — (SPARE)
- T — (SPARE)
- U — (SPARE)
- V — (SPARE)
- W — (SPARE)

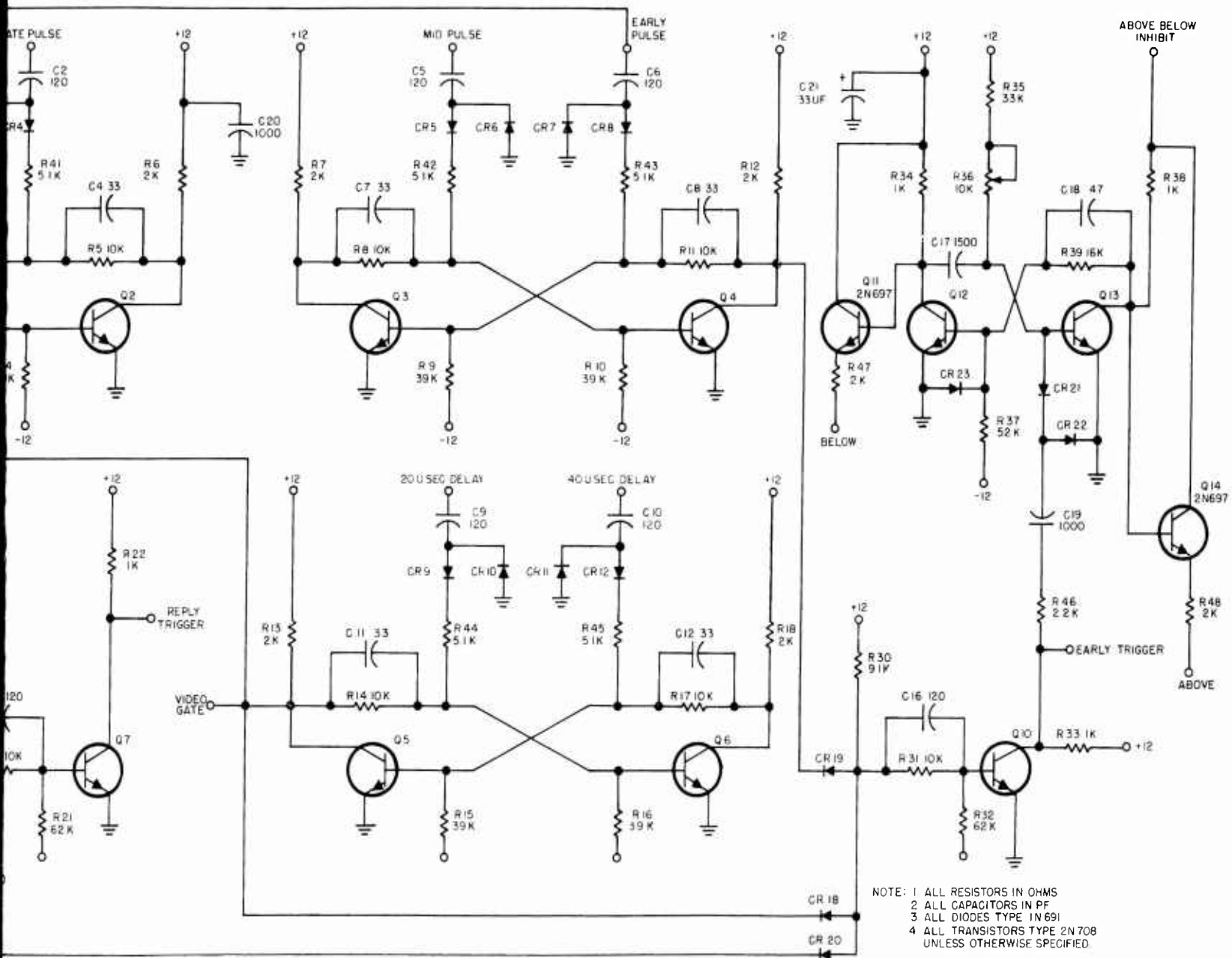
NOTES:
 1 J CONNECTS TO J
 X CONNECTS TO X
 Y CONNECTS TO Y
 Z CONNECTS TO Z
 2 ALL CAPACITORS IN μf UNLESS NOTED
 3 ALL RESISTORS IN OHMS UNLESS NOTED
 T1 - T2 ARE PCA TT211-05

3

FIGURE 5-36
 THREE-PULSE DELAY GENERATOR (4500)



1



2

FIGURE 5-37
VERNIER-DECODER (4600)

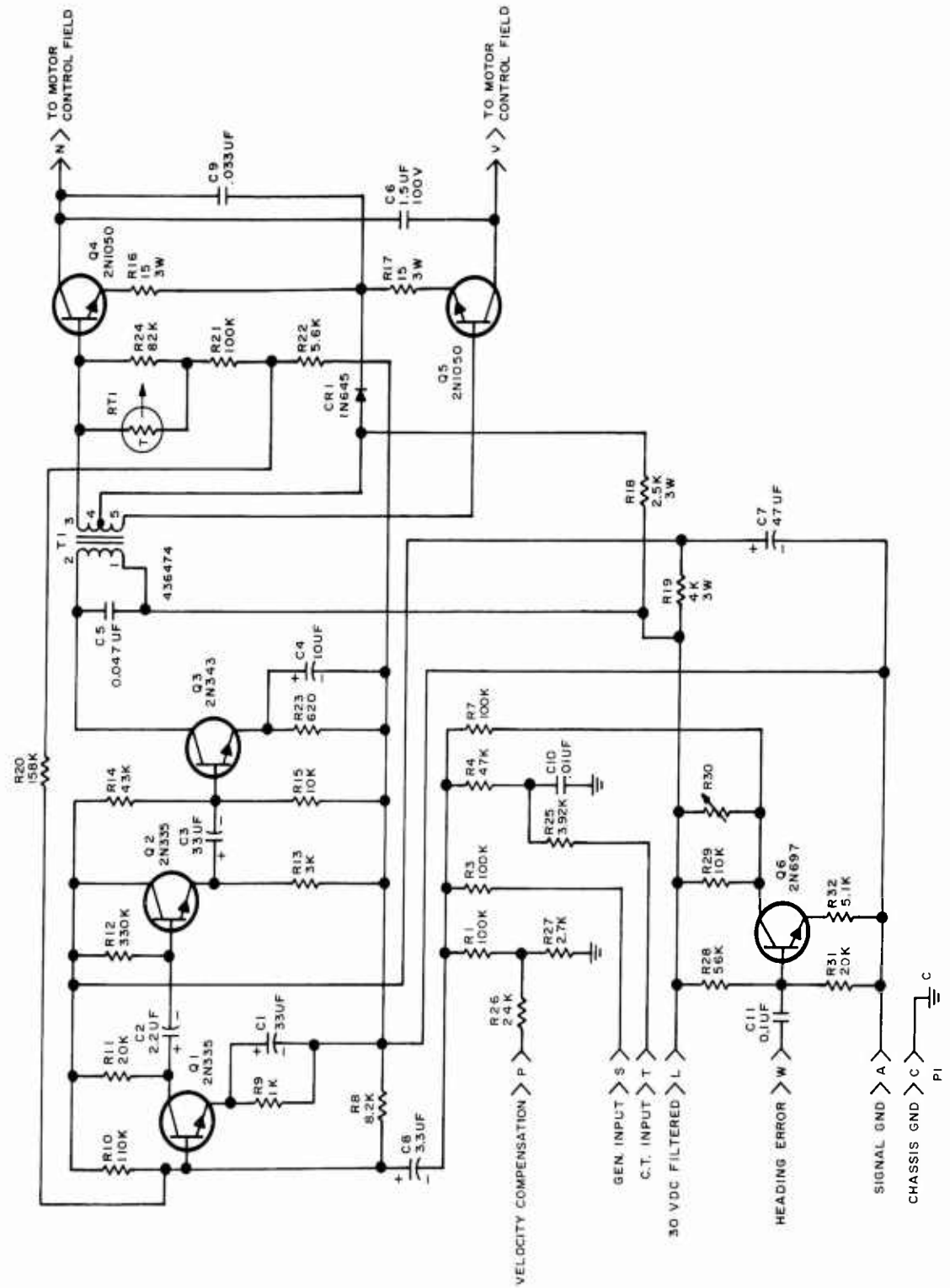
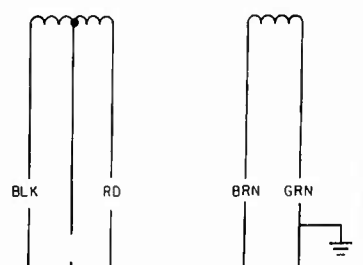
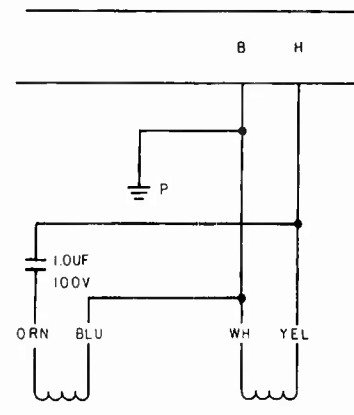
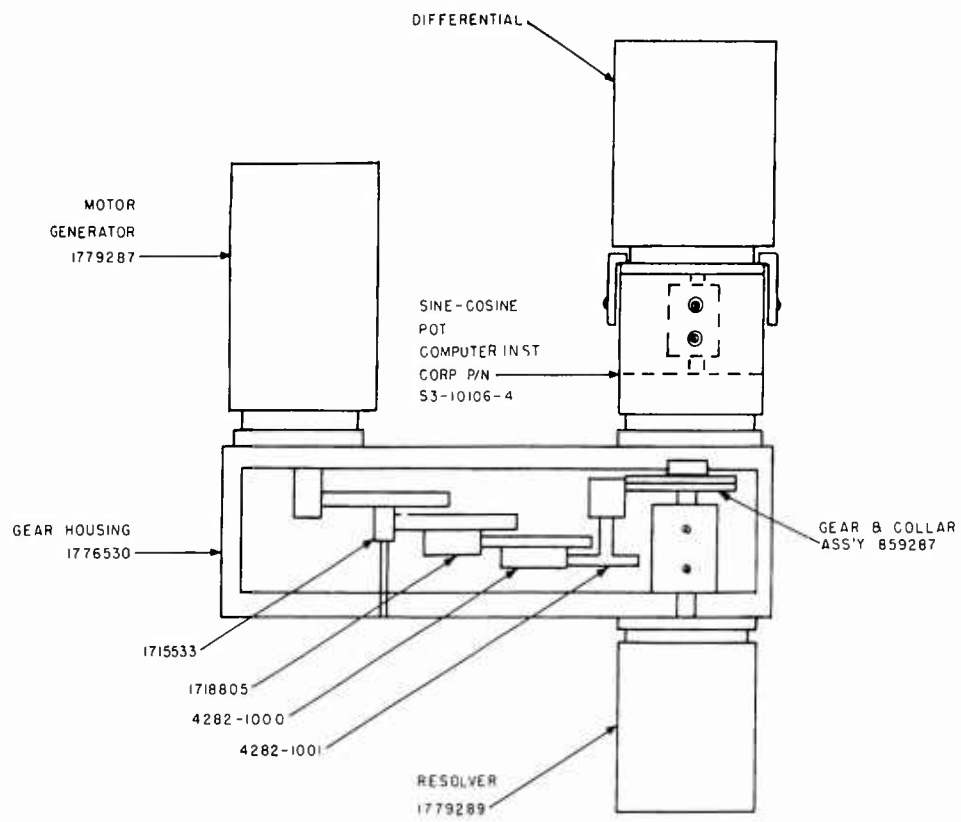


FIGURE 5-38. A-1 MAGNETIC BEARING MOTOR AMPLIFIER

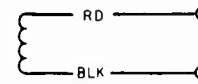
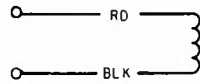


C L D D A

1

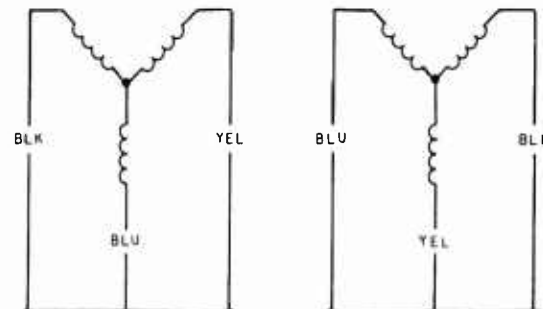
KEARFOTT
RS9114A
TRANSMITTER

26V 400 \sim



KEARFOTT
RS9114A
TRANSMITTER

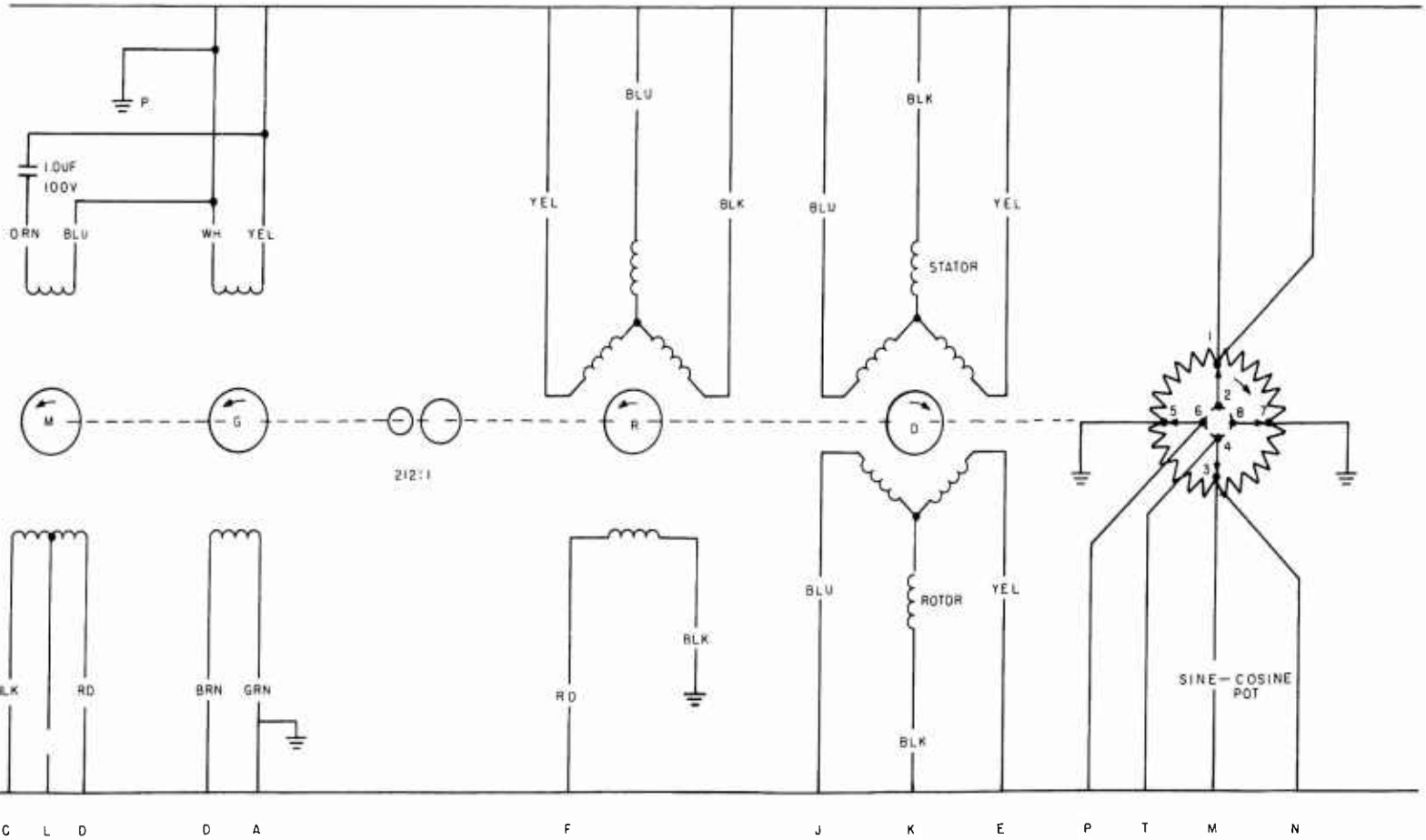
26V 400 \sim



B H

X Y W b a

R S



C L D

D A

F

J

K

E

P

T

M

N

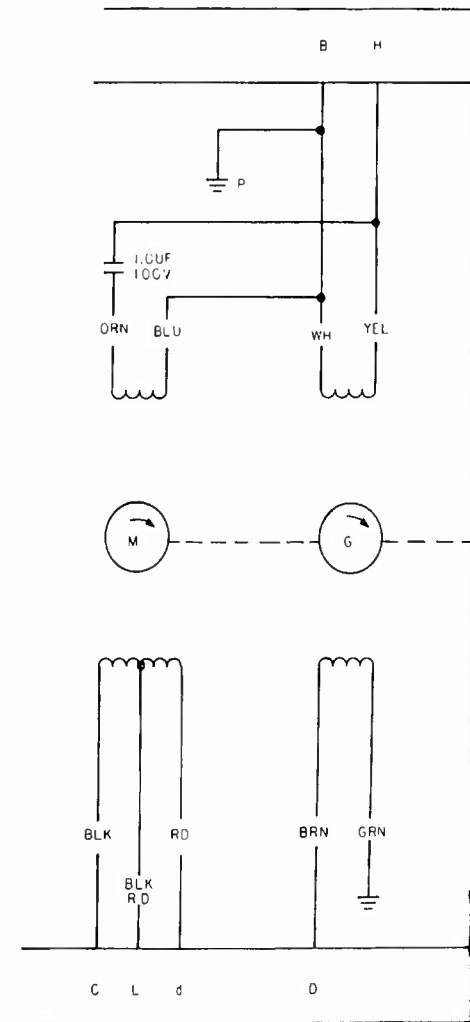
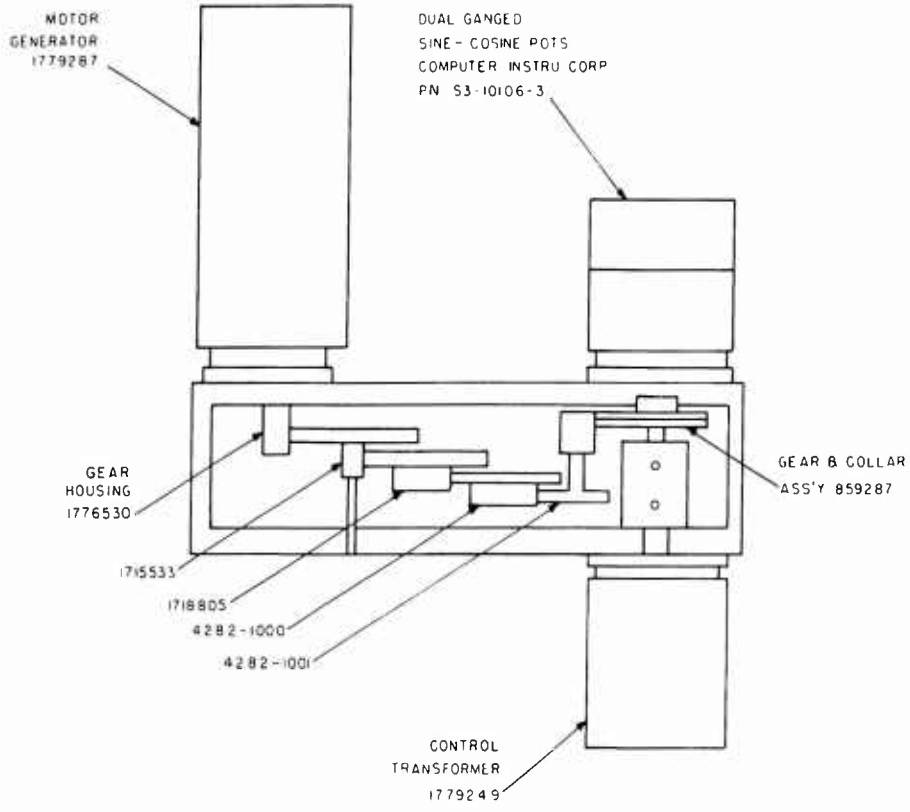
-

+

+SIN -COS

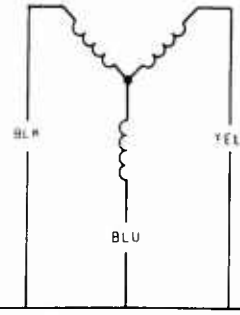
2

FIGURE 5-40
A-3 RELATIVE BEARING SERVO



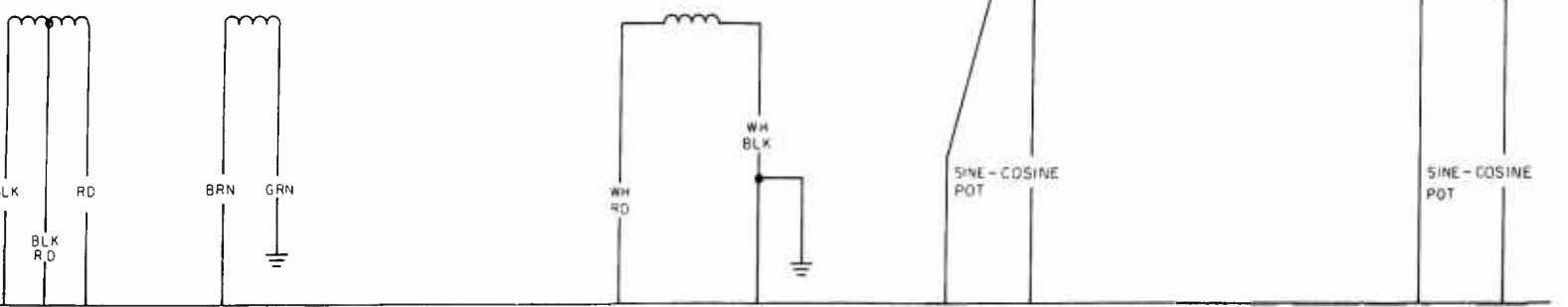
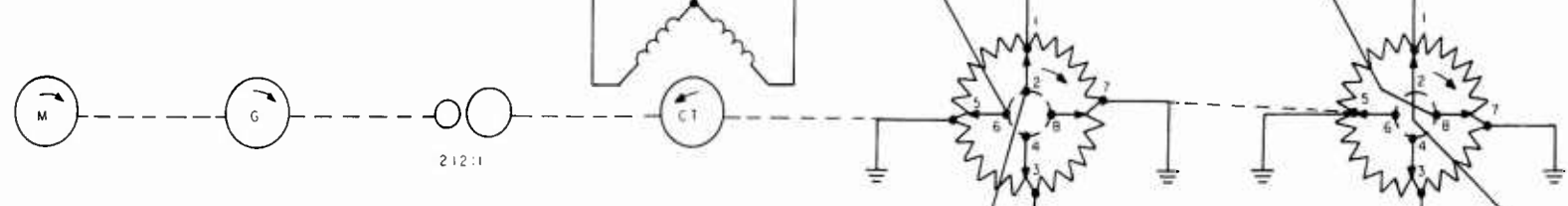
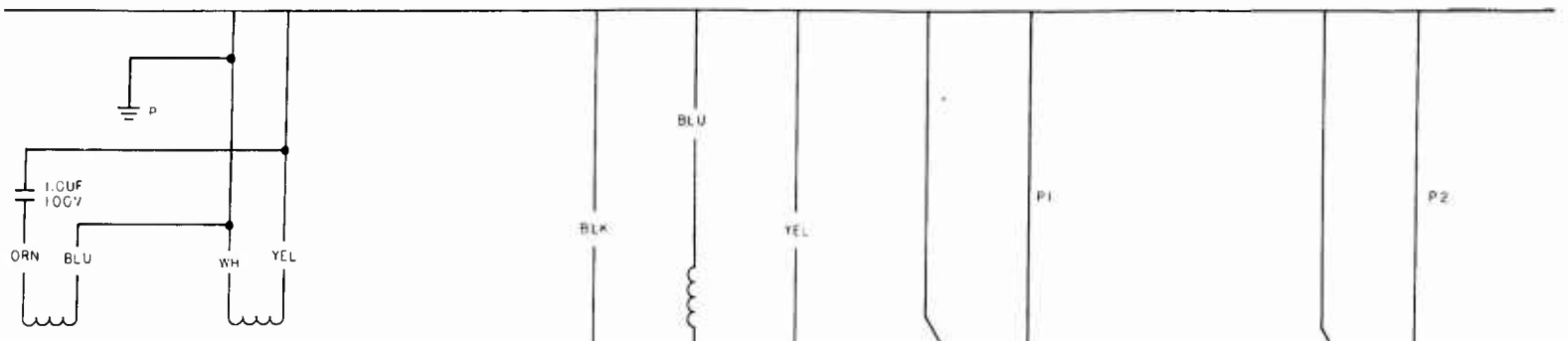
1

26V 400~
 + RD
 - BLK
 KEARFOTT
 RS9114A
 TRANSMITTER



$+V_E \sin \phi$
 $+V_E$
 $-V_N \sin \phi$
 $+V_N$

B H b o f K N T S

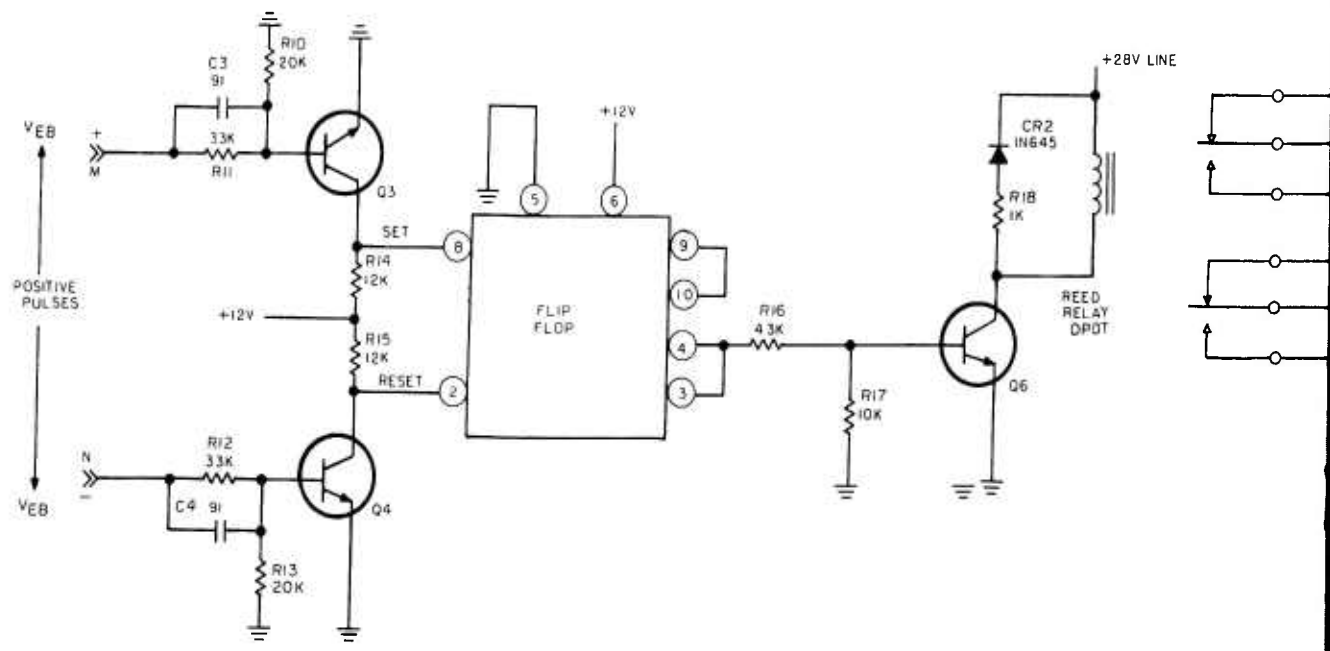
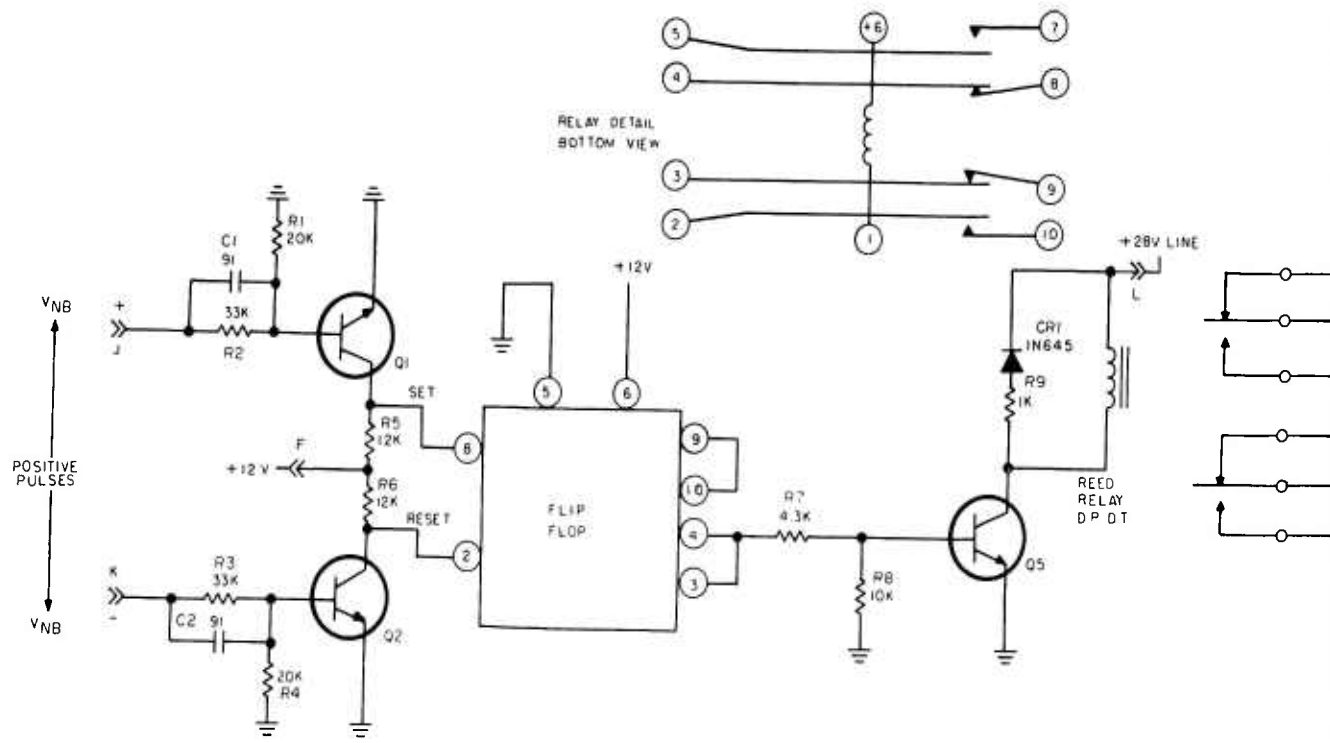


C L d D F A M J P R

$+V_E \cos \phi$
 $-V_E$
 $-V_N$
 $+V_N \cos \phi$

2

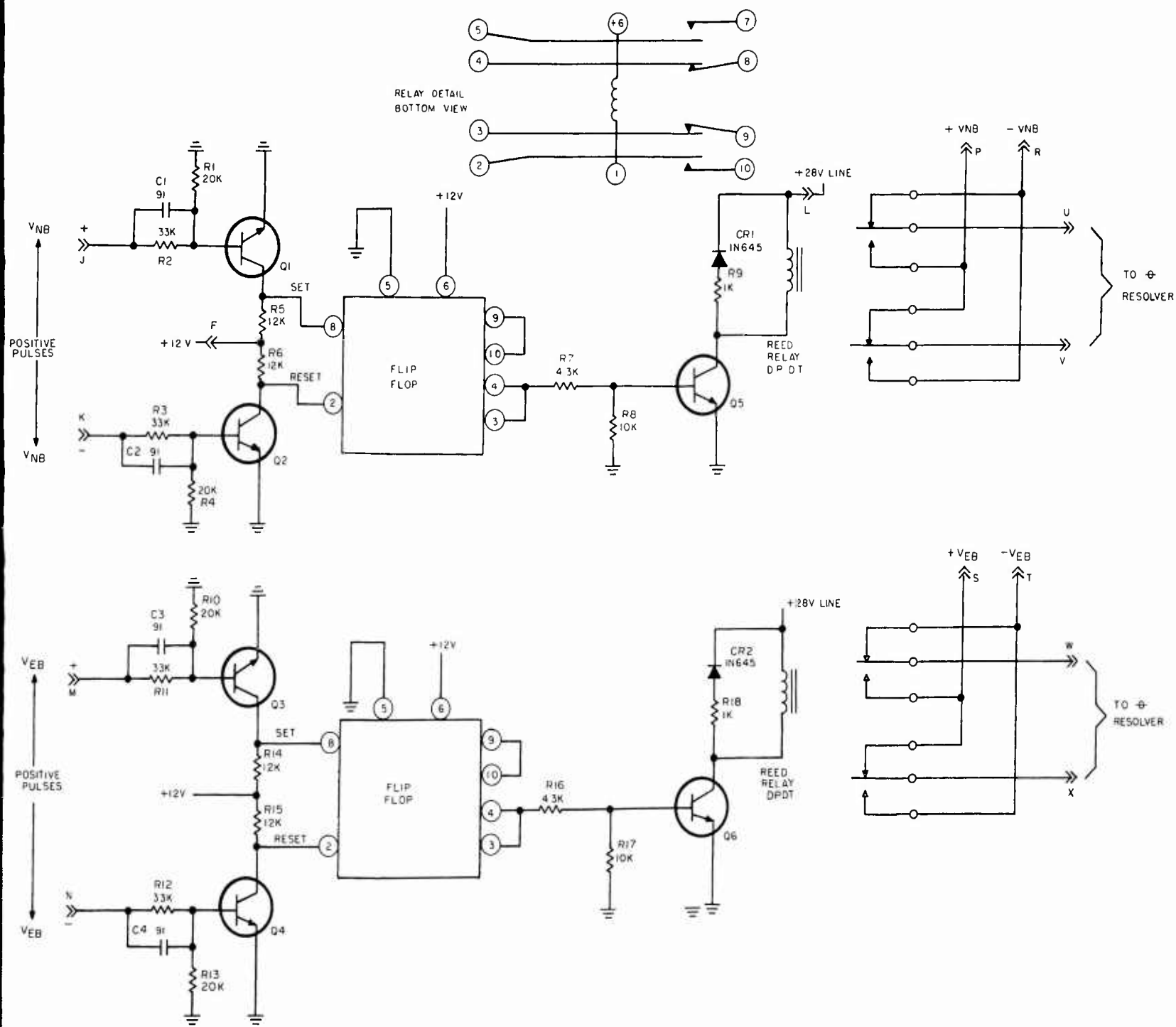
FIGURE 5-41
 A-4 MAGNETIC BEARING SERVO



Q₁, Q₂, Q₃, Q₄, ----- 2N697
 Q₅, Q₆ ----- 2N2087

NOTE: RELAY SHOWN IN DE-ENERGIZED STATE.
 CAPACITORS ARE IN pf



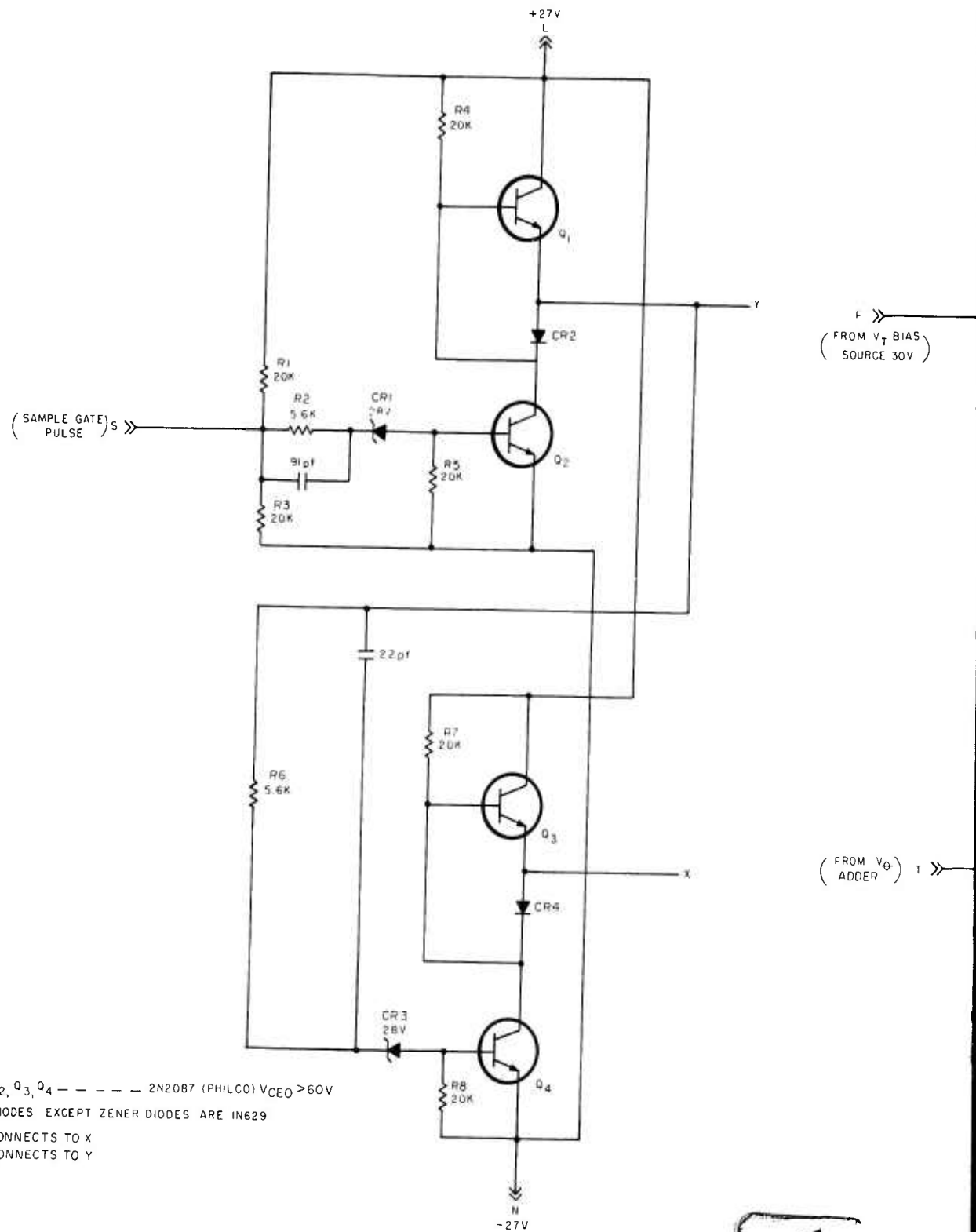


Q₁, Q₂, Q₃, Q₄, ----- 2N697
 Q₅, Q₆ ----- 2N2087

NOTE: RELAY SHOWN IN DE-ENERGIZED STATE
 CAPACITORS ARE IN pf

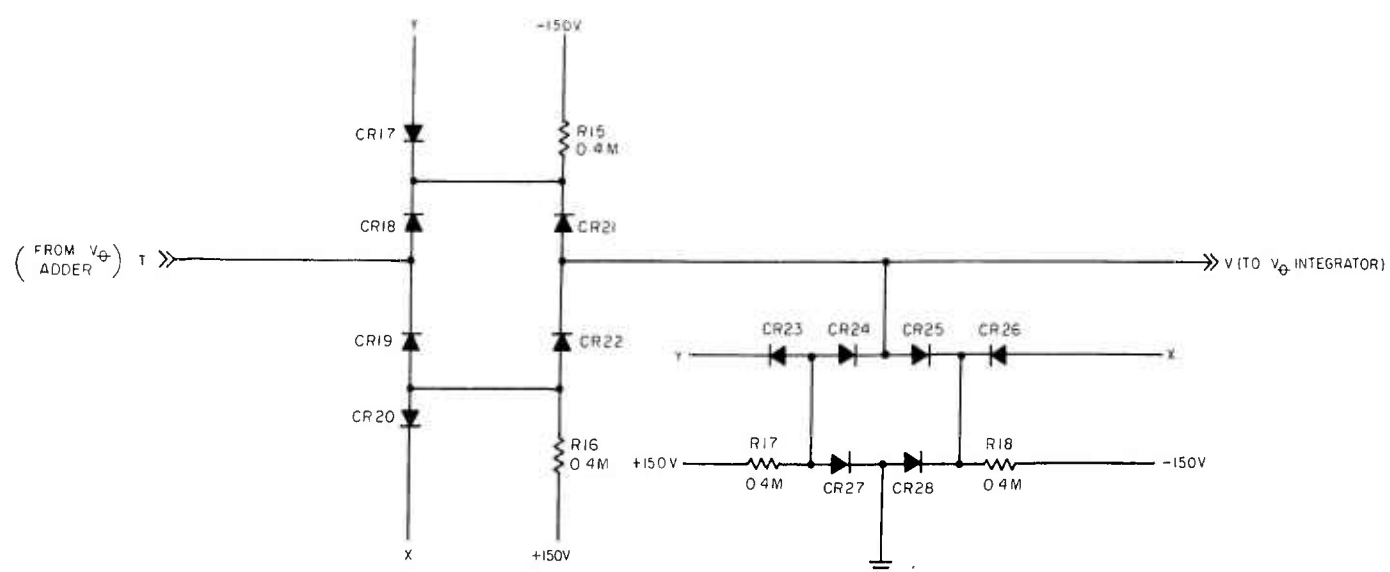
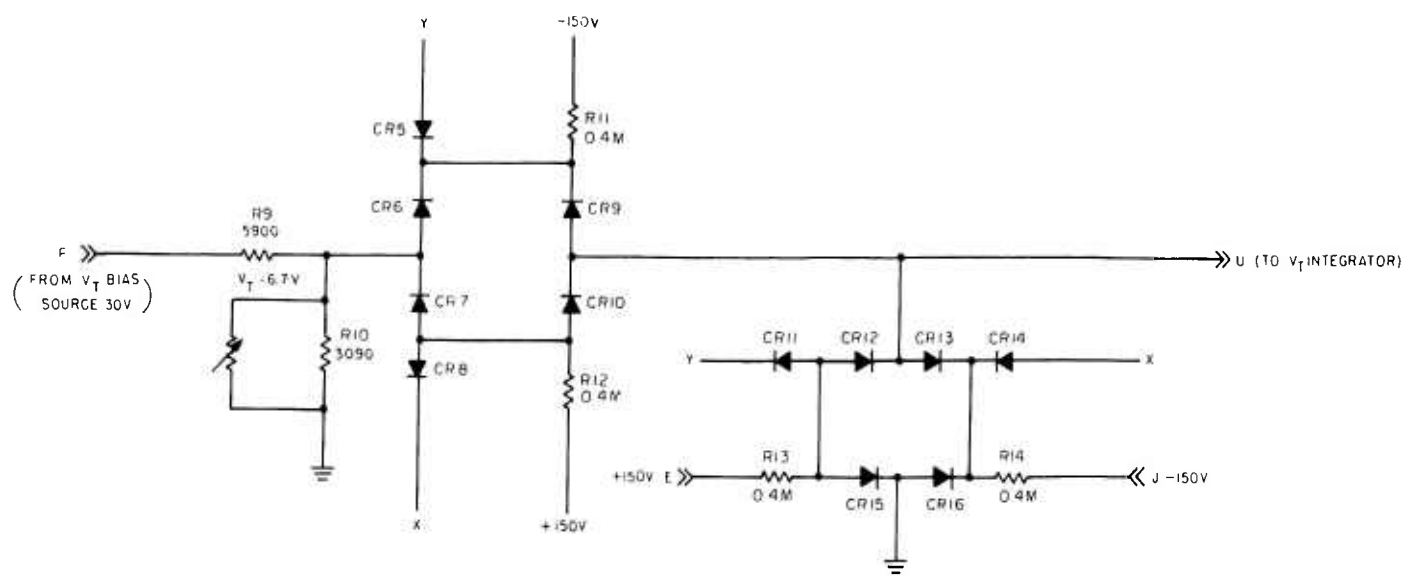


FIGURE 5-42
 A-5 POLARITY CONTROL CIRCUIT



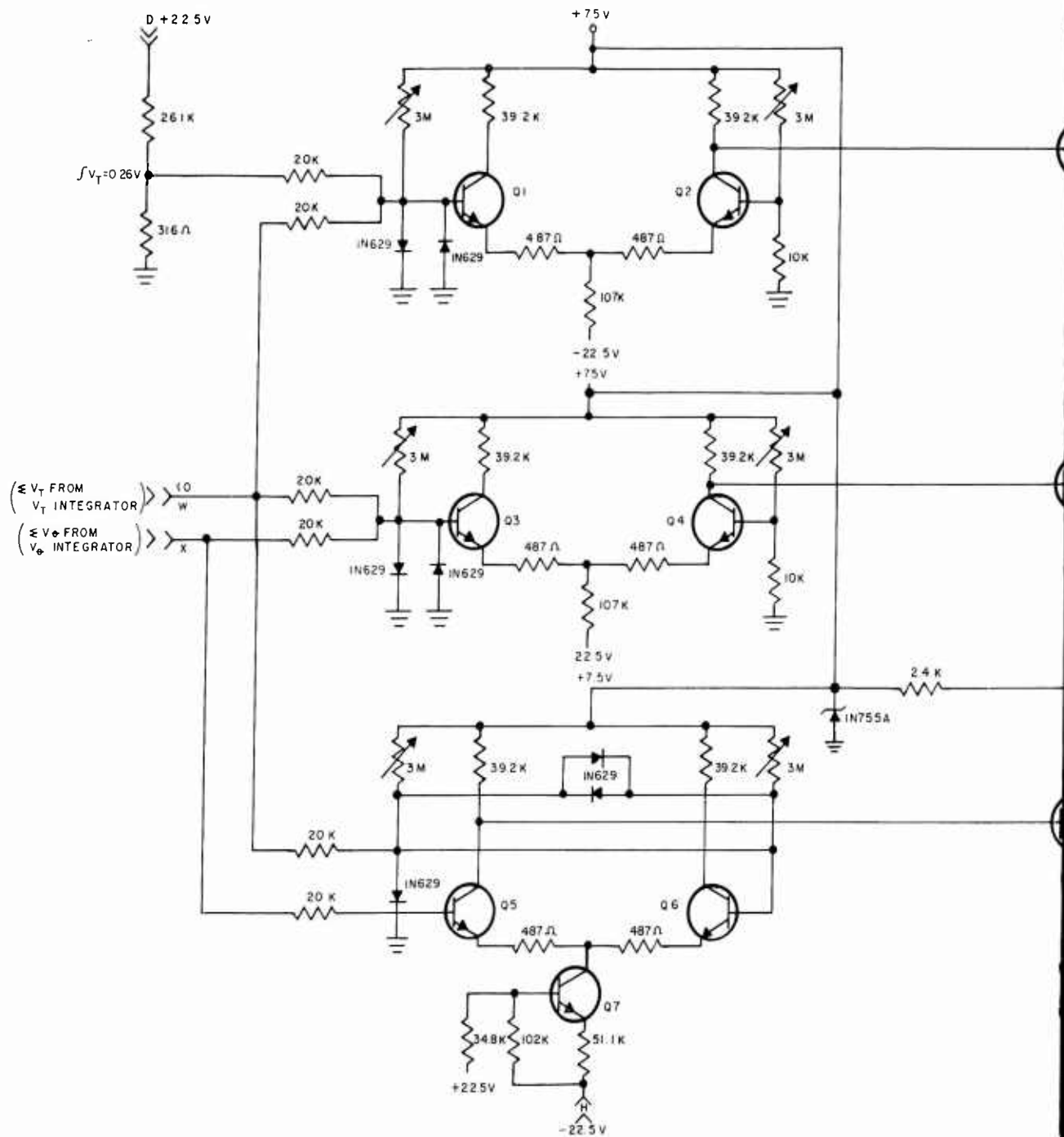
Q_1, Q_2, Q_3, Q_4 — — — — 2N2087 (PHILCO) $V_{CE0} > 60V$
 ALL DIODES EXCEPT ZENER DIODES ARE IN629
 X CONNECTS TO X
 Y CONNECTS TO Y

1



2

FIGURE 5-43
 A-6 NORMAL VELOCITY CRITERION COMPARATOR AND SAMPLE GATE CONTROLLER (SHEET 1 OF 2)



1

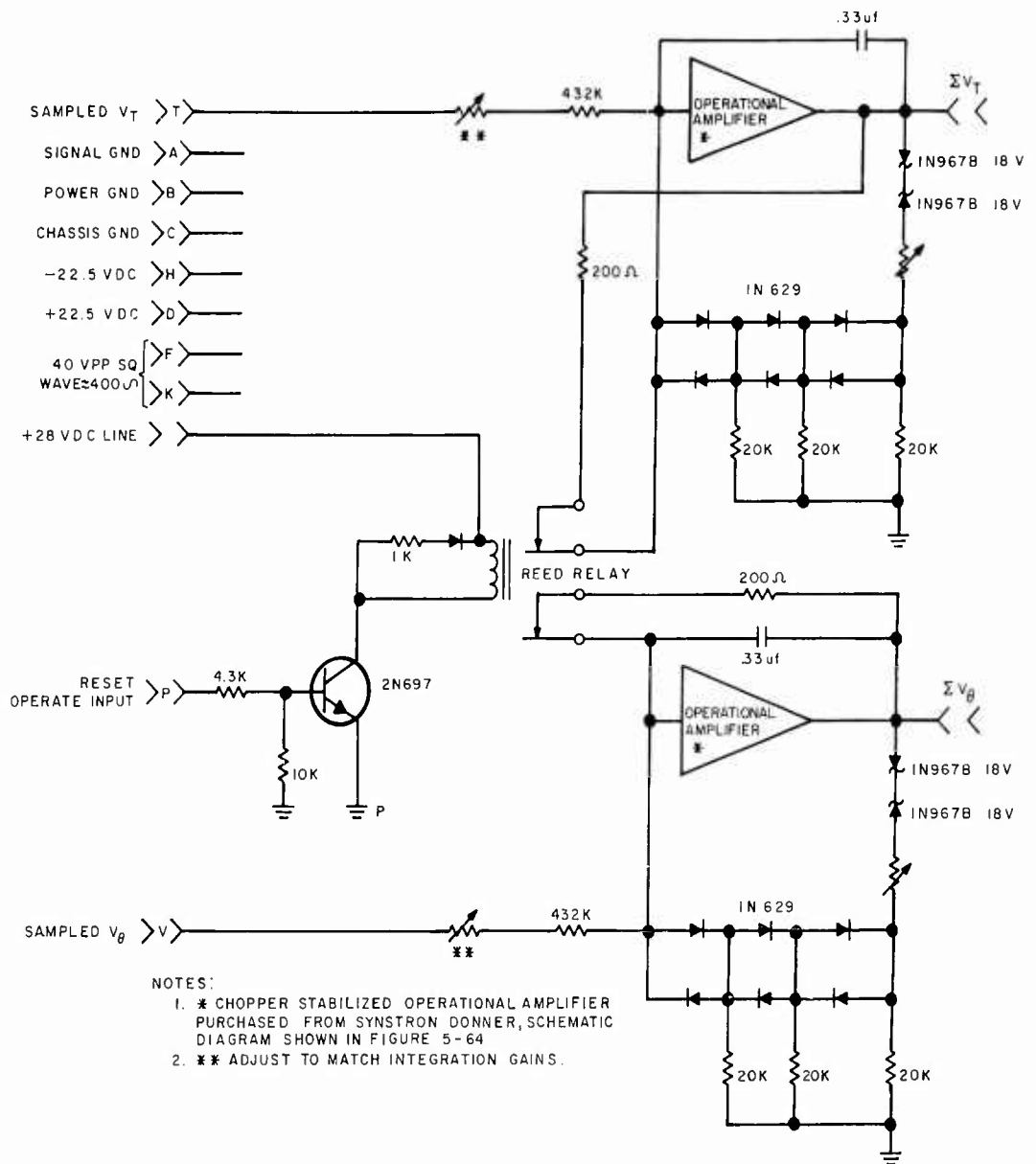
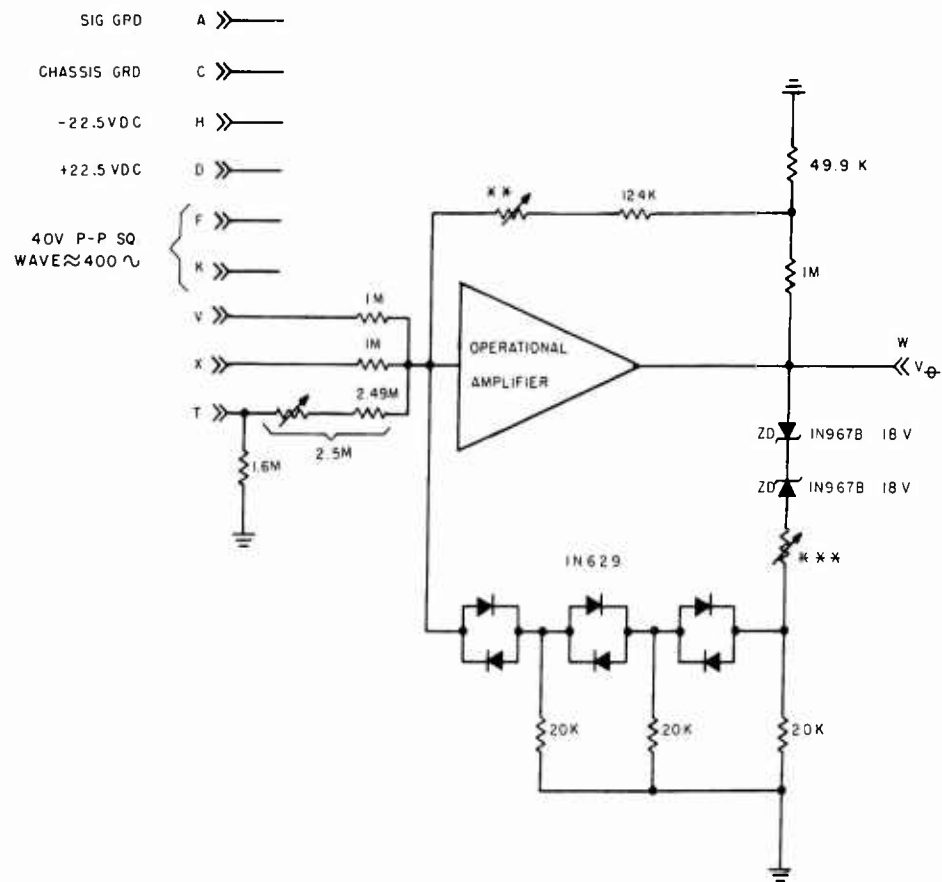
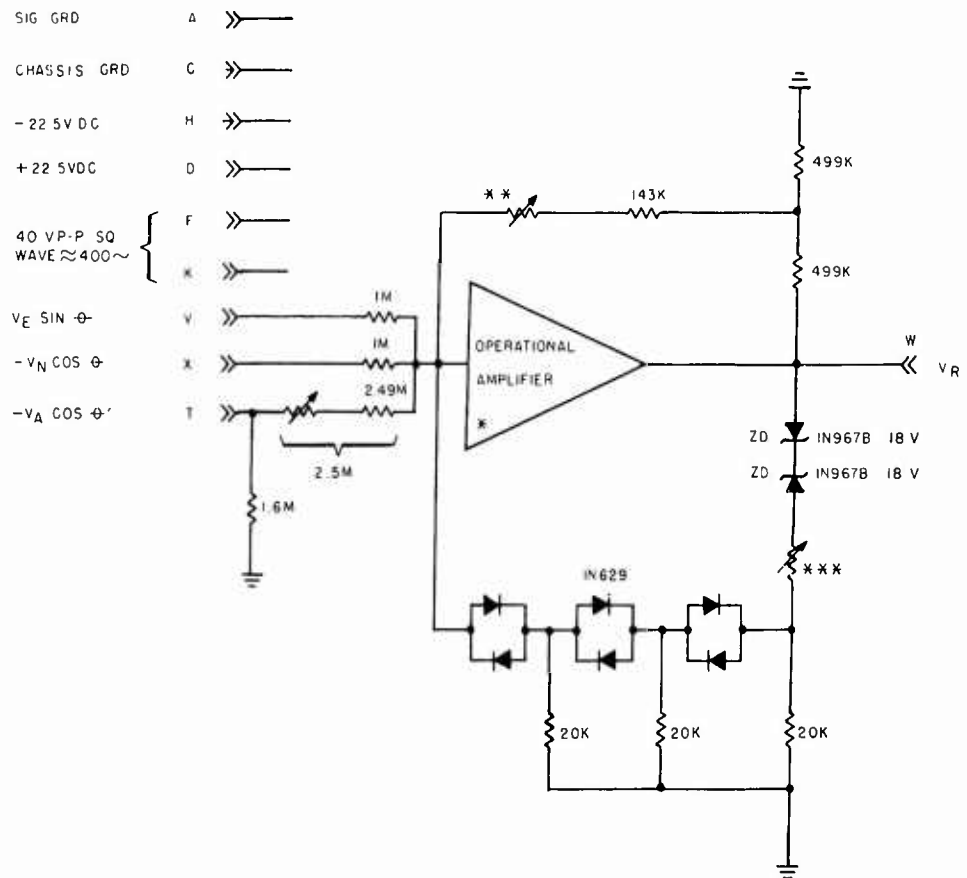


FIGURE 5-44. A-7 VELOCITY INTEGRATORS



- * CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER.
SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64
- ** ADJUSTED TO PRODUCE VOLTAGE GAIN OF 3.76 V/V FROM I-MEG INPUTS.
- *** ADJUSTS LIMIT VOLTAGE $\approx 0.15 \text{ V/K}\Omega$

FIGURE 5-45. A-B NORMAL VELOCITY ADDER



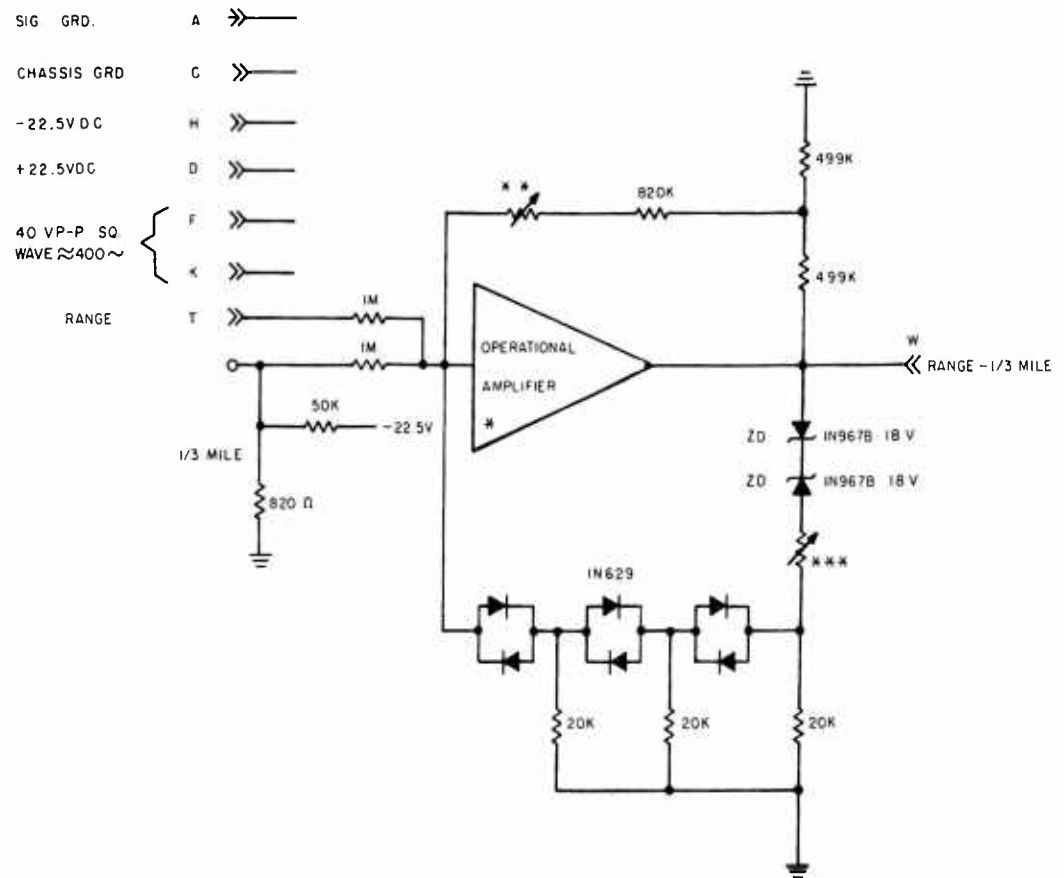
* CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER.

SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64

** ADJUSTED TO PRODUCE VOLTAGE GAIN OF 0.794 V/V FROM 1-MEG. INPUTS.

*** ADJUSTS LIMIT VOLTAGE $\approx 0.15V/K\Omega$

FIGURE 5 46. A-9 RADIAL VELOCITY ADDER

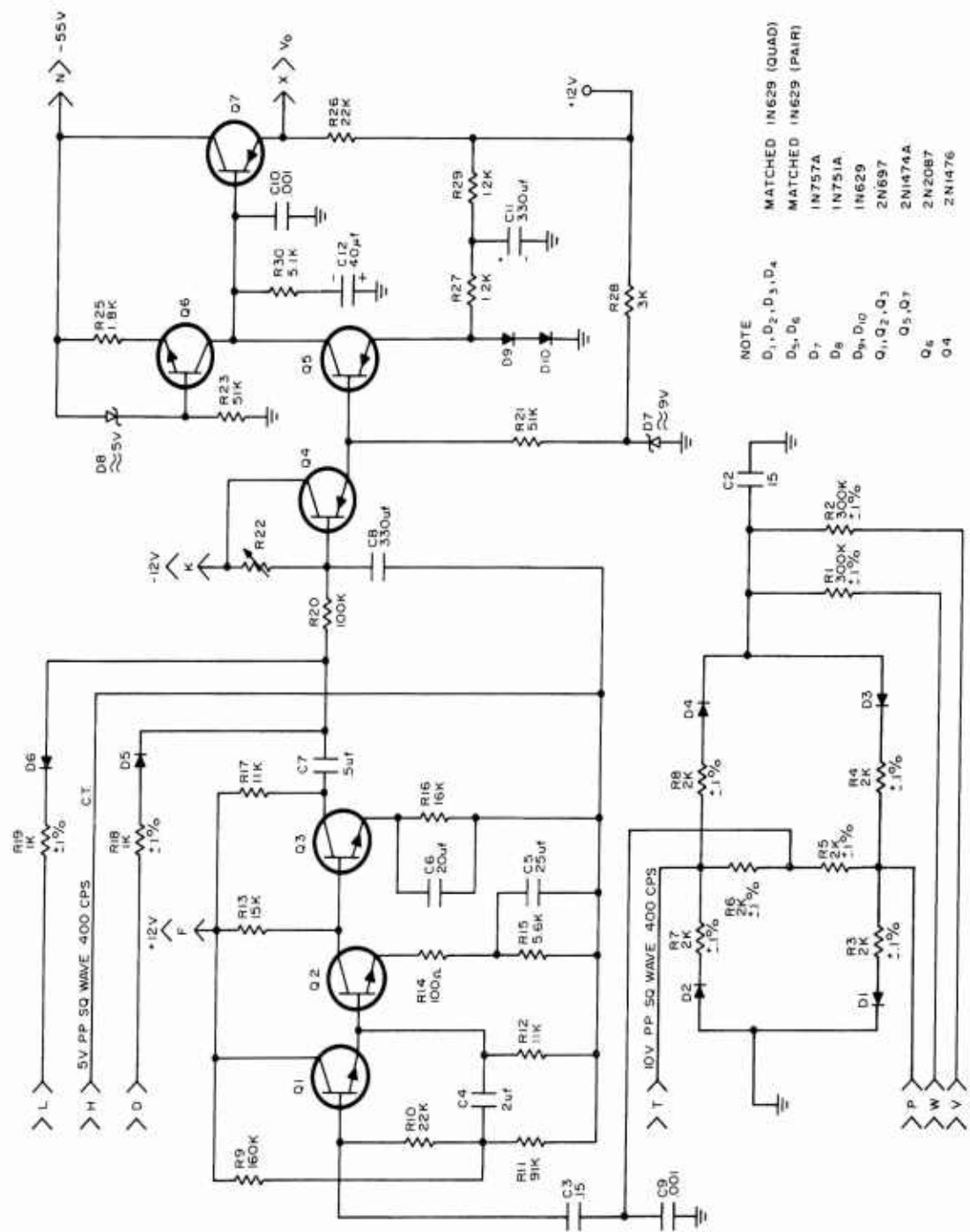


* CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER.
 SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64

** ADJUST TO PRODUCE VOLTAGE GAIN OF 2.14 V/V FROM I-MEG. INPUTS.

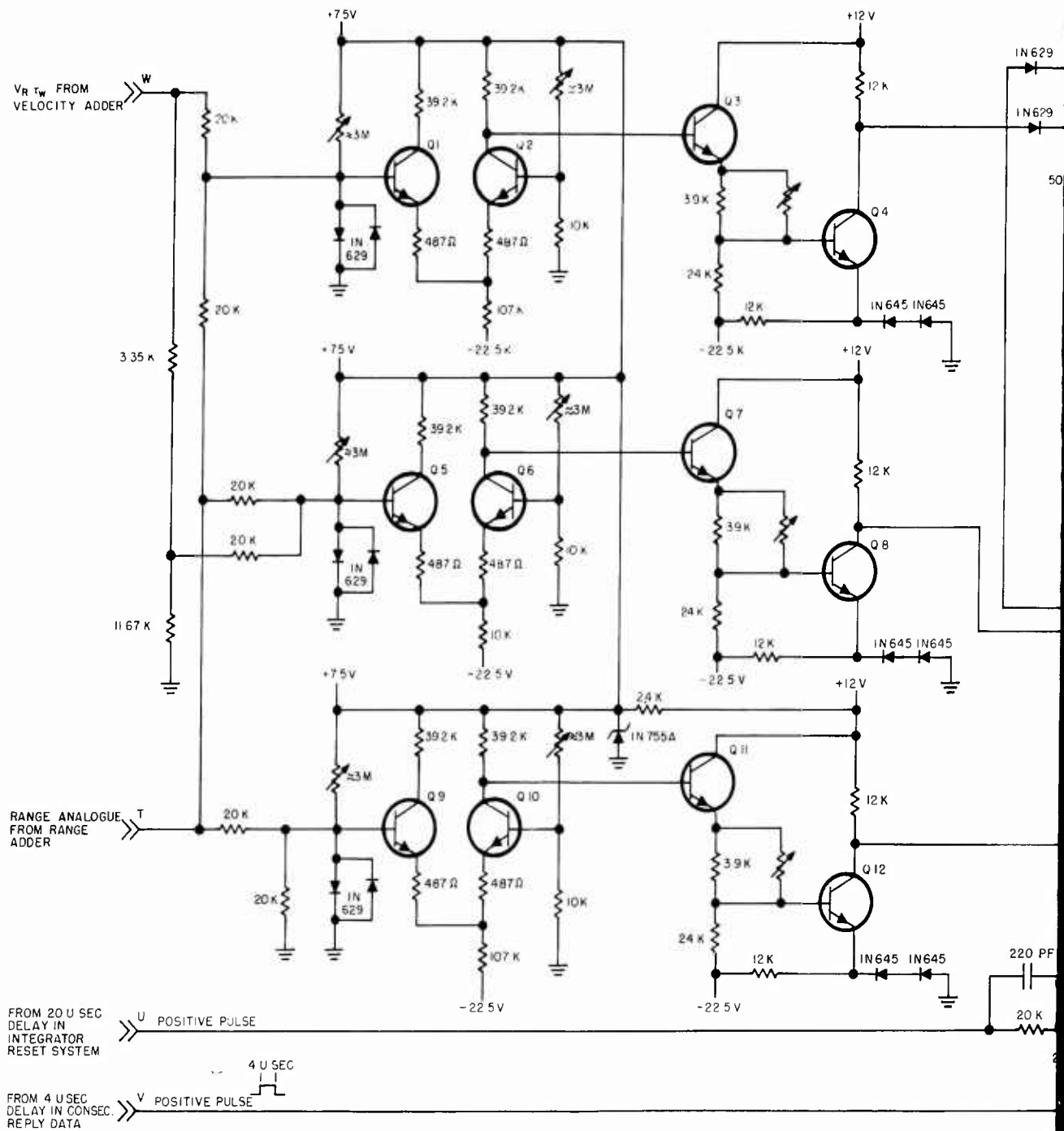
*** ADJUST LIMIT VOLTAGE $\approx 0.15 \text{ V/K}\Omega$

FIGURE 5-47. A-10 RANGE ADDER

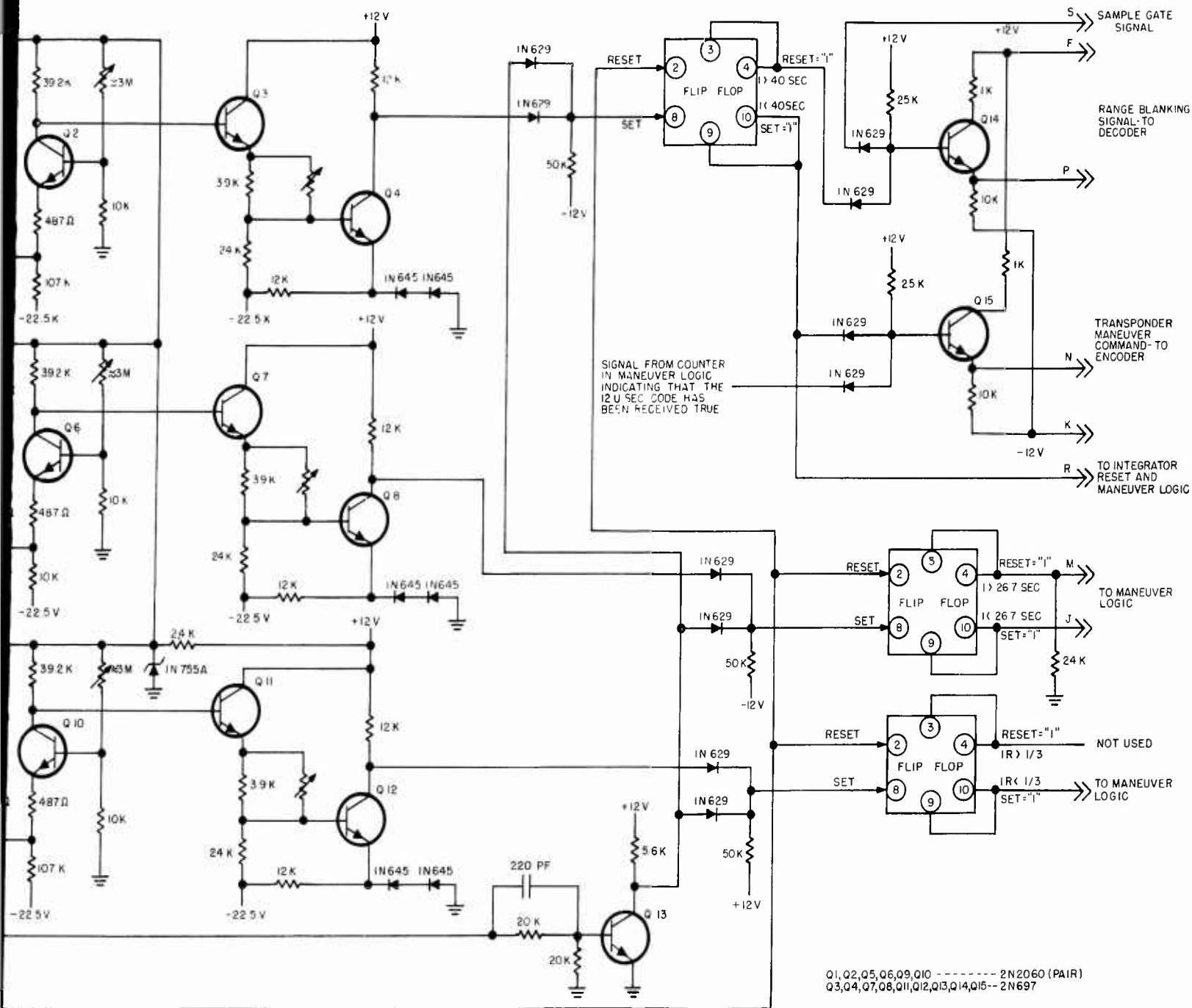


NOTE
 D₁, D₂, D₃, D₄ MATCHED IN629 (QUAD)
 D₅, D₆ MATCHED IN629 (PAIR)
 D₇ IN757A
 D₈ IN751A
 D₉, D₁₀ IN629
 Q₁, Q₂, Q₃ 2N697
 Q₅, Q₇ 2N1474A
 Q₆ 2N2087
 Q₄ 2N1476

FIGURE 5-48. A-11 POWER AMPLIFIER INVERTING (INTERROGATOR)



1



2

FIGURE 5-49
 A-12 RANGE CRITERION COMPARATORS

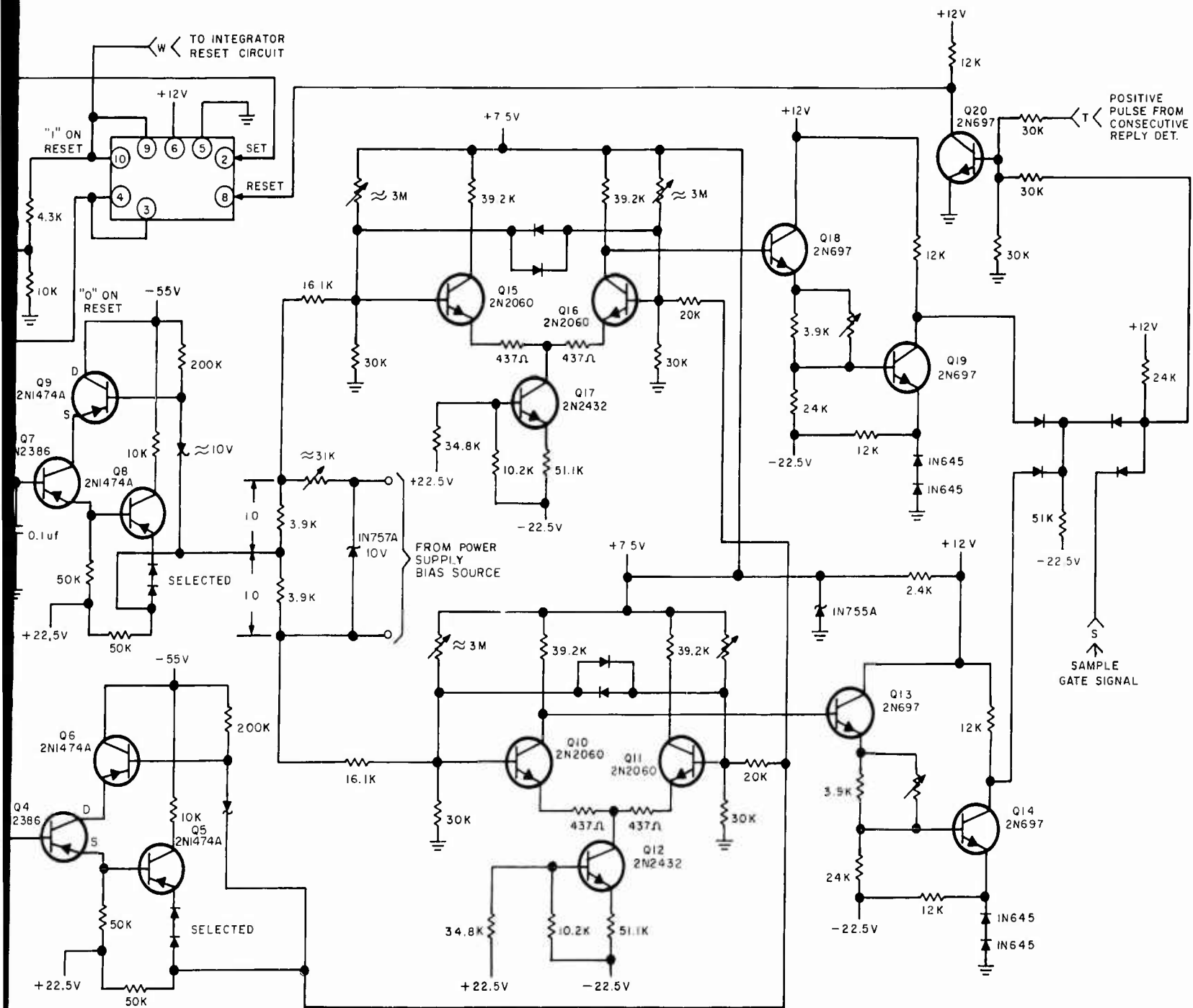


FIGURE 5-50
A-13 RANGE INCREMENT DETECTOR

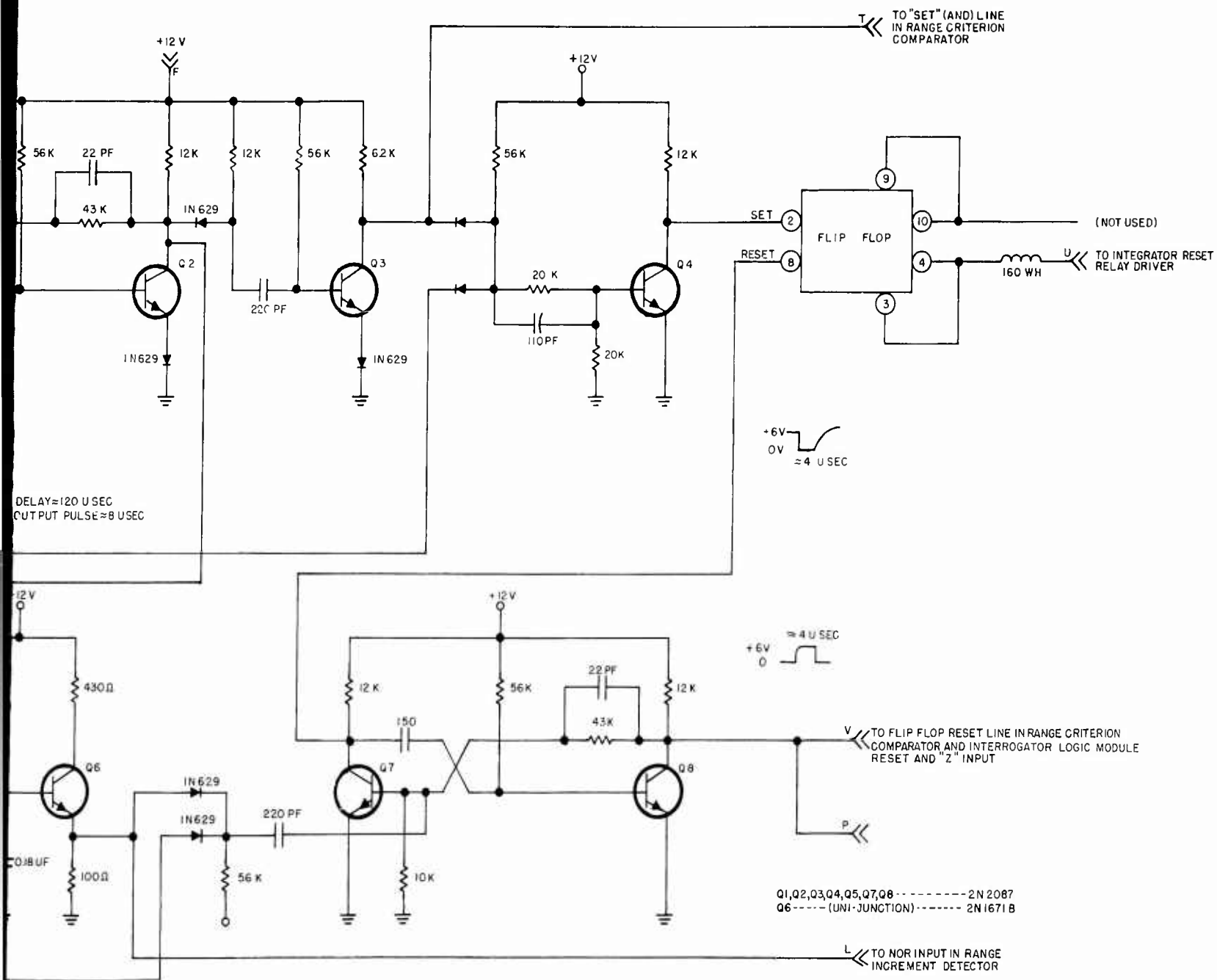
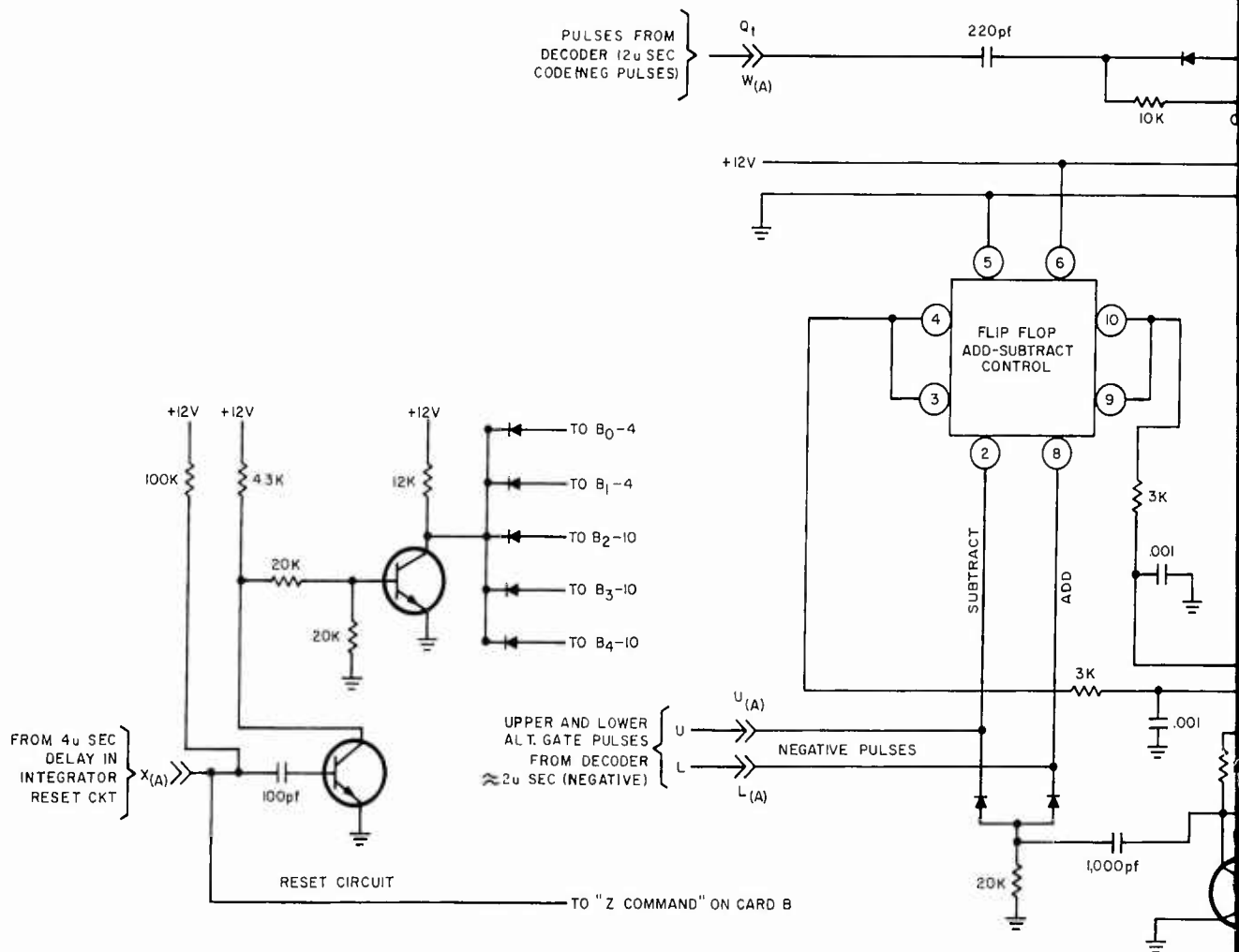
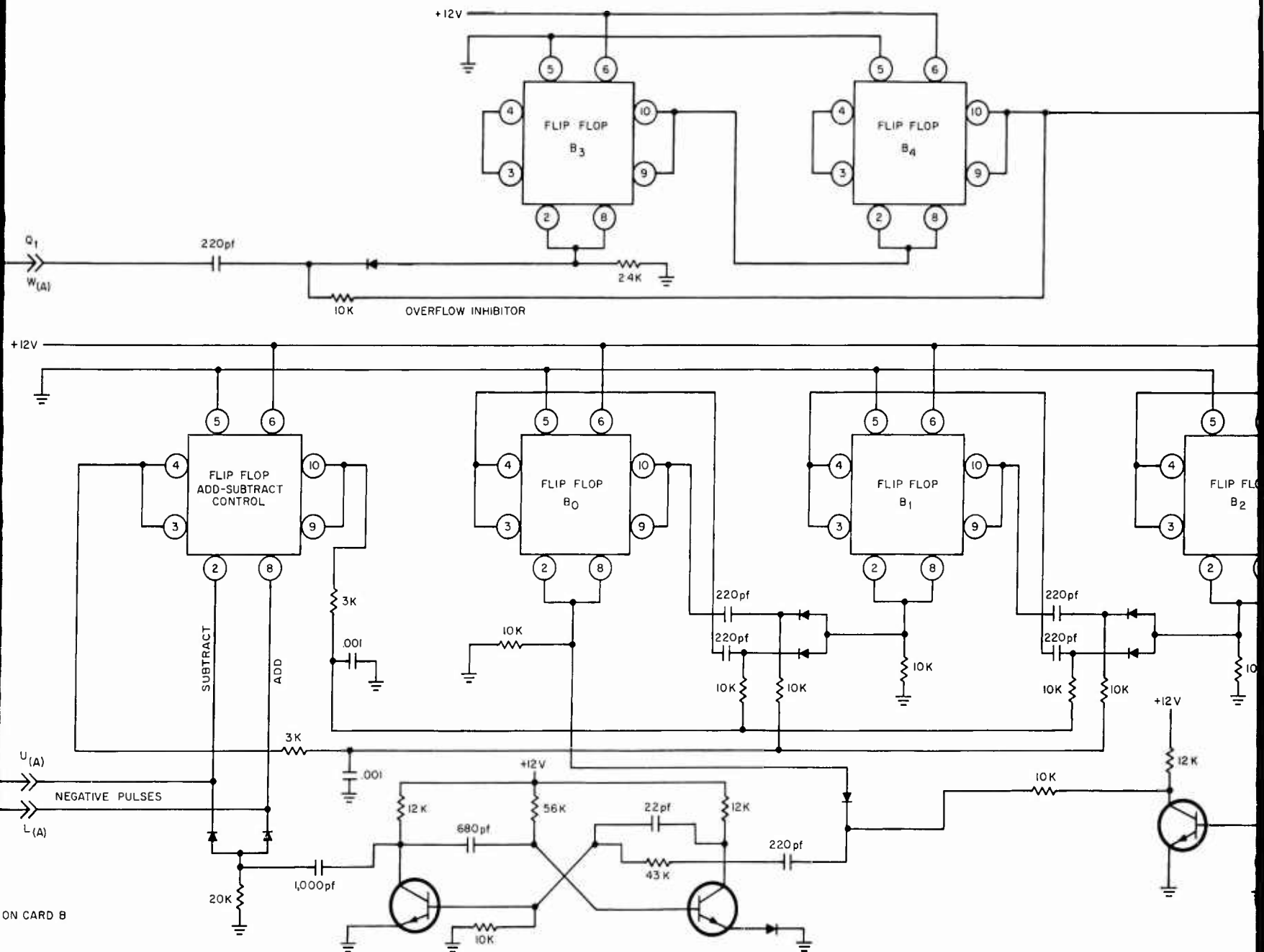


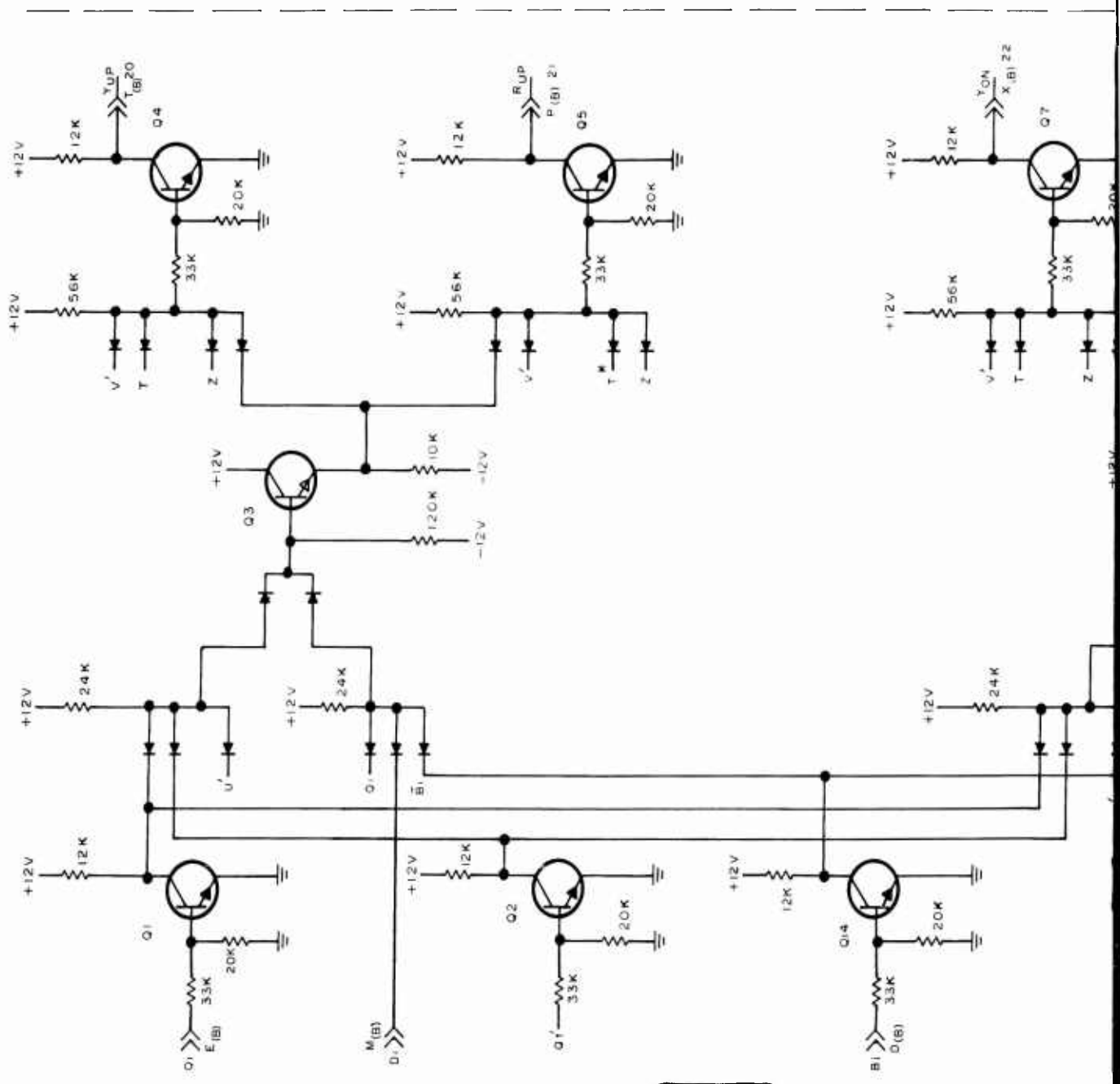
FIGURE 5-51
 A-14 INTEGRATOR RESET AND CONSECUTIVE
 REPLY DETECTOR



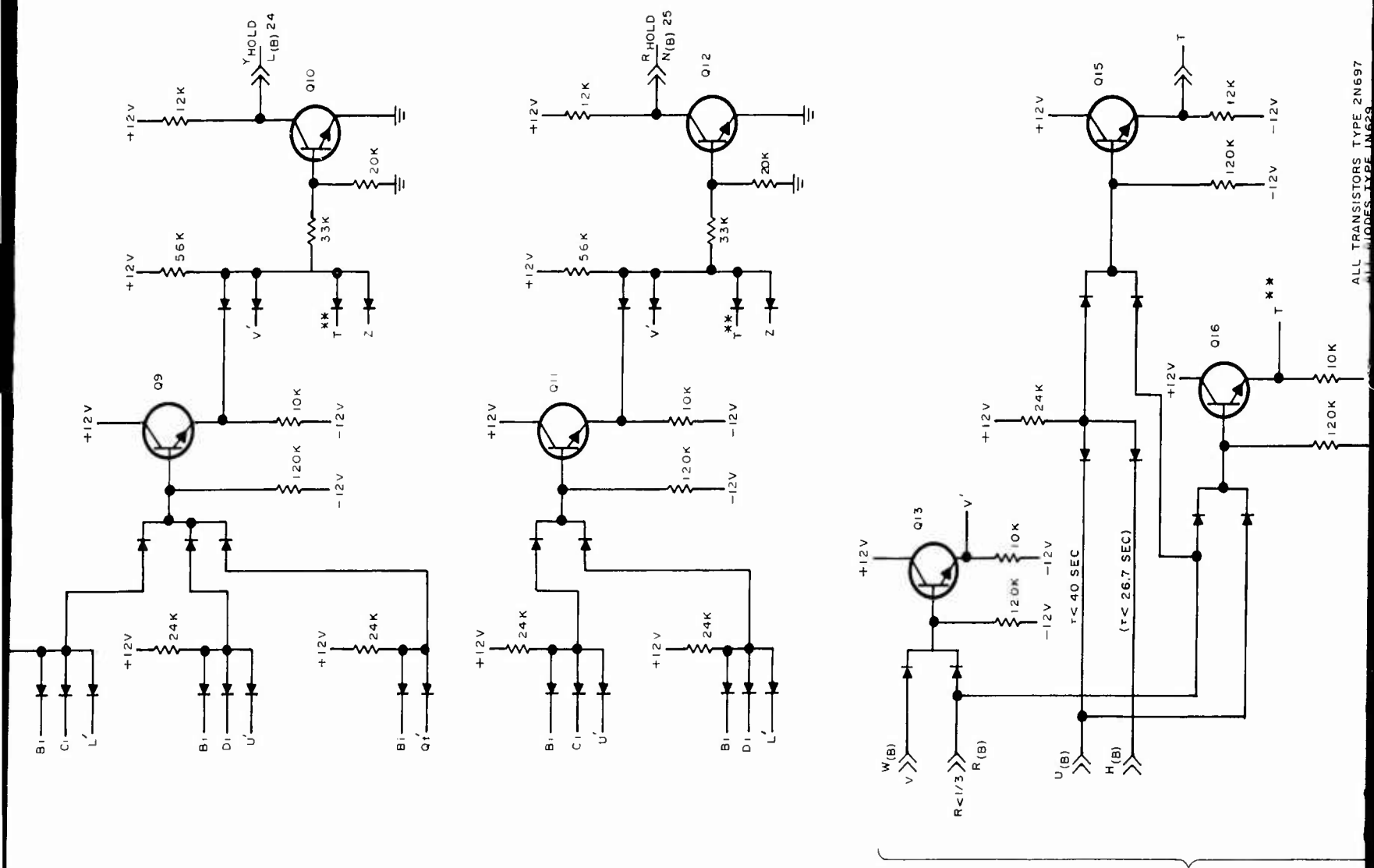
1



2



1

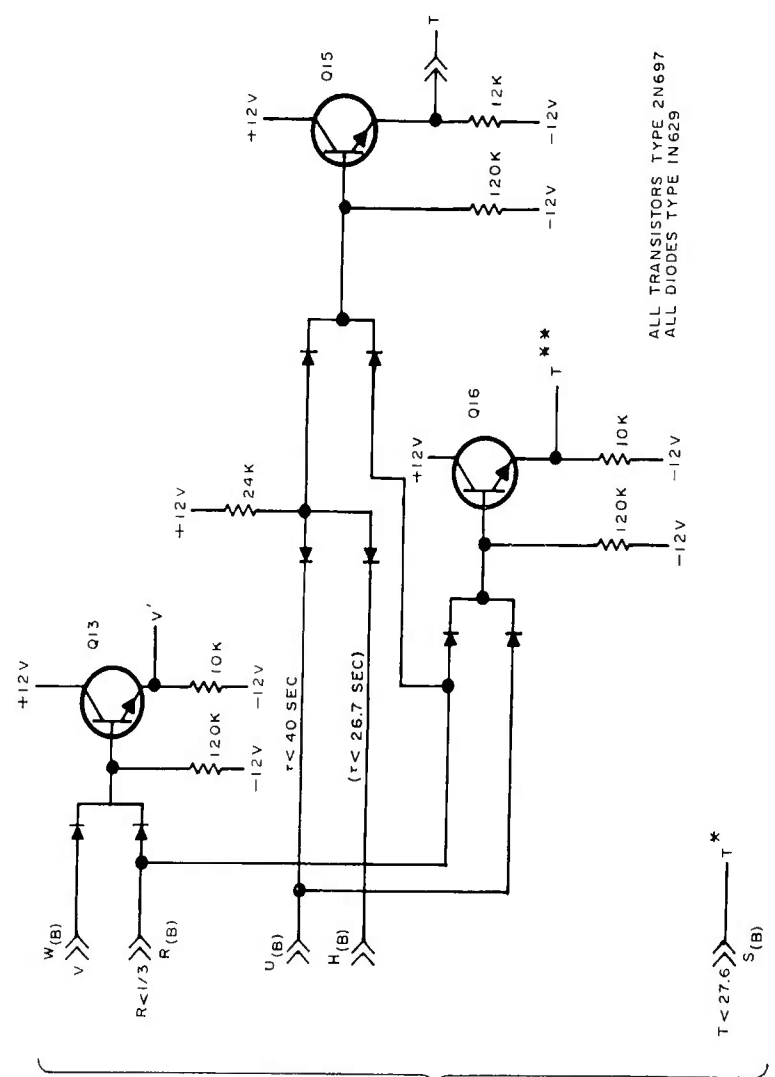
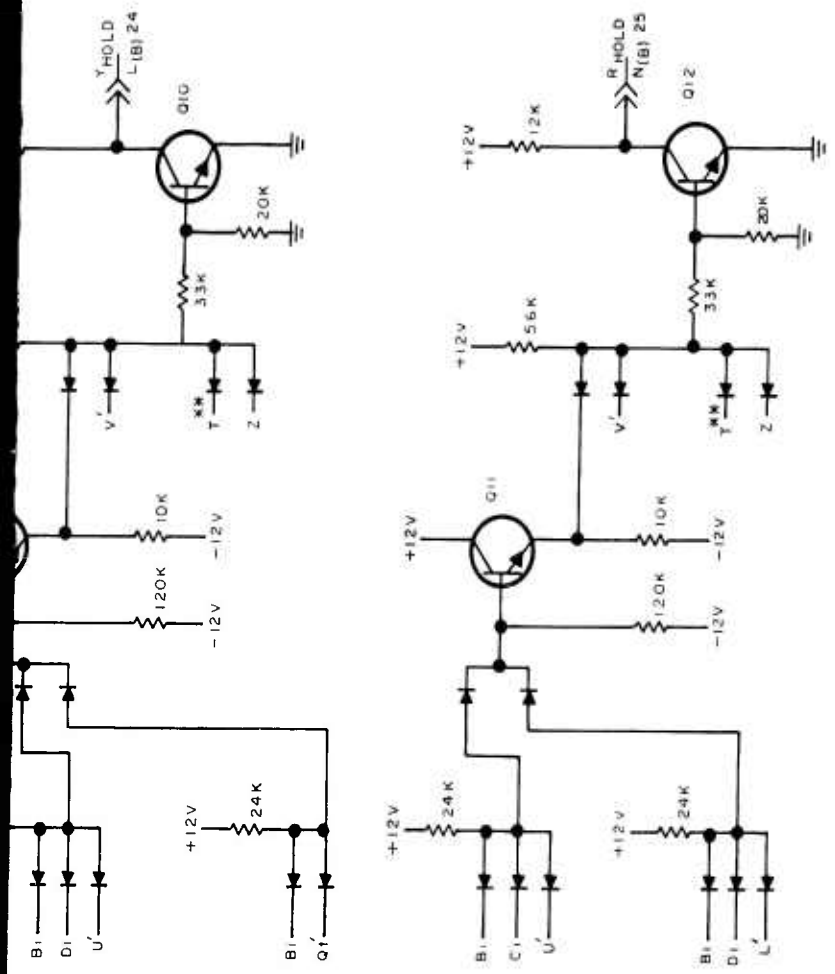


COLLISION CRITERION COMPUTER

3

FIGURE 5-52
A-15 INTERROGATOR MANEUVER LOGIC (SH

ALL TRANSISTORS TYPE 2N697
ALL DIODES TYPE 1N623

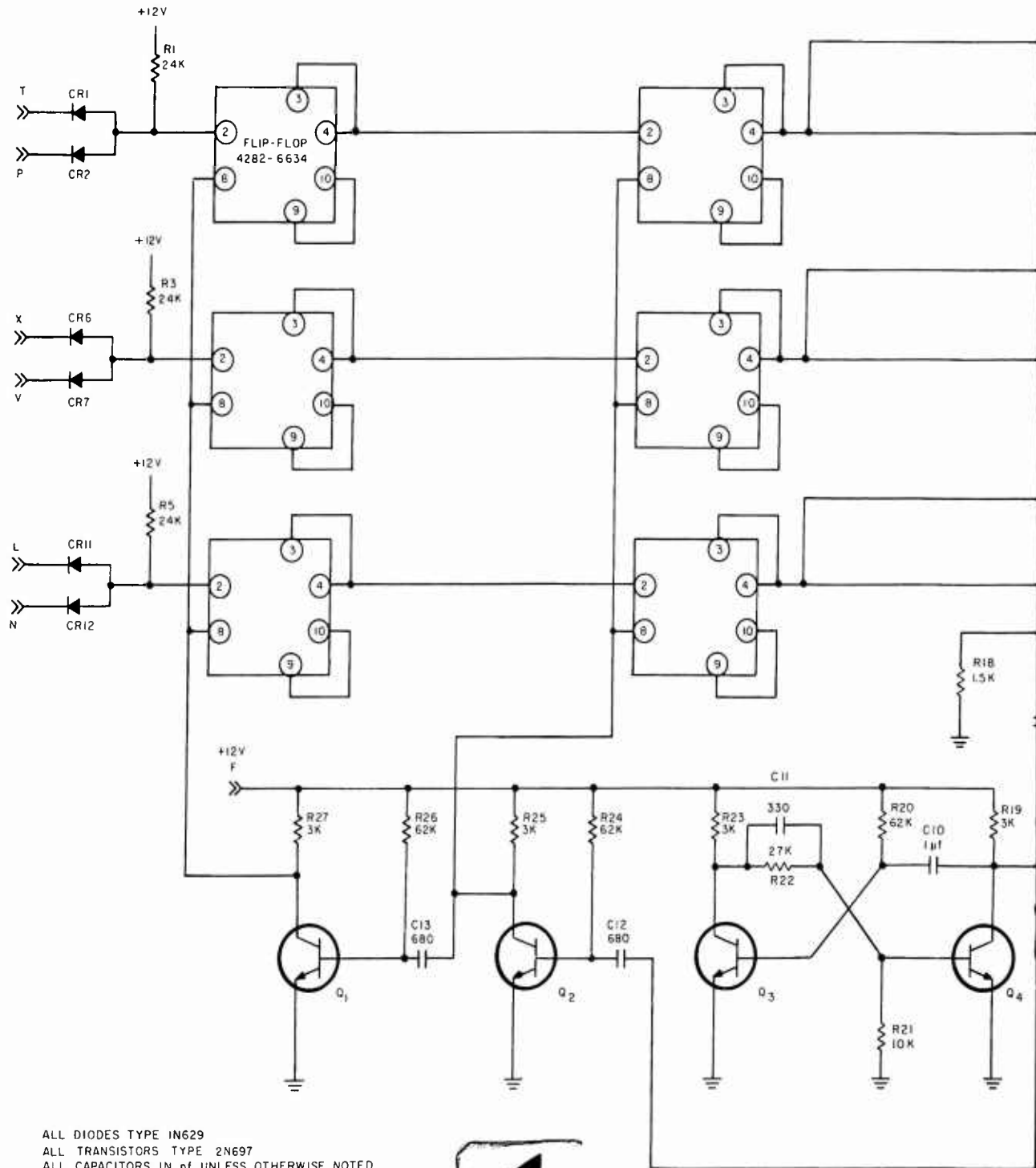


ALL TRANSISTORS TYPE 2N697
ALL DIODES TYPE IN629

COLLISION CRITERION COMPUTER

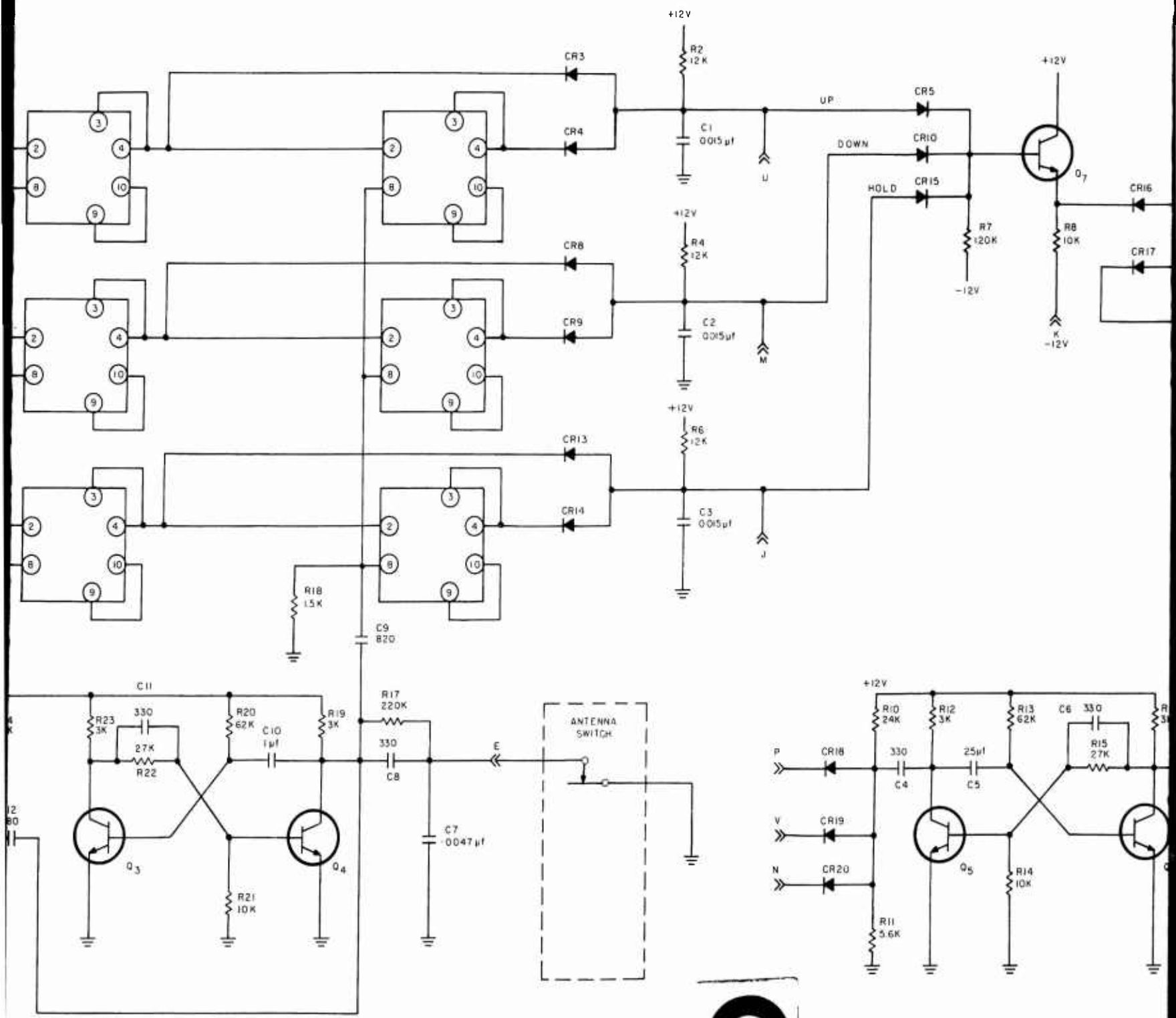
FIGURE 5-52
A-15 INTERROGATOR MANEUVER LOGIC (SHEET 2 OF 2)

4



ALL DIODES TYPE 1N629
 ALL TRANSISTORS TYPE 2N697
 ALL CAPACITORS IN pf UNLESS OTHERWISE NOTED





2

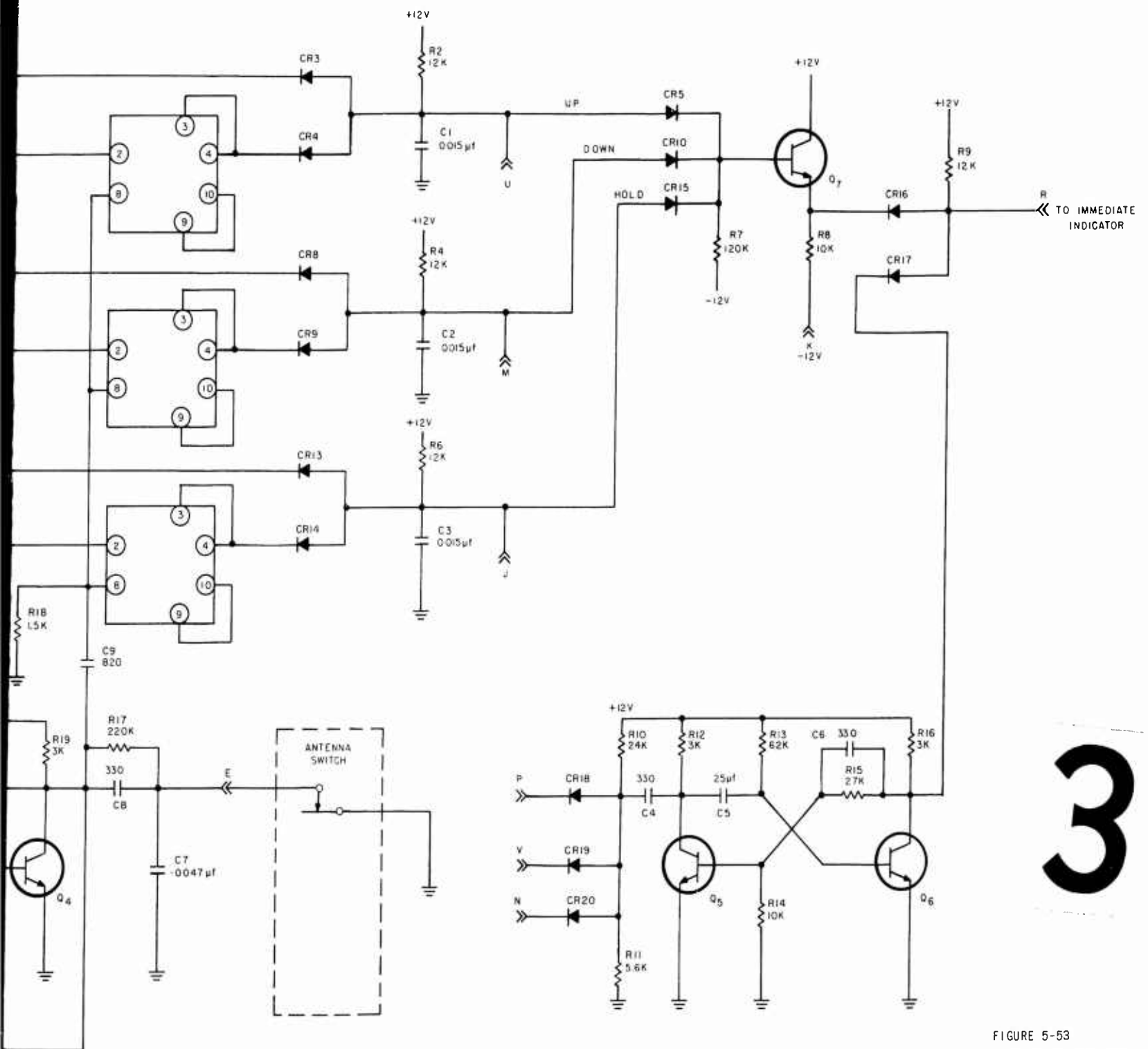


FIGURE 5-53

A-16 INTERROGATOR SCAN MEMORY

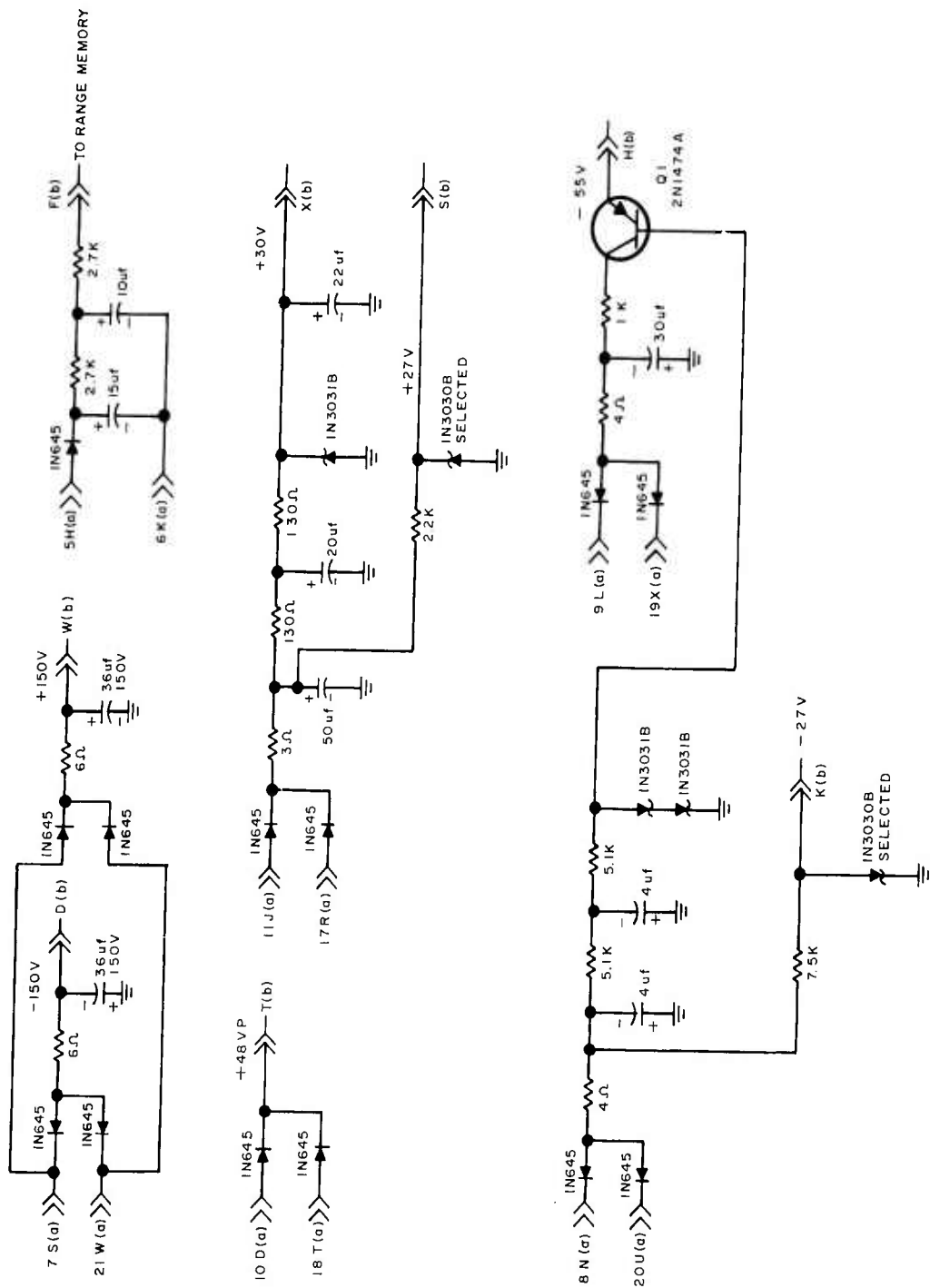


FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 1 OF 3)

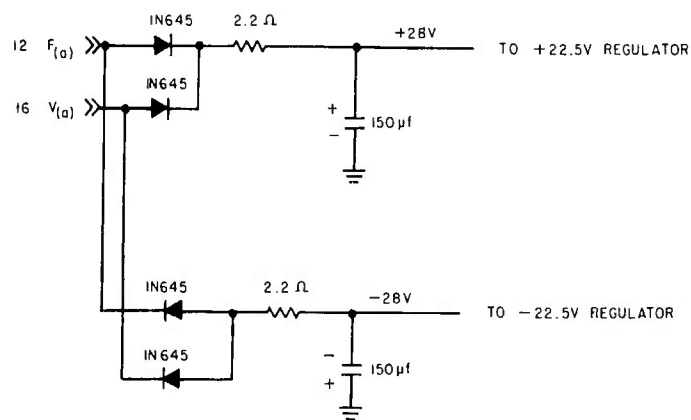
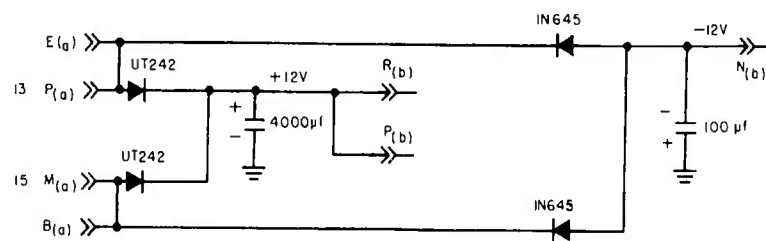
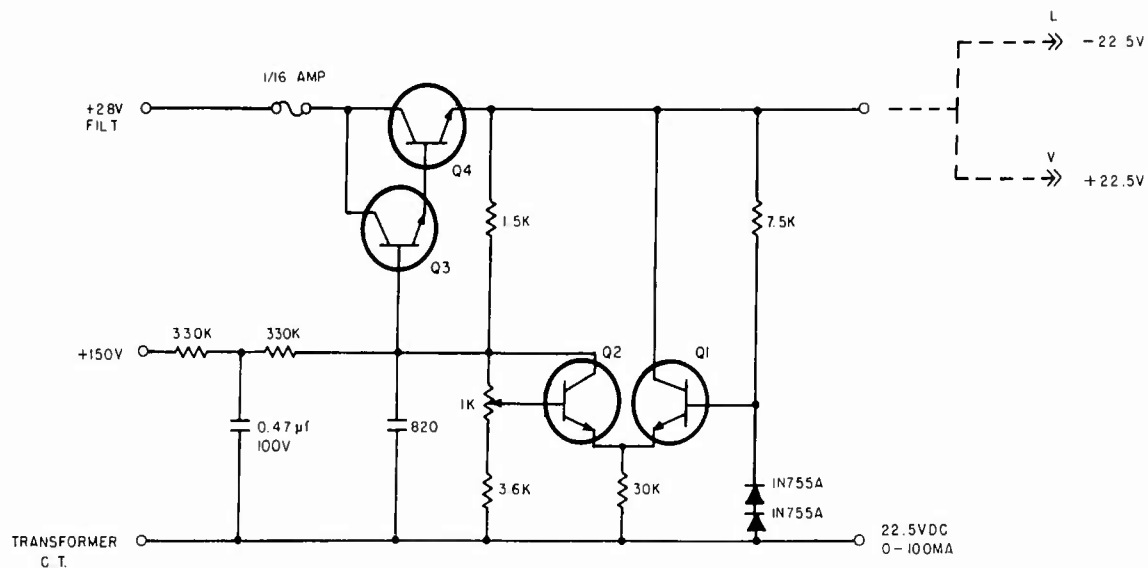


FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 2 OF 3)



NOTE: FOR +22.5V SUPPLY THE TRANSISTORS TO BE USED ARE AS GIVEN BELOW AND THE CONNECTIONS ARE AS SHOWN ABOVE.

Q₁, Q₂ — — — — 2N33B
 Q₃, Q₄ — — — — 2N697

FOR THE -22.5V SUPPLY THE TRANSISTORS TO BE USED ARE AS GIVEN BELOW, THE DIODES ARE REVERSED AND THE UN-REGULATED SUPPLIES ARE -28V AND -150V

Q₁, Q₂, Q₃, Q₄ — — — — 2N1474A

FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 3 OF 3)

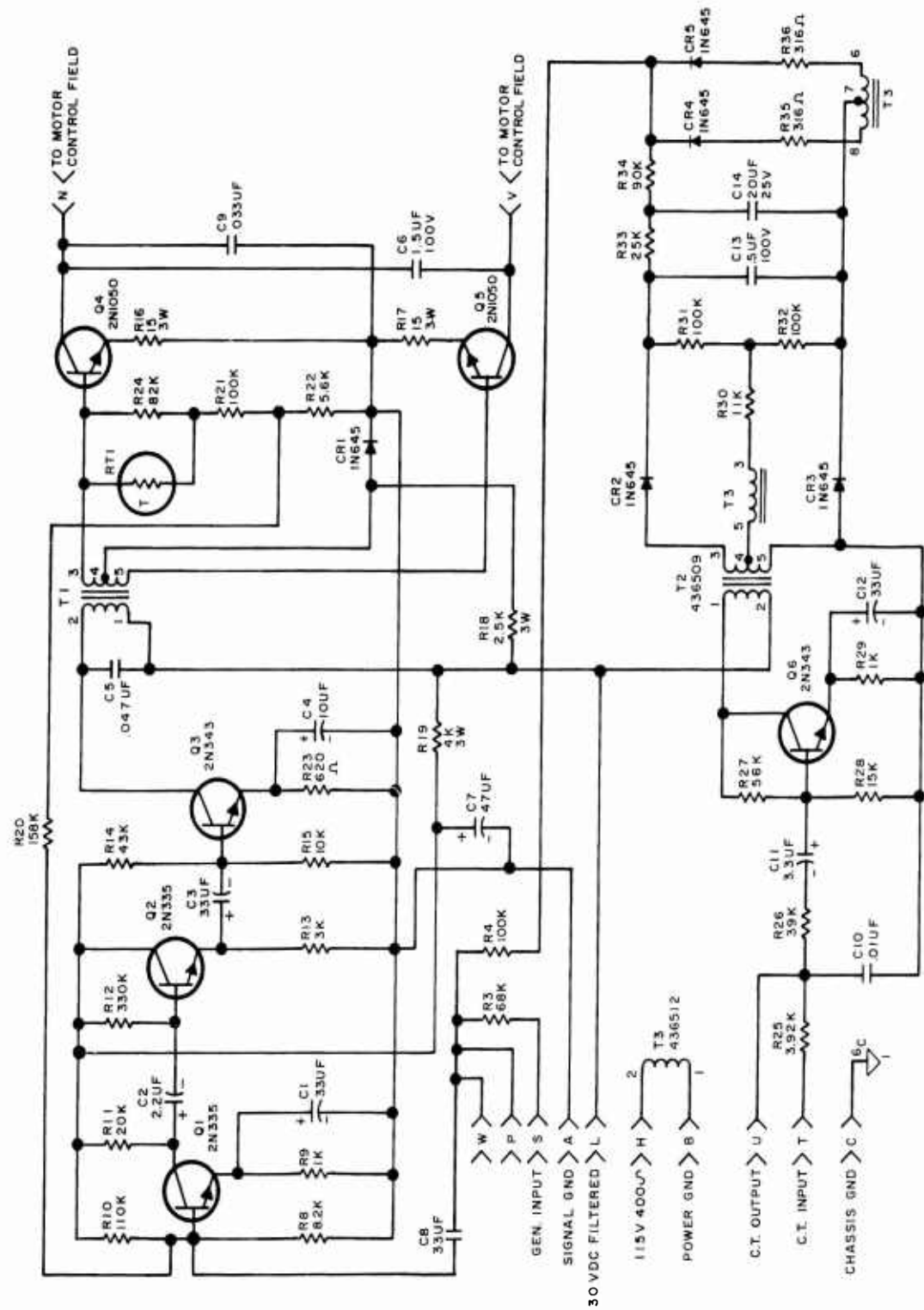


FIGURE 5-55. A-18 HEADING MOTOR AMPLIFIER (3)

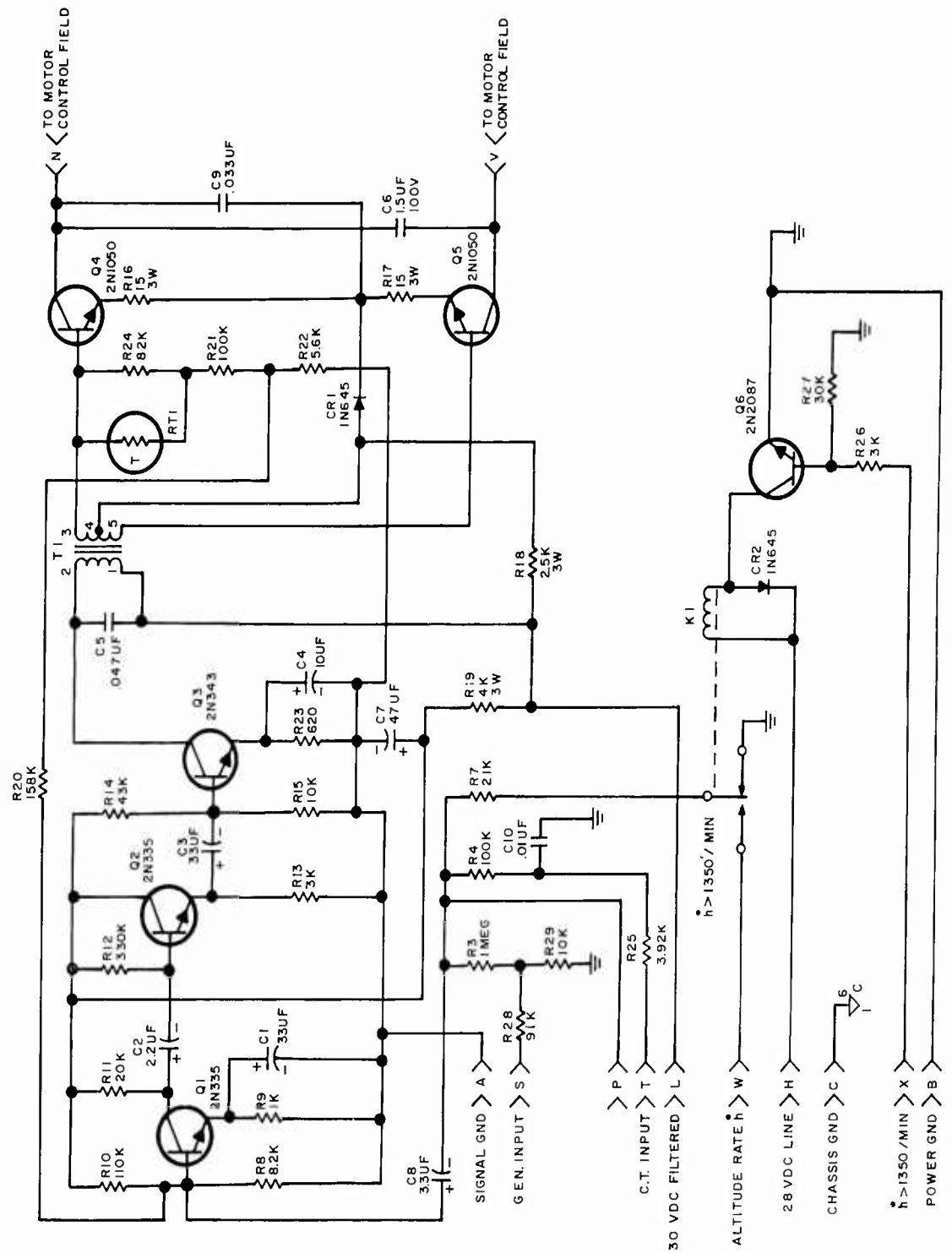


FIGURE 5-56. A-19 ALTITUDE MOTOR AMPLIFIER (h)

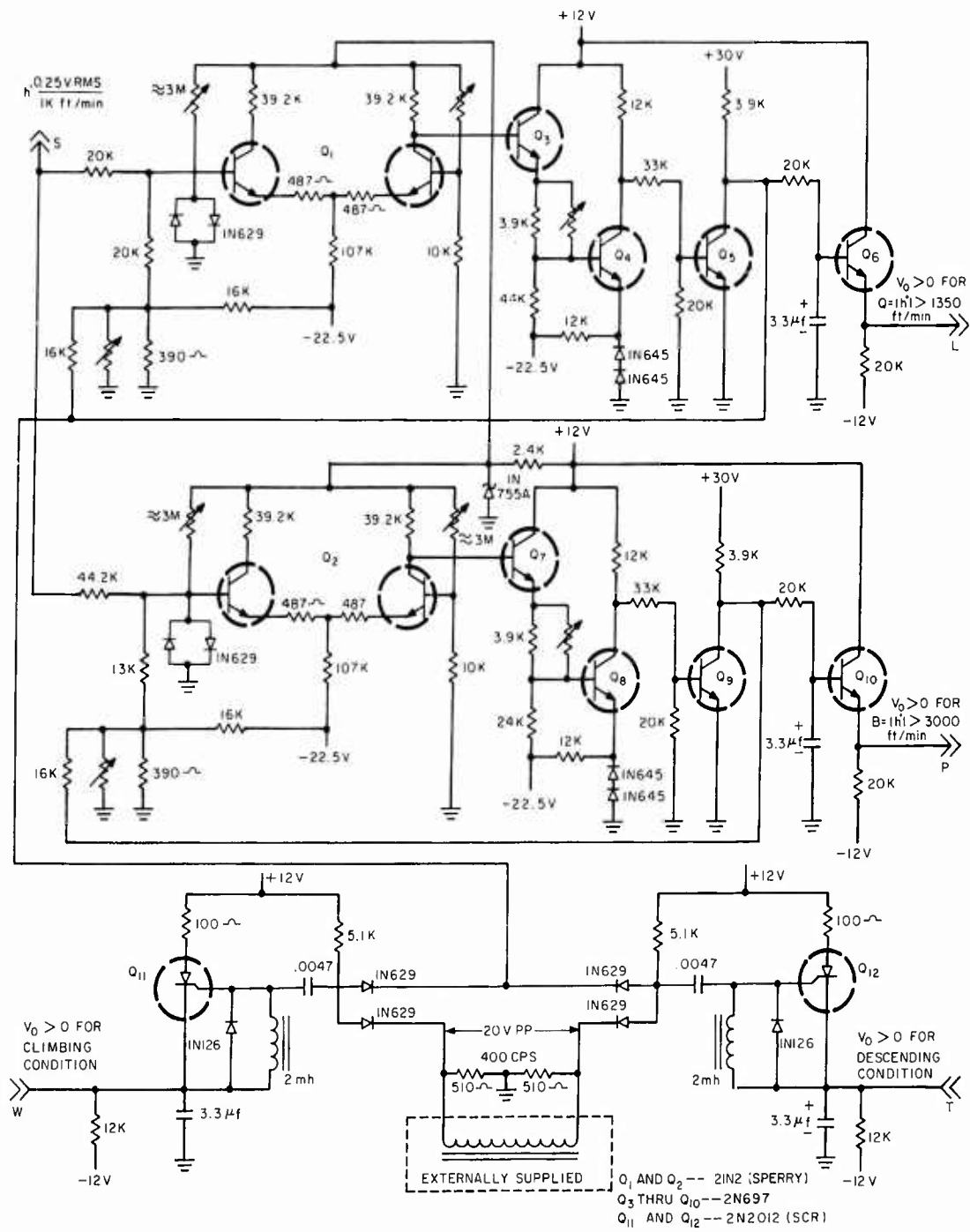
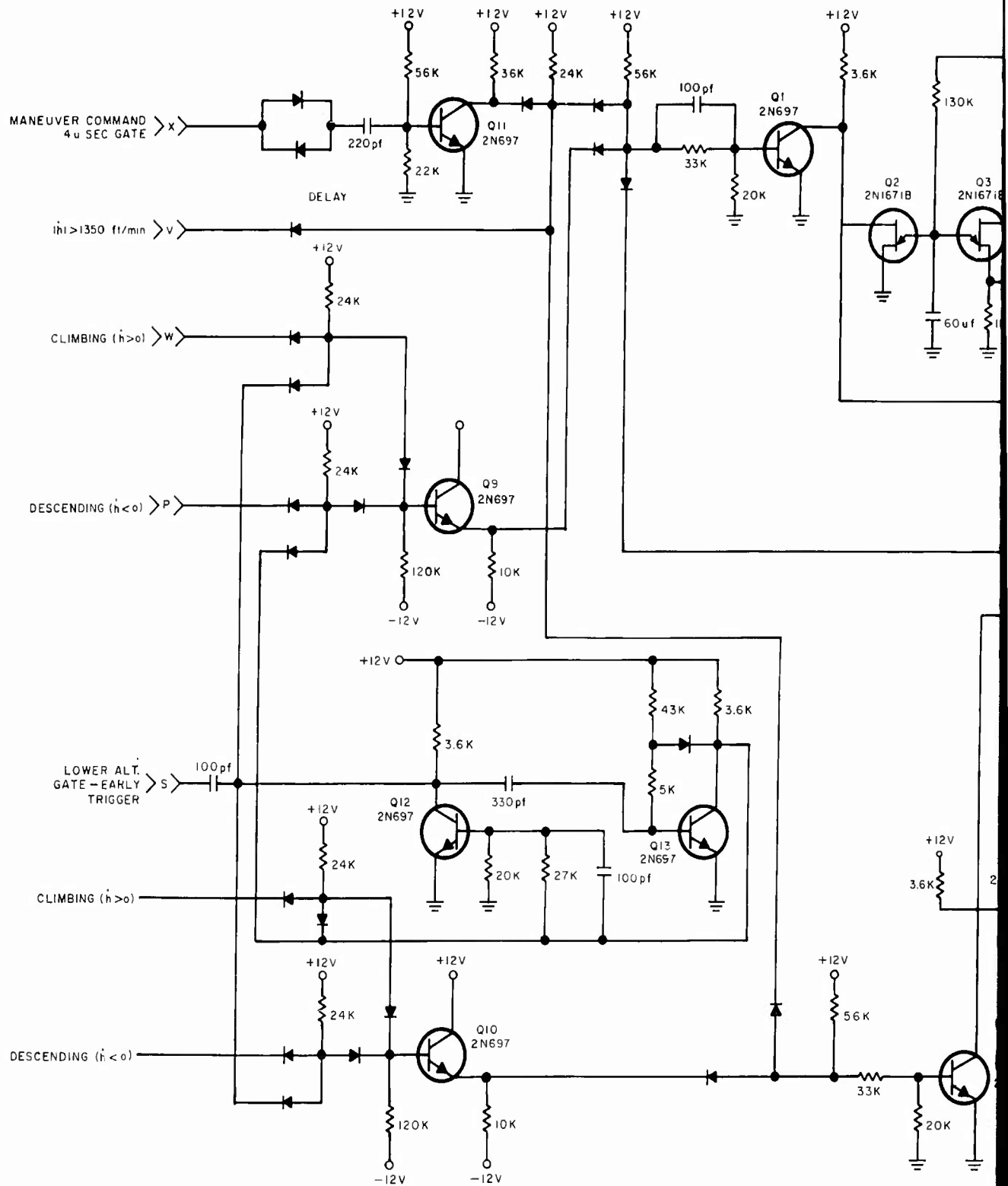
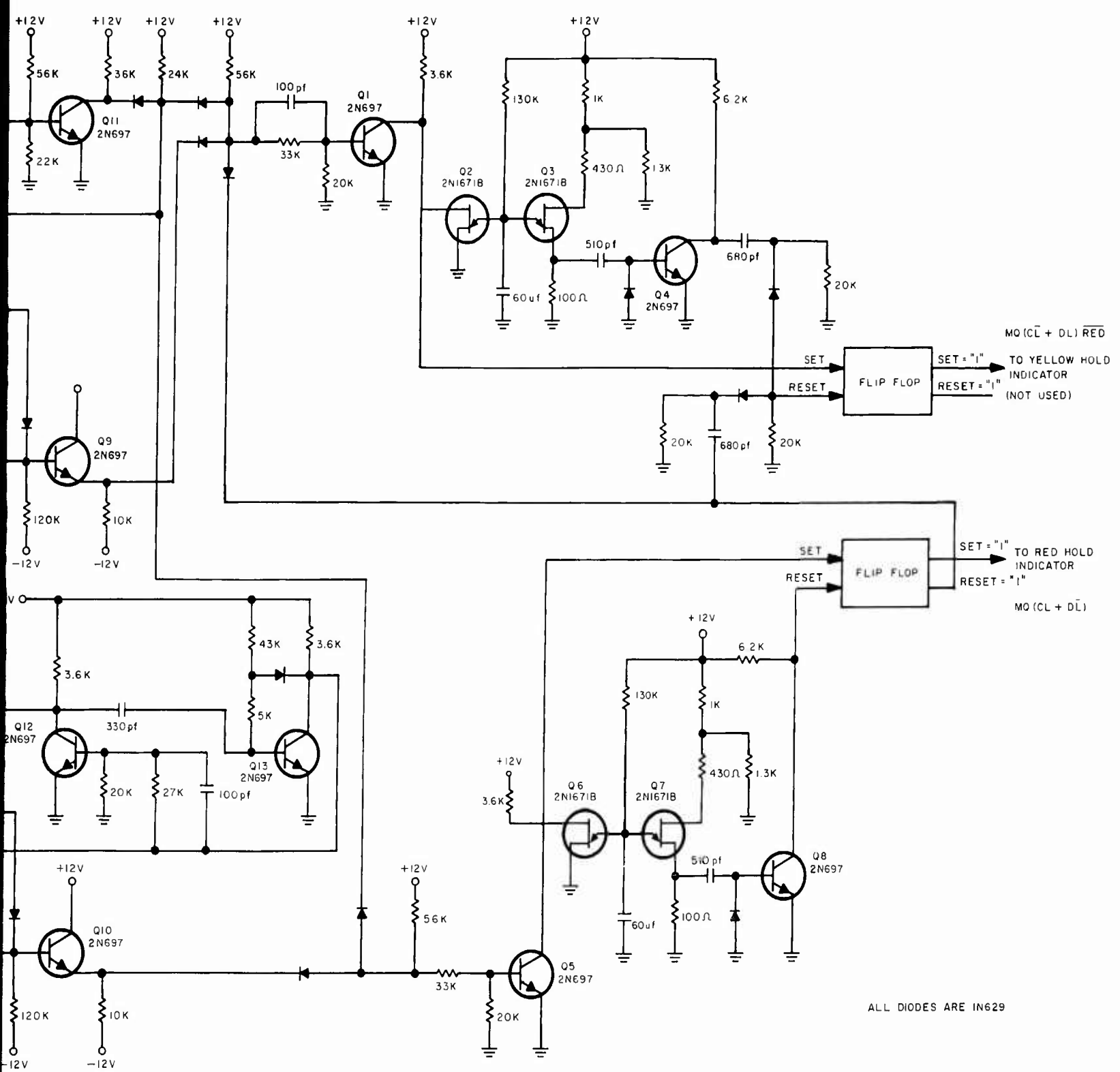


FIGURE 5-57
A-20 CLIMB RATE DETECTOR



1



ALL DIODES ARE IN629



FIGURE 5-58
A-21 TRANSPONDER MANEUVER LOGIC

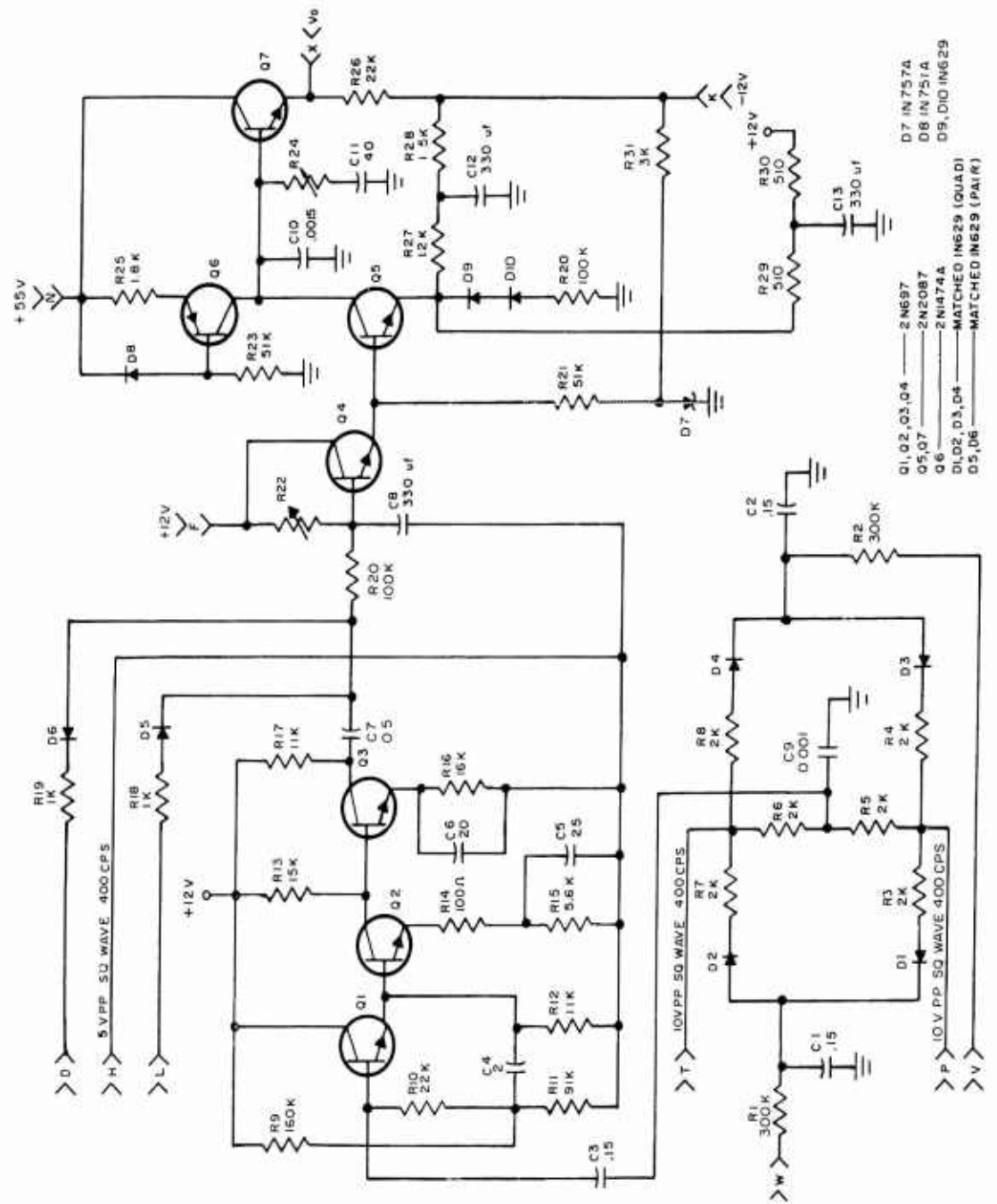


FIGURE 5-59. A 22 POWER AMPLIFIER (NON-INVERTING) (TRANSPONDER)

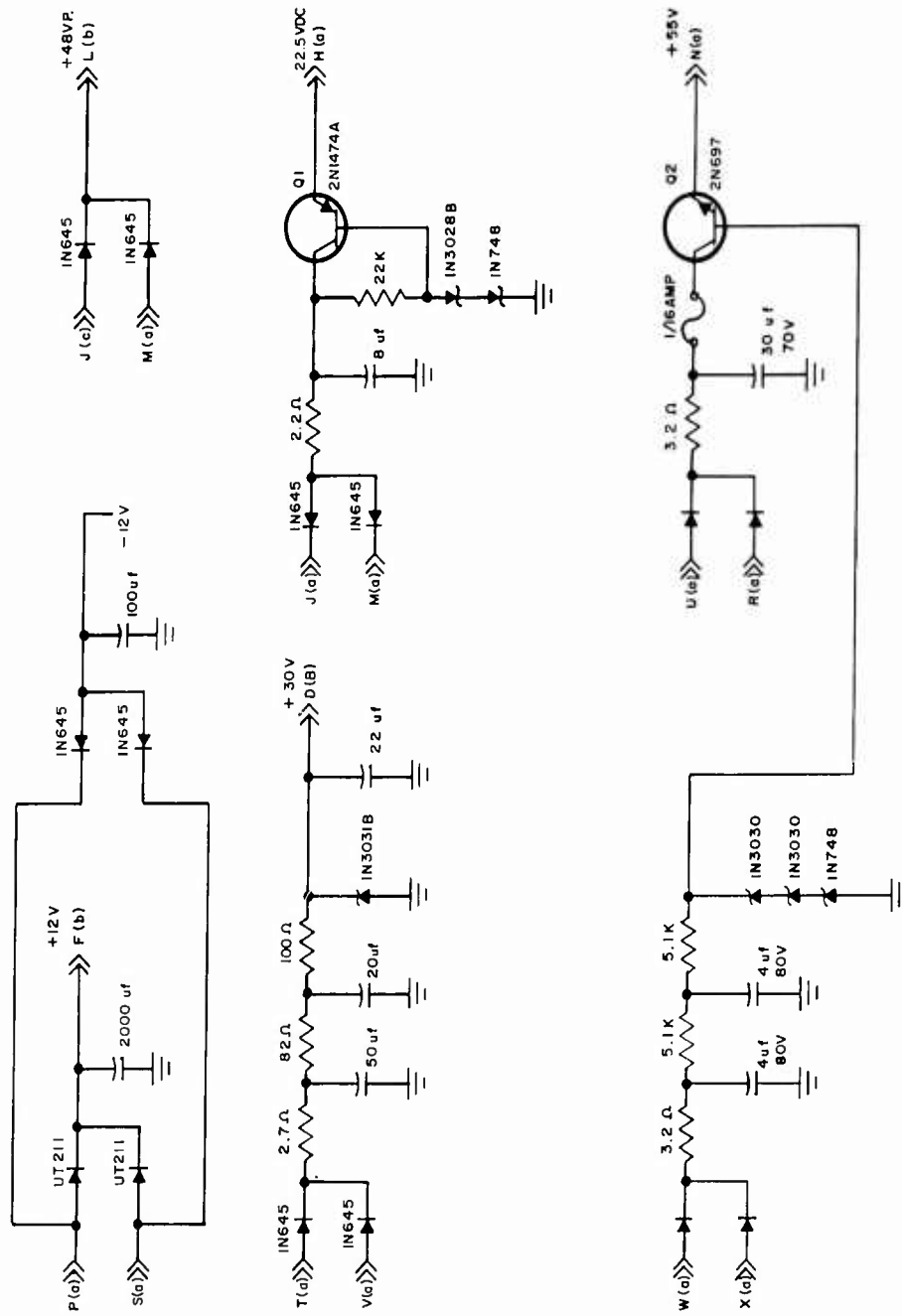
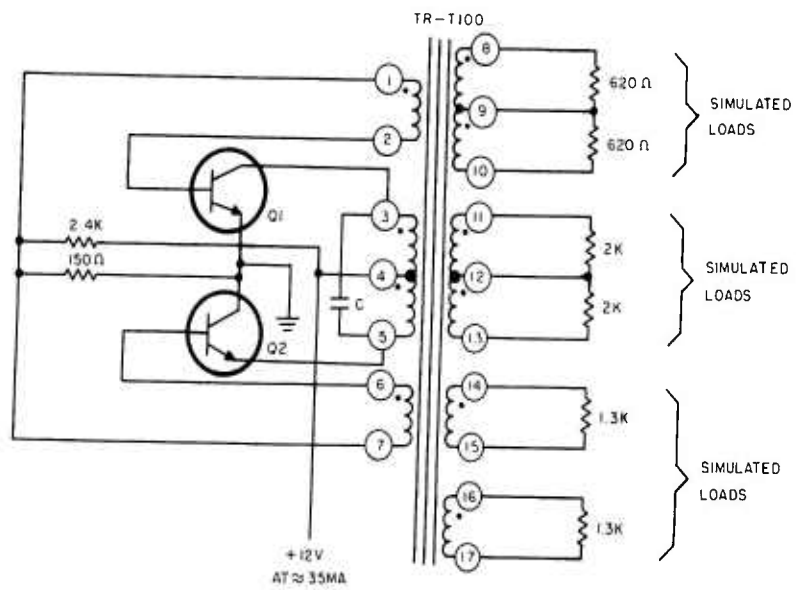


FIGURE 5-60. A-23 TRANSPONDER RECTIFIERS AND REGULATORS (SHEET 1 OF 2)

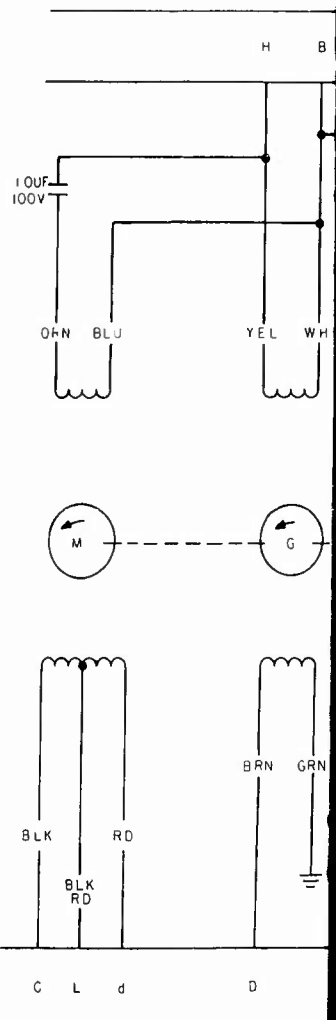
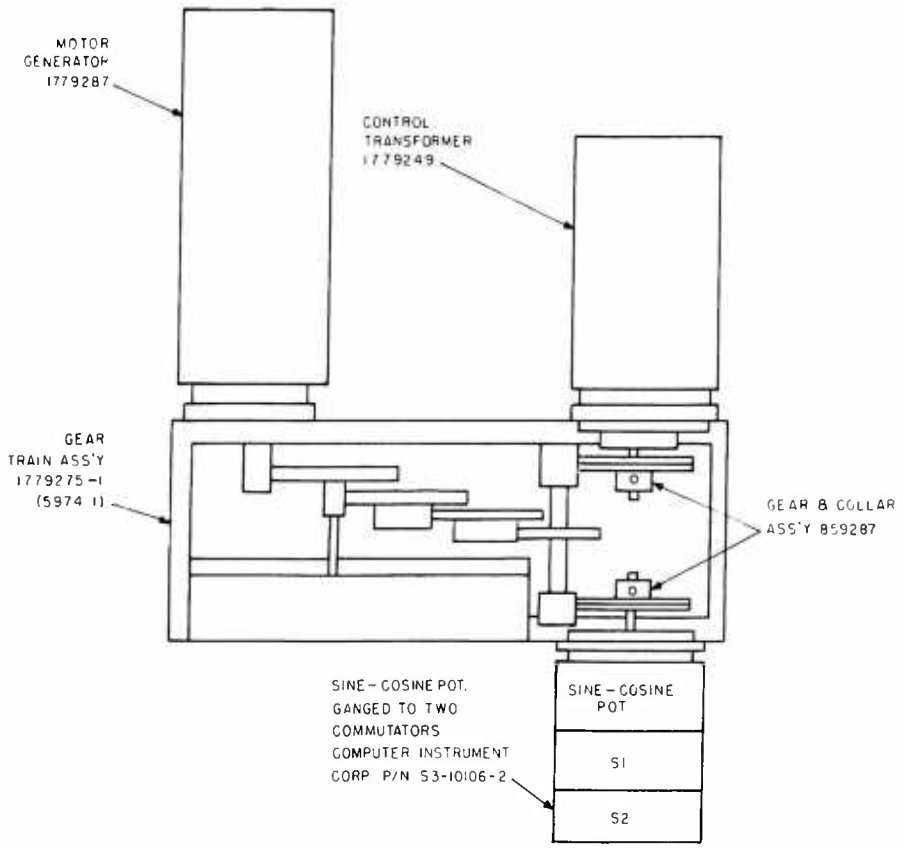


Q₁, Q₂ ——— 2N2087

CAPACITOR "C" IS SELECTED AS REQUIRED

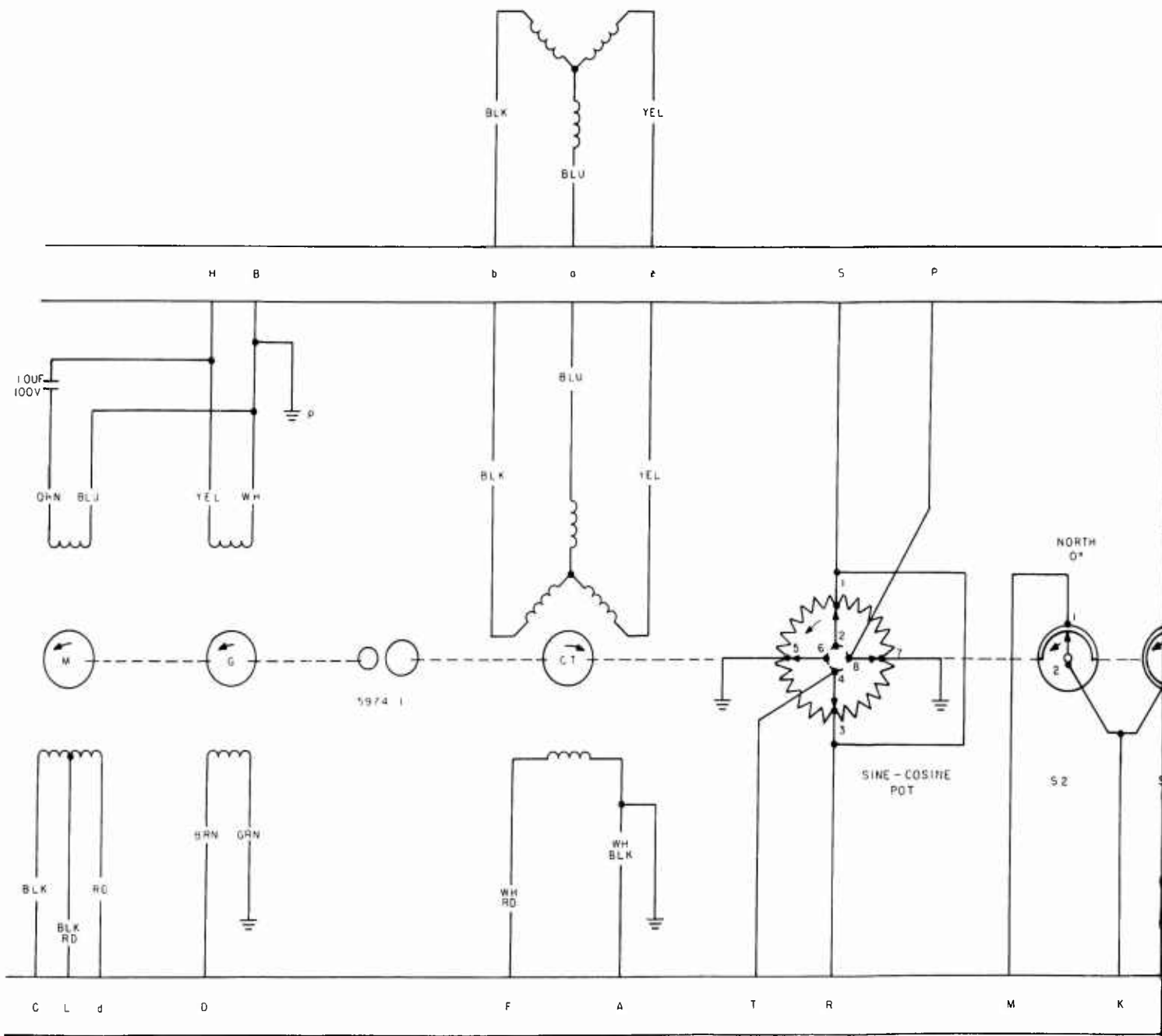
TO REDUCE SPIKES IF NECESSARY

FIGURE 5-60. A-23 TRANSPONDER RECTIFIERS AND REGULATORS (SHEET 2 OF 2)



1

26V 400 \sim + O — RD — KEARFOTT
 — O — BLK — R59114A
 TRANSMITTER

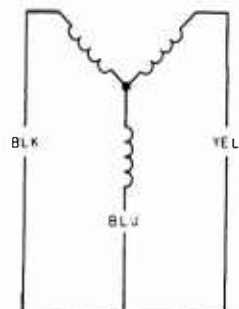


GEAR & COLLAR
 ASS'Y 859287

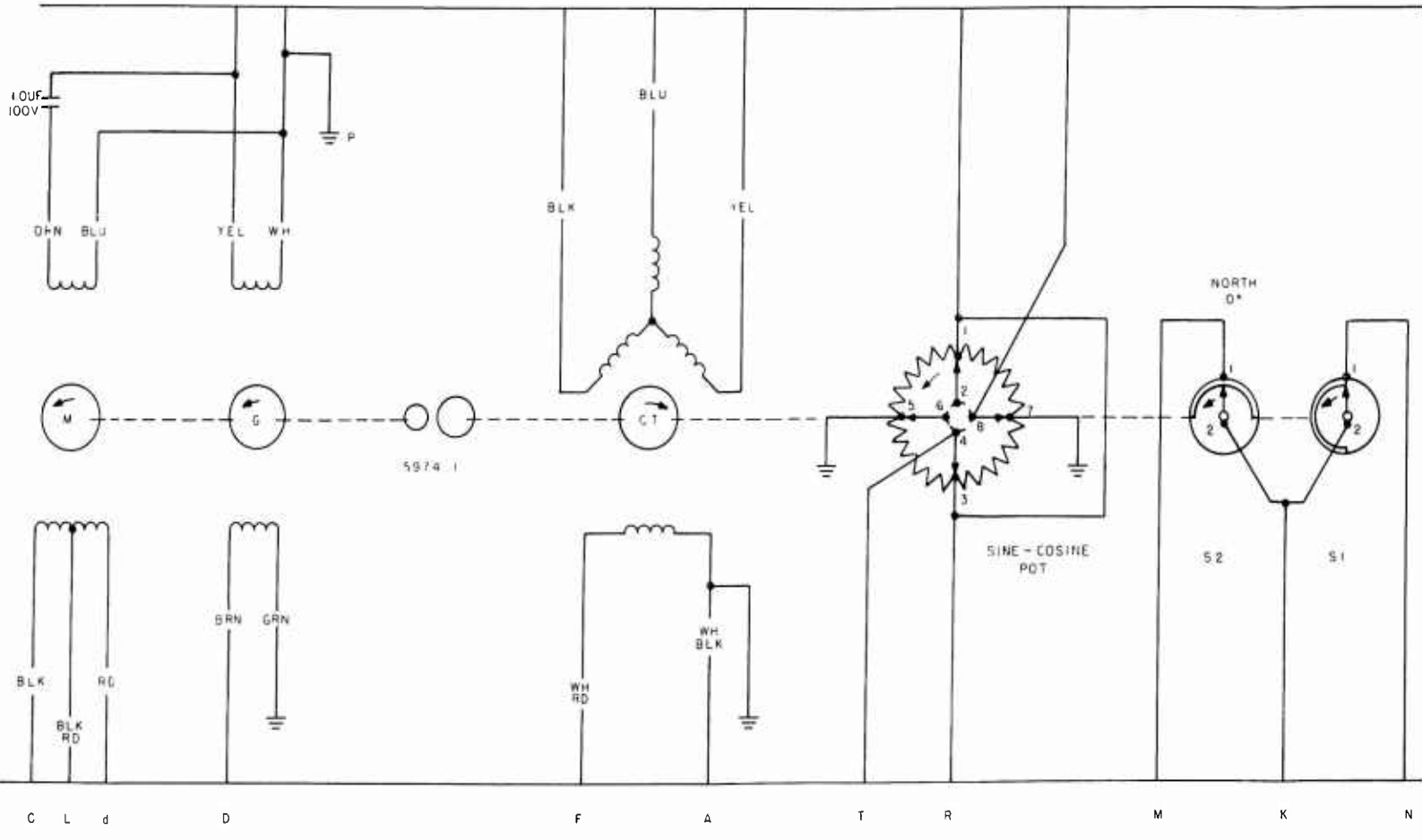
2

FIGURE 5-61
 A-24 HEADING SERVO (a) FOR CAS T

26V 400~ + O RD KEARFOTT
 - O BLK RS9114A
 TRANSMITTER



H B b o z S P



C L d D F A T R M K N

3

FIGURE 5-61
 A-24 HEADING SERVO (α) FOR CAS TRANSPONDER

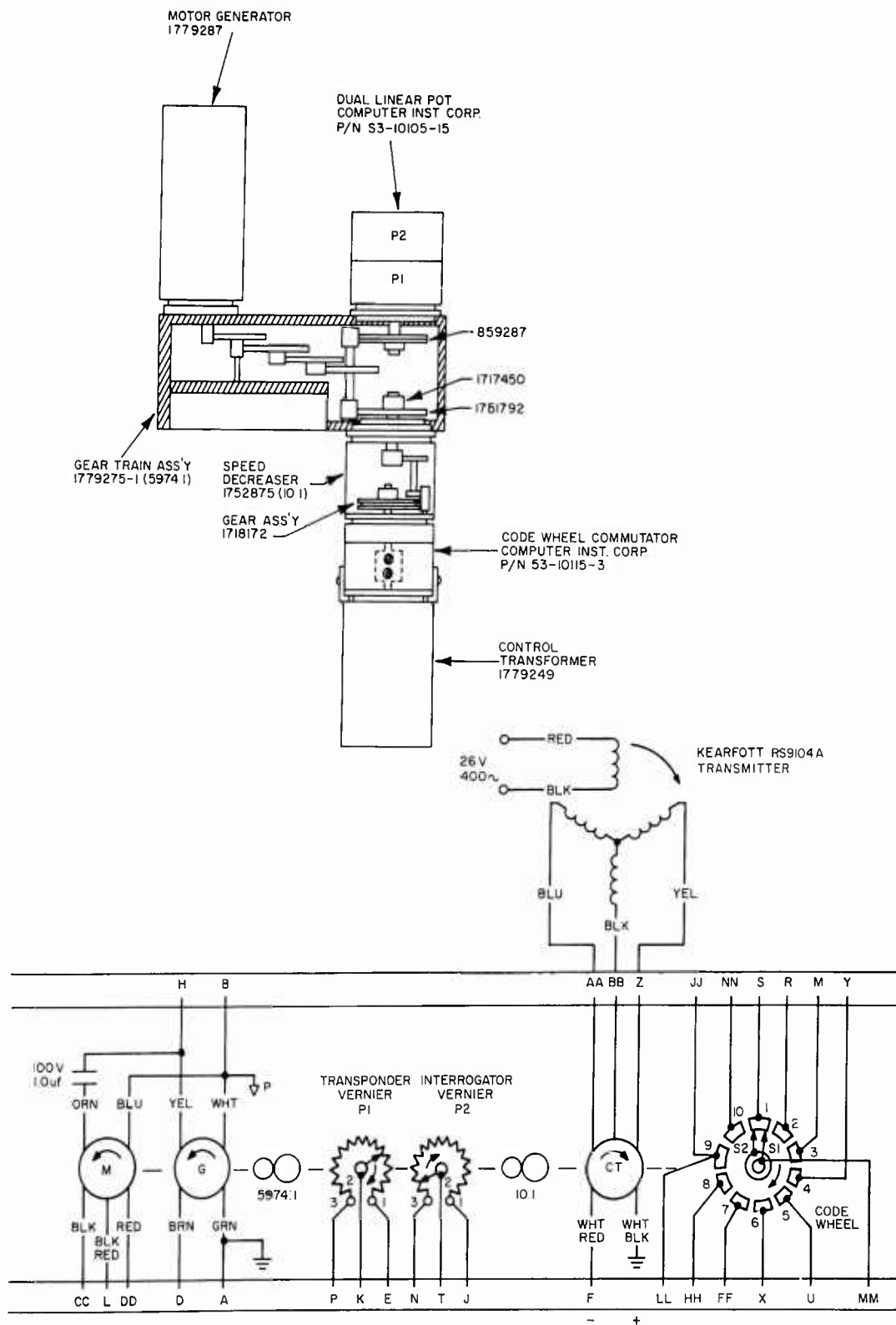
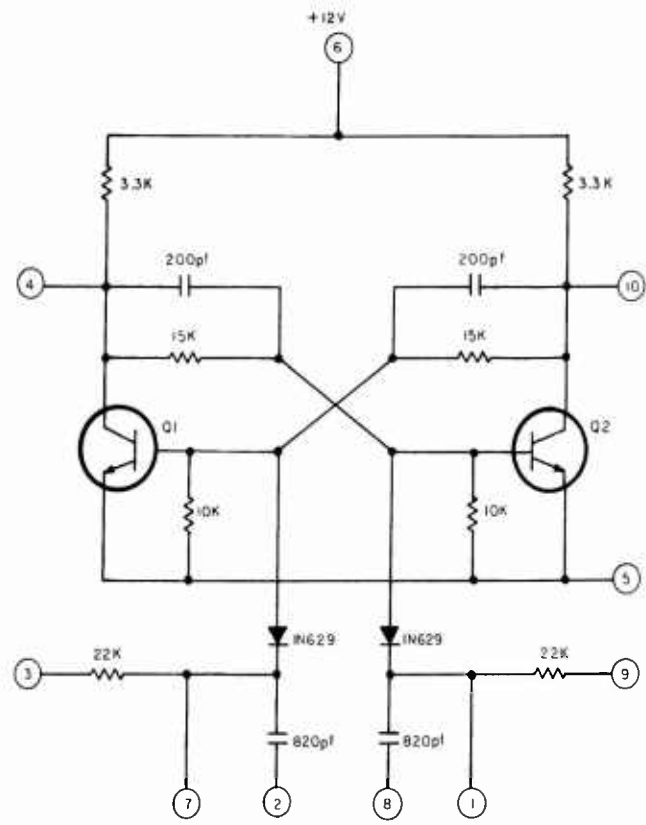


FIGURE 5-62 A-25 ALTITUDE SERVO (h) FOR CAS TRANSPONDER COMPUTER

1	2	3	4	
o	o	o	o	
		5	6	PIN LAYOUT
		o	o	
7	8	9	10	
o	o	o	o	



Q₁, Q₂ — — — — 2N706

FIGURE 5-63. SATURATED FLIP-FLOP PN4282-6634

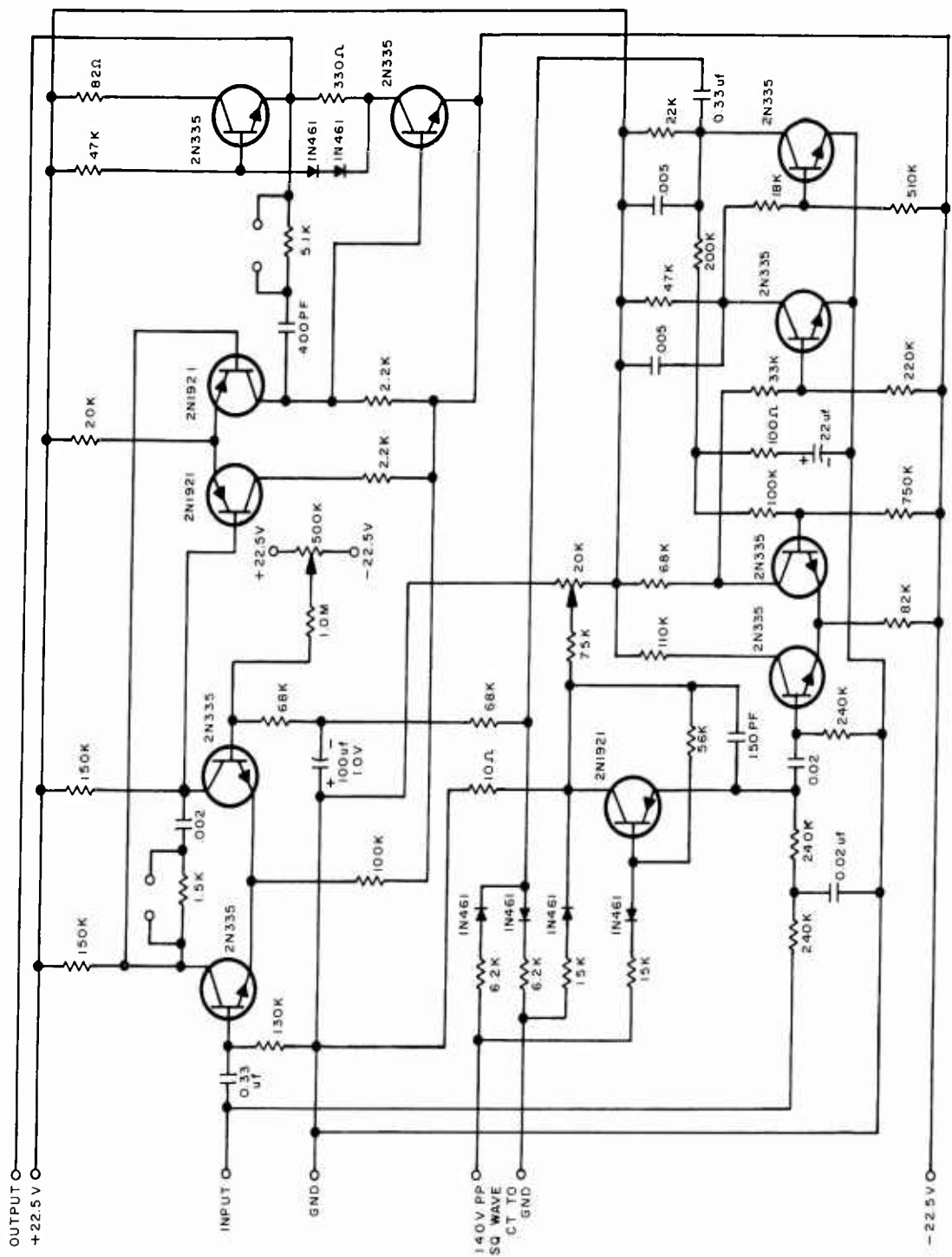


FIGURE 5-64. CHOPPER STABILIZED D-C OPERATIONAL AMPLIFIER

SECTION VI

OPERATION AND ALIGNMENT

A. OPERATION

Several items of special test equipment, or their equivalents, are necessary for operation of the breadboard equipment in a simulated encounter between two aircraft. These items of special test equipment and the functions they perform, are as follows:

- Test rack

The test rack provides simulated electrical input data required by the system and simulates the effect of the scanning antenna. It also contains the overheard reply generator.

- Background noise generators and signal conditioners

The background noise generators and signal conditioners provide random background noise signals to test their effect on the system, and generate properly shaped interrogation and reply pulses from the triggers generated by the breadboard encoders.

The following schematic information on these test units is included in this report:

- Test Rack Signal Schematic and System Interconnection Diagram
Figure 6-1
- Test Rack Power Schematic Figure 6-2
- Interrogation Background Noise Generator and Signal Conditioner
Figure 6-3
- Reply Background Noise Generator and Signal Conditioner Figure 6-4

In addition, schematics of electronic subassemblies of the test rack are included (figures 6-5 thru 6-7).

Some standard test equipment and power supplies are also required for operation, as detailed under Test Methods in Volume 1 of this report. Table 6-1

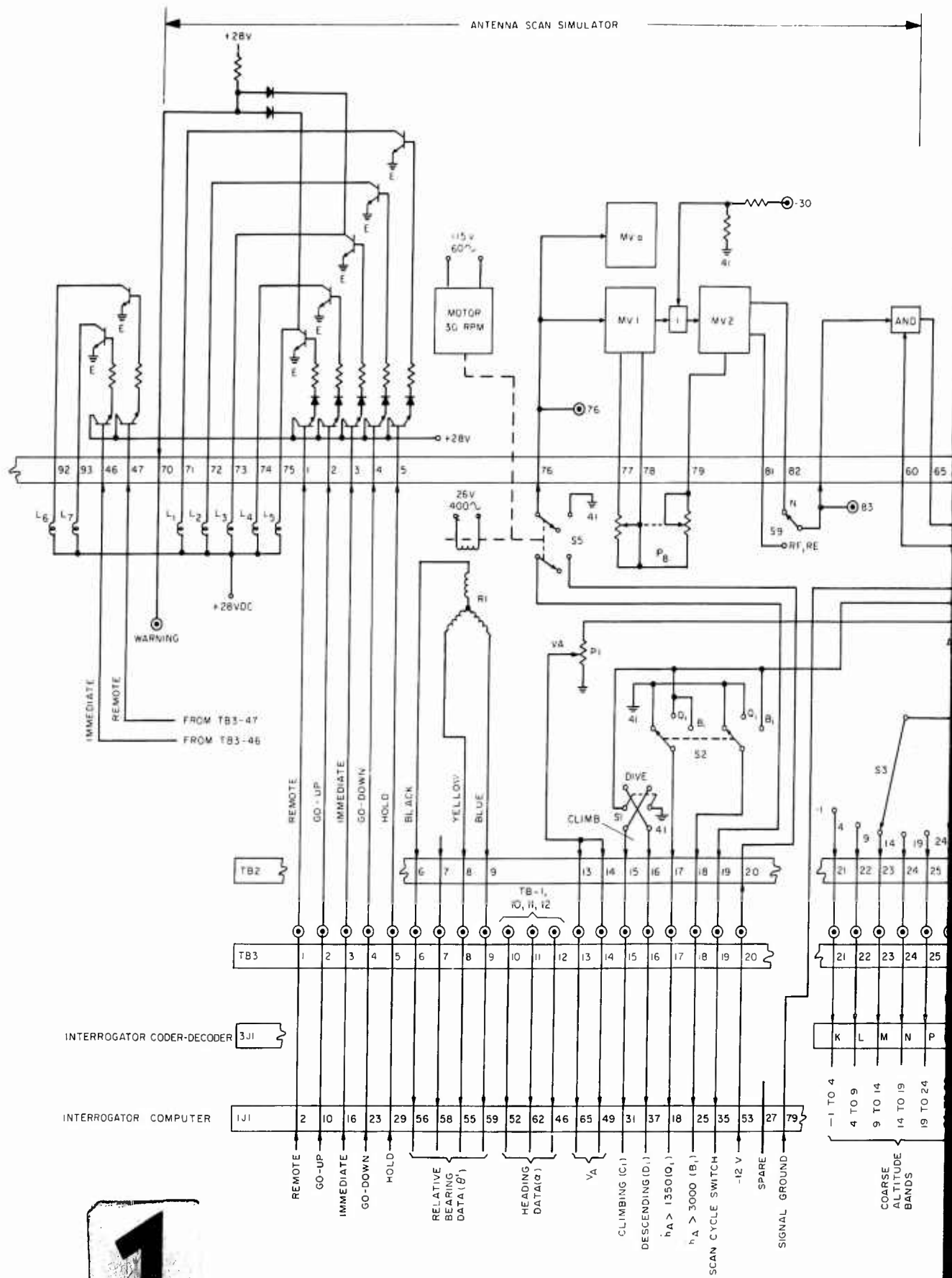
summarizes the power requirements of the breadboard coders and decoders. The breadboard computers have self-contained power supplies which operate from standard 115-volt, 400-cycle and 28-volt d-c sources.

TABLE 6-1
CODER-DECODER POWER REQUIREMENTS

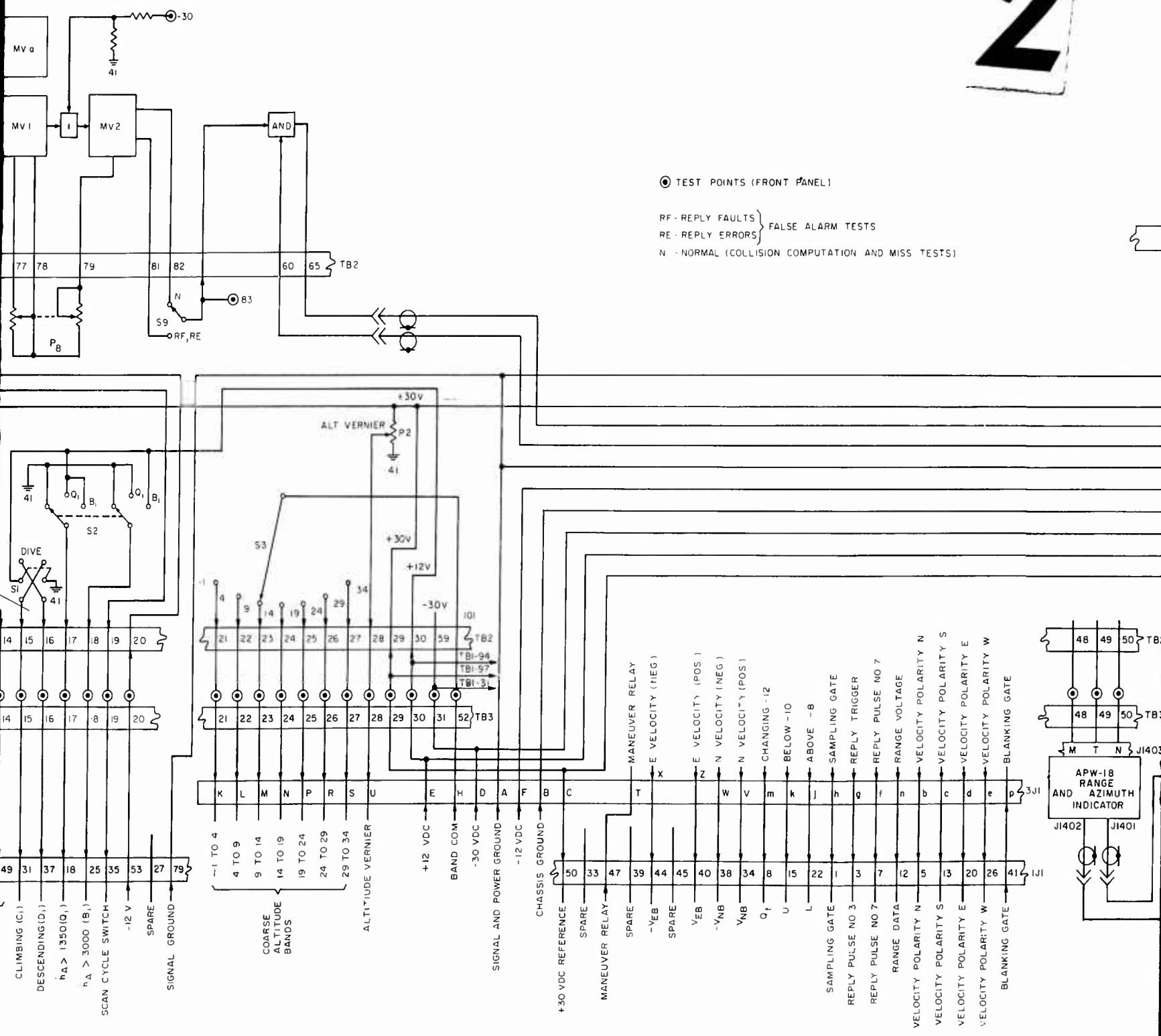
Supply Voltage	+30	-30	+12	-12
Interrogator (ma)	220	65	300	15
Transponder (ma)	200	20	300	10
Total (ma)	420	85	600	25

The primary controls used in operating the breadboard equipment are contained on the test rack. Figure 6-8 is a photograph of this rack with the various controls numbered. These controls are identified below by reference to these numbers, and operating instructions are included where necessary:

1. Interrogator Heading Reference Synchro
- 2., 3. Second Transponder Controls. Disconnected
4. Transponder Heading Reference Synchro
5. Variable Heading Drive Motor On-Off Switch. When variable heading is used, gears on transponder heading synchro (4) must be manually engaged using screw 4A.
6. Variable Altitude Drive Motor On-Off Switch
7. Interrogator Climb Rate Selector Switch
8. Antenna Scan Motor On-Off Switch
9. Interrogator Air Speed Control 0-300 Knots
10. Relative Bearing Reference Synchro
11. Interrogator Coarse Altitude Switch
12. Interrogator Vernier Altitude Control 0-5000 ft
13. Transponder Warning Lights
14. Interrogator Warning Lights
15. Transponder Vernier Altitude 0-5000 ft



2



● TEST POINTS (FRONT PANEL)

RF - REPLY FAULTS } FALSE ALARM TESTS
 RE - REPLY ERRORS }
 N - NORMAL (COLLISION COMPUTATION AND MISS TESTS)

CLIMBING (C.)
 DESCENDING (D.)
 $h_A > 1350(Q)$
 $h_A > 3000 (S)$
 SCAN CYCLE SWITCH
 -12 V
 SPARE
 SIGNAL GROUND

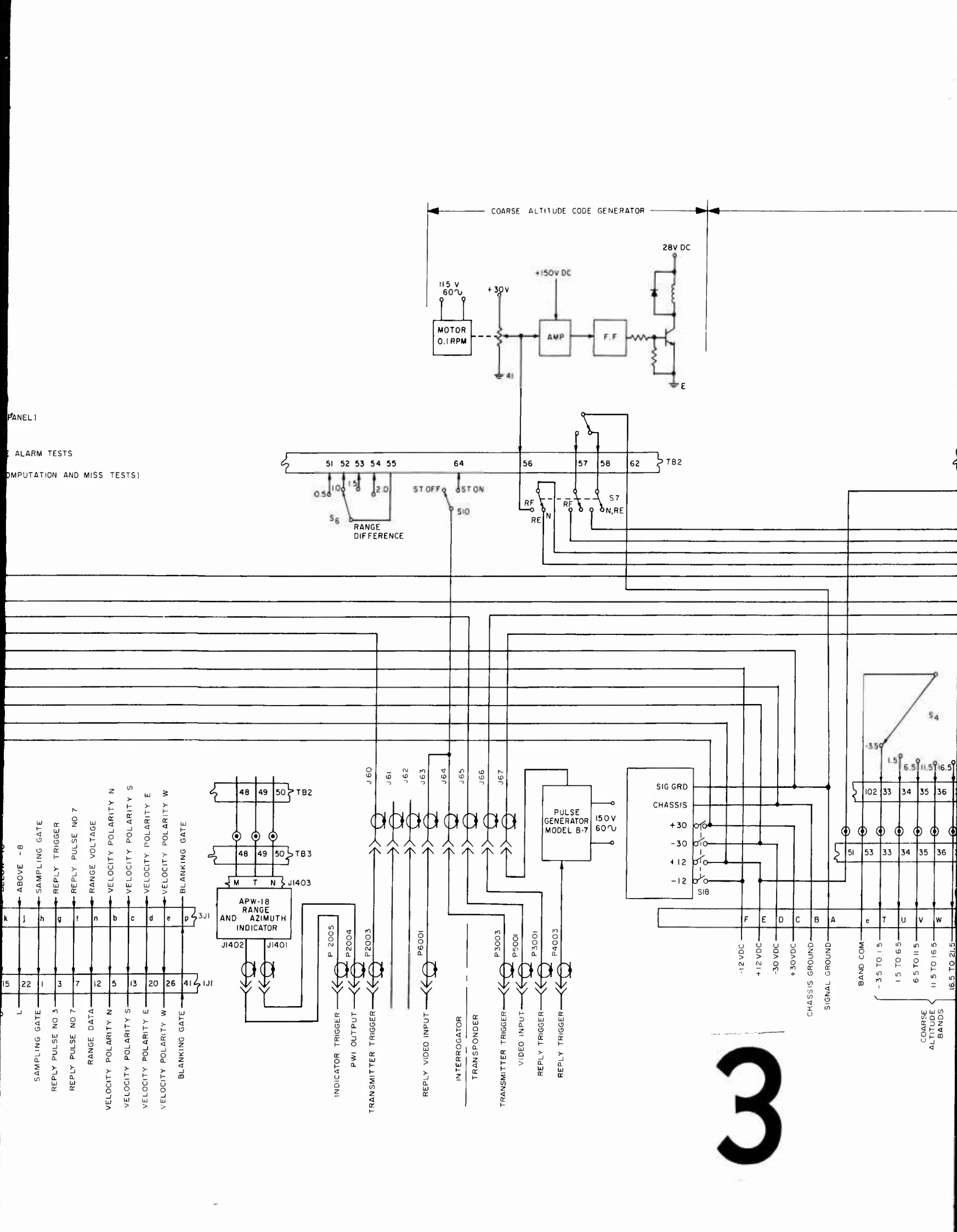
~1 TO 4
 4 TO 9
 9 TO 14
 14 TO 19
 19 TO 24
 24 TO 29
 29 TO 34
 ALTITUDE VERNIER

+12 VDC
 BAND COM
 -30 VDC
 SIGNAL AND POWER GROUND
 -12 VDC
 CHASSIS GROUND

+30 VDC REFERENCE
 SPARE
 MANEUVER RELAY
 SPARE
 -VEB
 SPARE
 VEB
 -VNB
 VNB
 Qf
 U
 L
 SAMPLING GATE
 REPLY PULSE NO 3
 REPLY PULSE NO 7
 RANGE DATA
 VELOCITY POLARITY N
 VELOCITY POLARITY S
 VELOCITY POLARITY E
 VELOCITY POLARITY W
 BLANKING GATE

APW-18
 RANGE
 AND AZIMUTH
 INDICATOR

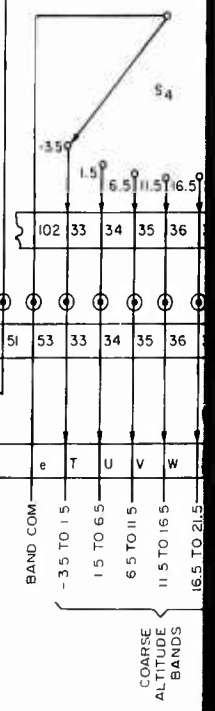
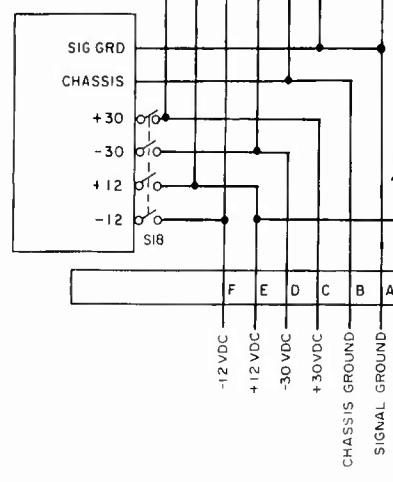
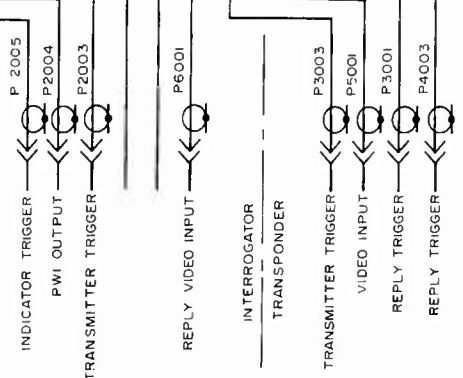
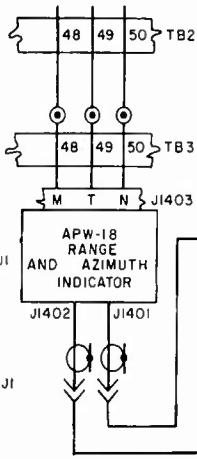
J1402 J1401



PANEL 1
 ALARM TESTS
 COMPUTATION AND MISS TESTS)

15 L
 22 k
 1 j
 3 h
 7 g
 12 f
 5 n
 13 b
 20 c
 26 d
 41 e
 31 p
 1 J1
 3 J1
 41 J1

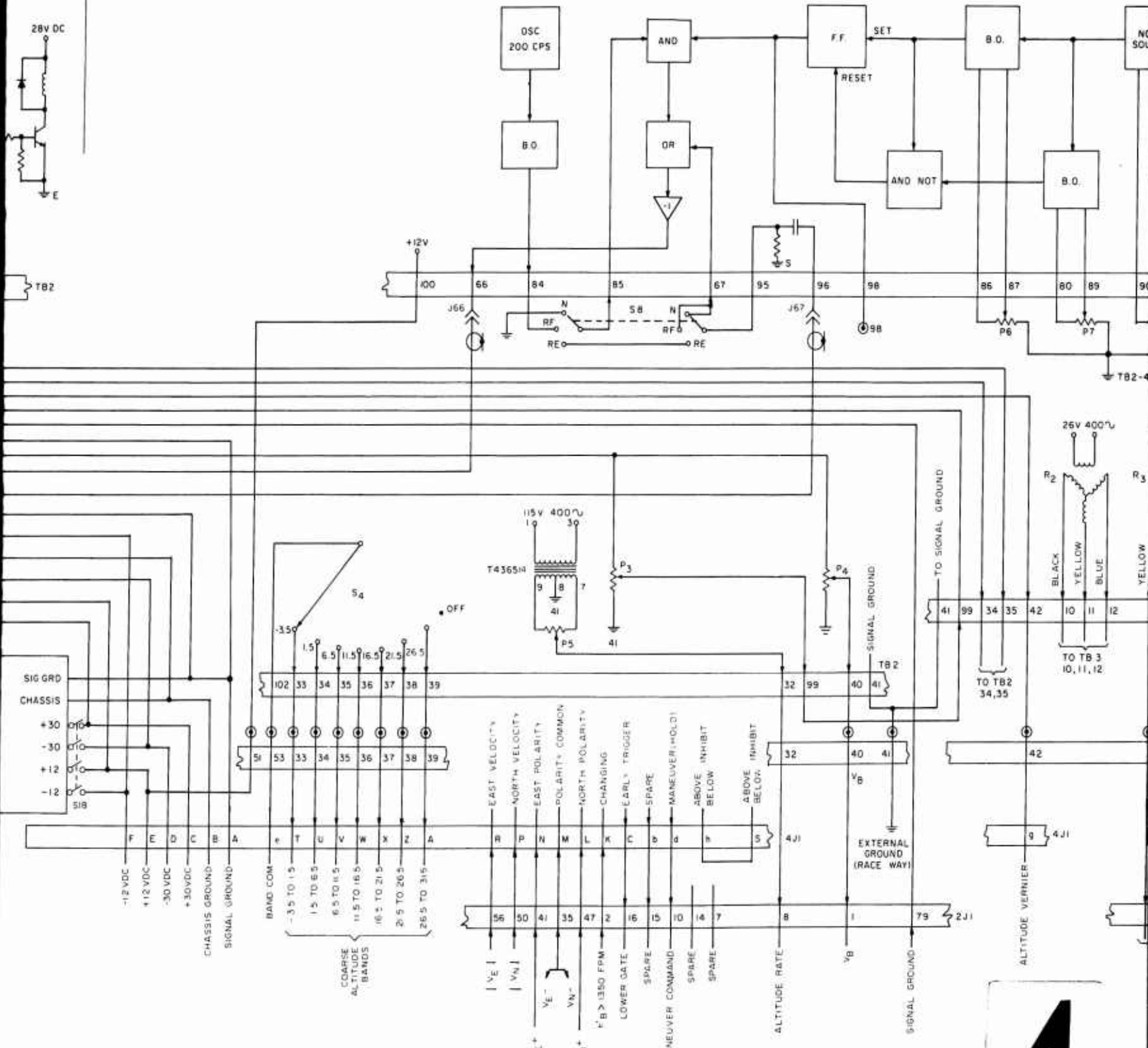
ABOVE -8
 SAMPLING GATE
 REPLY PULSE NO 3
 REPLY PULSE NO 7
 RANGE VOLTAGE
 VELOCITY POLARITY N
 VELOCITY POLARITY S
 VELOCITY POLARITY E
 VELOCITY POLARITY W
 BLANKING GATE



3

OVERHEARD REPLY GENERATOR

+150V DC



4

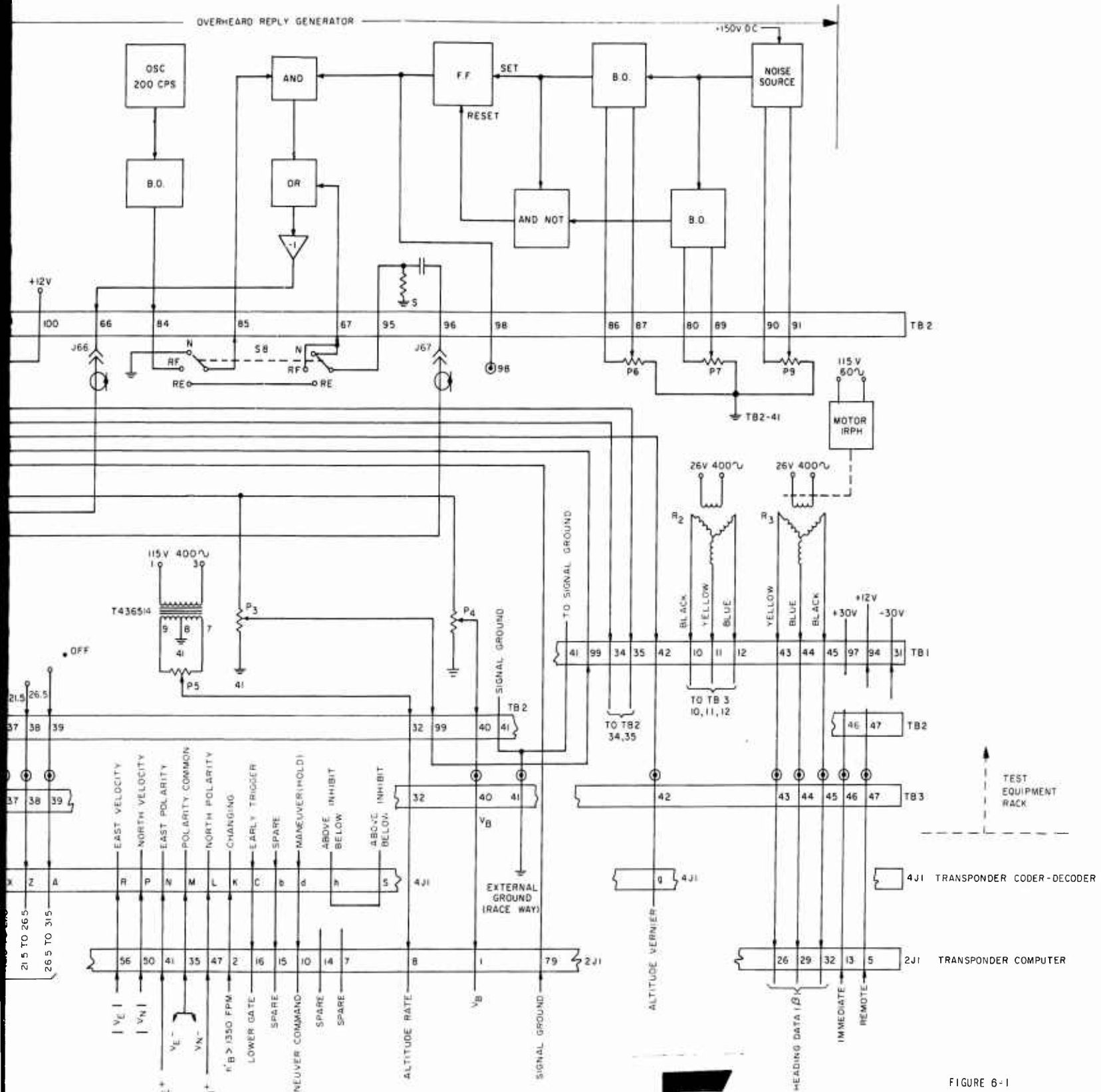
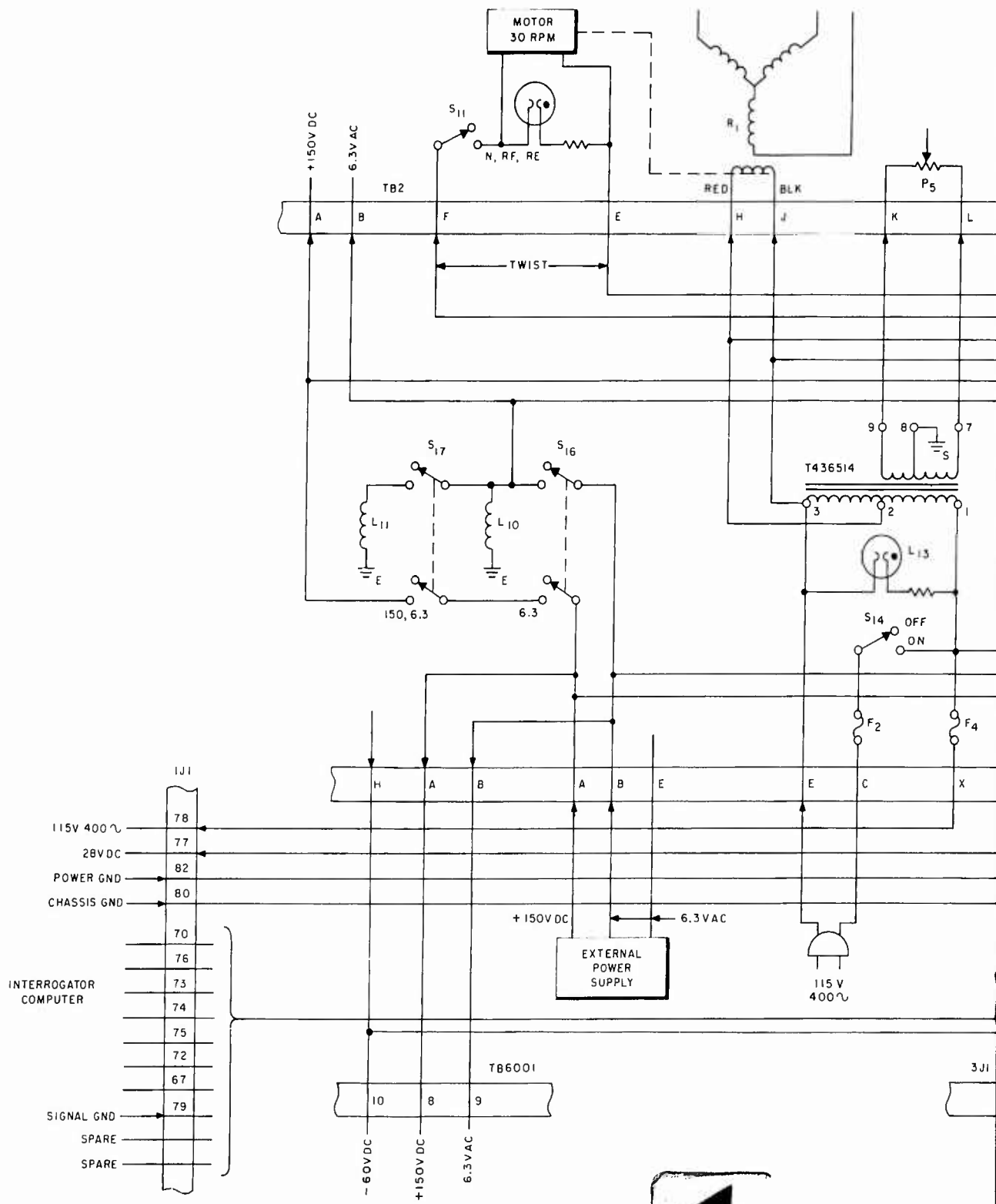


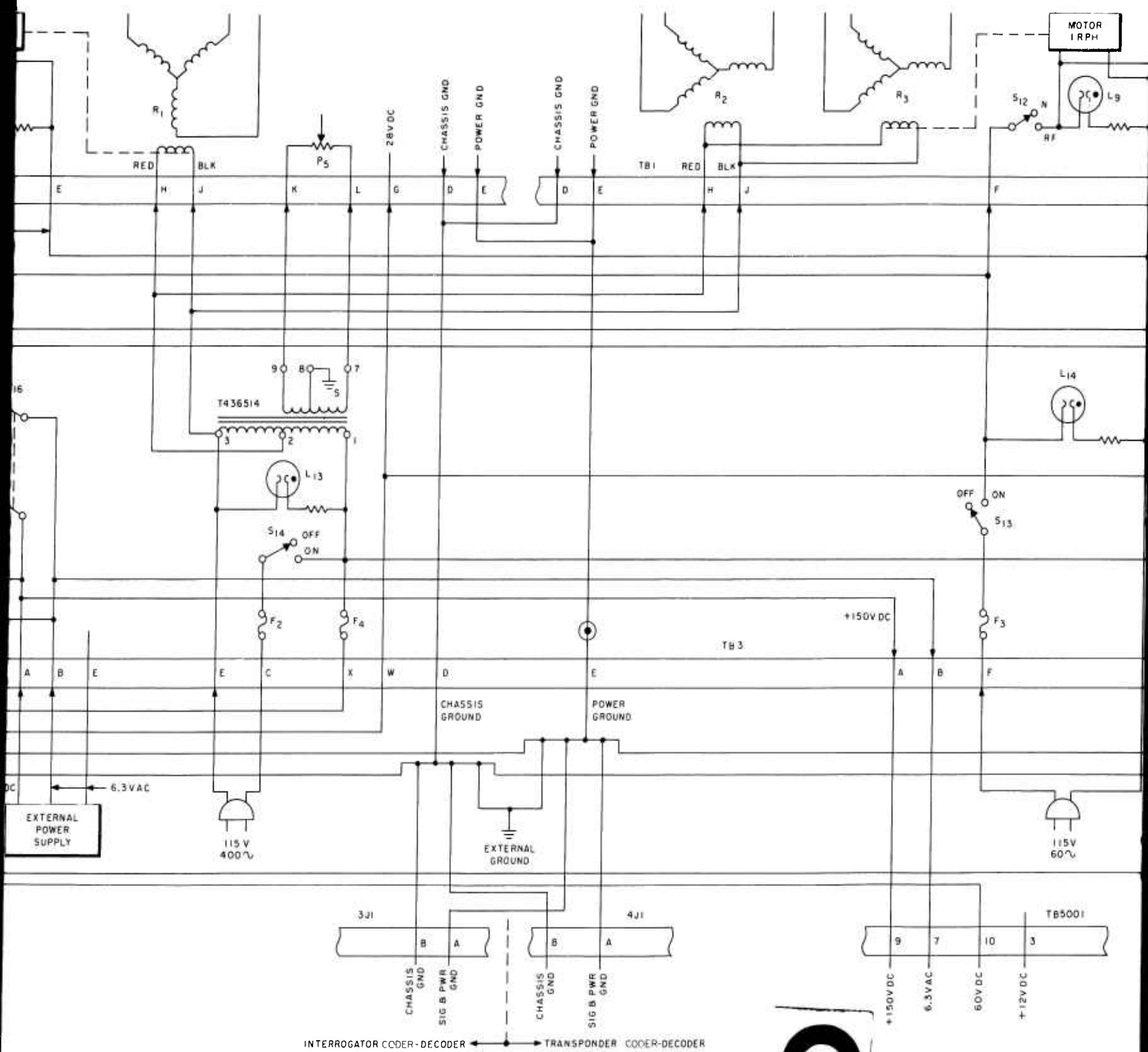
FIGURE 6-1
TEST RACK SIGNAL SCHEMATIC AND SYSTEM
INTERCONNECTION DIAGRAM

5



1

INTERROGATOR



INTERROGATOR CODER-DECODER TRANSponder CODER-DECODER

2

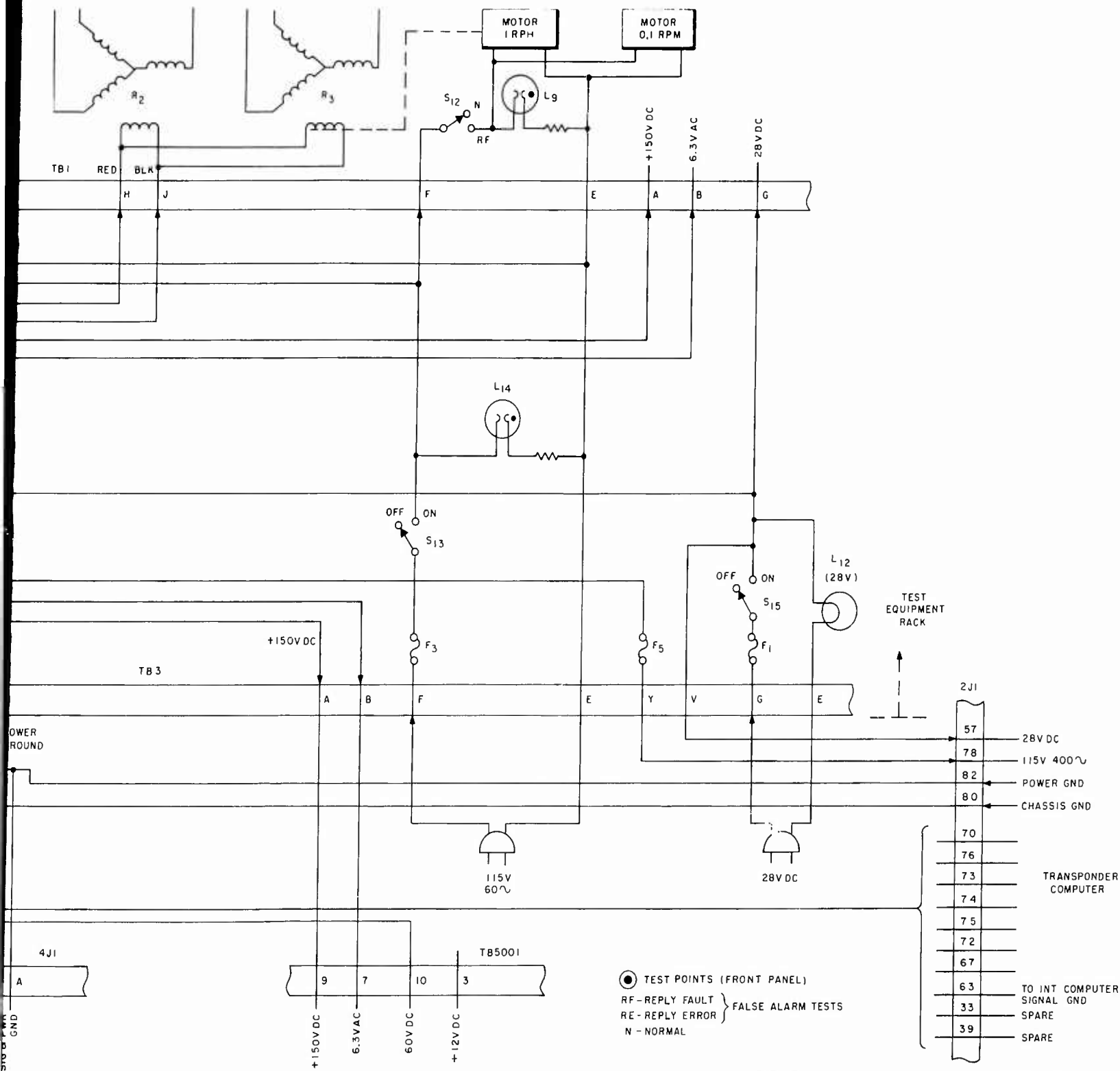
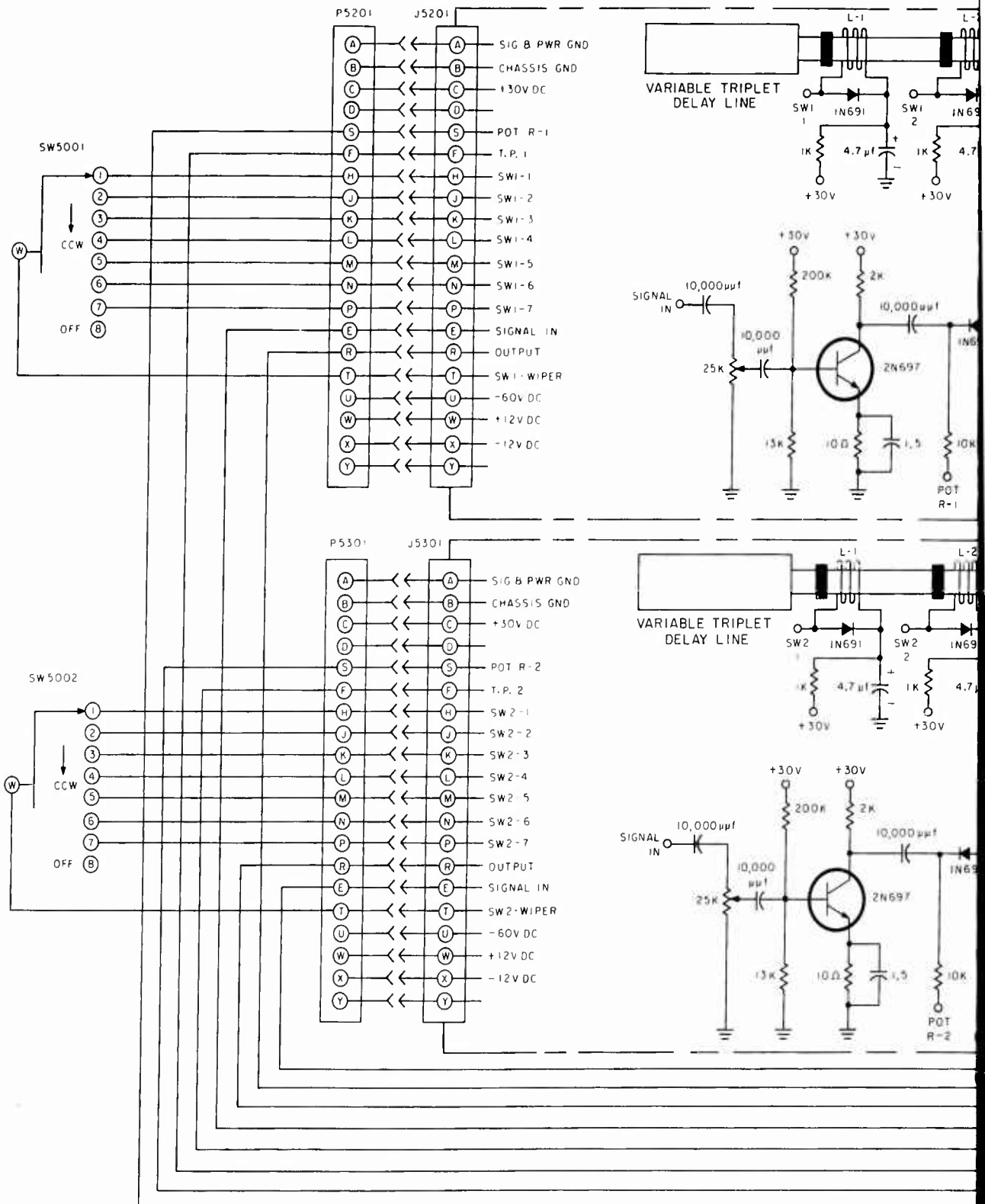
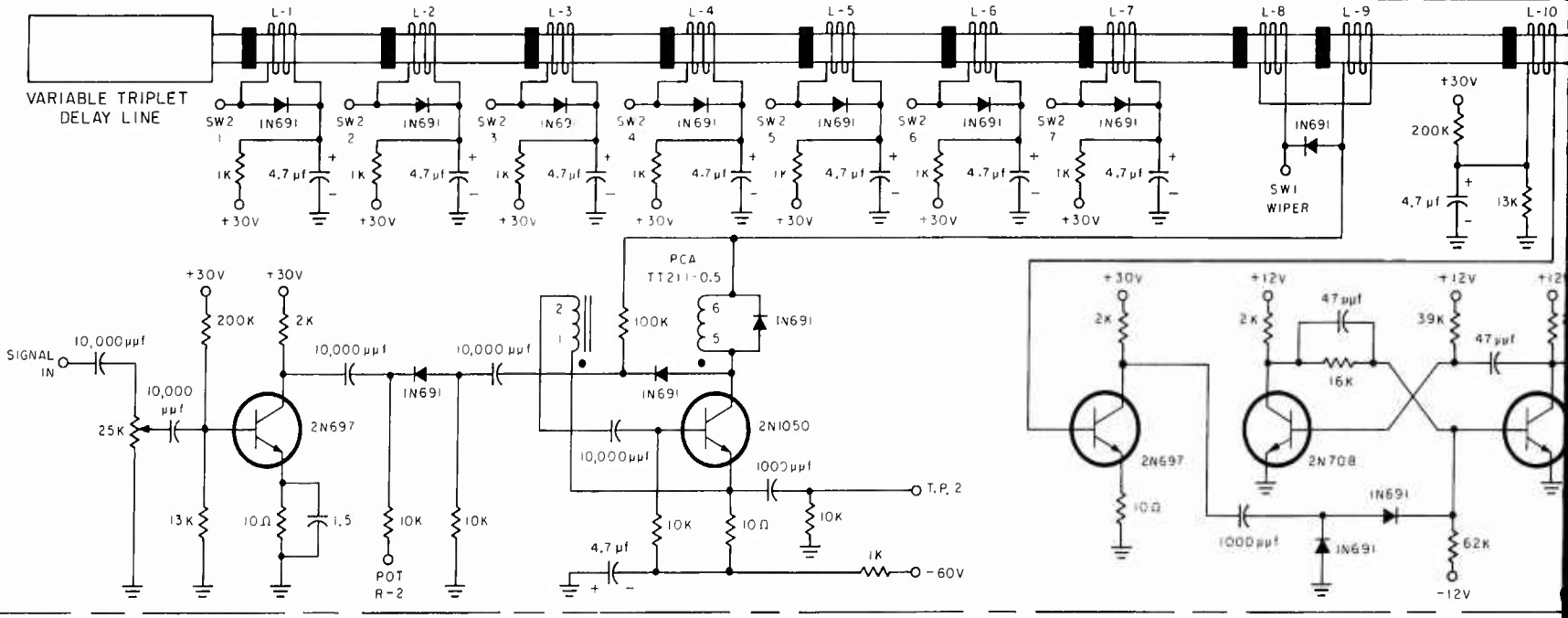
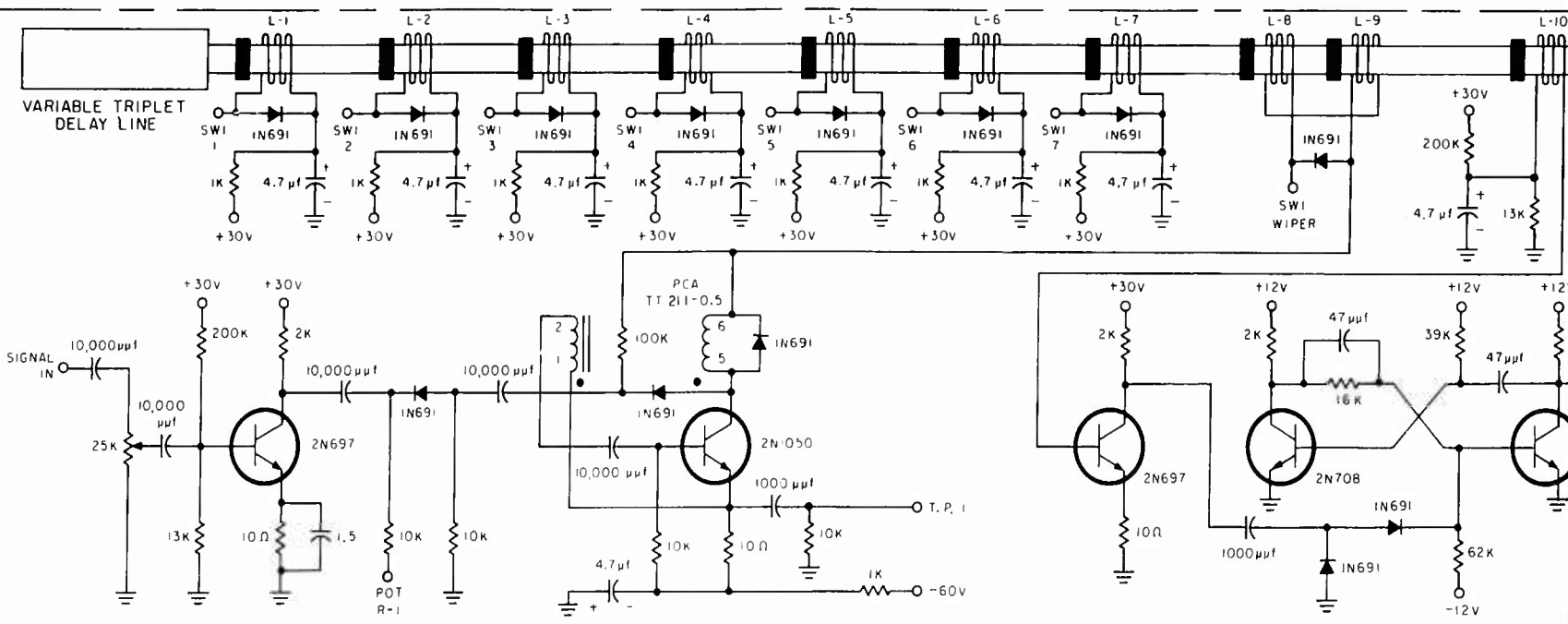
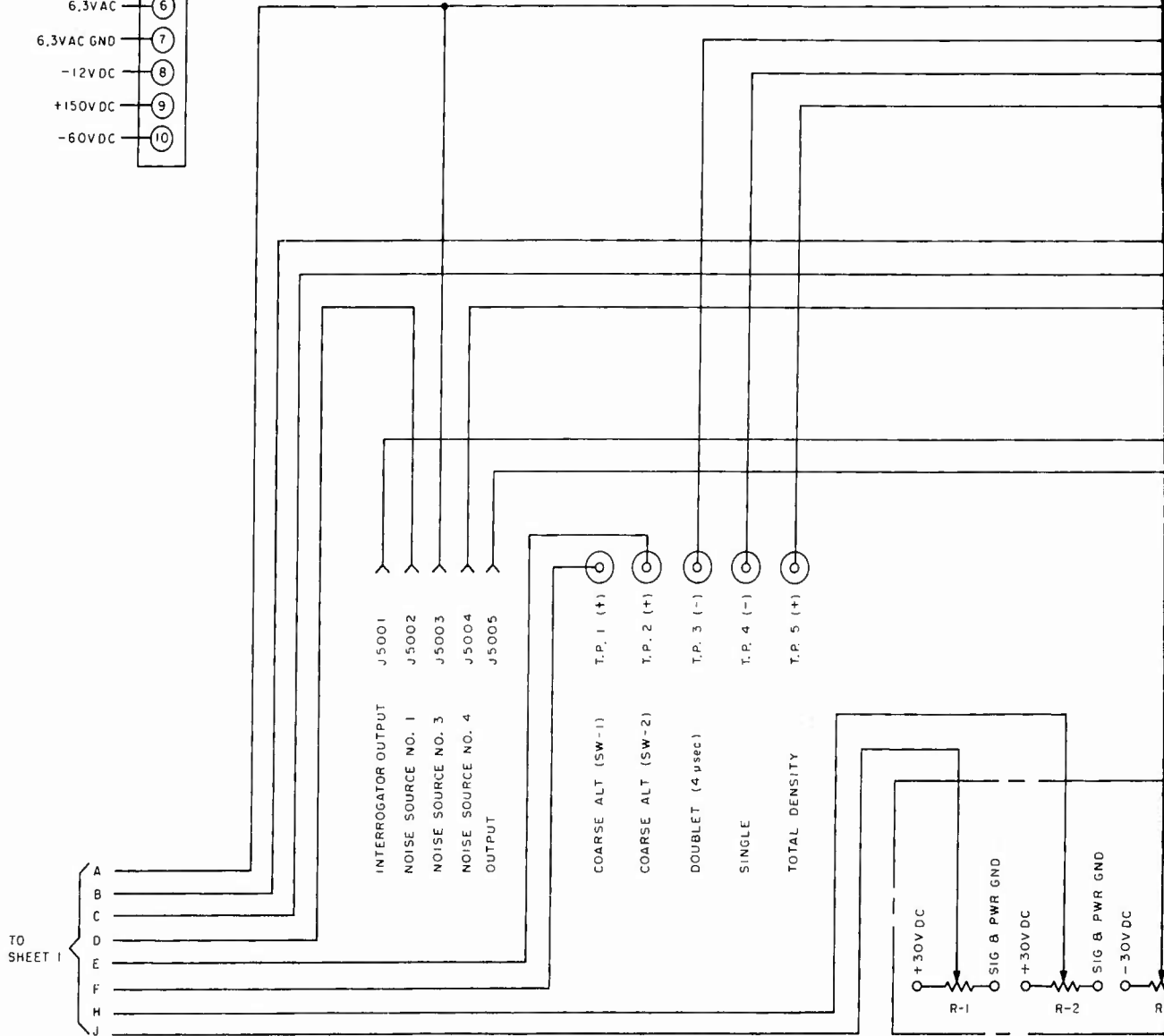
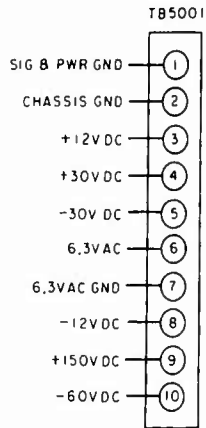


FIGURE 6-2
TEST RACK POWER SCHEMATIC

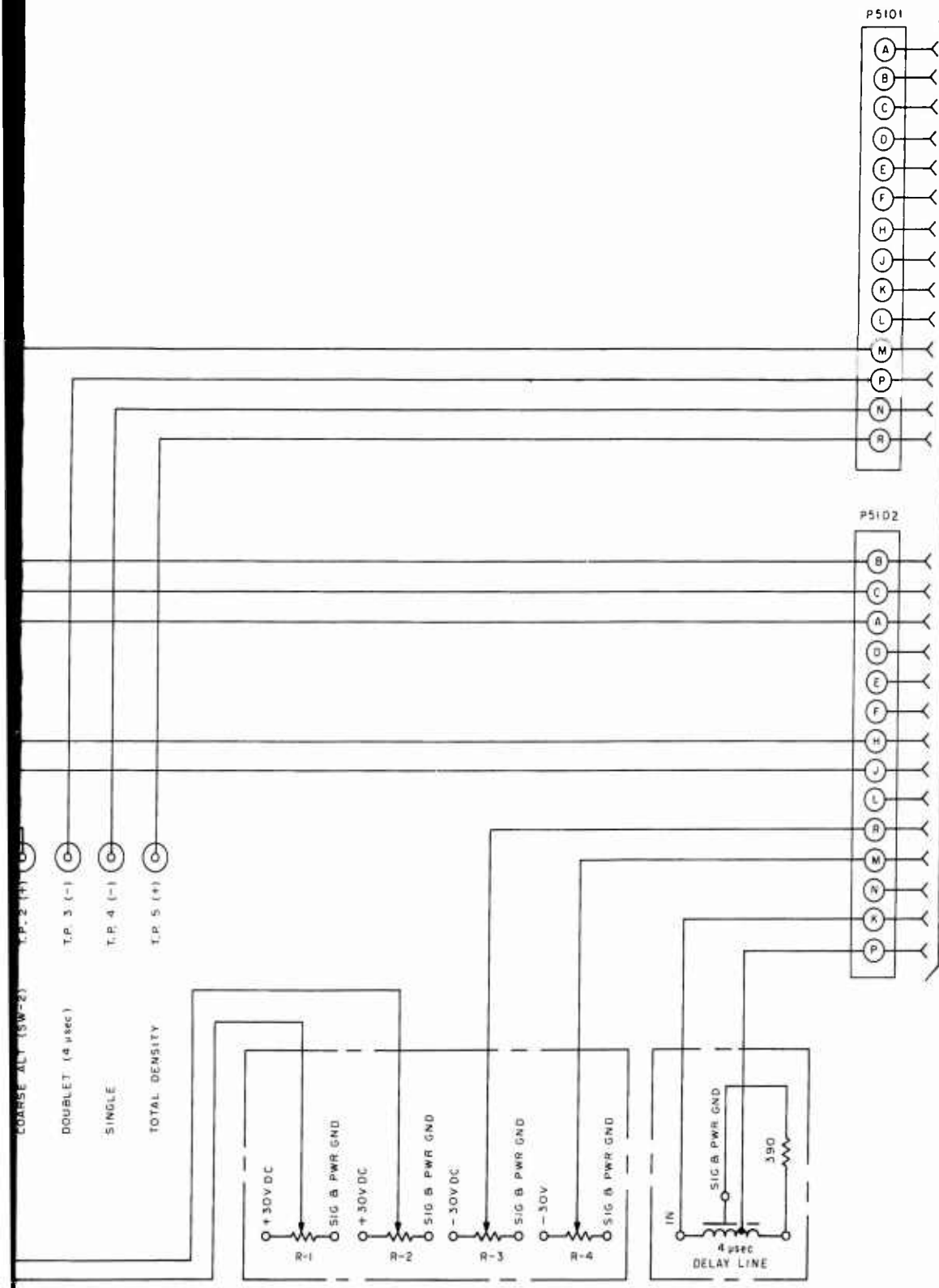




2



1



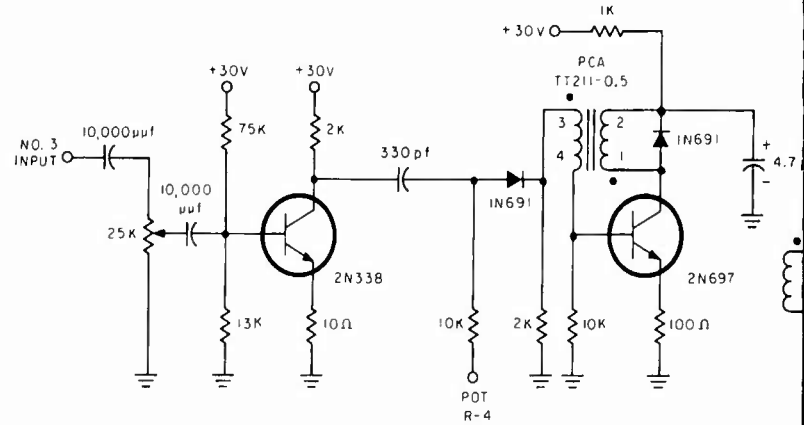
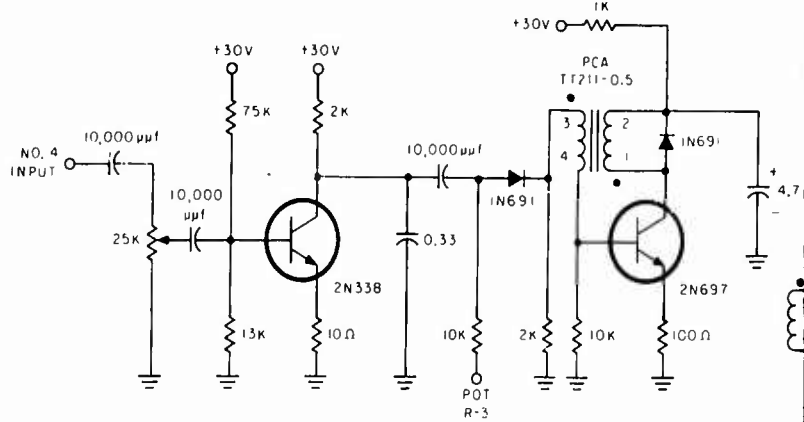
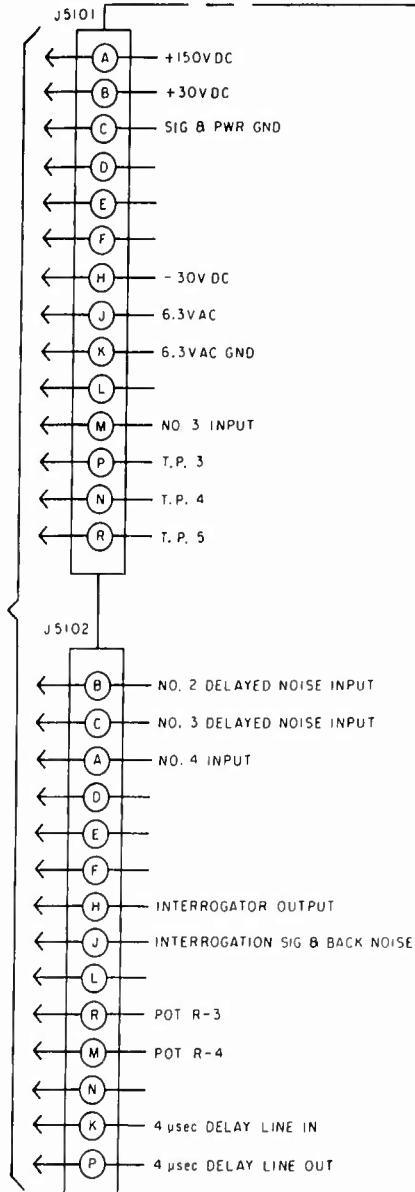
CONTINUED ON SHEET 3

2

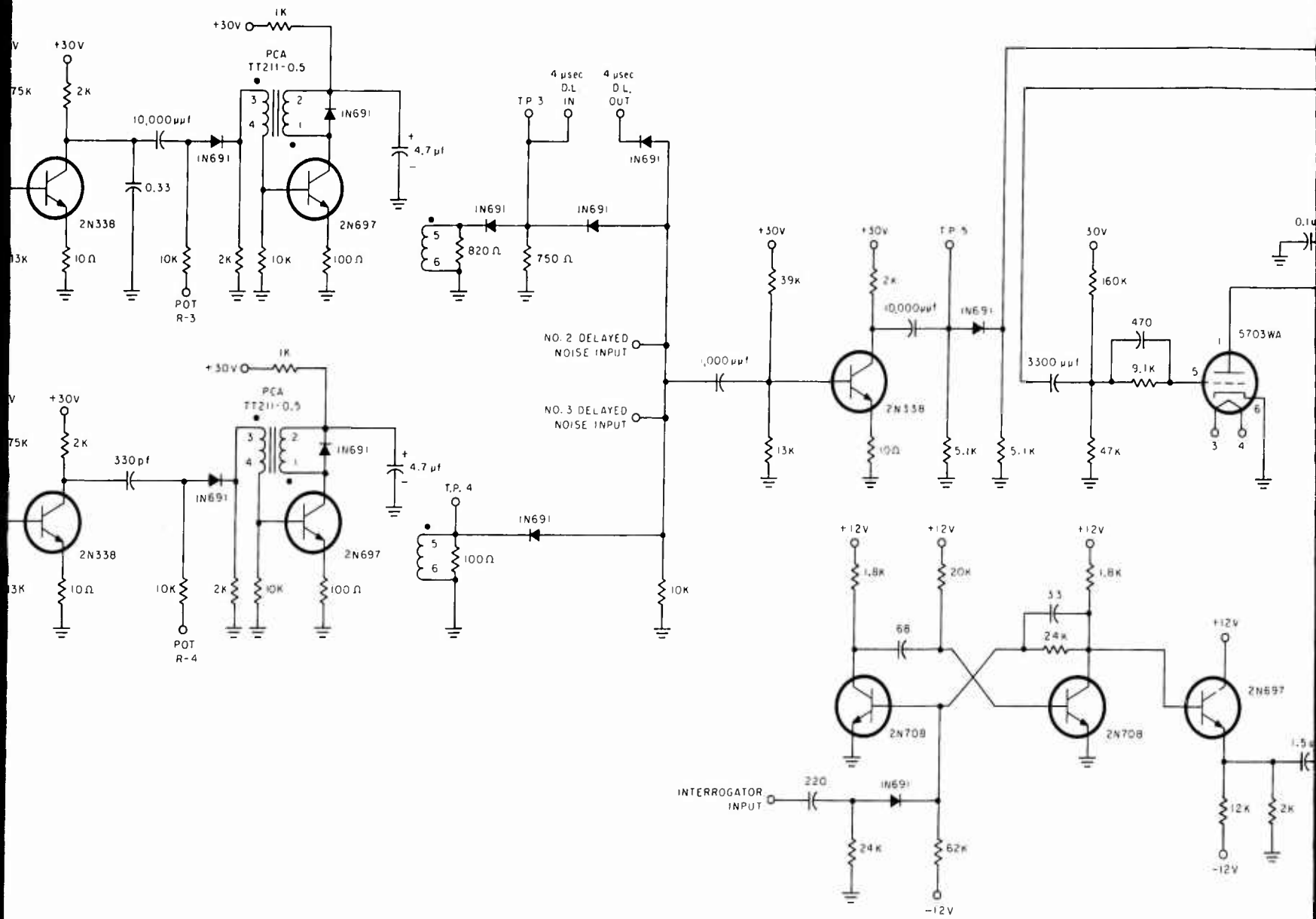
- NOTES:
- 1 POWER INTERCONNECTIONS NOT SHOWN
 - 2 R1-R4 100K 1W POTS
 - 3 DELAY LINE ASSY NO'S: COIL MOUNT ASSY. 4240-00147
PAD BASE 4240-00143
PAD COVER 4240-00144
 - 4 ALL TRANSFORMERS PCA ELECTRONICS TYPE AS SHOWN
 - 5 DELAY LINES: 0.5 μsec PCA TYPE DL1000D-05 RMT
4 μsec DWG NO. 4240-00174

FIGURE 6-3
INTERROGATION BACKGROUND NOISE GENERATOR AND
SIGNAL CONDITIONER (SHEET 2 OF 3)

CONTINUED FROM SHEET 2



LOGIC CIRCUIT BOARD



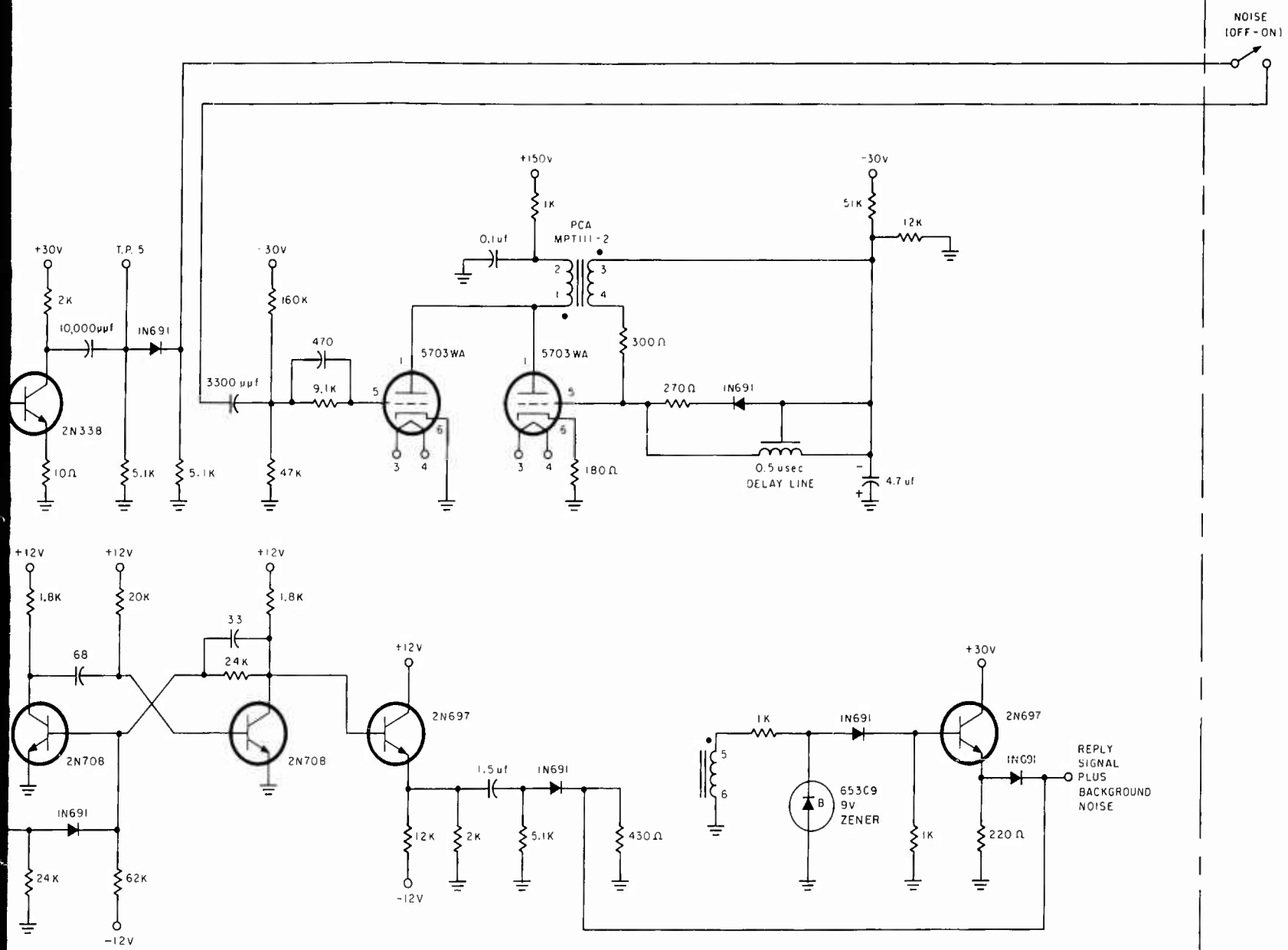
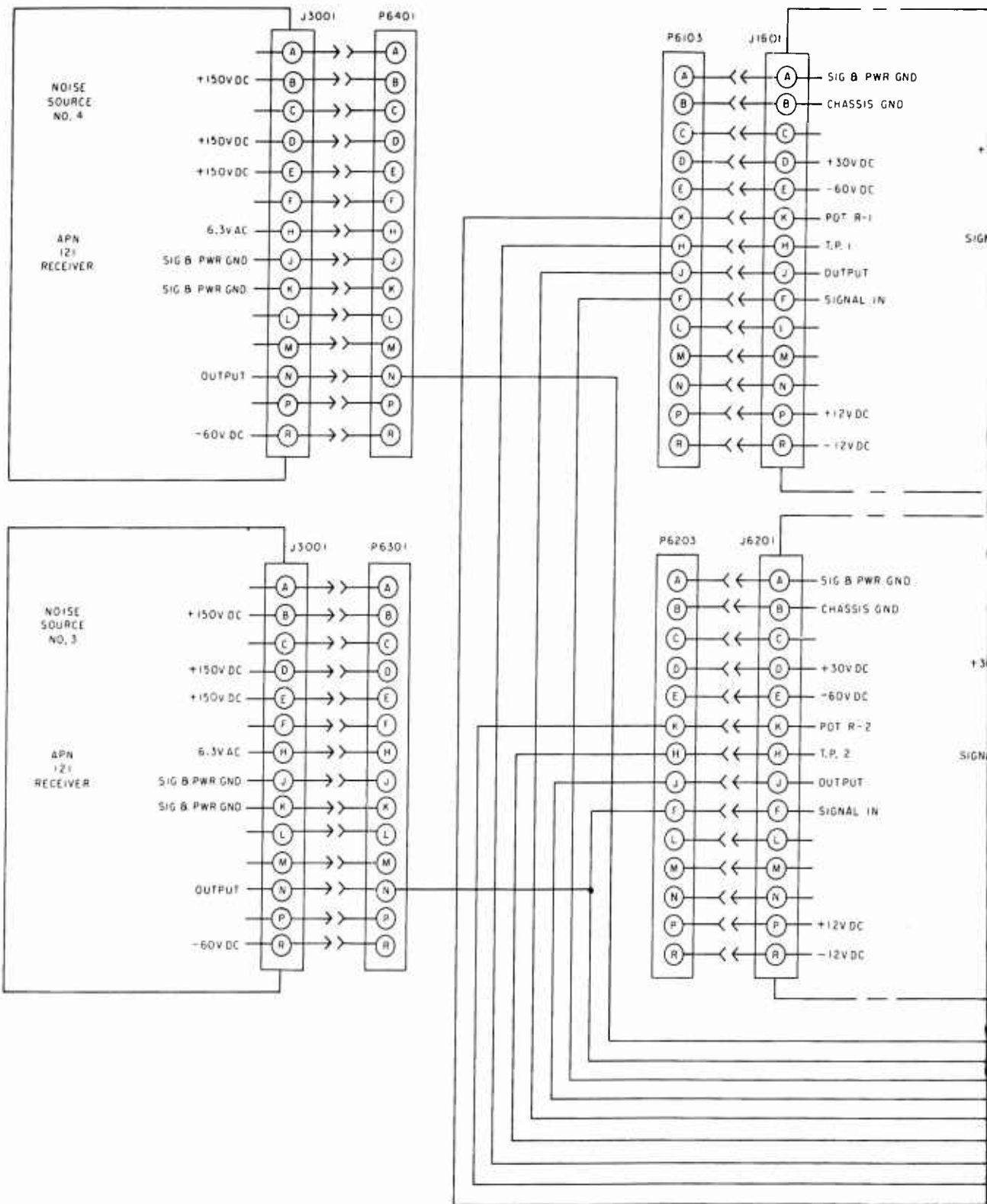
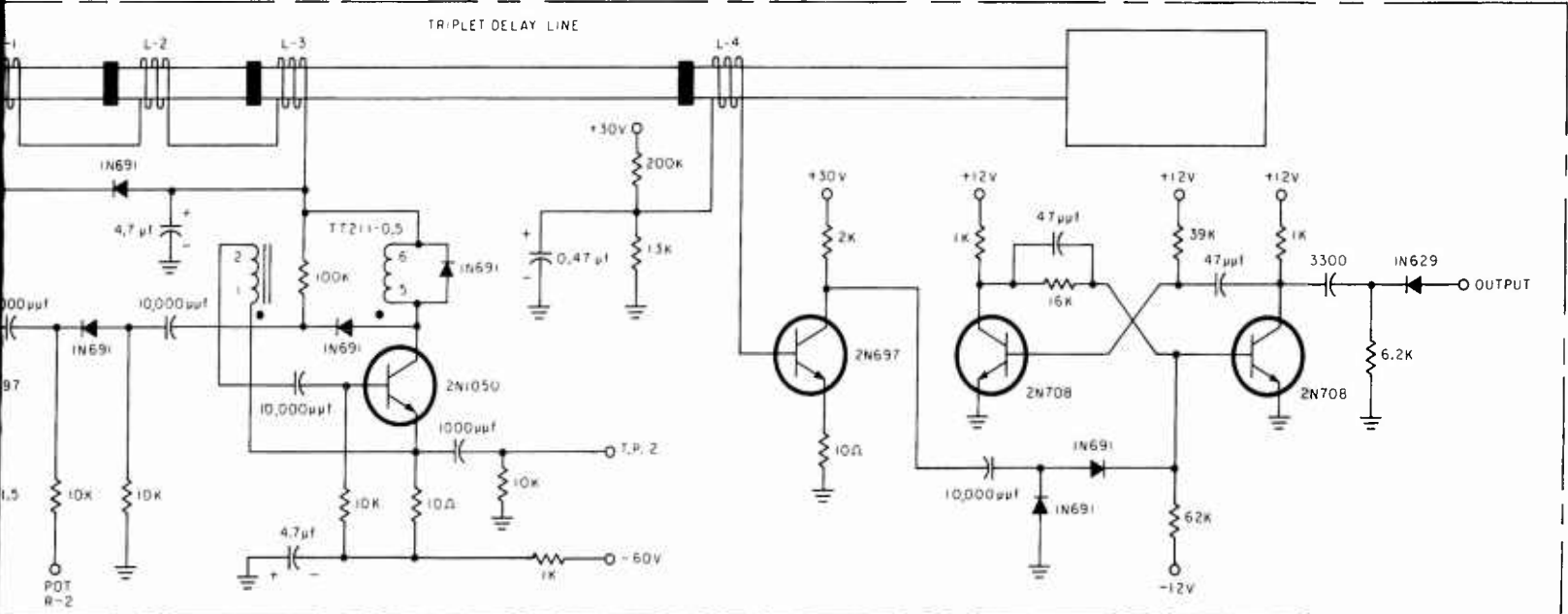
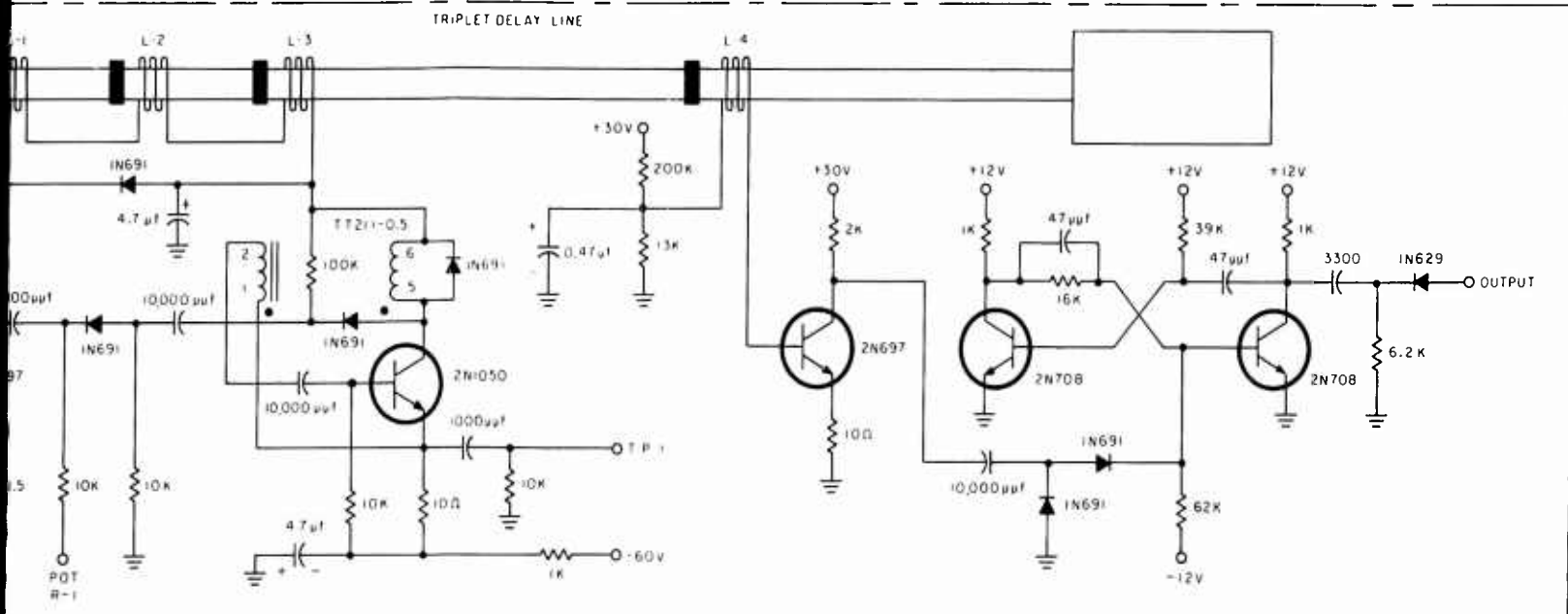


FIGURE 6-3
INTERROGATION BACKGROUND NOISE GENERATOR AND
SIGNAL CONDITIONER (SHEET 3 OF 3)



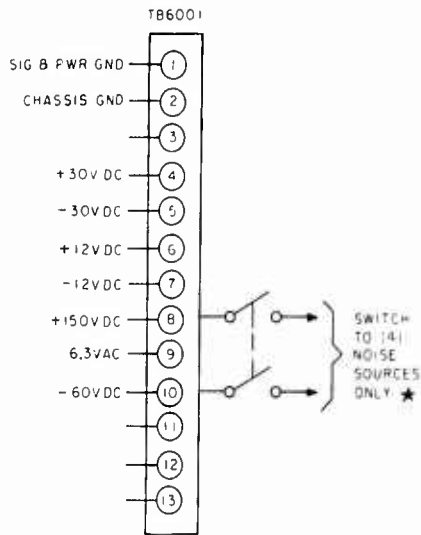
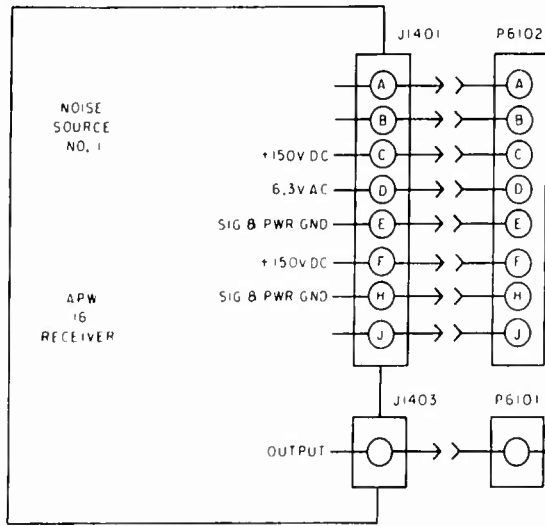
1



A
B
C
D
E
F
H
J
K
TO SHEET 2

3

FIGURE 6-4
REPLY BACKGROUND NOISE GENERATOR AND SIGNAL
CONDITIONER (SHEET 1 OF 3)



FROM SHEET 1

A

B

C

D

E

F

H

J

K

J6001

J6002

J6003

J6004

J6005

J6006

J6007

TRANSPOUNDER OUTPUT

NOISE SOURCE NO. 1

NOISE SOURCE NO. 3

NOISE SOURCE NO. 4

OUTPUT

SECOND TRANSPOUNDER SIMULATOR

T.P. 1

T.P. 2

T.P. 3

T.P. 4

T.P. 5

T.P. 6

(+) TRIPLET (INT ABOVE TRANS)

(+) TRIPLET (INT BELOW TRANS)

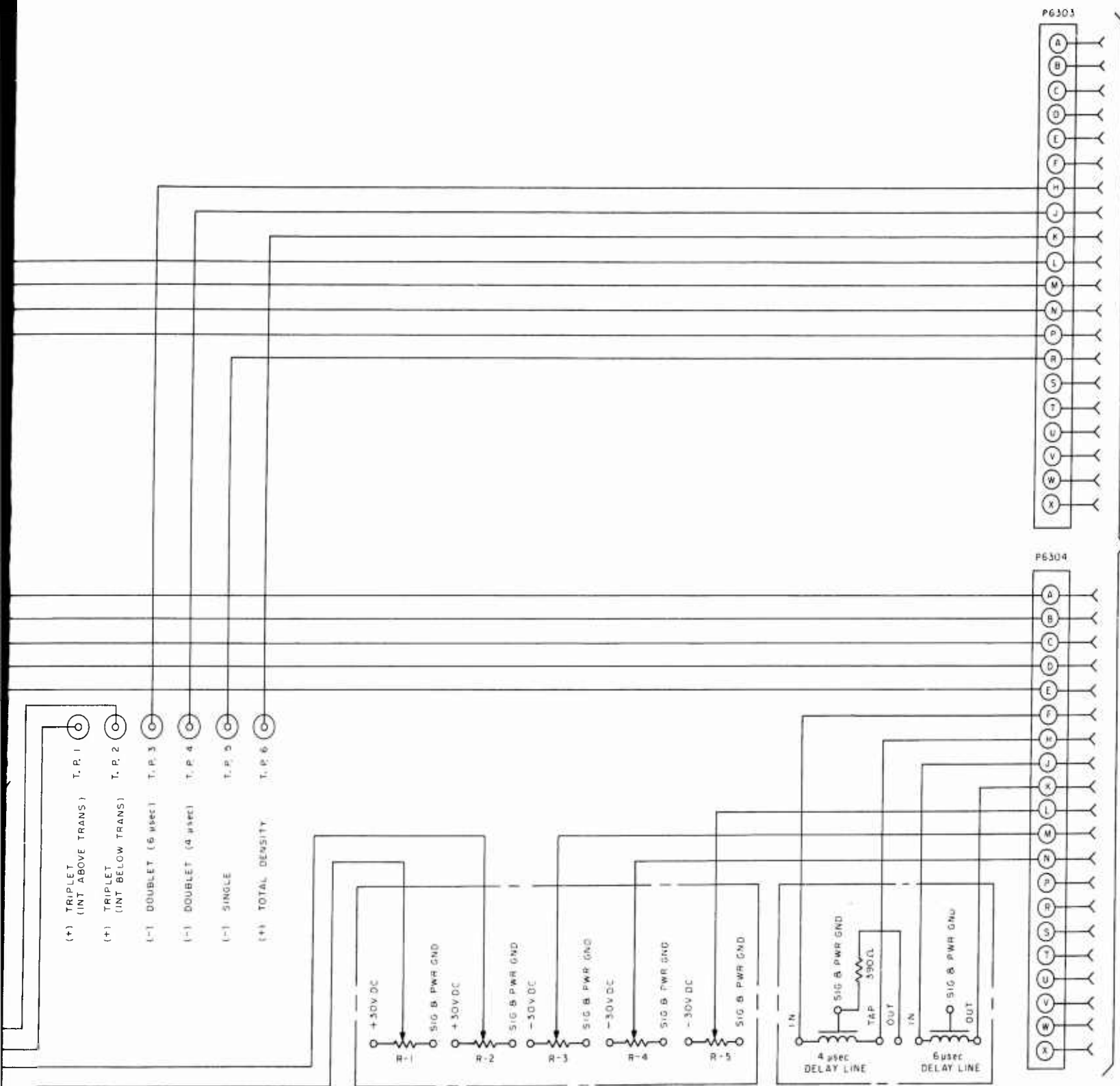
(-) DOUBLET (6 μsec)

(-) DOUBLET (4 μsec)

(-) SINGLE

(+) TOTAL DENSITY



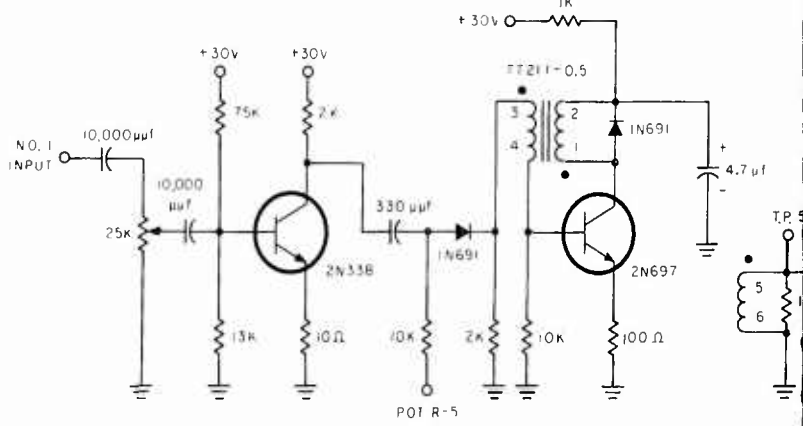
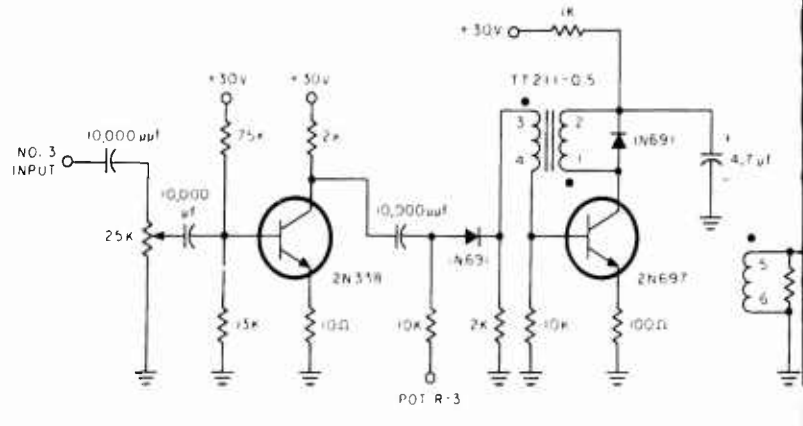
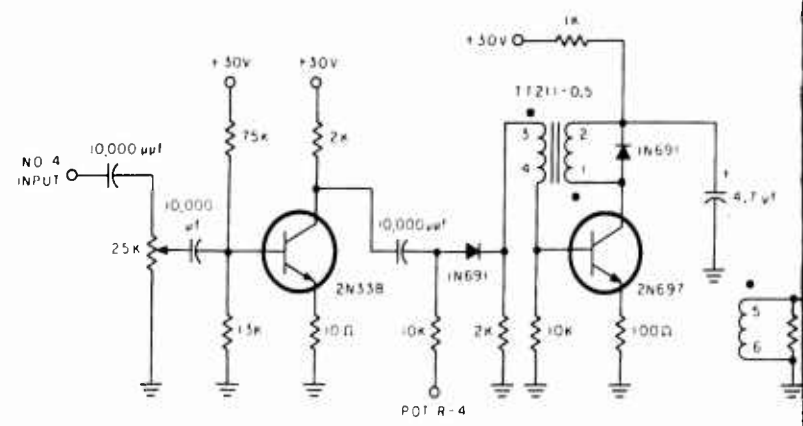
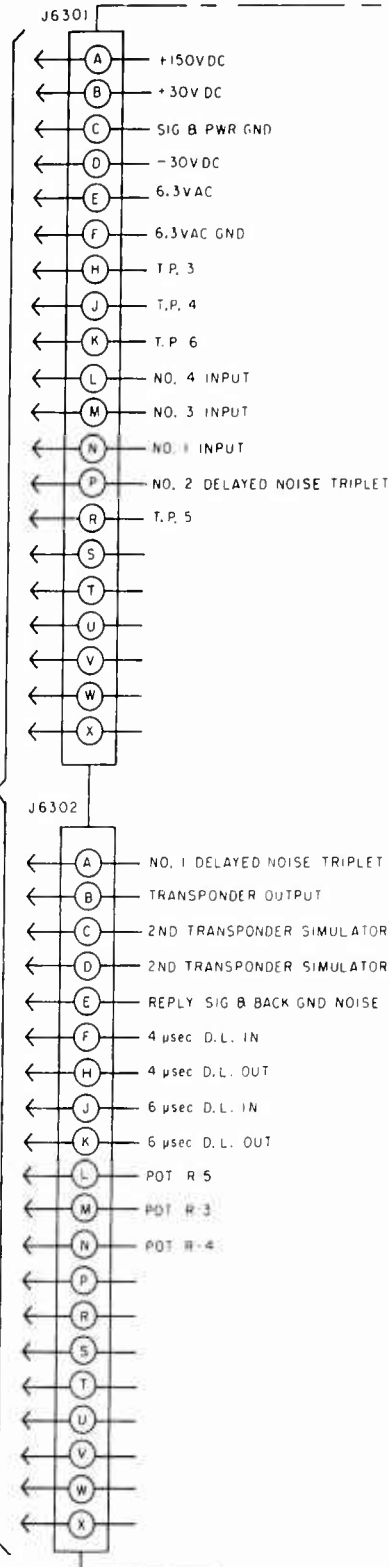


CONTINUED ON SHEET 3

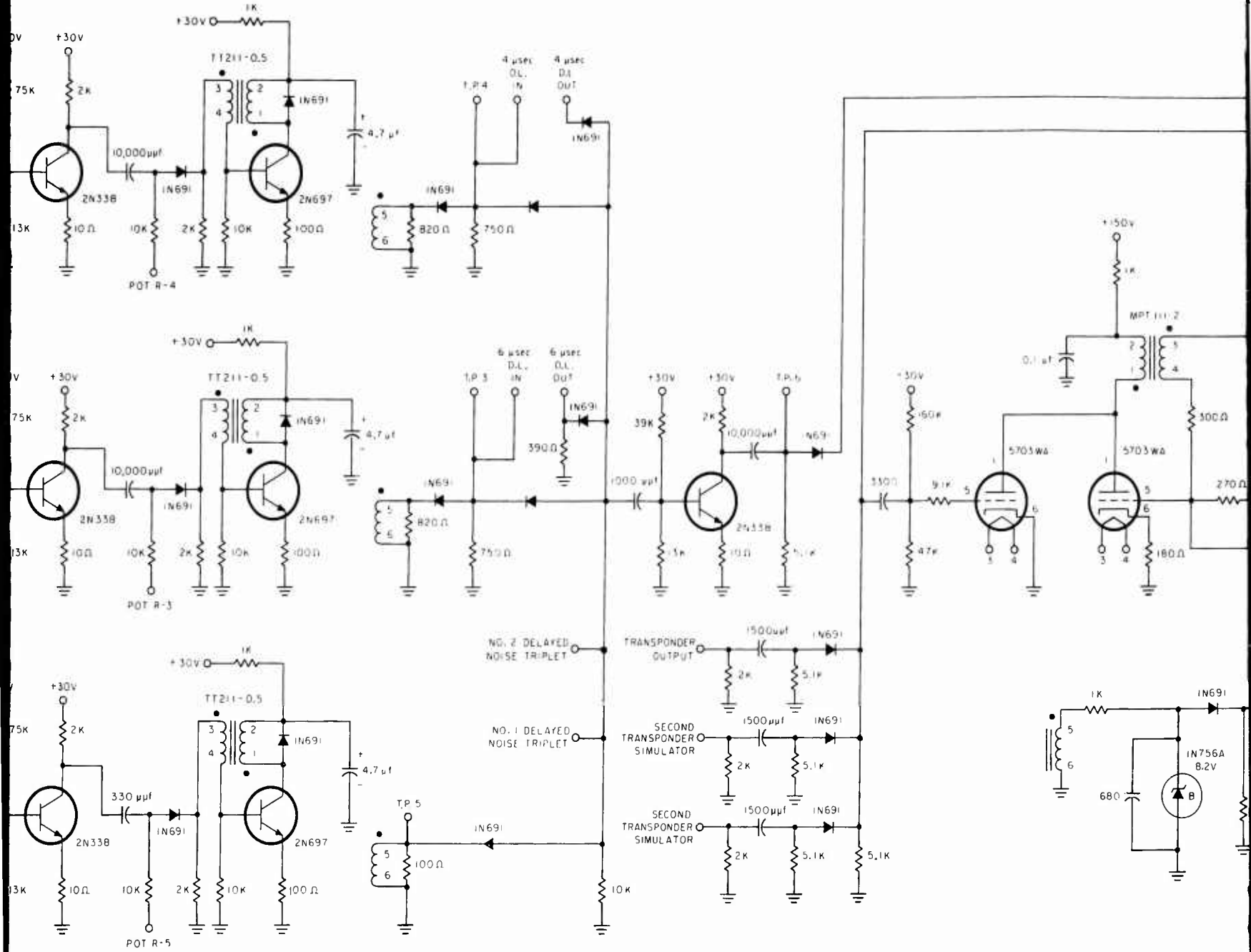
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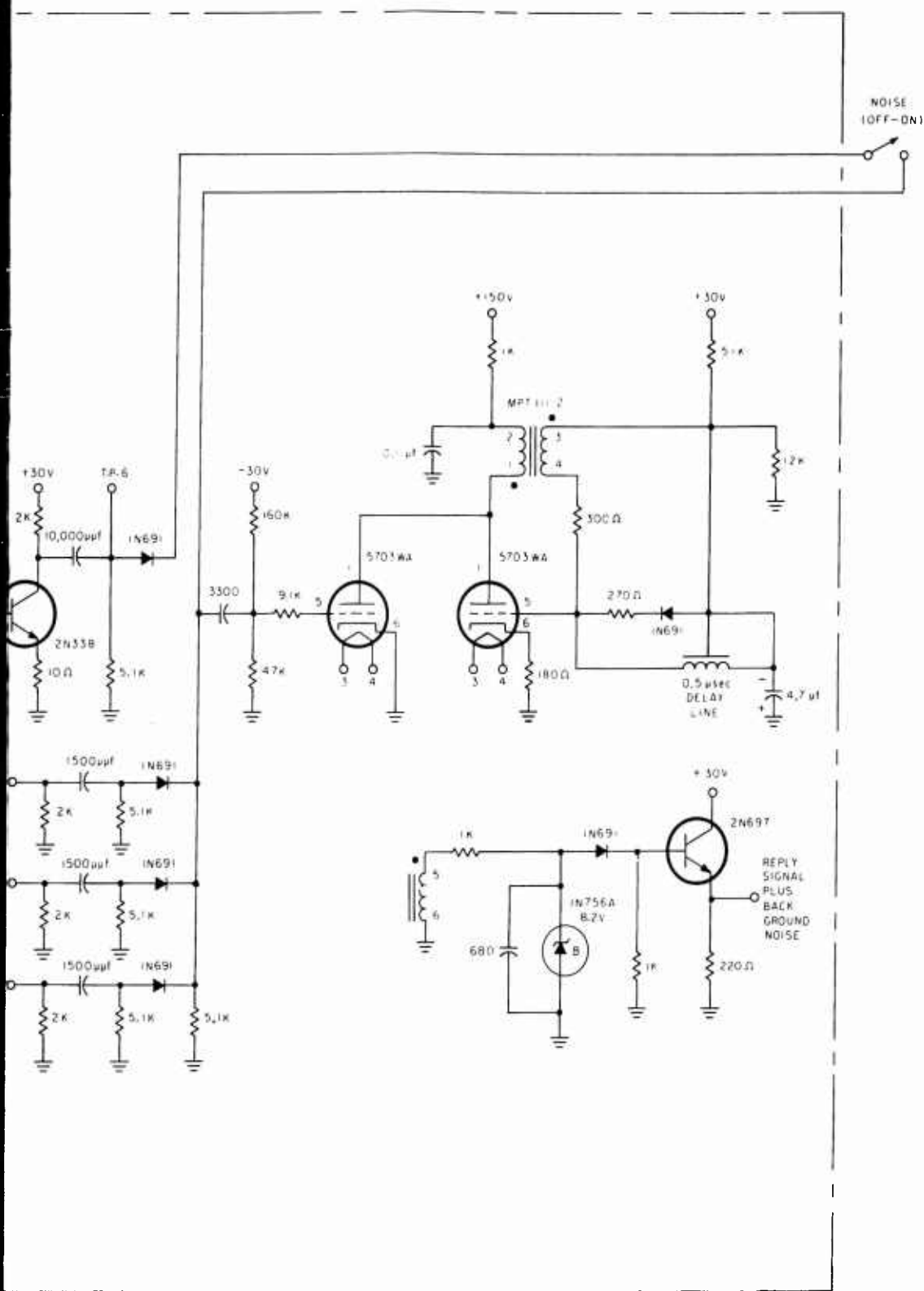
FIGURE 6-4
 REPLY BACKGROUND NOISE GENERATOR AND SIGNAL
 CONDITIONER (SHEET 2 OF 3)

CONTINUED FROM SHEET 2



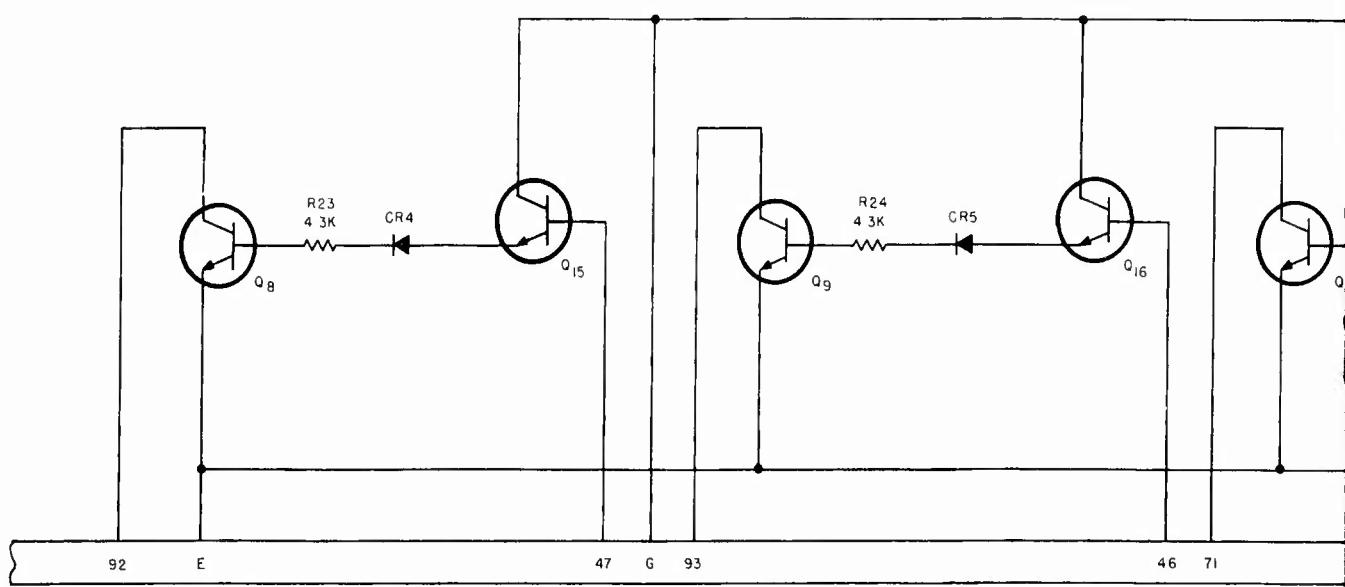
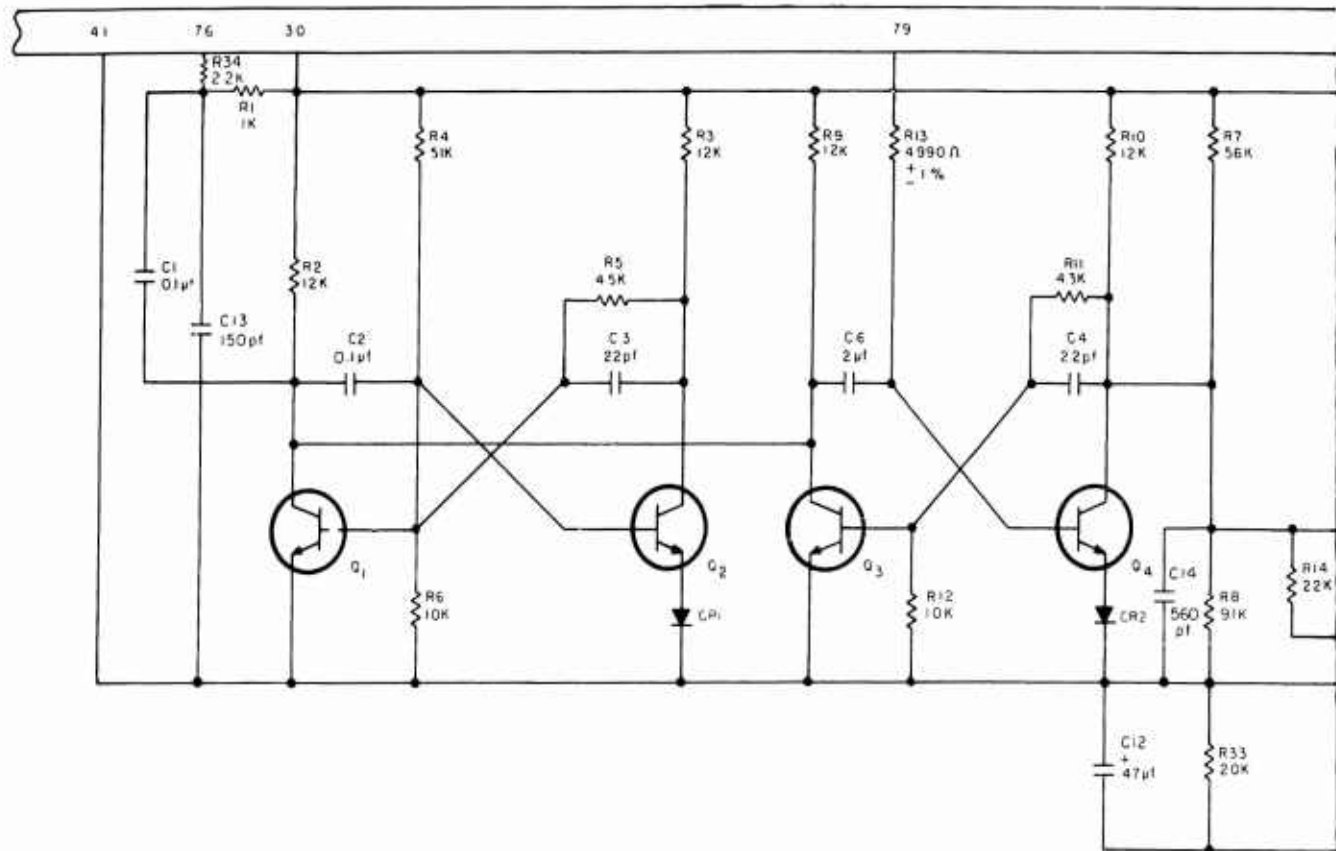
LOGIC CIRCUIT BOARD



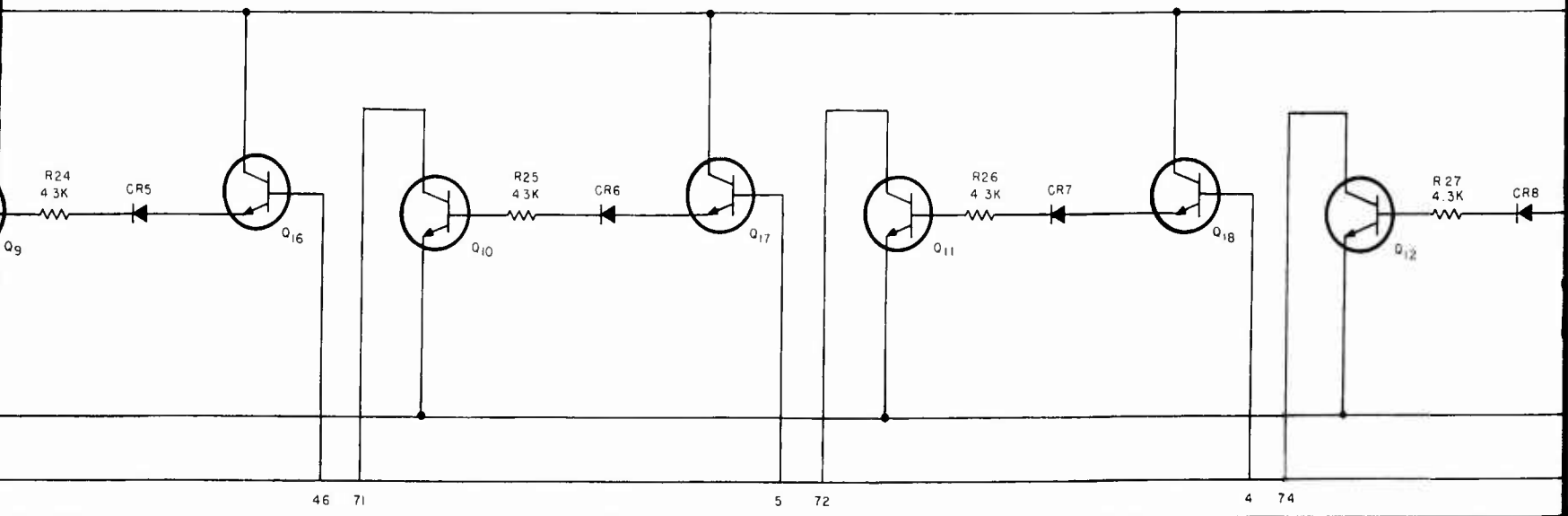
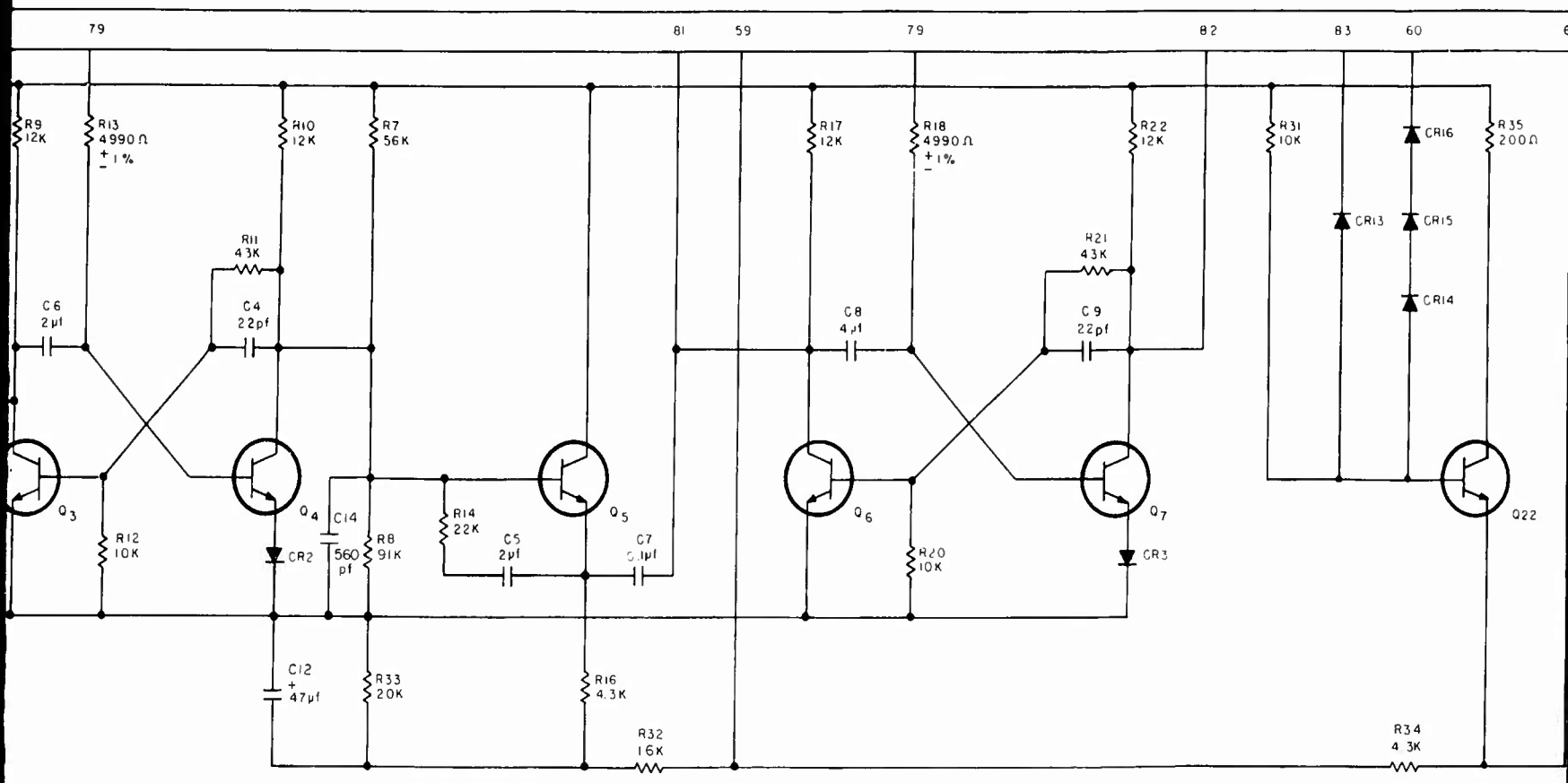


- NOTES:
- ① POWER INTERCONNECTIONS NOT SHOWN
 - ② R1 - R5 100K 1W POTS
 - ③ DELAY LINE ASSY NO'S: COIL MOUNT ASSY 4240-00147
PAD BASE 4240-00143
PAD COVER 4240-00144
 - ④ APW-16 RECEIVER DRAWING NUMBER 5223-94151
 - ⑤ APN-121 RECEIVER DRAWING NUMBER 4227-90568
 - ⑥ ALL TRANSFORMERS PCA ELECTRONICS TYPE AS SHOWN
 - ⑦ DELAY LINES: 0.5 µsec PCA TYPE DL1000D-0.5 RMT
4 µsec DWG NO 4240-00174
6 µsec DWG NO. 4240-00174
- ★ +150V AND -60V DC NORMALLY GO TO ALL OTHER CIRCUITS

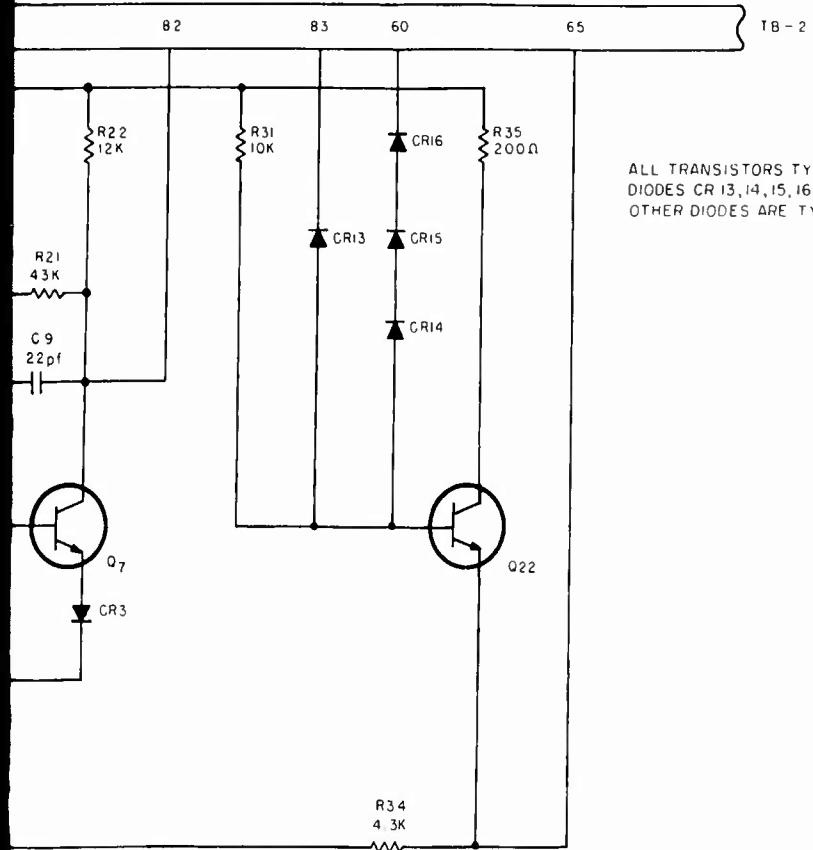
FIGURE 6-4
REPLY BACKGROUND NOISE GENERATOR AND SIGNAL
CONDITIONER (SHEET 3 OF 3)



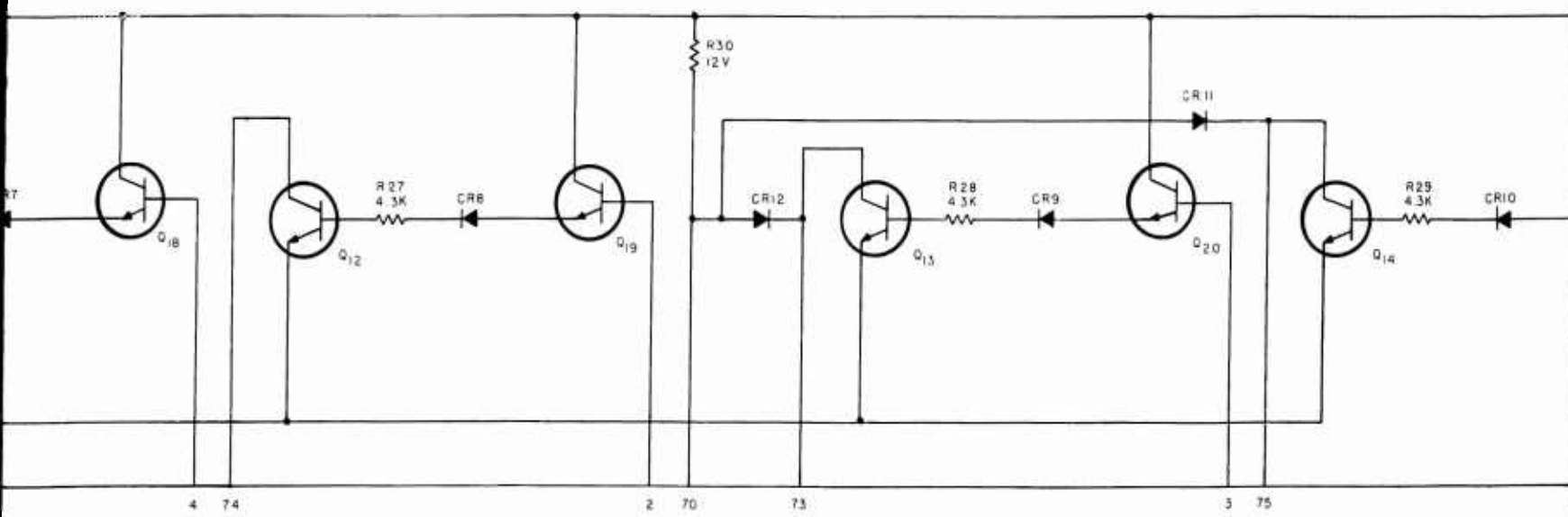
1



2



ALL TRANSISTORS TYPE 2N697
 DIODES CR13,14,15,16 ARE TYPE IN629
 OTHER DIODES ARE TYPE IN690



3

FIGURE 6-
 ANTENNA SCAN SIMULATOR AND CAS

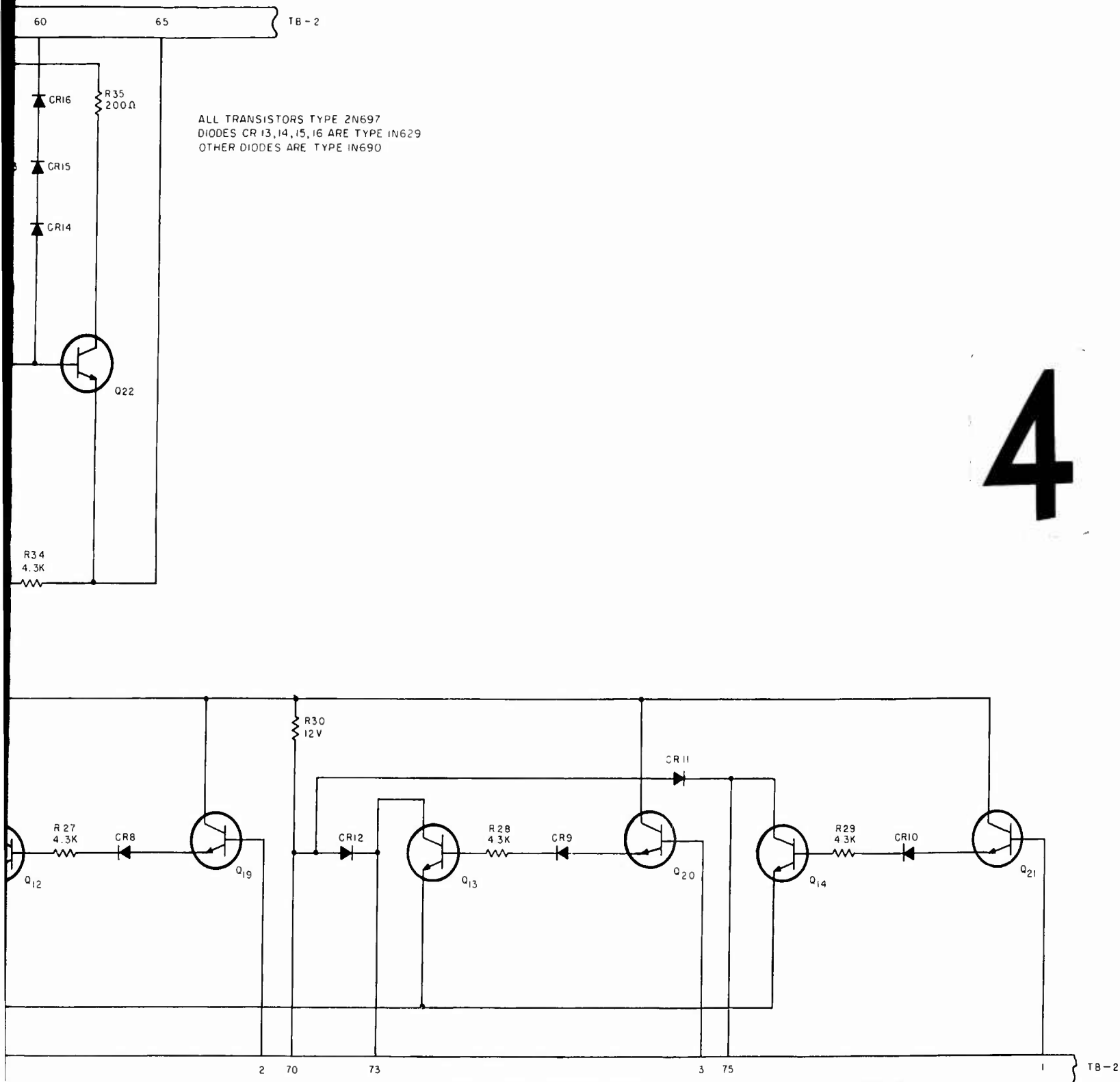
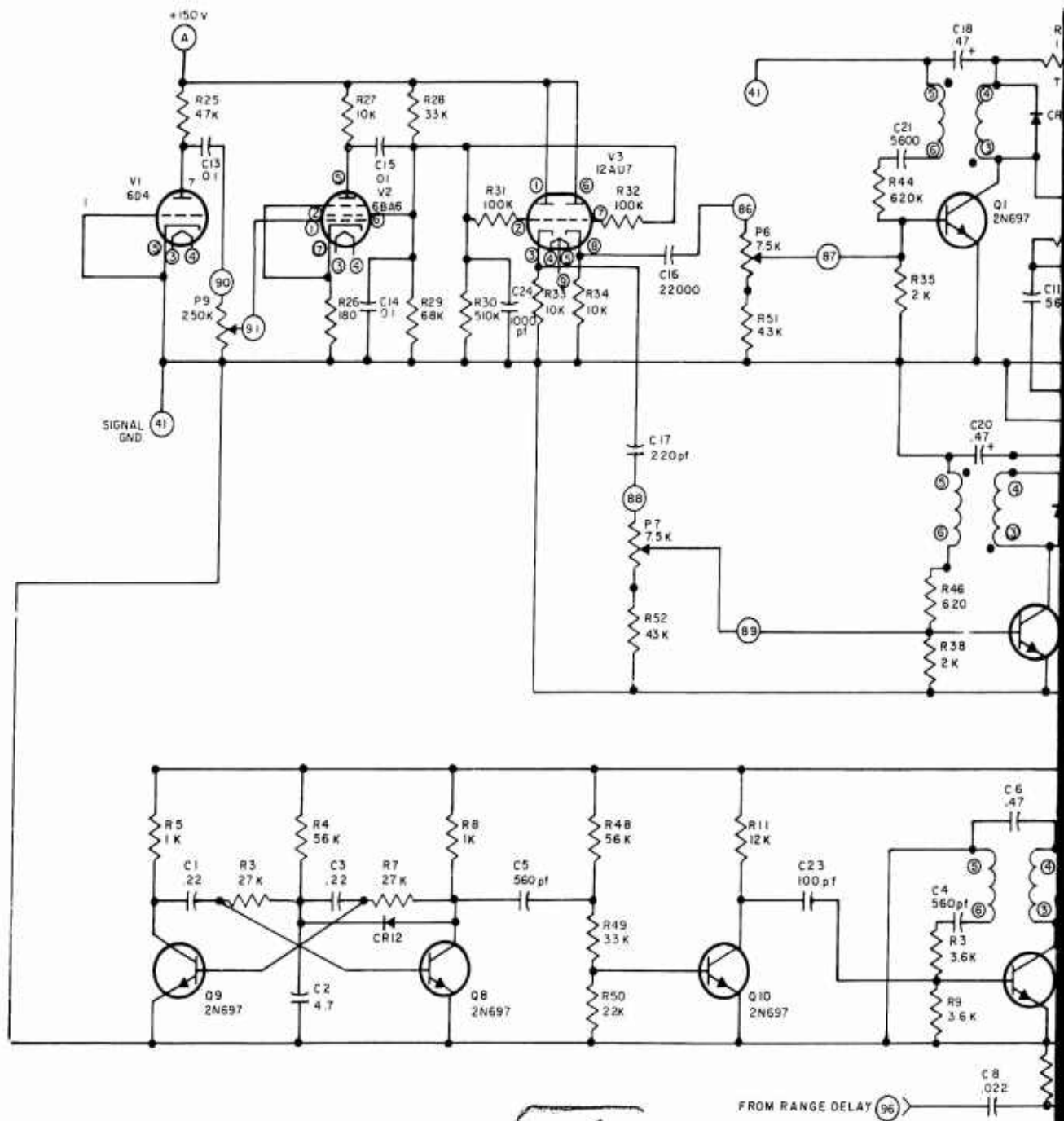
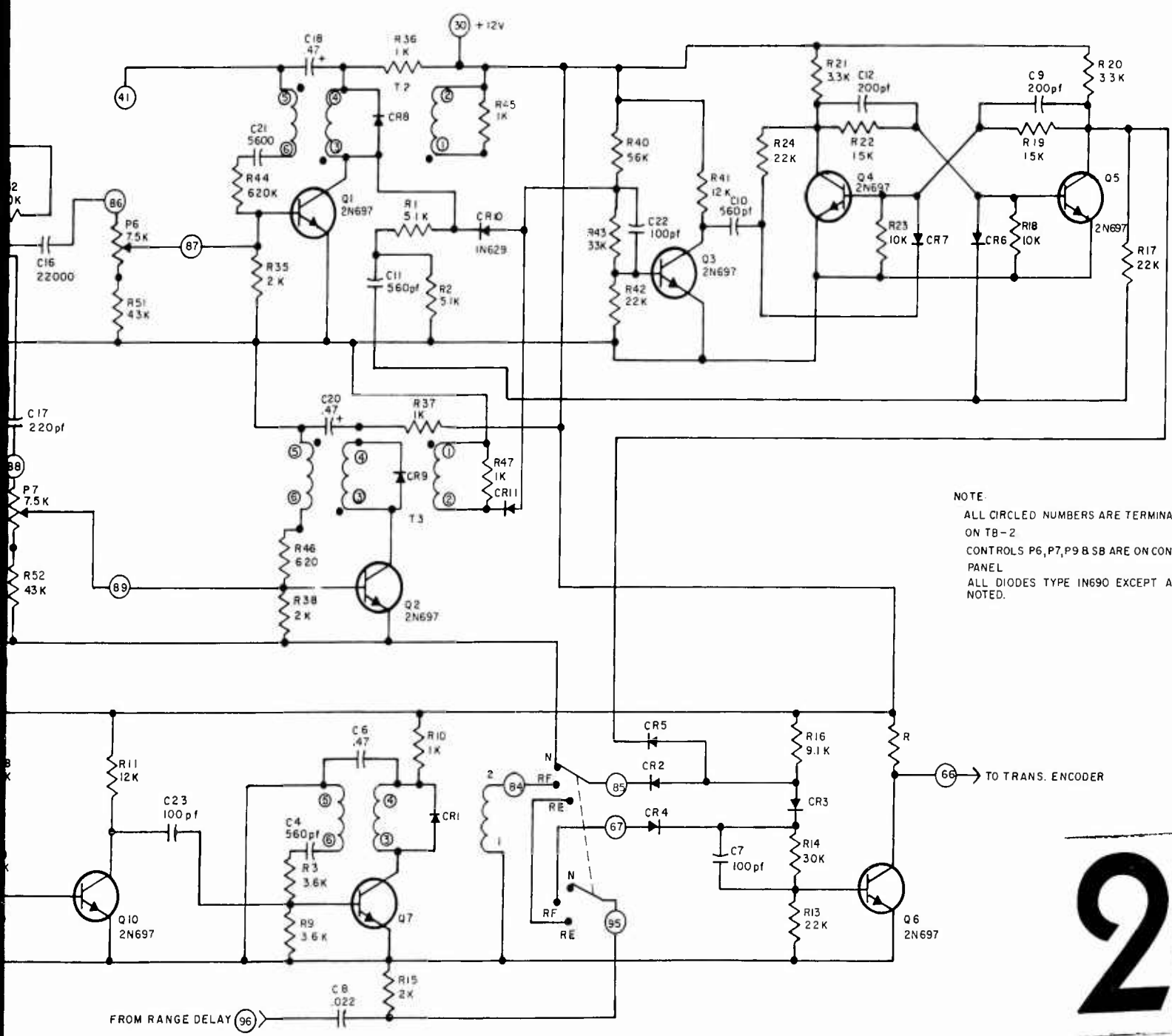


FIGURE 6-5.
 ANTENNA SCAN SIMULATOR AND CAS LIGHT INDICATOR CIRCUIT



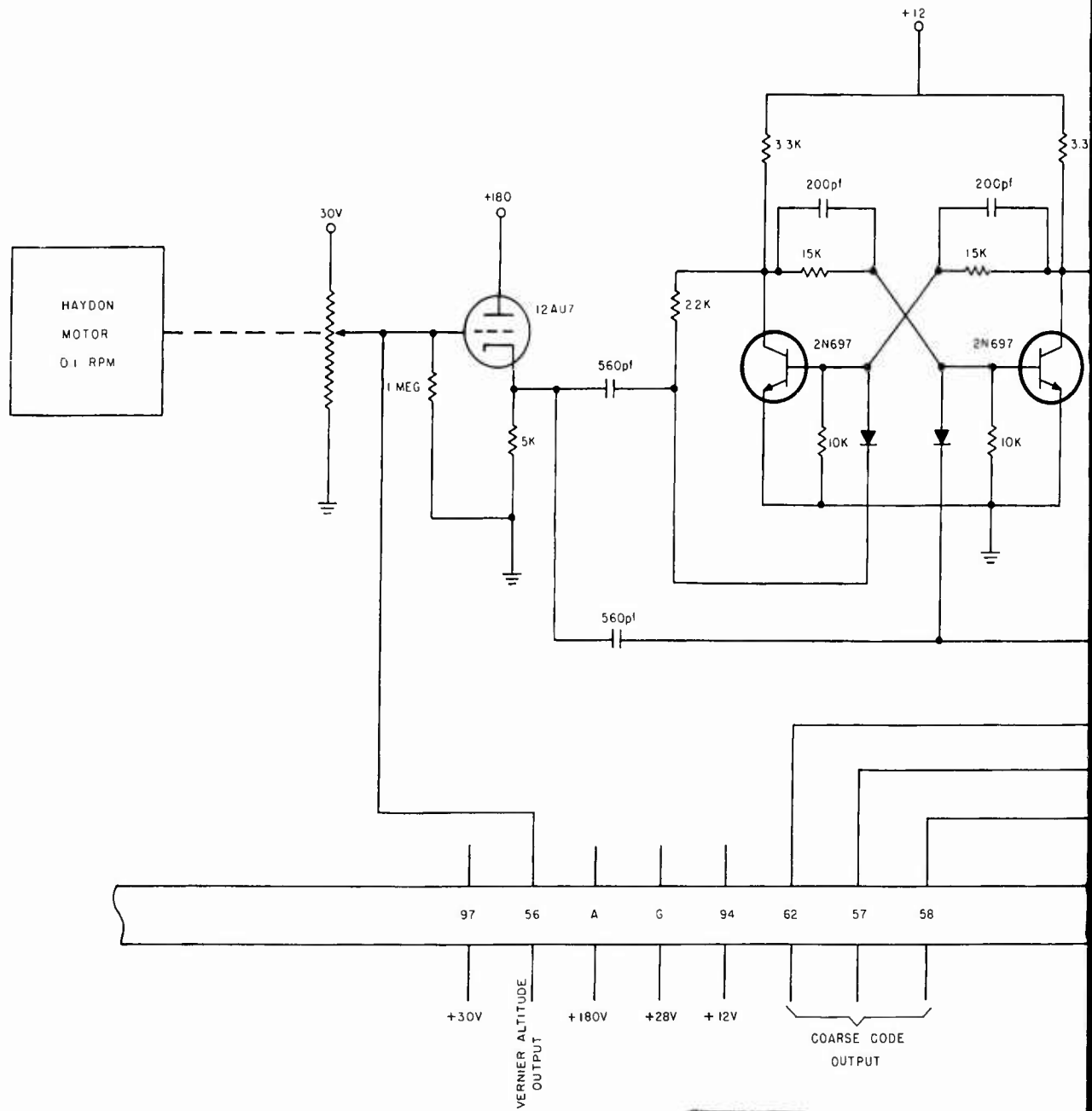
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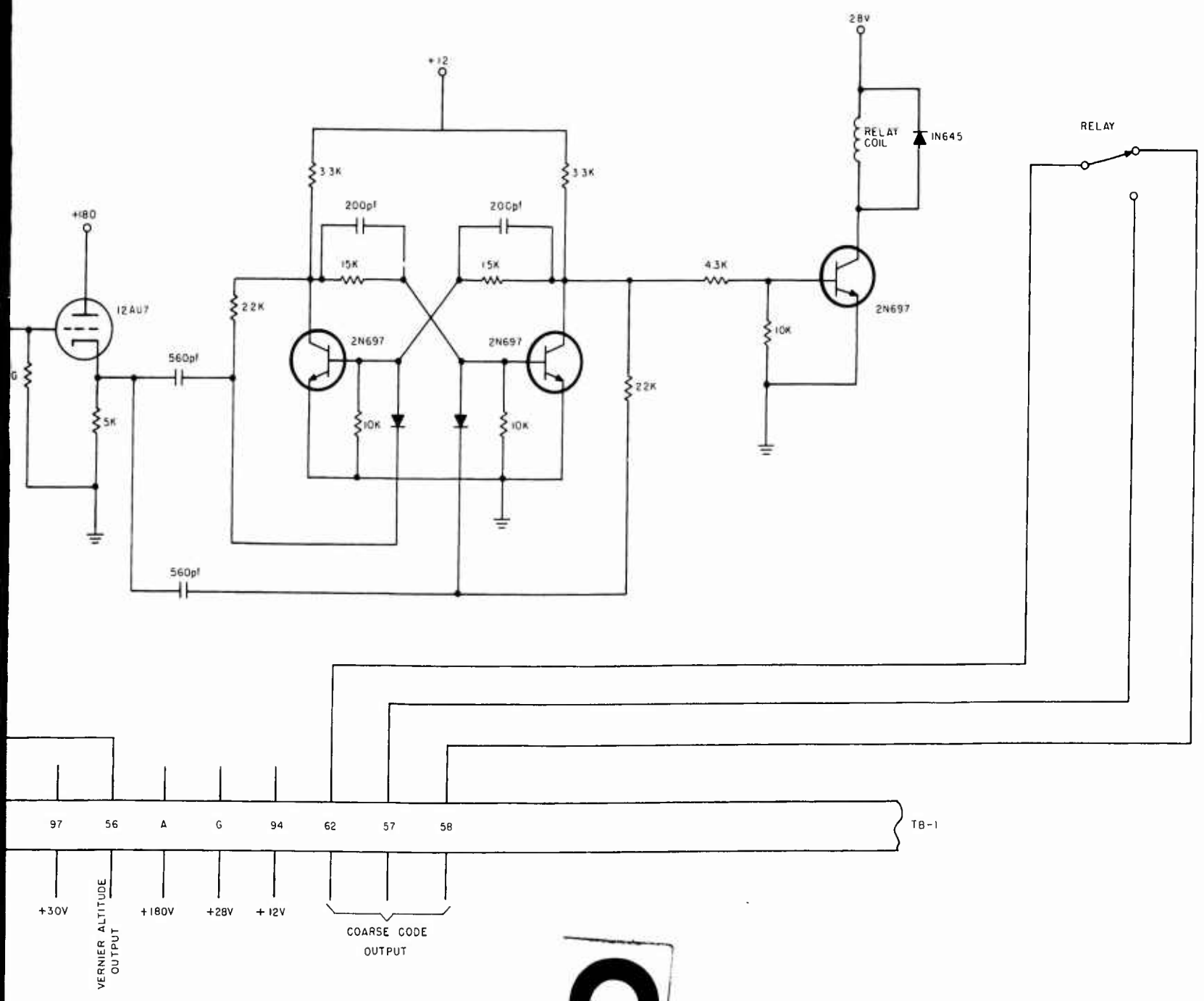
NOTE:
 ALL CIRCLED NUMBERS ARE TERMINALS
 ON TB-2
 CONTROLS P6,P7,P9 B 5B ARE ON CONTROL
 PANEL
 ALL DIODES TYPE IN690 EXCEPT AS
 NOTED.



FIGURE 6-6
 OVERHEARD REPLY GENERATOR



1



2

FIGURE 6-7. COARSE ALTITUDE CODE GENERATOR

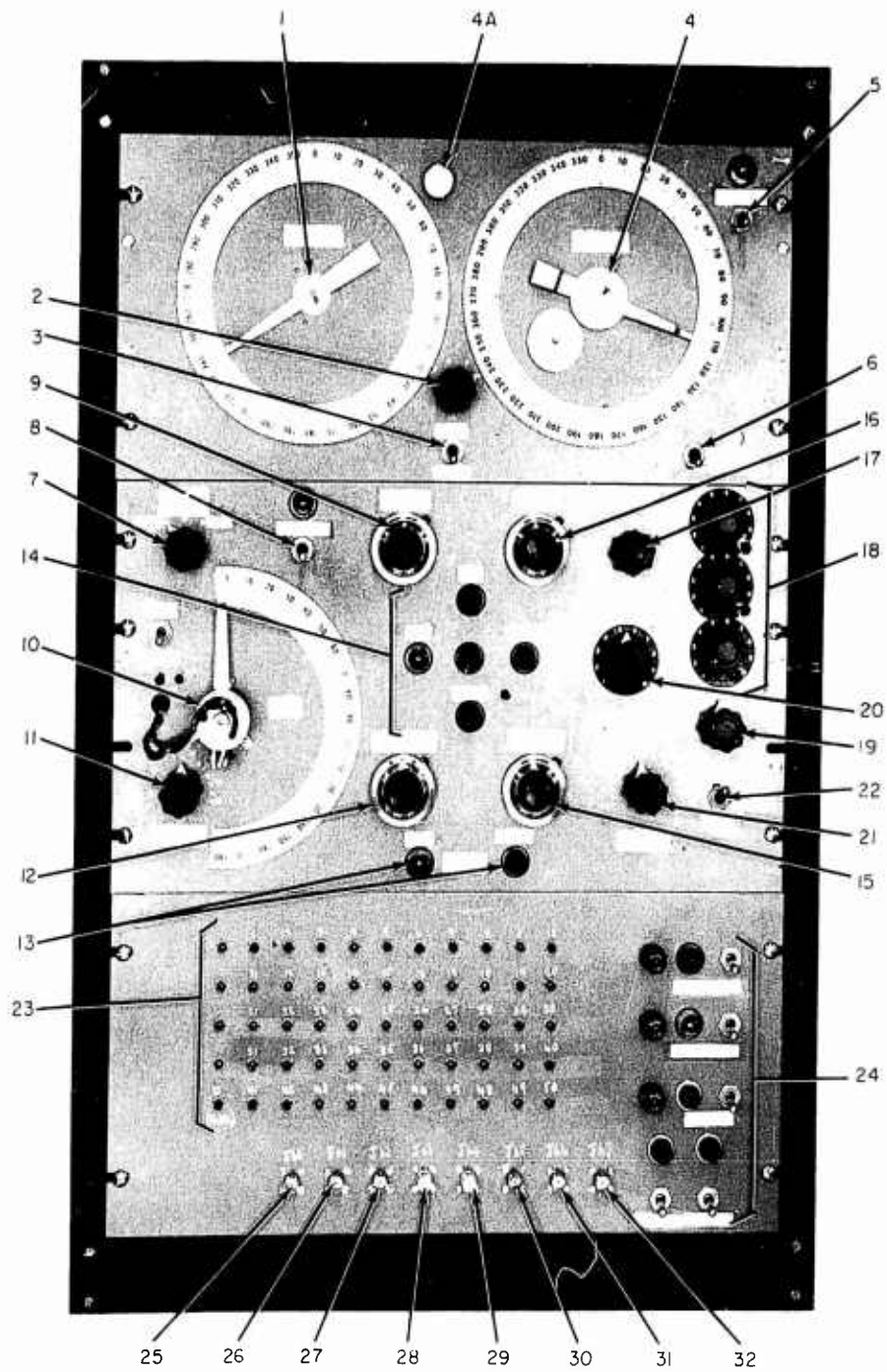


FIGURE 6 B. TEST RACK

- 16. Transponder Air Speed Control 0-300 Knots
- 17. Antenna Beam Width Control
- 18. Overheard Reply Noise Generator Density Controls

The bottom control in this group (P9) controls the output of the noise source and once it is set it can be left alone. The influence of P6 top control and P7 middle control is shown in the following listing:

To Reduce Number Of	P6	P7
Gates	Decrease	Decrease
Pulses	Decrease	Increase
To Increase Number Of	P6	P7
Gates	Increase	Increase
Pulses	Increase	Decrease

- 19. Overheard Reply Noise Generator Mode Switch

The positions on this switch have the following meanings:

- N Normal Triggers
- RF Overheard Reply Triggers Added to Normal Triggers
- RE Normal Triggers Interrupted by Random Gates

- 20. Transponder Altitude Rate Signal
CW rotation produces increasing rate of climb,
CCW rotation produces increasing rate of descent.
Gradient is 0.25v per 1000 feet per minute.
- 21. Transponder Coarse Altitude Selector Switch
- 22. Scan Simulator Mode Switch. RF., RE., positions not used
- 23. Test points associated with number designation of TB-3 on Test Rack Schematic Diagram
- 24. On-Off Power Switches
- 25. Transmit Trigger Pulses enter Test Rack from Interrogator Encoder
- 26., 27. Second Transponder Simulator Output Pulses. Not used.
- 28. Reply Video Input to Second Transponder Simulator. Not used.

- 29. Transmit Trigger Input to Second Transponder Simulator.
Not used.
- 30. Video Input from Interrogator Encoder to Transponder Decoder.
- 31. Delayed Transponder Reply Triggers Plus Overheard Reply Triggers.
- 32. Delayed Transponder Reply Triggers into Test Rack from Rutherford Range Delay Simulator.

B. ALIGNMENT

Instructions for alignment of the breadboard and test equipment, where adjustments are provided, are included here in the event that the adjustment is inadvertently changed or that some readjustment is required as the equipment ages. The instructions that follow for alignment of each circuit should be followed in the order given. In the cases where there are several adjustments made on one card the adjustments should be repeated until the desired result is obtained. This is necessary because some effects are influenced by more than one variable.

1. Test Equipment-Antenna Scan Simulator

Alignment of the antenna scan simulator is easily done by adjusting the bearing simulator synchro housing such that the synchro null lies at the center of the beam i. e. , at T_0 as is shown in figure 6-9. With this adjustment made as previously described the bearing pointer is set at 0 degrees on the scale and locked to the case. Thereafter, any rotation of the case will move the 0-degree null (and pointer) away from the beam center as desired for the purpose of setting relative bearing.

2. Breadboard Equipment

- 1100 Pulse and Gate Generator - Mixer Amplifier
 - R5 System Repetition Rate Adjustment (200 cps); Monitor J1101-M
- 1300 Vernier Coder
 - R14 Sweep Slope Adjustment; monitor J1301-S for a delayed pulse 40 usec from a pulse input at J1301-L when +30 volts is applied to J1301-P.
 - R25 Zero Set Adjustment; monitor J1301-S for a delayed pulse 20 usec from a pulse input at J1301-L when J1301-P is grounded.
 - R26 4-usec Adjustment; monitor J1301-R to obtain a pulse 4 usec prior to the pulse output of J1301-S for any voltage value (0 to 30 volts) input on J1301-P with a pulse input on J1301-L with no Maneuver Command from the computer.
 - R27 6-usec Adjustment; repeat R26 test with Maneuver Command input from computer on J1301-N to obtain a 6-usec spacing.

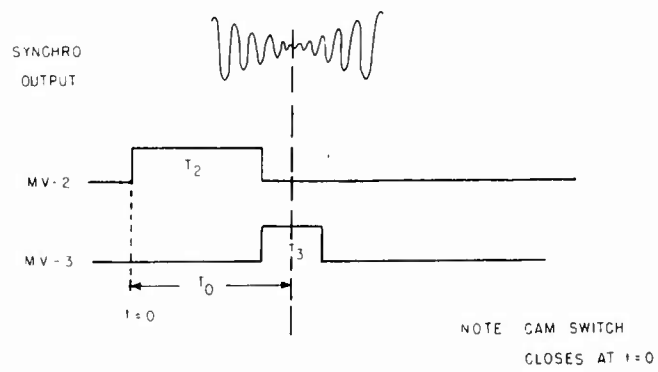


FIGURE 6 9. SCAN SIMULATOR ALIGNMENT

2500 A&B

North and East Velocity Decoders

- R25 & 39 Balance Control Adjustments; ground circuit between R-7 and C-5 and adjust R25 and R39 to give zero volts at J2501-M and -N respectively.
- R14 Slope Adjustment; with pulse inputs at J2501-K and -L at 30-usec spacing adjust R14 to give +12 volts and -12 volts at J2501-M and -N respectively (See Note 1)
- R24 Zero Set Adjustment; with pulse inputs at J2501-K and L at 10-usec spacing adjust R24 to give +12 volts and -12 volts at J2501-M and -N respectively (see Note 1).
(Note 1: Repetition rate of pulse inputs to be 200 cps (5000 usec) with positive and negative reset pulses of 7-usec duration at J2501-S and -R respectively appearing a minimum of 28 usec prior to the pulse input at J2501-K).

2600

Blanking Logic

- R3 Range Blanking Gate Width Adjustment; with a pulse input at J2601-R set R3 to give a 8-usec gate at J2601-J.
- R51 Maximum Range Gate Adjustment; with a pulse input at J2601-M set R51 to give a gate (X+28 usec long) at the collector of Q16, where X = 12.4 (desired max. range), in microseconds.

2700

Blanking Sweep Generator

- R25 Provide a jumper from collector of Q4 to ground. Adjust R-25 for a zero volts dc on pin X of J2701. Remove jumper.
- R24 Monitor the pulse output at J2801-M. Set the reply delay at short range and adjust R-24 such that the pulse at J2801-M precedes the reply trigger by 4-usec.
- R14 Repeat the procedure above except that the range delay should be set at about 200 usec and adjustment is made with R-14.

2800

Range Sweep Generator

- R25 Balance Control Adjustment; with circuit grounded between R-7 and C-5 set R26 to obtain zero volts at J2801-J.
- R14 Slope Adjustment; with pulse inputs at J2801-P and -L of 208-usec spacing adjust R14 to give +18 volts at J2801-J. (See Note 2)

R24 Zero Set Adjustment; with pulse inputs at J2801-P and -L of 40-usec spacing, adjust R24 such that the voltage at J2801-J crosses zero volts 28 usec after the pulse inputs at J2801-P. (See note 2)

(Note 2: Repetition rate of pulse inputs to be 200 cps (5000 usec) with positive reset pulse of 7-usec duration at J2801-R appearing a minimum of 36 usec prior to the pulse input at J2801-P).

R35 Blanking Pulse Zero Set; remove and ground lead to J2801-N, with pulse inputs at J2801-P and -L of spacing from 40 to 180 usec, adjust R35 to obtain a pulse output at J2801-M, 27 usec after the pulse input at J2801-P.

3200 A&B

North and East Velocity Coders

R17 Sweep Slope Adjustment; adjust R17 and monitor J3201-S for a delayed pulse 30 usec from a pulse input at J3201-L when +30 volts is applied to J3201-P.

R26 Zero Set Adjustment; adjust R26 and monitor J3201-S for a delayed pulse 10 usec from a pulse input at J3201-L when J3201-P is grounded.

R29 4-usec Adjustment; adjust R-29 and monitor J3201-R to obtain a pulse 4 usec prior to the pulse output of J3201-S for any voltage (0 to + 30 volts) input on J3201-P when +12 volts is applied to J3201-N.

R27 6-usec Adjustment; repeat as previously described but with R-27 and with lead to J3201-N open to obtain a 6-usec spacing.

4300

Band Decoder

R17 30-usec Gate Adjustment; lift and apply to Q-2 end of C-8 a negative trigger pulse, monitor the collector of Q-6 and adjust R-17 to obtain a 30-usec pulse.

4400

Two-Pulse Delay Generator

R17 Slope Adjustment; monitor emitter of Q-7 to obtain a 20-volt sweep in 50 usec with an input pulse to J4401-K. (R26 may require adjustment to obtain 50 usec)

R26 20-usec Adjustment; adjust R26 and monitor J4401-L to obtain a pulse 20 usec after the input pulse on J4401-K.

R60 40-usec Adjustment; adjust R60 and monitor J4401-M to obtain a pulse 40 usec after the input pulse on J4401-K.

4500

Three-Pulse Delay Generator

- R17 Slope Adjustment; monitor emitter of Q-7 to obtain a 20-volt sweep in 50 usec with an input pulse to J4501-K. (Note: R79 may require adjustment to obtain 50 usec.)
- R78 Mid-Pulse Adjustment; monitor J4501-R with +30 volts applied to J4501-M adjust R-17 and R78 for a pulse 40 usec after the pulse applied to J4501-K. Apply 0 volts to J4501-M and adjust R78 for a pulse 20 usec after the pulse applied to J4501-K.
- R79 Late-Pulse Adjustment; monitor J4501-P. Apply 0 volts to J4501-M and adjust R79 for a pulse 22.4 usec after the pulse applied to J4501-K.
- R80 Early-Pulse Adjustment; monitor J4501-S. Apply 0 volts to J4501-M and adjust R80 for a pulse 17.6 usec after the pulse applied to J4501-K.

A-3 Relative Bearing Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to transmitter rotor red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees (north).

Alignment Procedure for Differential

Connect differential to transmitter as shown with transmitter at 0 degrees. Rotate differential housing for a null across rotor black and yellow (low) leads. Rotation of the transmitter rotor shaft cw shall produce an increasing in-phase voltage across the differential rotor black and yellow (low) leads.

Alignment Procedure for Resolver Transmitter

Apply 26v, 400 cps to resolver transmitter rotor white-red and white-black (low) leads with white-yellow and white-black leads connected together. Rotate rotor for a null across red and black (low) leads of stator. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and red (low) leads of stator. This position is 0 degrees for the antenna train angle.

Alignment Procedure for Resolver

Connect resolver transmitter to resolver as shown with transmitter at 0 degrees. Rotate resolver housing for a null across rotor black and red (low) leads. Rotation of resolver transmitter shaft cw shall produce an increasing out-of-phase voltage across resolver rotor black and red (low) leads.

Alignment Procedure for Sine-Cosine Pot

With transmitter at 0 degrees connect 3 volts dc across 1 and 3 (low). Connect a d-c voltmeter across 1 and 4. Rotate potentiometer housing for a null, connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 8 to 3, 6 to 3, 7 to 3, which shall be 15v dc and 2 to 3 which shall be a null.

A-4 Magnetic Bearing Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads of stator. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees, $(\theta' + \theta_c + \alpha) = 0^\circ$

Alignment Procedure for Sine-Cosine Pot P1

With transmitter at 0 degrees connect 3 volts dc across 1 and 3 (low) connect a dc voltmeter across 1 and 2. Rotate potentiometer housing for a null. Connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 7 to 3, 8 to 3, 6 to 3. which shall be 1.5v, while 4 to 3 shall be a null.

Alignment Procedure for Sine-Cosine Pot P2

The potentiometer shafts of P1 and P2 should be aligned by the vendor. To check alignment repeat the same test for P1 as previously described.

Operational Amplifiers

All of the operational amplifiers are nulled by the following procedure. Special conditions for the particular amplifier being adjusted are as follows:

Test Conditions

A-7 Velocity Integrators

Short A-7-T and V to Ground. Open A-7 P. Add 100K ohm resistor across each 0.33 μ f capacitor. Proceed with adjustments.

A-8 Normal Velocity Adder

Open terminals P8-V, X, T. Short 1-megohm resistor from P8-V to ground. Proceed with null adjustments.

A-9 Radial Velocity Adder

Open terminals P9-V, X, T. Short 1-megohm resistor from P9-V to ground. Proceed with null adjustments.

A-10 Range Adder

Open terminal P10-T, short circuit 820-ohm resistor of input bias circuit on A-10 card. Proceed with null adjustments.

Nulling Procedure

Place a one-millivolt meter from the amplifier output terminal to the summing junction. This meter input must be isolated from ground. Place another millivolt meter from the output terminal of the amplifier to ground. Alternately adjust the offset potentiometer at the rear of the card and the current null potentiometer located at the center of the card to produce readings as near zero as possible on both meters.

A-24 Heading Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to rotor of transmitter red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low), this position is 0 degrees (north).

Alignment Procedure for Control Transformer (CT)

Connect transmitter to CT as shown. With transmitter at 0 degrees rotate housing of CT for a null across CT rotor leads white-red and white-black (low). CW rotation of transmitter shaft shall produce an increasing in-phase voltage across white-red and white-black (low) leads.

Alignment Procedure for Sine-Cosine Pot

Disconnect all leads from terminal 3 on potentiometer. Connect 3v dc across 1 and 3 (low) (transmitter at 0 degrees). Rotate potentiometer housing for a null across 1 and 2. Connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 6 to 3, 8 to 3, 7 to 3, which shall be 1.5v while 4 to 3 shall be a null. Reconnect wires to terminal 3. The pot and switch shafts are aligned by the vendor. To check alignment, connect an ohmmeter across 1 and 2 of S1 with the 0-degree condition previously described. If there is continuity, no more than three turns ccw of the slotted journal of the gear train shall break continuity. If there is no continuity, no more than four turns cw shall produce continuity. With 3v dc across 1 and 5 (low) of pot, rotate slotted journal ccw for a null across 6 to 1. Check alignment of S2 the same as S1 previously described. Rotate slotted journal cw for a null across 1 and 2 of pot. The CT a-c voltage F to A (low) shall be at a null. Rotation of the slotted journal ccw shall produce an out-of-phase voltage across CT output F and A (low).

A25 Altitude Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v. 400 cps to transmitter rotor red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads of stator. CW rotation of the rotor shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees (zero altitude).

Alignment Procedure for Potentiometer P1

For zero altitude, wiper 2 must be 250.2 degrees cw from terminal 3. To accomplish this the set-up in figure 6-10a is used. Select a value of $R_1 = 10K$. Then R_2 will be

$$R_2 = 10K \times \frac{356.4}{250.2} - 10K$$

$$R_2 = 4244\Omega$$

Connect R_1 and R_2 as shown in figure 6-10a. Rotate housing of P1 for a null on voltmeter. Resistors should be $\pm 1\%$ or less.

Alignment Procedure for P2

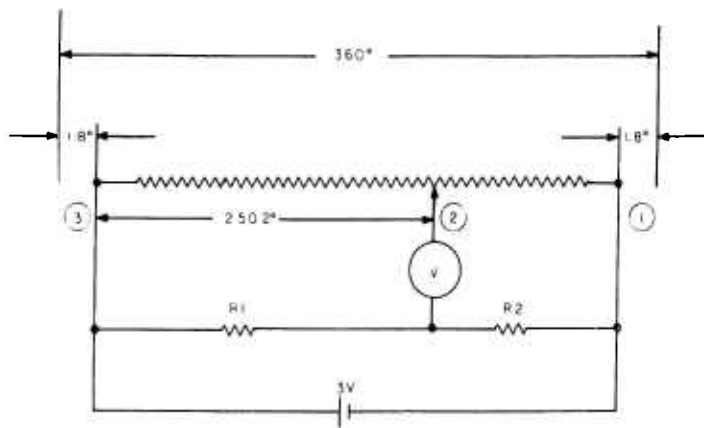
The wiper of P2 shall be 180 degrees away from wiper of P1. This should be done by the vendor. To check it use the set up in figure 6-10a. The wiper will be at 70.2 degrees; therefore

$$R_2 = 10K \times \frac{356.4}{70.2} - 10K$$

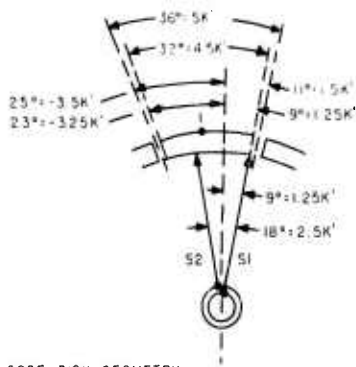
$$R_2 = 40767\Omega$$

Alignment Procedure for Code Wheel Commutator

From the geometry of figure 6-10b, it is seen that for zero altitude, brush S1 is at the edge of segment 1 of the commutator. Set transmitter for 0 degrees (zero altitude). Connect an ohmmeter (on the R x 100 scale) across 1 and S1. Rotate code wheel housing ccw until continuity just exists. There should be continuity from 1 to S2. If there is not, rotate housing ccw until continuity just disappears across 1 and S1.



A TEST CIRCUIT FOR ALTITUDE POTENTIOMETERS



B ALTITUDE CODE DISK GEOMETRY.

FIGURE 6-10. ALTITUDE SERVO ALIGNMENT