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A General Analysis of the False-Lock Problem Associated with the Phase-Lock Loop

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Prepared for COMMANDER SPACE SYSTEMS DIVISION
UNITED STATES AIR FORCE
Inglewood, California

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This technical documentary report has been reviewed and is approved for publication and dissemination. The conclusions and findings contained herein do not necessarily represent an official Air Force position.

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ABSTRACT

An approximate analysis is made of phase-lock loop false locks as determined by the gain-phase characteristics of the phase-lock loop. The solutions presented enable the calculation of the false-lock frequencies if the open-loop phase characteristic is known. A simple design criterion is suggested to permit the design of a loop with no stable locks other than the desired lock frequency.

CONTENTS

FIGURES

I. INTRODUCTION

A general block diagram of a phase-lock loop is shown in Fig. 1. The equivalent diagram generally employed to analyze this phase-lock loop is shown in Fig. 2. In this paper, all of the zeros[1] (frequencies of the voltage-controlled oscillator for which the loop will remain in stable lock) of a phase-lock loop for a given input frequency, f_i, are determined using the loop of Fig. 1.

A nomenclature of symbols is presented at the end of the paper.

II. ANALYSIS

A convenient approach to the determination of all of the zeros of a phase-lock loop is to open the loop at the input to the operational amplifier and manually sweep the voltage-controlled oscillator (VCO), while examining the output of the phase detector. This can be easily accomplished in the laboratory by placing a capacitor between the phase detector and the operational amplifier. This practice keeps the loop closed for ac but open for dc. Figure 3 illustrates the method employed.

For simplicity, the phase and amplitude characteristics of the mixer and IF amplifier are included in the bandpass filter, F_1.

The phase detector of Fig. 1 is replaced by a subtractor, followed by a gain of K_0, and the VCO is replaced by an integrator of gain K_1.

Figures 4 and 5 show the frequency components of interest at various points in the loop of Fig. 3. In construction of Fig. 4 and 5, it has been

[1] This is probably the same phenomenon described by R. Leek, "Phase-Lock A.F.C. Loop," Electronic and Radio Engineer (Great Britain) (April 1957).

assumed that only first-order sidebands are of importance, i.e., that the VCO modulation index is small. This is usually a good approximation for values of the beat frequency larger than the loop bandwidth.

For the situation depicted in Fig. 4, it is evident that

$$\gamma + \phi_1 + \delta_2 = \phi_2 \tag{1}$$

The lower sideband phase (ϕ_{LSB}) is given by

$$\phi_{LSB} = \gamma - \phi_3 + \pi + \phi_1 + \delta_1 \tag{2}$$

Thus,

$$\phi_{LSB} = \phi_2 - \phi_3 + \pi + \delta_1 - \delta_2 = \pi - \alpha_1 \tag{3}$$

and

$$V_{o_{dc}} = \beta \cos \phi_{LSB} = \beta \cos (\phi_2 - \phi_3 + \pi + \delta_1 - \delta_2) = \beta \cos (\pi - \alpha_1) \tag{4}$$

where β is a composite amplitude function resulting from the two-phase functions $\phi_2 - \phi_3$ and $\delta_1 - \delta_2$, as well as from the changing sideband amplitude resulting from the VCO input varying in amplitude and frequency. It has been assumed that the phase detector is characterized by

$$V_{o_{dc}} = A \cos \Delta\phi$$

where A is the signal input amplitude and $\Delta\phi$ is the phase difference between the signal and reference. Higher order sidebands are of little concern since

they neither correlate to produce a $V_{o_{dc}}$ contribution nor appreciably affect the carrier phase when the VCO modulation index is small.

A similar analysis for the upper sideband (ϕ_{USB}) case depicted in Fig. 5 yields

$$\phi_{USB} = \phi_3 - \phi_2 + \delta_3 - \delta_2 = \alpha_2 \tag{5}$$

Thus

$$V_{o_{dc}} = \beta \cos \phi_{USB} = \beta \cos (\phi_3 - \phi_2 + \delta_3 - \delta_2) = \beta \cos \alpha_2 \tag{6}$$

Equations (4) and (6) represent the principal results of this paper. To illustrate their utility, typical β and α curves for a phase-lock loop are shown in Fig. 6(a) and 6(b), and the resulting $V_{o_{dc}}$ curve is shown in Fig. 6(c). From Fig. 6(c), it is seen that zeros occur at all frequencies for which the loop phase shift α is equal to $\pi/2$, $3\pi/2$, $5\pi/2$, $7\pi/2$, and $9\pi/2$. The zeros are alternately stable and unstable, beginning with an unstable zero at $\pi/2$. Clearly, if the phase shift were not bounded,[2] as would be the case for a true transportation lag, there would be an infinity of zeros[3] occurring at $(2n - 1)\,\pi/2$, $n = 1, 2, 3, \ldots$. Again, these zeros would be alternately stable and unstable, beginning with an unstable zero at $\pi/2$.

Equations (4) and (6) also give insight into the effect of loop bandwidth on the problem. Commonly, loop bandwidth is changed by changing G(s). The G(s) function is usually of the lead-lag type. Thus, as the bandwidth is increased, the G(s) transmission is increased (assuming constant damping),

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[2] John G. Truxal, Automatic Feedback Control System Synthesis (McGraw-Hill Book Company, Inc., New York, 1955), Section 9.8, pp. 546-553.

[3] The idealized transportation lag problem has been solved by Jean A. Develet, "The Influence of Time Delay on Second-Order-Phase Lock Loop Acquisition Range," Report No. 9382.6-9, Space Technology Laboratories, Inc., Los Angeles (1 September 1962).

with a resulting increase in β at any given frequency. The net result is a slight shift in the zeros and an increase in the magnitude of the false peaks. Hence, the wider the loop bandwidth, the greater the stress necessary to ride over the false peaks. This leads one to the conclusion that perhaps a more optimum G(s) function [e.g., another pole in the G(s) function] might be employed to reduce the effect.

III. CONCLUSIONS

A solution for all the zeros of a phase-lock loop has been presented. The solution permits the prediction of the location of these zeros if knowledge of the open-loop characteristics is obtainable. The solutions are generally applicable to any phase-lock loop of the type shown in Fig. 1.

The solutions obtained suggest a simple design criterion to avoid the false-lock problem. It is necessary merely to keep the value of α less than $\pm\pi/2$ within the allowable range of VCO frequencies. If this is not feasible, it is necessary to compute the β and α functions to properly set the magnitude of the stress necessary to override the false peaks.

NOMENCLATURE

f_1	Input frequency to phase-lock loop
f_2	Local oscillator frequency
f_3	Beat frequency appearing at phase detector output
f_4	VCO carrier frequency
α	α_1 for $f_1 - f_4 > f_2$
α	α_2 for $f_1 - f_4 < f_2$
β	Sideband amplitude function
γ	Phase of f_4 at $t = o$
δ_1	Phase shift at the VCO lower sideband frequency through mixer, IF, filter and phase detector
δ_2	Phase shift at the VCO carrier frequency through the mixer, IF, filter and phase detector
δ_3	Phase shift at the VCO upper sideband frequency through the mixer, IF, filter and phase detector
ϕ_1	Phase of f_1 at $t = o$
ϕ_2	Phase of f_3 at input of G(s) at $t = o$
ϕ_3	Phase of f_3 at output of G(s) at $t = o$
$\phi_{LSB} = \pi - \alpha_1$	Lower sideband phase shift ($f_1 - f_4 > f_2$)
$\phi_{USB} = \alpha_2$	Upper sideband phase shift ($f_1 - f_4 < f_2$)

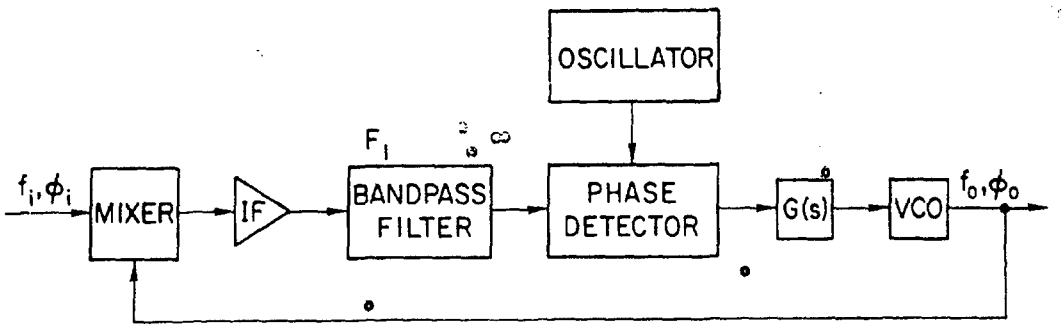


Fig. 1. Block Diagram, Phase-Lock Loop

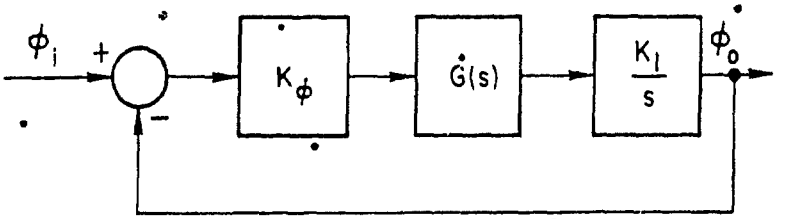


Fig. 2. Equivalent Block Diagram, Phase-Lock Loop

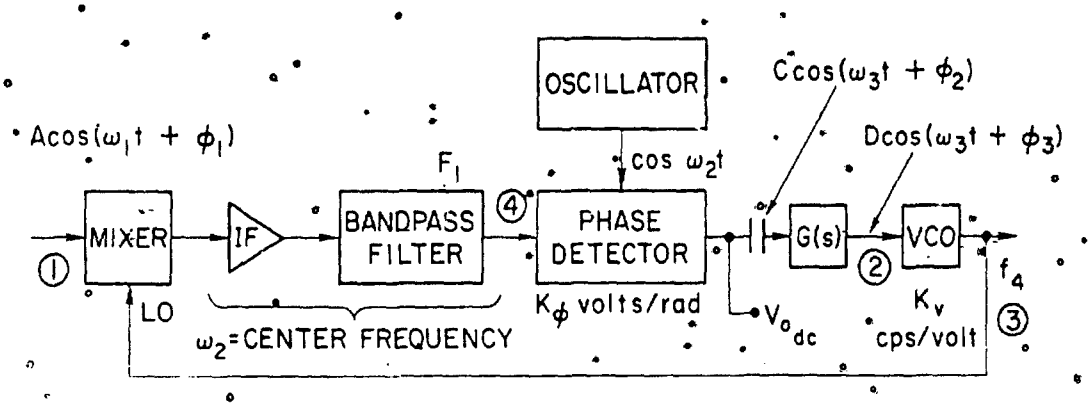


Fig. 3. Laboratory Test Configuration, Phase-Lock Loop

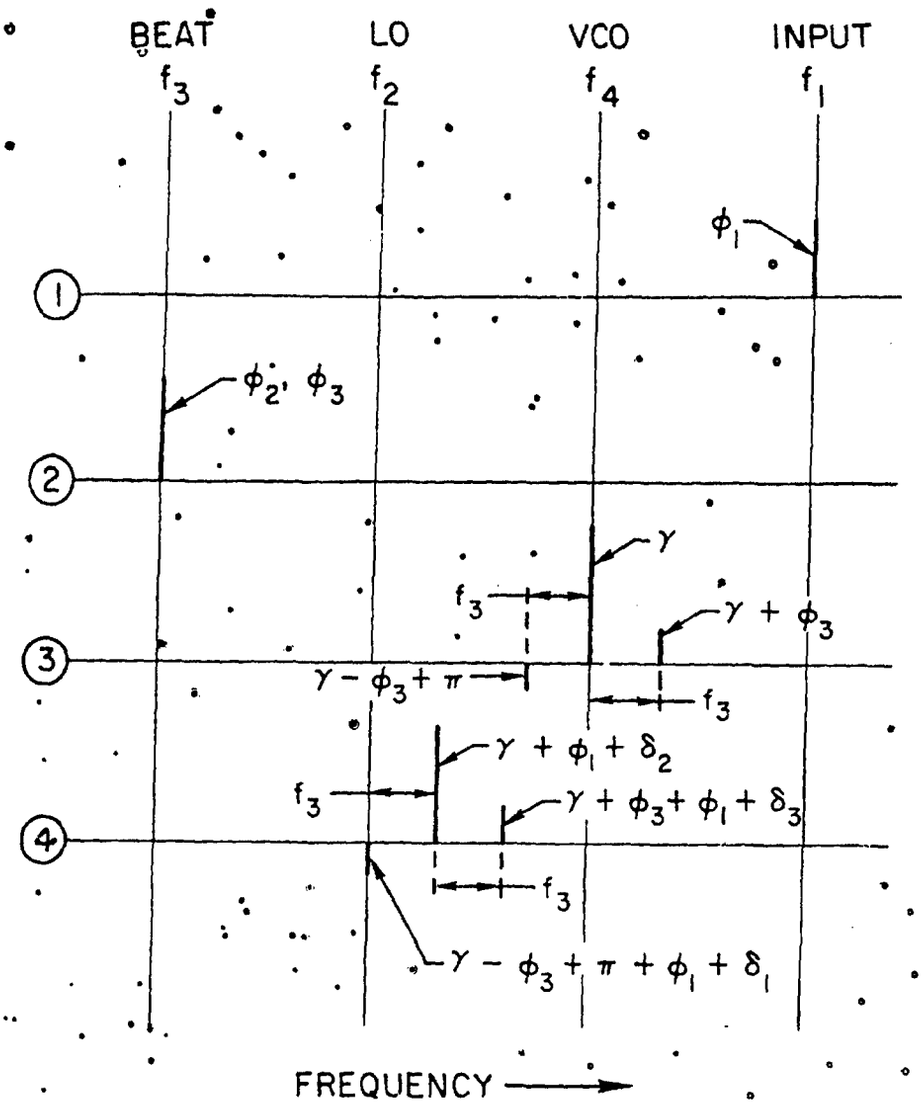


Fig. 4. Phases of Frequency Components, $f_1 - f_4 > f_2$

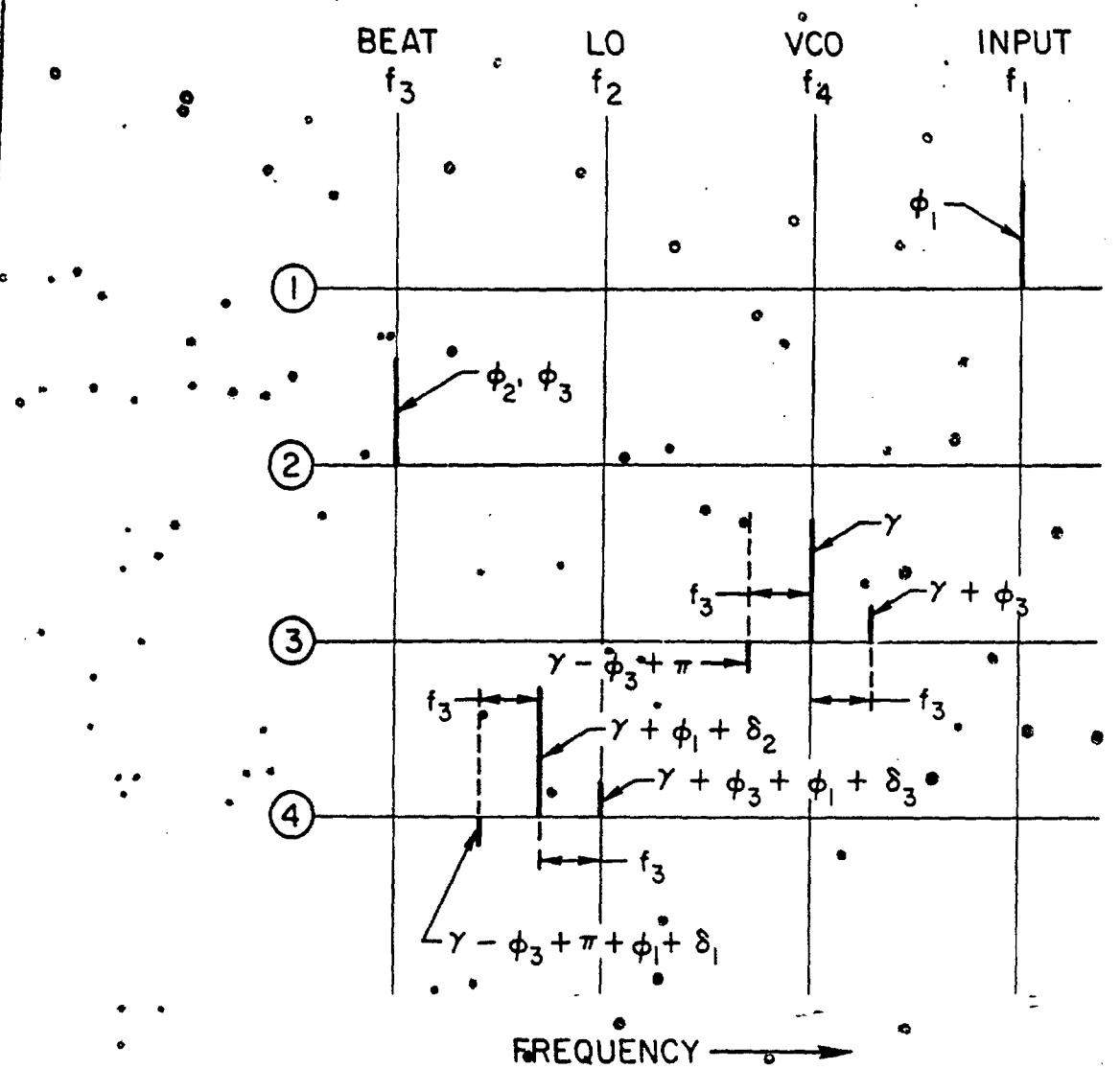
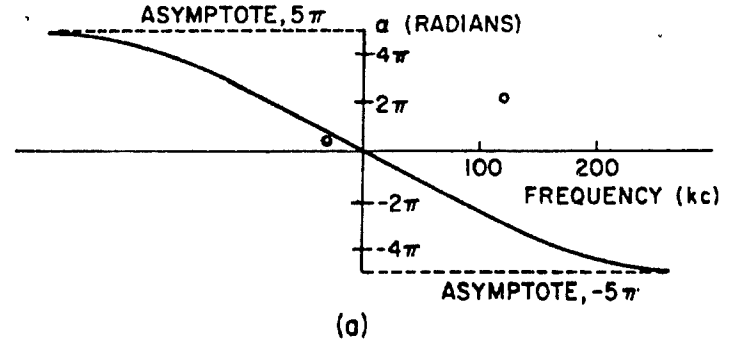
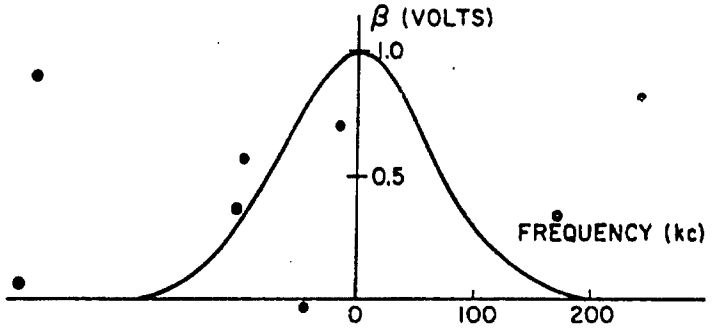


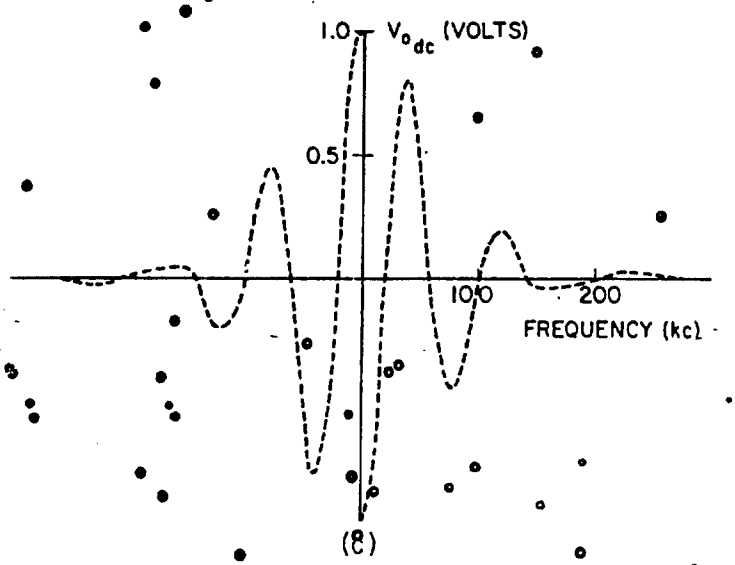
Fig. 5. Phases of Frequency Components, $f_1 - f_4 < f_2$



(a)



(b)



(c)

Fig. 6. Zeros of a Typical Phase-Lock Loop

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