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64-11

PRODUCTION ENGINEERING MEASURES TO INCREASE TRANSISTOR RELIABILITY

FOURTH QUARTERLY PROGRESS REPORT

FOR THE PERIOD
APRIL 1, 1963 THRU JUNE 30, 1963

CONTRACT NO. DA-36-039-SC-86730
ITEM 4

PLACED BY
U.S. ARMY ELECTRONICS MATERIEL AGENCY
PHILADELPHIA, PENNSYLVANIA

433496

03-64-16

TEXAS INSTRUMENTS INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
DALLAS, TEXAS

PRODUCTION ENGINEERING MEASURES TO INCREASE TRANSISTOR RELIABILITY

FOURTH QUARTERLY PROGRESS REPORT

FOR THE PERIOD

APRIL 1, 1963 THRU JUNE 30, 1963

OBJECT:

To evaluate and adopt proposed process improvements toward achieving a maximum failure rate of 0.01% per 1,000 hours at a 90% confidence level for the Silicon Triple Diffused Transistor Type 2N656.

CONTRACT NO. DA-36-039-SC-86730

ORDER NO. 19052-PP-62-81-81

CONTRACT ITEM 4, 2N656

Earl Gomersall - Power Department Manager

Elmer Wolff - Branch Manager of Power Department Engineering

Milton K. Mack - Power Department Section Head

James H. Overman - Power Department Group Leader

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SECTION I

ABSTRACT

The process improvement work on the 2N656 device has been completed. Thermal resistance measurements indicate a power dissipation capability of 15 watts at 100°C case temperature. The Planar device improvements include "hard" gold alloy wafer mounting, ultrasonically cold-bonded contacts, and an improved "slug" package. Varnishes and organics have been completely eliminated from the inside of the package. Purity of the encapsulated atmosphere is assured by a thorough cleaning and baking of all parts and by rigid control of the assembly and canning dry-box atmosphere. The aluminum wafer contacts are never exposed to etchants. Corrosive chemicals have been eliminated from the assembly process. Improved processes in the diffusion, photo resist, etch, evaporation and plating areas have contributed to significantly increased product yields, quality and uniformity.

These process improvements have not only upgraded the 2N656, but also made possible the EIA reservation of a new device series, 2N2987 to 2N2994 — rated at 25 nanoamperes maximum I_{CEX} at 150% of rated BV_{CEO}. Saturation properties and current-carrying capabilities have been sufficiently improved such that V_{BE} and $V_{CE(sat)}$ are specified at a collector current of 500 milliamperes as compared to the 200 milliampere rating of the Mesa 2N656.

SECTION II

PURPOSE

The purpose of the work provided in this contract is to:

1. Evaluate and adopt improved production processes.

2. Determine the degree of improvement in the operating failure rate resulting from the process improvements.

3. Supply the specified number of engineering test samples and reports to confirm the progress toward or attainment of the contract objective.

SECTION III

NARRATIVE AND DATA

1. This section covers the engineering progress made during the fourth quarterly period of the contract. The engineering work items shown in the program plan, Table 1, have been completed.

Results of tests conducted in the first production planar devices were so impressive that all process improvement work performed during the fourth quarter was concentrated on the planar device. Work was discontinued on the mesa processes because it was felt that work in that area would detract from the process optimization effort on the planar device which has potential of much greater reliability. It should be noted that all 2N656 mesa devices produced since the start of this contract have benefited greatly from the process improvement work on this device series. The mesa has enjoyed the benefits of: improved photo-resist and diffusion processes; oxide-protected emitter-base junctions; improved processes for preparing collector side of the wafer; improved control over slug and crimp location; and improved electrical parameter data handling for process control. All tests that have been conducted on the mesa 2N656 series show that the quality and reliability have improved significantly since the start of the contract. However, it is felt that the mesa device will be rapidly replaced by the planar in all higher reliability applications as soon as availability of the planar is announced and reliability data distributed. The following narrative details the progress made on each of the items in the order they appear in Table 1.

1.01 Uniform Penetration in Diffusion — Dale Bennett, Edmond McGhee

The improved diffusion and photo-resist facilities continue to produce high quality material at steadily increasing yields.

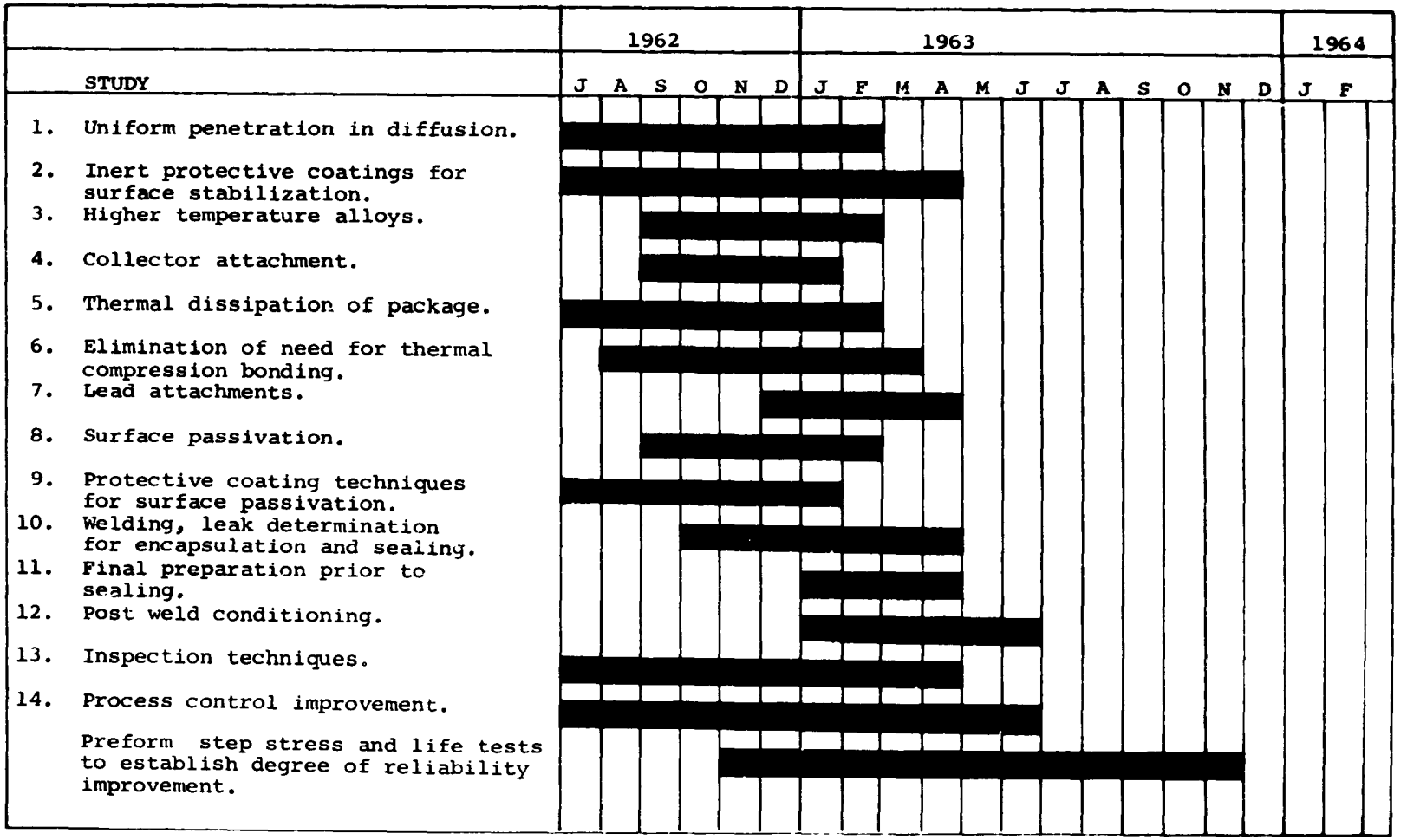
Planar diffusion processes have stabilized at reasonable production levels. Tests are in process to further improve yields by determining the optimum base penetration to get as far as practical below the mechanically disturbed silicon surface without sacrificing any of the electrical characteristics. The results of this work will come too late for any deeper base devices to be included in the reliability tests that will be conducted during the fifth and sixth quarters. However, experience has shown that the depth of the base has little, if any, effect on device reliability; but it may have a significant effect on yields and therefore affect costs. The improved cost situation will enhance the mass production capabilities of the planar device at prices competitive with the mesa, thus the decision was made to continue this engineering effort into the fifth quarterly period.

The economics of the automatic pre-diffusion slice cleaner mentioned in previous quarterlies have been re-evaluated and considered impractical at our present production levels. Consequently, it has been decided to continue with our present manual techniques and await production build-up before purchasing automatic or semi-automatic equipment

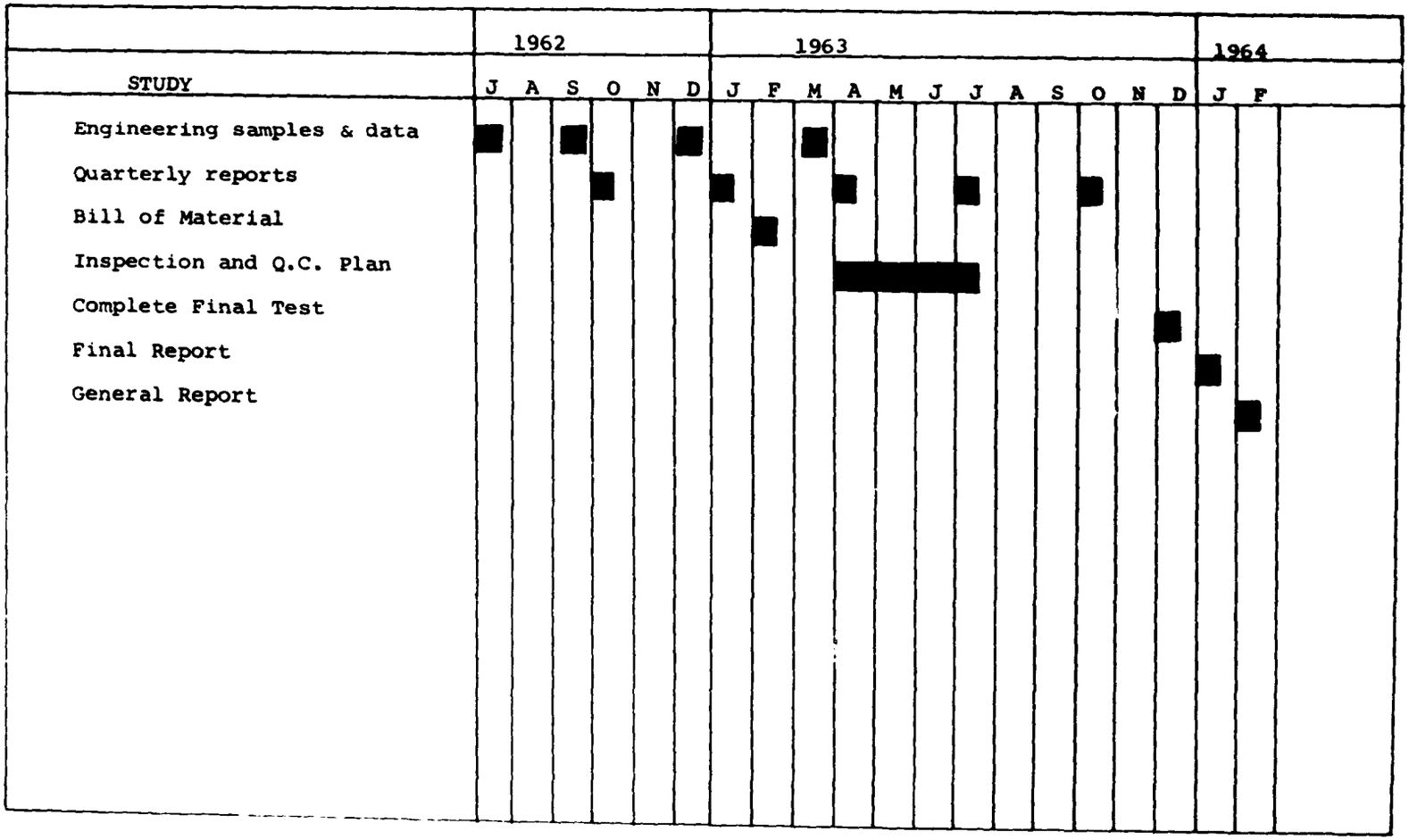
TABLE NO. 1

PROGRAM PLAN

FOR 2N497 SERIES USASSA PROCESS IMPROVEMENT CONTRACT



FOR 2N497 SERIES USASSA PROCESS IMPROVEMENT CONTRACT



1.02 Inert Protective Coatings for Surface Stabilization — Edmond McGhee

The planar phase-in program shown in the third quarterly and on Table 1 was completed on schedule and formal production specifications were released early this quarter. Production devices were placed on environmental and life tests as follows:

TEST #	NO. DEVICES	DESCRIPTION OF TEST	PARAMETERS TO READ
1	67 (TO5)	200°C Storage for 1000 hours.	I_{CES}, BV_{CEO}, I_B
2	57 (TO5)	800 mw Operating at 25°C Ambient for 1000 hours.	I_{CES}, BV_{CEO}, I_B
3	36 (studded)	15 Watt Operating at 100°C Case for 1000 hours.	I_{CES}, I_{EBO}, BV_{CEO}, V_{BE} h_{FE}, V_{CES}
4	37 (TO5)	1 Watt Operating at 25°C Ambient for 1000 hours.	Same as above
5	65 (TO5)	800 mw Operating at 25°C Ambient for 1000 hours.	I_{CES}, I_{EBO}, V_{EBF}, BV_{CEO} h_{FE}, V_{BE}, V_{CES}
6	65 (TO5)	200°C Storage for 1000 hours	(Same as above)
7	193 (TO5)	Mil-S-19500/263 (EL) Environmental Tests	(Same as above)

Tests 3 through 7 are incomplete; however, the incomplete data is quite good, indicating that our process improvement efforts have indeed yeilded a high reliability device. Tests 1 and 2 have been finished with no failures per MIL-S-19500/74A criteria. The test results are shown on Tables 2 and 3. It should be noted that these devices were taken from the first lot of production devices, and some difficulty was being experienced with the purity of the final bake-out atmosphere (see 1.08 below). In spite of this, only 7 of the 124 devices started with $I_{CES} > 2$ nanoamps and only 5 ended the test with $I_{CES} > 2$ nanoamps. Both BV_{CEO} and h_{FE} were stable throughout the test.

This data and the incomplete data from the other tests have been evaluated and the decision has been made to register a new device. The key ratings and guaranteed parameters that will be on the new device data sheet are shown in Table 4. The most significant improvements in ratings and parameters on the new data sheet are: higher dissipation, lower leakages, higher current capabilities and lower saturation properties.

Data are being taken and compiled in order to show typical characteristics on a published data sheet. This sheet should be available next quarter.

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DATA SHEET (16-25)

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TABLE 2

Planar 2N656 Life Test
1000 hr. at 800 mw

	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
UNIT #	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
68	< 1	< 1	1	97	95	94	2.68	2.87	2.88
69	1	1	2	101	101	99	2.94	3.21	3.23
70	< 1	< 1	1	91	89	88	2.63	2.72	2.69
71	1	1	2	99	96	95	2.74	2.85	2.80
72	1	1	2	102	100	98	3.14	3.22	3.17
73	121	710	522	96	93	91	2.36	2.46	2.43
74	1	< 1	1	91	90	89	2.19	2.30	2.27
75	< 1	< 1	1	107	105	103	2.48	2.59	2.53
76	< 1	< 1	2	110	107	105	3.66	3.86	3.80
77	< 1	< 1	1	104	102	101	3.56	3.62	3.60
78	8	< 1	1	92	91	91	3.32	3.53	3.43
79	1	541	639	93	92	90	2.14	2.26	2.20
80	< 1	< 1	2	106	102	101	2.78	2.86	2.80
81	1	1	1	117	114	113	3.52	3.65	3.61
82	1	< 1	1	98	96	94	3.93	4.10	4.05
83	< 1	< 1	2	98	96	95	2.56	2.67	2.62
84	1	1	1	100	97	96	2.86	2.92	2.82
85	< 1	1	2	92	90	89	2.86	2.99	2.95
86	1	< 1	2	102	100	98	2.80	2.90	2.85
87	< 1	< 1	1	114	112	111	2.63	2.73	2.69
88	2	1	1	87	86	85	2.22	2.33	2.30
89	< 1	1	1	96	94	93	2.88	3.08	2.88
90	1	< 1	2	118	113	113	2.92	3.01	2.97
91	1	< 1	2	103	101	99	3.26	3.36	3.31
92	6	< 1	2	93	91	90	3.38	3.50	3.45

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TABLE 2

Planar 2N656 Life Test
1000 hr. at 800 mw

	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
UNIT #	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
93	< 1	< 1	1	88	87	86	2.48	2.58	2.56
94	1	< 1	1	91	88	88	2.73	2.86	2.81
95	1	< 1	2	118	116	115	3.23	3.32	3.29
96	1	185	210	90	89	88	2.70	2.81	2.77
97	1	1	1	94	94	93	3.01	3.34	3.18
98	< 1	< 1	1	98	97	95	3.32	3.44	3.40
99	5	1	1	105	103	102	2.59	2.69	2.61
100	1	< 1	2	108	104	103	2.66	2.79	2.73
101	1	< 1	1	99	96	95	3.40	3.51	3.45
102	< 1	< 1	1	98	95	94	2.71	2.82	2.79
103	< 1	< 1	2	99	98	96	4.01	4.15	4.09
104	2	< 1	2	95	92	91	3.11	3.12	3.01
105	< 1	1	1	99	96	95	3.62	3.74	3.69
106	< 1	< 1	11	99	99	97	3.61	3.81	3.60
107	1	< 1	1	99	99	99	2.63	3.00	3.12
108	1	< 1	1	97	95	94	3.31	3.43	3.38
109	< 1	< 1	1	96	94	93	2.96	3.04	2.98
110	< 1	< 1	2	95	92	91	2.77	2.87	2.83
111	< 1	< 1	1	96	96	94	3.29	3.39	3.28
112	1	< 1	1	90	89	88	2.74	2.87	2.82
113	1	< 1	1	98	95	96	3.20	3.35	3.29
114	< 1	< 1	1	98	96	95	2.84	2.94	2.90
115	< 1	< 1	1	96	94	93	2.42	2.51	2.46
116	1	1	1	98	97	96	4.03	4.55	4.45
117	< 1	< 1	1	93	90	89	2.22	2.30	2.25

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TABLE 2

Planar 2N656 Life Test
1000 hr. at 800 mw

UNIT #	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
118	1	1	2	100	99	98	2.51	2.59	2.83
119	1	< 1	2	97	96	96	3.61	4.13	4.04
120	1	1	1	113	112	110	3.68	4.06	3.95
121	< 1	< 1	2	99	97	95	3.28	3.51	3.45
122	< 1	< 1	1	90	89	87	2.39	2.59	2.56
123	< 1	1	1	98	99	98	2.59	2.83	2.79
124	< 1	< 1	1	107	105	103	3.52	3.78	3.73

DATA SHEET (16-25)

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TABLE 3

Planar 2N656 Life Test
1000 Hr. at 200°C

UNIT #	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
1	< 1	< 1	2	96	94	93	4.00	3.80	3.90
2	36	< 1	2	96	94	92	3.45	3.32	3.30
3	< 1	< 1	2	109	106	105	3.59	3.55	3.47
4	< 1	< 1	2	115	110	108	3.50	3.50	3.31
5	1	< 1	2	102	98	97	2.52	2.51	3.52
6	1	< 1	1	97	94	92	3.58	3.32	3.27
7	1	< 1	2	87	85	84	2.27	2.32	2.38
8	< 1	< 1	2	115	112	111	3.35	3.31	3.30
9	< 1	< 1	1	98	95	93	4.07	4.01	4.01
10	1	< 1	2	94	91	90	3.08	2.81	2.76
11	1	< 1	2	89	86	85	2.46	2.52	2.50
12	1	< 1	2	90	88	87	2.73	2.74	2.74
13	1	< 1	2	94	92	91	2.70	2.73	2.70
14	< 1	< 1	2	98	94	93	4.04	4.01	4.00
15	1	< 1	2	91	89	88	2.86	2.89	2.87
16	< 1	1	2	90	88	87	2.06	2.15	2.10
17	< 1	< 1	2	114	109	108	2.87	2.85	2.83
18	< 1	< 1	2	115	110	111	3.45	3.41	3.41
19	1	1	2	90	88	87	2.70	2.78	2.75
20	< 1	1	1	87	85	84	2.18	2.28	2.26
21	< 1	< 1	1	104	100	100	3.39	3.38	3.37
22	1	< 1	2	90	88	86	2.75	2.77	2.76
23	< 1	1	2	92	89	88	2.96	2.96	2.88
24	30	31	33	90	88	86	2.54	2.56	2.56
25	1	1	2	98	94	93	2.52	2.55	2.54

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DATA SHEET (16-25)

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TABLE 3

Planar 2N656 Life Test
1000 Hr. at 200°C

	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
UNIT #	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
26	< 1	1	2	113	109	108	3.20	3.17	3.15
27	< 1	< 1	2	99	95	95	2.56	2.53	2.54
28	1	< 1	2	89	85	86	2.35	2.38	2.39
29	< 1	1	2	115	110	109	3.43	3.41	3.41
30	1	< 1	2	106	101	99	2.66	2.65	2.59
31	1	< 1	1	115	112	109	2.74	2.74	2.74
32	< 1	< 1	2	98	95	95	2.57	2.58	2.58
33	1	1	2	96	92	92	2.59	2.60	2.60
34	1	< 1	1	98	95	94	4.09	4.09	3.87
35	< 1	< 1	2	118	113	112	3.07	2.97	2.90
36	21	1	2	98	93	93	3.45	3.11	3.03
37	< 1	< 1	2	97	94	94	4.08	4.02	3.95
38	< 1	< 1	11	92	89	88	2.90	2.97	2.89
39	1	< 1	1	97	94	93	3.15	3.19	3.12
40	< 1	1	1	106	102	100	3.30	3.20	3.23
41	1	< 1	1	90	89	88	2.94	2.99	2.97
42	1	< 1	1	98	93	93	3.42	3.13	3.08
43	< 1	< 1	1	117	112	110	3.19	3.19	2.93
44	< 1	< 1	1	89	87	88	2.30	2.37	2.29
45	< 1	1	2	100	96	94	3.58	3.35	3.29
46	1	1	2	99	94	93	3.92	3.68	3.58
47	< 1	< 1	1	98	94	93	3.46	3.23	3.20
48	< 1	< 1	2	103	97	97	3.69	3.42	3.37
49	1	< 1	2	92	90	88	2.87	2.91	2.90
50	1	< 1	2	106	101	101	3.09	3.09	3.02

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TABLE 3

Planar 2N656 Life Test
1000 Hr. at 200°C

UNIT #	I_{CES} at V_{CE} = 60 V			BV_{CEO} at I_C = 30 ma			I_B at V_{CE} = 5 V, I_C = 200 ma		
	0 Hr NA	500 Hr NA	1000 Hr NA	0 Hr VOLTS	500 Hr VOLTS	1000 Hr VOLTS	0 Hr ma	500 Hr ma	1000 Hr ma
51	< 1	1	2	112	108	107	3.31	3.28	3.11
52	2	1	2	97	94	93	2.68	2.72	2.59
53	< 1	< 1	1	100	95	95	3.66	3.39	3.29
54	< 1	1	1	105	101	99	4.40	4.39	4.36
55	1	1	2	103	99	98	3.18	3.20	3.11
56	< 1	< 1	1	109	104	104	2.45	2.47	2.42
57	1	< 1	1	90	87	86	2.48	2.60	2.52
58	1	< 1	2	97	94	93	3.72	3.80	3.63
59	1	1	1	98	94	93	3.35	3.34	3.22
60	< 1	1	1	90	87	86	2.45	2.58	2.51
61	< 1	1	2	104	100	101	2.59	2.63	2.58
62	1	< 1	1	104	100	99	2.85	2.88	2.75
63	1	1	1	93	91	89	3.03	3.11	2.86
64	< 1	1	2	95	93	93	2.59	2.61	2.59
65	< 1	< 1	2	90	86	86	3.23	3.12	3.00
66	< 1	1	2	114	110	109	3.07	3.05	2.99
67	1	< 1	2	94	91	89	2.55	2.60	2.56

TABLE 4

A Summary of the Maximum Ratings and Guaranteed Parameters for the 2N2987 Series

Absolute Max. Ratings at 25° Case Temp.	2N2987 2N2989	2N2988 2N2990
Collector-base Voltage	95 V	155 V
Collector-emitter Voltage	80 V	100 V
Emitter-base Voltage	7 V	7 V
Total Device Dissipation at 25°C Free Air Temp.	1 W	1 W
Total Device Dissipation at 100°C Case Temp.	15 W	15 W
Operating Case Temp. Range	-65 to +200°C	

GUARANTEED PARAMETERS

PARAMETER	CONDITIONS	2N2987	2N2988	2N2989	2N2990	UNITS
BV_{CEO}*	I_C = 30 ma, I_B = 0	80 Min	100 Min	80 Min	100 Min	V
I_{CEO}	V_{CE} = 50 V(2N2887) or (2N2989) 90 V(2N2988), I_B = 0 (2N2990)	0.1 Max	0.1 Max	0.1 Max	0.1 Min	μa
I_{CEX}	V_{CE} = 90 V(2N2987) or (2N2989) 150 V(2N2988), V_{BE} = -1.5 V (2N2990)	0.025 Max	0.025 Max	0.025 Max	0.025 Max	μa
I_{CEX}	Same as above at T_C = 175°C	15 Max	15 Max	15 Max	15 Max	μa
I_{EBO}	V_{EB} = 7 V, I_C = 0	0.025 Max	0.025 Max	0.025 Max	0.025 Max	μa
h_{FE}*	V_{CE} = 5 V, I_C = 200 ma	25 to 75	25 to 75	60 to 120	60 to 120	—
h_{FE}*	V_{CE} = 5 V, I_C = 500 ma	20 Min	20 Min	40 Min	40 Min	—
V_{BE}*	V_{CE} = 5 V, I_C = 200 ma	0.9 Max	0.9 Max	0.9 Max	0.9 Max	V
V_{BE}*	I_B = 50 ma, I_C = 500 ma	1.4 Max	1.4 Max	1.4 Max	1.4 Max	V

TABLE 4 (Continued)

PARAMETER	CONDITIONS	2N2987	2N2988	2N2989	2N2990	UNITS
$V_{CE(SAT)}$*	I_B = 20 ma, I_C = 200 ma	0.8 Max	0.8 Max	0.8 Max	0.8 Max	V
$V_{CE(SAT)}$*	I_B = 50 ma, I_C = 500 ma	3.0 Max	3.0 Max	3.0 Max	3.0 Max	V
h_{fe}	V_{CE} = 10 V, I_C = 100 ma, f = 1 kc	25 to 85	25 to 85	50 to 170	50 to 170	—
$\|h_{fe}\|$	V_{CE} = 10 V, I_C = 100 ma, f = 30 mc	1	1	1	1	—

* Pulse Test

Some difficulty has been experienced with the scribing and breaking of the planar device, but it was traced to the optical system of the scriber and corrected. The system has been adequate for our mesa devices for there is adequate natural contrast between the mesa and the bottom of the "moat" where the scribing must be done. However, natural contrast is almost completely absent on the planar device; therefore, an improved lighting and optical system was essential before the operator was able to efficiently and accurately align the slices for scribing.

1.03 Higher Temperature Alloys — Edmond McGhee

The "hard" gold eutectic alloy that was adopted for the planar device early in the process improvement program continues to give good results. (The "soft" solder used on the mesa device melts at 315°C and the "hard" gold eutectic melts at 356°C.)

1.04 Collector Attachment — Edmond McGhee, Herbert D. Locke

The .010" thick molybdenum collector mounting substrate and the silver-copper eutectic braze continue to give excellent results. A specification was adopted which prohibits braze from creeping across the top of the "moly" any further than .010 in from the edge. This assures a uniform mounting surface for the collector side of the wafer.

The improved processes for preparing the collector side of the wafer are still yielding good results. Rigid control of the collector surface prior to and during the collector plating processes, and lot acceptance tests on the finished wafers are maintaining a high quality collector bond. The higher cost of the 200 microinch gold plate on the slugs, along with a slight problem with peripheral voids in the wafer mounting alloy, indicated a need to evaluate thinner gold plates. An evaluation determined that 50 microinch of gold yielded better peripherial void situation as well as lower costs.

1.05 Thermal Dissipation of Package — John Kauffman

The improved dual tab package and the improvements in collector mounting, package staking, and crimping process have permitted us to increase the dissipation rating of the planar device. The device dissipation rating is now one (1) watt in 25°C ambient atmosphere and 15 watts with the case held at 100°C.

1.06 Elimination of Need for Thermal Compression Bonding — Edmond McGhee, Dale Bennett

Ultrasonic cold bonding and the improved high capacity processes for making the evaporated contacts continue to give good results. No difficulty has been experienced with opens or shorts in environmental tests to date. Complete data will be available next quarter.

1.07 Lead Attachments — Edmond McGhee

The aluminum wafer lead welded to the gold plated Kovar header lead performs satisfac-

torily. The "fixed head" welder and microscope have virtually eliminated the "poor weld" problem that existed when hand held "tweezer" welders were used.

1.08 Surface Passivation — Herbert Locke, Edmond McGhee

Initial experience with the planar processes indicated that the oxide must be extremely dry to be truly passive. Improved processes that were developed in our Semiconductor Research & Development Laboratories were evaluated and it was found that a 48-hour, high temperature, pre-can bake in a rapidly circulating, dry, inert atmosphere was adequate to achieve this passivation. The devices are then handled and canned in an inert atmosphere of no greater than 10 ppm moisture in order to maintain this passivation.

The importance of the purity in bakeout atmosphere was emphasized when a minute leak developed in an oven sufficient to slightly tarnish the parts in process. The tarnished devices were found to contain an appreciable quantity of electrically leaky devices. The oven leak was repaired and specifications were changed to prevent the recurrence of the situation.

1.09 Protective Coating Techniques for Surface Passivation — Herbert Locke, Edmond McGhee

A test was conducted to determine the effect of the best available silicone surface coating on the leakage level and/or stability of the planar device. Fifty-five (55) devices were surface treated and placed on 200°C storage and sixteen (16) devices on 800 mw operating test. Data are shown in Table 5. The test indicated excellent leakage stability at 200°C storage for the six weeks of the tests. However, the devices on 800 mw operating deteriorated rapidly with leakage of approximately half the devices increasing over four orders of magnitude in one week. The results of this test led us to conclude that the optimum protective coating for high reliability devices is clean, dry, silicon (planar) oxide.

1.10 Welding, Leak Determination — James Overman

The quality of our final seal weld has improved significantly since the start of the contract. This has been a result of the excellent care and maintenance the welders receive from trained set-up men and the routine changeout and maintenance of the welder electrodes. The electrodes are changed after every 3000 welds and are dressed on an automatic refacing machine specifically designed to maintain the tight tolerances required for quality welds.

Attempts to determine the advisability of performing the helium leak test at a different point in the process were discontinued because of the availability of a radioactive tracer gas leak detecting process. The radioactive process is a standard leak test that costs more to perform than the helium leak test, but is considered by many to be more sensitive. Because of the cost, this test will not be adopted as the standard leak detection process for the production device. However, it will be available for those customers who request it and it will be used to check the devices that are going on test to confirm the degree of reliability improvement.

1.11 Final Preparation Prior to Sealing — Edmond McGhee

Improved processes in this area continue to give good results. All parts are rigorously cleaned, and hydrogen fired and sealed in dust-free plastic bags. The devices are removed from the bags in the dry box and are baked out in an inert atmosphere immediately prior to canning and are maintained in an inert atmosphere of < 10 ppm moisture until after canning.

1.12 Post Weld Conditioning — Edmond McGhee

Processes developed by our Semiconductor Research and Development Laboratory personnel have indicated that no heat aging or burn-in of the planar devices is required. However, it was decided to use a 48-hour, 200°C heat-age as a precautionary measure.

1.13 Inspection Techniques — Herbert Locke

The process improvement whereby 100% of the wafers are electrically probed while still in slice form is giving excellent results. This technique permits us to salvage some of the increased planar material costs by reducing assembly and final test costs. These cost reductions are possible because the major portion of the defective wafers are now taken out prior to assembling — not at final test, after a slug, header, can and considerable labor have been expended.

It was determined that some of the good wafers were being damaged by the marker attachment to the probe. (The marker is used to identify defective wafers for post scribe and break culling.) The operator was having difficulty applying the correct amount of pressure to leave a visible mark without fracturing the slice. The problem was solved by designing a light, spring-loaded probe which would always apply the same pressure to the wafer during the defective wafer marking operation.

1.14 Process Control Improvement

Daily random samples are being pulled from the production line. Once each week the accumulated devices are run through a TACT (Transistor and Component Tester) machine and data are taken on the fifteen (15) different parameters and conditions shown in Table 6. This information is compiled and shown as distributions by our IBM 7074 computer. A weekly time plot of these parameter trends is maintained, showing the tenth, fiftieth and ninetieth percentile level for each parameter. This is an invaluable aid to the product engineer for detecting and correcting undesirable trends in the device.

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DATA SHEET (16-25)

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TABLE 5

Life Test on Planar 2N656 Devices with High Purity Silicone Varnish Applied over Wafer.
Devices 9 thru 17 on 200°C Storage, Devices 65 thru 80 on 800 mw Operation

	DEVICE #	I_{CES} at V_{CE} = 90 V INITIAL	1 Wk.	3 Wk.	6 Wk.	h_{FE} at V_{CE} = 5 V, I_C = 200 ma INITIAL	1 Wk.	3 Wk.	6 Wk.
200°C Storage	9	.16 na	.16 na	.12 na	.14 na	31.2	26.4	22.7	22.7
	10	.12	.12	.11	.13	32.3	27.8	22.7	22.2
	11	.11	.11	.11	.12	26.3	25.0	21.3	20.8
	12	.16	.16	.14	.16	27.0	25.0	20.0	20.0
	13	.21	.21	.16	.19	23.2	23.2	19.6	19.6
	14	.22	.22	.19	.21	33.3	31.3	24.4	23.8
	15	.13	.13	.13	.13	25.	22.2	19.2	19.0
	16	.19	.21	.18	.18	24.4	20.8	17.9	17.5
	17	.16	.16	.15	.16	25.0	23.8	20.0	20.0
800 MW Operating	65	.14	.56 na	1.4 na	97 na	23.6	20.8	22.1	25.3
	66	.17	36 µa	59 µa	15.3 na	23.8	Too Leaky	Too Leaky	22.2
	67	.24	5.2 µa	39 µa	71 µa	28.6	52.6	Too Leaky	Too Leaky
	68	.14	11 µa	23 µa	54 µa	32.3	45.5	58.9	32.8
	69	.17	1.5 na	52 µa	3.9 µa	27.0	32.2	Too Leaky	Too Leaky
	70	.56	.35 na	16 µa	41 µa	25.6	25.4	Too Leaky	Too Leaky
	71	.68	1.1 na	28 µa	220 µa	27.0	26.3	Too Leaky	Too Leaky
	72	.12	.41 na	24 µa	26 µa	41.6	45.5	Too Leaky	Too Leaky
	73	.19	750 µa	68 µa	.48 µa	38.5	Too Leaky	Too Leaky	Too Leaky
	74	.16	450 µa	295 µa	.33 na	27.8	Too Leaky	Too Leaky	Too Leaky
	75	.17	860 na	14 µa	26 µa	24.4	32.2	43.5	Too Leaky
	76	.21	.62 na	78 na	.34 µa	25.6	27.0	37.0	Too Leaky
	77	.16	.8 na	.39 na	40 na	30.3	26.2	14.9	16.4
	78	.14	.45 na	.42 na	.54 na	25.6	25.0	13.0	16.7
	79	.14	21 µa	17 µa	66 µa	25.0	Too Leaky	Too Leaky	Too Leaky
	80	.12	.27 na	3.6 na	12 µa	25.0	23.8	12.8	22.2

TABLE 6

Test 2N2987 (Raw) Daily Production Samples on the TACT Machine for the Following Parameters, Conditions and Limits.

PARAMETER	CONDITIONS	FULL SCALE READING	MIN READING	CELL
I_{EBO}	V_{EB} = 7 V	Automatic Range	0	.001
I_{CEO}	V_{CE} = 50 V	Automatic Range	0	.001
I_{CEO}	V_{CE} = 90 V	Automatic Range	0	.002
I_{CEX}	V_{CE} = 90 V, V_{CE} = -1.5	Automatic Range	0	.002
I_{CEX}	V_{CE} = 150 V, V_{BE} = -1.5	Automatic Range	0.0	.001
BV_{EBO}	I_E = 10 microamp	100 V	6	.25
h_{FE}	I_C = 1 ma, V_{CE} = 5 V	1 ma	0	2.5
h_{FE}*	I_C = 200 ma, V_{CE} = 5 V	100 ma	0	5
h_{FE}*	I_C = 500 ma, V_{CE} = 5 V	100 ma	20	1.5
V_{BE}*	I_C = 200 ma, V_{CE} = 5 V	10 V	0.5	.01
$V_{CE(SAT)}$*	I_C = 200 ma, I_B = 20 ma	10 V	0	.01
$V_{BE(SAT)}$*	I_C = 200 ma, I_B = 20 ma	10 V	0.6	.01
$V_{CE(SAT)}$*	I_C = 500 ma, I_B = 50 ma	10 V	0.4	.03
$V_{BE(SAT)}$*	I_C = 500 ma, I_B = 50 ma	10 V	0.7	.01
BV_{CEO}*	I_C = 30 ma	1000 V	50	2.5

* Pulse Test

SECTION IV

CONCLUSIONS

The process improvement work on the 2N656 device has been completed. Significant process improvements and production capabilities have dictated registration of a separate device series with the EIA. During this report period, request for EIA reservation was made and temporary EIA numbers were received.

The following process changes have contributed most to the improvement of the device.

OLD PROCESS	NEW PROCESS
Mesa Wafer	Planar Wafer
Single .017 Dia. Slug Support	Double .012 x .075 Slug Support
Soft Solder	Hard Gold Alloy
Au to Al Thermocompression Bond	Al to Al Ultrasonic Bond
Inline (Post Mount) Etch	No Etchants Used in Assembly
Silicone Wafer Varnish	All Wafer Coating Eliminated

The Planar (2N2987 series) device is unilaterally interchangeable with the Mesa (2N656) device. Planar process improvements described in this report have been adopted as the standard parent production process from which both the 2N2987 series and the 2N656 can be supplied. To insure optimum utilization of the advantages gained through these process improvements, serious consideration should be given to specifying the planar process.

SECTION V

PROGRAM FOR NEXT INTERVAL

All preliminary environmental and life tests started on early production devices will be completed and analyzed. Planar 2N656 production devices will be screened from the 2N2987 series parent material and placed on test to confirm the degree of reliability improvement.

SECTION VI

IDENTIFICATION OF PERSONNEL

HERBERT D. LOCKE

1961 - Present	Device Engineer, Silicon Power Transistors, TI
1959 - 1961	Engineering Technician, Silicon Power Transistors, TI
1958 - 1959	Assistant Supervisor, Silicon Power Transistors, TI

MILTON K. MACK

1956 - Present	Cost Center Supervisor, Silicon Power Transistor, TI
1949 - 1956	Manager, Compounding Laboratory, Dr. Pepper Company
1945 - 1949	Analytical Chemist, National Aniline Company

Author of "Polarographic Water Analysis" Control Engineering, October 1954

Holder of Patents No. 2,956,913 - Transistor and Method of Making Same
No. 2,970,896 - Method for Making Semiconductor Devices

EDMOND W. MC GHEE

B.S. in Physics, Baylor University, 1959
B.Mus. in Theory and Composition, Baylor University, 1949
M.Mus. in Music Literature, Baylor University, 1951

1959 - Present	Product Engineer, Silicon Power Transistor, TI

CLARENCE H. MUNCIE

B.S. in Electrical Engineering, Southern Methodist University, 1962

1962 - Present	Product Engineer, Silicon Power Transistors, TI
1959 - 1962	Co-Op Engineer, TI
1958 - 1959	Co-Op Engineer, GE

B. DEAN SCALLORN

B.S. in Chemical Engineering, University of Texas, 1956

1959 - Present	Quality and Reliability Assurance Engineer, Semiconductor Division, TI
1958 - 1959	Development Engineer of Vinyl Plastisols, The Barrier Corporation
1956 - 1958	Process Engineer on Manufacturing of Sulphuric Acid, Stauffer Chemical Company

JOHN E. KAUFFMAN

1963 - Present	Product (Mechanical Design) Engineer, Silicon Power Transistors, TI
1960 - 1963	Engineering Technician, Silicon Power Transistors, TI
1959 - 1960	Engineering Technician, Silicon Material Manufacturing, TI

SECTION VII

IDENTIFICATION OF TECHNICIANS AND MANHOURS WORKED

POWER DEPARTMENT PERSONNEL	HOURS WORKED
Salaried	
Edward McGhee	406
Richard Stead	277.5
James Overman	296
Dale Bennet	246
Dean Scallorn	144
Hourly	
Harold Duncan	500
Dalma McBride	50 est.
John Kauffman	100 est.
Charles Ansley	50 est.
Quality Assurance Personnel	50 est.