TR-1198

TRANSISTOR FLIP-FLOP AND RING COUNTER WITH NONVOLATILE MEMORY

Ira R. Marcus

5 February 1964

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Ira R. Marcus

FOR THE COMMANDER:
Approved by

R. S. Hoff
Chief, Laboratory 400

CONTENTS

ABSTRACT

A modification of the standard transistor flip-flop and ring counter circuits was made that allows setting information to be inserted by an electrical pulse. The supply voltage is not applied to the stages during the insertion of the setting information. When the supply voltage is applied, the flip-flop and ring counter stages assume the desired state. In addition, if during normal operation the supply voltage is interrupted and reapplied, the stages will return to the state they were in before the interruption. These features are incorporated into the flip-flop and ring counter circuits with the addition of one square-loop magnetic core per stage.

1. INTRODUCTION

The transistor flip-flop and ring counter are the basic circuits used in many computers, programmers, and timers. In some applications it is desired to put the stages of these circuits into particular states before the device containing them is called upon to operate. To do this, the supply voltage must be applied to these circuits during the initial setting period. They will retain this initial setting, until they are called upon to operate, as long as the supply voltage is maintained. If power is removed and reapplied, the stages may assume different states. The device must thus be powered during setting and continued to be powered until the device has accomplished its function.

This report describes a modification of these standard circuits that enables setting information to be inserted without the supply voltage being applied. Once the setting information is inserted, it will be retained indefinitely without power. Upon application of the supply voltage, the circuits will assume the desired state. If the supply voltage is subsequently interrupted, the same circuit modification allows them to return to the state they were in before the interruption.

2. FLIP-FLOP

2.1 Circuit Description

Figure 1 shows a standard transistor flip-flop circuit. Figure 2 shows a standard flip-flop circuit modified to have memory without the supply voltage applied to it. Tl is a square-loop magnetic core. Rc, Cc, Rcc, and Dc form a clamping circuit. Ri, Ci and Ric form an interrogating circuit for Tl. Sl and S2 are the terminals of the set winding for Tl and, as will be shown, for the flip-flop. We will now "set the flip-flop" to the "zero" state without the supply voltage on the flip-flop. (When Q2 conducts, the flip-flop is defined to be in the zero state.) A positive current pulse enters the set

winding at S1. This puts T1 into the zero state. If the supply voltage is now applied to the flip-flop, it will go into the zero state. Upon application of the supply voltage, T1 is pulsed toward the zero state by the interrogation circuit. Since T1 is in the zero state, due to its initial setting, no voltage other than a zero noise pulse is induced in windings XZ and WY. The clamping circuit causes the collector of Q2 to momentarily go to ground. This is enough to allow Q2 to latch-on and the flip-flop assumes the zero state. The collector current of Q2 flows through winding XZ driving T1 to the zero state. If the supply voltage is subsequently interrupted and reapplied, the interrogation and clamping circuits operate as before.

We now want to set the flip-flop to the "one" state without the supply voltage on the flip-flop. A positive current set pulse enters the S2 terminal of the set winding. T1 goes into the one state. Supply voltage is now applied to the flip-flop. The clamping circuit again tends to cause Q2 to conduct. However, the interrogation circuit causes T1 to switch toward the zero state from the one state. This causes voltages to be induced on all the core windings. X goes positive with respect to Z, and W goes negative with respect to Y. This tends to turn Q1 on and Q2 off. The switching time of T1 is designed to be longer than the time constant of the clamping circuit. The flip-flop is now in the one state. The collector current flowing through Q1 flows through the WY winding and returns T1 to the one state. If the supply voltage is now interrupted and reapplied, the clamping circuit and the interrogation circuit operate as before and the flip-flop assumes the one state. The cycle may be repeated indefinitely.

2.2 Design Considerations

2.2.1 Clamping Circuit

Figure 2 shows one type of clamping circuit--a simple RC circuit. The RC time of RcCc should be greater than the longest zero noise pulse and shorter than the one pulse from the core T1 when the core is driven by the interrogation circuit. Another type of clamping circuit is shown in figure 3. This is a better clamping circuit than the simple RC since the potential at point C is clamped to ground for a finite time and then rises exponentially. With the RC clamp it rises exponentially from ground. Rcc is a leakage resistor and removes the charge from Cc if the power supply voltage is interrupted and then reapplied within a short time.

One clamping circuit may be used for many flip-flops. Figure 4 shows a typical arrangement. When a single clamping circuit is used for many flip-flops, care must be taken in the design so that the clamping time is not affected by how many ones are in the system.

2.2.2 Interrogation Circuit

The RC time constant of RiCi should be longer than the time interval during which the clamping circuit is effective. It must also be longer than the switching time of the core. The maximum interrogation current is determined by the pulse current capacity of the power supply. The number of turns on the interrogation winding is determined by the interrogation current and the switching properties of the core. The ampere-turn drive of the interrogation winding should switch the core in the required time. The leakage resistance Ric is used to discharge Ci so that the interrogation circuit will be ready to interrogate if the supply voltage is interrupted and reapplied within a short period of time. Ric should be at least ten times greater than Ri. Ric+Ri draws power continuously and the combined resistance must be high enough so as not to draw excessive current from the power supply. The time constant RicCi should be as small as possible and consistent with the previous constraints. Figure 5 shows how a single interrogation circuit can be used for many flip-flops.

When an interrogation circuit is used with many flip-flops, the system must be designed so that (a) the core switching time is longer than the clamping time when only one core is being switched from the one to the zero state and (b) the switching voltage induced in the WY, XZ windings is high enough to put the flip-flop into the one state when all the stages are being set into the one state, that is, when the maximum number of cores are being switched. If a large number of stages are being interrogated by one circuit, then it may be advisable to interrogate by a constant current pulse.

2.2.3 Square-Loop Memory Core

The choice of the magnetic core must satisfy a number of conditions. It must be large enough so that the windings XZ, WY, and the interrogation winding can be wound on the core. Winding XZ can have the same number of turns as winding WY. The number of turns of these windings must be great enough so that their ampere-turn drive switches the core. The current is fixed by the flip-flop. In addition, the number of turns must be great enough so that when the core switches during interrogation, sufficient voltage is induced to cause Q1 to conduct. The voltage induced in XZ and WY should be about equal to the supply voltage. The flux capacity of the core is determined by the desired switching time and the interrogation drive. The exact values for the core and its windings can be computed best after determining the requirements dictated by the application. The above listed constraints can then be applied. The addition of the square-loop magnetic core does not greatly affect the maximum operating frequency of the flip-flop.

3. RING COUNTER

3.1 Circuit Description

Figure 6 shows a single stage of a transistor ring counter. This circuit is described in detail in HDL TR-1154.* When the stage is in the zero state, neither the PNP nor the NPN transistor conducts. When the stage is in the one state, both the PNP and NPN transistors are conducting. Figure 7 shows the basic stage modified to have memory. Core T1 is a square-loop magnetic core. Ri, Ci, and Ric form the interrogating circuit which functions about as the interrogating circuit in the memory modified flip-flop. If the supply voltage is on and the stage M is in the one state, core T1 is driven toward the one state by winding YZ. If stage M+1 is in the one state, then stage M is in the zero state and core T1 is driven toward the zero state by the current in winding AB. The core in stage M+1 will be in the one state. Thus the state of the core is determined by the state of the stage. Figure 8 is a block diagram of a multistage counter with memory. Figure 9 is a detailed schematic of a ring counter with memory. In figure 9, resistors P and R allow only one stage to be on, in the one state, at any one time. Assume the core in stage 1 is set to the one state by the set winding DE, and all the other cores in the remaining stages are set to the zero state. If B+ is now applied to the circuit, all the cores are driven toward the zero state by the interrogation circuit GFH. The core in the first stage switches, inducing voltages in windings ZY and AB so that the first stage is turned on while the second stage is turned off, because the base-to-emitter junction of Q2 in stage 1 is forward biased while the base-to-emitter junction of Q2 in stage 2 is not forward biased. Since all the other cores are in the zero state, only noise or zero voltages are induced in their windings. The first stage turns on and returns the one back into its core. When the first state turns on, it prevents all the other stages from turning on from noise pulses. An explanation of why only one stage can be on at any one time is given in detail in TR-1154. When the one is shifted to stage 2, stage 2 switches the core in stage 1 back to the zero state through the AB winding.

Thus the transistor ring counter can store setting information without the supply voltage on, and will assume the set state when the supply voltage is applied. In addition, if the supply voltage is interrupted and then reapplied, the ring counter will assume the state it was in before the interruption.

3.2 Interrogation Circuit

The requirements for the interrogation circuit used with the ring counter are simpler than those for the flip-flops, because the

*Ira R. Marcus, "Design Procedure for a Transistor Ring Counter, 15 October 1963.

ring counter has only one stage on at any one time, and thus only one core has to be switched by the interrogation circuit. The general comments on the interrogation section circuit in the flip-flop section are applicable to the ring counter. As with the flip-flop, the RC time must be long enough to switch the core. In figure 9, diode G is added. This prevents H from discharging back through the cores when the supply voltage is interrupted.

3.3 Square-Loop Memory Core

The characteristics of the memory core required for the ring counter are few. When the core is switched from the one to the zero state, winding ZY (fig. 7) must have a voltage induced in it equal to, or greater than, V_{be} of the PNP transistor, so that the stage will turn on. The ampere-turns of windings YZ and AB must be able to switch the core.

4. BREADBOARD MODELS

4.1 Flip-Flop

Figure 10 is a schematic of the breadboard circuit used to demonstrate the principles discussed in the previous paragraphs. Four series flip-flops share a common interrogation and clamping circuit. The lamps in the collector loads are used as indicators. The states of the four binaries are changed by putting pulses into the first flip-flop. For simplicity, the input pulse circuitry is not shown. Although the four binaries are in series, it is easily seen that they could be interconnected to form a binary decade and still retain the memory features. The clamping time is 6 μsec when there is one "one" in the system and 4 μsec when there are four "ones" in the system. The difference in clamping time is explained as follows.

When there is one "one" in the system, three of the flip-flops go into the zero state and the transistor in the flip-flop nearest the clamping diode immediately conducts, due to the action of the clamping circuit. When these three transistors conduct, the current through their loads goes through these transistors rather than the transistor in the clamping circuit. Thus the clamping circuit transistor has a light load. However, if there are four "ones" in the system, all four of the transistors in the flip-flop nearest the clamping diode do not conduct, and the transistor in the clamping circuit is loaded by four flip-flop collector loads. This brings the clamping circuit transistor out of saturation sooner. When there is one "one" in the system, the switching time of the core is 7 μsec; and when there are four "ones" in the system, the switching time of the four cores is 19 μsec. The zero noise pulses are less than 1 μsec wide. Performance is very reliable. However, the switching time of the core and the clamping time of the clamping circuit are too close when there is one "one" in the system. If the memory circuit is

to be used over any appreciable temperature range, the ratio of the single core switching time to the clamping time should be two or greater.

Figure 11 is a photograph of the breadboard of the four flip-flops with memory cores.

4.2 Ring Counter

Figure 9 is a schematic of the breadboard used to demonstrate the modified ring counter. Four stages were used. A lamp, placed in series with the X resistor in each stage, served as an indicator. The components had the following values:

Lamp	= 0.01 amp at 1.3 v	C	= 0.01 μf
X	= 270 ohms	NPN	= 2N2221
P=R	= 180 ohms	PNP	= 2N863
Core	= 0745134C2 (Dynacor)	H	= 1 μf
AB	= 10 turns	K	= 15 kohms
DE	= 10 turns	G	= 1N792
YZ	= 10 turns	S	= 430 ohms
B+	= 5.4 v	Y	= 1500 ohms

This circuit was extremely reliable. One pulses across winding AB were 3.5 v and 5 μsec wide. Zero pulses were 1.0 v and 1 μsec wide.

Figure 12 is a photograph of the breadboard of the ring counter with memory.

5. CONCLUSIONS AND RECOMMENDATIONS

A simple modification of standard transistor flip-flop and ring counter circuits allows setting information to be inserted by an electrical pulse. The supply voltage need not be applied during the insertion of the setting information. When the supply voltage is applied, the flip-flop and ring counter stages assume the desired state. In addition, if during normal operation the supply voltage is interrupted and reapplied, the stages will return to the state they were in before the interruption.

It is recommended that consideration be given to incorporating these memory circuits into transistor timing systems containing flip-flops and ring counters. This will allow remote setting at any time before the system is used with no power on the system until it is required to operate.

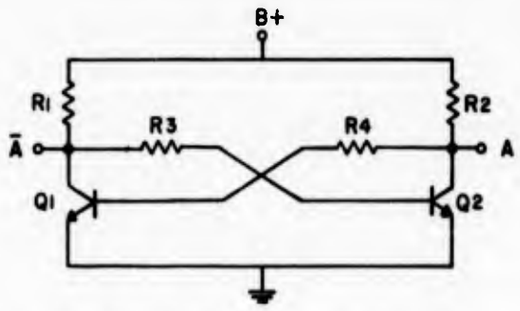

Figure 1. Standard flip-flop circuit.

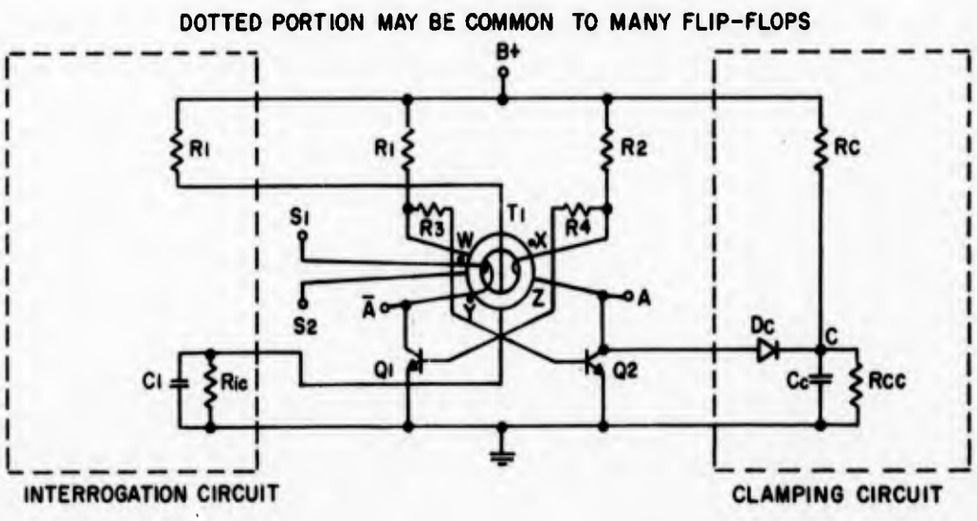

Figure 2. Standard flip-flop modified to have memory without power.

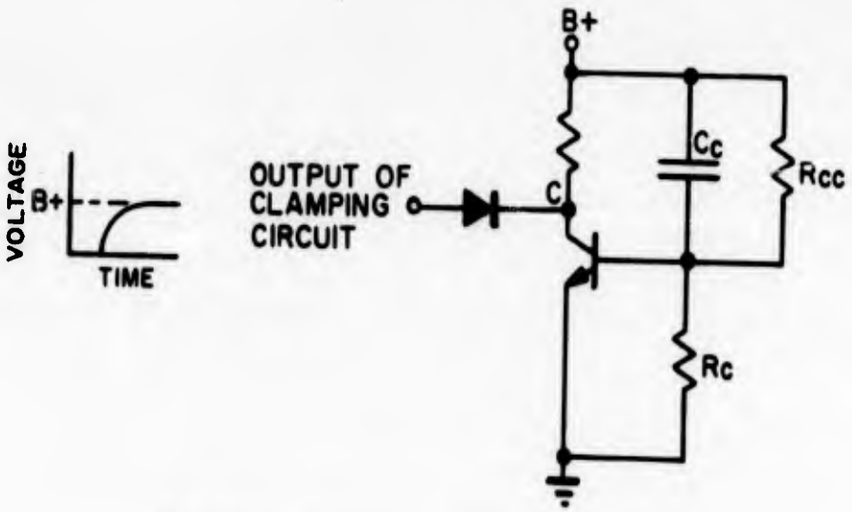

Figure 3. Transistor clamping circuit.

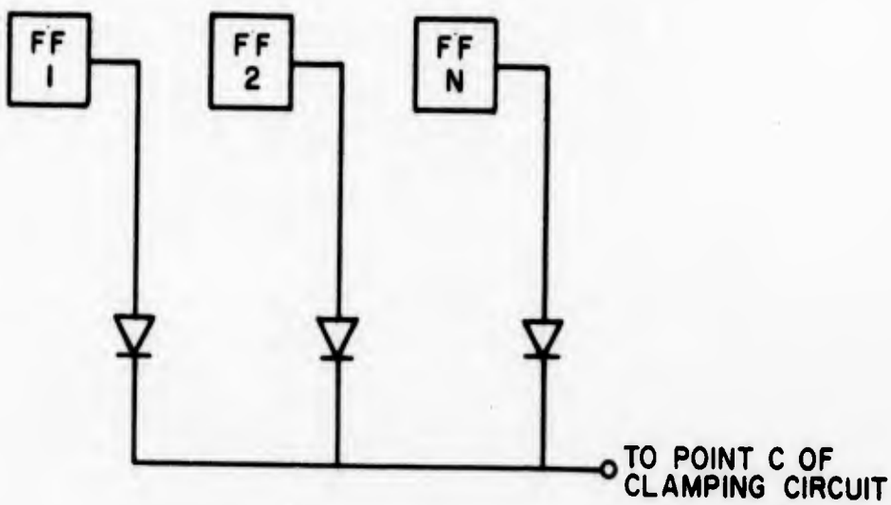

Figure 4. Multiple flip-flops clamped by one clamping circuit.

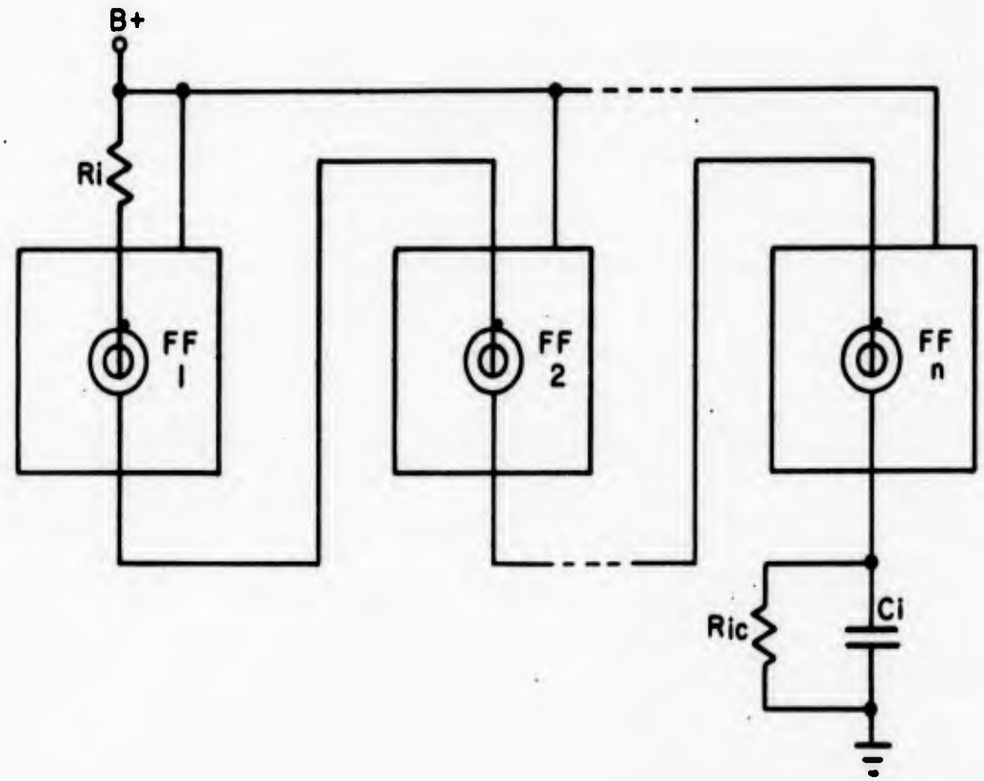

Figure 5. Multiple flip-flops interrogated by a single interrogation circuit.

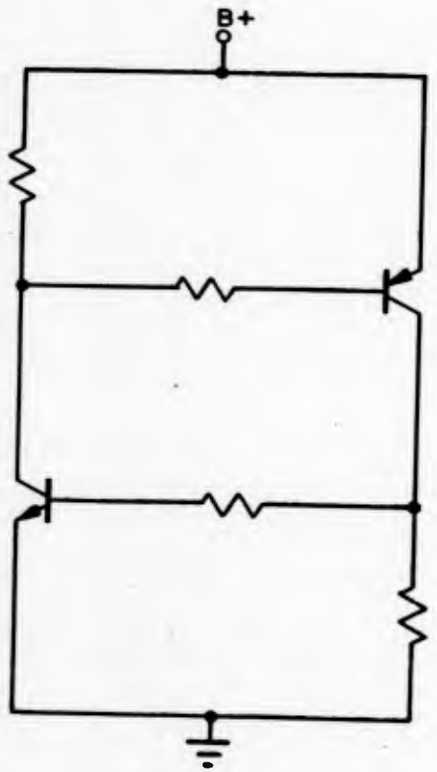

Figure 6. Standard ring counter stage.

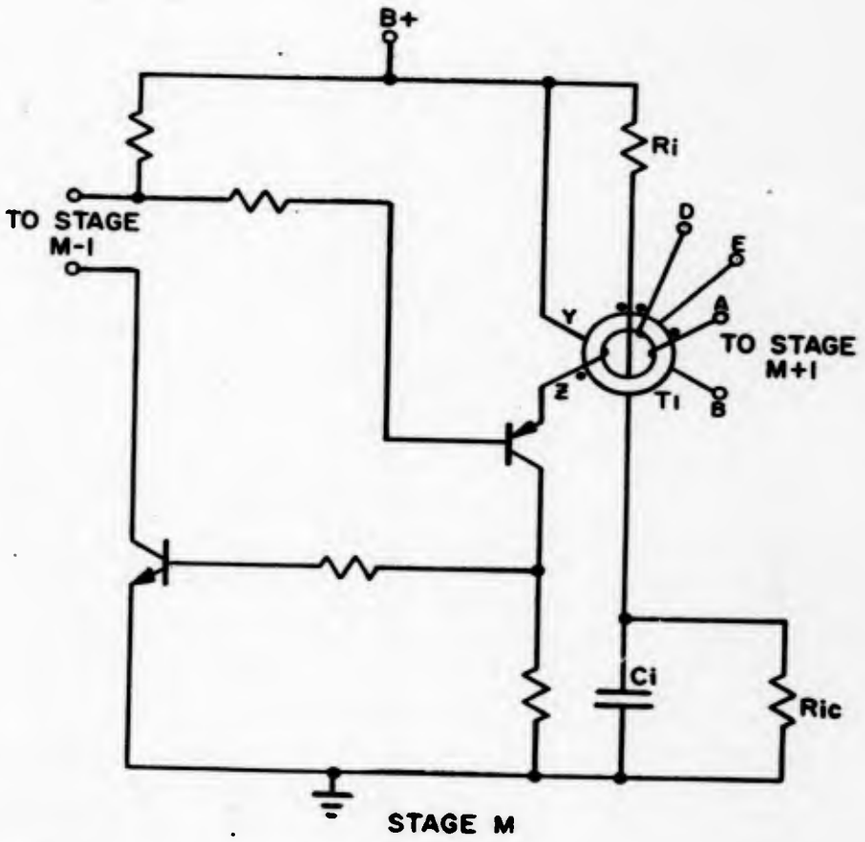

Figure 7. Ring counter stage with memory.

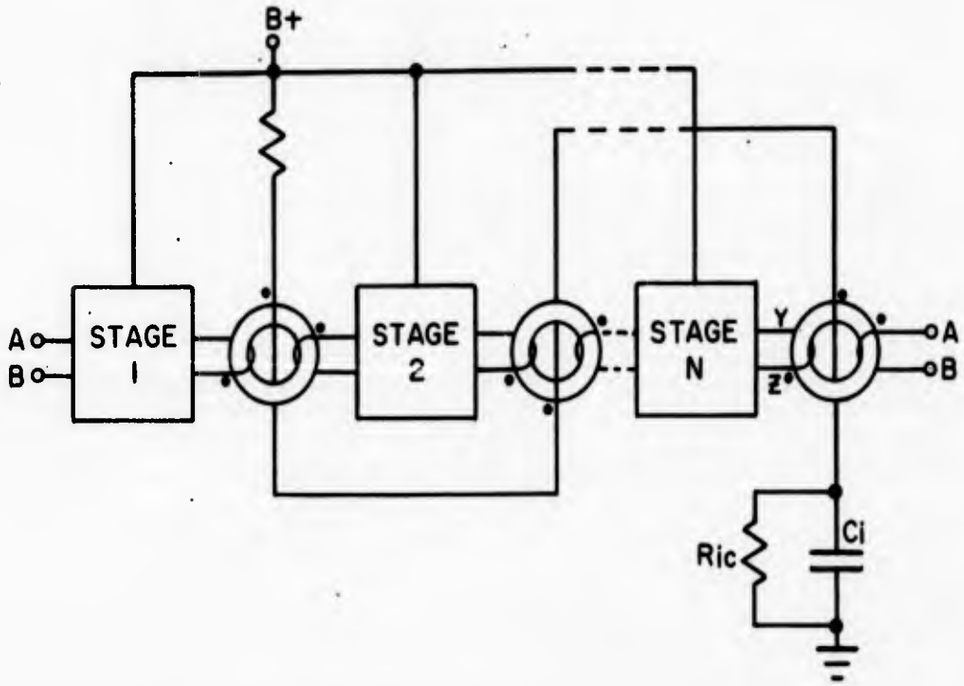

Figure 8. Block diagram of ring counter with memory and with a common interrogation circuit.

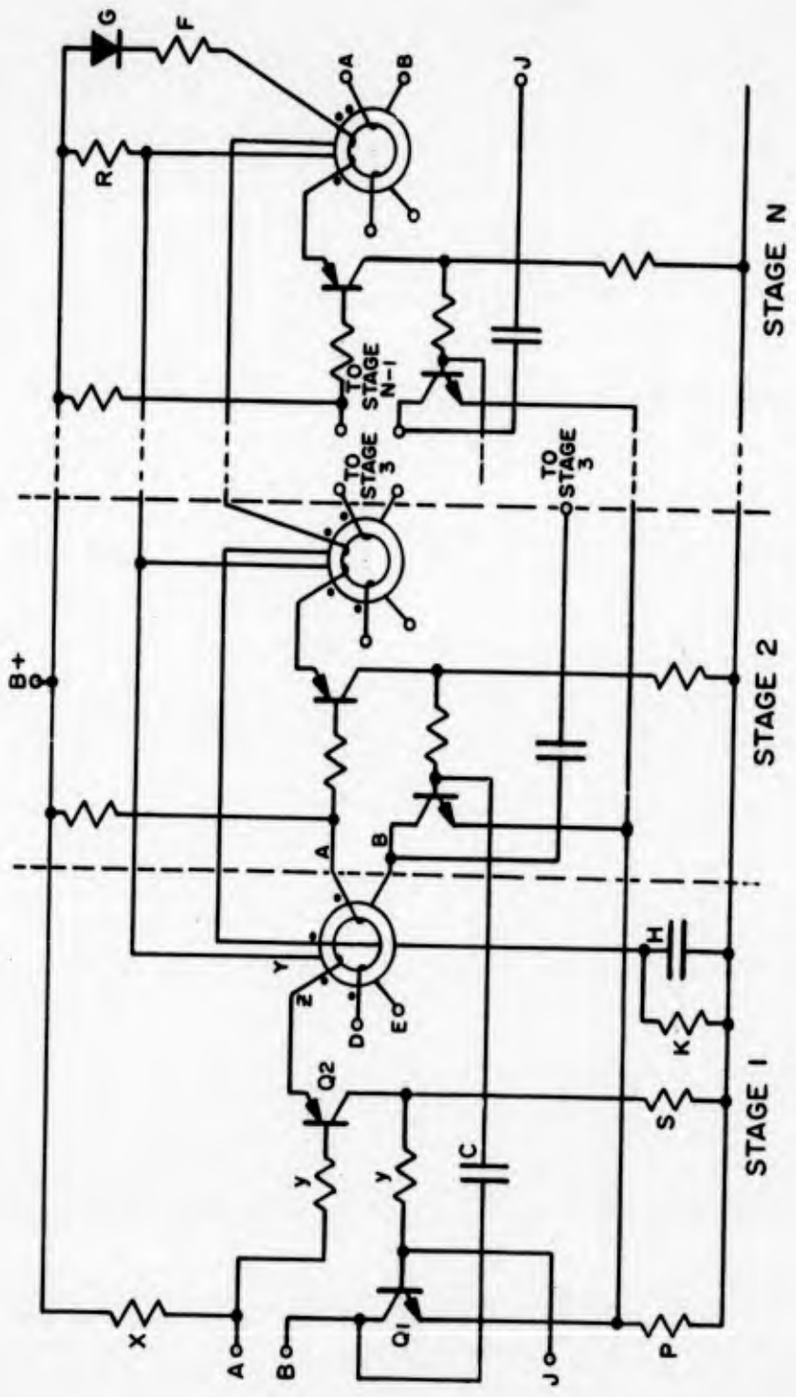

Figure 9. Transistor ring counter with memory.

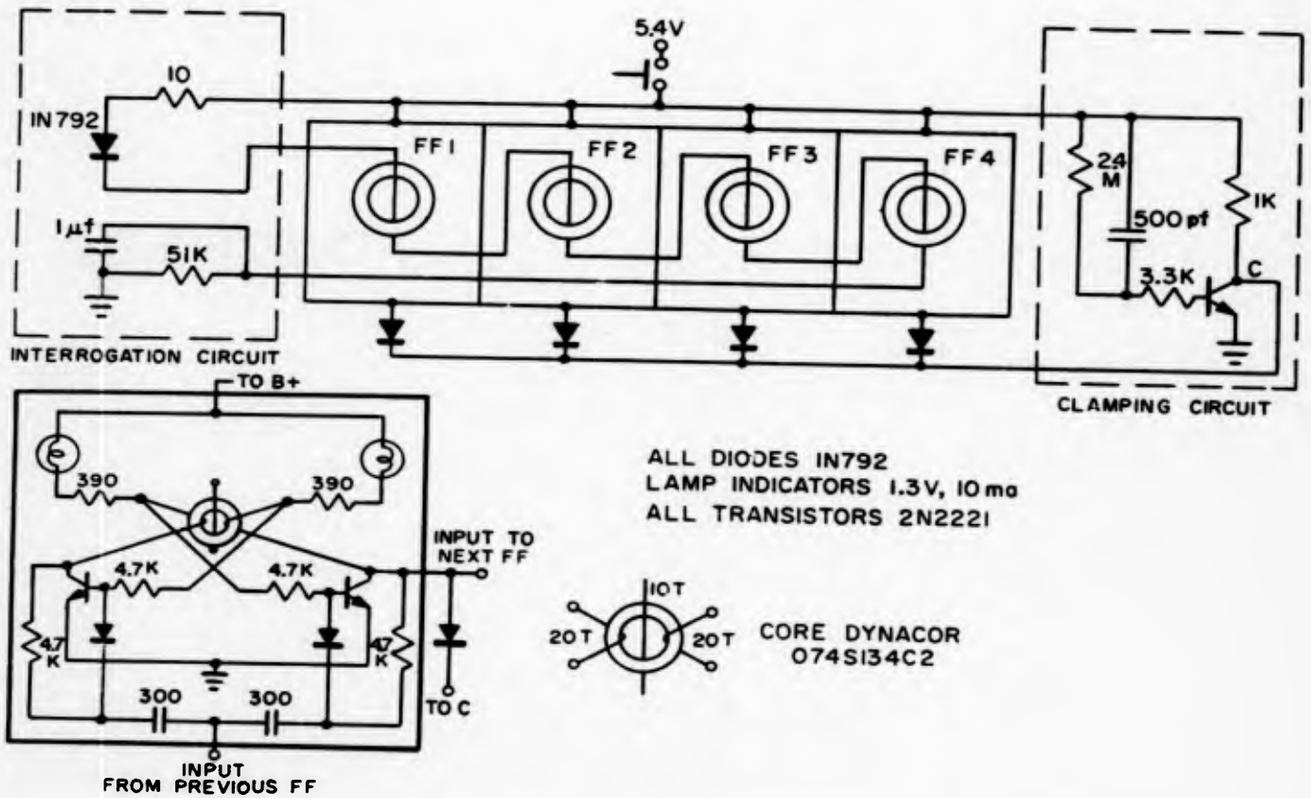

Figure 10. Breadboard schematic of four series flip-flops with common clamping and interrogation circuits.

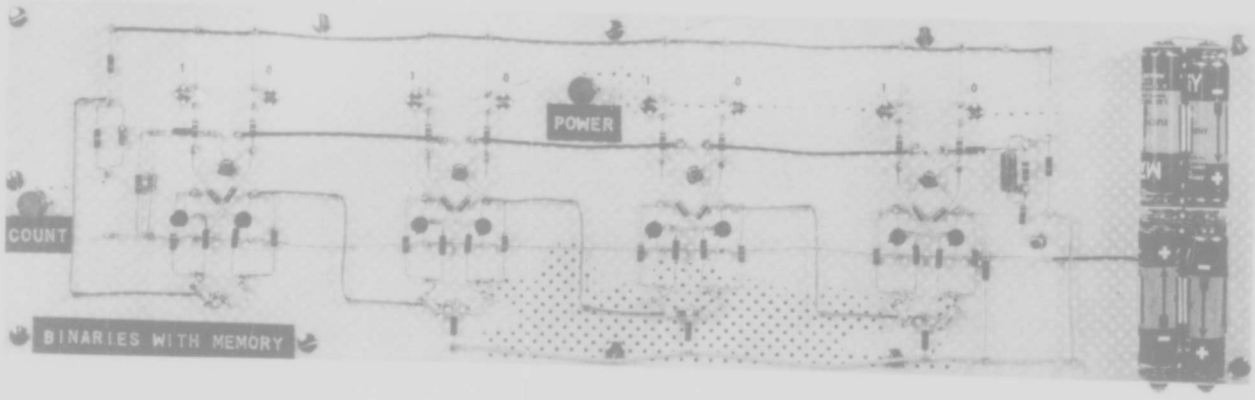

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Figure 11. Breadboard of four flip-flops with memory.

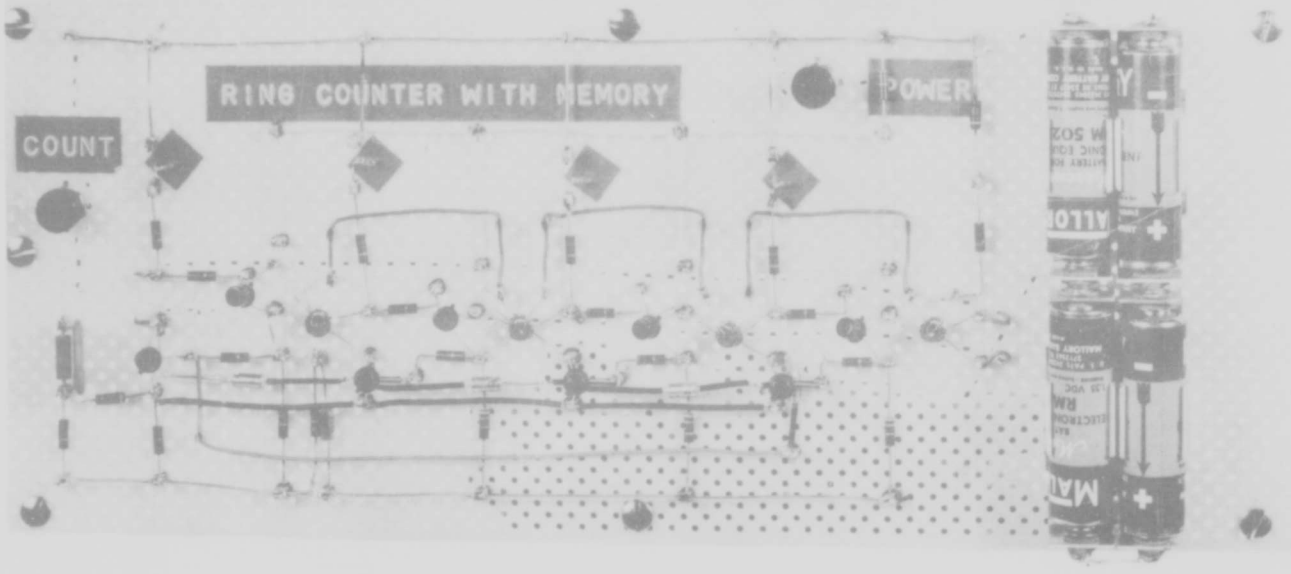

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Figure 12. Breadboard of a four-stage ring counter with memory.

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1. Transistor flip-flop with memory
2. Memory circuit
3. Ring counter with memory
4. Computing circuit

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A modification of the standard transistor flip-flop and ring counter circuits was made that allows setting information to be inserted by an electrical pulse. The supply voltage is not applied to the stages during the insertion of the setting information. When the supply voltage is applied, the flip-flop and ring counter stages assume the desired state. In addition, if during normal operation the supply voltage is interrupted and reapplied, the stages will return to the state they were in before the interruption. These features are incorporated into the flip-flop and ring counter circuits with the addition of one square-loop magnetic core per stage.

1. Transistor flip-flop with memory
2. Memory circuit
3. Ring counter with memory
4. Computing circuit

AD_____ Accession No._____

Harry Diamond Laboratories, Washington, D. C. 20438

TRANSISTOR FLIP-FLOP AND RING COUNTER WITH NONVOLATILE MEMORY--
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