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FINAL REPORT
FOR THE PERIOD
APRIL 1, 1963 TO MAY 30, 1964

TRANSISTORS, TRIODE, SILICON, PNP SWITCHING

U.S. ARMY SIGNAL SUPPLY AGENCY
CONTRACT NO. DA-36-039-AMC-00145(E)

U.S. Army Electronics Research and
Development Laboratory
Fort Monmouth, New Jersey

03-64-30 July 30, 1964

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TRANSISTORS, TRIODE, SILICON, PNP SWITCHING

FINAL REPORT

PERIOD OF

1 APRIL 1963 TO 30 MAY 1964

U.S. Army Signal Supply Agency

Contract No. DA-36-039-AMC-00145(E)

Development of

PNP High Speed Switching Transistor

John Blair
Larry G. Lands
Paul C. Nagle
Robert P. Williams

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PURPOSE

The contract specified the development of a PNP, high-speed silicon switching transistor. Objectives or specifications of major importance are as follows:

1. Leakage currents: I_{CBO}, I_{CEO}, I_{EBO} less than 1 na.
2. Breakdown voltages: BV_{CEO} = 25 v and BV_{EBO} = 6 v at leakage current level of 1 na.
3. Saturation voltage: $V_{CE(sat)} \leq 0.05$ v.
4. Switching times: $t_d \leq 4$ nsec, $t_r \leq 6$ nsec, $t_s \leq 9$ nsec, $t_f \leq 6$nsec.
5. Maximum ratings: I_C = 50 ma, P_C = 0.35 watts, t_j = 200°C, T_{stg} = -65 to 200°C.

Work was broken down into the design, material, diffusion, and contact programs. The associated technology for suitable base contact was of major importance and was the first step in achieving a basic switch design. The development of the diffusion process and material specifications were coordinated with the design in order to improve the device to optimize critical specifications. Lifetime investigations, surface studies, contact techniques, and material preparation were pursued to achieve the design.

Objectives and specifications were re-evaluated in terms of the results in each of the areas of investigation in order to develop the high-speed, switching transistor.

ABSTRACT

Development of the PNP switching transistor specified by contract number DA-36-039-AMC-00145(E) is discussed in detail with emphasis on the design parameters. Problems associated with each of the design parameters are stated and discussed. The methods of approach along with the experimental results are presented for each problem area and the over-all conclusions based upon these experimental results summarize the technical effort of the program. Recommendations are also presented for possible improvement of the transistor. The diffusion and contact procedures as well as the material and electrical specifications are presented in detail enabling a competent technician to produce the developed switching transistor.

Specifically, the transistor has a typical total switching time of 35 nanoseconds and a typical cutoff frequency of 800 megacycles. The delay and rise times are 3.3 and 4.0 nsec respectively. The storage time is 15 nsec. The fall time averages 12 nsec. Gold diffusion would have reduced the storage, but would have had other undesirable effects.

The diffusion process is discussed in detail presenting the techniques involved with $POCL_3$ and BBr_3 as impurity sources. The molybdenum-gold contact system is also presented in detail.

The complete design, assembly, and electrical specifications are presented at the end of the report.

REPORTS

The first quarterly report for the period of 1 April 1963 to 30 June 1963 was published during the second quarter of contract work. Texas Instruments personnel contributing to the report were:

James A. Cunningham
Joseph E. Hall
Larry G. Lands
Paul C. Nagle
Robert P. Williams

The Abstract of the report is as follows:

The design of the PNP silicon switching transistor is discussed in detail. Assuming the desired switching times of 10 and 15 nanoseconds for turn-on and turn-off respectively, the switching time constants are determined and shown to be obtainable by present techniques. Specifically, junction capacitances, $C_{TC} \leq 0.5$ pf and $C_{TE} \leq 2.3$ pf, will be met by shallow diffusions and small unit geometry. Collector-base junction areas of 12 $mils^2$ and 2 $mils^2$ are discussed. The collector-base breakdown voltage of 50 volts is based upon the resistivity and thickness of the epitaxial layer 1.4 Ω-cm and 0.12 mils respectively. For an emitter-base breakdown voltage greater than 6 volts, a base surface concentration of 10^{18} atoms/cc is needed. These requirements place restrictions on the diffusion and contact techniques. The low saturation voltage will be a compromise for low storage time.

The diffusion techniques for obtaining a base depth of 0.035 mils are presented with special attention given to the N+ base contact region. Because of the low base surface concentration, contact to the base region necessitates specific diffusion in the contact area to reduce

the contact resistance. Breakdown voltage data are presented in conjunction with diffusion procedures.

Use of bi-metallic contacts has given favorable results (low contact resistance). Also, degradation of h_{FE} and breakdown voltages is prevalent with many of the contact metals which were investigated.

Surface study experiments show a marked reduction in leakage currents upon bake-out in an ambient atmosphere of O_2.

Data for fabricated units indicate problem areas. These areas are low h_{FE} and f_T, high leakage currents and $V_{CE(sat)}$, and poor breakdowns as a result of contact problems. The sample units sent to the Signal Corps had low h_{FE} (below 10) which did not enable measurement of switching times. Following devices were improved and switching times of 17 and 41 nanoseconds for turn-on and turn-off respectively were obtained.

Second Quarterly Report

The second quarterly report covering the work performed from 1 July to 30 September 1963 was published January 20, 1964, during the fourth quarter of contract work. Texas Instruments personnel contributing to the report were:

Larry G. Lands
Paul C. Nagle
Robert P. Williams

The Abstract of the report is as follows:

Sample devices are discussed in detail, with explanations of the problem areas and results of the experimental investigations reported.

Using the small geometry (1.96 $mils^2$ base area), a turn-on time of less than 10 nanoseconds and a turn-off time of less than 20 nanoseconds have been achieved. The reduction of storage time by the use of gold doping is discussed.

Saturation voltage, $V_{CE(sat)}$, is a major problem, but the data indicate possible improve-

ments. Leakage currents are discussed and it is shown that use of a guard ring reduces these currents considerably. Slice preparation, diffusion and contact techniques are examined in detail and conclusions are stated.

The design of material specifications is described and the effect upon the device parameter is indicated.

Specifically, sample device parameters have the following typical values:

I_{CBO}, I_{CEO}	100	μa
I_{EBO}	1	na
BV_{CEO}	20	v
BV_{EBO}	9	v
$\|h_{fe}\|$	15	db
h_{FE}	50	
$V_{CE(sat)}$	.3	v
LV_{CES}	20	v
C_{ob}	2	pf

The program for the next interval is discussed in detail based on the conclusions stated in this report.

Third Quarterly Report

The third quarterly report covering the work performed from 1 October to 31 December was published February 25, 1964 during the fourth quarter of contract work. Texas Instruments personnel contributing to the report were:

Larry G. Lands

Paul C. Nagle

The Abstract of the report is as follows:

The PNP silicon switching transistor is discussed in detail with emphasis on the design parameters. Switching time constants are determined and correlated with the present diffusion techniques. The junction capacitances, $C_{TC} \leq 0.5$ pf and $C_{TE} \leq 2.8$ pf, have been met by the shallow diffusions and small unit geometry. As a consequence, the delay time is within the specified limits. Rise time and storage time requirements also have been met. The fall time, however, is twice as long as required primarily due to the 0.25-ma turn-off current.

It is shown that the base transit time has been increased to 160 psec which is larger than expected and is the major delay time contributing to the measured frequency response of 800 mc. The curves for concentration and depletion layer width indicate the relative concentration levels for large and small area units. A comparison of f_T versus emitter current for these geometries shows that the peak is at 3 ma for small area units and 10 ma for the large area units. Other parameters are discussed and examined as well as the restrictions which are placed on the device by the diffusion and contact techniques.

Experimental work in diffusion has been concerned with a device analysis of the second diffusion sequence which was presented in the second quarterly report. Both geometries were used for this study. An additional study was conducted to determine the effect of the N+ deposition on device characteristics. Data are presented indicating the degradation of BV_{CBO} as a result of the N+ diffusion sequence. Current gain is shown to be at the same levels for both geometries.

Reliability data for preliminary large area units are presented. The leakage current level was high, however, and the problems involved with its improvement are discussed.

The present design and electrical parameters are stated for the PNP switch developed with the small area geometry.

CONFERENCES

The first meeting during the contract period was held on May 22, 1963. William Kiss of USAEMA visited Texas Instruments to discuss Signal Corps requirements and the progress of the contract work. Texas Instruments personnel present at the meeting were:

J. A. Cunningham
J. E. Hall
L. G. Lands
A. T. Nemecek
F. J. Strieter
W. P. Waters

The second meeting for the Signal Corps Contract — PNP logic switch was held at the U.S. Army Electronics Material Agency, Fort Monmouth, New Jersey, on October 4, 1963.

The USAEMA personnel attending the meeting were Konrad Fischer and William Kiss. Texas Instruments personnel were Paul Nagle, Semiconductor Research & Development Laboratory, and Dave McGrath, TI Elizabeth office.

The device specifications were discussed in detail and unofficial changes were agreed upon and signed by William Kiss. These specifications are listed on the following page.

SYMBOL	CONDITION	PRESENT VALUE	PREVIOUS VALUE
BV_{CEO}	I_{CEO} = 1 na	25 Vdc	35 Vdc
BV_{EBO}	I_{EBO} = 1 na	6 Vdc	12 Vdc
I_{CBO}	V_{CB} = 25 Vdc I_E = 0	1 na	1 na at V_{CB} = 35 Vdc
I_{CEO}	V_{CE} = 25 Vdc I_B = 0	1 na	1 na at V_{CE} = 35 Vdc
I_{EBO}	V_{EB} = 6 Vdc I_C = 0	1 na	1 na at V_{EB} = 6 Vdc
I_C		50 ma dc	100 ma dc
P_C		0.35 watts	1.0 watts
Operating Life	V_{CE} = 10 v I_C = 35 ma 1000 hours		V_{CE} = 15 Vdc I_C = 66 ma dc 1000 hours
End Test Points I_{CBO}	V_{CB} = 25 Vdc I_E = 0	2 na dc	2 na at V_{CB} = 35 Vdc I_E = 0
I_{CEO}	V_{CE} = 25 Vdc I_B = 0	2 na dc	2 na at V_{CB} = 35 Vdc I_B = 0

Specifications of major importance were discussed and their attainment was clarified. Specifically, the storage time of 9 nsec will be attained without the use of gold diffusion techniques. This will keep $V_{CE(sat)}$ at the minimum design value. The N+ contact region in the low impurity concentration base allows adequate contact but restricts the base region and diffusion process. The problems concerning leakage currents and surface conditions were discussed.

TI expressed the need for the same evaluation procedures to be incorporated at the Agency as those used by TI. Switching circuits will be built for USAEMA use. The first quarterly report was reviewed, and the project status and direction was discussed in detail.

On December 10, 1963, William Kiss visited Texas Instruments and a conference was held concerning the contract requirements and the progress of the contract work. Texas Instruments personnel present at the conference were:

M. L. Barr
L. G. Lands
P. C. Nagle
A. T. Nemecek
D. Prohaska
F. J. Strieter
R. Webster
R. P. Williams

Current problem areas were discussed in detail and sample units were tested. The contract expenditures were reviewed in detail and forecast costs were presented. The second quarterly report was examined and corrected.

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SYMBOLS

BV_{CBO}	Collector-base breakdown voltage
BV_{CEO}	Collector-emitter breakdown voltage (open base)
BV_{EBO}	Emitter-base breakdown voltage
C_{TC}	Collector junction capacitance
C_{TE}	Emitter junction capacitance
C_{TOTAL}	Total capacitance (collector plus emitter junction plus interlead plus header shunt and circuit capacitance.)
C_C	Collector capacitance (junction plus interlead and circuit capacitance)
C_{OB}	Common base output capacitance (junction plus interlead plus header shunt)
D	Diffusion constant
f_T	Current-gain-bandwidth frequency
h_{FE}	Grounded-emitter d-c current gain
I_B	Base current
I_{B1}	Turn-on base current
I_{B2}	Turn-off base current
I_C	Collector current
I_{CBO}	Collector-base reverse current
I_{CEO}	Collector-emitter reverse current (open base)
I_E	Emitter current
I_{EBO}	Emitter-base reverse current
μ_p	Hole mobility
N	Impurity concentration
N_{BC}	Background impurity concentration
N_o	Surface impurity concentration
Q_B	Base charge
R	Resistance
R_L	Load resistance
r'_B	Base resistance
ρ	Resistivity

Φ	Contact Potential
$(K\epsilon_o)$	Dielectric Constant - 1.062×10^{-12} Farad/cm (silicon)
t	Time
t_d	Delay time
t_f	Fall time
t_r	Rise time
t_s	Storage time
τ_b	Base transit time
τ_d	Delay time constant
τ_r	Rise time constant
τ_f	Fall time constant
τ_s	Storage time constant
V_{BE}	Base emitter forward bias voltage
$V_{BE(off)}$	Emitter reverse bias voltage
V_C	Collector voltage
V_{CC}	Collector supply voltage
$V_{CE(sat)}$	Grounded-emitter saturation voltage
W	Effective base width
W_e	Epitaxial layer thickness
X_j	Junction depth from surface

SECTION I
DESIGN OF PNP SWITCHING TRANSISTOR

A. GENERAL DESCRIPTION

The developed device is a PNP silicon, triode junction, planar, epitaxial transistor for use in high speed switching applications. The transistor is made on P-type epitaxial material. The epitaxial layer is 5 microns thick and has a resistivity of 2 ohm-cm.

The base and emitter regions are formed by respective phosphorous and boron diffusions. These diffusions are extremely shallow. Specifically, the collector-base junction depth is 0.05 mils and the emitter-base junction depth is approximately 0.03 mils. The junctions produced by these ditfusions have graded concentration profiles.

A P+ recision ring is diffused during the emitter diffusion. This recision ring completely surrounds the base and contact areas of the transistor and is used to reduce leakage currents.

Photomasking techniques define the transistor areas and are incorporated with the diffusion procedure. Figure 1 shows the geometry used for the device. It has a base area of 2 $mils^2$ and an emitter area of 0.2 $mils^2$. This transistor because of its small areas has junction capacitances which are considerably less than those of commonly used structures. Figure 2 shows a larger, more conventional structure with a base area of 12 $mils^2$ and an emitter area of 0.6 $mils^2$. It was used in the early phases of the development. The area comparison of these two geometries is shown in Fig. 3. The lower capacitance produced by the 2 mil^2 geometry provides faster switching times than those resulting from the 12 mil^2 geometry.

This transistor has molybdenum-gold expanded contacts. Figure 4 illustrates the

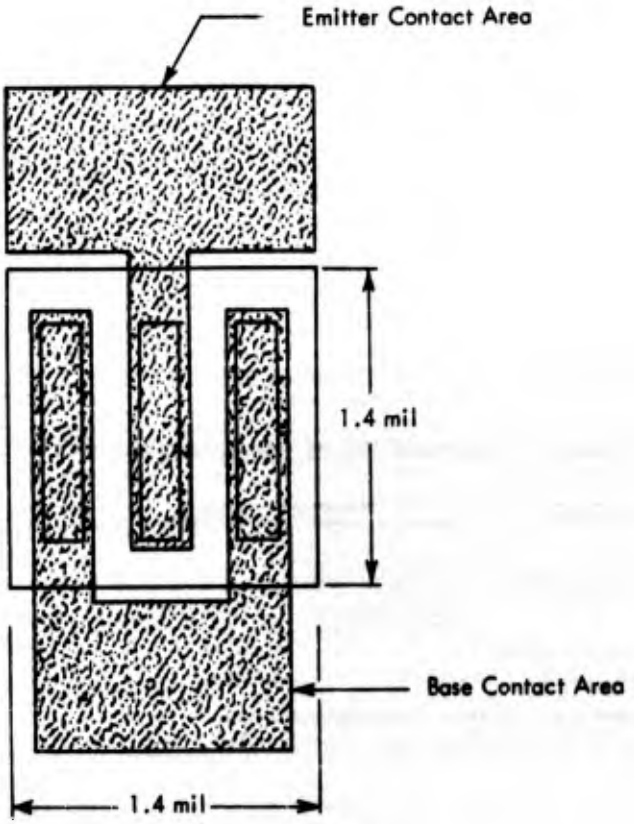


Fig. 1. Small Area Geometry

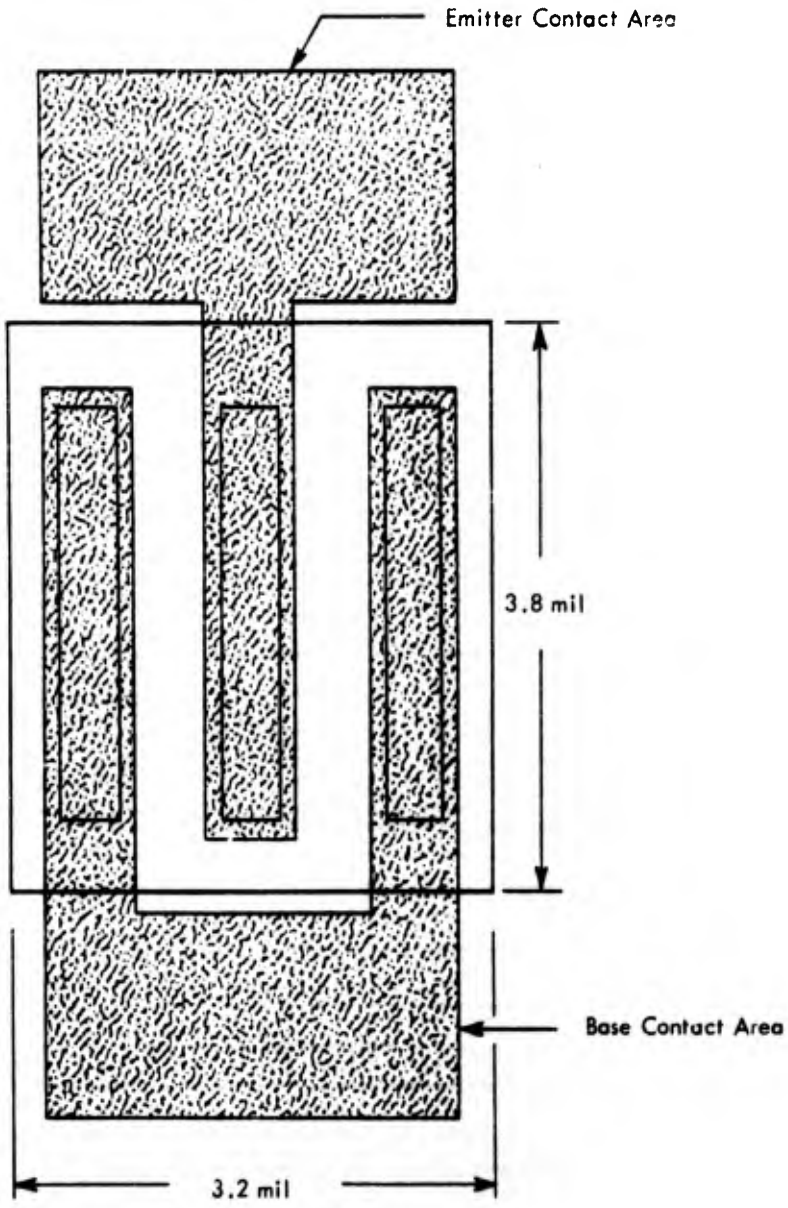
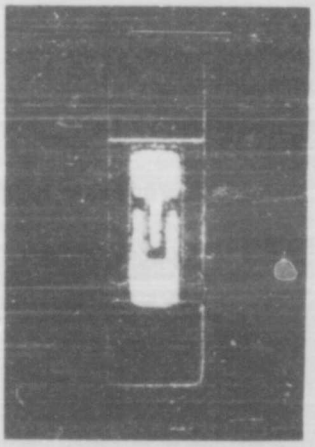


Fig. 2. Large Area Geometry



SIZE COMPARISON 300X

Fig. 3. Size Comparison — Large and Small Geometry

A. Small Area Unit

B. 1 Mil Scale

Fig. 4. Small Area Unit

expanded contact. Because of the small base and emitter areas, leads are connected (bonded) to these areas by providing larger emitter and base bonding areas or tabs outside of the base area. These tabs are insulated from the silicon surface by the protective oxide, SiO_2, grown on the surface at the beginning of the diffusion process. In conjunction with the MoAu contacts, an N+ region is diffused into the base region to provide a high surface concentration which is necessary for low contact resistance.

B. SWITCHING TIMES

The transistor switching performance is specified in terms of delay, rise, storage and fall times. These times must be related to internal device parameters which are more or less directly related to measurable physical properties of the device, if they are to have significant meaning in device design.

The principal relationships between switching time and device parameters are summarized below:

Switching Term	Symbol	Related Device Parameter	Symbol
Delay time	t_d	Collector junction capacitance	C_{TC}
		Emitter junction capacitance	C_{TE}
		Emitter-base junction turn-on voltage	$V_{BE(on)}$
Rise time	t_r	Collector junction capacitance	C_{TC}
		Cutoff Frequency	f_T
		Current gain	h_{FE}
Storage time	t_s	Storage time constant	τ_s
Fall time	t_f	Collector junction capacitance	C_{TC}
		Cutoff frequency	f_T
		Current gain	h_{FE}

In general, each of these may be related to specific physical properties of the device (with the possible exception of τ_s and h_{FE}).

The actual situation is more complicated than this simple view, since the related capacitances should include socket, wiring, and header capacitance.

The present device switches at very high speed and has very small capacitance, so that switching speed is seriously affected by circuit parasitics. In evaluating limits for capacitance, cutoff frequency, etc., values of these parameters for the circuit may be computed. However, the allowable device capacitance can only be estimated after suitable allowance for the header, socket, and test fixture.

In the following paragraphs which discuss switching time, the distinction between device junction capacitances and circuit capacitances must be kept in mind.

1. Delay Time

The delay time of the PNP switching transistor averages 3.3 nsec which is better than the design value of 4 nsec.

Early calculations indicated that the design value of the delay time could be met with a total capacitance of C_{Total}, of 3.3 pf.

The total capacitance, C_{Total}, is the sum of the collector junction capacitance, C_{TC}, and the emitter junction capacitance, C_{TE}, over the appropriate turn-on voltage range, plus the interlead capacitances and the shunt and switching jig capacitances.

Transistor geometries of 2 mil^2 and 12 mil^2 base area were used for preliminary units. The second sample of transistors sent to the Signal Corps indicated that the 2 mil^2 geometry would satisfy the capacitance requirement for the desired delay time[2]. Typical capacitance and delay time values for the two geometries are stated below.[3]

Geometry	Junction Capacitance	Total Capacitance	Delay Time
2 mil^2	0.8 pf	3.3 pf	4 nsec
12 mil^2	6.0 pf	8.7 pf	9.8 nsec

From previous experience with the 2 mil^2 geometry and knowledge of switching jigs, it became apparent that the total capacitance was larger than expected. Investigation indicated that the capacitance of the switching jig should be reduced. This investigation was reported in the Third Quarterly Report and was discussed at the second meeting with the Signal Corps.[3] The switching circuit is presented in Section VII of this report.

The delay time can be described by the following equation:[4]

$$t_d \simeq \frac{C_{Total}\left(|V_{BE(on)}| + |V_{BE(off)}|\right)}{I_{B1}}$$

This equation can be used to determine the total capacitance associated with the measured delay time. The turn-on current I_{B1} is 1 ma and the base to emitter voltage change is from + 0.5 v d-c to -0.9 v d-c. Under these conditions, the total capacitance is 2.3 pf for a measured delay time of 3.3 nsec. Refer to Fig. 5 for a summary of measured delay time vs total capacitance.

2. Fall Time

The fall time, t_f, averages 11 nsec, rather than 6 nsec as specified in the contract. The fall time is described in terms of the base transit time, τ_b, which is the reciprocal of $2\pi f_T$, and switching circuit parameters by the following equation:[4]

$$t_f \simeq h_{FE}\left(\tau_b + R_L C_C\right) \ln \frac{\left|\frac{I_C}{I_{B2}}\right| + h_{FE}}{0.1\left|\frac{I_C}{I_{B2}}\right| + h_{FE}}$$

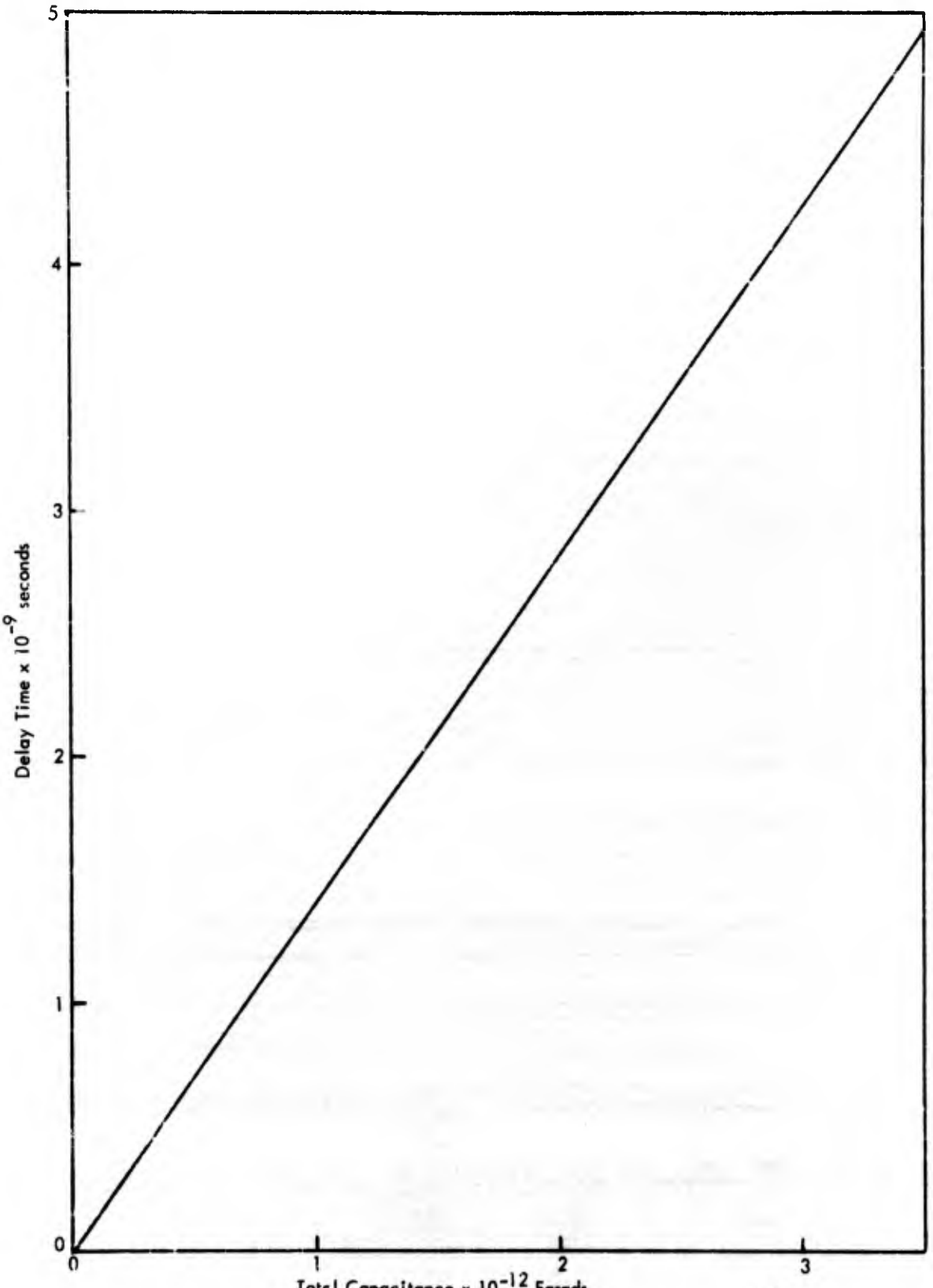


Fig. 5. Delay Time vs Total Capacitance

where ($\tau_b + R_L C_C$) is the fall time constant, τ_f and C_C is the collector capacitance which is the sum of the junction capacitance, the interlead capacitance, and the switching jig capacitance.

Calculations reported during the first quarter showed that for an h_{FE} of 50 the fall time constant, τ_f, needed to be of the order of 200 psec for a fall time of 6 nsec. Original calculations assumed a value of collector capacitance, C_C, of 0.5 pf which gives an $R_L C_C$ time constant of 150 psec. Thus, τ_b must be of the order of 50 psec and f_T must be about 2000 mc.

Data on the present units show that an h_{FE} of 30 should be used for switching time calculations. Also, the base transit time is actually 200 psec which corresponds to an f_T of 800 mc and the capacitance, C_C, is of the order of 0.8 pf. Therefore, in present devices, τ_b and $R_L C_C$ are both considerably greater than proposed above.

Reference is now made to Fig. 6 which is a plot of fall time, t_f, as a function of h_{FE} and f_T for the given circuit conditions and C_C of 0.8 pf. It should be noted that for a capacitance value of 0.8 pf, a considerable increase in f_T is needed to produce a sizable change in fall time.

3. Rise Time

The rise time is 4.0 nsec and is consistent with the design value. Figure 7 plots rise time as a function of h_{FE} and f_T. It should be noted that as the current gain, h_{FE}, increases, the rise time remains constant. This is not so with the fall time and for the specific turn-off current I_{B2} = 0.25 ma the fall time varies greatly with current gain.

The rise time can be calculated from the equation:[4]

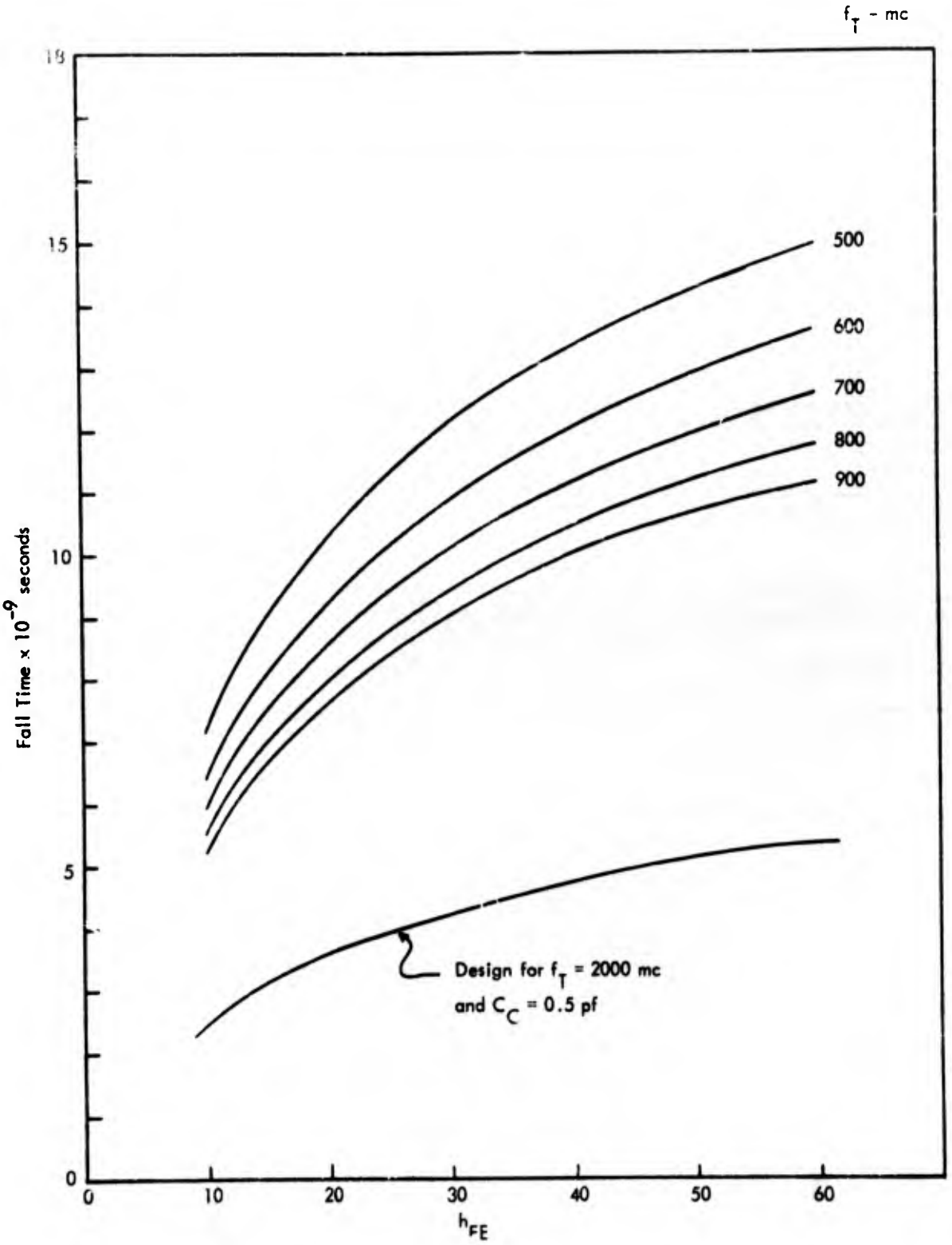


Fig. 6. Fall Time vs Current Gain and Cutoff Frequency C_C = 0.8 pf

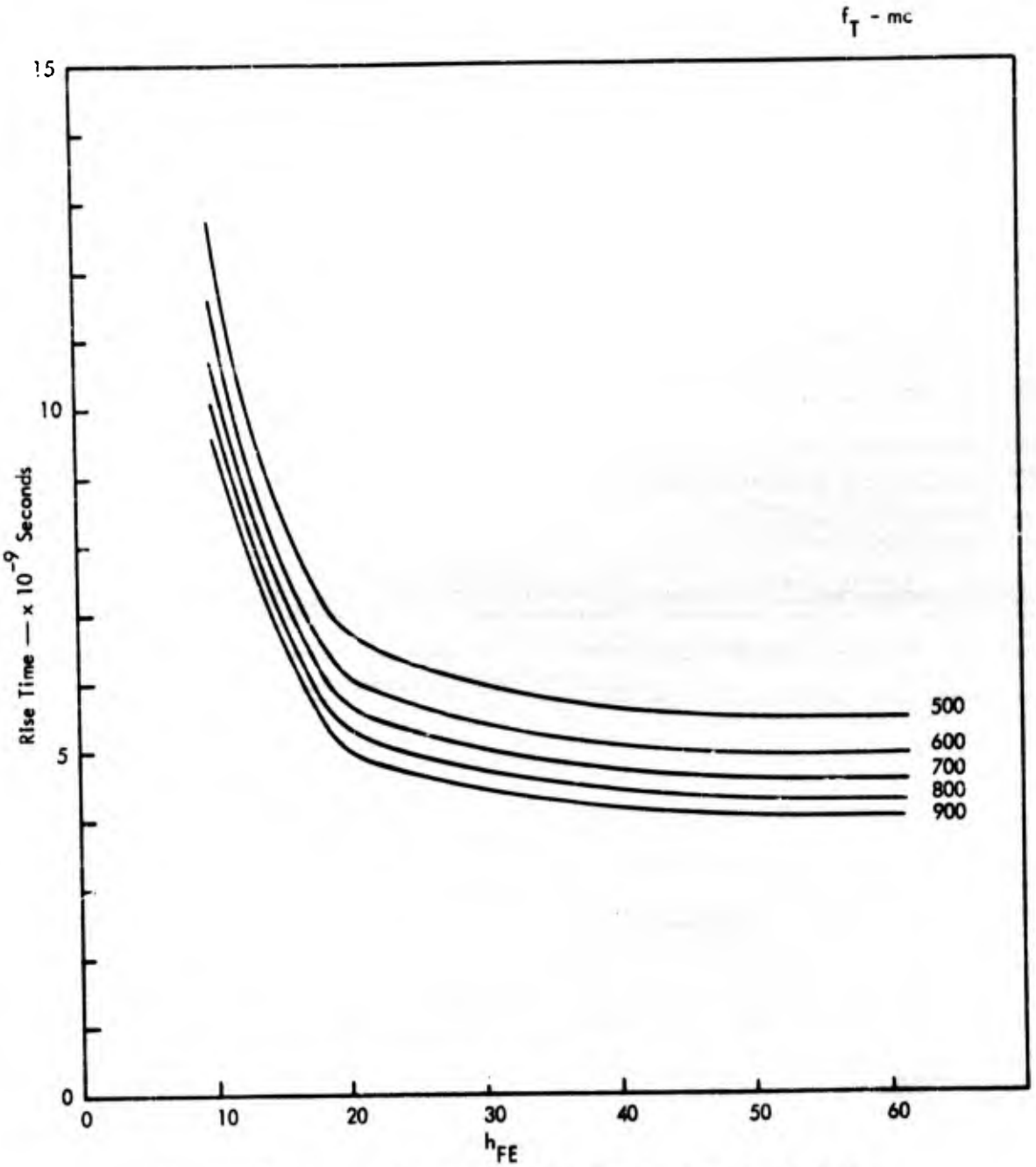


Fig. 7. Rise Time vs Current Gain and Cutoff Frequency C_C = 0.6 pf

$$t_r \simeq h_{FE} (\tau_b + R_L C_C) \ln \frac{h_{FE}}{h_{FE} - 0.9 \frac{I_C}{I_{B1}}}$$

where $(\tau_b + R_L C_C)$ is the rise time constant, τ_r, identical with the fall time constant discussed above. The rise time constant, τ_r, is 400 psec for this calculation. It is emphasized that in order to obtain the fall time specified by the contract, a fall time constant of less than half the required rise time constant is needed.

4. Storage Time

The storage time averages 15 nsec which is considerably greater than the desired value of 9 nsec. The storage time measured for previous units was approximately 10 nsec, [2,3] but this low value was the result of low current gain, h_{FE}. Figure 8 shows storage time vs h_{FE} and τ_s. It is calculated from the following equation:[4]

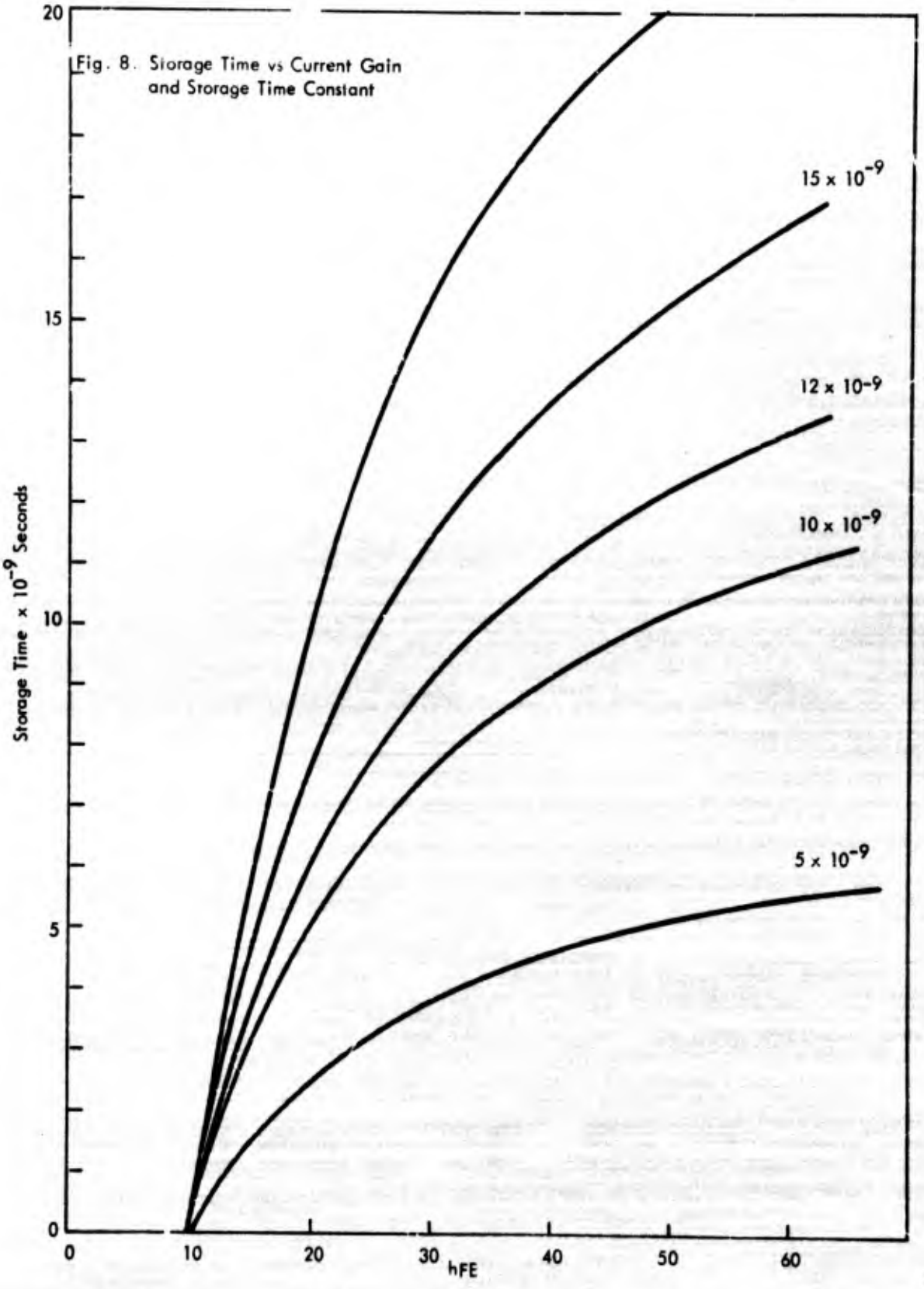
$$t_s \simeq \tau_s \ln \frac{I_{B1} - I_{B2}}{\frac{I_C}{h_{FE}} - I_{B2}}$$

where τ_s is the storage time constant.

The typical storage time constan for the developed transistors is 20×10^{-9} seconds. It is apparent from the curves that for this value of storage time constant, an increase in h_{FE} will produce a large increase in storage time. Also, it should be noted that if the storage time constant is less than 10×10^{-9} seconds, the increase in storage time with h_{FE} is reduced considerably. Good gold diffused NPN transistors have storage time constants around 5×10^{-9} seconds.[1] Therefore, it was expected that if lifetime could be controlled by gold diffusion techniques, the storage time constant could be reduced to its design value of 4×10^{-9} seconds. However, the component of

$20 \times 10^{-Y} = \tau_s$

Fig. 8. Storage Time vs Current Gain and Storage Time Constant



$V_{CE(sat)}$ due to transistor action is inversely proportional to stored charge, so that a compromise between $V_{CE(sat)}$ and storage time must be made.[5] Diffusion run 31A as reported in the second quarterly report was gold diffused in order to control the lifetime and, therefore, reduce the storage time. The data indicate that a storage time of 6 nsec was obtained, but the $V_{CE(sat)}$ was 1.5 v at I_C = 10 ma and I_B = 1 ma, an excessive value for a switching transistor. Saturation voltage will be discussed in Section I-F.

C. CAPACITANCES

The contract specified the value of the common base output capacitance, C_{OB}, to be a maximum of 2 pf at V_{CB} = 15 v. The C_{OB} values for present devices are 1.1 pf at the 15 volt level. It should be noted that this capacitance is the sum of the junction capacitance, the interlead capacitance, and the header shunt capacitance.

For switching transistor design, it is necessary to consider additional capacitance requirements. The switching time requirements t_d, t_r, and t_f set maximum values for the associated capacitances. These values are presented along with the values determined for actual units.

Associated Capacitance	Maximum Value	Actual Value
C_{Total}	3.3 pf	2.3 pf
C_C	0.5 pf	0.8 pf

The total capacitance, C_{Total}, is associated with the delay time and is the sum of the collector and emitter junction capacitances, the interlead capacitance, the header shunt capacitance, and the switching jig capacitance.

The collector capacitance, C_C, is associated with the rise and fall times and is the sum of the collector junction capacitance, the interlead capacitance, and the switching jig capacitance.

It is important to realize that capacitances other than the collector and emitter junction capacitances, C_{TC} and C_{TE}, greatly affect the switching performance of the developed transistors.

The junction capacitances C_{TC} and C_{TE} are the device capacitances which can be related to the internal physical properties of the transistor. Specifically, the junction capacitances are determined by geometry and impurity concentrations.

The collector junction capacitance, C_{TC}, can be calculated approximately from the following equation for capacitance which applies to a step junction:

$$\frac{C}{A} = \sqrt{\frac{q\,(K\epsilon_o)\,N_A}{2\,(V+\phi)}}$$

where Irvins curves[6] are used to relate N_A to resistivity. Assuming a contact potential of 0.5 volts, the capacitance calculated for a P-type collector resistivity of 2 Ω-cm ($N_A = 7 \times 10^{15}$ atoms/cc) and a collector area of 2 mils^2 is approximately 0.26 pf at $V_{CB} = 1$ volt. It is interesting to note that if the large area geometry (base area = 12 mils^2) is used, the collector resistivity necessary for a capacitance value of 0.26 pf is 10 Ω-cm.

Figure 9 shows the measured collector junction capacitance vs V_{CB} for the developed transistor (base area = 2 mils^2). For comparison, Fig. 10 shows measured C_{TC} capacitance vs V_{CB} for the large area geometry. The collector junction capacitance, C_{TC}, measured at $V_{CB} = 1$ volt for developed transistors is 0.4 pf. This is larger than the calculated value because the assumption of step junction is not necessarily valid for the diffused profile.

The emitter junction capacitance, C_{TE}, is even more difficult to calculate, since it depends on the graded concentration of impurities on both sides of a double-diffused junction. Measurement indicates, however, that a practical value of 0.4 pf at 0 v has been attained. Refer to Fig. 11 which shows C_{TE} vs V_{EB} for the developed tran-

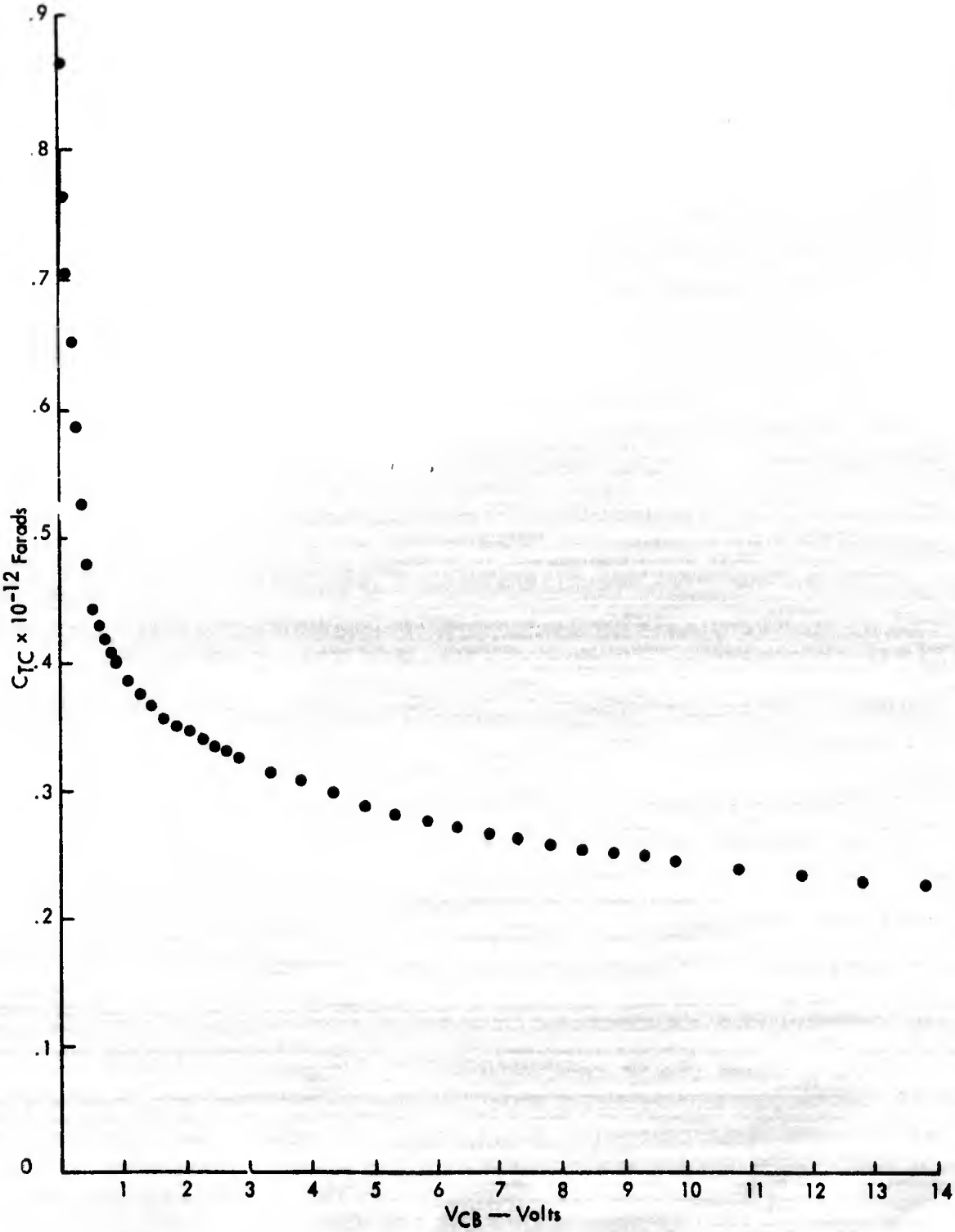


Fig. 9. Small Area Unit C_{TC} vs V_{CB}

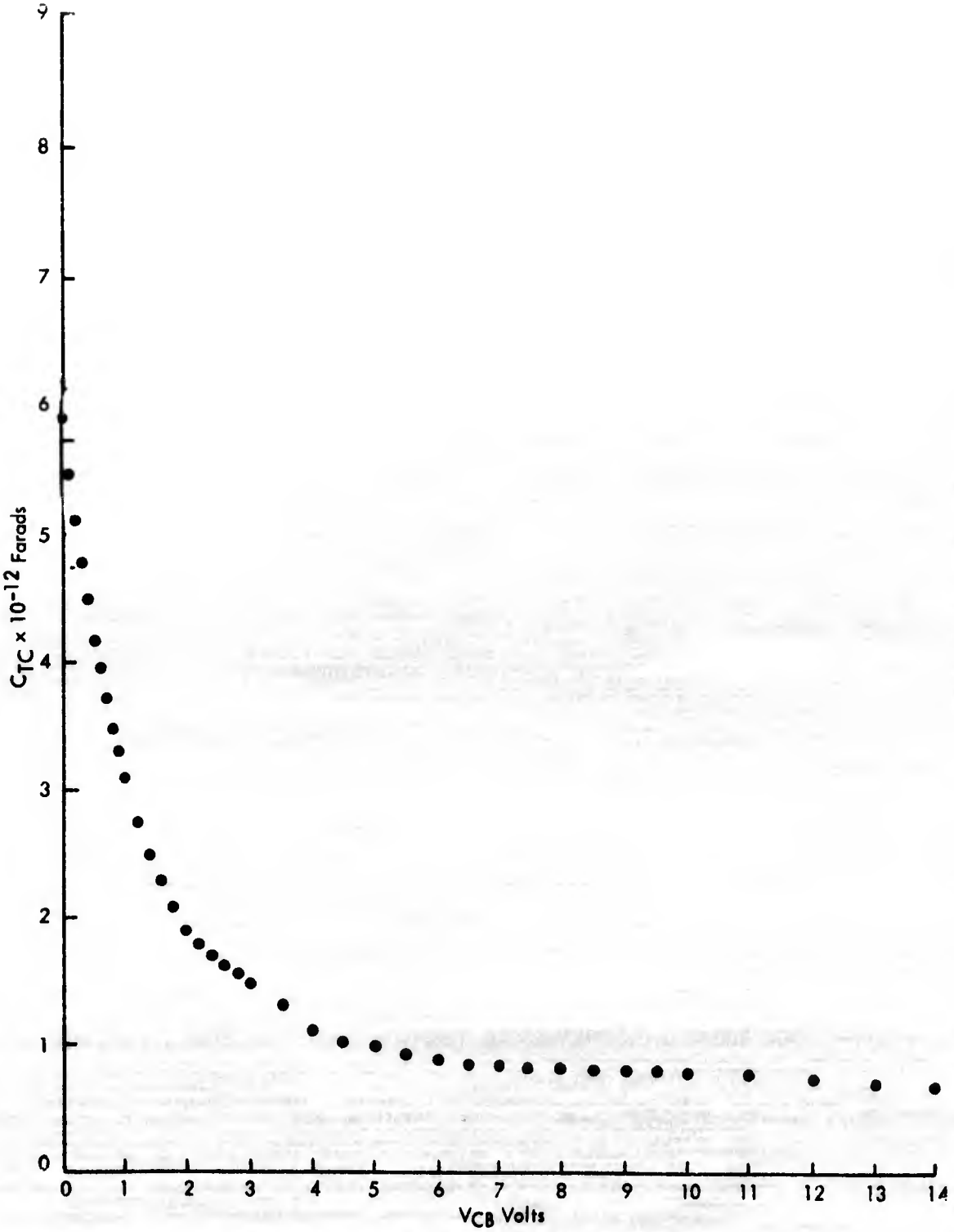


Fig. 10. Large Area Units C_{TC} vs V_{CB}

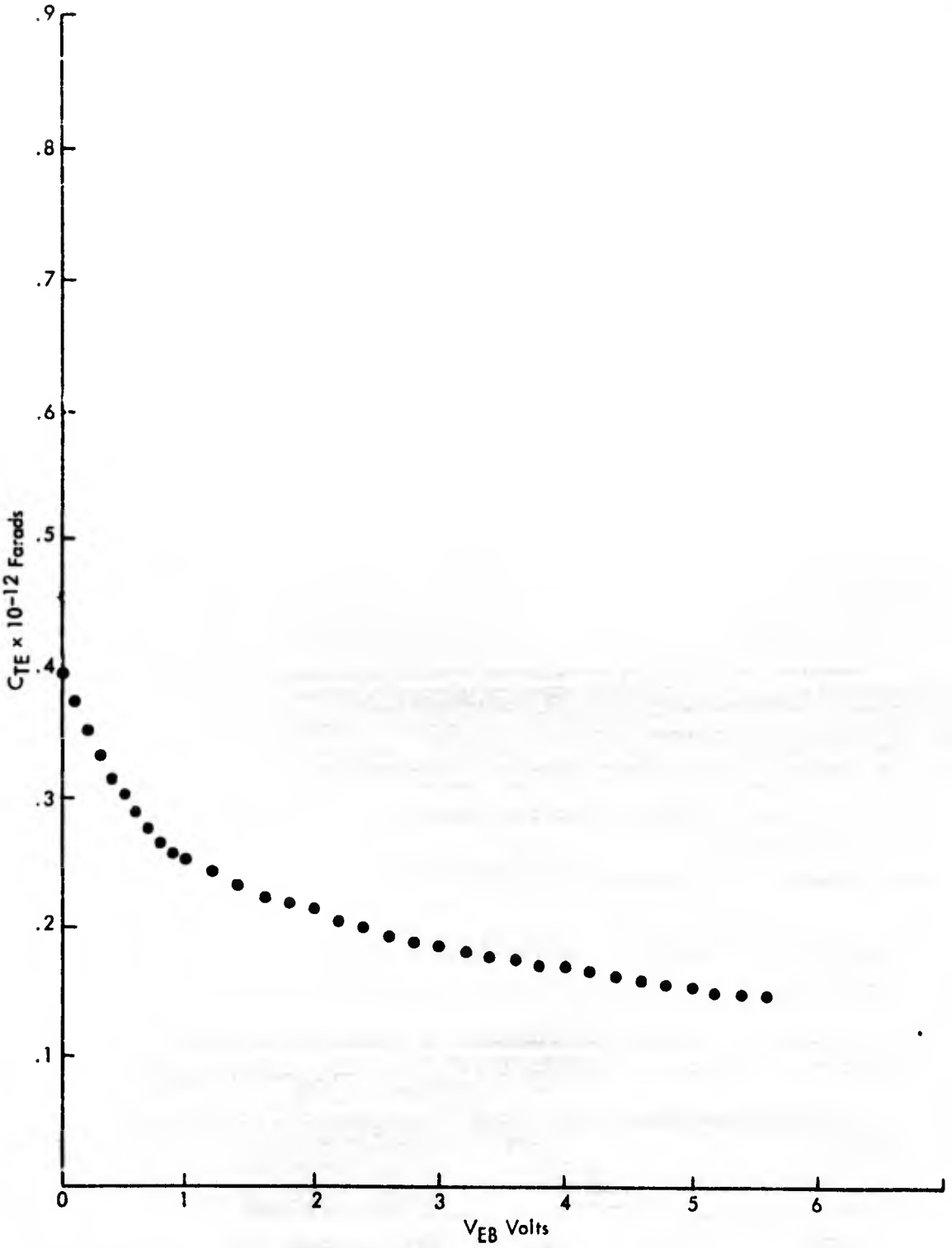


Fig. 11. Small Area Unit C_{TE} vs V_{EB}

sistor. Comparison may be made with Fig. 12 showing C_{TE} vs V_{EB} for the large area geometry.

As was previously stated, header shunt capacitance, interlead capacitance, and switching jig capacitance must also be accounted for in the design. Figures 13 and 14 are for a four-lead TO-18 header and are adequate approximations of the header shunt capacitance and the interlead capacitance.

Accounting for the junction and package capacitances above, a sizable switching jig capacitance is found to be associated with switching time measurements. Specifically, a switching time capacitance of approximately 1.0 pf is associated with the total capacitance, C_{Total}. A switching jig capacitance of the order of 0.3 pf contributes to the collector capacitance, C_C. These fixture capacitances were considerably higher in the original test fixture, and increased switching time considerably. They still are large enough to limit switching performance in the present redesigned jig.

D. BASE TRANSIT TIME

The base transit time averages 200 psec for the developed transistors. This is considerably greater than the proposed value of 35 psec.[1]

The original calculation was made using the following equation and assumptions:[4]

$$\tau_b = \frac{W^2}{2KD_p}$$

where the diffusion constant, $D_p = \frac{kT}{q}\mu_p$ and K is a correction to account for the drift field in the graded base. Curves by Prince[7] give hole mobility, μ_p, as a function of concentration and assuming an average impurity concentration in the base region underneath the emitter of 10^{17} atoms/cc, a hole mobility of 250 cm^2/volt-sec is determined from the curves. This is equivalent to a diffusion constant of 6.5 cm^2/sec. Assuming a base width, W, of 0.012 mils, the base transit time is calculated to be 35 psec.

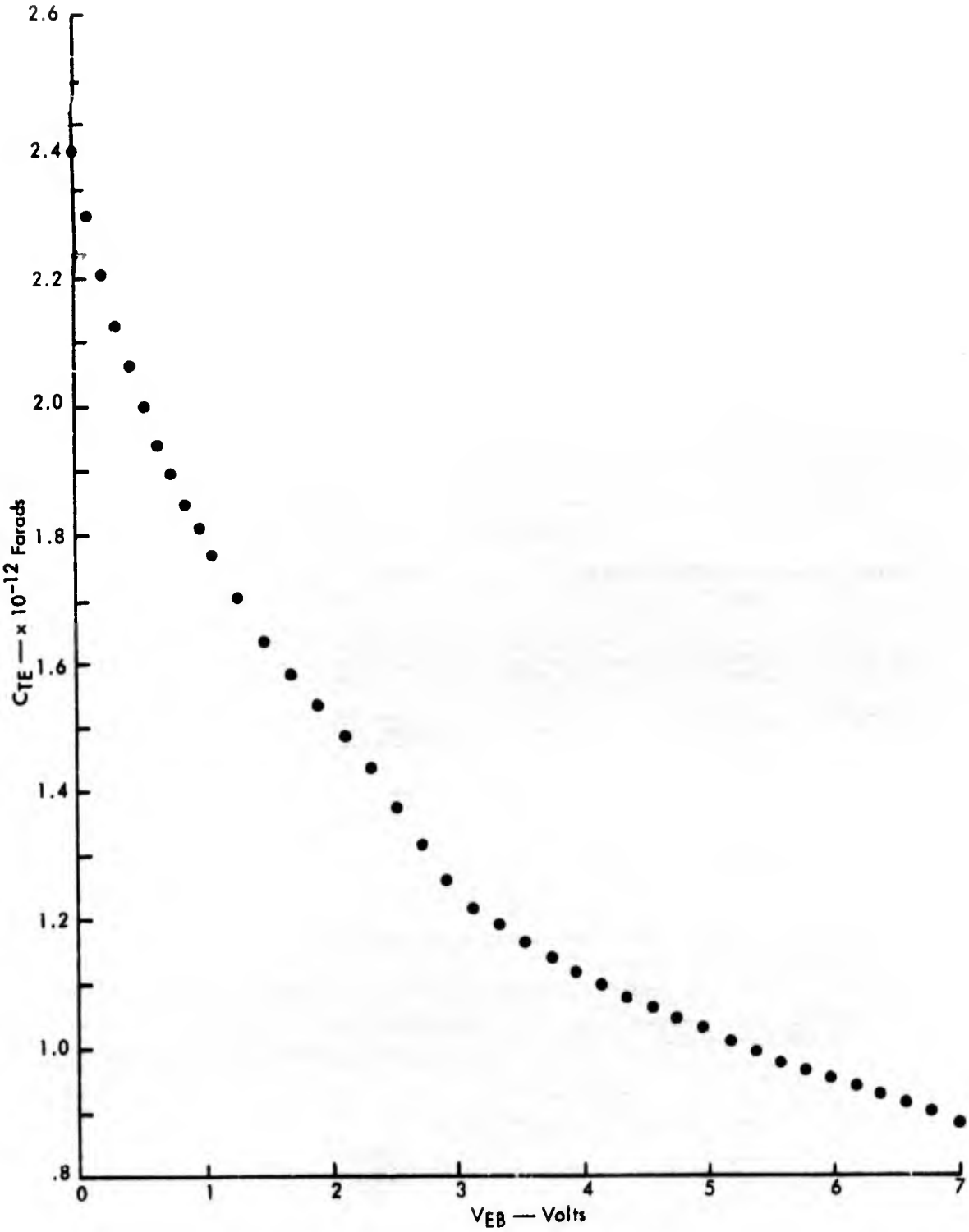


Fig. 12. Large Area Units C_{TE} vs V_{EB}

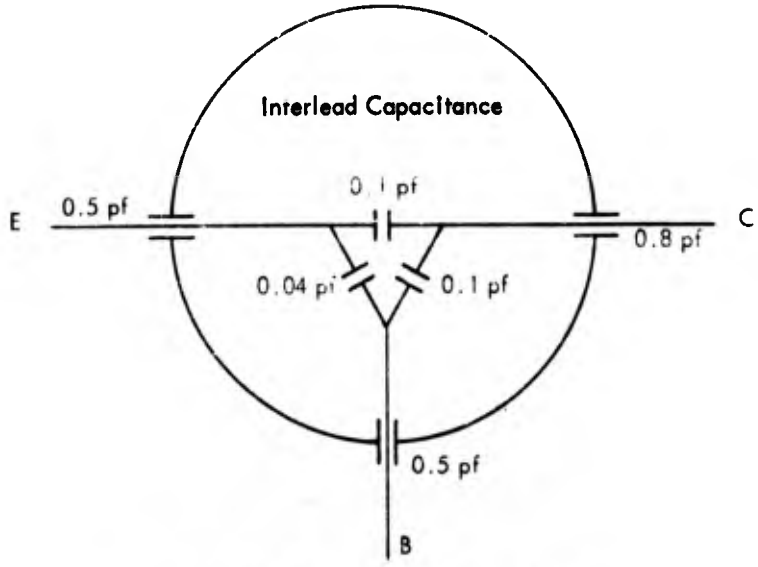


Fig. 13. Package Equivalent Circuit

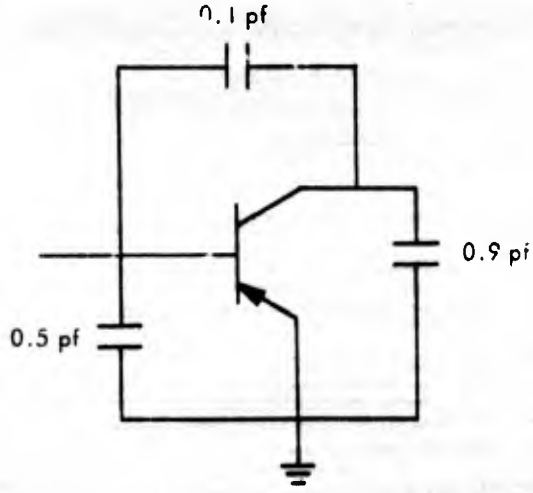


Fig. 14. Device with Package Capacitances (case grounded)

From the capacitance voltage plots (Figs. 9 and 11) and computer programming based on electrical charge and depletion region theories,[8] depletion layer widening versus impurity concentration can be obtained for the collector-base and emitter-base junctions. These are shown in Figs. 15 and 16. Figure 17 summarizes the information obtained and states that the base concentration underneath the emitter averages 5×10^{17} atoms/cc. This increase from the design value of 10^{17} atoms/cc is the result of the N+ regions and decision to have a 6-volt emitter-base breakdown instead of 12 volts. Figure 18 shows a base width, W, of approximately 0.02 mils instead of 0.012 mils as proposed. This value for the base width is in agreement with f_T considerations which will be presented in the next section. These changes over the proposed values produce a marked change in τ_b. The base transit time is greater than 160 psec upon this re-evaluation and is in agreement with the calculation based upon switching times in sections I-B and I-C.

The impurity concentration summary of Fig. 17 is the result of analysis of Figs. 15 and 16. This analysis is based on knowledge associated with capacitance-voltage techniques. The collector curve, Fig. 15, shows a background concentration in the collector region of approximately 7×10^{15} atoms/cc, corresponding to the 2 ohm-cm material used for the units. It can be shown that the slope of the impurity profile (Sj) at the junction is four times the asymptotic slope through zero on the concentration curves. An approximation for the concentration peak in the base region was made on Fig. 16. The depletion layer widths, Fig. 17, are for relative comparison of units at the reference points indicated on Figs. 15 and 16. The linear scale for Fig. 17 shows equal depletion areas on both sides of the junction.

E. CUTOFF FREQUENCY

The measured cutoff frequency, f_T, is approximately 800 megacycles. The proposed value for f_T was considerably higher, approximately 2000 megacycles. Previous calculations of f_T based on the base transit time ($\tau_b = \frac{1}{2\pi f_T}$) agree well with the measured values of cutoff frequency. Therefore, the low f_T and high τ_b are direct

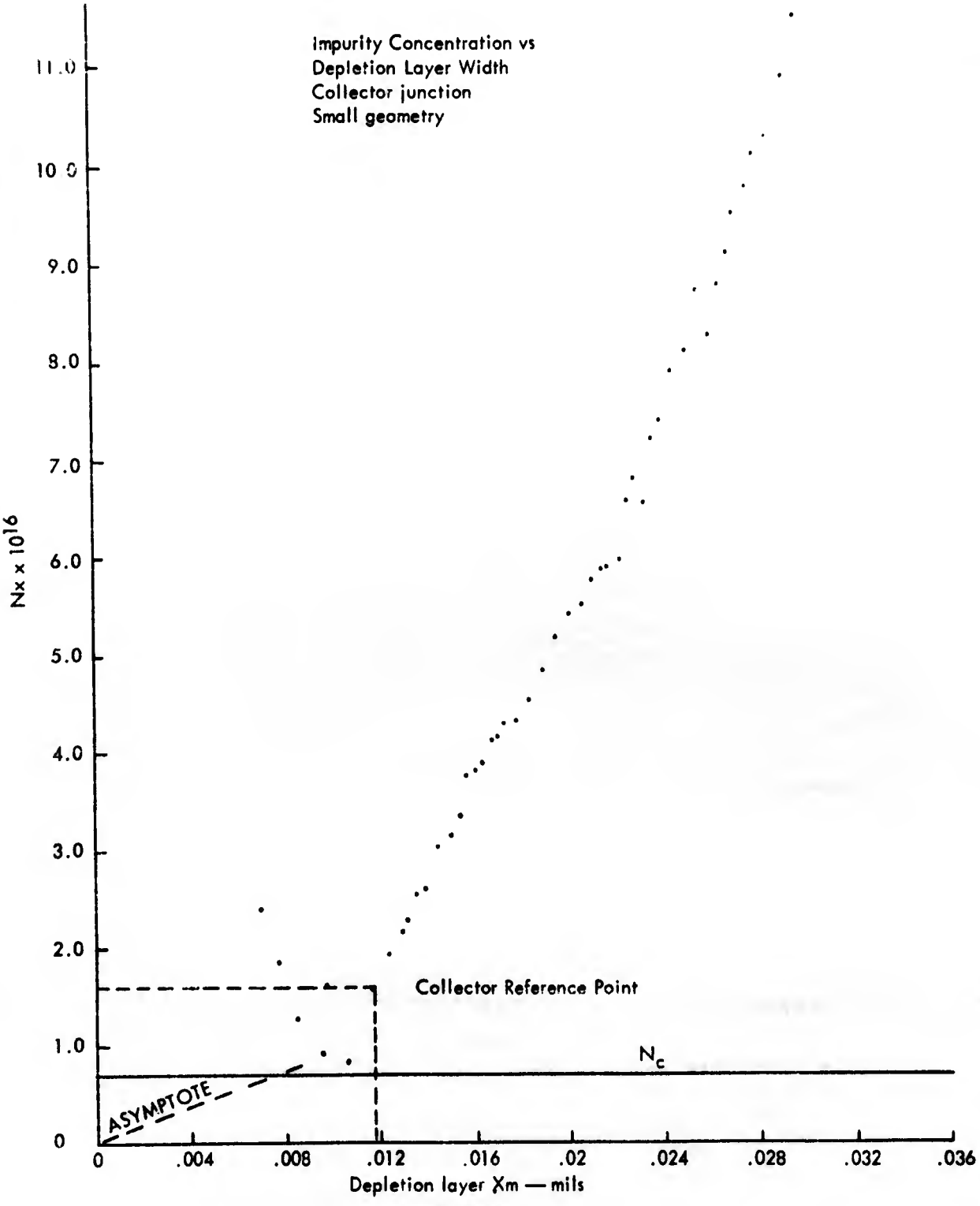

Impurity Concentration vs
Depletion Layer Width
Collector junction
Small geometry
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
Nx x 10^16
Collector Reference Point
N_c
ASYMPTOTE
0
.004
.008
.012
.016
.02
.024
.028
.032
.036
Depletion layer Xm — mils

FIGURE 15

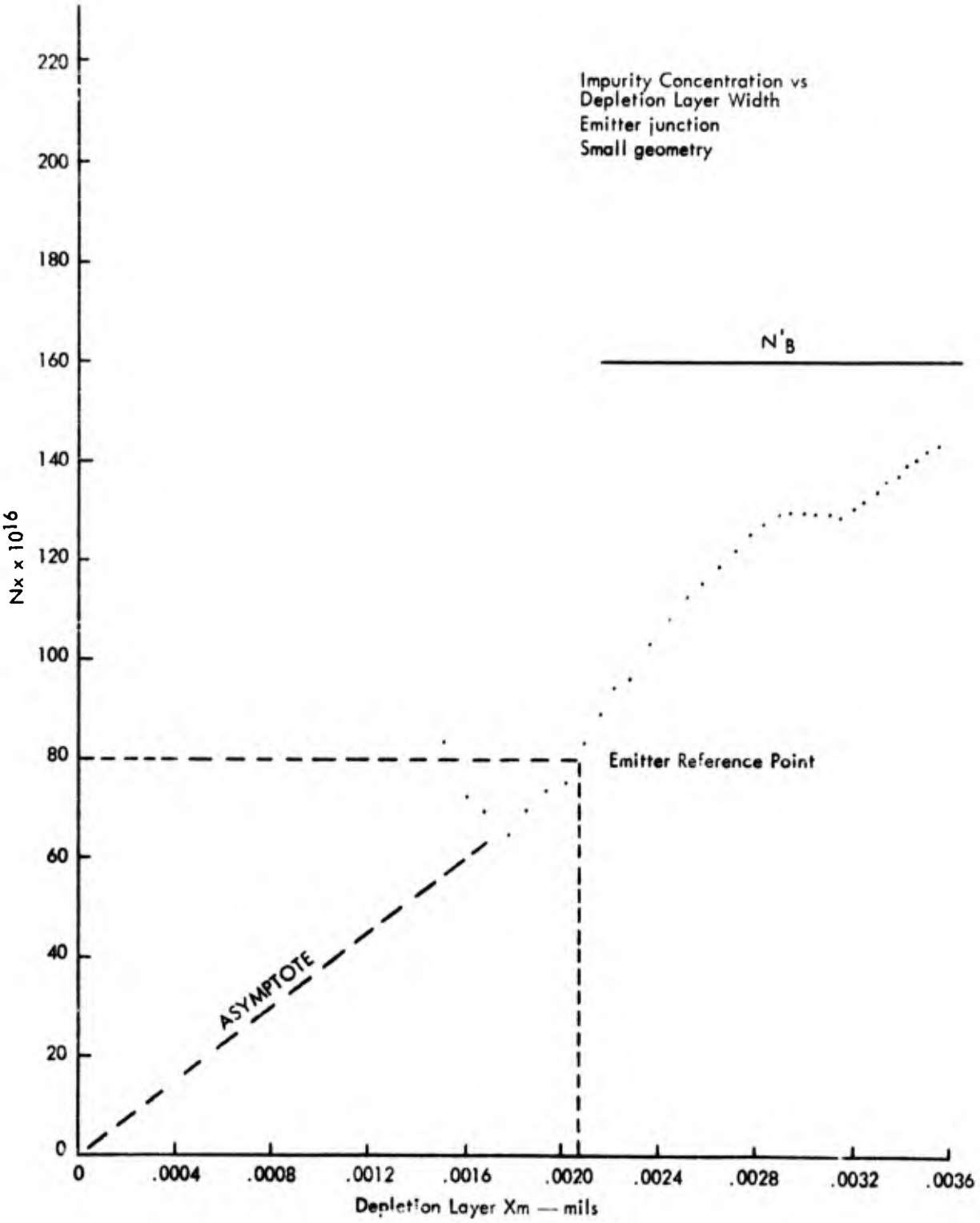

Impurity Concentration vs
Depletion Layer Width
Emitter junction
Small geometry
N'B
Nx x 10^16
220
200
180
160
140
120
100
80
60
40
20
0
Emitter Reference Point
ASYMPTOTE
0
.0004
.0008
.0012
.0016
.0020
.0024
.0028
.0032
.0036
Depletion Layer Xm — mils

FIGURE 16

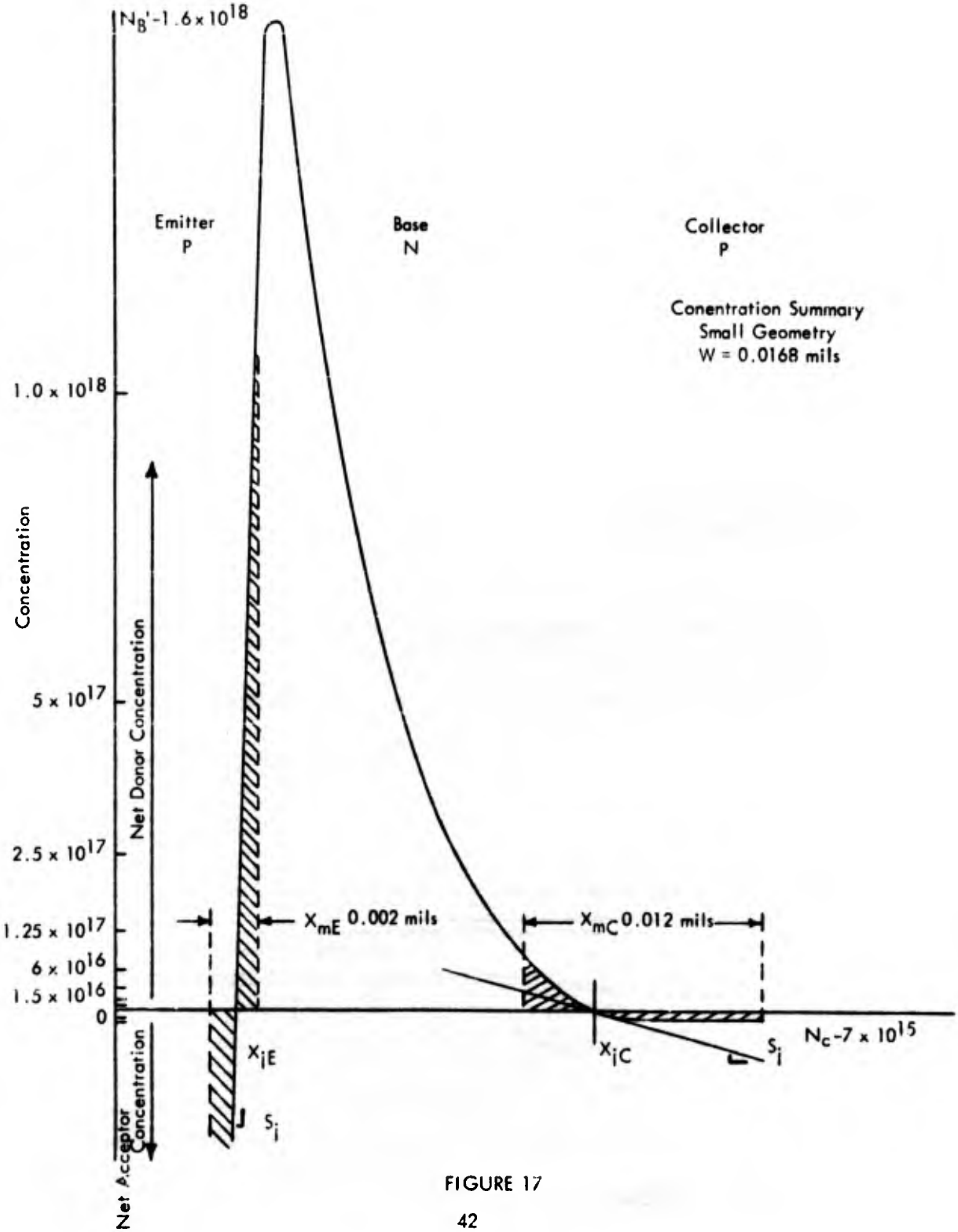

N_B'-1.6 x 10^{18}
Emitter
P
Base
N
Collector
P
Conentration Summary
Small Geometry
W = 0.0168 mils
1.0 x 10^{18}
5 x 10^{17}
2.5 x 10^{17}
1.25 x 10^{17}
6 x 10^{16}
1.5 x 10^{16}
0
Concentration
Net Donor Concentration
Net Acceptor Concentration
X_{mE} 0.002 mils
X_{mC} 0.012 mils
X_{jE}
X_{jC}
S_i
S_i
N_c-7 x 10^{15}

FIGURE 17

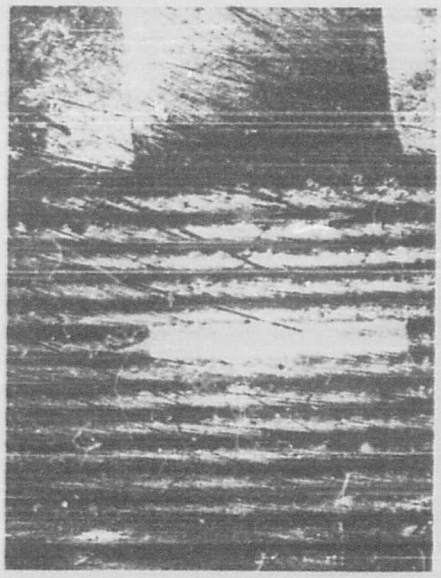


Fig. 18 Diffusion Cross Section

results of the base region being wider than the original design objective.

It is interesting to consider the time delays directly involved with the cutoff frequency. The cutoff frequency $\frac{1}{\omega_T}$ consists of four time delays as follows:[4]

$$\frac{1}{\omega_T} = \frac{1}{\omega_e} + \frac{1}{\omega_b} + \frac{1}{\omega_d} + \frac{1}{\omega_c}$$

where

$\frac{1}{\omega_e} = r_e C_{TE}$, the emitter charging time constant;

$\frac{1}{\omega_e} = \frac{W^2}{2KD_{pb}}$, the base transit time;

$\frac{1}{\omega_d} = \frac{x_m}{2v_{sc}}$, the collector depletion-layer transit time;

$\frac{1}{\omega_c} = (r_{SE} + r_e + r_{sc})\, C_{TC}$, the collector charging time constant.

Figures 19 and 20 show $|h_{fe}|$ vs V_{CB} and I_C, respectively, for a typical unit with a base transit time of 160 psec. It should be noted that the curves for $|h_{fe}|$ vs I_C are relatively flat except when the voltage is below 1.0 volt which indicates that the base width is near its maximum width at this voltage or, in other words, the base transit time is large.

The emitter time delay, $\frac{1}{\omega_e}$, is determined by the emitter resistance and emitter transition capacitance and was calculated in the third quarterly report to be approximately 6.7×10^{-12} seconds. Its effect upon f_T is seen in Fig. 19. At low currents, (below 3 ma in this device) f_T decreases with decreasing current due to the increasing emitter resistance:

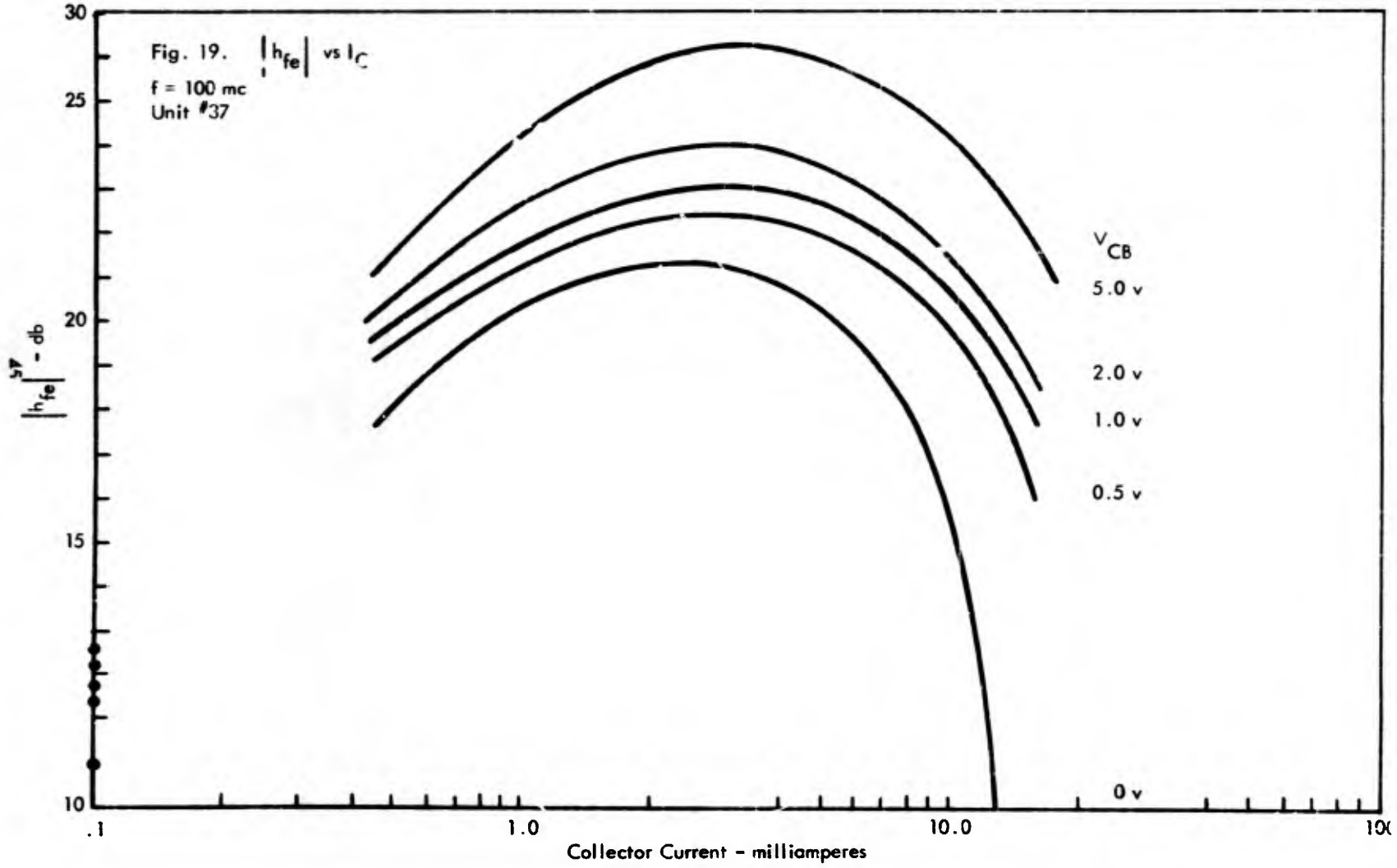
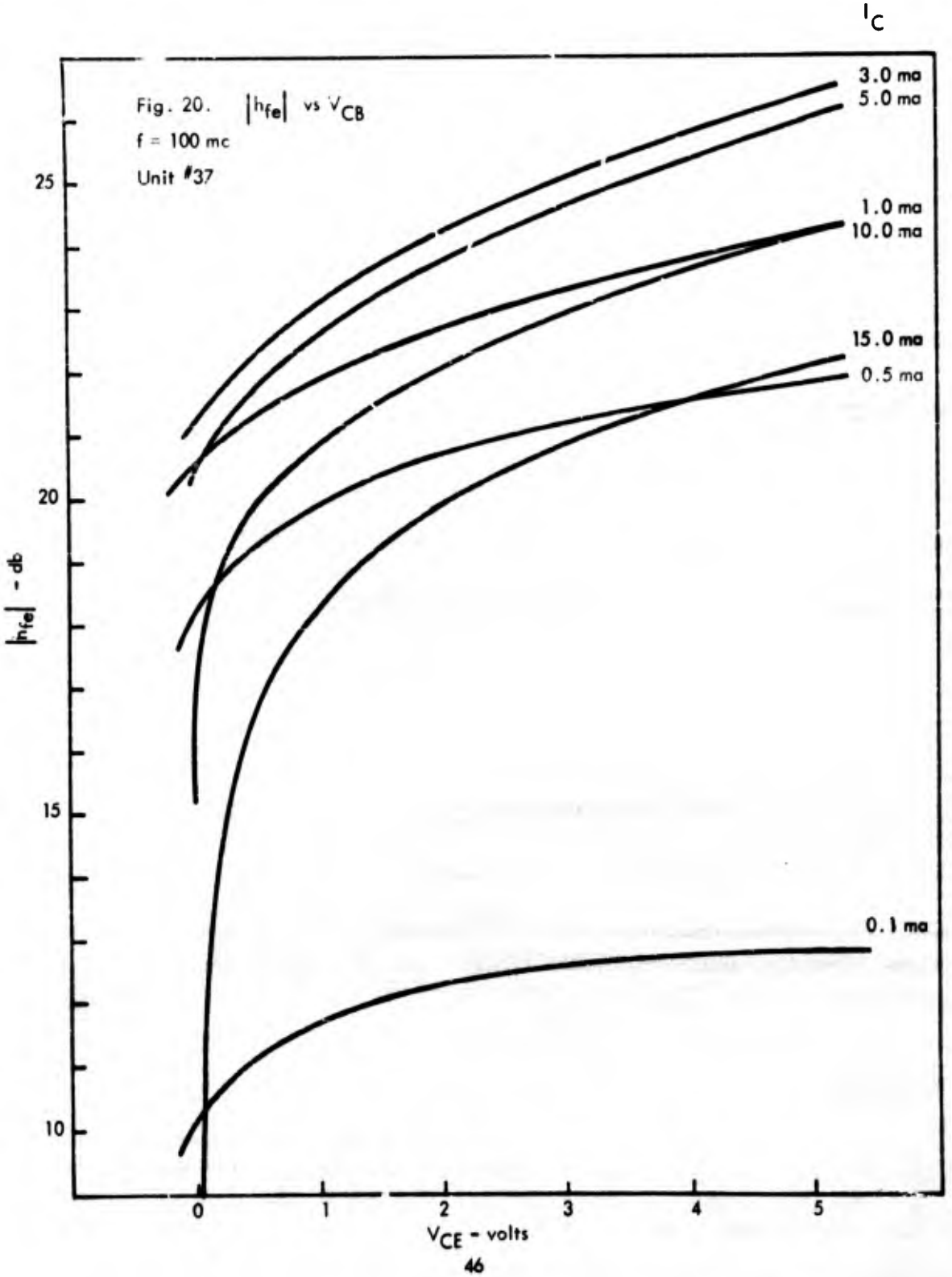


Fig. 19. $|h_{fe}|$ vs I_C
f = 100 mc
Unit #37
$|h_{fe}|^{37}$ - db
30
25
20
15
10
.1
1.0
10.0
Collector Current - milliamperes
V_{CB}
5.0 v
2.0 v
1.0 v
0.5 v
0 v


I_C
Fig. 20. $|h_{fe}|$ vs V_{CB}
f = 100 mc
Unit #37
3.0 ma
5.0 ma
1.0 ma
10.0 ma
15.0 ma
0.5 ma
0.1 ma
25
20
15
10
$|h_{fe}|$ - db
0
1
2
3
4
5
V_{CE} - volts

$$r_e = \frac{kT}{qI_E} .$$

The collector depletion-layer transit time, $\frac{1}{\omega_d}$, was calculated to be 1.9×10^{-12} seconds[3] and has a very slight effect on f_T. In fact, at $V_{CB} = 5$ v no decrease in f_T is noted. Refer to Fig. 19.

The collector time delay, $\frac{1}{\omega_c}$, is minimized by choosing the epitaxial layer resistance and width to minimize r_{sc} which is the most significant part of $\frac{1}{\omega_c}$. Also, a low value of r_{sc} will minimize $V_{CE(sat)}$. This will be discussed in the following section.

It is important to note that by thinning the base width, a significant reduction can be effected in the base transit time, greatly increasing the frequency response.

F. SATURATION VOLTAGE

The measured saturation voltage, $V_{CE(sat)}$, is 0.35 at $I_C = 10$ ma and $I_B = 1$ ma. This is seven times greater than the desired value of 0.05 volts.

An accurate prediction of $V_{CE(sat)}$ is prevented by the uncertainty associated with conductivity modulation and nonuniform injection from the emitter.[9] However, $V_{CE(sat)}$ consists of a component due to the collector resistance and a component due to transistor action. The former component contributes the most at currents greater than 1 ma. The collector resistance is described by the following equation:

$$r_{sc} = \frac{\rho_c l}{A}$$

where l is the collector epitaxial width and A is the device collector area.

It was reported[2] that with the use of the large geometry, a saturation voltage of 0.1 v at $I_C = 10$ ma was obtained. For the same collector epitaxial resistivity and

width, a reduction in emitter area to approximately 1/3 increases the r_{sc} by a factor of 3 and consequently increases $V_{CE(sat)}$. The small geometry devices exhibited $V_{CE(sat)}$ values of 0.3 v. An attempt to reduce $V_{CE(sat)}$ was made by reducing the epitaxial layer width and by proper control of ρ_c through the diffusion cycle. The second quarterly report presented epitaxial film data such as in Table 1 showing the effect of the diffusion cycle upon collector resistivity and thickness. Using this data, a collector resistance, r_{sc}, of 35 ohms is calculated which agrees well with the data in Table 2 and Fig. 21. Figure 22 shows a detailed view of $V_{CE(sat)}$ at low currents. Note that below 1 ma, the component of $V_{CE(sat)}$ due to collector series resistance is negligible. Also note that $V_{CE(sat)}$ starts to increase at very low currents due to h_{FE} decreasing.

Further reduction of collector resistivity and thickness would reduce the breakdowns further and a compromise has already been made by their initial reduction. The epitaxial layer thickness also has been limited by the need for an N+ diffusion which adds to the total up-diffusion time of the substrate. It has already been noted that gold diffusion which would control the lifetime, would also greatly increase $V_{CE(sat)}$. Figure 23 shows measurements of $V_{CE(sat)}$ at various current levels for a forced beta of 10. With reference to Fig. 21, it is noted that $V_{CE(sat)}$ is affected by the collector series resistance when the collector current reaches 1 ma and that at 5 ma, the value of $V_{CE(sat)}$ is comparable to that at 10 ma for most NPN switches.

In order to reduce the collector resistance, a substrate of 0.007 ohm-cm instead of the 0.06 ohm-cm which is used was considered. Assuming a total diffusion process time of 4.5 hours with 5 separate diffusion steps, an approximation can be made to determine the change of epitaxial layer thickness and the concentration during the process. The error function description for diffusion was used and is written as follows:[8, 10]

$$N_{(xt)} = \frac{N_1}{2}\left[1 - \operatorname{erf}\left(\frac{X}{2\sqrt{\Sigma Dt}}\right)\right] + \frac{N_2}{2}\left[1 + \operatorname{erf}\left(\frac{X}{2\sqrt{\Sigma Dt}}\right)\right]$$

where ΣDt is the sum of the diffusion steps and N_1 and N_2 are substrate and film

TABLE 1

EPITAXIAL FILM DATA

Material Specifications: 0.06 Ω-cm substrate
2.0 Ω-cm film

X	$\frac{N_1}{2}$ (1-erf Z)	$\frac{N_2}{2}$ (1 + erf Z)	N(x, t)	ohm-cm
1 μ	3.270×10^{17}	4.874×10^{15}	3.319×10^{17}	0.13
2 μ	1.363×10^{17}	5.939×10^{15}	1.422×10^{17}	0.23
3 μ	4.176×10^{16}	4.467×10^{15}	4.823×10^{16}	0.45
4 μ	9.36×10^{15}	6.648×10^{15}	1.601×10^{16}	1.1
5 μ	1.50×10^{11}	6.692×10^{15}	6.692×10^{15}	2.0

TABLE 2

SATURATION VOLTAGE DATA

Forced Beta = 10

Unit No.	Collector Current					
	50 μa	100 μa	1 ma	3 ma	5 ma	10 ma
	Units = Volts					
25	0.12	0.11	0.11	0.16	0.22	0.39
26	0.12	0.10	0.10	0.15	0.20	0.35
37	0.11	0.09	0.08	0.13	0.17	0.29
42	0.12	0.10	0.09	0.13	0.18	0.31

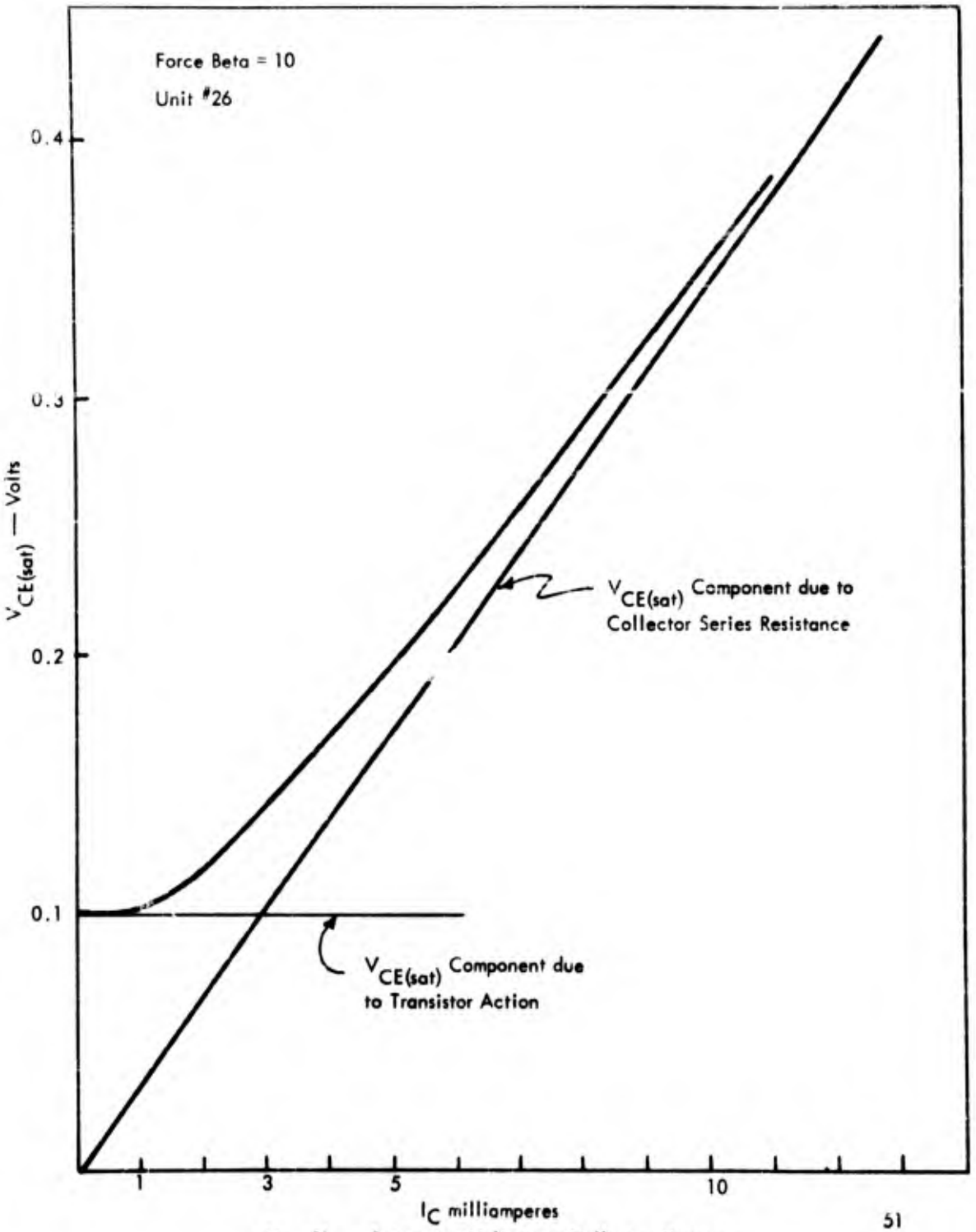


Fig. 21. Saturation Voltage vs Collector Current

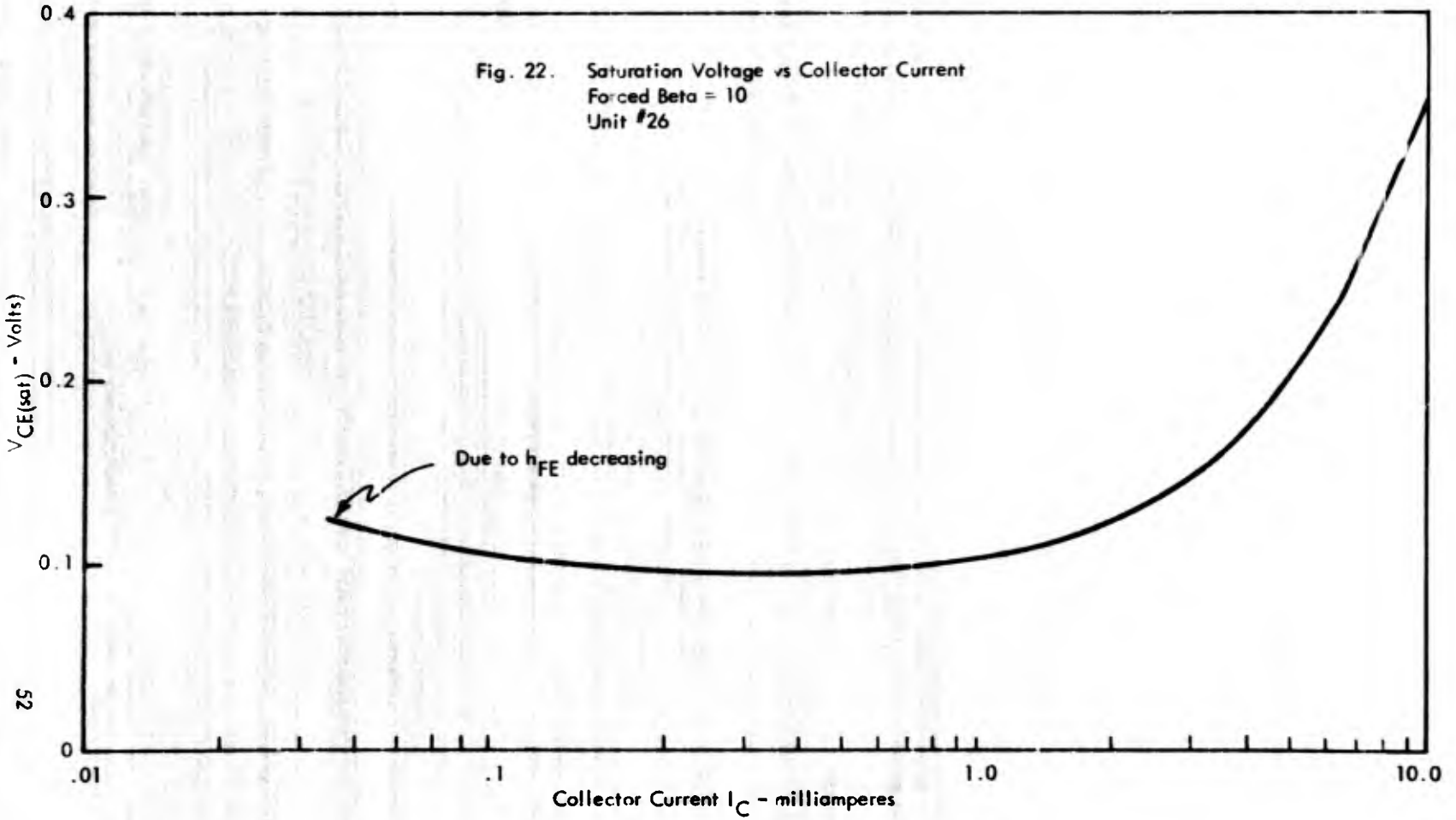
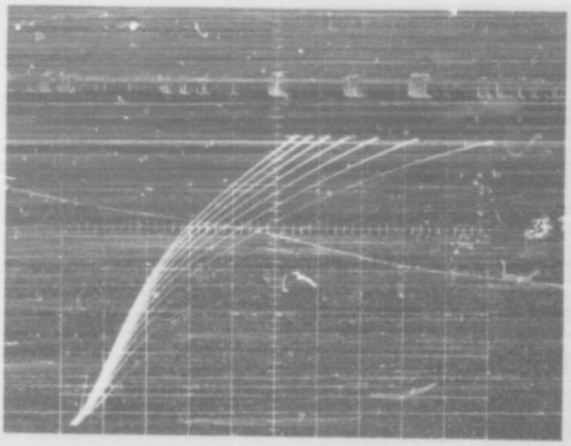
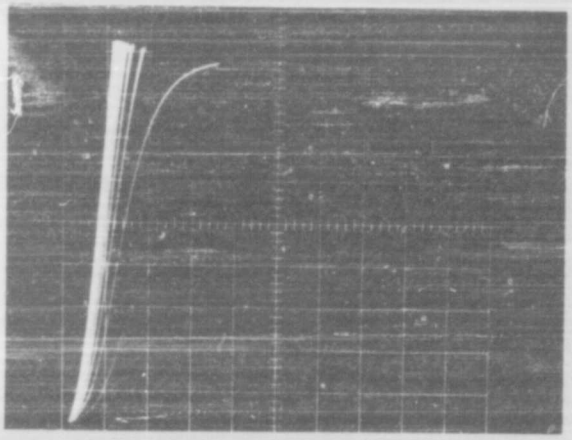


Fig. 22. Saturation Voltage vs Collector Current
Forced Beta = 10
Unit #26

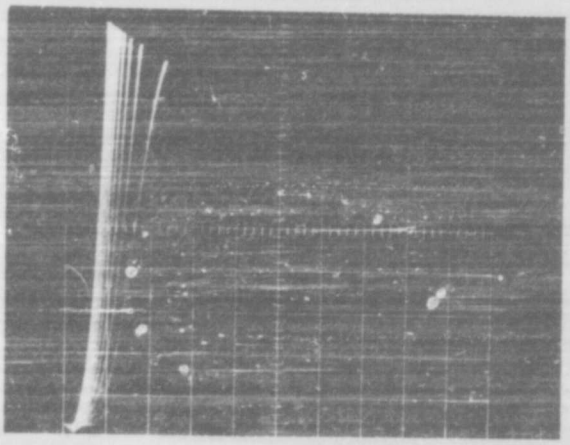
Fig. 23. Saturation Voltage Measurements
Forced Beta = 10



$V_{CE(sat)}$ = 0.3 volts
Ordinate: I_C, 2 ma/cm
Abscissa: V_{CE}, 0.1 v/cm
I_B, 0.1 ma/step



$V_{CE(sat)}$ = 0.08 volts
Ordinate: I_C, 0.2 ma/cm
Abscissa: V_{CE}, 0.1 v/cm
I_B, 0.01 ma/step



$V_{CE(sat)}$ = 0.08 volts
Ordinate: I_C, 0.02 ma/cm
Abscissa: V_{CE}, 0.1 v/cm
I_B, 0.001 ma/step

impurity concentration respectively. From this calculation it was determined that the epitaxial layer would have to be considerably thicker, 8-10 μ, and therefore would not benefit the design of the shallow base unit.

Also, a reduction of $V_{CE(sat)}$ was attempted by the use of different preforms in the alloying step of the assembly process. The data in Table 3 indicate that no reduction was produced by the use of a different preform.

As reported in the second quarterly report, a 0.06 ohm-cm substrate, $N_1 = 1.2 \times 10^{18}$ atoms/cc, and a 2.0 ohm-cm epitaxial film, $N_2 = 6.7 \times 10^{15}$ atoms/cc, and an epitaxial layer thickness of 5 μ or more will satisfy the requirement of maintaining the design thickness and resistivity after diffusion and still provide compromised $V_{CE(sat)}$ and breakdown voltages.

G. LEAKAGE CURRENTS

The original collector-base and collector-emitter leakage current specification was ≤1 na at 35 v. This was subsequently modified to ≤1 na at 25 v. The emitter-base leakage was originally 1 na at 12 v, but was also modified to ≤ 1 na at 6 v. These leakage currents were not attained in developed units. These units meet the following specifications:

I_{CBO}	$V_{CB} = 15$ v	1.0 na d-c max
I_{CEO}	$V_{CE} = 10$ v	1.0 na d-c max
I_{EBO}	$V_{EB} = 4$ v	1.0 na d-c max

Leakage currents are highly surface dependent and consequently, the last quarter of the contract was primarily devoted to optimizing the surface conditions. Refer to Figs. 31, 34, and 35 and note the soft breakdowns.

TABLE 3

SATURATION VOLTAGE, PREFORM DATA

$V_{CE(sat)}$ at I_C = 10 ma, I_B = 1 ma, Units = Volts

Sample Unit No.	Preform			
	AuB	Au	AuGa	AuGe
1	1.50	0.70	0.40	0.64
2	0.50	0.70	1.00	0.48
3	0.64	0.42	1.00	1.00
4	0.48	0.42	0.9[illegible]	0.70
5	0.48	0.50	0.65	9.00
6	0.42	0.48	1.25	0.41

All samples were from Diffusion Run No. 80

Figures 15 and 16 indicate the presence of inversion layers by the sharp negative slope at narrow depletion layer width (low voltage) which has been noted on other transistors having inversion layers. The use of a guard ring has been effective in reducing leakage currents. The guard ring is diffused during the emitter step and is a P+ region around the base for preventing the formation inversion layers.

Early in the contract work a series of surface study experiments were conducted in order to investigate the leakage current and h_{FE} problems. Leakage currents were high, averaging 200 na, and h_{FE} was degraded upon the application of contacts at 200°C to the diffused units. The following circuit was used in determining h_{FE} and I_{CBO} values.

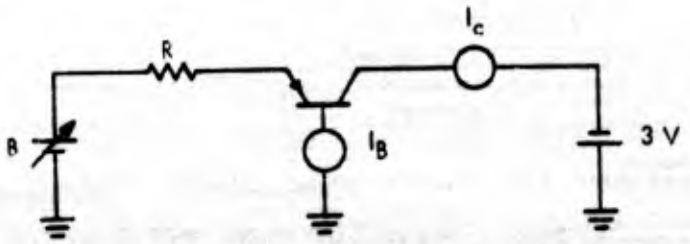


Fig. 24. Circuit for Surface Study

The devices were placed in a closed box in which the ambient temperature was measured and the appropriate environment was maintained. The following figure illustrates this arrangement.

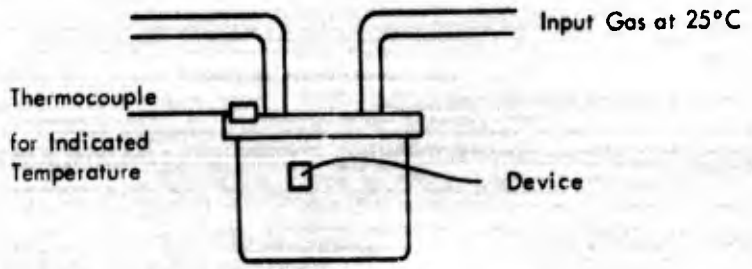


Fig. 25. Surface Study Apparatus

Measurements of I_{CBO} and h_{FE} were made following each of the surface study conditions.

Condition:

a. Original fabricated device in a sealed package (TO-18 header and can).
b. An opened package, i.e., TO-18 header exposed to environment at room temperature.
c. An opened package at room temperature in dry N_2.
d. An opened package at 200°C in dry N_2 for a period of 8 hours.
e. An opened package at room temperature in dry O_2 for 2 hours.
f. An opened package at 220°C in dry O_2 for 36 hours.
g. An opened package at 225°C in dry O_2 for 70 hours.

The results of measurements under these conditions show that the h_{FE} was not degraded at the temperatures involved. The leakage current, I_{CBO}, changed as indicated by the curves in Fig. 26.

Processed diffusion runs have resulted in random leakage current data and improvement was directed by controlled diffusion experiments. Pyrolytic oxide was placed on the units before contact evaporation and improved I_{CEO} substantially. Figure 27 shows the results of this experiment. Figures 28 and 29 indicate that no improvement in I_{CBO} or I_{EBO} occurred due to the deposition of pyrolytic oxide before contacts.

The major contribution to improved leakage currents, however, is due to controlled diffusion and contact procedures. Surface preparation at each step is essential and degradation of leakage current and h_{FE} results if proper control is not exhibited during the diffusion and contact steps. These steps are outlined in the specification section of this report.

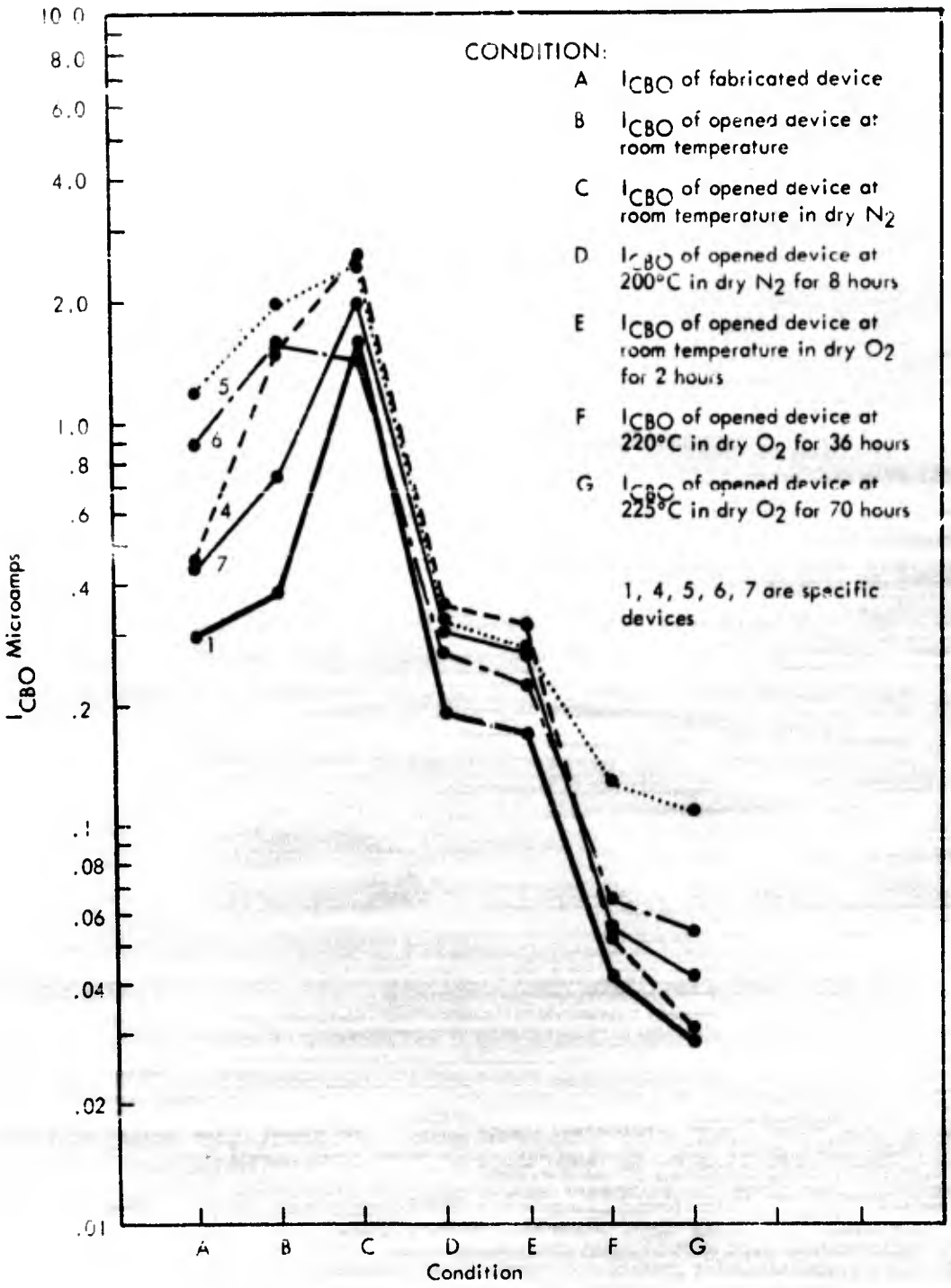
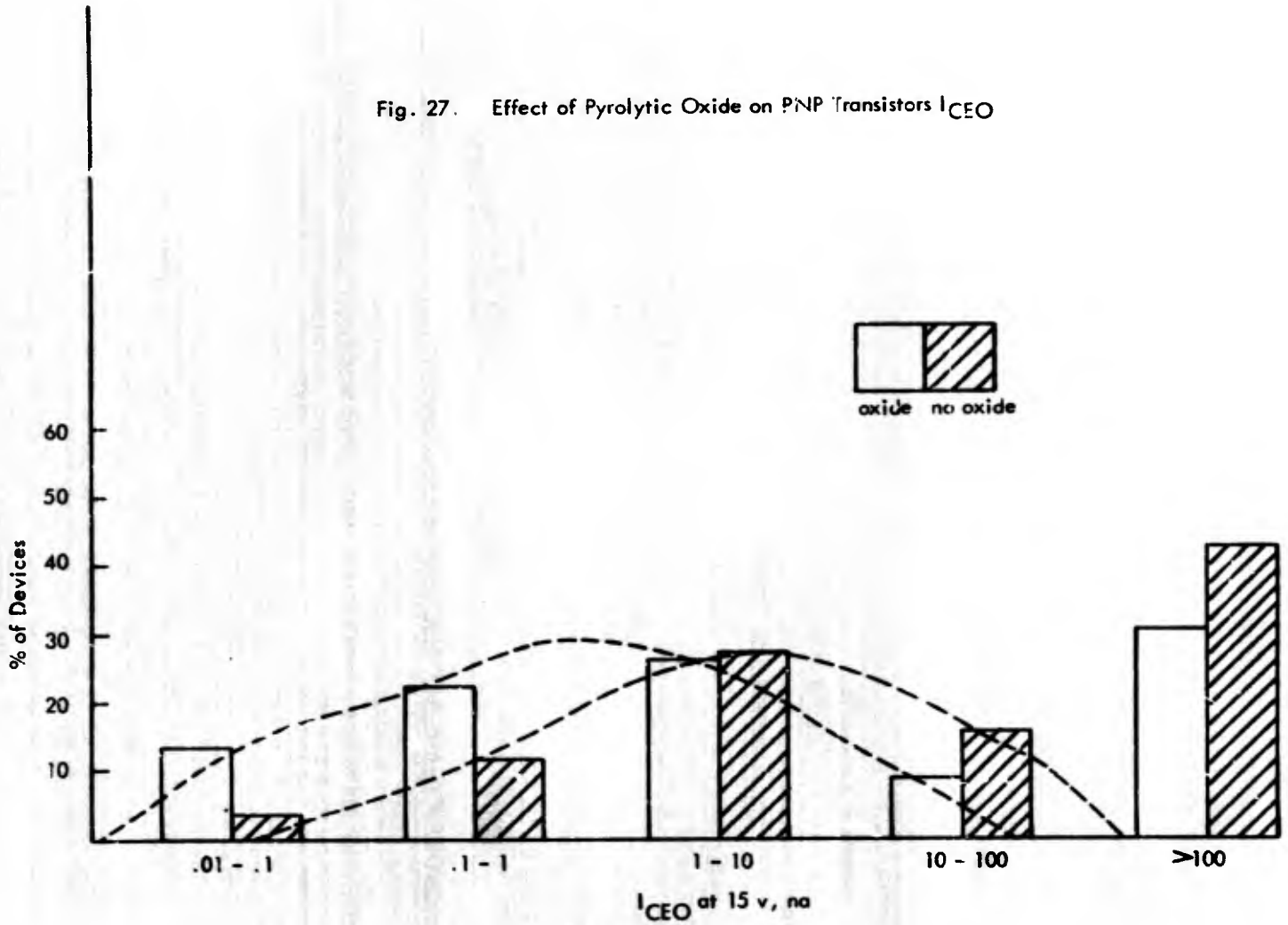


Fig. 26. Leakage Current I_{CBO} vs Surface Study Process

Fig. 27. Effect of Pyrolytic Oxide on PNP Transistors I_{CEO}



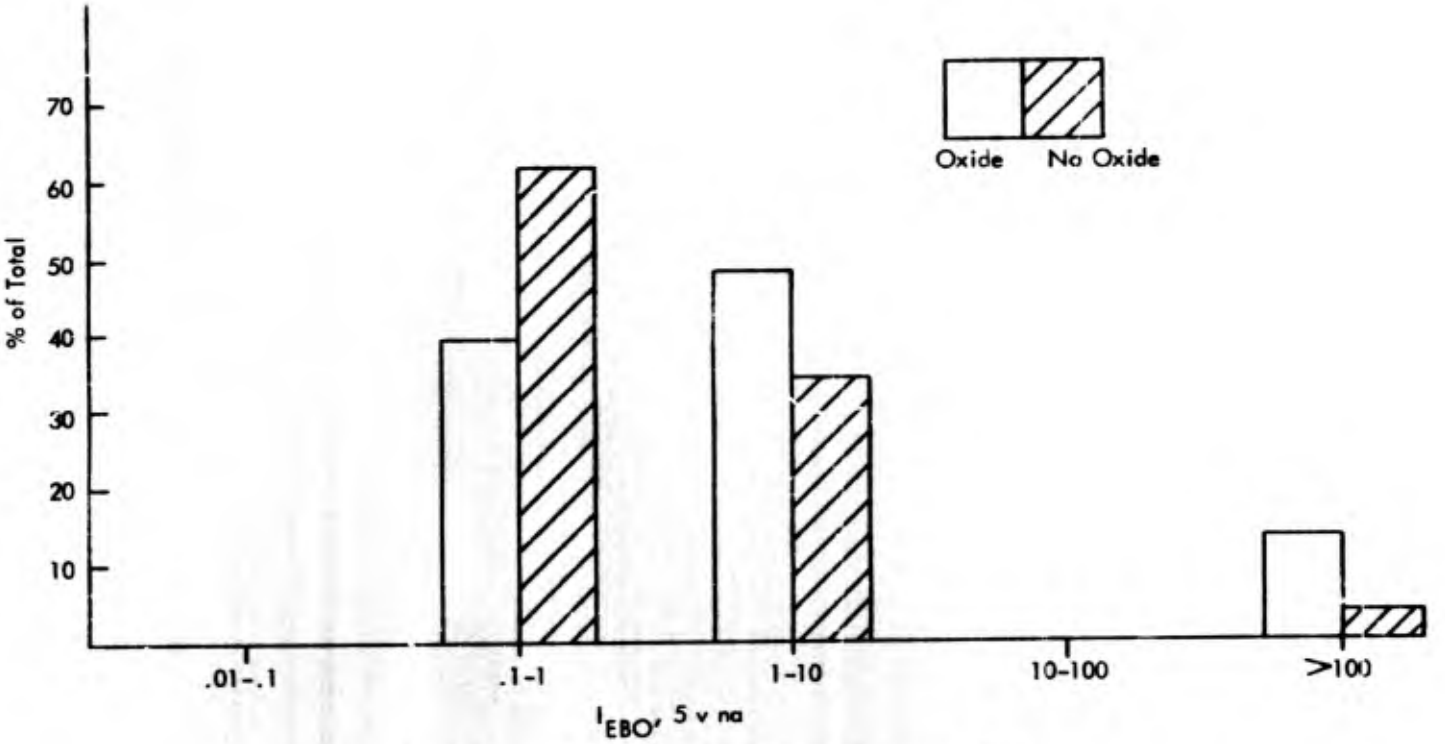


Fig. 28. Effect of Pyrolytic Oxide on PNP Transistors I_{CBO}

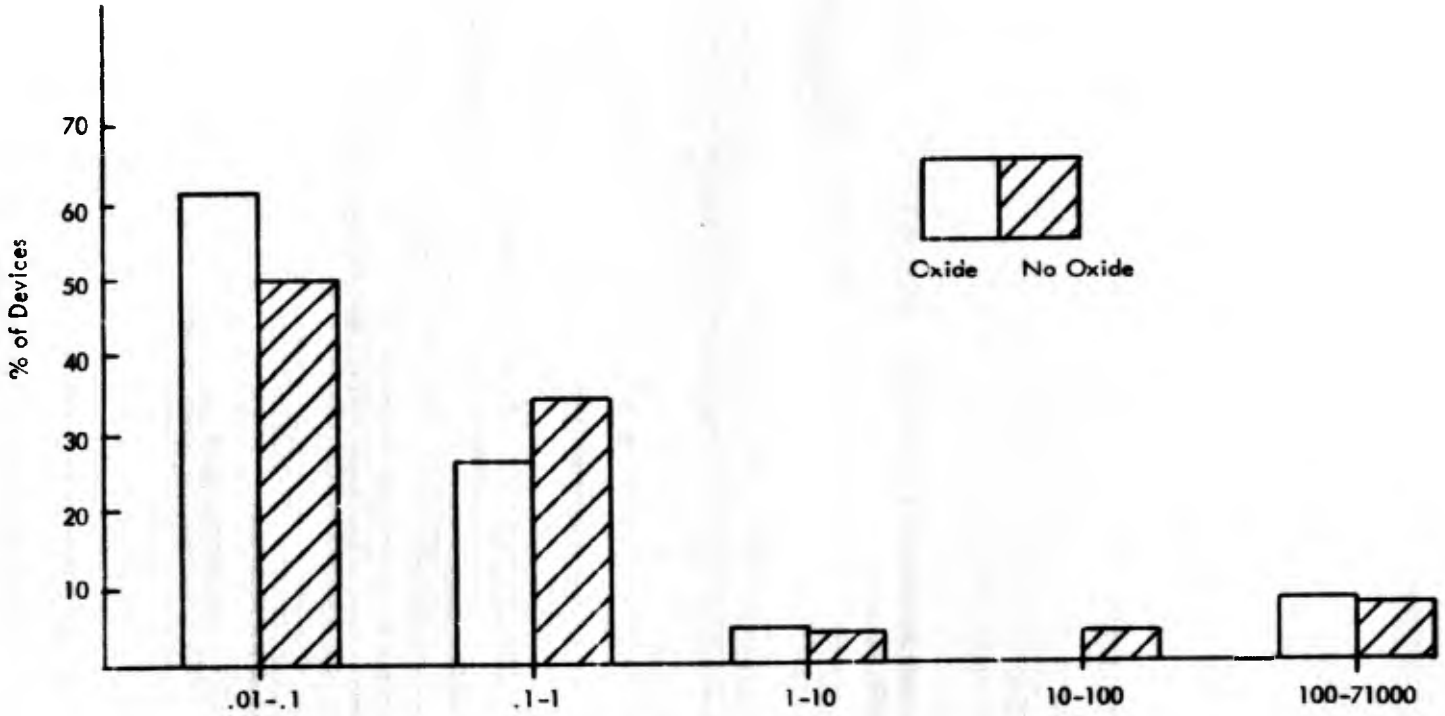


Fig. 29. Effect of Pyrolytic Oxide on PNP Transistors I_{EBO}

H. COLLECTOR-BASE BREAKDOWN VOLTAGE

The collector-base breakdown voltage was not specified in the contract. Since BV_{CBO} is an important design parameter, and is customarily given, the developed units have been specified at 20 v at 100 μa.

The first design was for a collector-base breakdown of 50 volts. The breakdown voltage of an epitaxial p+pn+ junction depends on the thickness as well as the resistivity of the P layer. Using charts available in literature,[11,12] a resistivity of 1.4 ohm-cm and an eptiaxial layer thickness of 0.12 mils are needed for a 50 volt breakdown. Refer to Fig. 30 for a summary of this information.

Figure 31 shows a typical collector-base breakdown of 22 volts at 100 μa. Note the relatively soft knee of the breakdown trace. Since the parameters, epitaxial layer thickness and impurity concentration, can be greatly altered by the diffusion sequence, BV_{CBO} was used as a measure of diffusion uniformity and control.

Collector-base breakdowns for small area units averaged the same as for large area units.

Data for units without the N+ base contact diffusion show that BV_{CBO} averages 45 volts; however, BV_{CBO} for units with the N+ base contact diffusion show a degradation to 25 volts. Figures 32 and 33 present this data.

The wide range of collector-base breakdown voltages is due to the shallow base. Extremely shallow diffusions are less likely to follow the error function relation for a semi-infinite solid[4,8] and more variation can be expected in the diffusion concentration profile.

I. COLLECTOR-EMITTER BREAKDOWN VOLTAGE

The collector-emitter breakdown is specified for the developed units by a minimum of 10 volts at 100 μa.

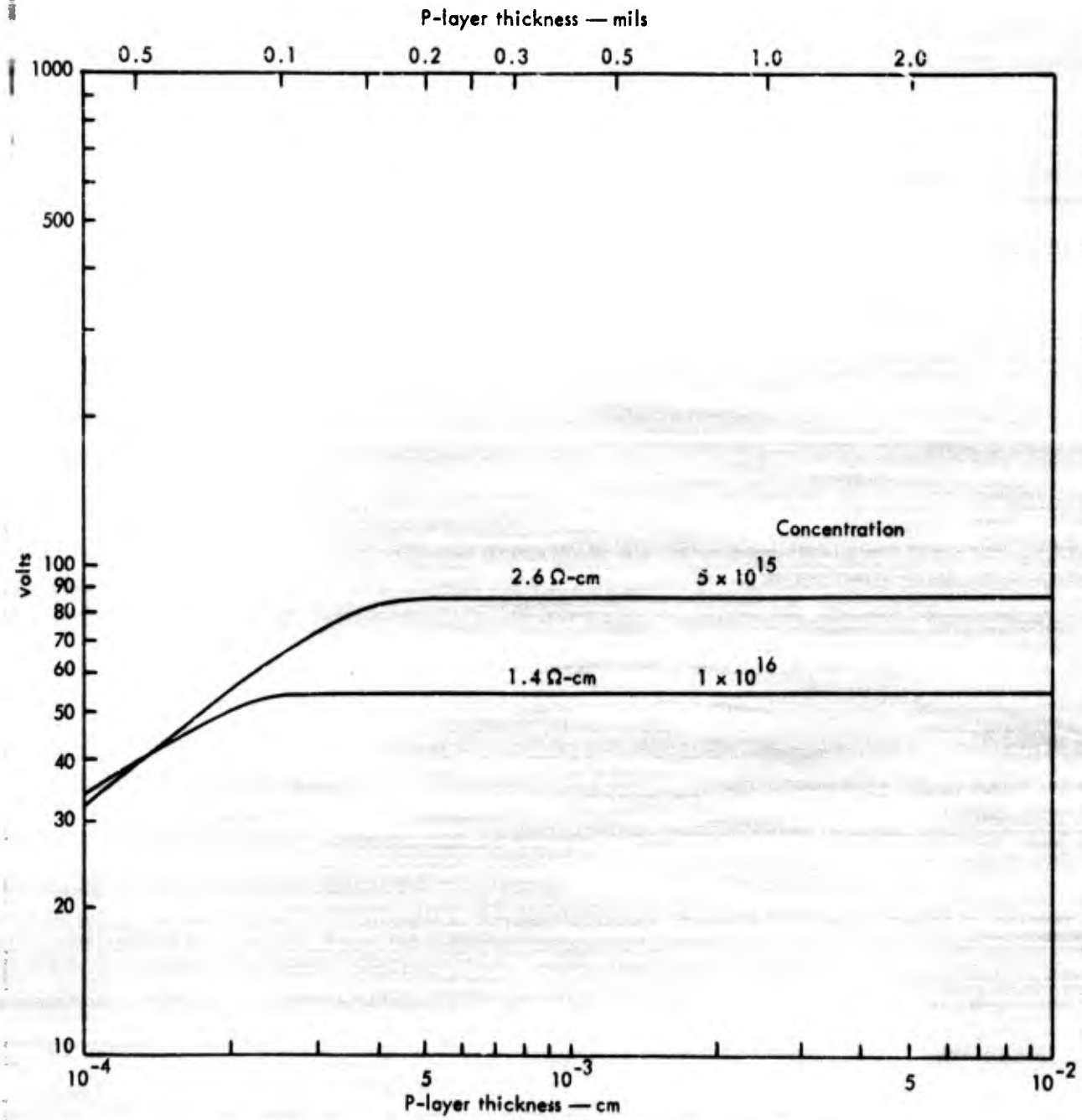
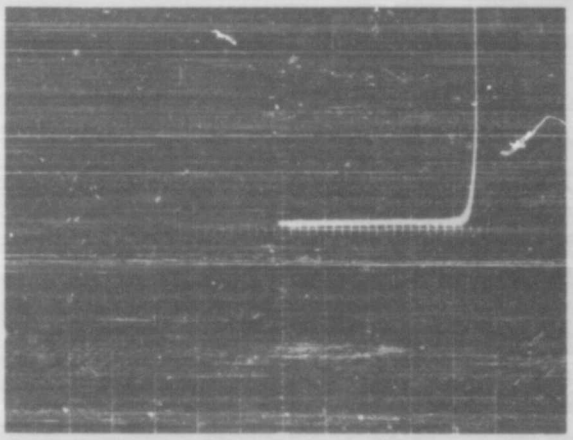


Fig. 30. Breakdown Voltage and Resistivity Summary n+pp+ Diodes



BV_{CBO} = 22 volts

Ordinate: 0.01 ma/cm

Abscissa: 5.0 v/cm

Fig. 31. Typical Collector-base Breakdown

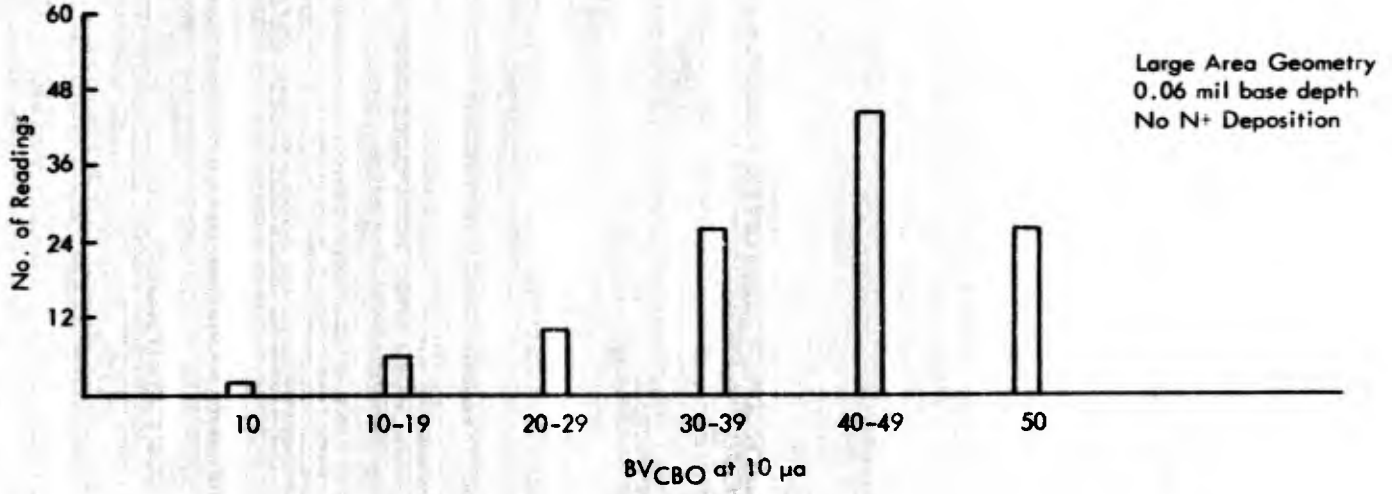

60
48
36
24
12
No. of Readings
10
10-19
20-29
30-39
40-49
50
BV_{CBO} at 10 μa
Large Area Geometry
0.06 mil base depth
No N+ Deposition

FIGURE 32

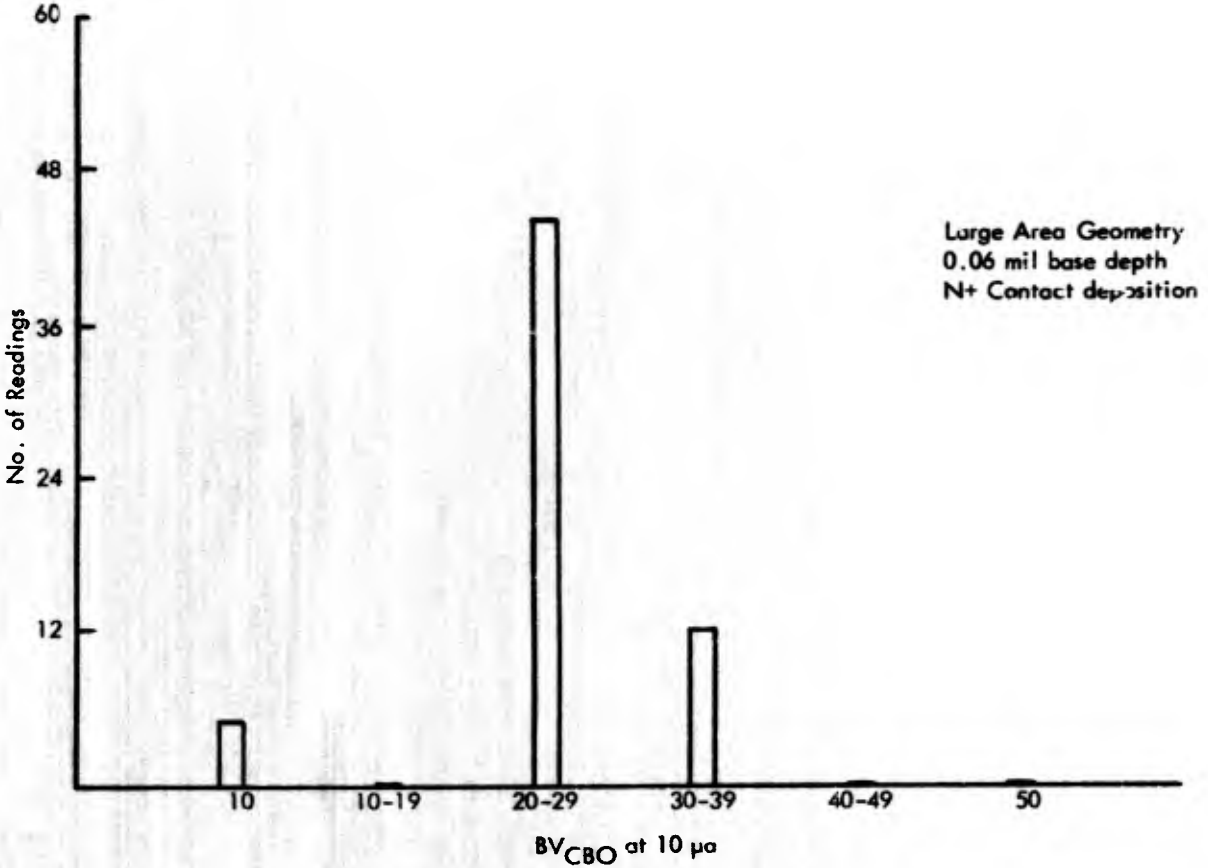

60
48
36
24
12
No. of Readings
Large Area Geometry
0.06 mil base depth
N+ Contact deposition
10
10-19
20-29
30-39
40-49
50
BVCBO at 10 μa

FIGURE 33

Previous experience indicates that BV_{CEO} of 25 volts and LV_{CES} of 20 volts at the specified currents can be obtained by designing for BV_{CBO} of 50 volts. Although the original design of BV_{CBO} was for 50 volts, the present collector-base breakdown is 25 volts. Consequently, BV_{CEO} averages 15 volts due to current gain and leakage current considerations. Figure 34 shows a typical collector-emitter breakdown. Also, note the relatively soft knee of the breakdown trace.

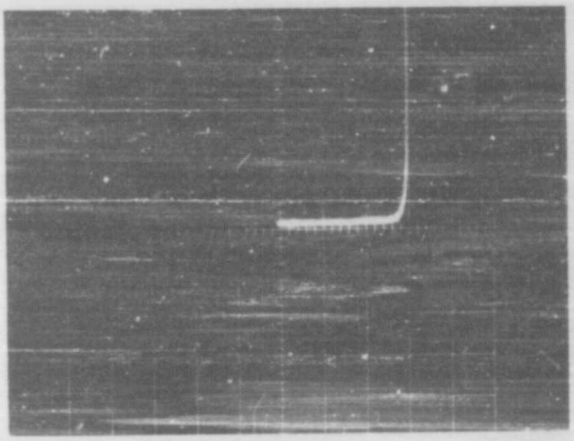
In addition to the above requirements for BV_{CBO} and BV_{CEO}, the base doping must be sufficient to insure that the punch through voltage, V_{PT}, is greater than the desired BV_{CEO}. If the base impurity profile is known, V_{PT} can be calculated. For the type of diffusion used, however, V_{PT} can only be estimated on the basis of previous results with similar devices. The base impurity concentration will vary directly with the base width and inversely with total base diffusion depth if the base surface concentration is held constant. Experience indicates that, for the base surface concentration of 10^{18} atoms/cc, the ratio of total base depth to base width should be 3/1 or less. For a base width of 0.02 mils, this requires a base depth of 0.06 mils or less (about 5 sodium interference lines; refer to Fig. 18). The sustaining voltage is 25 volts which meets the specified minimum value of 20 volts.

J. EMITTER-BASE BREAKDOWN VOLTAGE

The emitter-base breakdown voltage, BV_{EBO}, of the developed units is 6.4 volts at 100 μa. Refer to Fig. 35 for a typical BV_{EBO} trace.

The emitter-base breakdown is that of a p+n junction with n impurity concentration equal to that at the base surface. The base surface concentration for BV_{EBO} = 6 volts is about 10^{18} atoms/cc.

It is interesting to note that emitter-base breakdowns of 10 volts or greater were obtained at the start of the contract. This requires a base concentration of less than 10^{18} atoms/cc which is easily attained, but does not provide for adequate contact to be made to the device. Therefore, because of the inability to make adequate contact

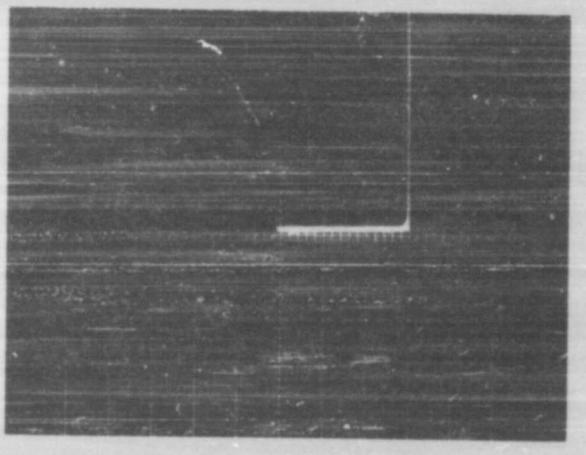


BV_{CEO} = 15 volts

Ordinate: 0.01 ma/cm

Abscissa: 5.0 v/cm

Fig. 34. Typical Collector-emitter Breakdown



$BV_{EBO} = 6.0$ v

Ordinate: 0.01 ma/cm

Abscissa: 2.0 v/cm

Fig. 35. Typical Emitter-base Breakdown

to a unit which has an emitter-base breakdown of 12 volts (base surface concentration of 10^{17} atoms/cc) and a very shallow base diffusion depth, the emitter-base breakdown was changed to 6 volts.

K. CURRENT GAIN

The current gain, h_{FE}, at $V_{CE} = 0.5$ v and $I_C = 10$ ma is 15. This is considerably less than the expected value of 40. However, this low h_{FE} at 10 ma is due to the fact that $V_{CE(sat)}$ is 0.35 v at 10 ma. Figure 36 indicates that h_{FE} falls off by a factor of two between 5 and 10 ma collector currents and 0.5 volts. At higher voltage this fall off is less than 20 per cent which is common for most switching transistors. Figure 37 presents h_{FE} as a function of collector voltage and shows the severe degradation of h_{FE} at collector currents above 4.0 ma at low voltage.

Figure 38 shows characteristic curves for various collector currents. The effect of $V_{CE(sat)}$ at 10 ma is apparent.

Since the $V_{CE(sat)}$ is high at 10 ma, it is reasonable to specify current gain at 1 volt and 10 ma. The h_{FE} at 1 volt and 10 ma averages 30 and this value was used for switching time calculations. It should be noted that both $|h_{fe}|$ and h_{FE} peak about 3 ma.

The current gain depends primarily on emitter injection efficiency and on surface conditions at the emitter base junction.[13,14,15] To improve the surface conditions, bakeouts at 400°C were used before and after contacts and increased h_{FE} by at least a factor of two. Bakeouts were performed in an atmosphere of N_2 and were effective within a period of 16 hours and with a gas flow rate of 2 liters per minute.

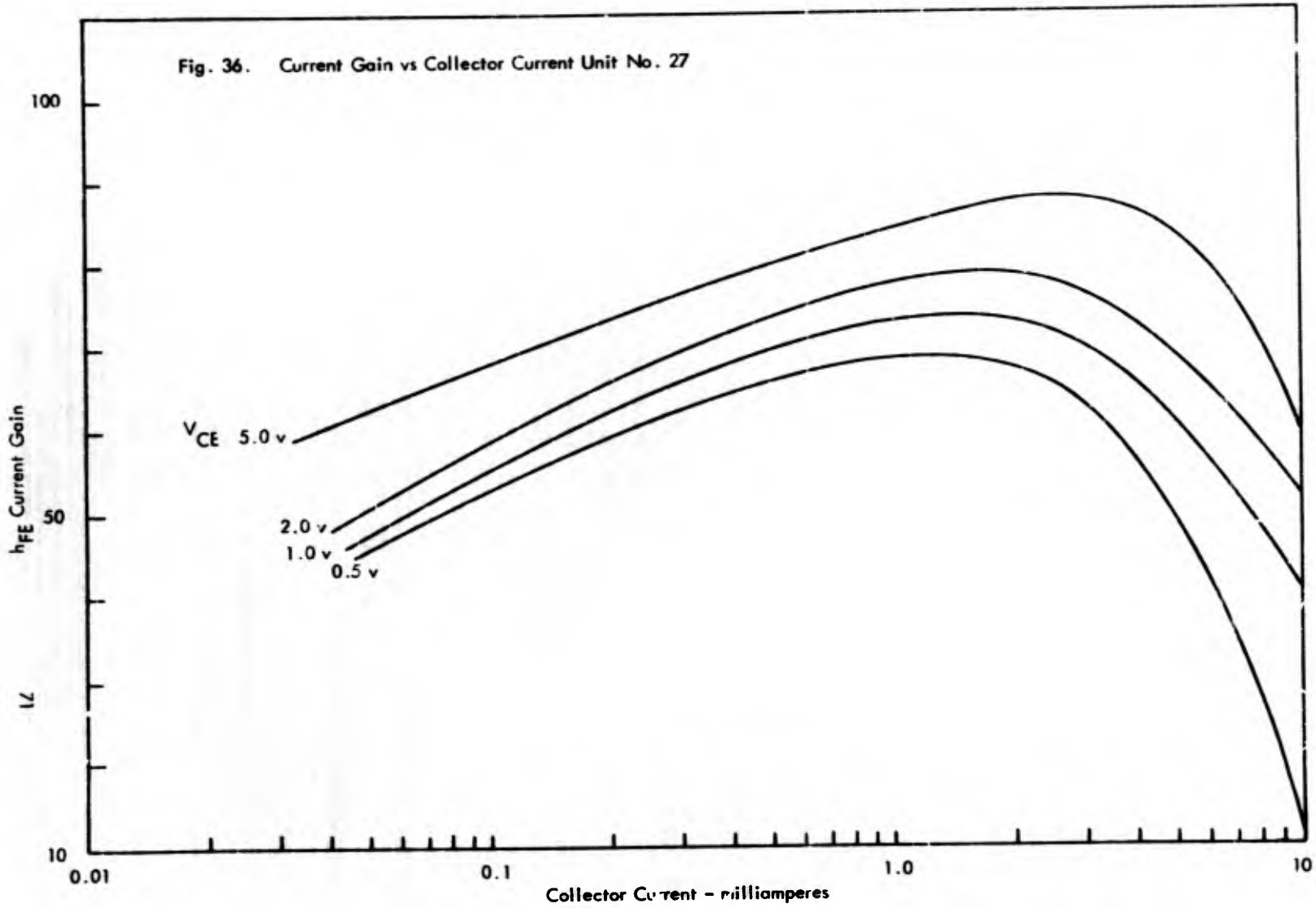


Fig. 36. Current Gain vs Collector Current Unit No. 27

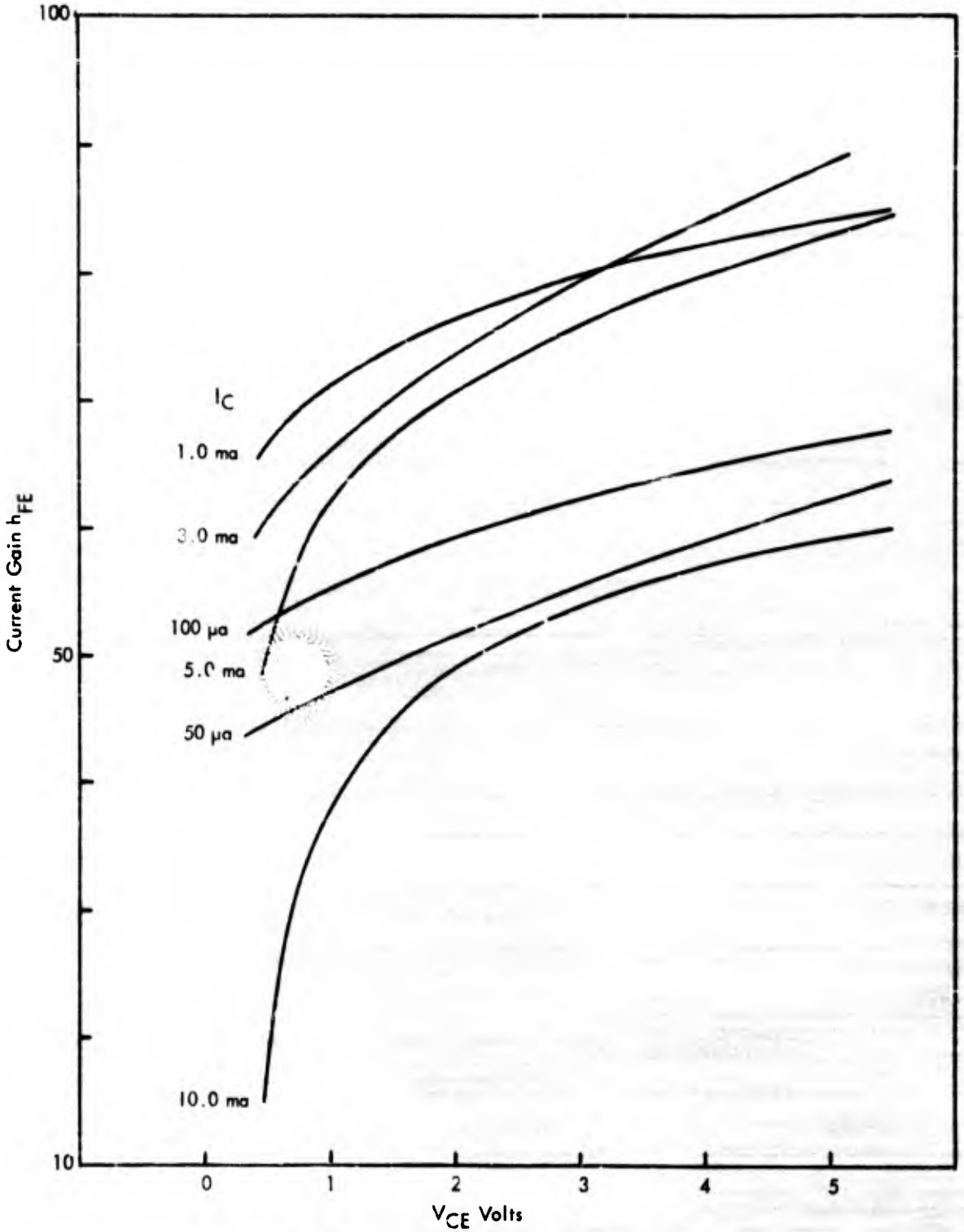
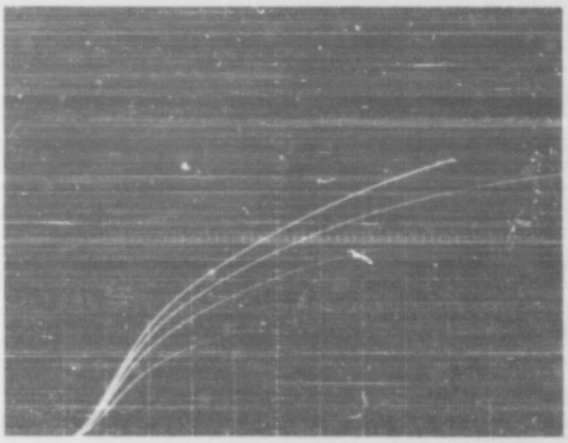
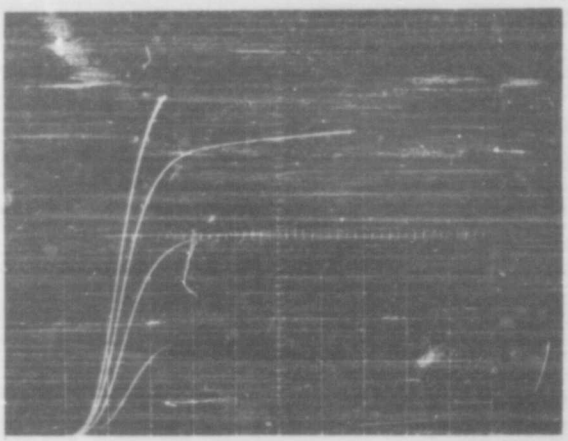


Fig. 37. Current Gain vs Collector Voltage

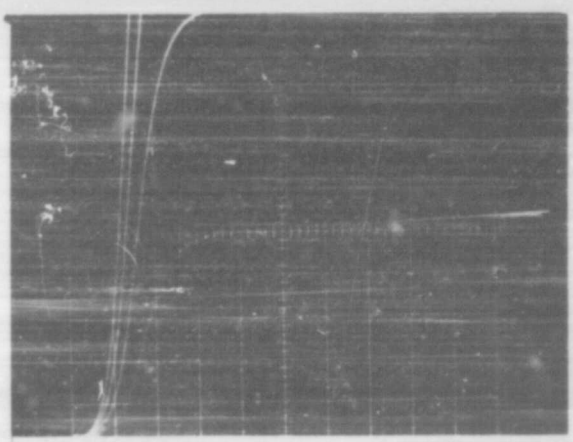
Fig. 38. Current Gain Measurements



h_{FE} = 25
at I_C = 10 ma, V_{CE} = 0.5 v
Ordinate: 2.0 ma/cm
Abscissa: 0.1 v/cm
I_B 0.1 ma/step



h_{FE} = 100
at I_C = 1 ma, V_{CE} = 0.5 v
Ordinate: 0.2 ma/cm
Abscissa: 0.1 v/cm
I_B 0.005 ma/step



h_{FE} = 100
at I_C = 0.1 ma, V_{CE} = 0.5 v
Ordinate: 0.02 ma/cm
Abscissa: 0.1 v/cm
I_B 0.001 ma/step

SECTION II
EPITAXIAL MATERIAL

Material for the high speed switching transistor requires a high resistivity collector region as well as low series resistance in the collector. Collector resistivity is important in saturation current, $V_{CE(sat)}$, and collector breakdown voltage, BV_{CBO}. Collector thickness determines the breakdown voltage if the collector-base junction depletes thru the layer, and collector thickness is an important factor in the series resistance of the collector, r_{sc}. Highly controlled epitaxial pon p+ is required to control the resistivity, thickness, and series resistance of the collector.

Epitaxial material was tailored to the diffusion process for optimum device performance. Impurity transport by diffusion from the heavily doped substrate into the deposited thin film occurs as a result of high temperature steps in the processing of a device. Collector resistivity and thickness are modified by impurity diffusion in the process and therefore, in addition to collector series resistance r_{sc}, film resistivity and thickness, the substrate resistivity must be considered. For example, calculations using 0.05 and 0.007 Ω-cm substrates were made, based on the fabrication process of high temperature steps (Table 4), using the error function distribution to determine the resulting resistivity profile in the substrate-epitaxial silicon region. Using the following equation [8, 10] which was presented in section I-F.

$$N(x,t) = \frac{N_1}{2}\left[1-\text{erf}\left(\frac{X}{2\sqrt{\Sigma Dt}}\right)\right] + \frac{N_2}{2}\left[1+\text{erf}\left(\frac{X}{2\sqrt{\Sigma Dt}}\right)\right]$$

where: N_1 and N_2 are the impurtiy concentration in substrate and film respectively.
X is the distance into the epitaxial layer from the initial step profile.
Dt is the diffusion coefficient-time product for each process step.

one obtains the resistivity profile given in Fig. 39.

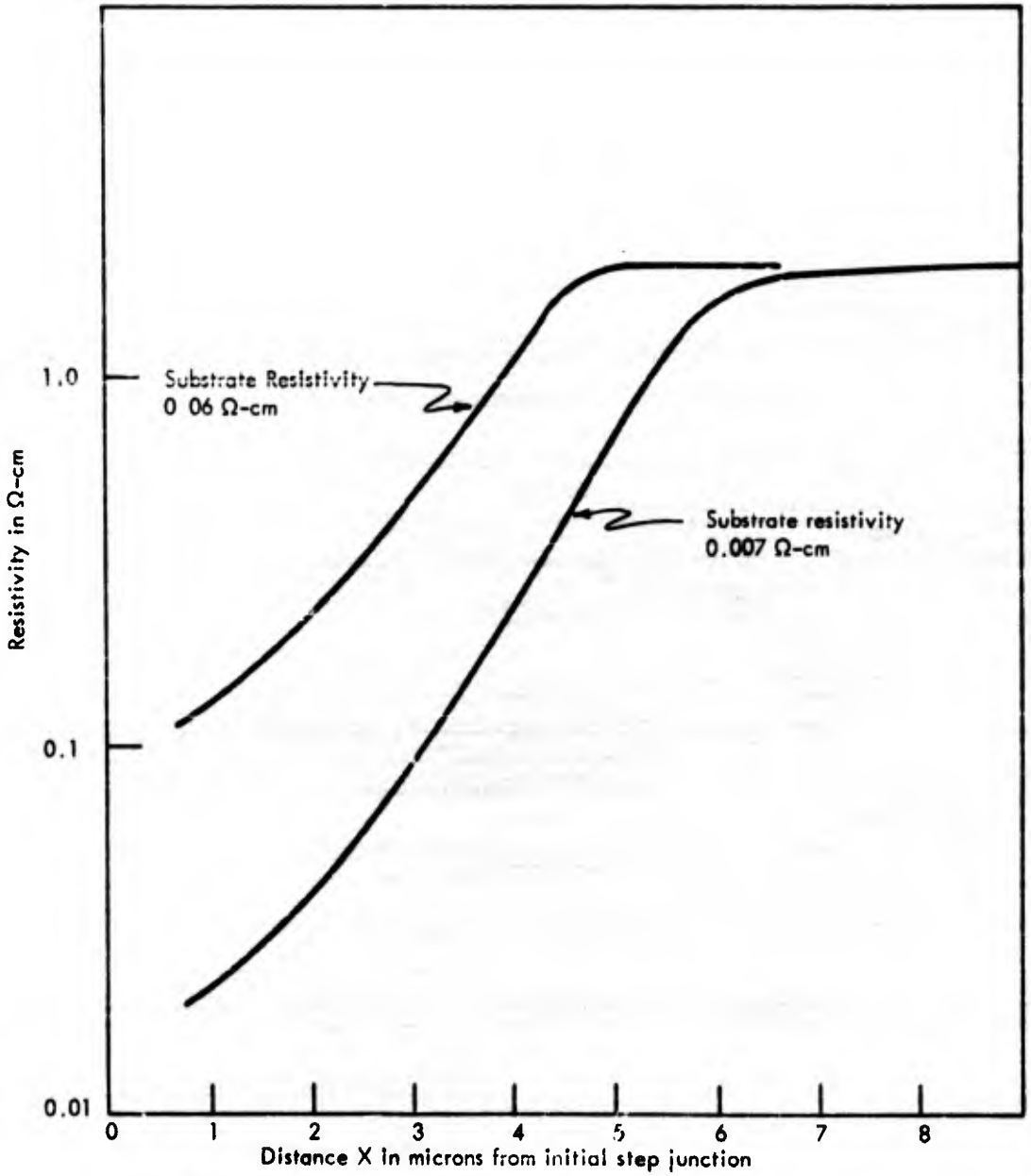


Fig. 39. Impurity Diffusion from Substrate into Film During Fabrication Processing of the Device

Since the device is fabricated in the epitaxial film, crystalline perfection of the film will influence device characteristics. A very clean epitaxial system, select substrate crystals, high purity reactants, and deposition process techniques are required to produce highest quality films.

Film resistivity was controlled by reactor and feed system calibration. Calibration is made on 8 micron p on p+ films using a three-point avalanche breakdown test set. The thicker film is required to unambiguously identify avalanche type breakdown from punch-through on the 2.0 Ω-cm films. All epitaxial material was checked for low avalanche voltage breakdown given by films lower than 2 Ω-cm resistivity.

Table 4

Significant Diffusion Process Steps

Step	Time in Minutes	Temperature °C with Diffusion Coefficient
1st Oxidation	55	1200° (2.95×10^{12})
Base Deposition	30	800° ($> 10^{15}$)
Base Diffusion	120	1100° (3.60×10^{-13})
N+	8	1050° (1.25×10^{-13})
Oxidation	45	950 (1.30×10^{-14})
Emitter	50	1025° (7.60×10^{-14})

Film crystalline quality was evaluated by visual inspection to be free of haze, surface, blemishes, tetrahedrons, and slip. Frequent spot inspection of the surface was made using a metallographic microscope before and after dislocation etching of film. Stacking fault and etch pit densities are estimated on the etched films.

A 316 stainless steel feed system was used for the epitaxial reactor. The system is flowmeter monitored, needle valve controlled, and electrically operated. The flow rate was 40 liters per minute. Silicon tetrachloride vapor concentration, controlled by vapor pressure and dilution, is used to adjust the deposition rate. The deposition rate of this system is 2 microns per minute. The reaction occurred at atmospheric reactants (silicon tetrachloride and hydrogen) and flush gases (helium, Forming gas, and diborane) manipulated by the feed system are of high purity.

Reactor construction is of metal and is water cooled. This is a multi-slice reactor with horizontal gas flow. The heater is silicon coated graphite that is resistance heated. Temperature is controlled by means of a transistorized optical sensor component of the power supply.

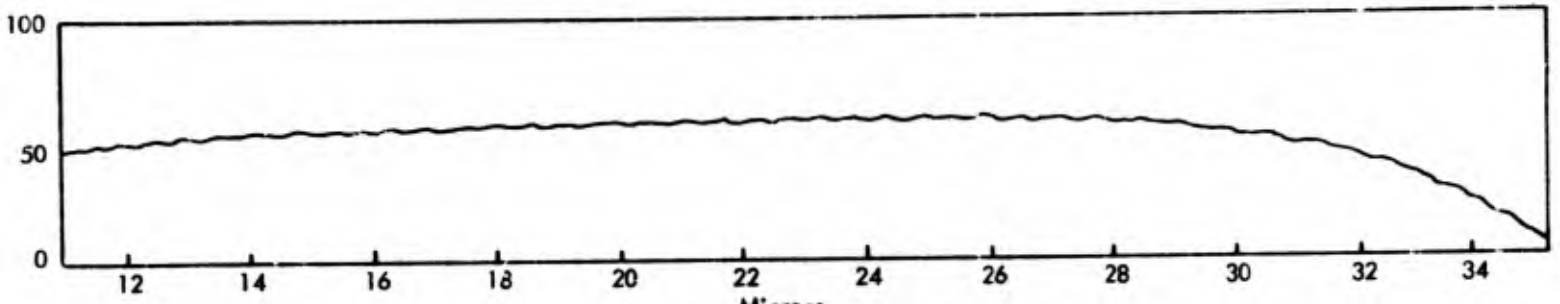
In operation, clean substrates are loaded into the clean deposition chamber which is then flushed. After heat-up in hydrogen at 1270°C the slices are etched in 5% hydrogen chloride. Then the heater temperature is programed to 1150°C where the film is deposited. The chamber is cooled and flushed with forming gas before unloading.

Epitaxial material is quality controlled by film evaluation for thickness, resistivity, and crystalline perfection. A Beckman IR5A with micro-reflectance attachment is employed for film thickness and film thickness profile. Thickness resolution by this technique is dependent on the impurity gradient. Resolution is reduced (Fig. 40) with gentle gradients which are noted when:

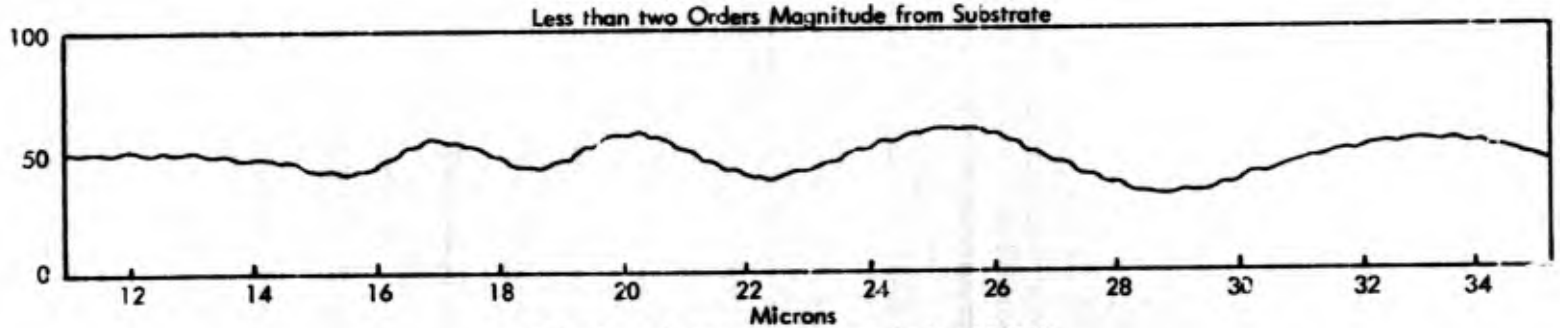
1. Film-substrate impurity concentrations are not greatly different.
2. Substrate dopant is transported (known as mass transport) into the growing film.
3. Diffusion of impurities across the concentration step from substrate into the film during film growth.

Material specified for this device is resolved by the preamplifier modified IR5A when the film is deposited at the specified temperature.

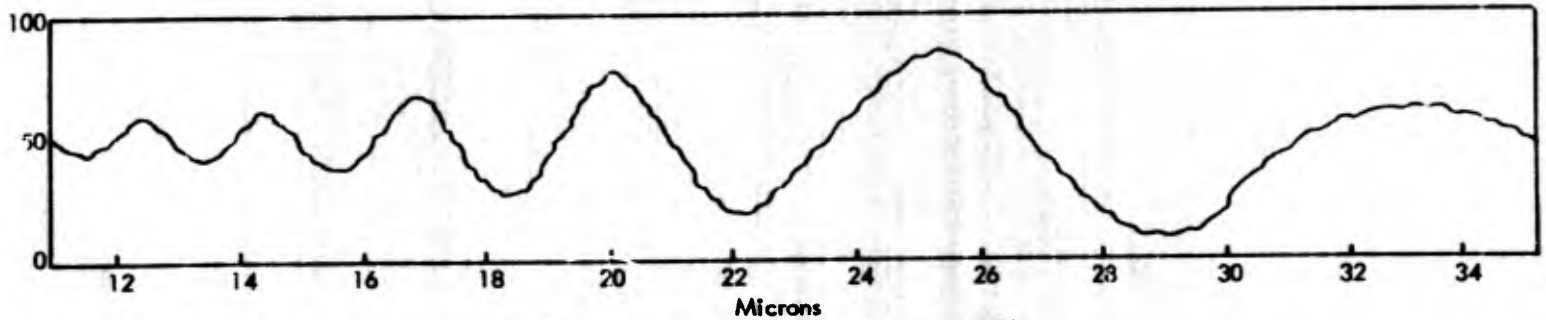
Epitaxial film resistivity is an open-ended type of inspection. Films of 2 Ω-cm that are thicker than 5 microns can be reliably evaluated on the resistivity test set by avalanche breakdown. However, films 5 microns or less give punch-through breakdown for films 2 Ω-cm or higher. The technique employed to produce desired material is to adjust the epitaxial deposition system so as to deposit 2 Ω-cm resistivity films which are 8 microns thick. Then on subsequent deposits to decrease the film thickness using the same feed settings, but decreasing the deposition time. The resistivity test set is used to reject material on the low side of the resistivity specification (low avalanche breakdown) and films below the thickness specification (low punch-through breakdown) but does not identify



Reflectance Trace of Film with Resistivity
Less than two Orders Magnitude from Substrate



Reflectance Trace of Film Deposited at 1250°C



Reflectance Trace of Film Deposited at 1150°C

Fig. 40. IR Thickness Evaluation of Epitaxial Films

5 micron films with resistivity above the resistivity specification. Therefore, the epitaxial reactor system must be calibration checked frequently.

SECTION III
DIFFUSION PROCEDURE

A. OXIDATION

Each p-type epitaxial silicon wafer is cleaned with mineral acids and deionized water immediately prior to thermal oxidation in steam. The oxidation is performed at 1200°C ± 1°C for a period of thirty minutes (5600 Å of oxide — see Fig. 41). The slices are dried for 15 minutes under dry nitrogen and then removed from the furnace. This is to insure the removal of moisture trapped in the oxide structure. Infrared measurements indicate that oxides produced in this manner contain no water.

The material is processed by photo-etching techniques and prepared for base deposition and diffusion.

B. BASE PROCESS

A silicon wafer with oxide selectively removed from the base areas is diffused with phosphorus, a donor. The diffusion apparatus consists of a quartz tube and impurity trap extending over two controlled temperature zones. The first zone is used to control the diffusant vapor pressure and the second to heat the silicon wafers. The furnace temperature is regulated to ± 1°C. The positive temperature gradient between the two zones prevents the deposition of the impurity vapor before reaching the silicon samples. The vapor from the diffusant in the first temperature zone is carried by a gas past the silicon heated in the second zone. $POCl_3$ (16), a low-boiling liquid, is the phosphorus source material used and the system is shown diagrammatically in Fig. 42.

A two step diffusion process is used. The prediffusion is carried out at a relatively low temperature, producing thin layers with minimum surface concentration. The

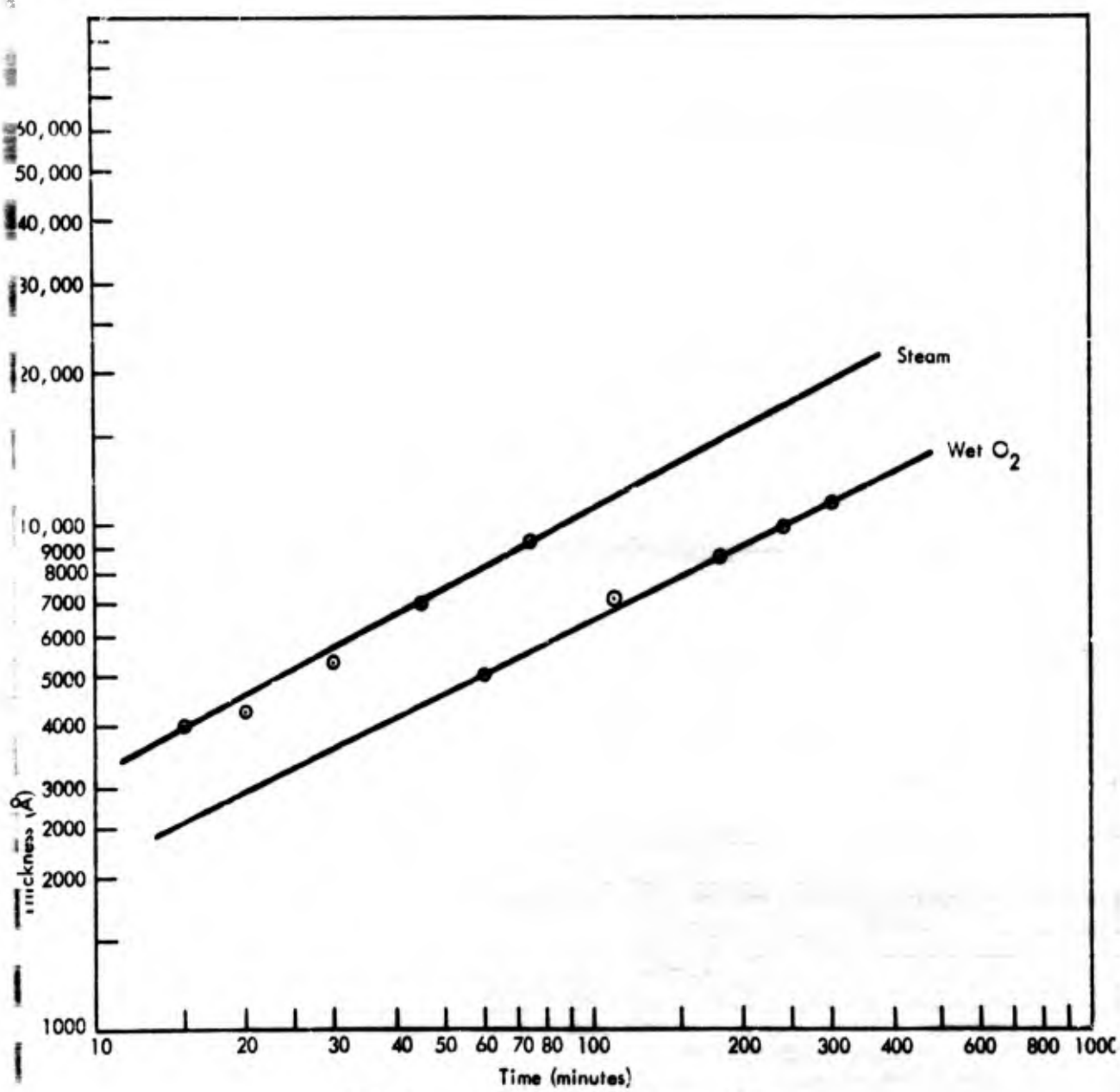


Fig. 41. Oxidation Growth Rate at 1200°C

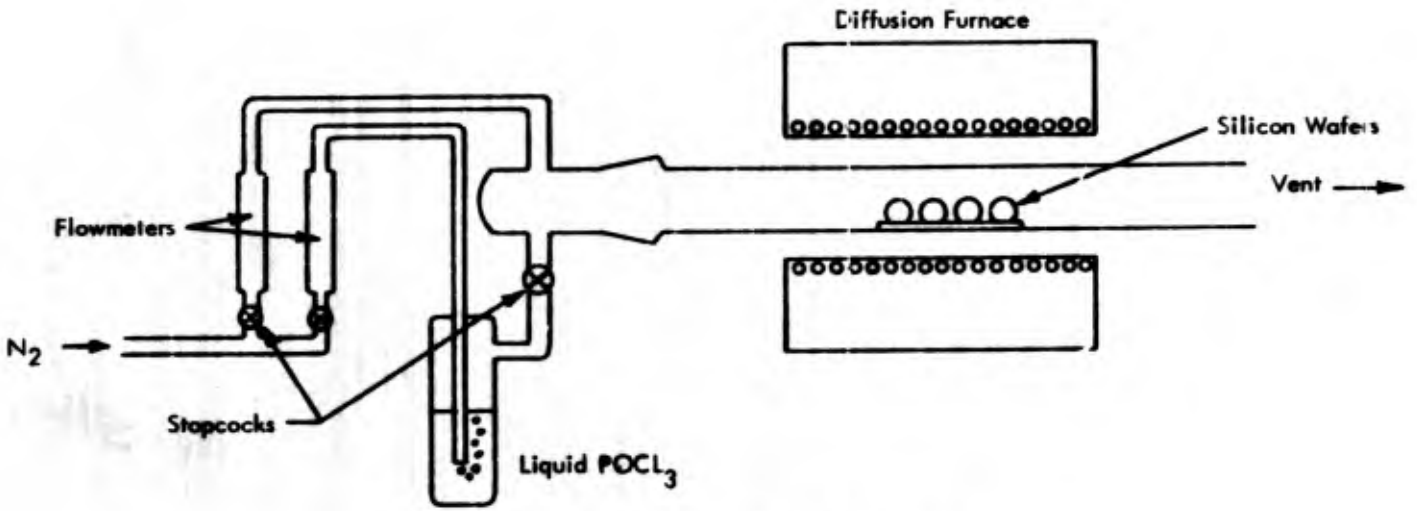


Fig. 42. Schematic Diagram of System for $POCl_3$

main diffusion is then carried out in the absence of additional impurities at higher temperatures. During the prediffusion an essentially sheet source is produced in the surface of the solid. An oxidizing atmosphere grows an oxide layer and no impurities are lost during the main diffusion. In such a process the total number of atoms in the diffused layer is controlled by the deposition. This number may be varied by changing the temperature and time. See Table 5 for experimental data.

TABLE 5 — BASE DIFFUSION DATA

DEPOSITION		SHEET RESISTANCE	DIFFUSION		SHEET RESISTANCE
Temp. (°C)	Time (min.)	Ps (Ω/□)	Temp. (°C)	Time (min.)	(Ω/□)
700	20	2000-3000	1100	120	1300-1700
730	30	1500-2000	1100	120	400-800
760	30	500-900	1100	120	350-450
800	30	100-150	1100	120	35-55
800	20	125-175	1100	120	50-70
800	15	175-225	1100	120	55-75

The values in the sheet resistance column are the minimum and maximum readings possible for a particular time-temperature combination. Three additional factors control the sheet resistance reproducibility from run to run and within a run.

1. The system described in Fig. 42 must be cleaned with deionized water prior to each day of operation. This prevents a phosphorus accumulation in the furnace tube, which would dope subsequent runs as a secondary source.

2. A four-point probe is used to measure sheet resistivity of the diffused layer; however, at very low impurity concentrations the instrument becomes less accurate (i.e. ± 20%).

3. Initially it was not found possible to achieve diffused layer sheet resistance of the order of several hundred ohms/square. This result was interpreted as indicating the presence of a secondary phosphorus source and was partially corrected

by the procedure in (1) above. In addition it was determined that the prediffused layer contained a large concentration of phosphorus atoms which were electrically inactive, but were ionized in the diffusion step. Since most of this phosphorus was expected to be located near the surface an effort was made to remove it by controlled etching of the silicon surface prior to drive-in. The slices were rinsed in dilute HF (10%) for varying periods of time and sheet resistivities measured. See Fig. 43. The results indicate that this method can be used to control the conecntration of inactive phosphorus in the initial predeposited layer.

Tables 6 and 7 give typical sheet resistivities for a twenty slice test run. The prediffusion was performed at 800°C for thirty minutes and the slices were diffused for two hours at 1100°C.

C. CONTACT AREA N+

Early in the fabrication phase of this PNP project, it was determined that present contact technology could not provide a contact for the lightly doped PNP base region. This prompted the addition of a selective N+ deposition to the diffusion sequence. The deposition will produce a thin N+ layer with high surface concentration in the base contact area, and facilitate the use of conventional contact methods. The diffusion apparatus is identical to that represented in Fig. 42.

The initial diffusion process as indicated in Table 8 produced a deep N+ region before the base deposition and a high surface concentration. However, the effect upon the device characteristics was detrimental. The N+ region was diffused for 30 minutes at 1050°C and therefore incompatible with the total diffusion process time of three hours. A schematic representation of this process is shown in Fig. 44. The N+ "fingers" extended into the P+ substrate of the epitaxial slice. The p-n junction formed in the low resistivity substrate gave the units low BV_{CBO} values (i.e. 10-12 volts). However, the high phosphorus concentration ($>10^{21}$ atoms/cc) in the base contact area made V_{BE} values less than one volt possible.

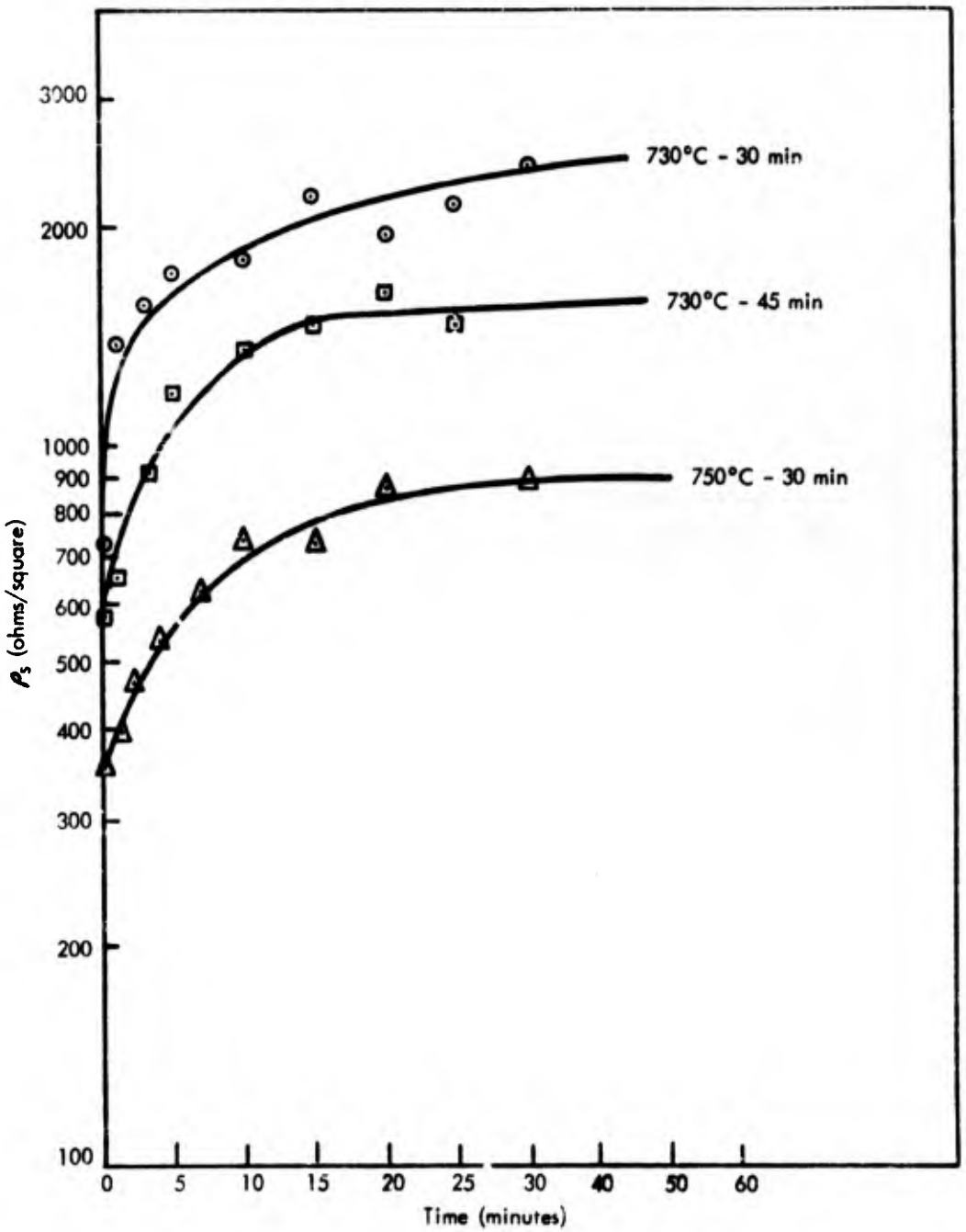


Fig. 43. ρ_s vs Deglaze Time in 10% HF

TABLE 6: BASE DEPOSITION DATA

CONDITIONS: 1. $POCl_3$ depositon at 800°C for 30 minutes

2. All slices probed with Texas Instruments Silicon AC Resistivity Test Set, Model AC-10A.

3. Each slice measured on both sides.

Slice No	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□
1	101	108	5	110	107	9	104	112	13	107	109	17	103	111
	102	109		111	107		105	112		104	108		102	112
	102	108		110	106		105	113		106	109		103	111
	102	109		113	110		107	113		108	112		105	113
	102	104		107	103		102	108		108	108		103	111
2	108	106	6	105	109	10	108	110	14	113	112	18	110	111
	108	105		107	109		108	111		113	113		111	111
	109	105		108	109		109	112		113	113		111	111
	111	108		110	112		112	114		115	111		113	113
	103	100		106	102		104	107		107	108		108	108
3	103	108	7	107	106	11	110	111	15	109	110	19	110	110
	103	107		107	106		111	111		109	109		110	111
	104	106		104	107		111	112		104	110		111	111
	109	110		110	104		113	112		110	113		112	113
	109	105		103	103		103	105		106	108		108	108
4	105	105	8	103	108	12	110	107	16	106	111	20	113	108
	105	106		102	108		110	107		107	111		113	108
	106	105		102	108		110	105		107	111		113	108
	106	105		103	111		112	106		108	116		118	110
	103	103		102	105		107	108		106	108		112	108

TABLE 7: BASE DIFFUSION DATA

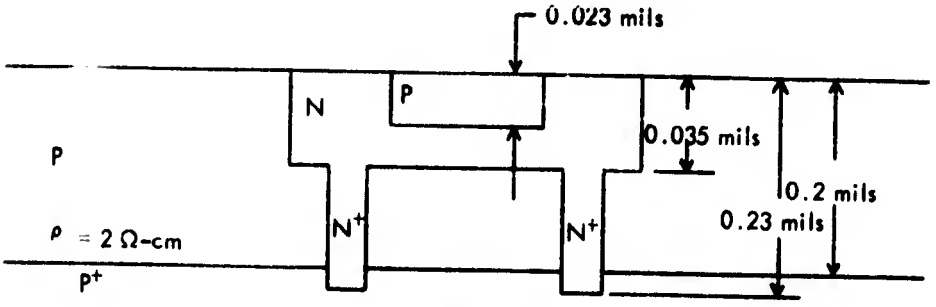
CONDITIONS:
1. Two hours at 1100°C under wet O_2
2. All slices probed with TI Model AC-10A Resistivity Bridge.
3. Each slice is numbered according to Table 2.

Slice No.	Front Ω/□	Back Ω/□	Slice No	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□	Slice No.	Front Ω/□	Back Ω/□
1	35	34	5	35	34	9	37	36	13	37	36	17	35	34
	35	34		34	35		37	36		36	34		35	34
	36	34		34	35		37	35		38	33		35	34
	35	34		34	34		36	34		37	33		34	33
	35	34		34	35		38	35		37	35		35	35
2	34	34	6	33	35	10	35	34	14	36	35	18	35	35
	34	34		34	35		33	35		36	34		35	35
	34	34		35	35		34	34		36	35		35	34
	34	34		34	34		34	35		35	34		35	34
	34	34		35	32		36	35		35	35		36	36
3	34	34	7	33	33	11	36	36	15	35	34	19	33	34
	35	34		33	34		36	36		34	35		33	34
	34	34		32	33		36	35		34	34		34	34
	35	35		33	33		35	35		34	33		33	34
	35	34		33	34		38	36		35	35		34	35
4	33	35	8	36	35	12	36	37	16	36	35	20	36	36
	33	35		36	34		37	37		36	35		36	36
	33	35		36	34		36	37		36	35		36	37
	33	35		36	33		35	38		35	34		34	37
	33	35		36	34		38	37		36	35		36	37

TABLE 8

INTEGRATION OF N^+ PROCESS WITH DIFFUSION SEQUENCE

1st Process	2nd Process	3rd Process
N^+ Deposition	Base Deposition	Base Deposition
Base Deposition	Base Diffusion	Base Diffusion
Base Diffusion	N^+ Deposition	Emitter Deposition
Emitter Deposition	Oxidation	Oxidation
	Emitter Deposition	N^+ Deposition



1st Process

DIFFUSION PROCESSES

Fig. 44

The second process in Table 8 is designed to eliminate low breakdown voltage, but maintain the V_{BE} characteristic of the first process. The process, represented schematically in Fig. 45, reduced the N^+ furnace time 65%. The N^+ region is contained in the epitaxial layer but extends below the base p-n junction. This diffusion sequence proved the most consistant and was used for the major part of the contract period.

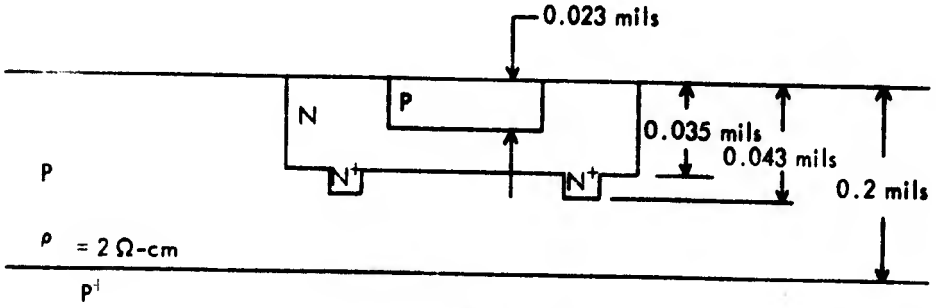
The third process reduced the N^+ depth to a minimum (see Table 8 and Fig. 46), but produced erratic V_{BE} values. Experimental data are shown in Table 9.

N^+ deposition times and temperatures were selected to give a junction depth less than 0.02? mils. BV_{CEO} breakdowns showed marked improvement, especially in the case of no N^+ deposition. However, the erratic V_{BE} values indicate an unsatisfactory base contact region for all samples. Since calculations indicate a high surface concentration (10^{21} atoms/cc) for the N^+ samples, the V_{BE} variance must also be related to the junction depth. The BV_{CEO} "shorts" for samples 43, 45 and 47 were produced by a physical penetration of the emitter into the collector region. The relationship between N^+ surface concentration and V_{BE} values is discussed in more detail in the contact section of this report.

D. EMITTER PROCESS

The PNP emitter process is a one step diffusion. During the early portion of the contract period, the emitter process consisted of a deposition in a closed platinum box with a boric oxide source. The box method for boron diffusion was first discussed by B. T. Howard[17] and L. A. D'Asaro [18] of Bell Telephone Laboratories. Subsequent refinements were made at Texas Instruments[19].

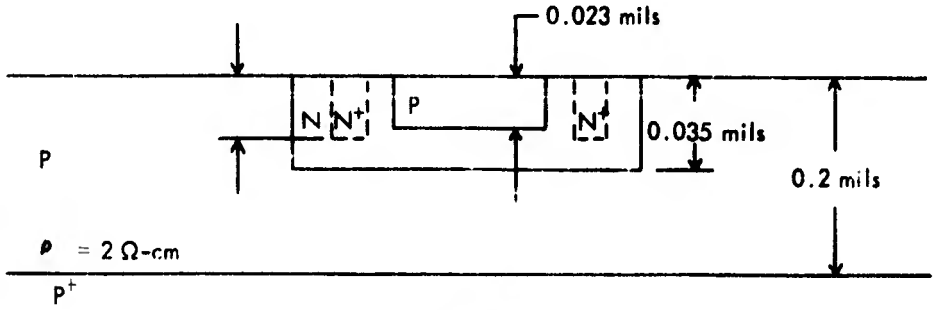
The platinum reactor is contained in a quartz tube which is regulated to ±1°C. Dry filtered nitrogen gas is used as the ambient and when the box and source are not being used, they are stored in the furnace heat zone.



2nd Process

DIFFUSION PROCESSES

Fig. 45



3rd Process

DIFFUSION PROCESSES

Fig. 46

TABLE 9

THIRD DIFFUSION PROCESS DATA

Sample	Deposition Time and Temperature		BV_{CEO}	BV_{CBO}	V_{BE}
	Min.	°C	Volts at 10 μa	Volts at 10 μa	Volts I_C = 1 ma I_B = 0.5 ma
42	No N+		25	*	*
45	30	750	short	12	2.25
47	30	800	short	20	0.82
49	30	850	11	22	3.75
50	10	900	13	12	1.0
51	10	950	13	24	0.93
52	5	1000	15	26	1.54
43	5	1050	short	11	1.75

* No contact to the base region

Reactor construction is shown in Figs. 47 and 48, and slice holders are represented in Figs. 49 and 50. Sheet resistance measurements made on both sides of the slices indicated good uniformity from front to back of an individual slice and from slice to slice. For a given slice the variation in sheet resistance was about ± 5% and from slice about ±10%. The sheet resistance after deposition versus deposition temperature is given by the curve in Fig. 51. The points plotted are the result of numerous experiments [19] for a deposition time of 30 minutes.

There are several disadvantages in the box system which make it undesirable for a production process. The chief problem is the number of slices (6 to 12) that may be deposited during a single deposition. In addition to the limited capacity the system must be cleaned with mineral acids at periodic intervals. This requires one - two days for completion.

It was decided to change the system described in Figure 42. Boron tribromide, a liquid at room temperature, can be used for the source at a temperature of 33°C. The carrier gas was N_2 at a flow rate of 10 cc per minute. The temperature of the silicon was 1025°C in an ambient of N_2 at a flow rate of 1.7 liters per minute and of O_2 at a flow rate of 50 cc per minute. This system can handle a large number of slices and "cleaning time" is reduced to a minimum. The sheet resistance curve in Figure 51 applies to BBr_3 as well as the box - B_2O_3 system. Both systems have the same doping mechanism:

B_2O_3 - Platinum Box:

$$B_2O_3 + Si \qquad SiO_2 + B_{lattice}$$

BBr_3:

$$BBr_3 + O_2 \qquad B_2O_3 + Br_2$$

$$B_2O_3 + Si \qquad SiO_2 + B_{lattice}$$

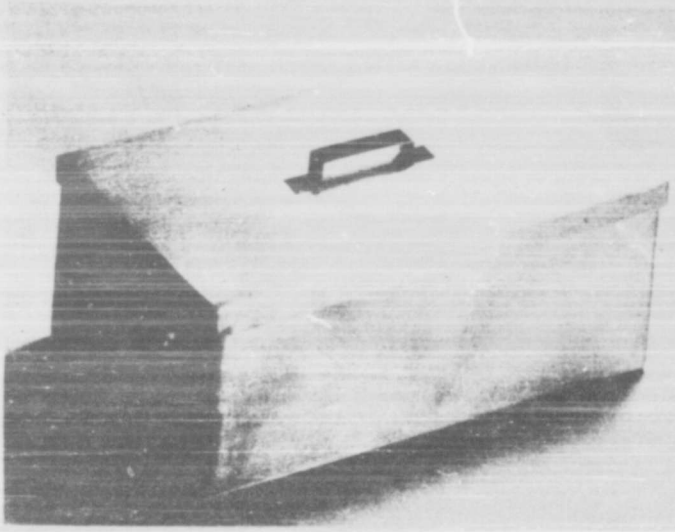


Fig. 47. Platinum Box

Fig. 48. Platinum Box Loaded with Silicon Slices and Source

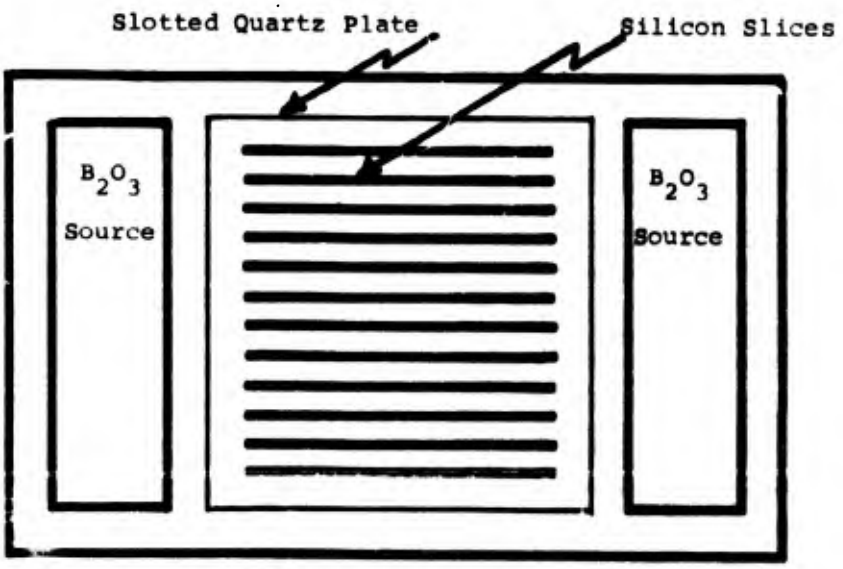


Fig. 49. Slice Holders I

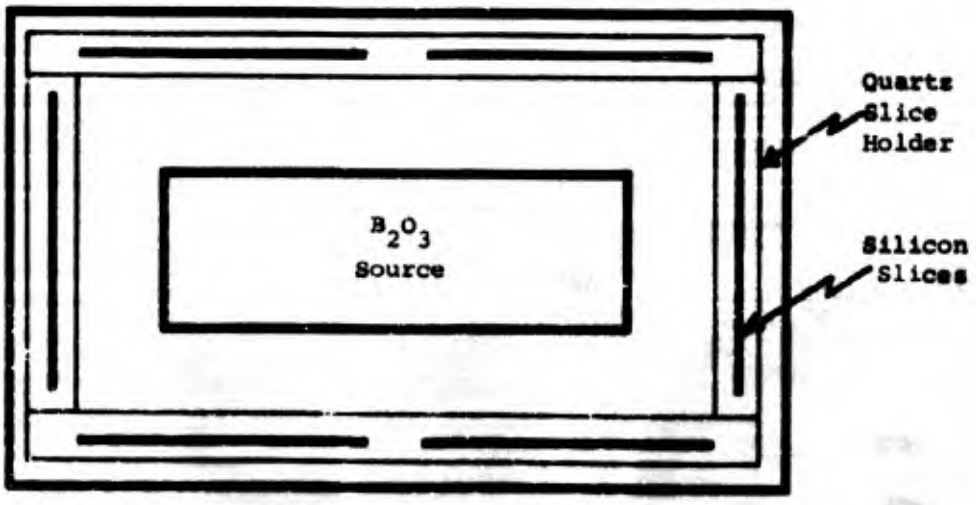
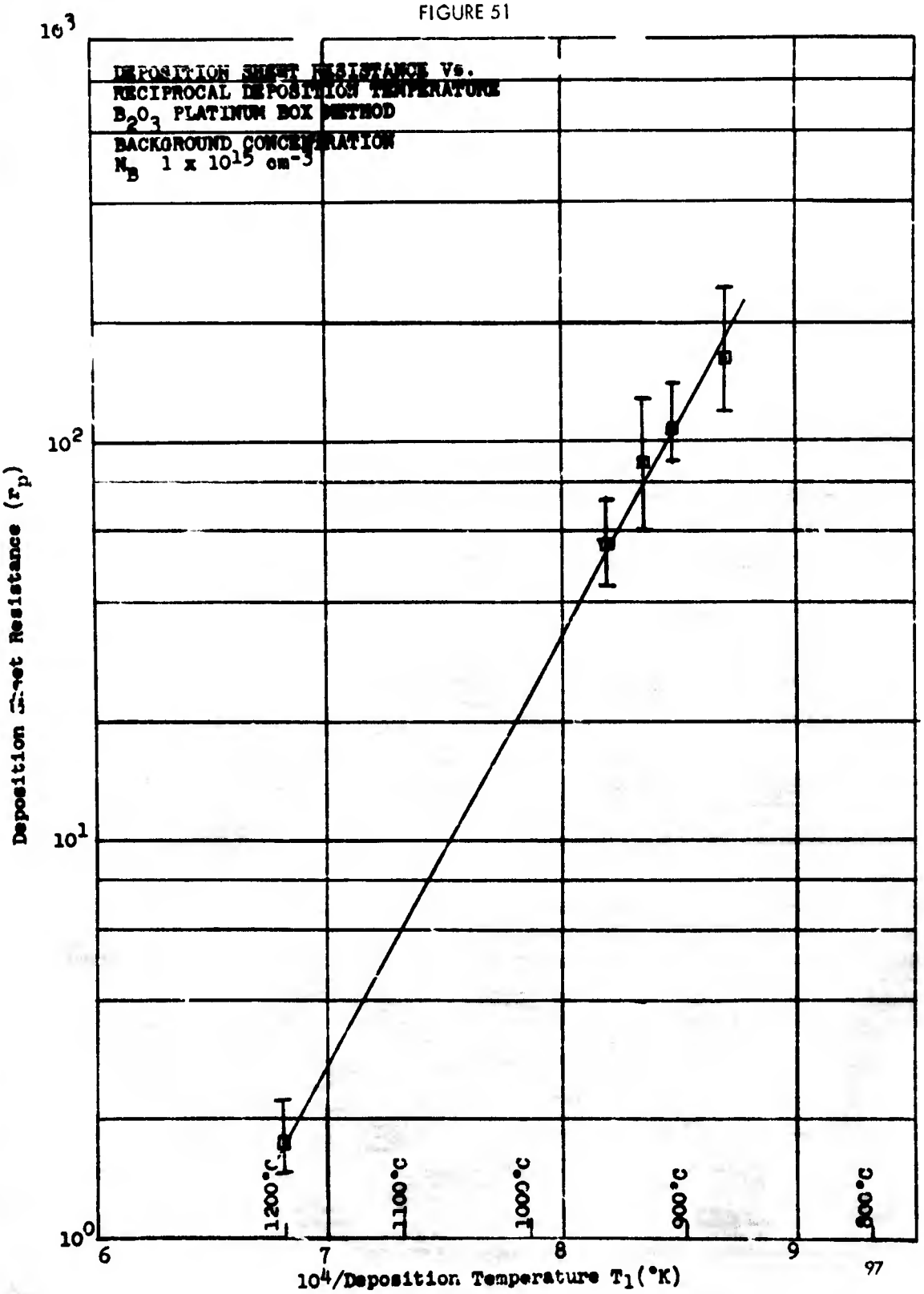


Fig. 50. Slice Holders II

FIGURE 51


DEPOSITION SHEET RESISTANCE Vs.
RECIPROCAL DEPOSITION TEMPERATURE
B_2O_3 PLATINUM BOX METHOD
BACKGROUND CONCENTRATION
N_B 1 x 10^{15} cm^{-3}
Deposition Sheet Resistance (r_p)
10^3
10^2
10^1
10^0
1200°C
1100°C
1000°C
900°C
800°C
6
7
8
9
10^4/Deposition Temperature T_1(°K)
97

SECTION IV
CONTACTS

A. INTRODUCTION

The developed transistor employs a molybdenum-gold expanded contact system which was developed by Texas Instruments with company funds prior to the initiation of this contract. The problem of getting a good ohmic contact to the PNP transistor appeared quite formidable, at the outset, because of several of its design characteristics, such as:

1. Small narrow stripes
2. Very shallow diffusions
3. Low surface concentrations, especially on the N-type base. (2×10^{17} -6×10^{18} atoms/cc)

The physical size of the device requires the use of an "expanded" contact. (The contact extends out over the oxidized collector material and is made large enough to facilitate bonding of the lead wire.)

Various contact systems used, reasons for their use, and pertinent results are described in this section.

B. RESULTS

Early experiments, performed on material with a relatively low surface concentration of P atoms, i.e. 10^{17} - 10^{19} atoms/cc, involved contact systems which employed different metals on the base and emitter regions. Figure 52 is a drawing of some of the contact systems that were worked out. These geometries were achieved by

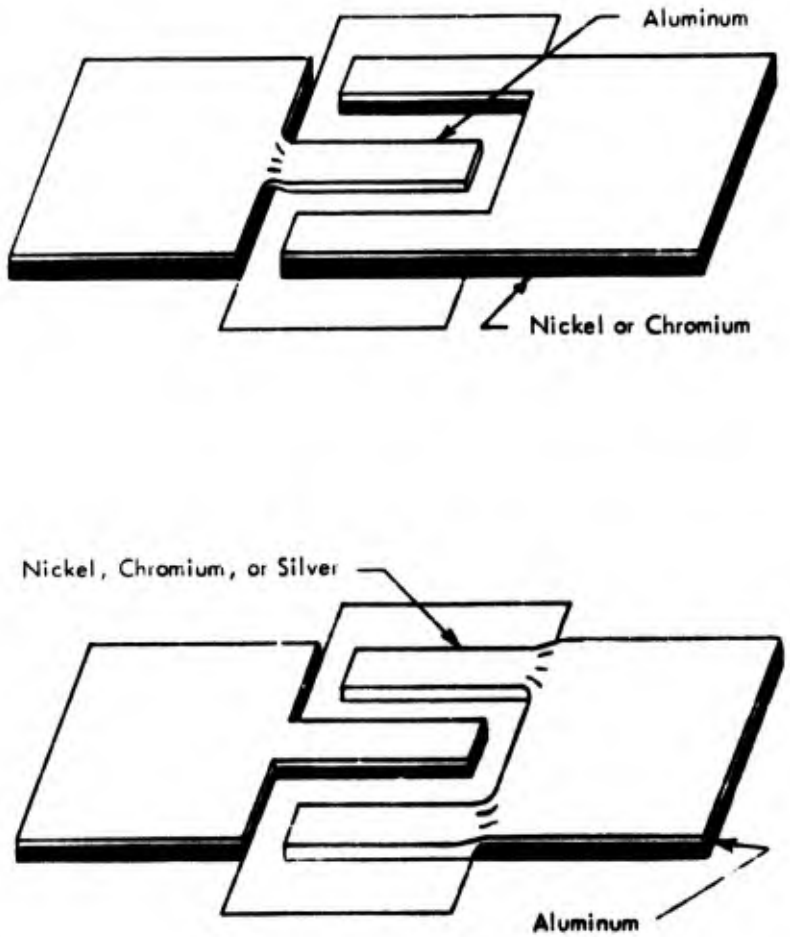


Fig. 52 PNP Contact Investigations

"evaporation-KMER masking-etching" operations. Figures 53 and 54 are photographs that illustrate two stages of completion of the device. Although the physical characteristics (definition, thickness, appearance) of these contacts were acceptable, severe electrical degradation resulted in each case. Particularly serious was the fact that the devices exhibited high forward voltages indicating, of course, high resistance and/or rectifying contacts. It was noted that sintering operations usually produced shorted junctions.

The results of single metal contacts and of contacts which employed different metals on the base and emitter regions are listed below.

1. Aluminum Contacts

Poor contacts resulted on low surface impurity concentration material. However, a good contact resulted when the surface concentration approached 10^{21} atoms/cc. It should be noted that in every case there was junction degradation in the form of high leakage currents. Baking at 300°C sometimes reduced the level of leakage. Sintering or alloying the contacts caused further electrical degradation. Most significant was the severe reduction of h_{FE}. The value of h_{FE} in some cases dropped from 30 to values of less than 1.

2. Magnesium

The magnesium contact had an extremely high V_{BE}. The emitter-base breakdown voltage was severely degraded.

3. Gold

Gold was evaporated on one slice of low surface concentration material in a manner to cause alloying of the first very thin layer. The contact resistance was poor and h_{FE} low. The reverse breakdown characteristics were not degraded.

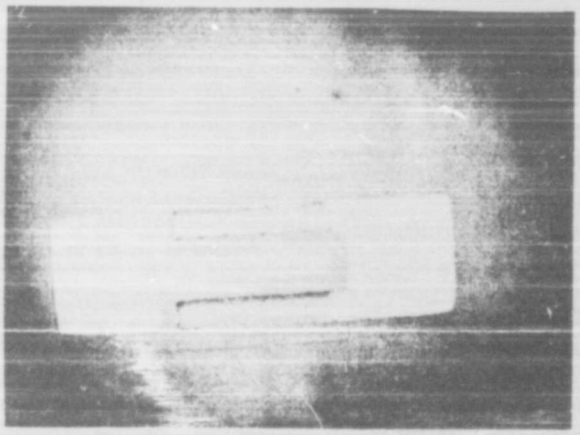


Figure 53 Al over emitter window only. 400X

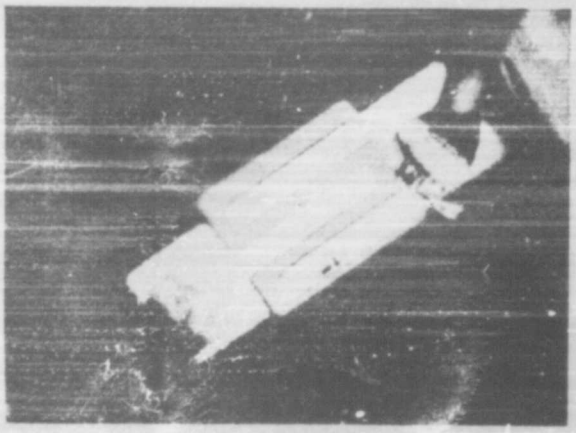


Figure 54 Completed device showing 0.7 mil Al wires attached. 400X

4. Chrome and Nickel

Chromel, which was 70% Ni and 30% Cr, was evaporated as the under layer in combination with silver-gold, aluminum and silver all on low surface concentration material. In each case the contact resistance (V_{BE}) was high, h_{FE} low, and the junction had soft breakdown voltages. The same was true for the nickel-silver contact.

5. Chromium-Aluminum

Contacts with this system on low surface concentration material were not acceptable. Chromium, which oxidizes rapidly, could not be protected sufficiently during the photomasking and leaching process to allow good adherence of the aluminum to the chromium. No other sandwich or multi-layer contacts were used that had to be removed from the evaporator before the final top layer metal was applied.

Since the impurity concentrations and diffusion depths are closely related to the problems involved in the application of contacts, Table 10 is included for the readers convenience.

A molybdenum-gold contact system has been used without inducing electrical degradation on high surface concentration material. Essentially, the system utilizes a first protective metal of molybdenum covered by gold to which the wire weld is made.

TABLE 10

BASE SURFACE IMPURITY DATA

kun No.	Resistivity Ω cm	P_S (Ω/□)	Diffusion, mils	C_S (Atoms/cc)	N^+
4	.00385	208	.0073	1.1×10^{20}	No
8	.0288	722	.0158	6×10^{18}	No
9	.0933	2333	.0158	5×10^{17}	No
10	.0796	1990	.0158	7×10^{17}	No
15	.168	1900	.0348	2×10^{17}	No
16	.121	1363	.0348	3×10^{17}	No
18	.00065	1.3	.1972	2×10^{21}	Yes
19	.000486	1.1	.174	3×10^{21}	Yes
20	.078	1320	.0232	7×10^{17}	No

SECTION V
RELIABILITY STUDIES

Units from run numbers 34-41, large and small geometries, were placed on group B inspection examinations. Very few conclusions could be reached regarding the collector cutoff current reliability. The cutoff currents ranged from nanoamps to milliamps, thereby making correlation after testing difficult.

The contacts functioned well through temperature and shock testing. Refer to Table 17 for the Group B inspections and test end points.

Listed in Table 11 are preliminary test data for units subjected to temperature cycling. The temperature cycle was between -65 and 200°C.

TABLE 11

Unit Number *	Initial			Final		
	I_{CBO} NA	I_{CEO} μa	h_{FE}	I_{CBO} NA	I_{CEO} μa	h_{FE}
1	0.002	.0001	571	0.03	0.01	53
2	9.0	0.3	133	8.8	0.44	130
3	0.8	0.03	142	1.09	0.11	139
4	0.02	.005	80	0.03	0.01	76
5	0.02	0.2	167	0.03	0.5	166
6	98 μa	3000	110	μa	μa	116
7	940	240	303	μa	μa	29

* These units are from run #41 (large geometry).

This group shows two failures on h_{FE} degradation and two on cutoff current.

Shock tests were 500 G for 1.0 nsec in the $X_1Y_1Y_2Z_1$ planes. Acceleration tests were 10,000 G for one minute in each plane. Vibration fatigue tests were 20 G for 32 hours per plane (X_1, Y_1, Z_1) and variable frequency at 100-2000-100 cps in 4 minute sweeps. Listed below are the results of seven units from run #41 large geometry for the above tests.

TABLE 12

Unit Number	Initial			Final		
	I_{CBO} na	I_{CEO} μa	h_{FE}	I_{CBO} na	I_{CEO} μa	h_{FE}
8	0.02	11	172	0.03	36.0	187
9	48 μa	1.3 ma	71	46 μa	2.0 ma	90
10	89 μa	1.7 ma	167	80 μa	27 ma	196
11	3.7 μa	26	21	0.02	3.0 ma	NR
12	0.25	0.7	131	0.27	.76	146
13	0.06	0.15	149	0.07	.15	167
14	0.08	15	147	0.12	15	162

The current gain values are consistent, but the cutoff current values are not; no major failures are observed.

Operating life tests were for 1000 hours. End test results for run #41 follow:

TABLE 13

Unit No.	Initial I_{CBO}	Initial I_{CEO}	Initial h_{FE}	500 hours I_{CBO}	500 hours I_{CEO}	500 hours h_{FE}	1000 hours I_{CBO}	1000 hours I_{CEO}	1000 hours h_{FE}
	na	na		μa	μa		μa	μa	
15	.005	0.42	117	1.0	400	105	2.2	270	103
16	.075	360	179	0.4	25	142	0.3	20	141
17	180 μa	3 ma	95	77	1000	83	82	700	83
18	.06	228	192	0.2	94	77	0.1	40	143
19	0.02	193	200	0.9	290	143	0.7	220	156
20	2.0	5	42	1.3	1000	91	0.5	0.5	41
21	82 μa	3 ma	108	86	1.3	39	83	690	83

All data were measured at the following conditions:

I_{CBO}	$V_{CB} = 10$ v	$I_E = 0$
I_{CEO}	$V_{CE} = 10$ v	$I_B = 0$
h_{FE}	$V_{CE} = 5$ v	$I_C = 10$ ma

Reliability data on the final version of the developed units could not be obtained before the completion of the contract because of the time required for the 1000 hour life and storage tests.

SECTION VI
CONCLUSIONS

A. COLLECTOR SERIES RESISTANCE AND SATURATION VOLTAGE

The collector series resistance of the developed transistors is twice as large as desired. Data presented in the saturation voltage section indicate that the collector series resistance is the major component of the high $V_{CE(sat)}$ at the operating current level of 10 ma. The epitaxial layer width was reduced once during the contract period; however, the reduction of $V_{CE(sat)}$, although substantial, was not adequate in order to reduce the effect of the high $V_{CE(sat)}$ upon h_{FE} at the 10 ma level. Figures 35 and 36 illustrate this effect. The current gain below 10 ma is adequate enough to allow the device to be used as an amplifier at low current levels.

The 2 mil^2 geometry was used for the developed transistor because of its low capacitance due to its small area. The emitter area of 0.2 mil^2 produced a much larger collector series resistance than the 0.6 mil^2 emitter of the 12 mil^2 geometry transistor. This result has been noted many times with NPN switches and is at least partially compensated by the reduction of the collector resistivity and layer thickness. Consequently, a substantial reduction of the collector epitaxial resistivity and thickness is required for the reduction of r_{sc}. This would decrease $V_{CE(sat)}$ as well as improve current gain and switching times.

B. CURRENT GAIN

The fall off of h_{FE} at low voltage and 10 ma collector current is primarily due to the high $V_{CE(sat)}$ at 10 ma and is not due to inadequate emitter injection efficiency. However, undesirable surface conditions at the emitter-base junction are contributing to some degradation of h_{FE}. Bake-out techniques affecting these surface conditions have

improved h_{FE} and were employed on all final diffusion runs.

The peak h_{FE} occurs at 3 ma which is comparable to that for NPN switching transistors employing this 2 mil^2 geometry. The level of h_{FE} is above 50 at peak current and fall off (except for that due to $V_{CE(sat)}$) is not drastic. Consequently, current gain is adequate providing the $V_{CE(sat)}$ and surface conditions can be controlled.

C. BASE-EMITTER VOLTAGE

A base-emitter voltage, V_{BE}, of 0.9 volt at I_C = 10 ma and I_B = 1 ma had been achieved by providing an adequate N^+ surface concentration in conjunction with the MoAu contacts. Contact to the experimental units was difficult. High V_{BE} values resulted from high contacts resistance which was attributed to the low surface concentration and the shallow diffusions. However, the MoAu contact system provides a lower contact resistance for a given N^+ profile than any other contact system investigated.

Slice preparation techniques before contacts also contribute to V_{BE} variation. Because of the shallow diffusion, surface conditions, as mentioned above, affect the contact resistance. Consequently, surface preparation procedures and techniques contribute considerably to the success of the MoAu contact system. The procedures outlined in the specification section provided the best results for contact evaporation and V_{BE} measurements.

D. LEAKAGE CURRENTS

Leakage currents I_{CBO}, I_{CEO}, I_{EBO} are at the 1 na level when measured at 15 v, 10 v, and 4 v, respectively. Problems with inversion layers and soft breakdowns were observed with the majority of the experimental runs. The use of the p^+ guard ring improved the leakage currents to a noticeable degree; however, the control of leakage current across the slice is not adequate. Of course, the shallow diffusions make the control of surface conditions more difficult, but improvement was attained by the development of compatible diffusion steps and slice preparation techniques. Also, the

use of pyrolytic oxide indicared that the oxide mask which is thermally grown needs to be investigated and improved to protect the surface during the diffusion and contact procedures.

E. COLLECTOR AND EMITTER BREAKDOWN VOLTAGES

The high emitter breakdown voltage of 12 volts as originally specified in the contract was incompatible with the shallow diffusions and the N^+ contact diffusion. Upon reduction of the emitter-base voltage requirement, adequate contact (V_{BE} = 0.9 volts) was made to the shallow diffused-base region. A low concentration base is desirable for high f_T and high speed switching provided the N^+ region does not alter the designed base region. Heavily doped base regions can provide high f_T values when the base width is 0.01 mils or less such as with many NPN switches. This increase in base concentration would demand, however, a low emitter-base voltage, but would provide a lower contact resistance.

The collector breakdown voltages, BV_{CBO}, BV_{CEO}, were reduced by the attempt to lower $V_{CE(sat)}$ and by the N^+ diffusion step. It has not been determined whether the N^+ diffusion will always lower the collector breakdowns. In fact, the final diffusion runs resulted with BV_{CBO} = 40 v and BV_{CEO} = 30 v.

F. STORAGE TIME

The storage time constant, τ_s, is approximately 20×10^{-9} seconds and is too high a value for a switching transistor. Life time killing techniques are essential for the reduction of τ_s. Adequate lifetime controls were exhibited by gold diffusion which reduced the storage time constant to 5×10^{-9} seconds. However, saturation voltage increased by a factor of two or three which made the use of gold diffusion impractical for the present design.

G. FALL TIME

In order to attain a fall time of 6 nsec with a 300 ohm load resistance (I_{B2} = 0.25 ma), it is necessary to have a fall time constant, τ_f, of less than 200 psec. The base transit time of the developed transistors is much too large in order to meet this requirement. Also, the capacitance, C_C, is large primarily due to capacitances other than the junction capacitance. In fact, the switching times are reaching the point of being circuit limited instead of device limited and reconsideration of circuit requirements is necessary in order to specify the switch parameters

The redesigning of the switching fixtures improved switching performance noticably. This was accomplished by reducing the parasitic capacitances associated with resistor and capacitor positions and lead lengths in the switching fixture.

H. CONTACTS

A good low resistance expanded PNP contact was achieved with several systems. These systems were chromium-gold, chromel-gold, vanadium-gold, cobalt-gold, molybdenum-aluminum, nickel-aluminum, and molybdenum-gold. The molybdenum-gold system was selected as the best of these. Careful control of several critical factors must be maintained during the evaporation and during the pre-evaporation cleanup. For example, the material must be free of organic contamination, and the base and emitter surfaces must be free of oxide.

I. SUMMARY OF OVER-ALL CONCLUSIONS

Listed below are the over-all conclusions reached as a consequence of the analysis of the developed transistor designed toward the contract specification.

1. The high saturation voltage at 10 ma and the 35 ohm collector series resistance are largely the result of the very small area of the device (emitter area $\simeq$ 0.20 mil^2).

2. Current gain fall off at V_{CE} = 0.5 and I_C = 10 ma is caused by the high saturation voltage at this level.
3. Current gain at low current levels is adequate for the device to be used as an amplifier.
4. A base-emitter voltage, V_{BE}, of 0.9 v at I_C = 10 ma and I_B = 1 ma can be attained with the use of an N^+ contact region ($N_S \geq 10^{20}$ atoms/cc) and the MoAu contact system.
5. Leakage currents I_{CBO}, I_{CEO}, I_{EBO} can be less than 1 na, but are highiy dependent upon slice preparation techniques.
6. Reduction of collector and emitter breakdown voltages allowed for adequate contact to be made to the shallow diffused-base region.
7. Storage time constant, τ_s, can be reduced to 5×10^{-9} seconds by gold diffusion techniques.
8. To obtain a fall time, τ_f, of 6 nsec with a 300 ohm load resistance and turn-off current of 0.25 ma, it is necessary to have an f_T of 2 Kmc.
9. The molybdenum-gold contact system provides the best low resistance expanded PNP contact.

SECTION VII
RECOMMENDATIONS

A. BASE WIDTH AND CONCENTRATION

The transistor base width should be reduced to less than 0.01 mils in order to increase the cutoff frequency, f_T, and consequently the switching speed. This reduction over the present width of 0.02 mils is possible based upon the control exhibited on similarly diffused NPN transistors. This reduction has also been achieved on several PNP experimental tests after the completion of contract work. Refer to Fig. 55 for a cross section of such a base width. The cutoff frequency, f_T, which depends upon the square of the base width would be considerably increased by such a reduction. As Figs. 2 and 3 indicate, an increase in f_T by 500 mc would produce a major reduction in switching time.

An increase in base concentration would provide lower contact resistance enabling better contact to be made to a shallow base (less than 0.04 mils). Of course, the emitter-base breakdown would be reduced; however, a BV_{EBO} of 5 volts would be adequate.

B. GOLD DIFFUSION

A reduction of the storage time constant, τ_s, would result from gold diffusion techniques employed to control lifetime. Data obtained from the contract work as well as NPN switch development indicate that a storage time constant of less than 5×10^{-9} seconds can be produced by gold diffusion.

A substantial decrease in $V_{CE(sat)}$ could still be produced even though it has been stated in this report that gold diffusion increases $V_{CE(sat)}$, by using lower resistivity

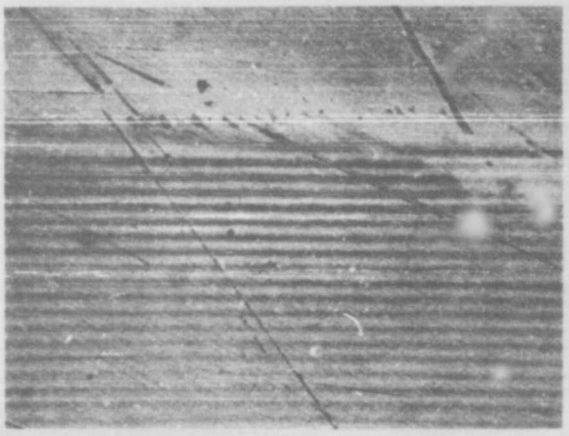


Fig. 55. Diffusion Cross-section
Base Width <0.01 mils

material. This has been successful on NPN switching transistors. Also, high-resistivity material may be used to obtain the same effect by reducing the epitaxial layer width and producing an intrinsic concentration layer.

C. EPITAXIAL MATERIAL

Since the transistor is about one micron deep, while the epitaxial layer is 4 to 5 microns deep, improved characteristics would be expected if thinner films on lower resistivity substrates were used. Approximately half of the value of the summation of the Dt product is produced in the initial oxidation step of the device fabrication. An alternate rapid method for this oxidation step would facilitate thinner films and/or lower resistivity substrates. Only boron doped substrate silicon has been used to date. Substrate crystal doped with a slower diffusing p-type impurity could also be used to reduce the required epitaxial layer thickness.

The recommended changes in epitaxial layer resistivity and thickness would cause a reduction of the collector breakdown voltage to 10 volts. However, improvements in other characteristics would result in overall improvement in performance.

D. SUMMARY OF RECOMMENDATIONS

Listed below are the recommendations developed as a result of the overall conclusions reached at the completion of this contract.

Recommendations

1. Reduce the base width to less than 0.01 mils in order to decrease the base transit time, τ_b.
2. Reduce the storage time constant, τ_s, to less than 5×10^{-9} seconds by gold diffusion techniques.
3. Reduce the epitaxial layer resistivity and thickness in order to lower the collector-series resistance, r_{sc}.

SECTION VIII
SPECIFICATIONS

A. ELECTRICAL SPECIFICATIONS

1. Final Test Table 14

Parameter	Condition	Symbol	Limits Min.	Typ.	Max.	Units
Collector cutoff Current	V_{CB} = 15 v I_E = 0	I_{CBO}		0.1	1.0	na
Collector cutoff current	V_{CE} = 10 v I_B = 0	I_{CEO}		0.1	1.0	na
Emitter Cutoff current	V_{EB} = 4 v I_C = 0	I_{EBO}		0.1	1.0	na
Collector breakdown voltage	I_C = 100 µa	BV_{CBO}	20	22		v
Collector breakdown voltage	I_C = 100 µa	BV_{CEO}	10	15		v
Emitter-base breakdown voltage	I_E = 100 µa	BV_{EBO}	6.0	6.4		v
Saturation voltage	I_C = 10 ma I_B = 1 ma	$V_{CE(sat)}$		0.3	0.5	v
Static forward current transfer ratio	V_{CE} = 0.5 v I_C = 10 ma	h_{FE}	10	20		
Static forward current transfer ratio	V_{CE} = 1.0 v I_C = 10 ma	h_{FE}	30	40		

Parameter	Condition	Symbol	Limits Min.	Typ.	Max.	Units
Static forward current transfer ratio	V_{CE} = 2.0 v I_C = 3 ma	h_{FE}		65		
Sustaining Voltage	I_C = 10 ma V_{EB} = 0	LV_{CES}	20	25		v
Output Capacitance	V_{CB} = 15 v	C_{ob}		1.1	2	pf
Small Signal Common emitter forward current transfer ratio	V_{CE} = 1 v I_C = 10 ma f = 100 mc	$\|h_{fe}\|$	10	15		db
Small Signal common emitter forward current transfer ratio	V_{CE} = 1.9 v I_C = 10 ma f = 100 ma	$\|h_{fe}\|$	15	18		db
Delay Time	V_{CC} = 3.0 v R_L = 300 ohms $V_{BE(off)}$ = 0.5 v	t_d		3.3	4.0	nsec
Rise Time	I_{B1} = 1.0 ma	t_r		4.0	6.0	nsec
Storage Time	V_{CC} = 3.0 v R_L = 300 ohms I_{B1} = 1.0 ma	t_s		15	20	nsec
Fall Time	I_{B2} = 0.25 ma	t_f		12	15	nsec

2. Maximum Ratings Table 15

Parameter	Value
BV_{CEO}	10 v
BV_{EBO}	6 v
I_C	20 ma
P_C	0.20 watts
T_j	200°C
T_{stg}	-65 to 200°C

3. Reliability Table 16

Examination or Test	Conditions	Symbol	Limits Min.	Limits Max.	Units
Temperature Cycling	-65 to 200°C 5 cycles				
Shock	Non-operating 500 g				
Constant Acceleration	10,000 g Non-operating				
Thermal resistance		θj-A		0.175	°C/mw
Storage life	T_A = 200°C 1000 hours				
Operating life	V_{CE} = 10 v I_C = 20 ma 1000 hours				

4. Test End Points Table 17

Test	Conditions	Symbol	Limits Min.	Limits Max.	Units
Collector cutoff current	V_{CB} = 15 v I_E = 0	I_{CBO}		2.0	na
Collector cutoff	V_{CE} = 10 v I_B = 0	I_{CEO}		2.0	na
Static forward current transfer ratio	V_{CE} = 10 v I_C = 10 ma	h_{FE}	30	120	

B. DESIGN SPECIFICATIONS

1. Constants Table 18

Parameter	Symbol	Condition	Value
Delay time constant	$\tau_d = C_{TOTAL}$		2.3 pf
Rise and Fall time constant	$\tau_r = \tau_f = (\tau_b + R_L C_C)$		400 psec
Storage time constant	τ_s		16 nsec
Collector junction capacitance	C_{TC}	V_{CB} = 1 v	0.4 pf
Emitter junction capacitance	C_{TE}	V_{EB} = 0 v	0.4 pf
Collector capacitance	C_C		0.8 pf
Base Transit Time	τ_b		160 psec
Base Width	W		0.02 mils
Collector series resistance	r_{sc}	I_C = 10 ma	35 ohms

2. Geometry

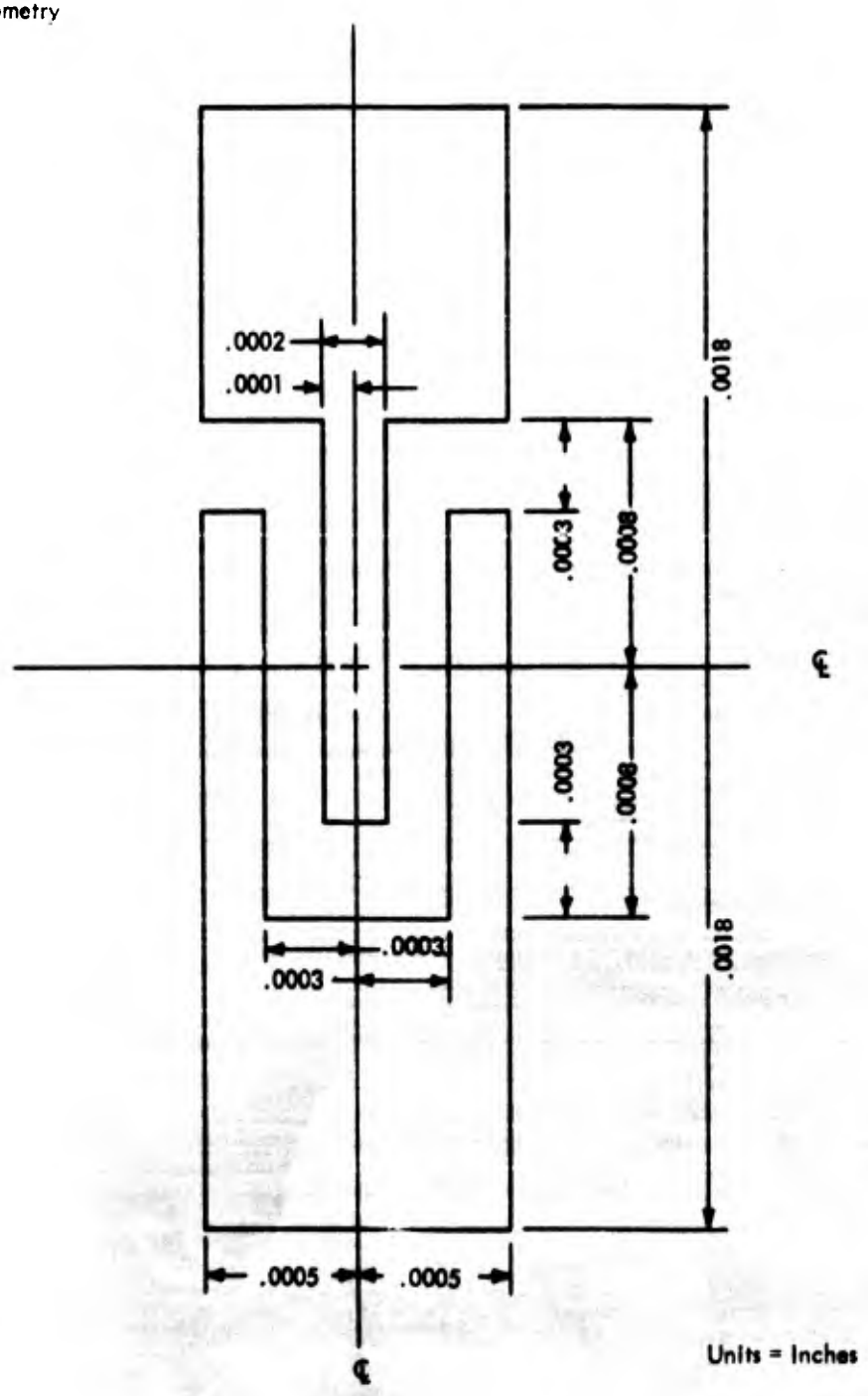


Fig. 56. Contact Mask Dimensions

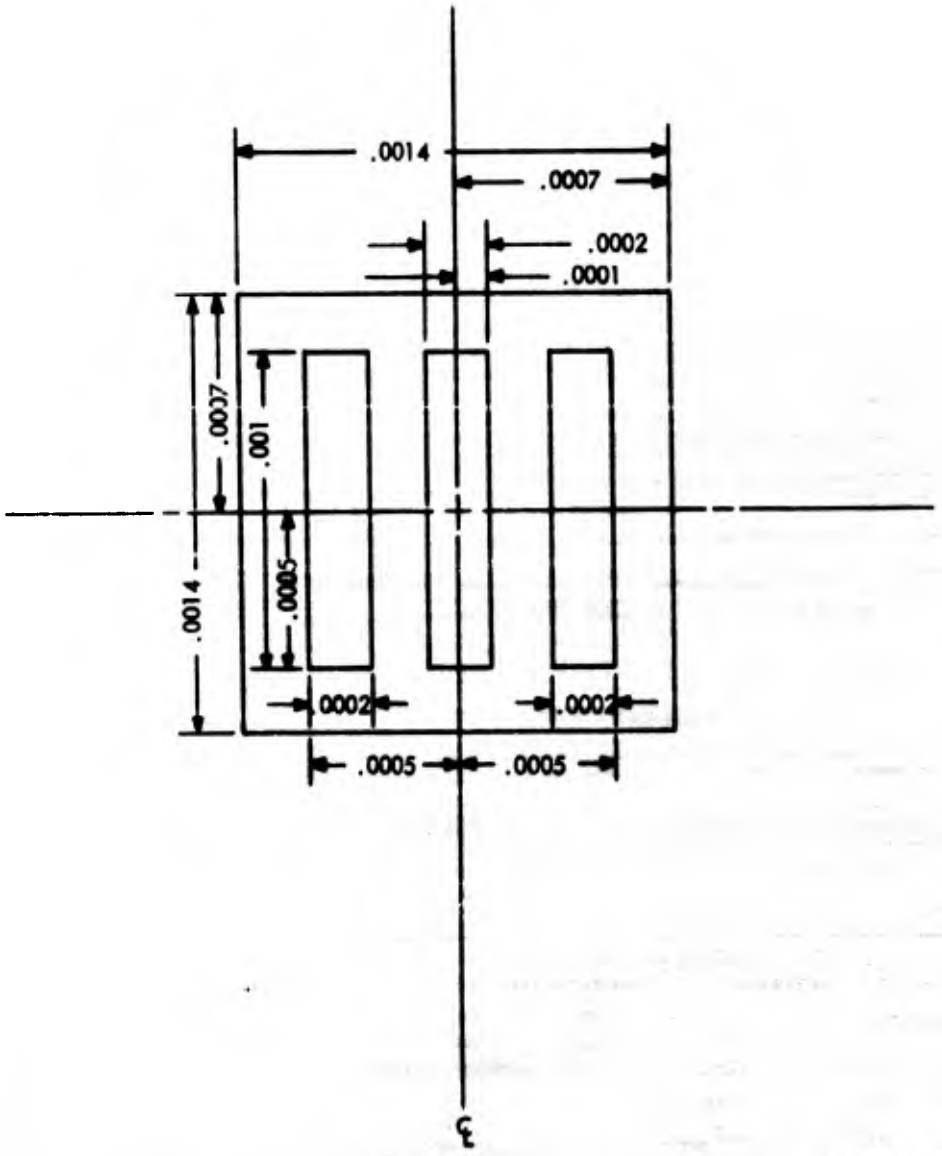


Fig. 57. Transistor Mask Dimensions

C. SWITCHING CIRCUIT

L-42 PNP SWITCHING CIRCUIT

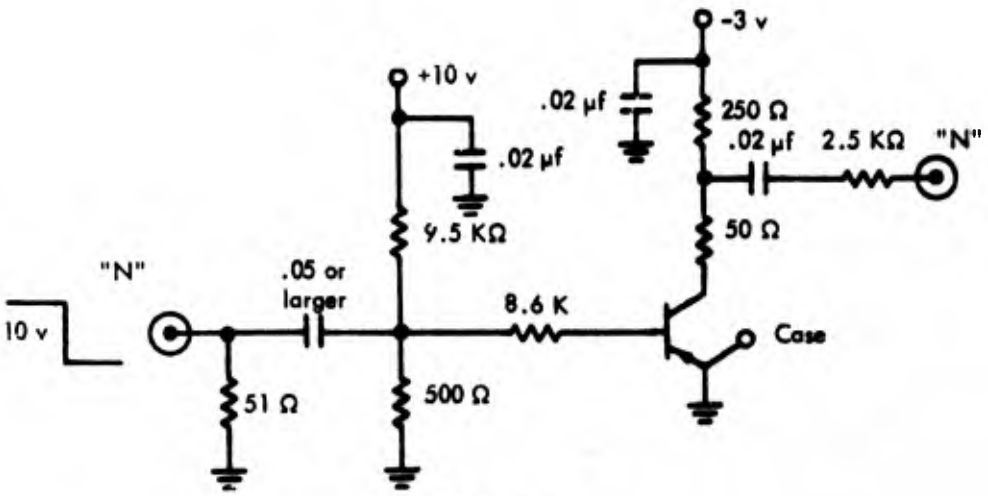


Figure 58. T_{ON}

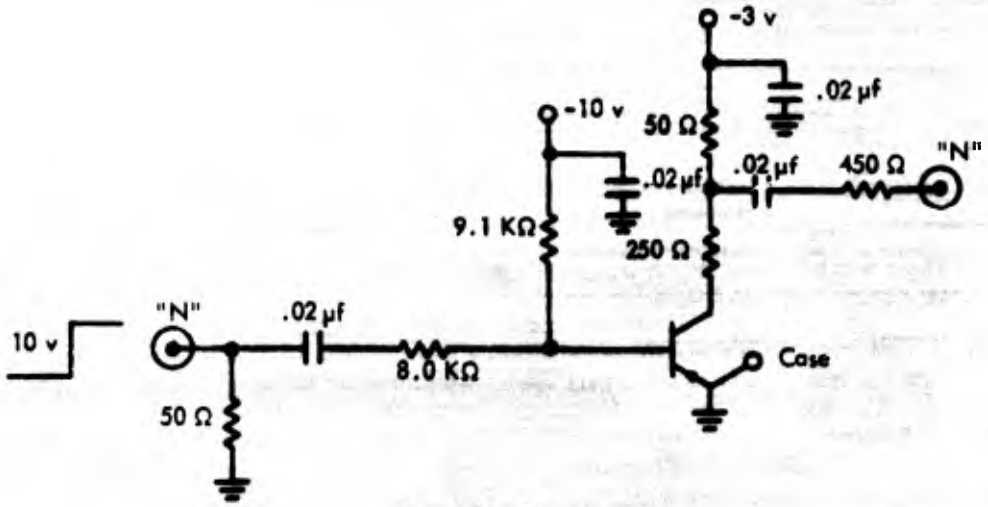


Figure 59. T_{OFF}

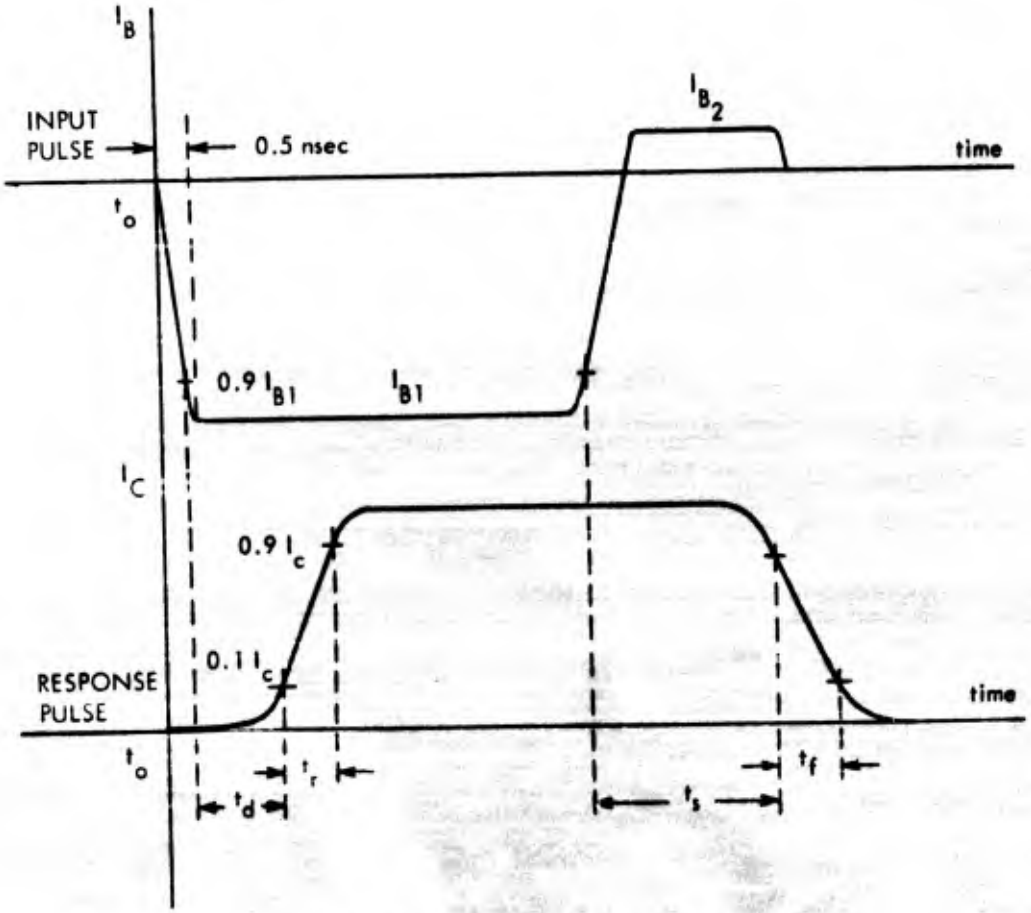


Fig. 60. Definition of Switching Times PNP

D. PNP SWITCHING TRANSISTOR PROCESS TABLE 19

1. Material preparation
2. Slice clean
3. Oxidation
4. Base KMER
5. Slice clean
6. Base deposition
7. Slice clean
8. Base diffusion
9. N^+ KMER
10. Slice Clean
11. N^+ deposition
12. Slice clean
13. Oxidation
14. Emitter KMER
15. Sample probe, BV_{CBO} (recommended)
16. Slice clean
17. Emitter deposition
18. Oxide etch
19. Reverse contact KMER
20. Sample probe BV_{CBO}, BV_{CEO}, BV_{EBO}, h_{FE} (recommended)
21. Slice clean
22. Contact evaporation - MoAu
23. Contact KMER
24. Sample probe BV_{CBO}, BV_{CEO}, BV_{EBO}, h_{FE}, V_{BE} (recommended)
25. 100% probe and ink, BV_{CEO} (recommended)
26. Lap and Scribe, clean after each
27. Break and sort
28. Inspect wafers
29. Clean header
30. Clean preform

31. Clean wafer
32. Alloy wafer to header
33. Wash unit (prebond)
34. Bond contacts
35. Inline test (recommended)
36. Bake
37. Varnish
38. Bake, vacuum
39. Bake
40. Bake, vacuum
41. Can weld
42. Stabilization bake
43. Cycle temperature
44. Centrifuge
45. VEECO
46. Pre-test, Clean
47. Final test
48. Symbolize
49. Reliability

E. EPITAXIAL MATERIAL SPECIFICATIONS

1. Crystal Material Table 20

Crystal boron doped in (111) growth direction

Crystal boron doped with resistivity range from 0.05 - 0.07 Ω-cm

Crystal diameter $1.000" \begin{bmatrix} +0.000" \\ -0.010" \end{bmatrix}$ centerless ground

Flat ground on (110) plane to ±2° with flat length of 0.25° ± 0.063

Crystal perfection be etch pit count less than 3000 per sq centimeter, no lineage, no slip, no star pattern

2. Substrate Slice Preparation Table 21

Slice sawed to expose (111) crystal plane ± 0.5°
Sawed slice 20.5 ± 0.5 mils thick
Slice lapped on both sides with 1800 grit aluminum oxide to 15.0 ± 0.5 mils
Substrate chemically polished with planar etch to 8.0 ± 0.5 mils. Cleaned substrate free of orange peel, bumps, scratches and haze

3. Epitaxial Film Table 22

Boron doped using diborane - film resistivity of 2.0 ± 0.2 Ω-cm
Film thickness of 5.0 ± 0.1 microns
Growth rate 2.0 ± 0.5 microns per minute
Growth temperature 1150°C

Etch prior to deposition with 5% by volume hydrogen chloride in hydrogen at 1270°C.

F. PNP DIFFUSION PROCESS TABLE 23

Process	Temperature (°C)	Time (minutes)	Dopant
Oxidation	1200 ± 1°C	30	Steam
	1st KMER-Base		
Base Deposition	800 ± 1°C	15	$POCl_3$
Base Diffusion	1100 ± 1°C	120	Wet O_2
	2nd KMER-Base Contact Stripes		
N^+ Deposition	1050 ± 1°C	3	$POCl_3$
Oxidation	950 ± 1°C	30	Steam
	3rd KMER - Emitter		
Emitter Deposition	1025 ± 1°C	35	BBr_3

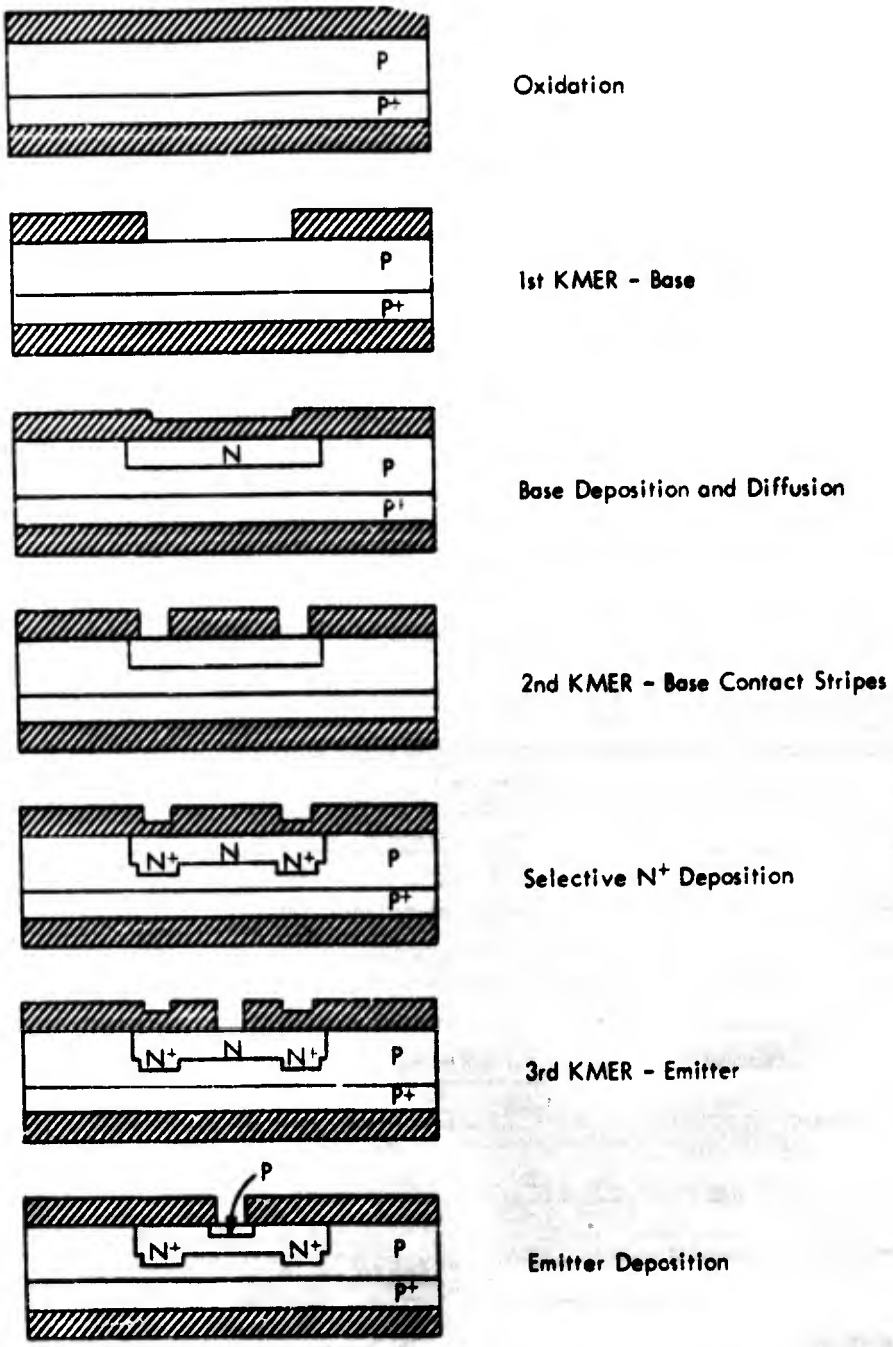


Fig. 61. PNP Process Steps

C. ASSEMBLY PROCEDURE PNP SWITCHING TRANSISTOR

1. Assembly Process Table 24

Step

a. Cleaned Slice
   Clean filaments
   Clean MoAu charges
b. MoAu Evaporation
c. Contact KMER
d. Slice Probe
e. Collector Etch
f. Scribe and Break
   Clean Headers
   Clean Preforms
g. Alloy
h. Chisel Bond
i. Wash Units (recommended)
j. Bake Units
k. Varnish Units
l. Vacuum Bake
m. Bake Units
n. Scope Inspect (recommended)
o. Inline Test (recommended)
p. Vacuum Bake
q. Can Weld

2. Collector Etch, Step e Table 25

Procedure

a. Measure and record slice thickness
b. Heat microscope slide until wax will melt and cover end of slide
c. Place slice, contacts down, on wax and seat. (Do not allow wax to flow

on back to slice or air bubbles to form around edges.)

d. Measure and record total thickness of mounted slice

e. Etch to 4-5 mils

f. Heat slice until wax melts and remove slice

g. Wash slice until all traces of wax are gone.

3. Scribe and Break, Step f Table 26

Procedure

a. Align and scribe 0.015 square

b. Ultrasonemate to break wafers apart

c. Rinse three times in hot DI H_2O

d. Dry in infrared oven 10 minutes

e. Separate inked rejects with magnet.

4. Alloy, Step g Table 27

Procedure

a. Place header on heater assembly

b. Place AuB preform on collector tab

c. Place wafer on preform and "scrub" until Au Silicon eutectic is formed

d. Remove unit and allow to cool.

5. Chisel Bond, Step h Table 28

Procedure

a. Place unit on heater assembly

b. Bond 0.7 gold wire

c. Bond first wire once to emitter pad and twice on top of emitter post

d. Bond second wire once on base pad and twice on top of base post.

SECTION IX
PERSONNEL

The following professional Personnel were actively engaged in work on the contract.

NAME	APPROXIMATE MAN-HOURS
S. S. Baird	35
J. W. Blair	353
J. A. Cunningham	269
C. F. Dennis	15
C. H. Douglas	172
J. E. Hall	471
L. G. Lands	1574
P. C. Nagle	714
F. W. Neal	54
F. J. Strieter	444
W. P. Waters	17
R. P. Williams	782

SECTION X
IDENTIFICATION OF PERSONNEL

Brief background descriptions of some of the personnel follow.

FREDERICK J. STRIETER

A. B. in Chemistry, Augustana College, Rock Island, Illinois, 1956
Ph. D. in Physical Chemistry, University of California, Berkeley, 1960

While at the University of California, Dr. Strieter was a teaching assistant in both Freshman Chemistry and Physical Chemistry. He was also a research assistant at the Lawrence Radiation Laboratory. His thesis, the Crystal Structure of Several Organic Molecules, was based on research done in X-ray crystallography. His main research interests were crystal structure studies, the use of computers in solving crystalographic problems, and structure determinations at low temperatures.

Dr. Strieter joined the Central Research Laboratories of Texas Instruments Incorporated in 1959. His initial assignment was the growth of single crystal Bi_2Te_3. Other areas of activity included studies in thermoelectric material technology, semiconductor metal contacts, diffusion in thermoelectric materials and fuel cell technology.

In 1962 Dr. Strieter transferred to the Semiconductor Research and Development Laboratory where his current responsiblity is manager of the device and surface projects section, diffusion technology for high frequency transistors. Among Dr. Strieter's current interests are the diffusion of impurities into silicon, current carrier lifetime control, p-n junction determination and silicon oxide studies.

Dr. Strieter has published papers in Acta Crystallographica, Journal of Chemical Physics and Journal of Advanced Energy Conversion.

PAUL C. NAGLE

B. S. in Physics, Rensselaer Polytechnic Institute
M.S. in Physics, Ohio State University

Mr. Nagle is a project engineer in the Semiconductor Research Laboratory where he is specially concerned with high speed logic switches. Having joined Texas Instruments in 1963, he was assigned to the Diffusion and Surface Technology group. His experience in this group was the diffusion process for amplifying and switching devices.

Member: Alpha Chi Rho

JOSEPH E. HALL

B. S. in Electrical Engineering, Southern Methodist University

Mr Hall has been employed by Texas Instruments since April, 1957. He is presently a project engineer in the Semiconductor Research and Development Laboratory, where he is engaged in the design and development of switching transistors. His previous work includes circuit development, transistor noise studies, and surface studies. Prior to joining Texas Instruments, Mr. Hall was employed by Collins Radio Co. and Chance Vought Aircraft.

LARRY G. LANDS

B. A. in Chemistry, Texas Christian University
M. S. in Chemistry, Texas Christian University

Mr. Lands joined Texas Instruments in 1960 and is now assigned to the Surface Technology Branch, Semiconductor Research and Development Laboratory. He is presently concerned with diffusion studies relating to high frequency, silicon switching transistors. Mr. Lands was associated with the Chemical Corps Biological Laboratory while on military leave from Texas Instruments. He has published in the Journal of Polymer Science.

Member: American Chemical Society

JAMES A. CUNNINGHAM

B. A. in Chemistry, University of Texas, 1957
M. A. in Physical Chemistry, University of Texas, 1958
Ph. D. in Inorganic Chemistry, University of Texas, 1961

Dr. Cunningham heads the High Frequency Device Fabrication section in the Semiconductor Research and Development Laboratory. He was formerly group leader in Surface Technology. Before joining Texas Instruments in 1961 he was employed at CONVAIR, Fort Worth, as an associate engineer in their Chemistry Laboratory. Dr. Cunningham has published in Journal of the Electrochemical Society.

Member: Phi Lambda Upsilon, Electrochemical Society

JOHN W. BLAIR

B. S. in Chemistry and Math, University of Arkansas
M. S. in Chemistry, University of Oklahoma

Mr. Blair has been employed by Texas Instruments since June of 1962 in the Materials Technology Branch of the Semiconductor Research and Development Laboratory. His work has been with problems associated with silicon epitaxy and with the materials aspect of device development programs. Prior to joining Texas Instruments he did research on an electrochemical method of water demineralization at Oklahoma Research Institute on a project supported by the Office of Saline Water. Mr. Blair has articles on chromatography and on electrochemical water demineralization.

Member: Alph Chi Sigma, Sigma Pi Sigma, Sigma Xi, American Chemical Society, Electrochemical Society

ROBERT P. WILLIAMS

B. S. in Chemistry, Texas Wesleyan University, 1952
Also attended Texas Technological College

Mr. Williams is currently engaged in semiconductor metal contact development in the Semiconductor Research and Development Laboratory. He joined Texas Instruments Research and Engineering Group on January 30, 1959, as an engineer to work on semiconductor surfaces. He was formerly employed as an associate chemist at Southwest Research Institute, San Antonio, Texas, from 1956 to 1959. From 1952 to 1956, he was a chemist with Texas Illinois Natural Gas Pipeline ompany at Joliet, Illinois.

Mr. Williams gave an oral presentation to the Electrochemical Society spring meeting, May, 1962, at Los Angeles. This paper was entitled "Results of High Temperature and Impressed Voltage on Transistor Devices."

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STEPHEN S. BAIRD

B. S. in Chemistry, Sul Ross State College, 1949
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Dr. Baird is currently in charge of Surface Technology in the Semiconductor Research and Development Laboratory. He joined Texas Instruments in 1958 as a member of the Analytical Chemistry Section of the Materials Research department and from 1959 to 1960 was manager of the Central Research Laboratories Silicon Transistor Reliability Project. Before coming to Texas Instruments, Dr. Baird was engaged in analytical methods development for the Research Department of Columbia-Southern Chemical Corporation at Corpus Christi, Texas, from 1954 to 1958. He was formerly with the Naval Powder Factory at Indian Head, Maryland, for two years. Dr. Baird has published in Talanta and Analytica Chimica Acta.

WARREN P. WATERS

B. S. in Physics, California Institute of Technology, 1949
M. S. in Physics, University of Southern California, 1954

Mr. Waters joined Texas Instruments Incorporated, Semiconductor-Components Division in 1962. Prior to his coming to TI, he was in charge of device development at Hughes Aircraft Company. There he developed germanium and silicon transistors, and fast recovery diodes. Mr. Waters has written many papers on the subject of semiconductor device development that have appeared in publications of IEEE.

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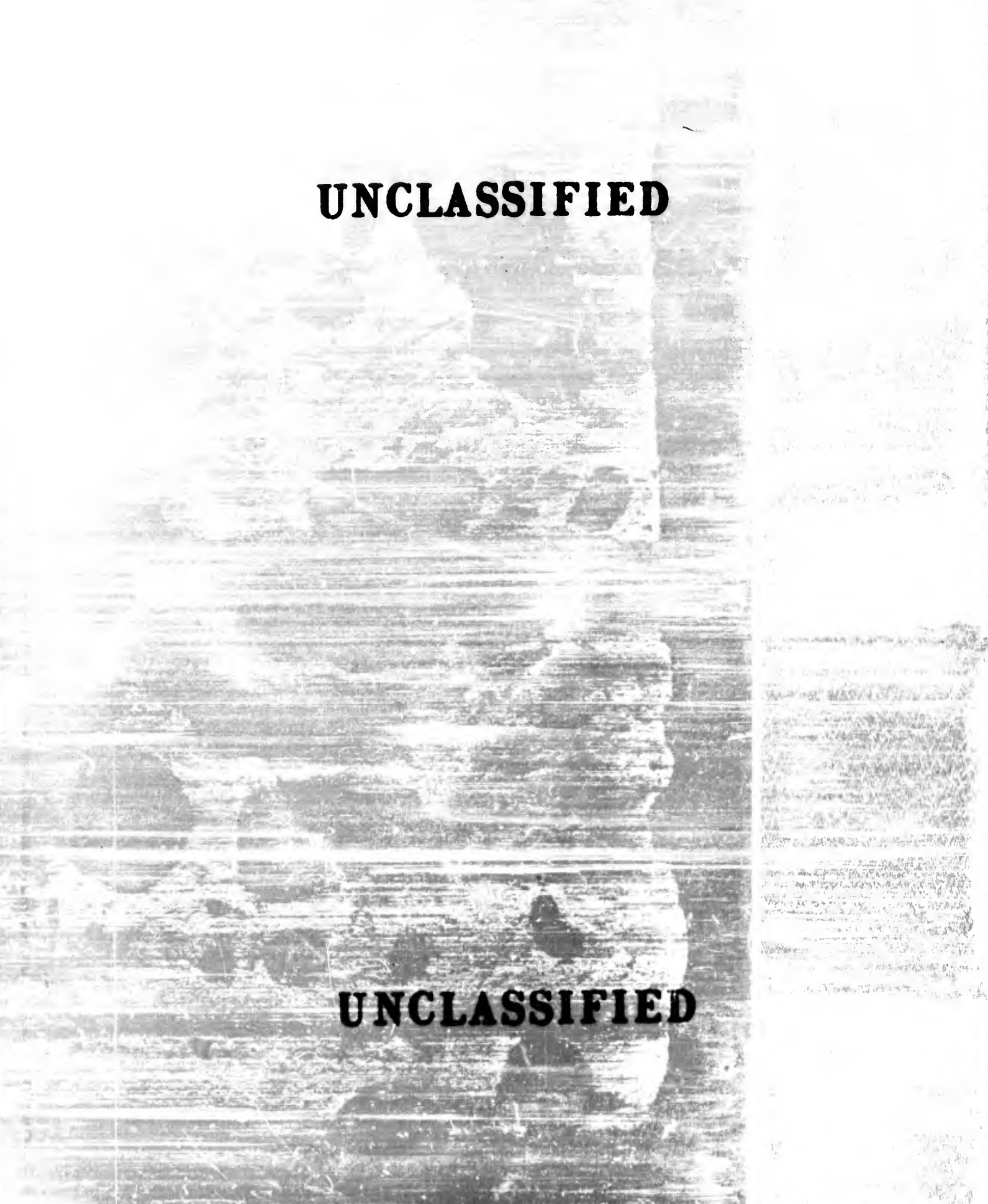

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