ELECTRICAL ENGINEERING DEPARTMENT
UNIVERSITY OF MINNESOTA
INSTITUTE OF TECHNOLOGY

Third Quarterly Report
February 1, 1964 through April 30, 1964

Study of Noise in Semiconductor Devices

Contract DA 36-039 AMC-03718 (E)
D.A. Proj. No. 10622001A056-0100

PLACED BY U. S. ARMY SIGNAL CORPS ENGINEERING LABORATORY
FORT MONMOUTH, NEW JERSEY

REGENTS OF THE UNIVERSITY OF MINNESOTA
MINNEAPOLIS, MINNESOTA

AD _____ Accession No. _____
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The object of this investigation is the study of noise in semiconductor devices and the theoretical interpretation of the results.

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A. van der Ziel, Chief Investigator

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I. Abstract

Equipment has been designed for measuring noise in FET's at low temperatures under pulsed conditions to avoid heating effects. The equipment is performing very satisfactorily.

Equipment is being designed for transistor noise measurements at v.h.f. and microwave frequencies.

Preparatory studies of noise in GaAs lasers are continuing.

The 1/f noise at 1000 cycles has been measured for various transistors as a function of temperature. Also noise measurements are being made on transistors that are life-tested at elevated temperatures.

Noise in unijunction transistors can to a certain extent be interpreted as being caused by drift of injected carriers in the region between the two base contacts. This is especially the case if the base-2 current is large in comparison with the emitter current.

Pulse noise measurements on FET's at liquid nitrogen temperatures reveal a white excess noise spectrum that is strongly affected by heating effects in the channel.

Noise measurements of enhancement mode FET's with insulated gate show a spectrum of the form const/$(1 + \omega^2\tau^2)$ with τ = 10 - 30 μ sec. This noise is attributed to traps. A higher frequences the noise is practically white, but it

is non-thermal. Various noise mechanisms seem to be present, and attempts are being made to sort them out.

A discussion of low frequency excess noise in FET's reveals that the present theoretical results cannot fully explain the data.

The (I_d,V_d) characteristic and the (g_m,V_g) characteristic of a diffused junction are calculated both for constant mobility and for a field-dependent mobility under the assumption of a linear impurity distribution in the junction.

The theory of thermal noise in an enhancement mode FET with insulated gate is developed. It is found that I_{eq} goes to zero if the device approaches saturation.

II. Purpose

The purpose of this report is to summarize the progress in the University of Minnesota Electrical Engineering Department during the period from February 1, 1964 to April 30, 1964 on Contract No. DA 36-039 AMC-03718(E).

The contract calls for an investigation to determine the cause and effect of the noise that occurs in semiconductor devices carrying dc current. It can be divided as follows:

(a) A study of noise in semiconductor devices such as e.g., junction diodes, junction transistors, field-effect transistors and similar devices.

(b) A study of the possible relationship between 1/f noise and reliability.

(c) A theoretical study in support of the experimental work.

III. Publications and Reports

Mr. Konrad Fischer, USAERDL representative, visited our laboratory during this period and discussed the research program.

The Third Monthly Report was submitted on March 2, 1964 and the Fourth Montly Report was submitted on April 1, 1964. The Second Quarterly report was submitted for approval on March 10, 1964.

The paper entitled:

"Small-Signal, High-Frequency Theory of Fiel.-Effect Transistors" by A. van der Ziel and J. W. Ero was published in the April, 1964 issue of the IEEE Transactions in Electron Devices (Vol. ED11, 128-135, April, 1964).

IV. Work Accomplished under the Program

A. Circuitry and Equipment

1. Pulse Measurement of FET Noise at Low Temperatures.

The measurement of the drain voltage dependence of the FET h.f. noise at 77°K, reported in the previous quarterly report, showed that the noise of a FET decreased appreciably with increasing drain bias voltage (V_d) in the saturation region. This noise was still of unknown origin, but it decreased very rapidly with increasing temperature. Because of this, the decrease in the FET noise with increasing V_d might be considered in the following way:

(Increase of V_d)→(Increase of the power dissipation in the channel)→(Temperature rise of the channel)→(Decrease of the noise).

To avoid the influence of such heating effects, the FET must be biased by a pulse for a short time and its noise must be measured within this time before the channel is heated. The pulse system described in the following paragraphs was built to measure noise by this method.

(a) General description of the system

Figure 1 shows the block diagram of the system for the pulse noise measurements. At present, the noise spectrum between 500 kc/s and 10 Mc/s can be measured by the drain bias pulse whose width ranges from 1 to 5 msec and whose repetition frequency is 40 c/s.

This system works in the following way. The pulse generator generates a train of positive pulses. The polarity of this pulse is inverted and amplified by a power amplifier. The negative power pulse thus obtained biases the N-channel FET from the source side. The terminal voltage of the FET is a superposition of the noise and the bias pulse voltages. This voltage is amplified by a preamplifier and then fed into a radio receiver (National Radio NC-125). Because the radio receiver is insensitive to low frequencies, the intermediate frequency output (455 kc/s) of the receiver is due to the FET noise and the harmonics of the bias pulse. The 455 kc output is subsequently amplified and then fed to a balanced gate amplifier. The gate amplifier operates in synchronization with the drain bias pulse such that it transfers the input signal to its output only when the FET is biased by pulse. The output of the balanced gate amplifier is then further amplified by a main amplifier and then fed to a quadratic detector through a cathode follower.

(b) Problems in the pulse measurement of noise

There are three problems to be considered:

(i) how to avoid the saturation of the preamplifier by large bias pulse applied to FET,

(ii) how to avoid the harmonics of bias pulse (such harmonics cannot be separated from the noise of FET),

(iii) how to calibrate the noise to obtain the equivalent noise diode current I_{eq}.

The solution to these problems was as follows:

(i) To avoid the saturation of the preamplifier, the FET was biased by the pulse from the source side as shown in Fig. 1 and Fig. 2a. The load impedance of the FET was a LC tank circuit tuned to the frequency at which the noise spectrum was measured (500 kc ~ 10 Mc/s). Because its resonant frequency was very high as compared with the pulse repetition frequency (40 c/s), this LC circuit presented a small impedance to the bias pulse and hence the pulse voltage developed across the tank circuit was very small and did not cause saturation of the preamplifier. The radio receiver (NC-125) following the preamplifier rejected the low frequency component due to the pulse so that no saturation occurred in the later stages.

(ii) There was no practical way to separate the noise of the FET from the high frequency harmonics of the drain bias pulse. Thus in this apparatus the noise spectrum was measured in the frequencies (500 kc ~ 10 Mc/s) which were substantially higher than the pulse repetition frequency (40 c/s). In the above frequency range, the harmonics of the bias pulse were very small as compared with the noise of FET and the measurements were successful.

(iii) Because the FET was biased only for a short time by the pulse, the noise must be measured and calibrated within this short time. To do this, the amplified noise voltage was

fed to the quadratic detector only when the FET was biased. This was done by means of the balanced gate amplifier operating in synchronization with the bias pulse as shown in Fig. 1 and Fig. 2b.

This technique allowed the calibration of noise by a noise diode connected in parallel to the FET.

(c) Details of the circuit

In this section, three important parts of the pulse noise measurement apparatus will be considered: (i) the jig for FET's, (ii) the balanced gate amplifier, (iii) the pulse generator and amplifier.

(i) The circuit of the jig for the FET is shown in Fig. 2a. The drain of the FET was connected to a LC tank circuit which was tuned to the frequency at which the noise spectrum was measured. The FET was biased from the source side by a pulse generator through a low-pass filter which eliminated unnecessary high frequency harmonics of the bias pulse (the time constant of the low-pass filter was such that the filter did not distort the pulse form). A floating gate bias supply was provided because the source side of the FET was not grounded.

(ii) The circuit of the balanced gate amplifier is shown in Fig. 2b. The balanced type circuit was used to avoid the occurrence of a large gate transient pulse. The control grids of the two push-pull sharp-cutoff pentodes (6AK5) were

biased to -6 V (cutoff region) in the absence of a gate pulse. When the FET is pulsed, the control grid voltage was raised approximately up to 0 V and the input signal was transferred to the output. Because the output frequency of the NC-125 receiver was 455 kc/s, the input and the output circuit of the gate amplifier was tuned to this frequency.

(iii) The circuit of the pulse generator and amplifier is shown in Fig. 3. A pulse generator of a gated beam tube 6BN6* (Fig. 3a) generated a pulse with the repetition frequency 40 c/s. The pulse width and its repetition frequency can be changed between 1 to 5 msec by changing the values of R and C in the limiter and the accelerator grid circuit of 6BN6. The negative pulse taken from the anode of 6BN6 was subsequently phase-inverted, and was fed to a cathode follower. A diode clipper circuit was provided at the output of the cathode follower to obtain a flat-topped pulse (Fig. 3b). This flat-topped positive pulse was used to drive the balanced gate amplifier. To obtain a power pulse to drive the FET, this pulse was further amplified and fed into a low impedance cathode follower (6Y6). A negative pulse whose maximum height was about 90 V was obtained at the output. Because an electrolytic capacitor of large capacity (200 μF) was used to couple the

*This circuit was invented by Prof. Koichi Shimoda, Department of Physics, University of Tokyo. See K. Shimoda, Electronics no Kiso, Shokabo, Tokyo (1964) pp. 230-231 (in Japanese).

final cathode follower to the FET through a pulse attenuator, a method to compensate for the dc leakage current of the electrolytic capacitor was provided together with the pulse attenuator (Fig. 3c).

This pulse measurement apparatus is now operating satisfactorily. Further improvement of this apparatus, especially the improvement of the accuracy by increasing the time constant of the detector, is now going on.

2. Noise on Transistors at VHF and Microwave Frequencies

The construction of equipment for measuring transistor noise at vhf and microwave frequencies has been continued during this period. Among the equipment built is a jig for mounting the transistor to be measured. The input and output impedance of this device is 50 ohm and tuning of the input and output is provided by a variable length shorted stub. The bias for the input and output junction is applied through the shorted stub.

For measurement of noise in lower frequencies up to 50 Mc/s a different biasing circuit has been built. For these frequencies the input and the output of the transistor is tuned by lumped tuned circuits.

In the frequency range between 50 Mc/s and 200 Mc/s the noise of the transistor stage under test drowned in the noise of the TV tuner used as a preamplifier. We are now building low noise preamplifiers for each channel.

Some low frequency noise measurements were made on the transistors supplied by the Signal Corps. Since the results of these measurements are not complete, they will be reported in the next quarterly report.

B. Measurements

1. Noise in GaAs Laser

It has been reported in previous quarterly reports about the noise measurement problems posed by pulsed operation of the GaAs laser. The first of these problems is that of background noise, which is always present, drowning out the laser noise, which is present only when the laser is turned on. A gating circuit has been devised which can be synchronized with the pulse driving the GaAs laser, and can turn off the background noise when the laser is off.

A second approach to the problem is that of attempting to operate the GaAs laser continuously. Figures 4 and 5 show very rough measurements of the current vs voltage characteristic of the laser at high forward currents, and of the power absorbed by the laser at these currents. Both curves refer to the laser cooled to liquid nitrogen temperature. If the laser were cooled to liquid helium temperatures, or even lower, the current threshold for lasing action should be reduced by a factor of 10 from the 20 amperes required for liquid nitrogen temperature. This reduction in threshold current will have an even greater effect on the power that must be dissapated by the laser. Our hope is that the lower

temperature will permit continuous action. But even an increased pulse length at a higher repetition rate would be a significant improvement.

Experiments using continuous operation of the laser must be carried out with great caution to avoid destruction of the laser.

2. 1/f Noise at 1000 Cycles and the Reliability of Transistors

More intensive measurement of the noise as a function of temperature was made for the Germanium transistor CK913. As shown in Fig. 6, the noise stays fairly constant until a certain critical temperature where the noise starts to increase rapidly.

The same kind of measurement was made for the silicon transistor 2N2808. It shows the same behavior (Fig. 7). The critical temperature of this kind of transistor can be seen from the figure to be higher than that of the above mentioned Germanium unit.

For unit #3 in Fig. 7 near 300° C, I_c failed to reach 1.0 mA (all other measurements were made at I_c = 1.0 mA) so that the noise was measured at I_c = 0.7 mA and was found to be below the expected value. Then a measurement of noise as a function of collector current was made on two different units, (Figs. 8 and 9). The noise was found to increase with increasing collector current. This suggests the dotted curve in Fig. 7 for unit #3.

Having estimated the critical temperature of silicon transistor 2N2808, two transistors with nearly the same $I_c - V_{cE}$ characteristic curve were heated up to the estimated critical temperature; namely, 280°C. Then a measurement of noise as a function of time was made. The noise of unit #6 stays fairly constant and has nearly the same value as that at room temperature (see Fig. 10). This suggests that 280°C is below the critical temperature for this unit. On the other hand, the noise of unit #5 (Fig. 11) is found to increase rapidly at 280°C as compared with the noise at room temperature. This suggests 280°C is either the critical temperature or above the critical temperature of unit #5. We see that critical temperatures are different even for the same type of transistors with very close $I_c - V_{cE}$ curve.

Further investigation on the cause of this difference in critical temperature will be carried on as well as the accelerated life test of the transistor.

3. Unijunction Transistors - Noise in the Negative Resistance Region

Under certain operating conditions the input impedancee between emitter and base-one is negative. This corresponds to the condition that I_{B2} is large compared to I_E.

For small I_E and large I_{B2}, the operation of the unijunction transistor can be understood in terms of a very simple model. It is assumed that the electric field in the base two region is constant and given by:

$$E_2 = \frac{I_{B2}}{A\, q\mu_p (p_o + bn_o)} \tag{1}$$

where $b = \mu_n/\mu_p$.

If the diffusion current is neglected, the continuity of hole and electron currents at the emitter yields:

$$q\, \mu_n\, n_o\, E_2 = q\, \mu_n (n_o + p' - p_o) E' \tag{2}$$

$$q\, \mu_p\, p_o\, E_2 + I_E/A = q\, \mu_p\, p'\, E' \tag{3}$$

Here E' and p' are the electric field and the hole concentration repsectively at the emitter. Solving for p' and E' we obtain:

$$E' = \frac{I_{B2} - I_E\,(bn_o + p_o)/(n_o - p_o)}{A\, q\mu_p (bn_o + p_o)} \tag{4}$$

$$p' = p_o + \frac{n_o\, I_E}{I_{B2}(n_o - p_o)/(p_o + bn_o) - I_E} \tag{5}$$

For extrinsic material; $n_o \gg p_o$ and (4) and (5) reduce to:

$$E' \simeq \frac{I_{B2} - bI_E}{A q\, \mu_p\, bn_o} \tag{6}$$

$$p' \simeq p_o + \frac{bn_o\, I_E}{I_{B2} - bI_E} \tag{7}$$

If the time required for the injected minority carriers to drift through the base is small compared to the minority carrier lifetime, then the electric field and the hole

concentration will be constant in the region between emitter and base one and will be given by (6) and (7).

For this case the noise can be calculated using the theory of Hill and van Vliet. They obtain the result:

$$S_p(f) = 4V\,P\tau_a\,\frac{2(1 - \cos\,\omega\tau_a)}{(\omega\tau_a)^2} \qquad (8)$$

Here $\tau_a \simeq \frac{L}{\mu_p E}$ = ambipolar drift time

p = hole concentration

V = volume

This can also be written as:

$$S_p(f) = 2V\,p\tau_a \cdot \left[\frac{\sin(\omega\tau_a/2)}{(\omega\tau_a/2)}\right]^2 \qquad (9)$$

Since:

$$S_I(f) = \left(\frac{I}{bn_o V}\right)^2 S_p(f) \qquad (10)$$

$$S_I(f) = \frac{2V\,p\tau_a I^2}{(bn_o V)^2} \cdot \left[\frac{\sin(\omega\tau_a/2)}{(\omega\tau_a/2)}\right]^2 \qquad (11)$$

Then substituting into (11) the following:

$$p = p' \simeq \frac{bn_o I_E}{I_{B2} - bI_E} \qquad (12)$$

$$\tau_a = \frac{L}{\mu_p E'} = \frac{q\,bn_o V}{(I_{B2} - bI_E)} \qquad (13)$$

$$I = I_{B2} + I_E \qquad (14)$$

We obtain:

$$S_I(f) = 2q\left(\frac{I_{B2} + I_E}{I_{B2} - bI_E}\right)^2 I_E \cdot \left[\frac{\sin(\omega\tau_a/2)}{(\omega\tau_a/2)}\right]^2 \qquad (15)$$

But for $I_{B2} \gg I_E$, this becomes

$$S_I(f) \simeq 2q\, I_E\left[\frac{\sin\,\omega\tau_a/2}{\omega\tau_a/2}\right]^2 \qquad (16)$$

Let

$$S_I(f) = 2q\, I_{eq} \qquad (17)$$

Then

$$I_{eq} \simeq I_e \cdot \left[\frac{\sin(\omega\tau_a/2)}{(\omega\tau_a/2)}\right]^2 \qquad (18)$$

By examining Eq. (18), it can be seen that the spectral intensity should depend linearily on I_E and should be independent of I_{B2}. Moreover since τ_a depends inversely on I_{B2}, the frequency at which the noise begins to decrease should depend linearily on I_{B2}.

Figure 12 shows a plot of I_{eq} measured across $B_1 - B_2$ as a function of I_E at 25 kc. The noise measured across $B_1 - B_2$ with $I_E = 0$ has been substracted. This means that part of the thermal and excess noise has been substracted. This is permissible only if the excess noise is uncorrelated with the generation-recombination noise. From Fig. 12 it appears that I_{eq} depends linearily on I_E from 10 μa to 200 μa. The magnitude of I_{eq} is slightly greater than I_E.

Figure 13 shows a plot of I_{eq} as a function of I_{B2} at 25 kc. Note that in the region $I_{B2} \gg I_E$, the noise is almost independent of I_{B2}. The agreement is best for very small I_E. For $I_{B2} \ll I_E$, the noise is essentially that associated with the diode.

Figure 14 shows the spectrum of I_{eq} for three different values of I_{B2}. If we define $\omega_a = 1/\tau_a$, it can be seen that ω_a depends heavily on I_{B2} as expected. However, the spectrum does not show the characteristic $\left(\frac{\sin x}{x}\right)^2$ dependence at high frequencies. This may be partly caused by the fact that the thermal noise level is appreciable compared to the generation-recombination noise level. It also could be caused by the geometry of the device. All the formulas used were derived on the basis of a one-dimensional geometry. In the device used, the length of the region from emitter to base one was only about twice the width of the base region. This may mean that the distances the individual carries drift are quite different. Thus, τ_a will be different for each carrier. This could cause a smoothing of the characteristic "bumps" in the $\left(\frac{\sin x}{x}\right)^2$ function.

4. Pulse Measurements of Noise at Low Temperatures

The system for pulse noise measurements described before was used to measure the drain voltage dependence of FET noise, I_{eq}, at 77°K. The FET measured was Crystalonics #2 which showed a white noise spectrum for frequencies between

50 kc/s and 8 Mc/s at 77°K. The results of dc measurements were reported in the previous quarterly report.

Figure 15 shows the result. Measurements were made for V_g = 0 and -3 volts. The remarkable point is that the results of pulse and dc measurements are considerably different from each other. For small drain voltages, these two methods give the same I_{eq}. However, for $V_d > 2$ volt, I_{eq} measured by the pulse method is larger than that measured by the dc method. Also the peak of the curve shifts toward higher drain voltages.

This result shows that a considerable heating effect of the channel occurs at low temperature measurements. As discussed in the section on equipment, the channel is less heated by the pulse method than the dc method, and hence higher I_{eq} values are obtained.

This result indicates that the pulse method must be used for an accurate measurement at low temperatures. This suggests considerable technical problems at low frequencies. A preliminary attempt to extend the measurements to low frequencies is now going on.

5. The Enhancement Mode FET

(a) Measurements

Measurements on two RCA enhancement mode FET's of silicon were made during this quarter. These FET's showed dc drain characteristics similar to those of ordinary FET's if the gates were biased positively a few volts.

Their transconductances in saturation (g_m) and zero voltage drain conductances (g_{do}) vary with gate voltage as shown in Fig. 16.

The noise spectra in saturation region are shown in Fig. 17 (between 1 and 800 kc/s) and in Fig. 18 (between 0.8 Mc to 22 Mc/s). The low frequency noise spectra are of the generation-recombination type whose characteristic frequencies are approximately 10 kc/s. For frequencies between 3 Mc/s and 15 Mc/s the spectra are essentially white. Above 15 Mc/s, a slight increase in the noise spectra with frequency is observed. Figure 19 shows the dependence of I_{eq} on the drain voltage (V_d) at 5.5 Mc/s. As is seen in Fig. 18, the noise spectra are white around this frequency. For gate voltages between 1.5 and 3 volts, $I_{eq}(V_d)$ decreases slightly with increasing V_d (for small V_d). This noise is the thermal noise of g_{do}.

If V_d is increased further, the noise increases sharply and finally approaches to another constant value when $V_d = V_g$ ($V_{d(sat)} = V_g$ is the drain saturation voltage). This voltage is indicated by arrow marks in Fig. 19. This sharp rise of $I_{eq}(V_d)$ occurs approximately $V_o = \frac{1}{3} V_g$. If V_d is increased further beyond saturation, I_{eq} increases again because of the breakdown noise of the insulator (gate leakage current appears). For V_g larger than 4 V, $I_{eq}(0)$ is considerably higher than the thermal noise level of g_{do}.

$I_{eq}(V_d)$ decreases quite rapidly with increasing V_d (for small V_d) as shown in Fig. 20. This indicates that a new noise mechanism occurs for small V_d. Because this noise becomes prominent for high gate voltages and decreases rapidly when the drain voltage is applied, this noise may be due to some breakdown mechanism sensitive to the relative voltage between the channel and gate. In Fig. 20, the drain voltage for zero drain current is not zero. The arrow mark indicate such points.

Figure 21 shows the plots of $I_{eq}(0)$ vs $\frac{2kT}{e} g_{do}$. Both of $I_{eq}(0)$ and g_{do} are the functions of V_g. The points on the curves are taken by changing V_g. The straight line shows the thermal noise level. This figure shows that for medium gate voltages $I_{eq}(0)$ is higher than the thermal noise level by only 20 ~ 30%. Thus this noise is considered to be a thermal noise. For lower and higher gate voltages, $I_{eq}(0)$ is much higher than the thermal noise level. The peculiar drain voltage dependence of the excess noise that occurs for large V_g was shown in Fig. 19. The nature of the excess noise that occurs for small V_g is not known.

(b) Classification of the noise of enhancement mode FET

Based on the experimental results discussed before, the noise of the enhancement mode FET can be classified into five kinds. To make the classification clear, the noise of

the device is regarded as a function of V_d and V_g. The following table gives the regions where each kind of noise is important.

Table 1

V_g \ V_d	0	Near Saturation	Beyond Saturation
small	III	IV*	V
medium	I*		
large	II		

*Essential noises of the enhancement mode FET.

These noises are explained briefly in the following.

The noise of the Ist kind is the thermal noise of g_{do}. Actually the measured I_{eq} is about 20 ~ 30% higher than the thermal noise. This is probably due to the noise of the IInd and IIIrd kind, which is not exactly zero in this region. The properties of this noise will be analyzed in the theory section (Cs).

The Noise of the IInd kind is characterized by a strong decrease of noise when small drain bias is applied. This noise is probably due to some kind of leakage between the gate and channel because this noise occurs only for large gate voltages.

The noise of the IIIrd kind appears for small V_g. Its nature is not known yet.

The noise of the IVth kind appears in the saturation region. This noise has a white spectrum above 3 Mc/s. As one possibility, this noise may be regarded as a suppressed shot noise. If this is true, its suppression factor at the saturation is about 0.25.

The noise of the Vth kind is due to the breakdown of the insulator by high drain voltages. This noise is accompanied with a gate leakage current.

Only the noises of the Ist, IIIrd and IVth kinds are essential to the enhancement mode FET because all the other noises are more or less related to the breakdown of the insulator.

6. Excess Noise in FET's

In an attempt to investigate further the origin of the excess noise in FET's, we have first tried to better understand the dc operation. In previous reports, the theoretical approaches have been presented for the alloy junction units using an abrupt junction model. These approaches considered a field dependent mobility and a combination of a constant and field dependent mobility for particular regions of the $I_d - V_d$ characteristics. However, since several units under investigation are diffused junction FET's, an approximate model in this case might be to assume a linear profile for the charge distribution at the gate junction. In the

theory section of this report, this model is used to calculate the dc characteristics both for a constant mobility and a field dependent mobility.

If we now make a comparison between the experimental results and those found theoretically, it becomes apparent that a combination of factors must be taken into account if the $I_d - V_d$ characteristics are to be explained for a particular FET. The first of these appears to be whether or not the device is an abrupt (alloy) junction device or a gradual (diffused) junction device. As illustrated on Fig. 23, the effect of the latter consideration appears to make the initial slope of the $I_d - V_d$ characteristic more nearly linear. However, a second effect to be included is the presence of a field dependent mobility. As was reported previously, the effect of this consideration appears to increase the initial slope and provide a sharper pinch-off. From the experimental results, it appears that these two effects are the most significant factors contributing to the $I_d - V_d$ characteristics deviation from those suggested originally by Shockley. In some instances, there still remains some discrepency between theory and experiment but because the construction may be non-uniform, it may be necessary to represent a FET by two equivalent FET's in parallel with different cutoff potentials. Thus to completely match the experimental $I_d - V_d$ characteristics, these three factors must be considered, making a

general theoretical expression for the characteristics of all FET's virtually impossible. However, in each particular case, by comparing the $I_d - V_d$ characteristics found experimentally with those found theoretically, at least some idea can be made concerning the mechanisms contributing to the dc operations.

Also of significant interest is the dc behavior of an FET, biased in saturation, for varying gate voltages. On Fig. 24 the results of several theoretical approaches for g_m/g_{mo} vs V_g/V_{go} are presented, but such results, while giving reasonable agreement with experiments for low gate voltages for some units, do not account for the experimental data for all cases for high and low gate voltages. A preliminary investigation of a plot of I_d/g_m vs V_g suggests a dependence of the current on the gate voltage given by

$$I_d/I_{do} = (1 - V_g/V_{go})^n$$

where apparently n is a rational number (in most cases n = 3/2, 2, or 4). However, as the limiting condition $V_g \rightarrow V_{go}$ is reached, this expression fails to agree with the experimental results. A point of ambiguity is in the choice of V_{go} and actually a modified exponential dependence may be a more accurate estimate. Thus before the noise as a function of gate voltage could be discussed, it is necessary to better understand what is happening with the channel in pinch off condition. Without giving any experimental comparisons at

this time, it should merely be mentioned that there appears to be an indication that the edge of the depletion region can not be considered as an abrupt transition or equivalently that the depletion region is not entirely void of carriers.

Apparently this effect is of second order for most cases when the FET is in saturation, until the gate voltage is such that the characteristics are altered. At this time the exact processes involved are not clearly understood and careful investigation is now being undertaken to find the correct theoretical approach. It is hoped that through this investigation that the actual noise processes contributing in each mode of operation of an FET will be more completely understood.

C. Theory

1. Linear Profile Approximation for a Diffused Junction, P-Channel FET

(a) Constant mobility; $I_d - V_d$ and g_m vs V_g characteristics.

Consider now the carrier concentration in a FET shown in Fig. 22a such that the charge density in the depletion region at any point y may be represented by:

$$\rho(y) = - \rho_o(1 - y/a) \qquad y > b$$

where y is the distance from the center of the p-region.

Now letting $E_y(y)$ be the electric field and V(y) the electrostatic potential in the depletion region, Poisson's equation becomes:

$$k\epsilon_o \frac{d^2V}{dy^2} = - k\epsilon_o \frac{dE_y}{dy} = - \rho(y)$$

Thus

$$\frac{dE_y}{dy} = \rho/k\epsilon_o = - \rho_o(1 - y/a) \qquad y > b$$

Now using the boundary conditions $E_y = 0$ for $y \leq b$ and $y \geq 2a-b$, the electric field becomes

$$E_{y1} = \frac{-\rho_o}{k\epsilon_o} \left[(y - b) - \frac{1}{2a} (y - b)^2\right] \qquad \text{for} \quad b < y < a$$

$$E_{y2} = \frac{-\rho_o}{k\epsilon_o} \left\{\left[(a - b) - \frac{1}{2a} (a - b)^2\right] - \left[(2a - y) - \frac{1}{2a} (2a-y)^2\right]\right\}$$

$$\text{for} \quad a < y < 2a - b$$

Now using $V = - \int E_y \, dy$ and for the total potential V across the depletion region, $V = V_1 + V_2$ where the voltages V_1 and V_2 are for the regions $b < y < a$ and $a < y < 2a - b$ respectively, then since $V = 2V_1$ we have

$$V = -2 \int_a^y E_{y1} dy$$

Thus

$$V = \frac{2\rho_o}{k\epsilon_o} \left[\frac{1}{2} \left\{(y - b)^2 - (a - b)^2\right\} - \frac{1}{6a} \left\{(y - b)^3 - (a - b)^3\right\}\right]$$

Then at $y = b$, the edge of the depletion region,

$$V(b) = -\frac{\rho_o a^2}{k\epsilon_o}\left[(1 - b/a)^2 - \frac{1}{3}(1 - b/a)^3\right]$$

or after simplification and taking the potential $W > 0$ to be the reverse bias we have

$$W = -V(b) = W_o\left(1 - \frac{3}{2}\frac{b}{a} + \frac{1}{2}\frac{b^3}{a^3}\right) \qquad (1)$$

$$\text{where } W_o = \frac{2}{3}\left(\frac{\rho_o a^2}{k\epsilon_o}\right)$$

V(y) and E(y) are shown on Figs. 22b and 22c respectively.

Now the current in the channel is given by

$$I = g(W)\frac{dW}{dx} \qquad (2)$$

where g(W), the channel conductance, for the model being considered is given by

$$g(W) = \frac{1}{2} q\mu N_{do}\left[1 - (a - b)/a\right] bw$$

where we will now take $\mu = \mu_p$, a constant. Thus,

$$g(W) = 2g_o\left[1 - \frac{1}{2}\frac{b}{a}\right]\frac{b}{a}$$

where

$$g_o = 2\sigma_o a = \frac{1}{2} q\mu_o N_{do} aw$$

Now rewriting Eq. (1) we have

$$\frac{b^3}{a^3} - 3\frac{b}{a} + 2(1 - W/W_o) = 0$$

This is a cubic equation in (b/a) and thus mathematically has three possible solutions. For this particular equation a trigonometric solution is possible[1] and coupling with the boundary conditions

$$(b/a) \rightarrow 1 \quad \text{as} \quad W \rightarrow 0$$

$$(b/a) \rightarrow 0 \quad \text{as} \quad W \rightarrow W_o$$

the only solution permissible is then

$$(b/a) = - 2\cos(\alpha/3 + 60°)$$

$$\text{where } \cos\alpha = - (1 - W/W_o)$$

Thus substituting in Eq. (3) for (b/a) we have

$$g(W) = - 4g_o \left[1 + \cos(\alpha/3 + 60°)\right] \cos(\alpha/3 + 60°) \quad (4)$$

$$\text{for} \quad \cos\alpha = - (1 - W/W_o)$$

(1) Drain characteristics

From Eq. (2) integrating over the length of the channel we have

$$I_o L = \int_{W_s}^{W_d} g(W)\, dW \quad (5)$$

or in terms of the trigonometric parameter α,

[1] Mathematical Handbook for Scientists and Engineers, Korn and Korn:, McGraw Hill Co., 1961, p.23.

$$I_o L = - W_o \int_{\cos^{-1}(W_s/W_o - 1)}^{\cos^{-1}(W_d/W_o - 1)} \sin\alpha \, g(\alpha) \, d\alpha$$

Then introducing the physical constraints ($I_o = I_d$)

$$I_d = 0 \quad \text{if} \quad W_s = W_d = 0$$

$$I_d = I_{d_{SAT}} \quad \text{if} \quad W_s = 0, \; W_d = W_o$$

$$I_d > 0 \quad \text{for} \quad W_d > 0 \quad \text{for a p-channel FET}$$

we then have

$$\frac{I_d L}{g_o W_o} = \left\{ 2.05 - \left[2\cos\alpha_d - \frac{3}{10}\left(\cos\tfrac{5}{3}\alpha_d + \sqrt{3}\sin\tfrac{5}{3}\alpha_d\right) \right.\right.$$

$$+ \frac{3}{4}\left(\cos\tfrac{4}{3}\alpha_d - \sqrt{3}\sin\tfrac{4}{3}\alpha_d\right)$$

$$\left.\left. + \frac{3}{2}\left(\cos\tfrac{2}{3}\alpha_d + \sqrt{3}\sin\tfrac{2}{3}\alpha_d\right) - \frac{3}{2}\left(\cos\frac{\alpha_d}{3} - \sqrt{3}\sin\frac{\alpha_d}{3}\right) \right] \right\}$$

for $W_s = 0$ and $180° \geqq \alpha_d \geqq 90°$ for $0 \leqq W_d/W_o \leqq 1$

The results of this formula, taking $I_{do} = I_{d_{SAT}} = g_o W_o/L$, compared to the abrupt junction result given by Schockley is shown on Fig. 23. It may be noted that the effect is to decrease the initial slope, finally reaching the same limit in slope near saturation.

(2) Transconductance

Consider now Eq. (4) for the current in the channel where it should be noted that

$$W_d = V_g + V_{dif} - V_d$$

$$W_s = V_g + V_{dif}$$

Now the transconductance is given by

$$g_m = - \frac{\partial I_d}{\partial V_g}$$

so that assuming I_d is continuous and differentiable, we have using Eq. (4),

$$g_m = \frac{4g_o}{L}\left\{\left[1 + \cos(\alpha_d/3 + 60°)\right] \cos(\alpha_d/3 + 60°) - \left[1 + \cos(\alpha_s/3 + 60°)\right] \cos(\alpha_s/3 + 60°)\right\}$$

where

$$\cos \alpha_d = - (1 - W_d/W_o), \quad \cos \alpha_s = - (1 - W_s/W_o)$$

Considering now $W_d/W_o = 1$, i.e., the FET is in saturation, then

$$g_m = - \frac{4g_o}{L}\left[1 + \cos(\alpha_s/3 + 60°)\right] \cos(\alpha_s/3 + 60°)$$

where $\cos \alpha_s = -(1 - W_s/W_o)$ and

for $0 \leqq W_s/W_o \leqq 1$, $180° \geqq \alpha_s \geqq 90°$

The results of this calculation compared to (1) Shockley's results, (2) Dacey and Ross[1] field dependent mobility results, and (3) a mobility dependence

$$\mu = \begin{cases} \mu_o , & W < W_o \\ \mu_o (E_c/E)^{1/2} , & W > W_o \end{cases}$$

is presented on Fig. 24, neglecting the diffusion potential (V_{dif}). From this normalized plot the most significant result appears to be that the initial slope is significantly decreased, perhaps reflecting the predominant effect of spreading the depletion region back toward the gate for low gate voltages for this model.

(b) Field dependent mobility; g_m vs $I_d(V_g)$ characteristics

Now it has been found for the linear profile approximation for the gradual junction FET that the channel conductance is given by

$$g(W) = -4g_o \left[1 + \cos(\alpha/3 + 60°)\right] \cos(\alpha/3 + 60°)$$

$$\text{where } \cos\alpha = -(1 - W/W_o)$$

$$\text{and } g_o = \tfrac{1}{2} q\mu N_{do} aw$$

Suppose now that the mobility is field dependent such that $\mu = \mu_o(E_c/E)^{1/2}$ where E is the electric field. Then

$$g_o = \frac{1}{2} q(E_o)^{1/2} \mu_o N_{do} aw\left(\frac{1}{E}\right)^{1/2}$$

or

$$g_o = \frac{1}{2} q(E_o)^{1/2} \mu_o N_{do} aw\left(\frac{dx}{dW}\right)^{1/2}$$

Now using the definition for the current in the channel

$$I = g(W) \frac{dW}{dx}$$

we have

$$I_o^2 dx = (4g_o')^2 \left\{ \left[1 + \cos(\alpha/3+60°) \right] \cos(\alpha/3+60°) \right\}^2 dW$$

where

$$g_o' = \frac{1}{2} q(E_o)^{1/2} \mu_o N_{do} aw$$

If we then integrate over the length of the channel for a fixed current $I_o = I_d$, we then find

$$I_d^2 L = (4g_o')^2 \int_{W_s}^{W_d} \left\{ \left[1-\cos(\alpha/3+60°) \right] \cos(\alpha/3+60°) \right\}^2 dW \qquad (1)$$

(1) Transconductance

Now using the definition of the transconductance $g_m = - \frac{\partial I_d}{\partial Vg}$ and using the definitions of W_d and W_s, we have after some manipulation

$$g_m = - \frac{(4g_o')^2}{2I_d} \left\{ \left[1 + \cos(\alpha_d/3+60°) \right]^2 \left[\cos(\alpha_d/3+60°) \right]^2 - \left[1 + \cos(\alpha_s/3+60°) \right]^2 \left[\cos(\alpha_s/3+60°) \right]^2 \right\}_{(2)}$$

$$\cos \alpha_d = -(1 - W_d/W_o) \quad ; \quad \cos \alpha_s = -(1 - W_s/W_o)$$

(2) DC characteristics

Now returning to a consideration of Eq. (1) and using

$$\cos\alpha = -(1 - W/W_o)$$

such that

$$dW = - W_o \sin \alpha \, d\alpha$$

Then

$$I_d{}^2 L = - (4g_o')^2 W_{oo} \int_{\cos^{-1}(W_s/W_o - 1)}^{\cos^{-1}(W_d/W_o - 1)} \sin \alpha \, g_1(\alpha) \, d\alpha$$

where

$$g_1(\alpha) = \left\{ \left[1 + \cos(\alpha/3 + 60°) \right] \cos(\alpha/3 + 60°) \right\}^2$$

Thus expanding sin α $g_1(\alpha)$ and after considerable manipulation and utilisation of trigonometric identities, we obtain upon integration:

$$\frac{I_d^2 L}{(4g_o')^2 W_{oo}} = \frac{1}{4}\left\{\frac{3}{56}\left(\sqrt{3}\sin\frac{7}{3}\alpha - \cos\frac{7}{3}\alpha\right) - \frac{1}{2}\cos 2\alpha\right.$$

$$- \frac{3}{5}\left(\sqrt{3}\sin\frac{5\alpha}{3} + \cos\frac{5}{3}\alpha\right) - \frac{9}{8}\left(\sqrt{3}\sin\frac{4}{3}\alpha - \cos\frac{4}{3}\alpha\right)$$

$$\left. + \frac{7}{2}\cos\alpha + \frac{9}{4}\left(\sqrt{3}\sin\frac{2\alpha}{3} + \cos\frac{2\alpha}{3}\right) + \frac{21}{8}\left(\sqrt{3}\sin\frac{\alpha}{3} - \cos\frac{\alpha}{3}\right)\right|_{\alpha_s}^{\alpha_d}$$

where

$$\cos\alpha_d = -(1 - W_d/W_o); \quad \cos\alpha_s = -(1 - W_s/W_o)$$

If we take $W_d = W_o$ for saturation so that $\alpha_d = 90°$, we then have

$$I_d^2 = I_{do}^2 \left\{2.75 + \frac{3}{56}\left(\cos\frac{7}{3}\alpha_s - \sqrt{3}\sin\frac{7}{3}\alpha_s\right) + \frac{1}{2}\cos 2\alpha_s\right.$$

$$+ \frac{3}{5}\left(\sqrt{3}\sin\frac{5}{3}\alpha_s + \cos\frac{5}{3}\alpha_s\right) - \frac{9}{8}\left(\cos\frac{4}{3}\alpha_s - \sqrt{3}\sin\frac{4}{3}\alpha_s\right)$$

$$\left. - \frac{7}{2}\cos\alpha_s - \frac{9}{4}\left(\cos\frac{2\alpha_s}{3} + \sqrt{3}\sin\frac{2}{3}\alpha_s\right) + \frac{21}{8}\left(\cos\frac{\alpha_s}{3} - \sqrt{3}\sin\frac{\alpha_s}{3}\right)\right. \tag{3}$$

for

$$I_{do}^2 = \frac{4 W_{oo}(g_o')^2}{L}$$

$$\cos\alpha_s = -(1 - W_s/W_{oo}), \quad 180° \geqq \alpha_s \geqq 90°$$

If we now return to the transconductance given by Eq. (2) and considering $W_d = W_o$ we thus finally obtain:

$$g_m(V_g) = \frac{(4g_o')^2}{4I_d}\left\{1.75 - \cos\alpha_s - \frac{3}{2}\left(\sqrt{3}\sin\frac{\alpha_s}{3} - \cos\frac{\alpha_s}{3}\right)\right.$$
$$\left. - \left(\sqrt{3}\sin\frac{2\alpha_s}{3} + \cos\frac{2\alpha_s}{3}\right) + \frac{1}{8}\left(\sqrt{3}\sin\frac{4\alpha_s}{3} - \cos\frac{4\alpha_s}{3}\right)\right\}$$

where

$$\cos\alpha_s = -(1 - W_s/W_o) \quad ,$$

$$\text{for } 0 \leqq W_s/W_o \leqq 1, \quad 180^\circ \geqq \alpha_s \geqq 90^\circ$$

These results are presented on Fig. 25 together with the constant mobility, linear profile approximation, and the results of Shockley and Dacey and Ross. Here it may be noted that the effect is to decrease the initial slope but the final slope is the same as in the constant and field dependent mobility cases of Shockley and Dacey and Ross, respectively.

2. Theory of Thermal Noise of an Enhancement FET

The noise of the Ist kind is a thermal noise of the induced carriers in the channel. Thus the property of this noise must be analyzed by taking into account the channel modulation effects as in the case of ordinary FET's. In this paragraph, the characteristic quantities of the enhancement mode FET are calculated based on the model of H. Borkan and P. K. Weimer and then the theory of the thermal noise is developed using these quantities.

(a) Characteristic quantities of the enhancement mode FET

The cross sectional view of an enhancement mode FET is given by Fig. 26 together with the definitions of necessary quantities. The induced surface charge density, Q(Z), is given by,

$$Q(Z) = \frac{\varepsilon}{d} V(z) \tag{1}$$

The channel current I is given by,

$$I = Q(Z)\ S\mu\ E_L(Z) = \frac{S\varepsilon\mu}{d} V(Z)\ E_L(Z) \tag{2}$$

where $E_L(Z)$ is the electric field in the channel as a function of Z · V(Z) and $E_L(Z)$ are related by

$$V(Z) = V_g - \int_0^Z E_L(x)\, dx \tag{3}$$

It is well known that there are energy levels on the surface of a semiconductor that can trap and immobilize the carriers. To take this effect into account, V(x) must be replaced by $V(x) - V_o$ everywhere. The physical meaning of V_o is the gate voltage needed to fill all the "surface states" of the channel. The above replacement is equivalent to using $(V_g - V_o)$ instead of V_g. The effective gate voltage V_g^* is then defined by

$$V_g^* = V_g - V_o \tag{4}$$

From (2) and (3),

$$V(Z) = \sqrt{V_g^{*2} - \frac{2Id}{Se\mu} Z} \tag{5}$$

V_D, the drain voltage, is given by

$$V_D = \int_o^L E_L(Z)\, dZ = \frac{Id}{Se\mu} \int_o^L \frac{dZ}{V(Z)} = \sqrt{\frac{2Id}{Se\mu}} \left[\sqrt{X_o} - \sqrt{X_o - L} \right] \tag{6}$$

where $X_o = V_g^{*2} \cdot \frac{Se\mu}{2Id}$.

From (6), the following two relations are derived.

$$V_D \sqrt{\frac{Se\mu}{2Id}} = \sqrt{X_o} - \sqrt{X_o - L}$$

$$\frac{L}{V_D} \sqrt{\frac{2Id}{Se\mu}} = \sqrt{X_o} + \sqrt{X_o - L} \tag{7}$$

By adding these two relations,

$$V_D \sqrt{\frac{Se\mu}{2Id}} + \frac{L}{V_D} \sqrt{\frac{2Id}{Se\mu}} = 2\sqrt{X_o} = 2 V_g^* \sqrt{\frac{Se\mu}{2Id}} \tag{8}$$

Solving (8) for I

$$I = \left(\frac{Se\mu}{2L} \right) V_D (2V_g^* - V_D) \tag{9}$$

If $V_D = 0$, $I = 0$. I attains a maximum when $V_D = V_g^*$. This corresponds to the saturation of the FET.

$$I_{sat} = \left(\frac{Se\mu}{2Ld}\right) V_g^{*2}, \quad \left|V_D\right|_{sat} = V_g^*$$

The transconductance g_m and the channel conductance g_d are given by

$$g_m = \frac{\partial I}{\partial V_g} = \frac{Se\mu}{Ld} V_d \ , \ g_d = \frac{\partial I}{\partial V_D} \ , = \frac{Se\mu}{Ld} (V_g^* - V_D) \tag{11}$$

Therefore

$$g_m + g_d = \frac{Se\mu}{Ld} V_g^* \tag{12}$$

and

$$g_{do} = g_{max} = \frac{Se\mu}{Ld} V_g^* \tag{13}$$

Next, g_d^2 is expressed by I in the following way

$$g_d^2 = \left(\frac{Se\mu}{Ld}\right)^2 (Vg^* - V_D)^2 = \left(\frac{Se\mu}{Ld}\right)^2 \left(V_g^{*2} - \frac{2Ld}{Se\mu} I\right)$$

$$= 2I_s \frac{Se\mu}{Ld} \left(\frac{I_s - I}{I_s}\right) = g_{do}^2 \left(\frac{I_s - I}{I_s}\right) \tag{14}$$

This relation will be used later.

(b) Theory of the thermal noise of an enhancement mode FET

To calculate the thermal noise of an enhancement mode FET by taking into account of the channel modulation effects, the channel is divided into small sections and the contributions from each small section are summed up by integration.

The contribution from the section ΔZ at Z is calculated as follows. The dc parts of V(X) and $E_L(X)$ are represented by $V_o(X)$ and $E_{Lo}(X)$ respectively. If there is a thermal noise $\Delta V(Z,t)$ in the section ΔZ (see Fig. 26)

$$\begin{aligned} V(X) &= V(X) \qquad 0 < X < Z \\ V(X) &= V_o(X) - \Delta V(Z,t) \qquad Z + \Delta Z \leqslant X \leqslant L \end{aligned} \tag{15}$$

The relative potential difference between the gate and the channel is reduced by the amount $\Delta V(Z,t)$ in the region $Z + \Delta Z \leqslant X \leqslant L$. Using the relation (2) of the previous section,

$$\begin{aligned} E_L(X) &= E_{Lo}(X) \qquad 0 \leqslant X \leqslant Z \\ E_l(X) &= E_{Lo}(X) + \frac{I.d}{S\epsilon\mu} \frac{\Delta V(Z,t)}{V_o(X)^2} \qquad Z + \Delta Z \leq X \leq L \end{aligned} \tag{16}$$

because $\Delta V(Z,t)$ is small as compared with $V_o(X)$.

From (16),

$$V_D = \int_o^L E_L(X)\, dX = \int_o^L E_{Lo}(X)dX + \Delta V(Z,t) + \int_Z^L \left\{ E_{Lo}(X) + \frac{I.d}{S\epsilon\mu} \frac{\Delta V(Z,t)}{V_o(X)^2} \right\} dX = \int_o^L E_{Lo}(X)dX + \Delta V(Z,t) \left[1 + \frac{I.d}{S\epsilon\mu} \int_Z^L \frac{dX}{V_o(X)^2} \right]$$

(17)

Therefore

$$\overline{(V - V_{Do})^2} = \overline{\Delta V(Z,t)^2} \left[1 + \frac{I.d}{S e \mu} \int_Z^L \frac{2dX}{V_o(X)^2} \right]^2 \tag{18}$$

because $V_{Do} = \int_o^L E_{Lo}(X)dX$

$\overline{\Delta V(Z,t)^2}$ is given by the Nyquist formula,

$$\overline{\Delta V(Z,t)^2} = 4kT \left(\frac{d}{S e \mu} \right) \frac{\Delta Z}{V_o(Z)} \quad \text{(per 1 c/s)} \tag{19}$$

Next, the contribution from every part of the channel is summed up by integration to obtain the total thermal noise.

$$\overline{(\Delta V_D)^2} = 4kT \left(\frac{d}{S e \mu} \right) \int_o^L \frac{dZ}{V_o(Z)} \left[1 + \frac{I.d}{S e \mu} \int_Z^L \frac{dX}{V_o(X)^2} \right]^2 \tag{20}$$

This expression is reduced to

$$\overline{(\Delta V_D)^2} = 4kT \frac{1}{g_{do}} + 8kT \left(\frac{d}{S e \mu} \right)^2 \cdot I \int_o^L \frac{dZ}{V_o(Z)} \left[\int_Z^L \frac{dX}{V_o(X)^2} \right]$$

$$+ 4kT \cdot \left(\frac{d}{S e \mu} \right)^3 I^2 \int_o^L \frac{dZ}{V_o(Z)} \left[\int_Z^L \frac{dX}{V_o(X)^2} \right]^2 \tag{21}$$

where $V_o(Z) = \sqrt{V_g{}^{*2} - \frac{2Id}{S e \mu} Z}$

The integrals are calculated as follows.

$$\int_0^L \frac{dZ}{V_o(Z)}\left[\int_Z^L \frac{dX}{V_o(X)^2}\right] = 2\left(\frac{Se\mu}{2Id}\right)^{3/2}$$

$$\left[\sqrt{X_o}\log\left(\frac{X_o}{X_o - L}\right) - 2\left(\sqrt{X_o} - \sqrt{X_o - L}\right)\right] \tag{22}$$

where $X_o = \left(\frac{Se\mu}{2Id}\right) V_g^{*2}$

$$\int_0^L \frac{dZ}{V_o(Z)}\left[\int_Z^L \frac{dX}{V_o(X)^2}\right]^2 = 2\left(\frac{Se\mu}{2Id}\right)^{5/2}\left[\sqrt{X_o}\left\{\log\sqrt{\frac{X_o}{X_o - L}}\right\}^2\right. \tag{23}$$

$$\left. - 2\sqrt{X_o}\left(\log\sqrt{\frac{X_o}{X_o - L}}\right) + 2\left\{\sqrt{X_o} - \sqrt{X_o - L}\right\}\right]$$

By substituting (22) into (21),

$$\overline{(\Delta V_D)^2} = 4kT\left[\frac{1}{g_{do}} + \frac{1}{4}\frac{V_g}{I}\left\{\frac{1}{4}\left(\log\frac{X_o}{X_o - L}\right)^2 + 3\log\frac{X_o}{X_o - L} - 6 + 6\sqrt{\frac{X_o - L}{X_o}}\right\}\right] \tag{24}$$

Using the relation $\frac{X_o}{X_o - L} = \frac{I_s}{I_s - I}$

$$\frac{1}{4}\frac{V_g}{I} g_{do} = \frac{1}{4}\frac{V_g \cdot g_{do}}{I_s}\frac{I_s}{I} = \frac{1}{2}\frac{I_s}{I} \tag{25}$$

$$\overline{(\Delta V_D)^2} = \frac{4kT}{g_{do}}\left\{1 + \frac{1}{2}\frac{I_s}{I}\left\{\frac{1}{4}\left[\log\left(1 - \frac{I}{I_s}\right)\right]^2 - 3\log\left(1 - \frac{I}{I_s}\right) - 6 + 6\sqrt{1 - \frac{I}{I_s}}\right\}\right\} \tag{26}$$

To obtain the expression for the noise current generator,

$$\overline{(\Delta I)^2} = \overline{(\Delta V_D)^2}\ g_d^2 = 4kTg_{do}\left(1-\frac{I}{I_s}\right)\left\{1 + \frac{1}{2}\frac{I_s}{I}\left\{\frac{1}{4}\left[\log\left(1-\frac{I}{I_s}\right)\right]^2 - 3\log\left(1 - \frac{I}{I_s}\right) - 6 + 6\sqrt{1 - \frac{I}{I_s}}\right\}\right\} \tag{27}$$

where the relation (14) in the previous section was used.

If $\lambda = \frac{I}{I_s}$

$$f(\lambda) = (1-\lambda)\left[1 + \frac{\frac{1}{4}\left\{\log(1-\lambda)\right\}^2 - 3\log(1-\lambda) - 6 + 6\sqrt{1-\lambda}}{2\lambda}\right]$$

$$= 1 - \frac{1}{2}\lambda + O(\lambda^2) \quad \text{(for small } \lambda\text{)}$$

$$\overline{(\Delta I)^2} = 4kT\ g_{do}\ f(\lambda) \tag{28}$$

If the equivalent noise diode current, I_{eq}, is introduced,

$$\frac{I_{eq}(I)}{I_{eq}(0)} = f(\lambda),\ I_{eq}(0) = \frac{2kT}{e}\ g_{do} \tag{29}$$

This relation is plotted in Fig. 27. The thermal noise of an enhancement FET becomes zero at suatration. This means that the channel modulation effect is not strong enough to cancel the decrease of g_d^2. Because of this, the noise of an enhancement FET at saturation is not due to thermal noise. The noise of an enhancement mode FET is essentially due to two different noise mechanisms. The thermal noise is important for small V_d, and another (still unknown) kind of noise predominates over the thermal noise near saturation.

V. Conclusions

The equipment designed for measuring noise in FET's at low temperature under pulsed conditions is operating satisfactorily and gives reliable results.

The program of studying the correlation between 1/f noise and reliability is continuing satisfactorily. Noise measurements have been carried out after life tests at elevated temperatures. No conclusions can be drawn as yet.

Noise in unijunction transistors can be successfully interpreted by drift of injected carriers when the base 2 current is large in comparison with the emitter current. The interpretation of the frequency dependence of the noise is still a problem, however.

Pulse noise measurements in FET's at liquid nitrogen temperatures show a white excess noise. Heating effects in the channel strongly affect the noise output. The noise might be caused by non-ionized donors in the channel.

Noise measurements on enhancement mode FET's with insulated gate show a spectrum caused by surface traps with a time constant of 10-30 μsec. The noise at higher frequencies is white but non-thermal. Some of the noise processes seem to be associated with the insulating layer whereas others seem to be associated with the channel.

Present theoretical results on low-frequency excess noise in FET's cannot fully explain the observed data.

The (I_d, V_d) characteristic and the (g_m, V_g) characteristic of a diffused junction FET was calculated both for constant mobility and for a field-dependent mobility under the assumption of a linear impurity distribution in the junction. The results obtained agree somewhat better with the experimental data than the Shockley model, but the agreement is not perfect.

The theory of thermal noise in an enhancement noise FET with insulated gate shows that I_{eq} goes to zero if the device approaches saturation.

VI. Program for Next Interval

It is hoped that the work in noise in unijunction transistors can be written up in its final form.

It is also hoped that the work on low-frequency excess noise in FET's can be written up in its final form.

It is planned to collect noise data of some transistors over a wide frequency range.

The work on the correlation between 1/f noise and reliability will continue with longer and more extended life tests.

An attempt will be made to measure noise in GaAs lasers under pulsed conditions. Plans will be made to measure GaAs lasers at liquid H_2 temperature under C.W. conditions.

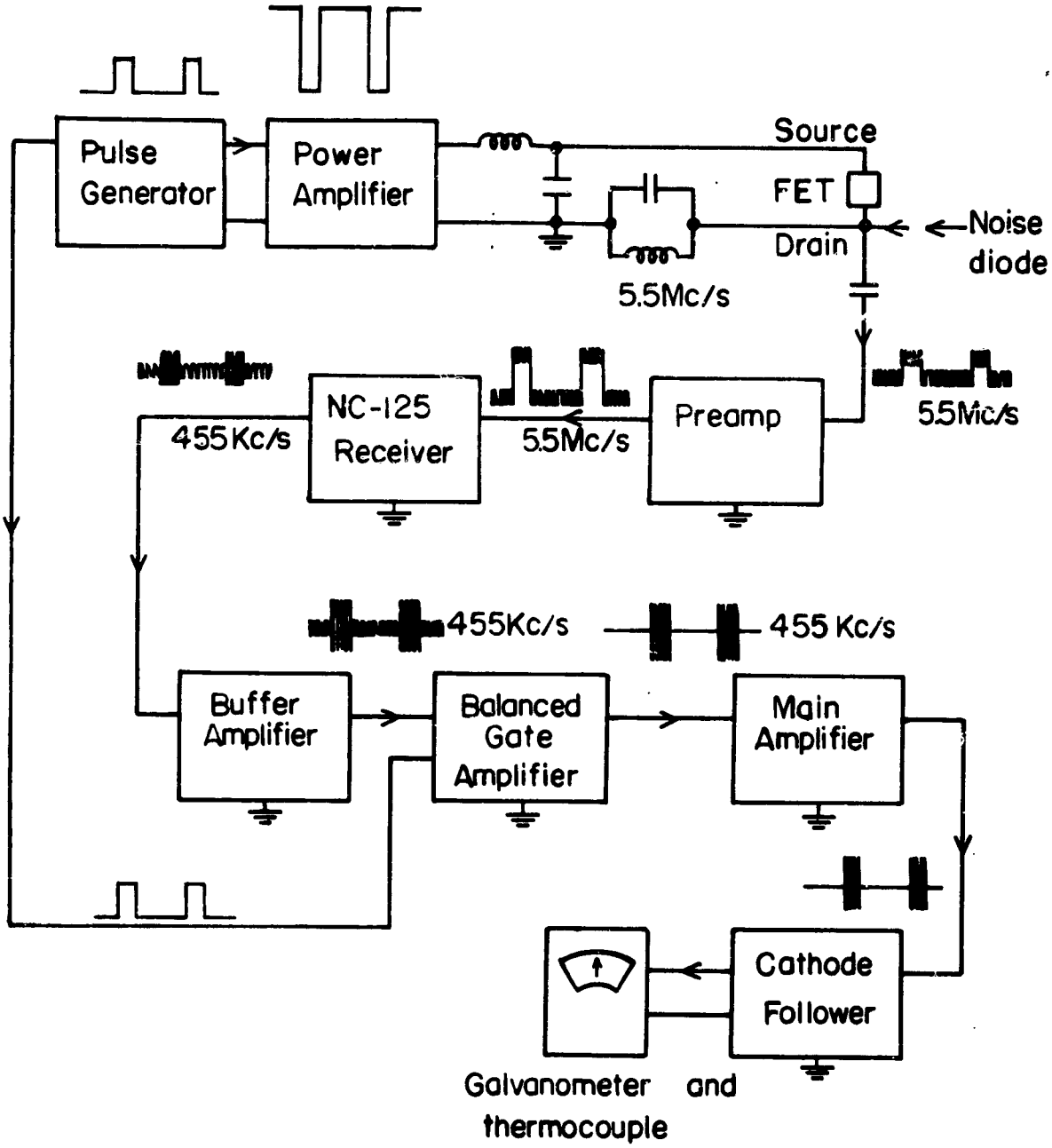
Work on enhancement mode FET's with insulated gate will continue and an attempt will be made to better localise the noise sources.

Work on depletion mode FET's with insulated gate will be extended to higher frequencies.

An attempt will be made to pinpoint the noise source giving the temperature dependent white noise in normal FET's at liquid N_2 temperature.

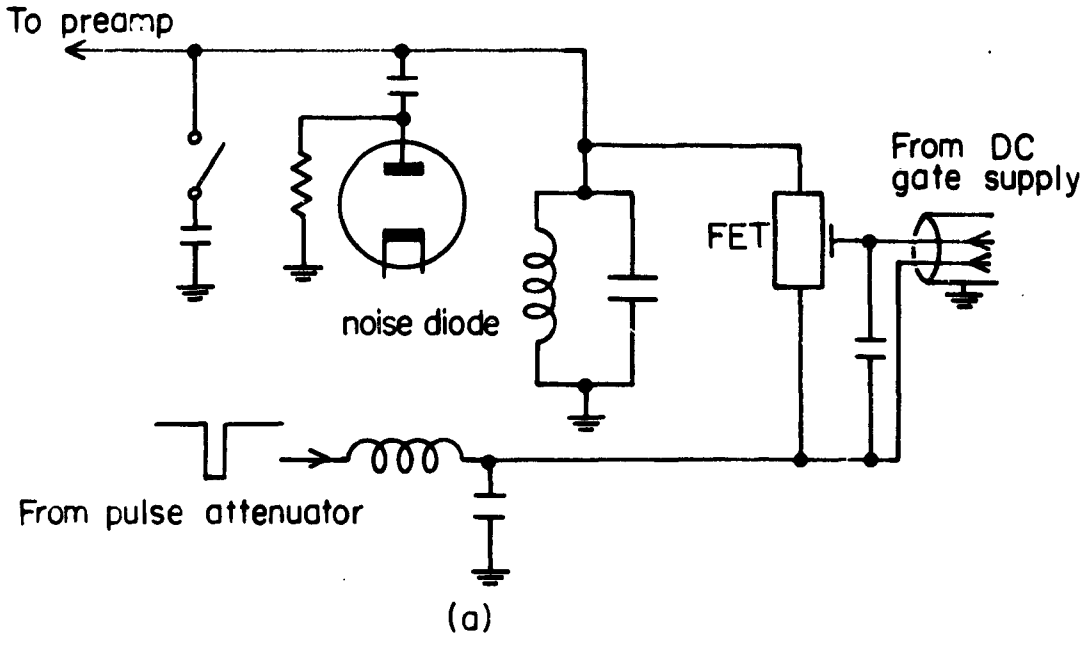
VII. Personnel Employed on Project

	Man Months
A. van der Ziel	.45
D. C. Agouridis	1.50
R. D. Baertsch	1.50
Henry Halladay	1.50
L. J. Prescott	1.50
M. Shoji	1.50
A. Tong	1.50
Laboratory Technical Assistants	321.3 Man Hours



The method of measurement of the noise of FET at low duty cycles

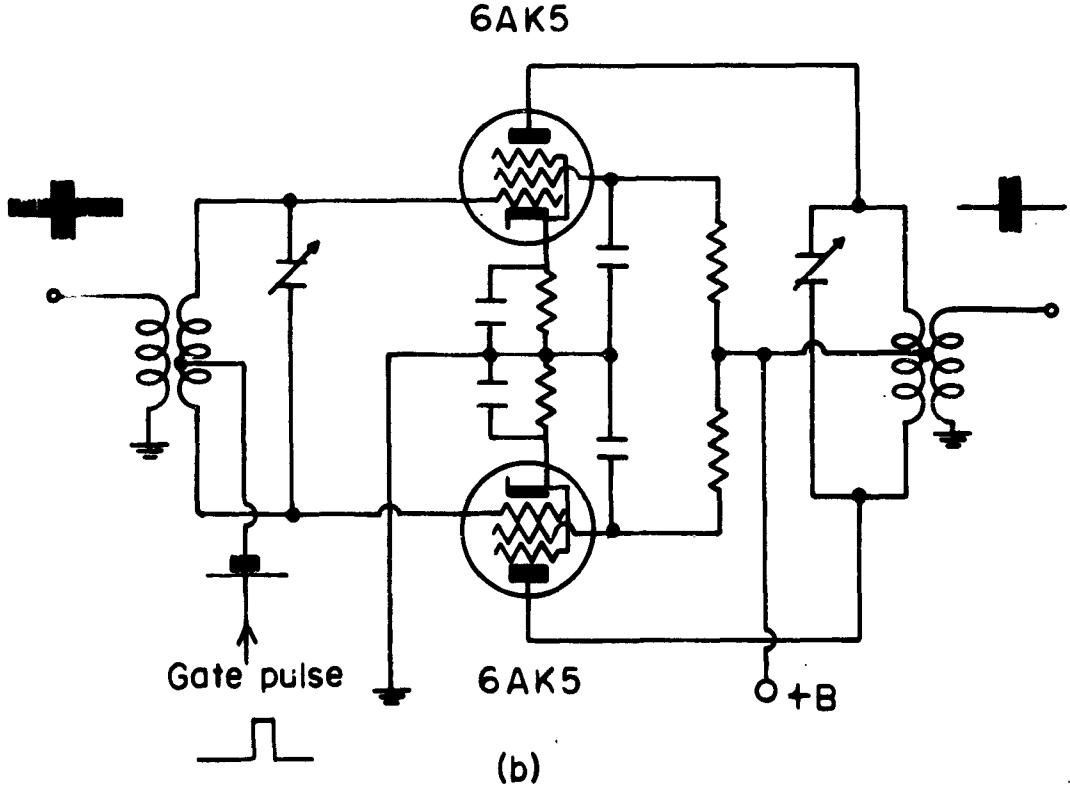
Fig. 1



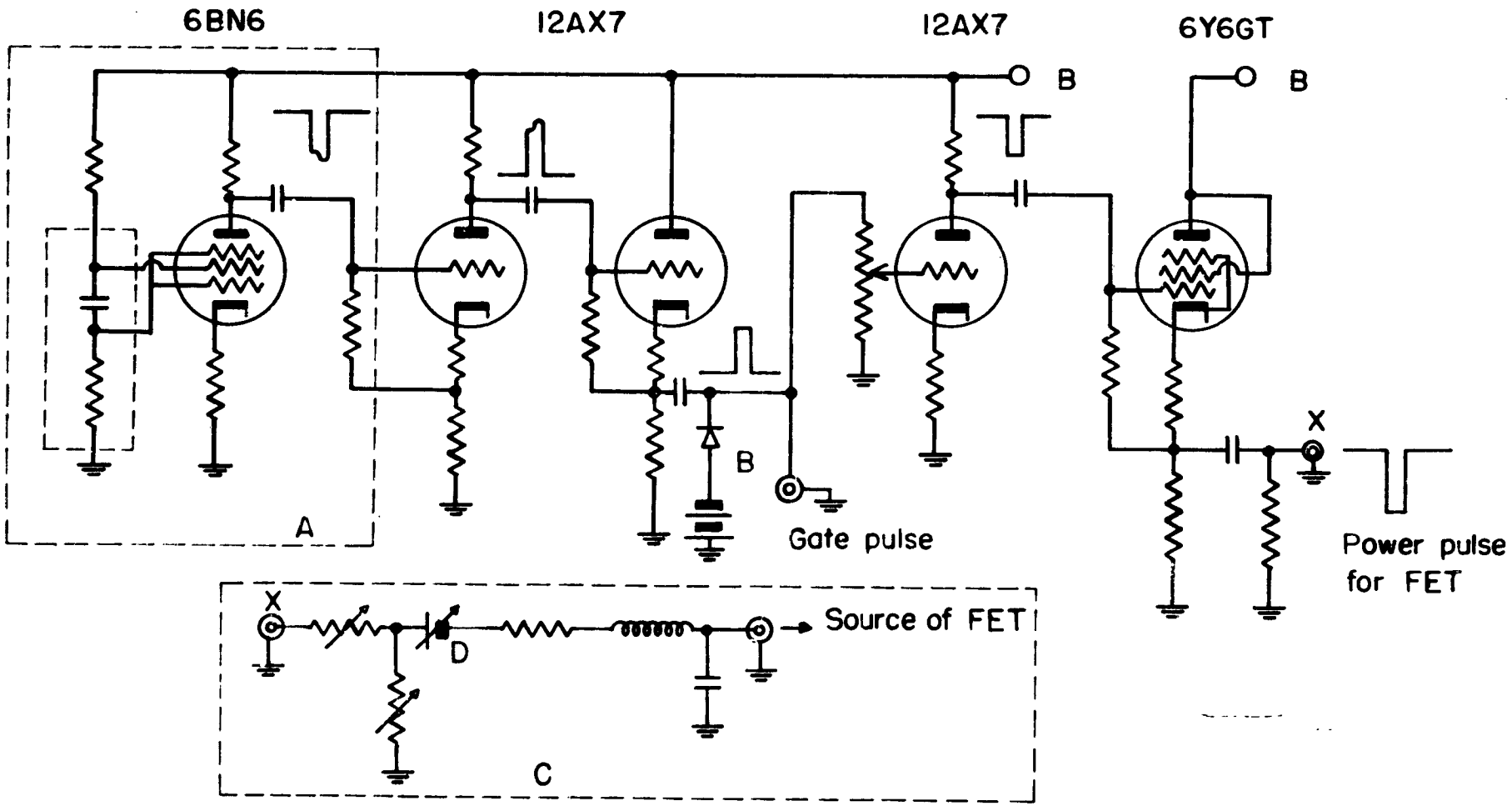
(a)

Fig. 2 (a) Jig for FET

(b) The balanced gate for 455Kc/s



(b)



A. Pulse generator by a gated beam tube.
B. Pulse shaper
C. Pulse attenuator and filter
D. Leakage compensating battery

Fig 3 Pulse generator and pulse amplifier

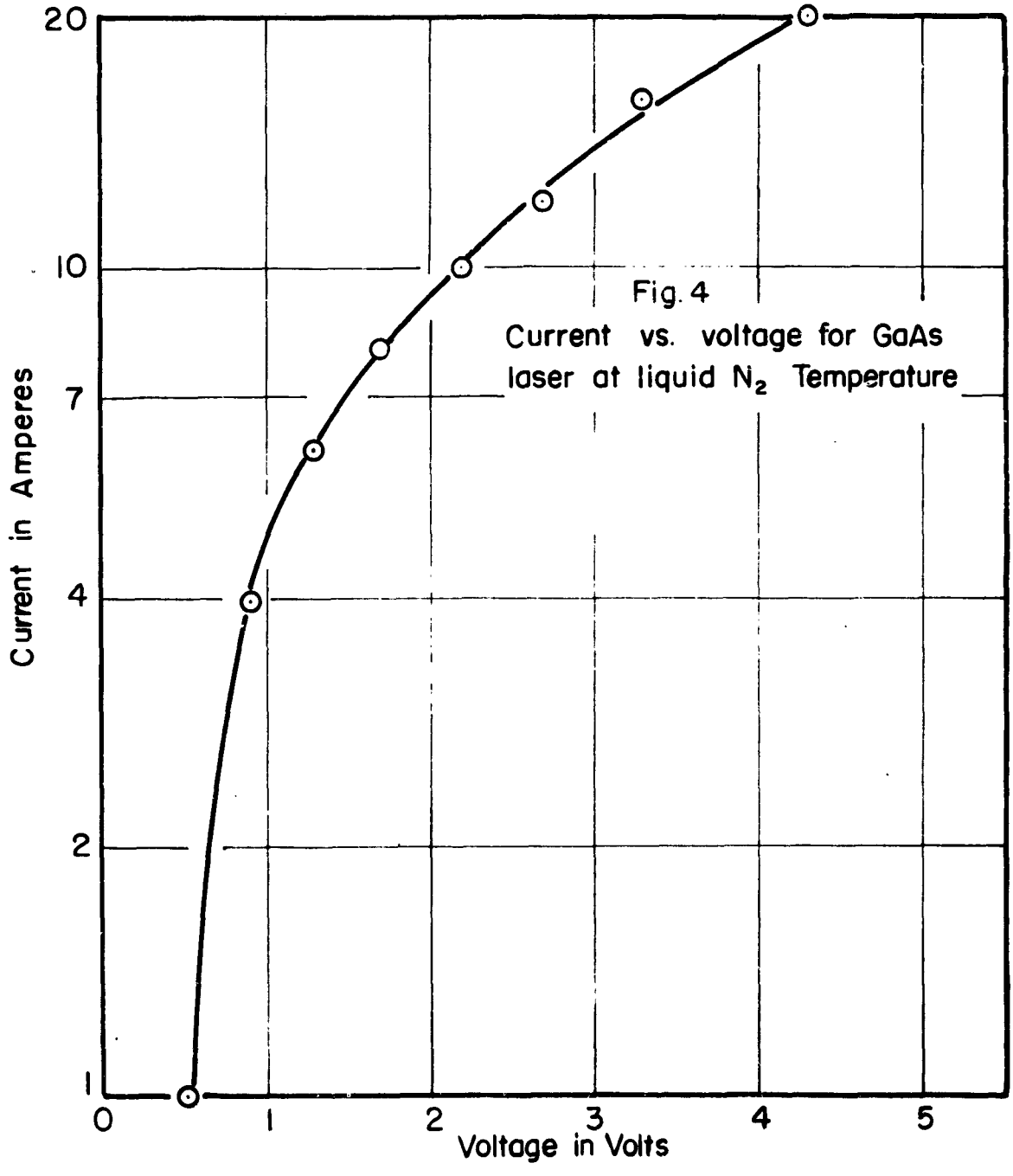


Fig. 4
Current vs. voltage for GaAs laser at liquid N_2 Temperature

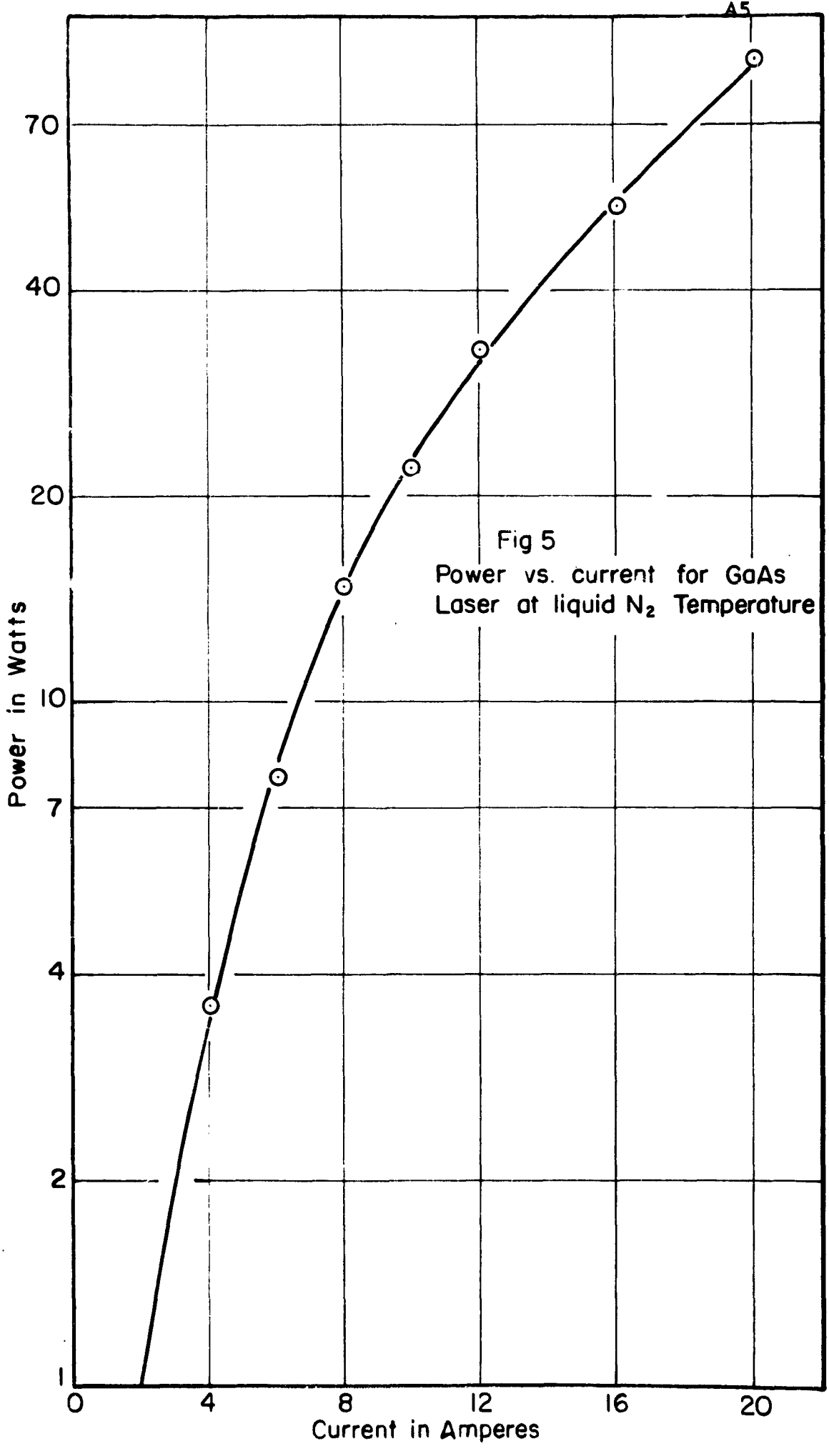


Fig 5
Power vs. current for GaAs Laser at liquid N_2 Temperature

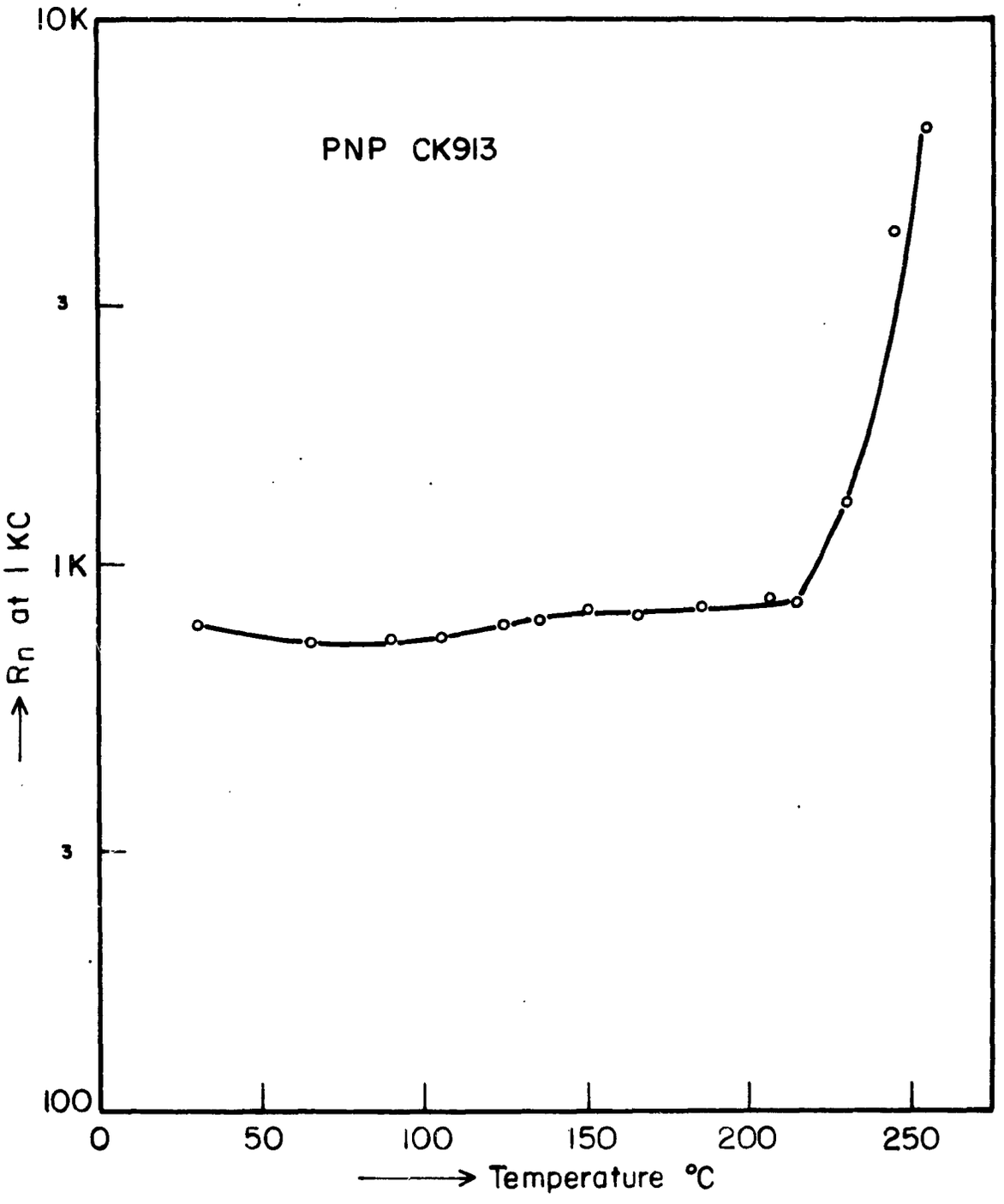
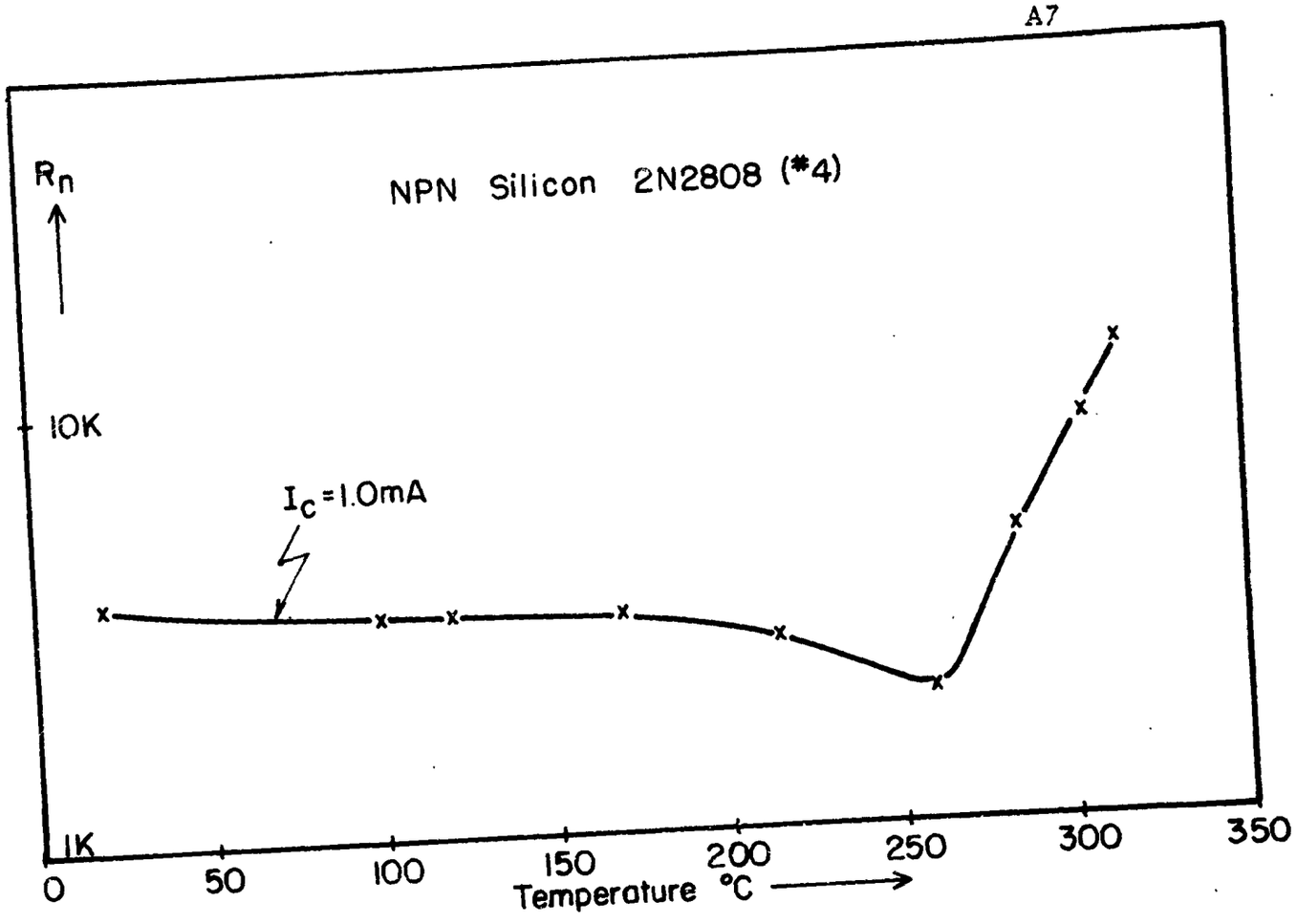


Fig. 6 Temperature dependence of R_n in PNPCK913



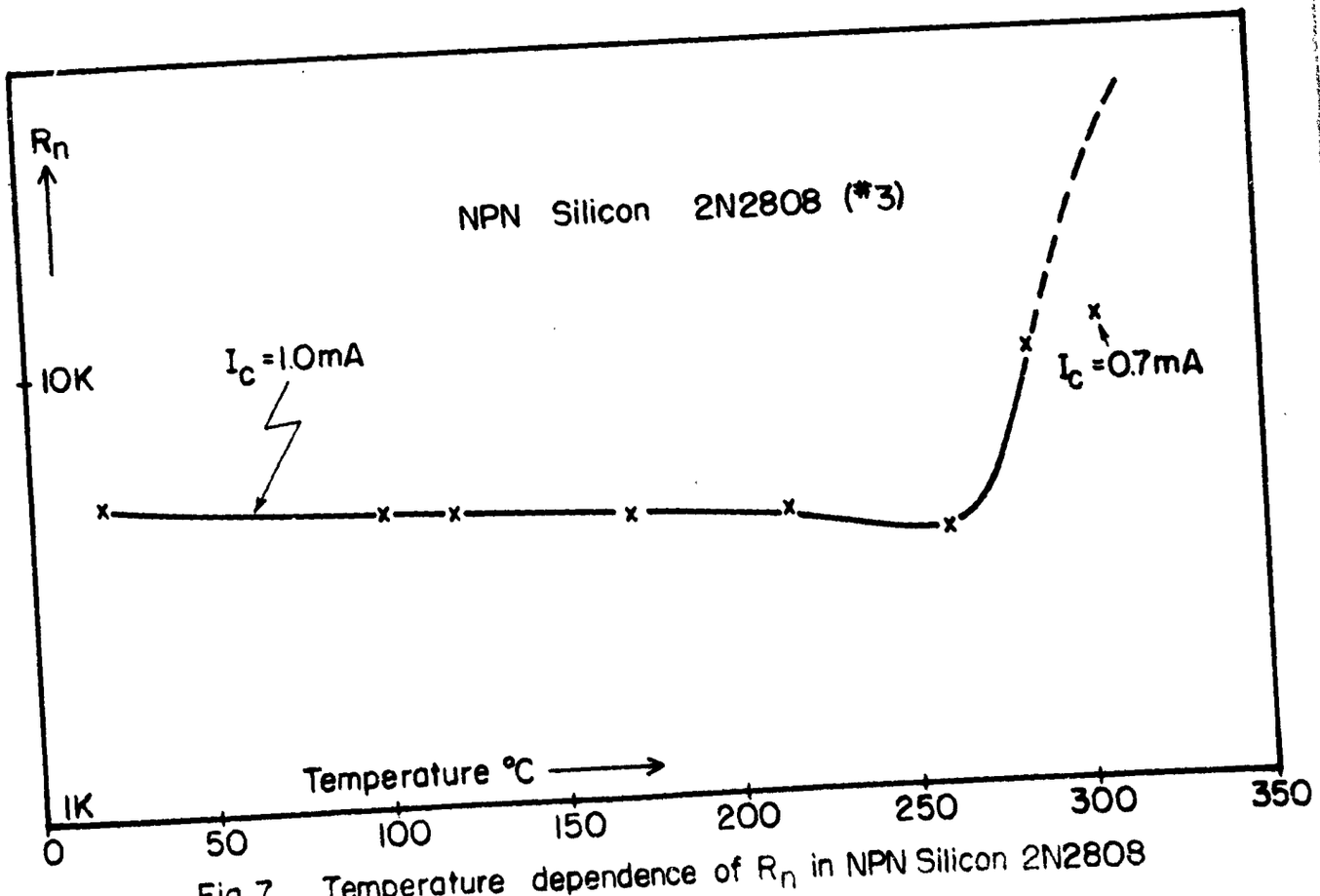


Fig 7 Temperature dependence of R_n in NPN Silicon 2N2808

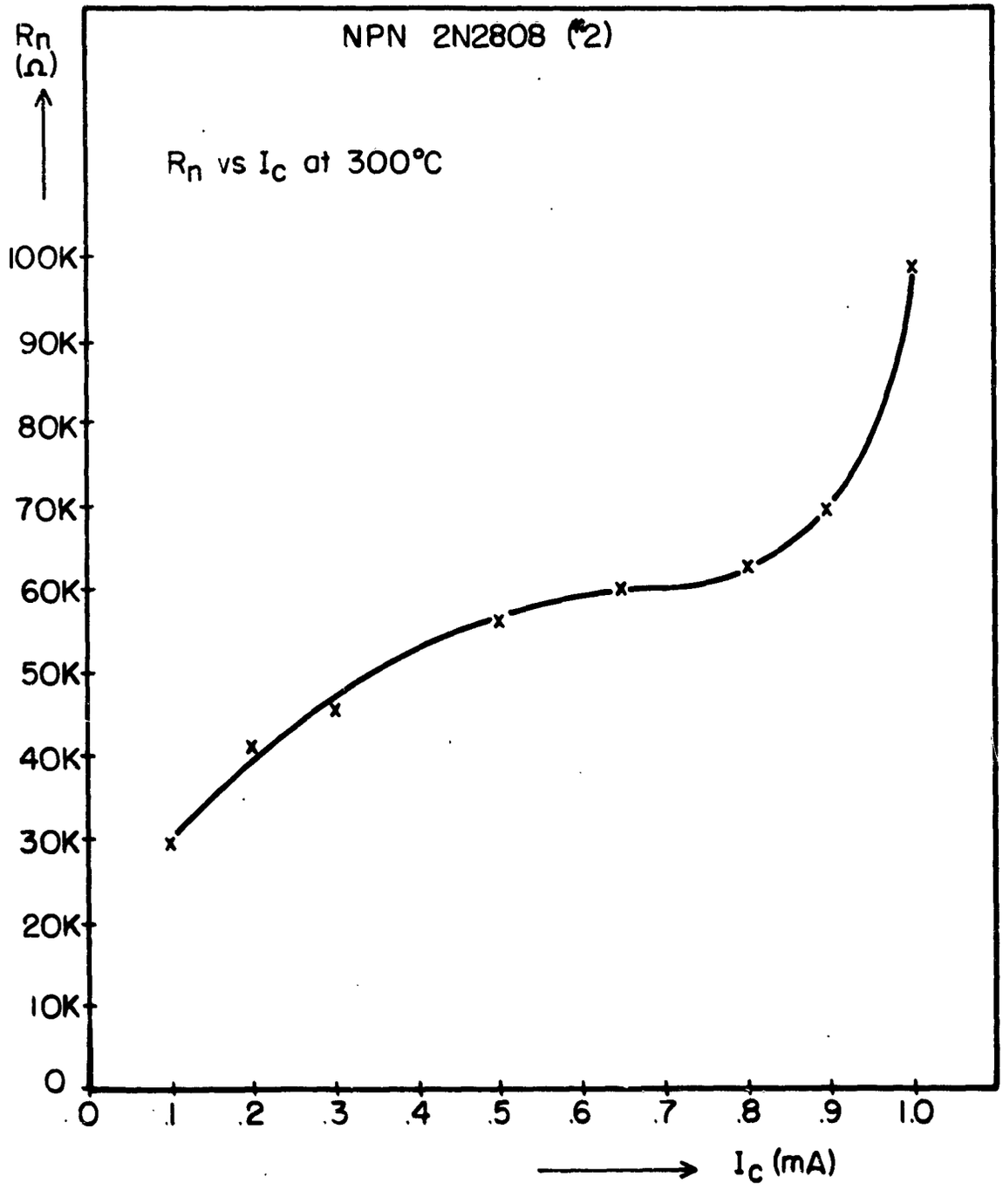


Fig. 8 R_n vs. I_C in NPN 2N2808 No. 2 at 300°C

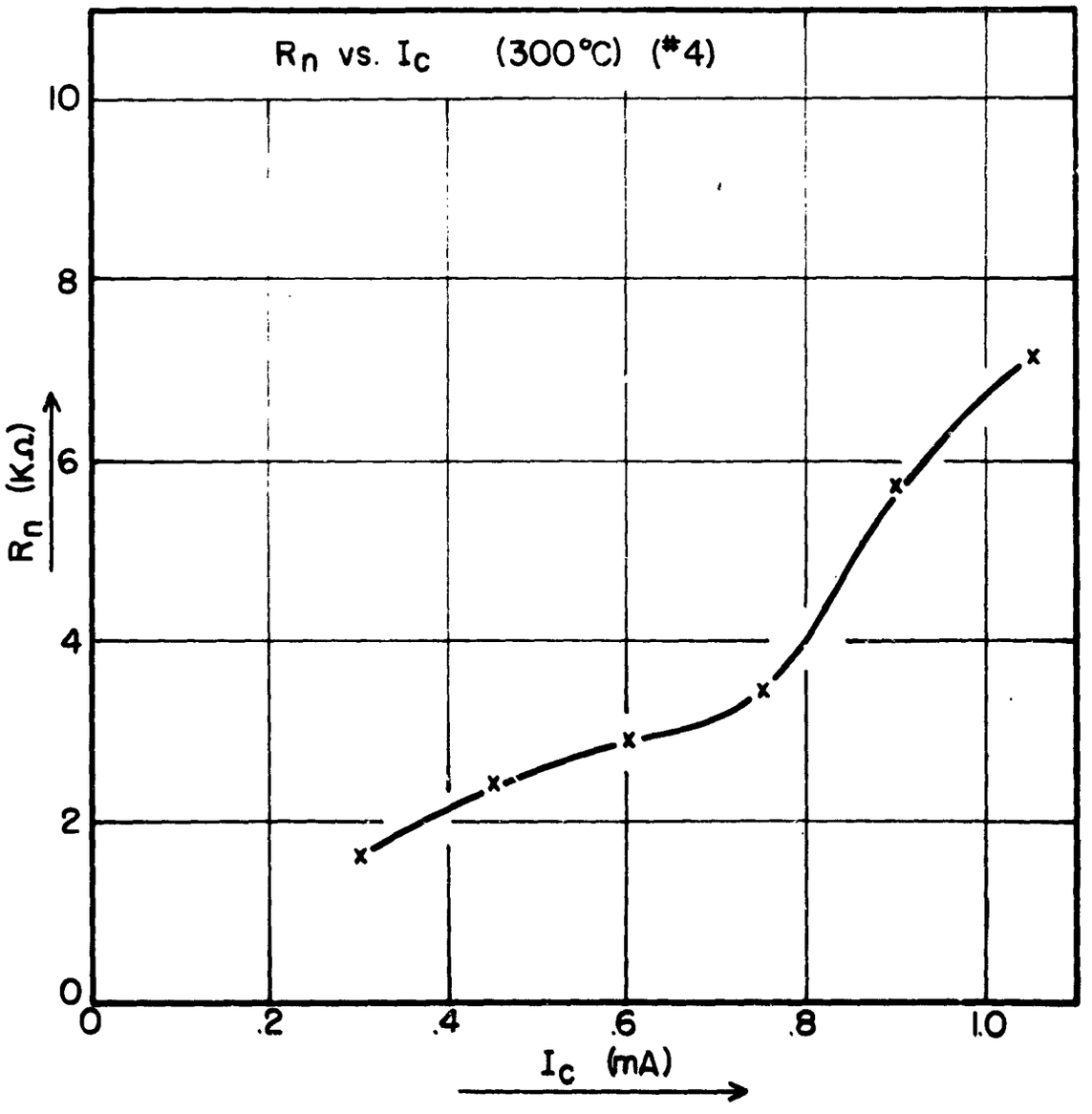


Fig. 9 R_n vs I_c in NPN 2N2808 No 4

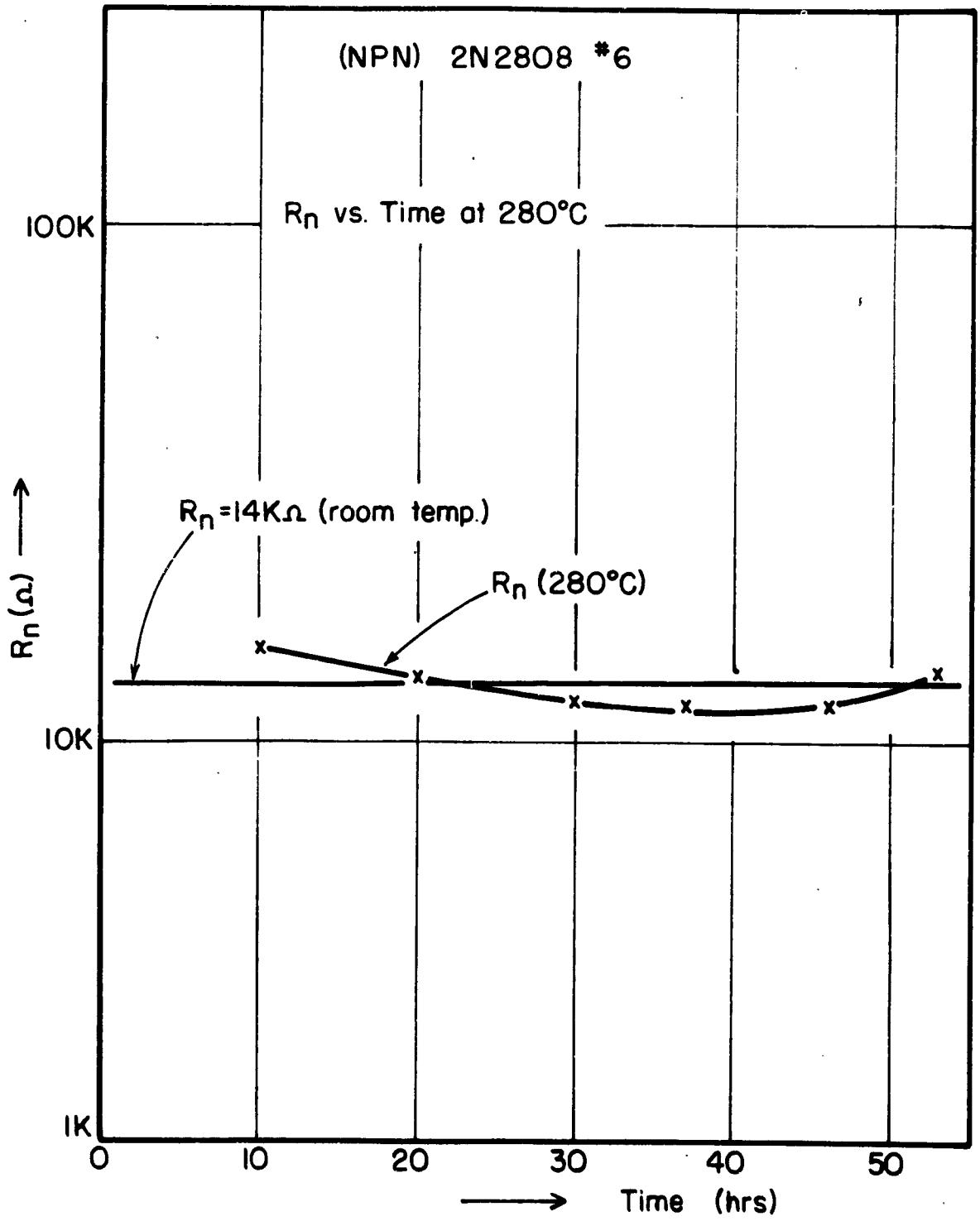


Fig. 10 R_n vs. time for 2N2808 #6

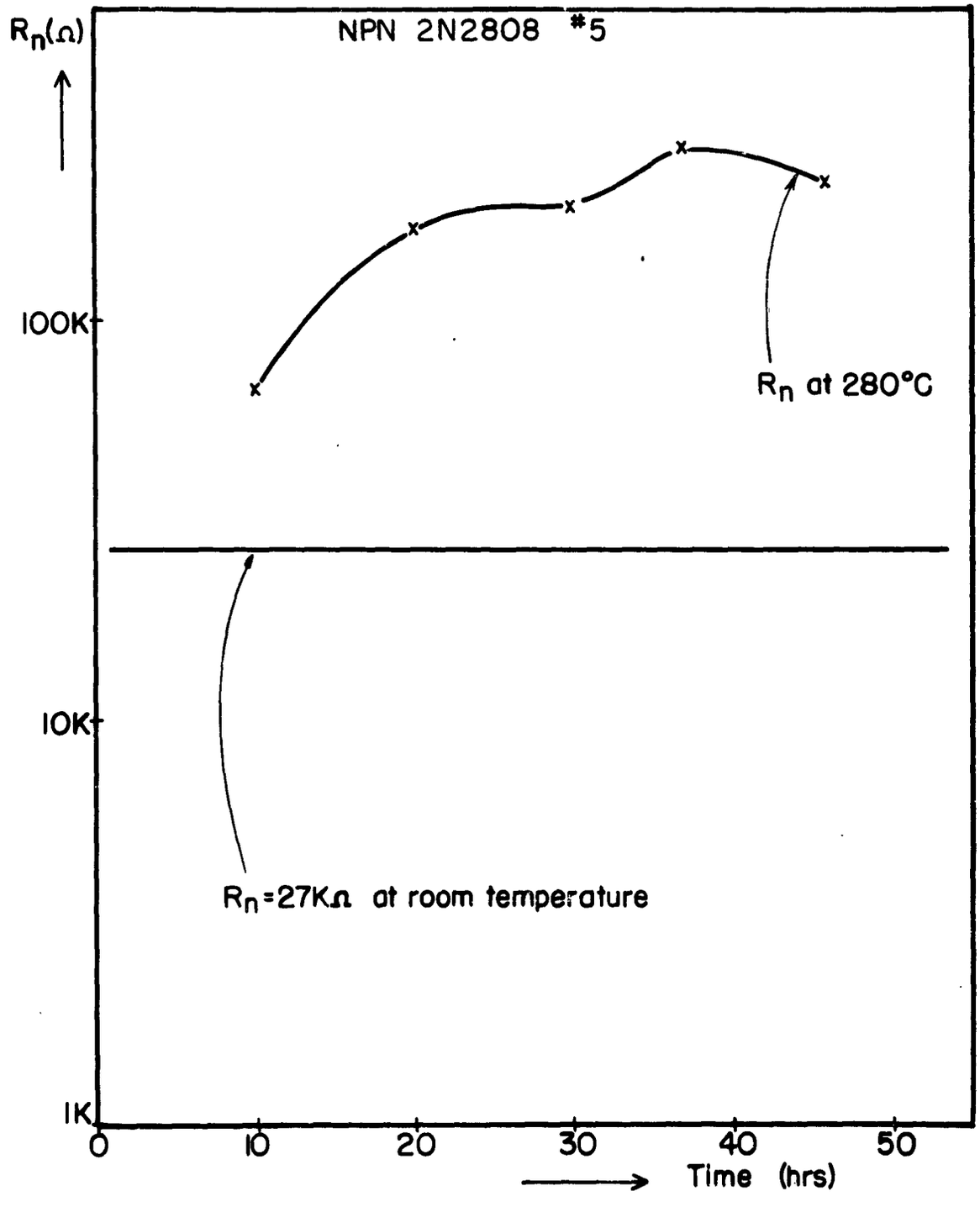


Fig.11 R_n as a function of time for 2N2808 No.5

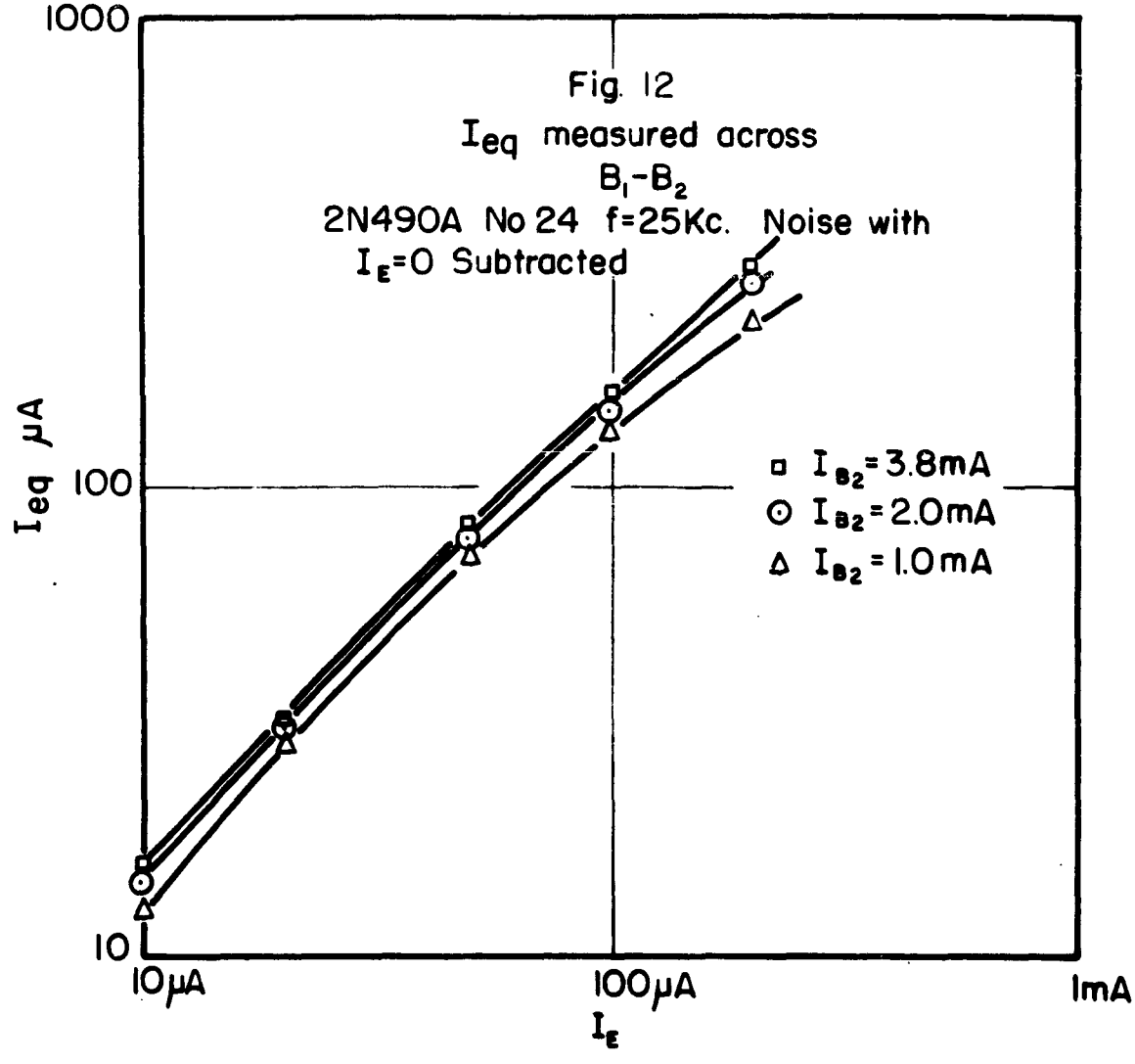


Fig. 12
I_{eq} measured across
B_1-B_2
2N490A No 24 f=25Kc. Noise with
I_E=0 Subtracted

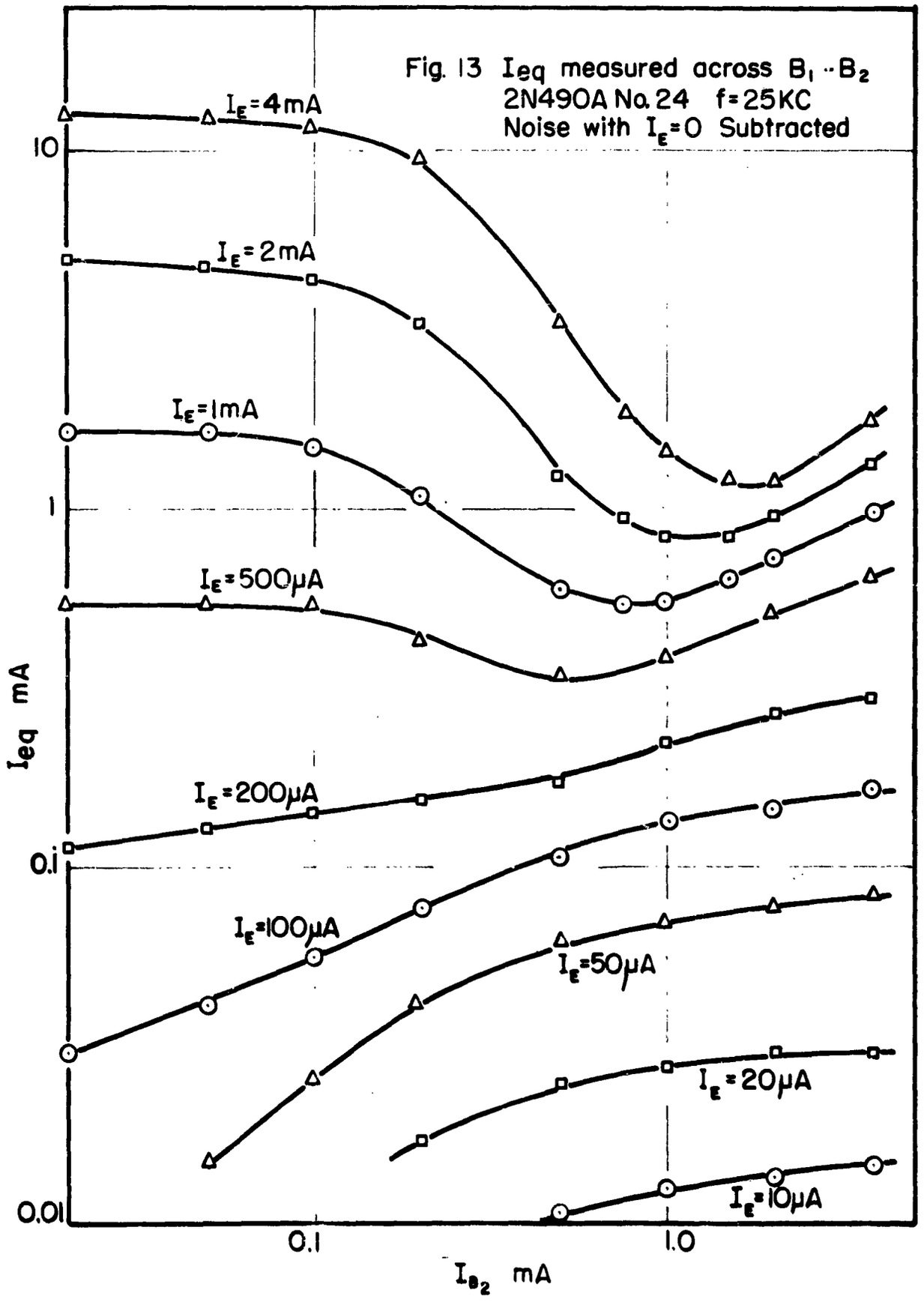


Fig. 13 Ieq measured across B1 - B2
2N490A No. 24 f=25KC
Noise with IE=0 Subtracted
IE=4mA
IE=2mA
IE=1mA
IE=500μA
IE=200μA
IE=100μA
IE=50μA
IE=20μA
IE=10μA
10
1
0.1
0.01
Ieq mA
0.1
1.0
IB2 mA

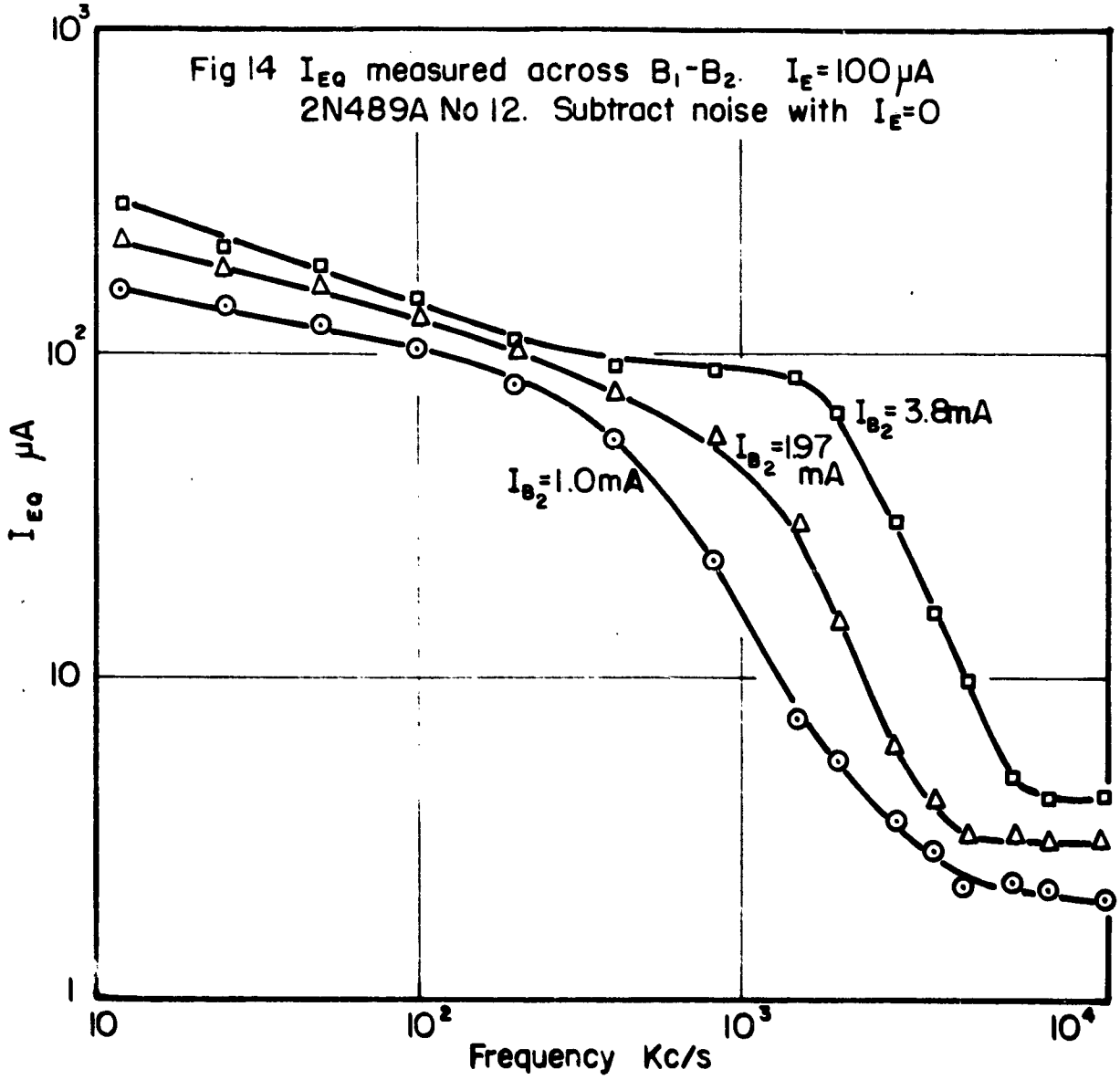
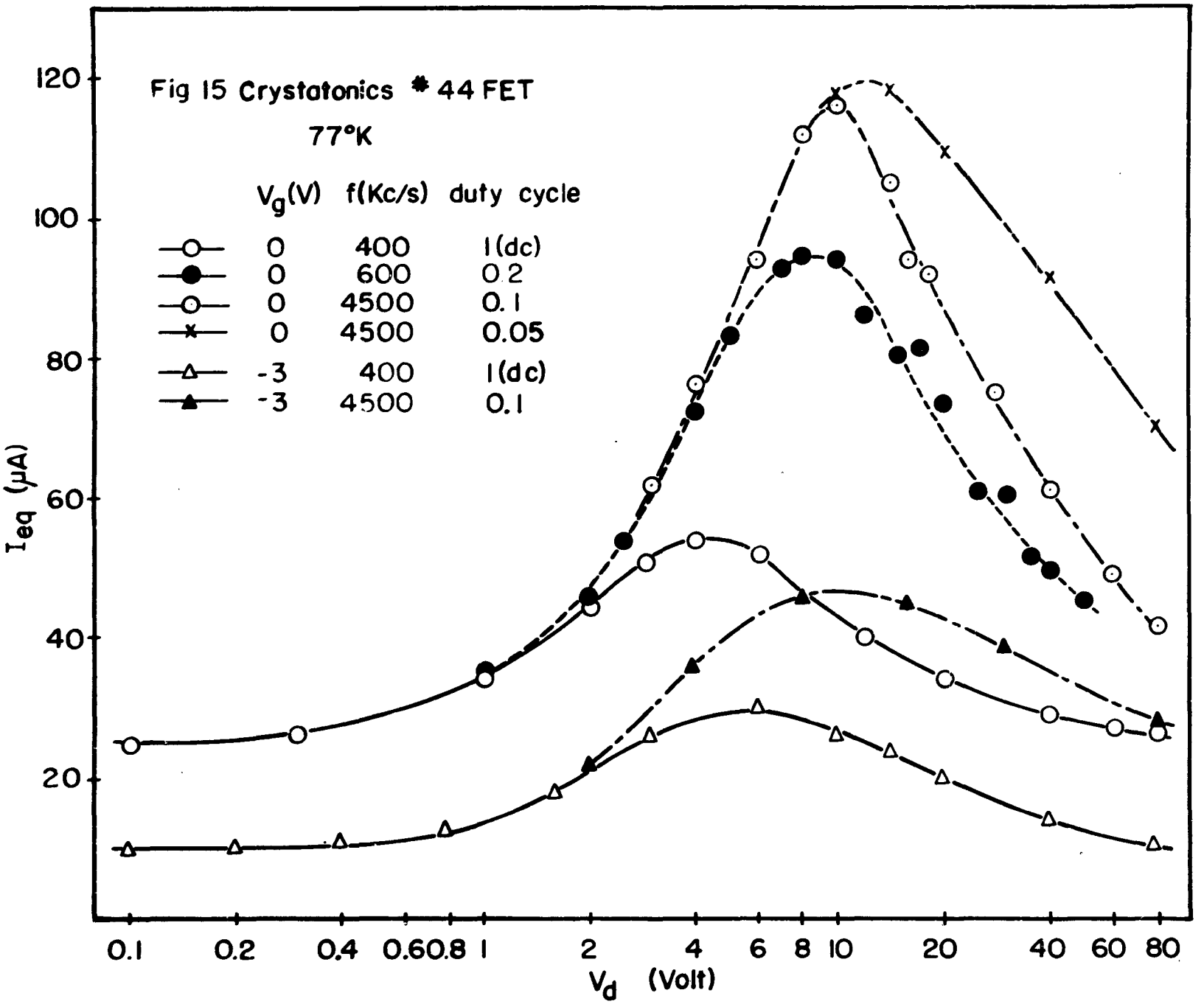


Fig 14 I_{EQ} measured across B_1-B_2. I_E=100 μA
2N489A No 12. Subtract noise with I_E=0
10^3
10^2
10
1
I_{EQ} μA
I_{B_2}= 3.8mA
I_{B_2}=1.97 mA
I_{B_2}=1.0mA
10
10^2
10^3
10^4
Frequency Kc/s



Results of the pulse noise measurements at 77°K

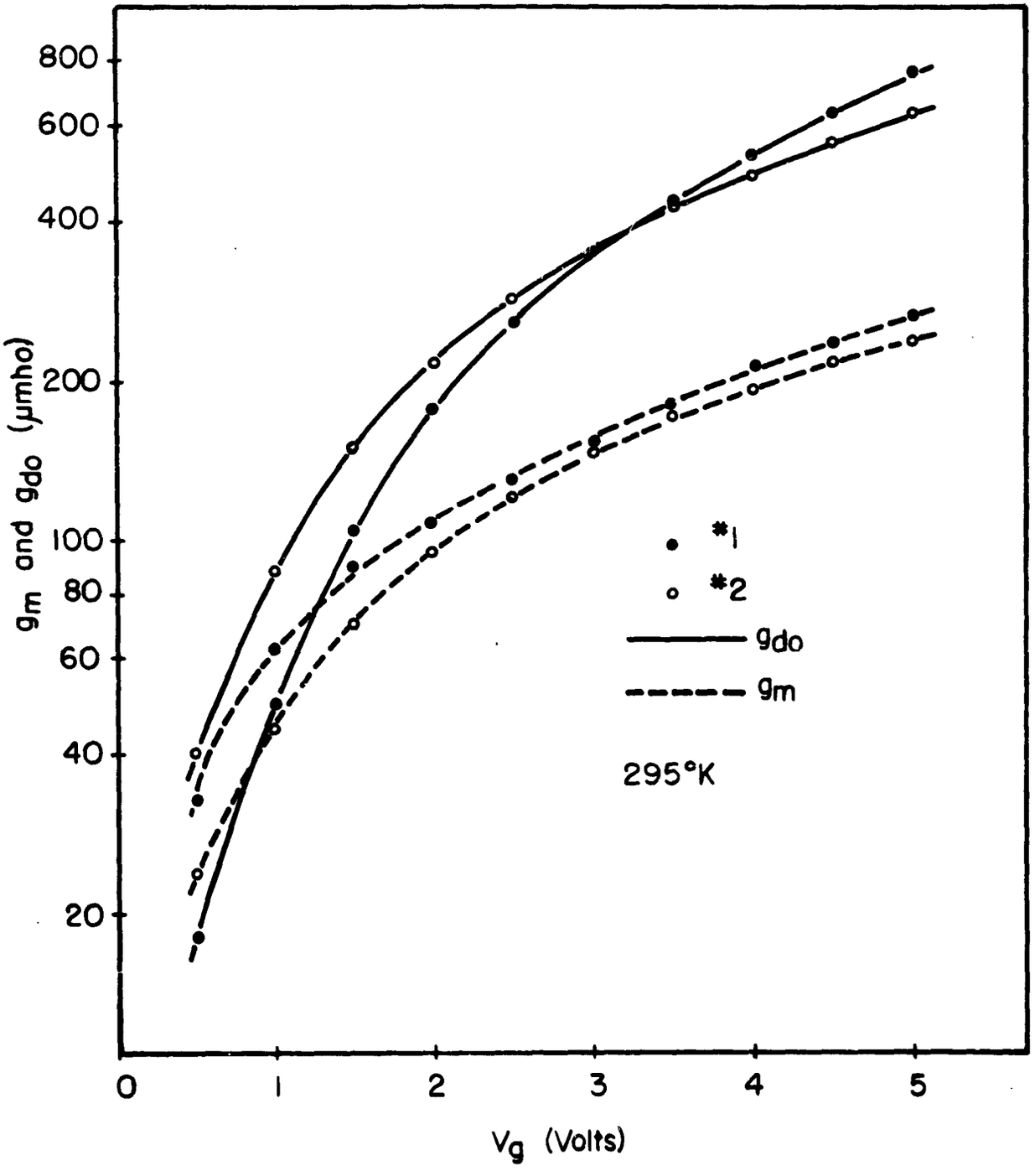


Fig. 16 Dependence of g_m and g_{do} on V_g of the RCA enhancement mode FET

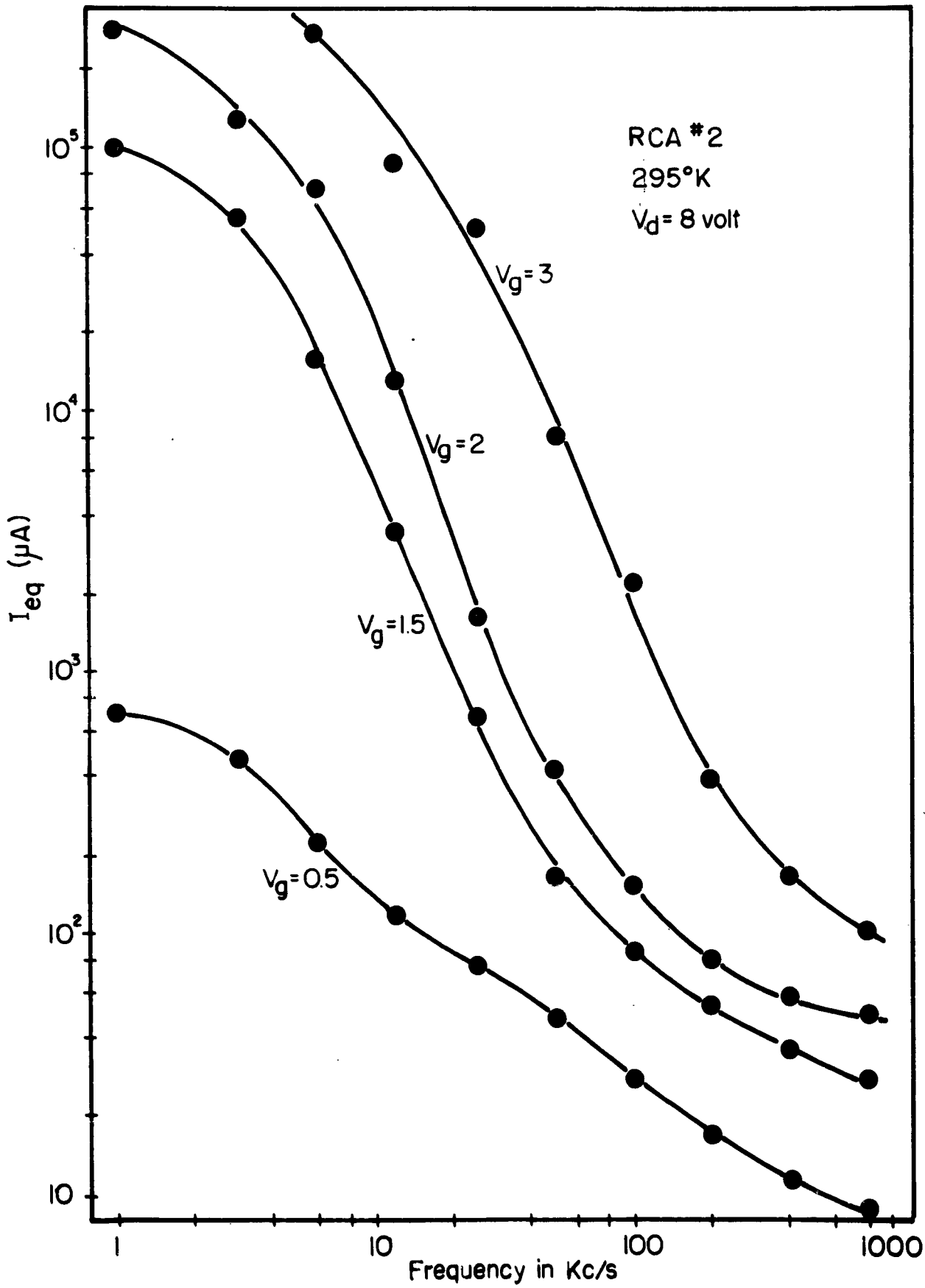


Fig. 17 Dependence of the frequency spectra of the RCA enhancement mode FET on the gate voltage

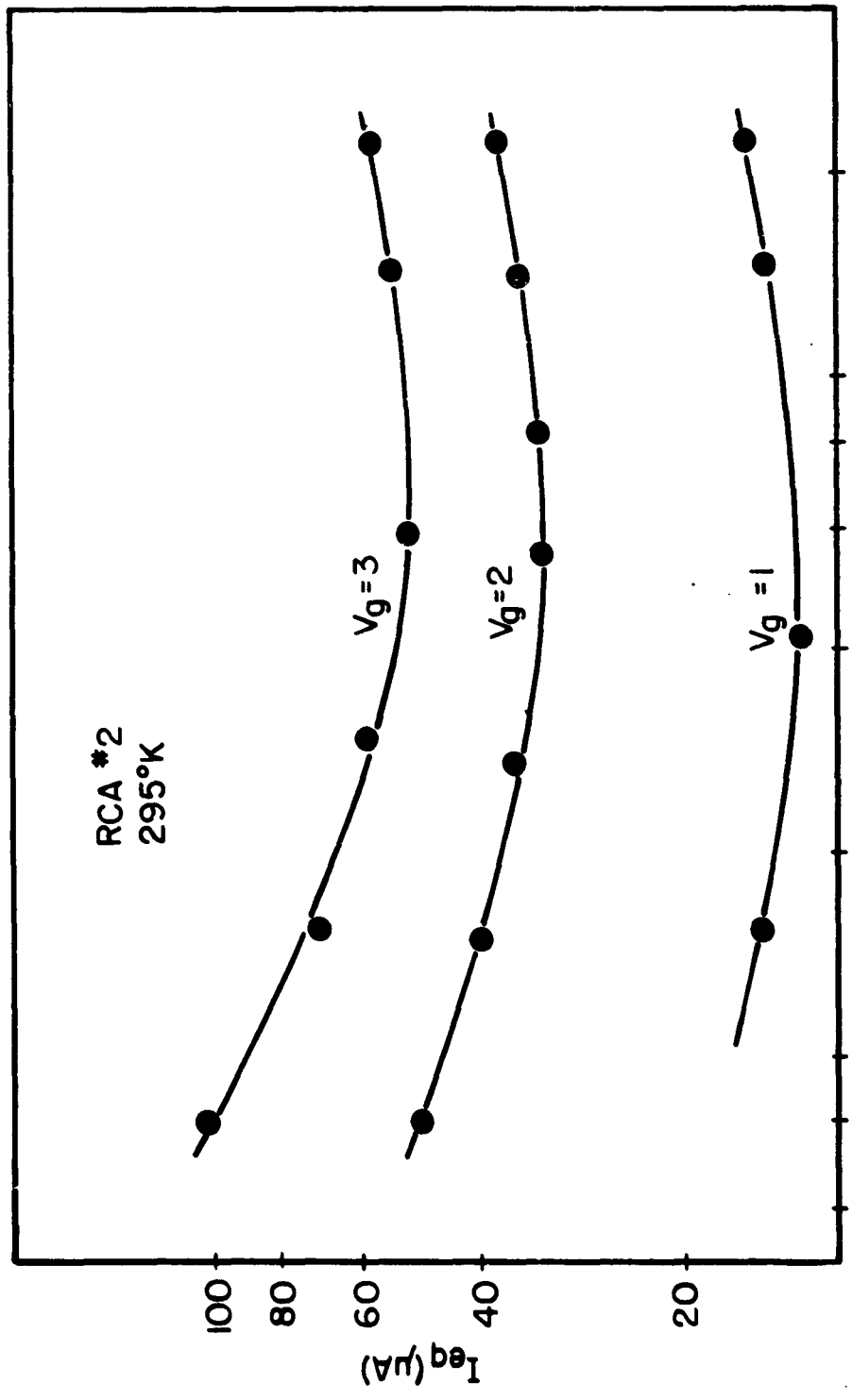


Fig. 18 High frequency noise spectra of the RCA enhancement mode FET

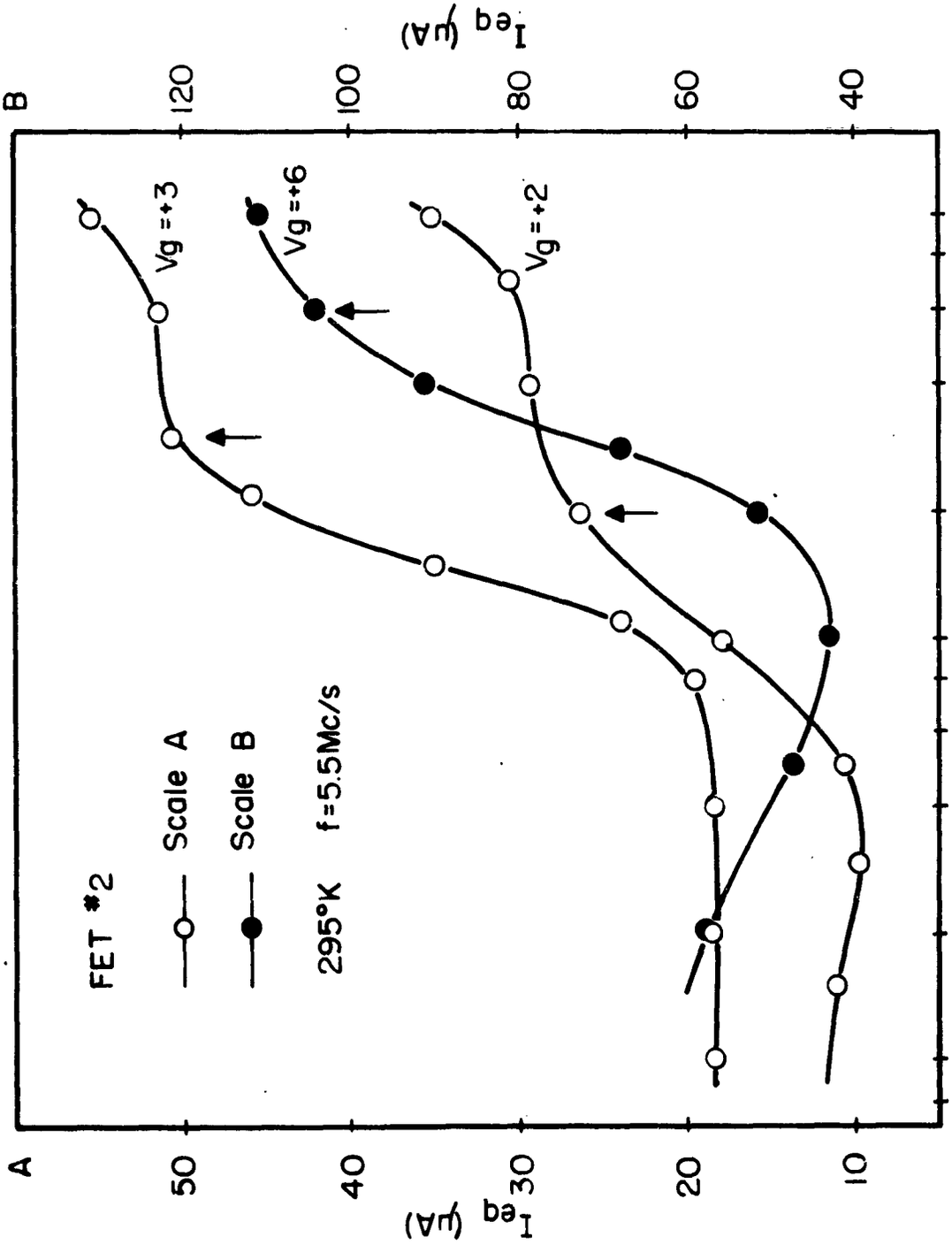


Fig. 19 Dependence of I_{eq} on V_d of the RCA enhancement mode FET

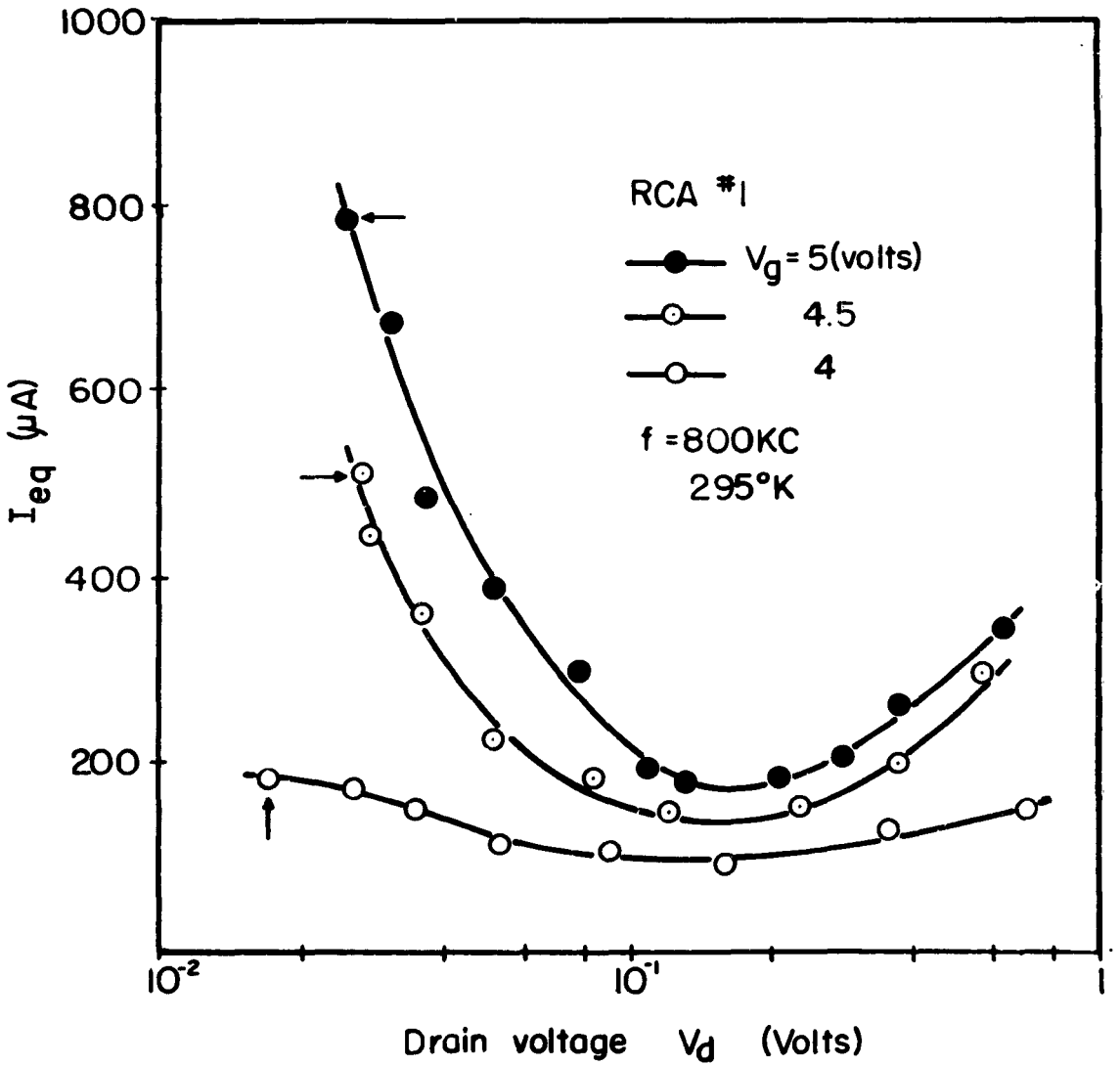


Fig. 20 Dependence of I_{eq} on V_d near V_d=0

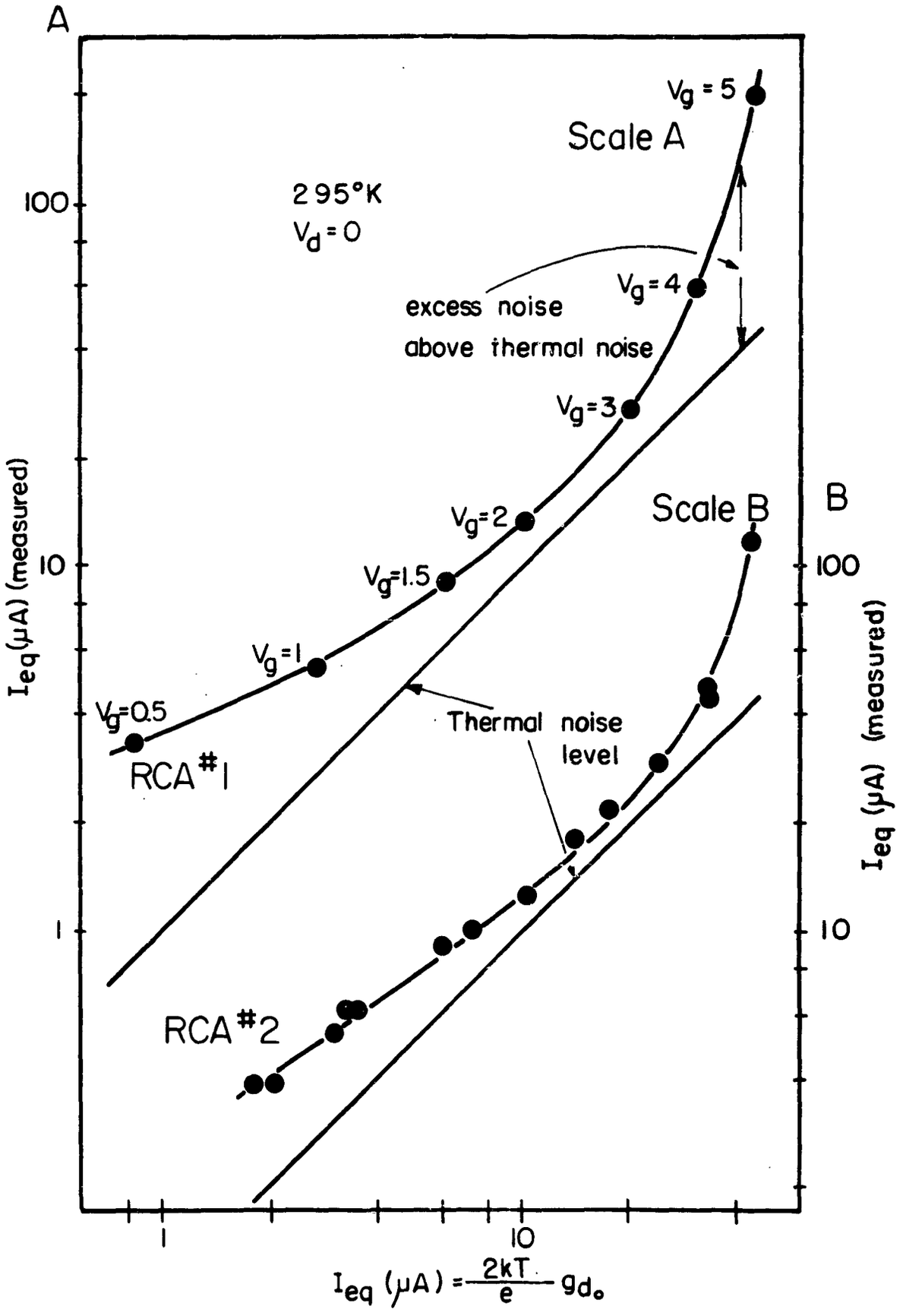


Fig. 21 Noise of RCA enhancement mode FET when $V_d = 0$

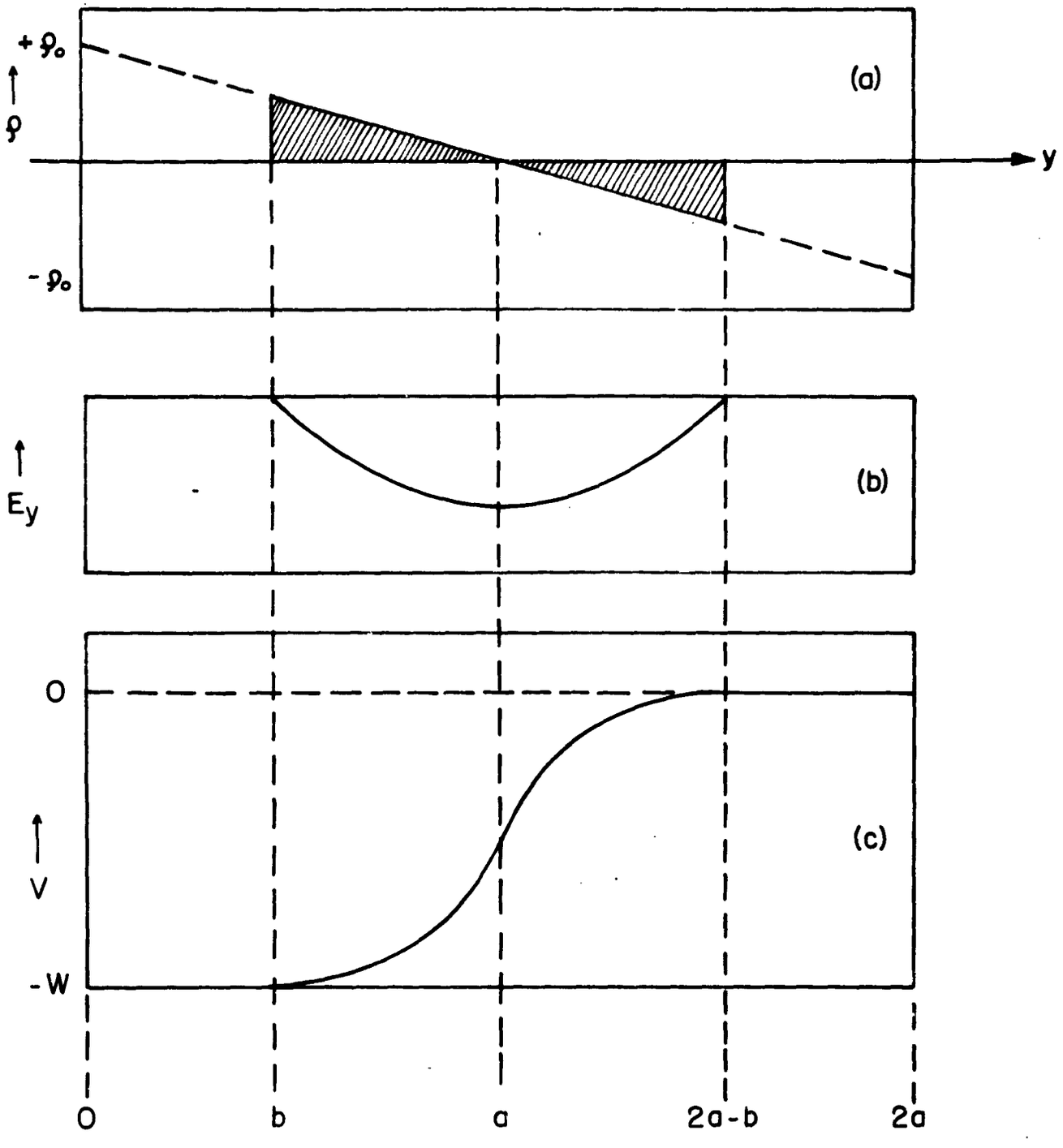


Fig.22 Penetration of the space-charge region into the p and n regions for a linear profile (diffused) junction.

(a) Space charge (b) Electric field (c) Electrostatic potential.

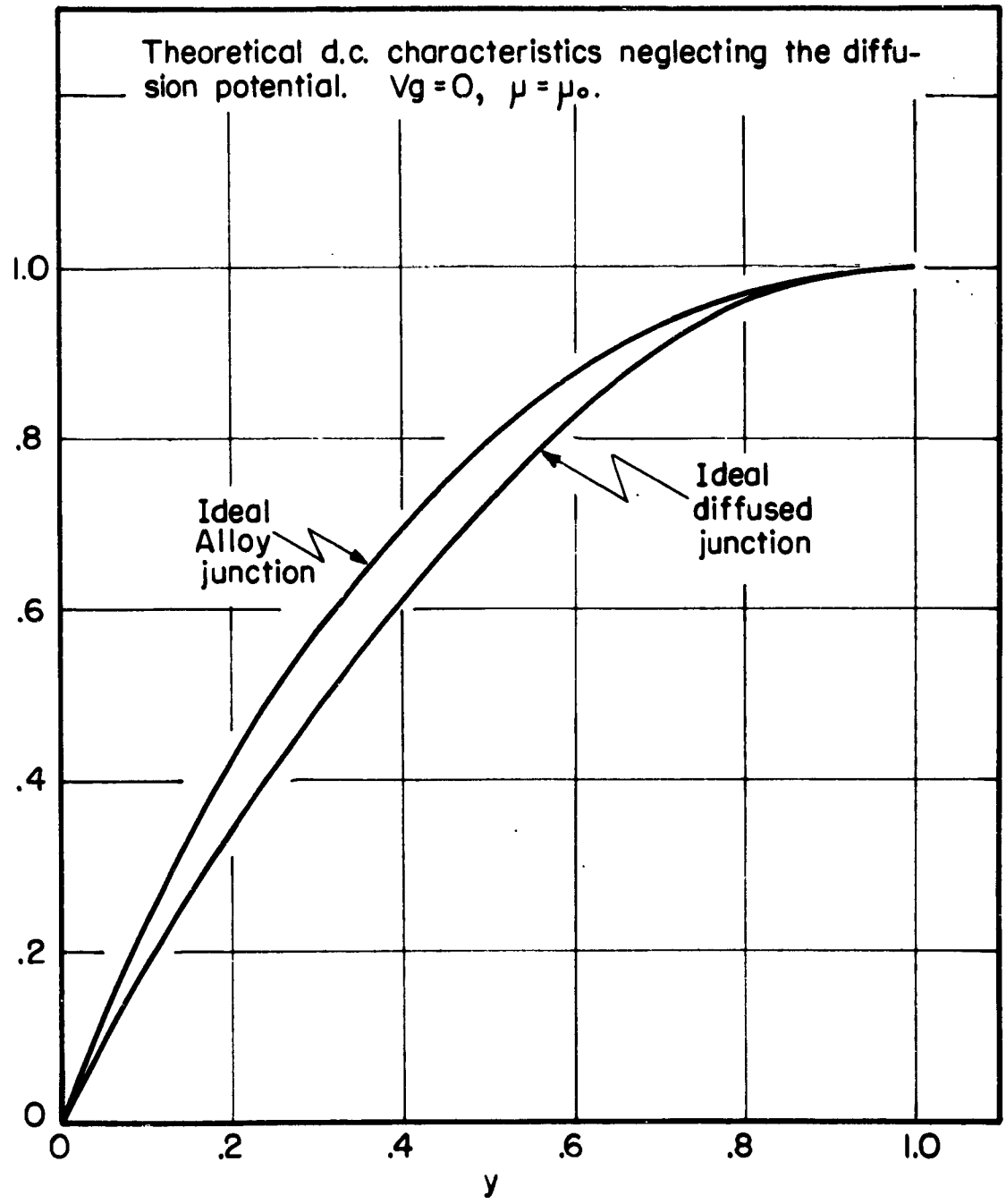

Theoretical d.c. characteristics neglecting the diffusion potential. Vg = 0, μ = μo.
Ideal Alloy junction
Ideal diffused junction
1.0
.8
.6
.4
.2
0
0
.2
.4
.6
.8
1.0
y

Fig. 23

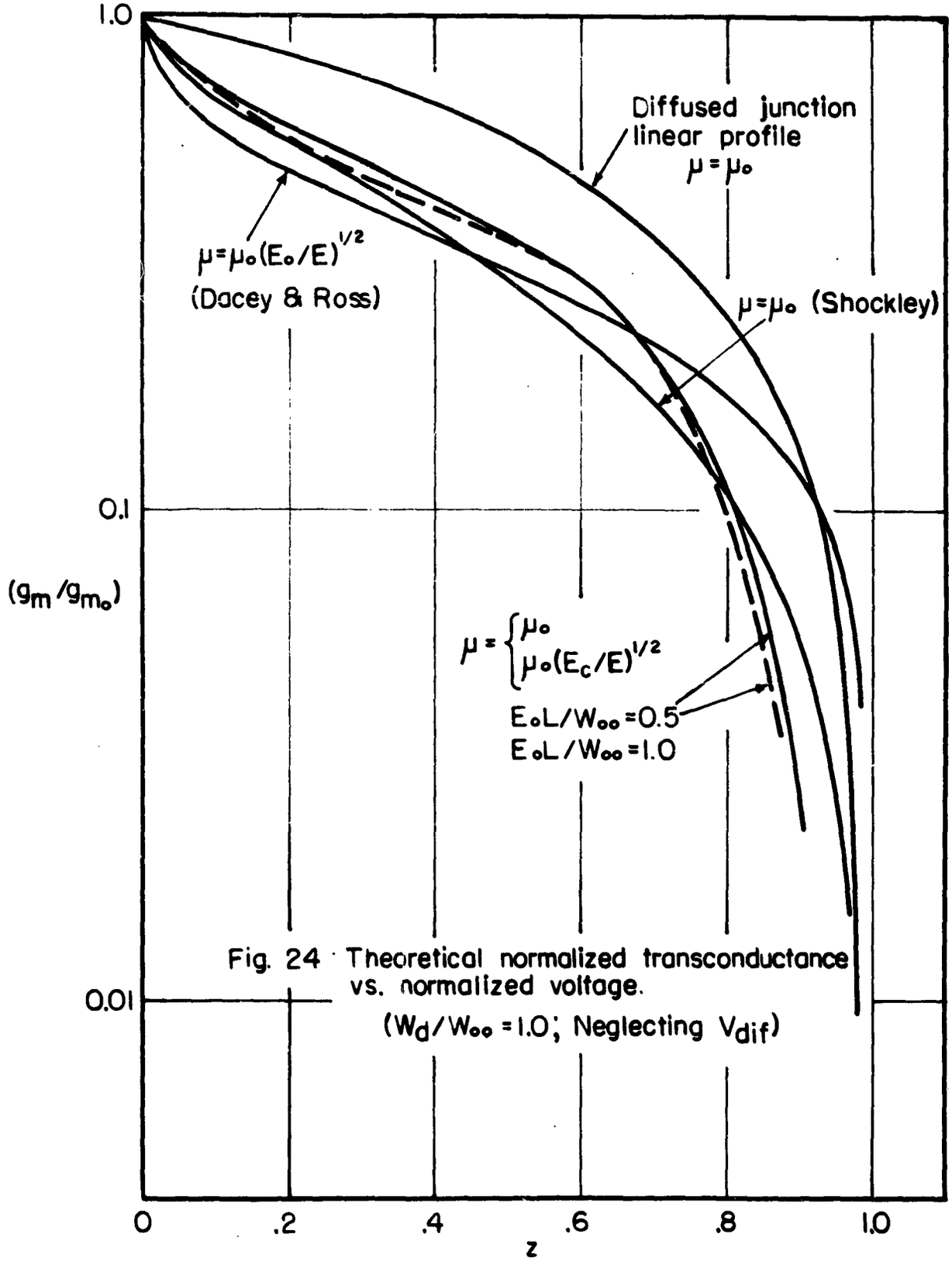


Fig. 24 Theoretical normalized transconductance vs. normalized voltage.
($W_d/W_{oo}=1.0$; Neglecting V_{dif})

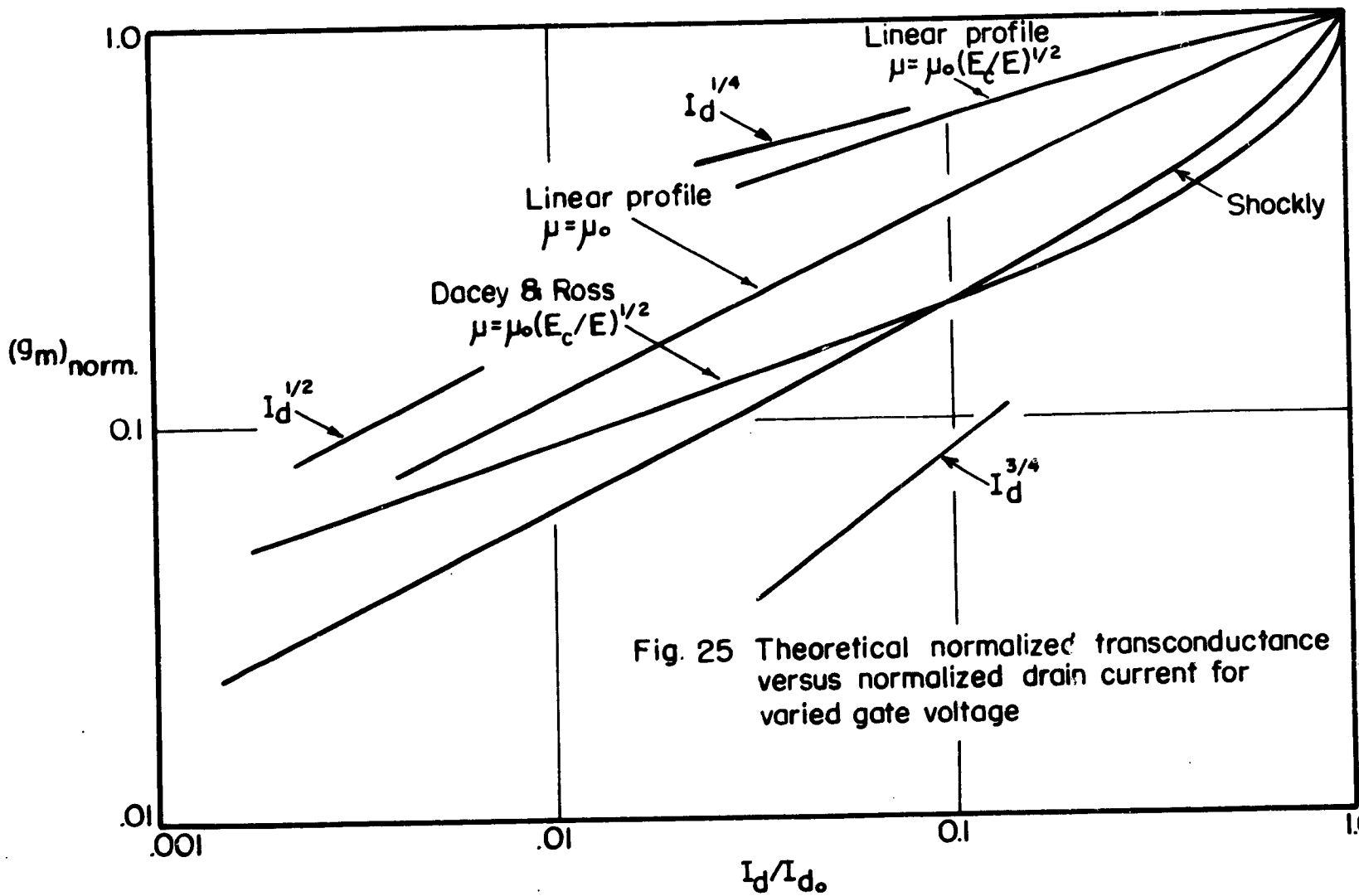


Fig. 25 Theoretical normalized transconductance versus normalized drain current for varied gate voltage

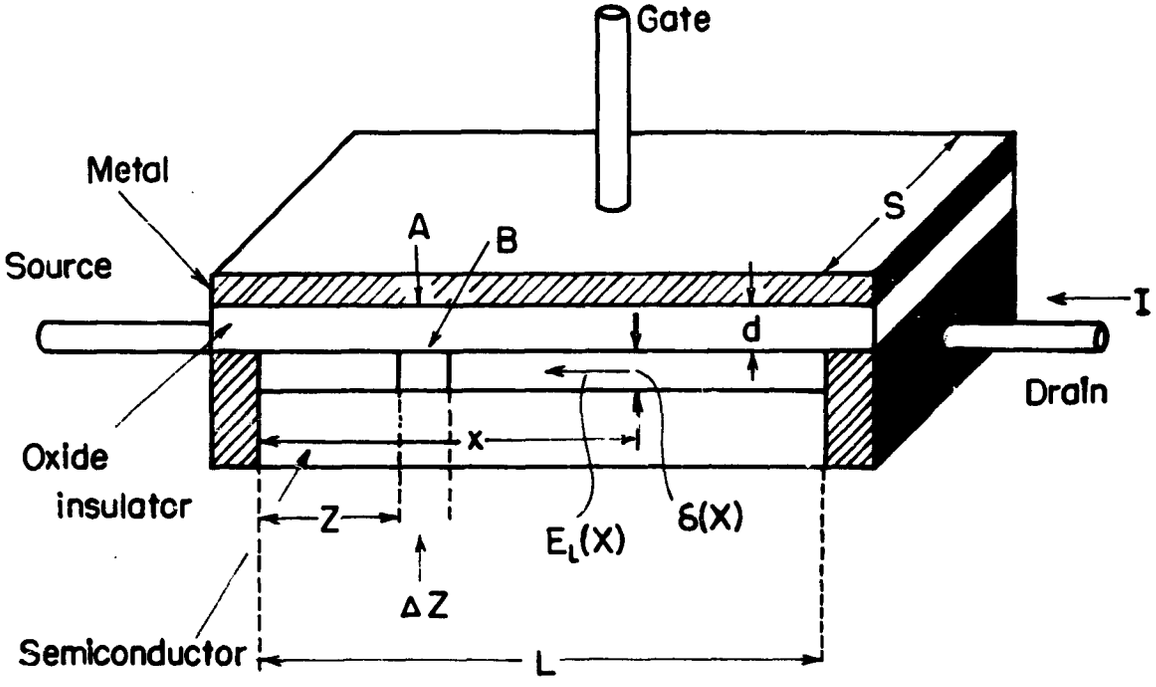
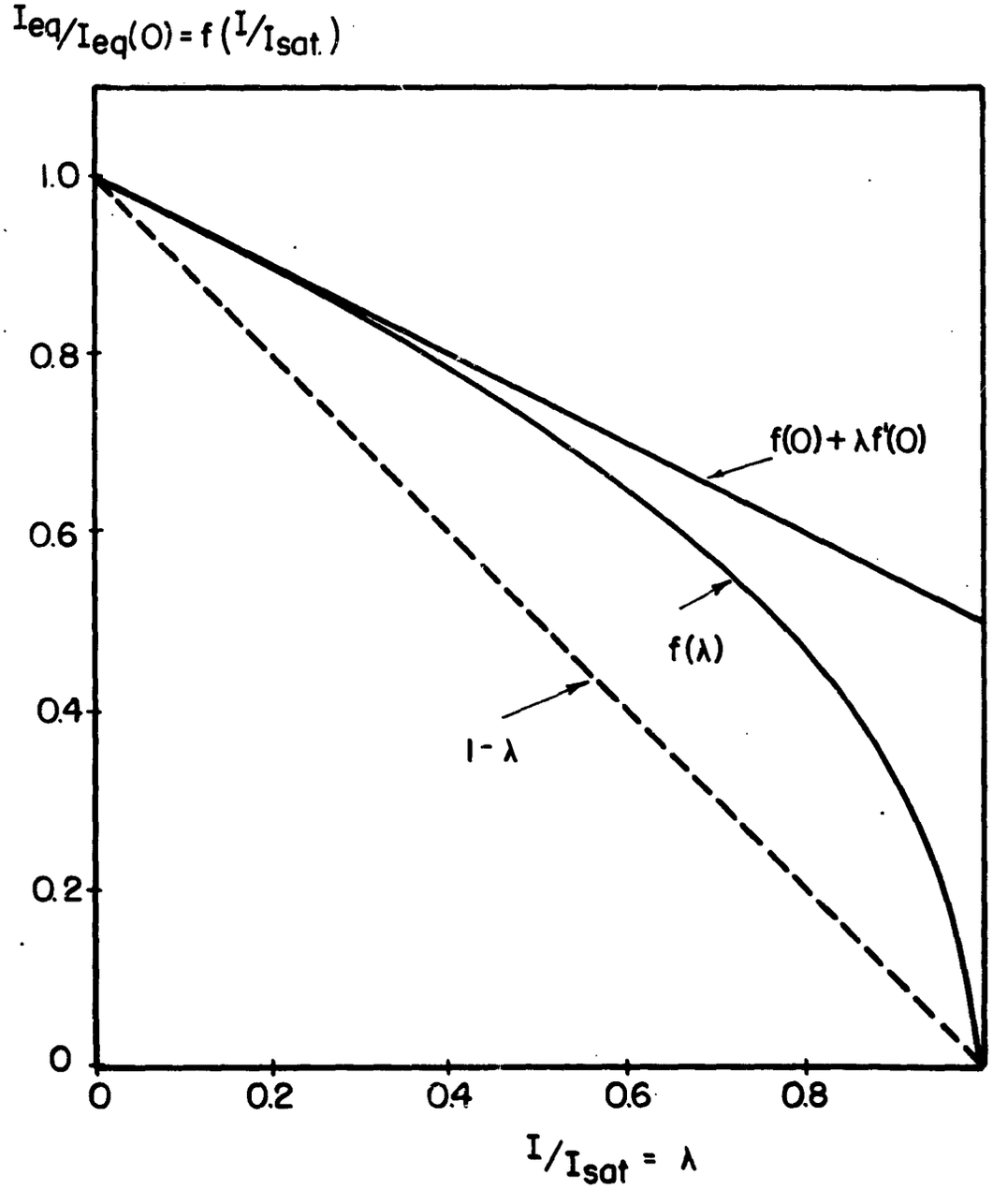


Fig. 26 Enhancement mode FET

ε: dielectric constant of insulator, Q(Z): surface charge density at B, P(Z): volume charge density at B, μ: surface mobility, V(Z): voltage difference between points A and B, Vd: drain voltage, Vg: gate voltage.



$\frac{I_{eq}}{I_{eq}(0)}$ vs $\frac{I}{I_{sat}}$ for enhancement mode FET calculated by thermal noise theory

Fig. 27

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