UNCLASSIFIED

AD 452571L

DEFENSE DOCUMENTATION CENTER

FOR

SCIENTIFIC AND TECHNICAL INFORMATION

CAMERON STATION ALEXANDRIA, VIRGINIA

UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

BY DDC
AD 452571
CATALOGED
AS AD NO.

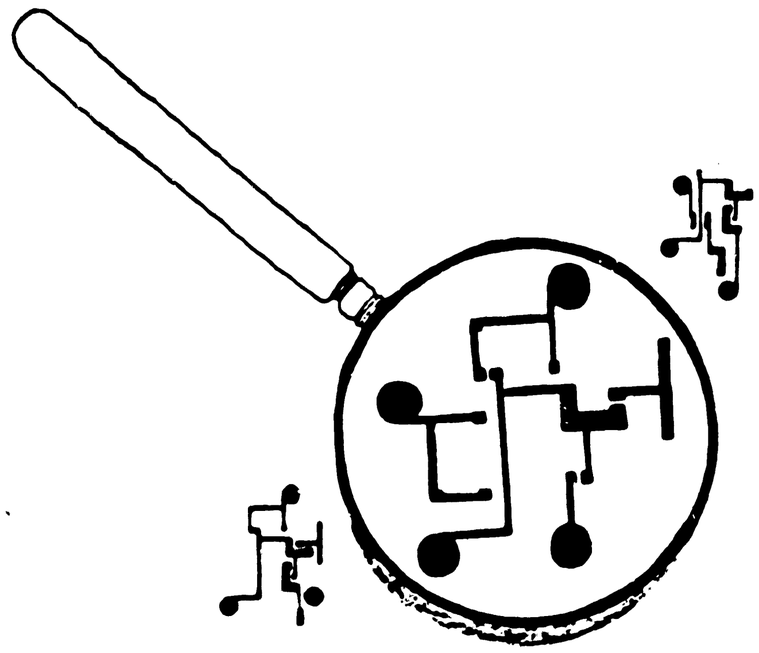
452571L

μ-Notes

INFORMATION ON MICROELECTRONICS
FOR NAVY AVIONICS EQUIPMENT

μ-NOTES NO. 9

1 DECEMBER 1964



PREPARED BY

U.S. NAVAL AMMUNITION DEPOT
CRANE, INDIANA

U.S. NAVAL AIR DEVELOPMENT CENTER
JOHNSVILLE, PENNSYLVANIA

DDC
RECEIVED
DEC 14 1964
DDC-IRA C

QUALITY EVALUATION LABORATORY
NAD Crane
WEPTASK NO. RAV03D001/3231/R008-03-01
Problem Assignment No. 2

AERONAUTICAL AND ELECTRICAL LABORATORY
NADC Johnsville
WEPTASK NO. RAV03J002/2021/R008-03-01
Problem Assignment No. 14

μ-NOTES NO. 9

1 DECEMBER 1964

The Avionics Division of the Bureau of Naval Weapons has embarked upon a program utilizing microelectronics in Airborne electronic equipment. Two BUWEPS field stations, U. S. Naval Ammunition Depot, Crane and U. S. Naval Air Development Center Johnsville, have been assigned tasks implementing the BUWEPS program. The two activities were directed to make information on microelectronics available to Avionics equipment and systems manufacturers by distributing a periodic newsletter.

The purpose of the newsletter, μ-NOTES, is to provide information on evaluation, application, availability, research and development, and standardization activity pertaining to state-of-the-art circuits, devices and materials. Inquiries, comments, or suggestions are invited and should be addressed to the Commanding Officer, U. S. Naval Ammunition Depot, (Code QECA) Crane, Indiana 47522

Approved by:

E. R. PETTEBONE
Commanding Officer
U. S. Naval Ammunition Depot
Crane, Indiana

A. E. PADDOCK
Commanding Officer
U.S. Naval Air Development Center
Johnsville, Pennsylvania

NAD Crane Report No. QE/C 64-782

P R E F A C E

The newsletter, μ-NOTES, is divided into topic sections (Research and Development, Standardization, Evaluation, Application, Availability) containing information of similar nature, in order to provide logical grouping and easy location of articles.

Each article, μ-NOTE, is numbered in the following manner:

First digit - "μ-NOTES" issue number

Second digit - Section number

Third digit - Consecutive number in the section. This will provide easy referral to articles and retain continuity when adding information to previous articles on the same topic.

The contents of this publication have been prepared by the Aeronautical Electronic and Electrical Laboratory, NAVAIRDEVCEN and the Quality Evaluation Laboratory, NAD, under the direction of:

J. H. NAMAROFF, Development Support Division, AEEL,
NAVAIRDEVCEN Johnsville

M. R. BUFFINGTON, Aircraft Equipment Branch, QEL,
NAD Crane

N O T I C E

Publication of data in the μ-NOTES or comments regarding the products of any manufacturer does not constitute exclusive acceptance, approval or disapproval by the Government of the vendors products.

C O N T E N T S
μ-NOTES NO. 9

		Page
PREFACE		i
NOTICE		ii
SECTION 1 - RESEARCH AND DEVELOPMENT		1.0.0
μ-NOTE 911	Microelectronic Power Supply Program	1.1.0
μ-NOTE 912	Resume of Epitaxial Studies Report (Part 1)	1.2.0
SECTION 2 - STANDARDIZATION		2.0.0
	No additional information available for this issue.	
SECTION 3 - EVALUATION		3.0.0
μ-NOTE 931	Evaluation of Siliconix Digital Microelectronic Functional Devices	3.1.0
μ-NOTE 932	Evaluation of General MicroElectronics Digital Microelectronic Functional Devices	3.2.0
μ-NOTE 933	Evaluation of Sylvania Digital Microelectronic Functional Devices	3.3.0
SECTION 4 - APPLICATION		4.0.0
μ-NOTE 941	Failure Analysis and Reliability Estimates of AN/ASW-25(XN-) Microelectronic Digital One-Way Data Link	4.1.0
SECTION 5 - AVAILABILITY		5.0.0
μ-NOTE 951	Compilation of Microelectronic Functional Devices Evaluated to Date	5.1.0

Section 1

RESEARCH AND DEVELOPMENT

Section 1 - Research and Development

μ-Note 911

Microelectronic Power Supply Program

The objective of this program, under contract NOw 63-0749-di, and described briefly in μ-Note 811, was to standardize regulated voltage power supplies to be used in conjunction with microelectronic circuitry, a reduction in size and weight, and an improvement in efficiency and MTBF over available hardware.

Voltages and their regulation for the six different modules were also contained in μ-Note 811.

The modules were packaged in sizes ranging from 7 to 15 cubic inches for power ratings from 6 to 60 watts. Figures 1 through 4 show the final version of the experimental models, the first of three developmental stages of this contract. The final versions of the succeeding developmental models will contain simplified circuitry and will use greater efficiency in packaging.

No forced air cooling or external means, other than a heat sink, is necessary. The specified cooling requirements indicate meeting the requirements of MIL-E-5400 for Class 3 equipment except that the maximum temperature of the supply mounting plate will be +55°C, and the maximum temperature of the surrounding ambient air will be +85°C. Internal cooling is provided by conduction paths to the base plate of the power supply.

Figures 5 and 6 show the final production version of the power supply developed for the one-way Data Link equipment, AN/ASW-25(XN-1), under a NAVAIRDEVCEN contract.

FIGURE 1 - Experimental Models -
6W to 60W

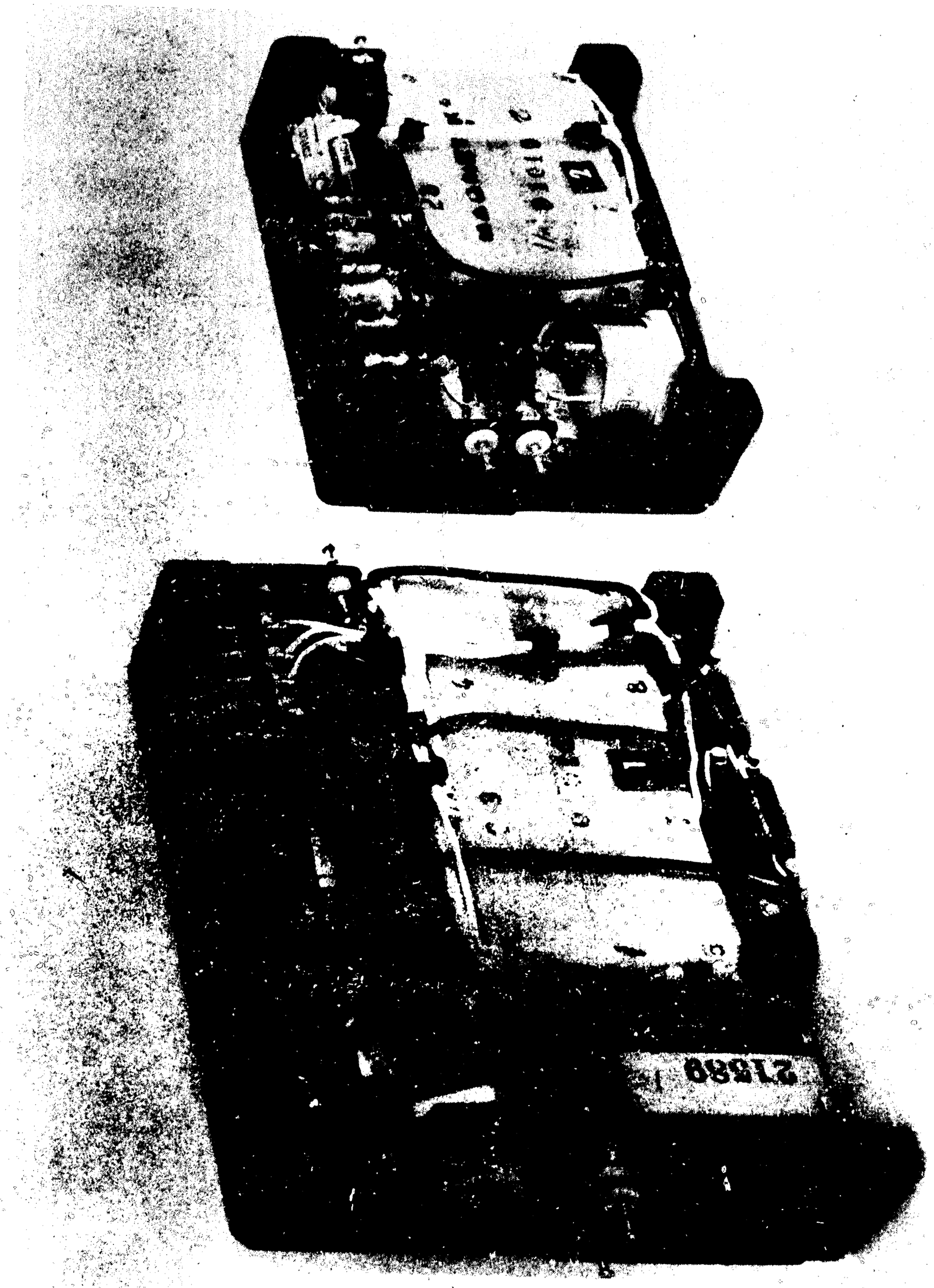


FIGURE 2 - Comparison of GOV to G

FIGURE 3 - Size Portrayal of 60M Module

FIGURE 4 - Comparison to Conventional Laboratory Power Supply

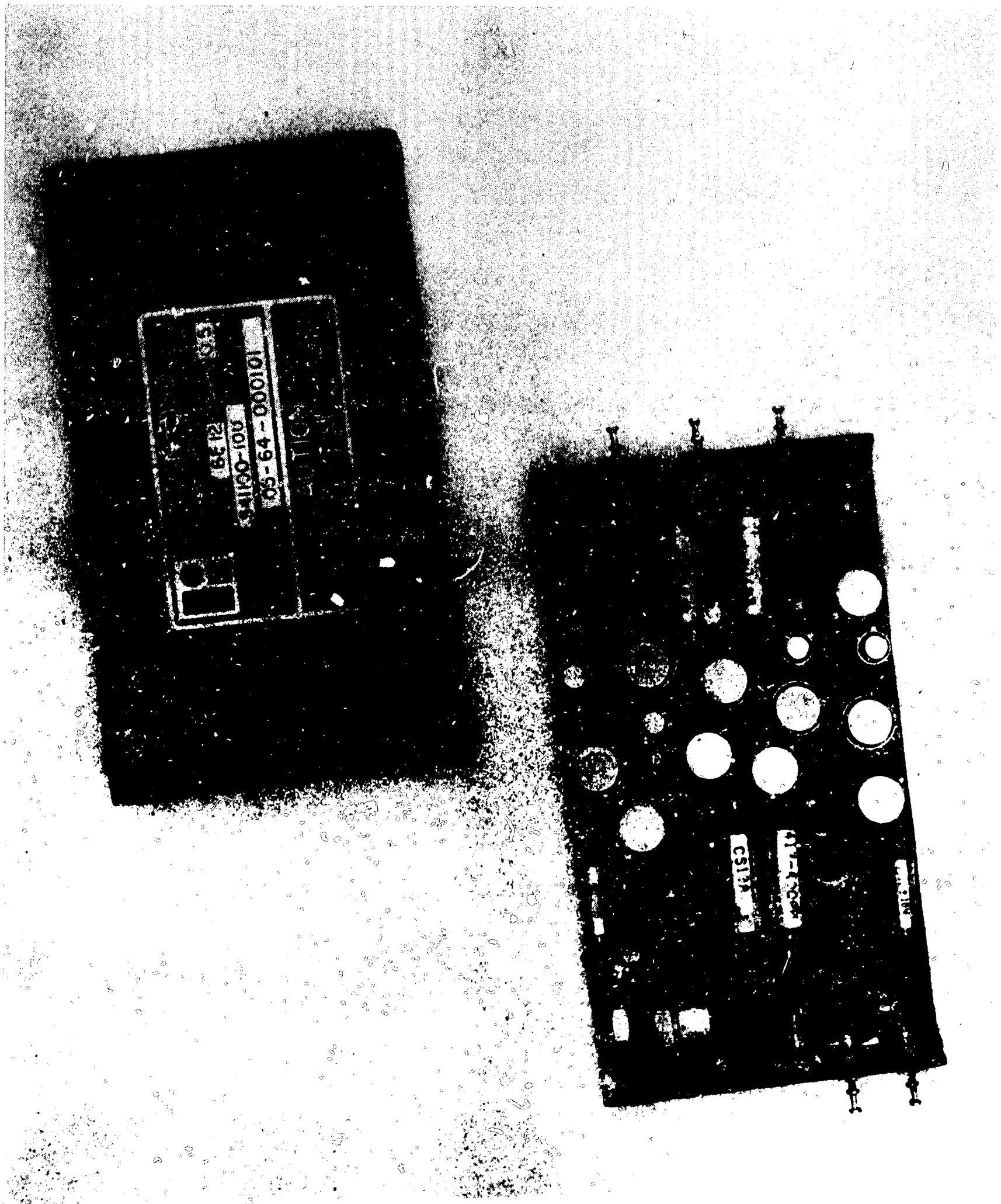


FIGURE 5 - Data Link Version Module

FIGURE 6 - Size Portrayal of D-L Module

μ-Note 912

Resume of Epitaxial Studies Report - Part I

Battelle Memorial Institute under NAVAIRDEVCEN Contract N62269-2470 prepared a Special Report on Microelectronic Studies entitled Epitaxial Studies. This report consists of a summary of the many articles which have appeared in the literature on epitaxial films on semiconductors in recent years and describes the bibliography covering different aspects of epitaxy.

This μ-Note will present the first part of this report and will consist of the Introduction, Summary and Background.

Introduction

The semiconductor industry is one in which the technologies used are subject to refinement and change continuously. The introduction of epitaxial technology for fabrication of semiconductor devices in the early 1960's represents a step forward for the industry because of the additional possibilities for devices that the technology offers. However, as with any new technology, there are many aspects and variations to be explored; consequently a considerable number of papers on the subject have appeared in the literature during the last four years. It was decided that this would be an opportune time to review the state-of-the-art. In this report, more than 100 papers have been reviewed and classified as to subject matter in a bibliography. The opportunity was taken to assess the state-of-the-art for different aspects of epitaxy which have potential semiconductor device applications. The state-of-the-art assessment forms the major part of this report, and the bibliography forms the supporting part.

Summary

The process of epitaxial growth has permitted production of transistors and microcircuits of superior characteristics compared to those which had been made before the development of this process. It makes possible devices such as heterojunctions and retrograde junctions which cannot be formed by other methods. It permits the growth of thin single crystalline semiconductor films which are of controlled resistivity and thickness and relatively free of lattice imperfections.

There are many techniques which can be used to deposit epitaxial films. The most important at the present time appears to be the hydrogen reduction of silicon tetrachloride. The hydrogen reduction of trichlorosilane and decomposition of silane have been used to a lesser extent. Germanium can be deposited by hydrogen reduction of germanium tetrachloride or disproportionation of germanium di-iodide. It is also possible that vacuum evaporation of silicon and germanium on single-crystal substrate will prove to be a useful technique, especially since vacuum evaporation is already widely used in microcircuit fabrication.

There are still many unknown factors involved in the epitaxial deposition of thin films of silicon on silicon substrates. The cause of these stacking faults is not yet established. The actual reaction taking place at the gas substrate interface has not been well defined. The control of thin film resistivity and thickness is not as good as desired. Therefore, it seems likely that epitaxial growth will be a subject of continued research for some time in the future.

Background

The term epitaxy ("orderly arrangement on") was introduced by L. Royer in 1928 to denote the phenomenon of oriented growth of one crystal onto another. This was first found to occur naturally on certain materials; two crystals of different species had grown together with a definite unique orientation relationship between their crystal axes.

The first successful attempt to produce epitaxial growth in the laboratory was apparently made by Frankenheim in 1836 who grew sodium nitrate from a water solution in perfect orientation onto a calcite crystal. Other methods which have subsequently been successful in producing epitaxial layers are:

1. Electroplating
2. Vacuum evaporation
3. Sputtering
4. Chemical reaction - For example, if a single crystal of silver is placed in a solution of chlorine in water, an epitaxial deposit of silver chloride grows on the crystal surface.
5 Chemical vapor deposition - This is a process wherein a material is deposited onto a surface as a result of chemical reactions between gaseous reagents taking place preferentially on the surface. This process has been used almost exclusively for the epitaxial deposition of germanium and silicon onto parent substrates for electronic device fabrication.

The successful achievement of an epitaxial deposit depends on satisfying certain requirements involving the structural nature and material of the surface on which deposition is proceeding, the surface

temperature, and the rate of deposition. If these requirements are not met, the resulting deposit will be polycrystalline or amorphous. Partial orientation may also occur in which only one crystal direction in the deposit bears a unique relation to the crystal axes of the substrate, and this is termed "partial epitaxy." For complete epitaxy, all three crystal axes in the deposit should be related to the substrate crystal axes.

Isoepitaxy is a term used to denote the growth of a layer onto a substrate of the same material, and this is often done in semiconductor device fabrication, as when n-type silicon is deposited epitaxially on a p-type silicon substrate.

Rheotaxy is a term recently coined to describe the growth of a solid, single-crystal deposit on a substrate which, at the elevated temperatures used for deposition, is covered with a liquid glaze.

Future issues of μ-Notes will contain additional information regarding the epitaxial process.

Section 2

STANDARDIZATION

Section 3

EVALUATION

EVALUATION OF SILICONIX INC. "A" SERIES INTEGRATED DIGITAL CIRCUITS

"A" SERIES INDEX

	Page
Circuit Description	3.1.1
Circuit Tests	3.1.2
Circuit Performance	3.1.3
A02 Dual Power Gate Characteristic Data and Graphs	3.1.5
A03 Counter Shift-Register Circuit Characteristic Data and Graphs	3.1.19
A04 Diode Array Characteristic Data and Graphs	3.1.31
A05 Dual Line Driver Characteristic Data and Graphs	3.1.34
A08 Monostable Multivibrator Characteristic Data and Graphs	3.1.45
A20 Dual NAND/NOR Gate Equivalent Circuit and Siliconix Test Circuits and Waveform Definitions	3.1.56

INVESTIGATION OF SILICONIX INCORPORATED "A" SERIES LCDTL INTEGRATED CIRCUITS

I. Circuit Description

A. This family of circuits is designed around the basic NAND Gate shown in Figure 3.1.1. Each type is a true monolithic integrated circuit, i.e., all active and passive components in the circuit are produced integrally with, and inseparable from, the substrate. All circuits use epitaxial transistors. Multiple diffusions are used to complete the active and passive circuit components. The structures are packaged in either modified TO-5 cans or in flat pack form for higher density systems.

B. The siliconix DTL Gate has two circuit-design modifications from conventional DTL circuits. They are: (1) the addition of emitter follower Q_1 to relax gain restrictions and (2) the use of clamping diode D_3 to prevent inverter saturation. These modifications have led to the term load compensated DTL or LCDTL.

C. The Siliconix family of DTL circuits consists of the following units.

1. A02 and A07 - Dual Power Gate and Dual NAND/NOR Gate. The A02 and A07 circuits are identical except for fan-out. The A02 can drive a fan-out of 15 and the A07 can drive a fan-out of 5. See Figure 3.1.1.

2. A01 and A06 - Single Power Gate and Single NAND/NOR Gate. The A01 and A06 Single NAND/NOR Gates have the same electrical characteristics as the A02 and A07 dual gates with the addition of a fan-in expansion terminal. See Figure 3.1.1. The A01 and A06 are identical, except for fan-out. The A01 and A06 have fan-out capabilities of 15 and 5 respectively.

3. A03 - Counter, Shift-Register Circuit. The A03 is a flip-flop for use in counter and register applications. Designed for use with a single-phase clock, the A03 may be operated asynchronously or synchronously. Eight separate inputs can be connected to implement a variety of logic functions. The A03 is a monolithic array of six direct-coupled NAND Gates. See Figure 3.1.11 for a block diagram of the circuit and the truth table defining its operation.

4. A04 - Diode Array. The A04 is a diode array used to extend single gate fan-in (A01 and A06) ir increments of six, to a limit depending upon input loading and circuit speed. See Figure 3.1.19.

5. A05 - Dual NAND/NOR Gate Line Driver. The A05 is identical to the A07 Dual NAND Gate with the addition of an internally connected pull-up resistor (See Figure 3.1.21) which provides a charge path for capacitive loads and increases the high output level.

6. A03 - Monostable Multivibrator. The A08 is a six-gate array connected to perform the one-shot function. Delays are implemented by connecting external capacitors from D-D' to ground. Three inputs and complimentary outputs are provided to increase the circuits' versatility. See Figure 3.1.28.

7. A20 - Dual NAND/NOR Gate. The A20 is a selected dual NAND/NOR Gate for special applications such as buffers and FET commutator drivers. Selection is based on BV_{cex} of Q_2. When used with external load resistors and an external source voltage, V_s, an output voltage swing of 15 volts is possible. See Figure 3.1.35.

II. Circuit Tests.

A. The D-C characteristics of the Siliconix A series of LCDTL circuits were obtained using a transistor curve tracer. Six curves make up the family of D-C characteristics. They are as follows: (1) V_{in} vs V_{out}, (2) I_{in} vs V_{out}, (3) V_{in} vs I_{in}, (4) V_{out} vs I_{out}, (5) V_{cc} vs V_{out} and (6) V_{cc} vs I_{cc}. Temperature was used as a parameter on those curves where important variations were noted. Included in the information obtainable from these curves are: (1) the worst-case output voltage under full load, (2) maximum low or "false" output voltage, (3) minimum high or "true" output voltage, and (4) worst-case input current.

The curves plus any necessary explanation are presented with the data for each device.

Due to the identical nature of some of the devices (see the equivalent circuits, Figure 3.1.1) only the following were tested.

(1) A02 - Dual Power Gate
(2) A03 - Counter, Shift Register Circuit
(3) A05 - Dual NAND/NOR Gate Line Driver
(4) A04 - Diode Array
(5) A08 - Monostable Multivibrator

B. Dynamic tests were performed on four of the seven designated types of circuits manufactured by Siliconix. Tests on all types would have been redundant because of the similarity noted previously. The circuits dynamically tested were the A02 Dual NAND/NOR Power Gate, Figure 3.1.1; the A03 Counter, Shift-Register Circuit, Figure 3.1.11; the A05 Dual NAND/NOR Gate Line Driver, Figure 3.1.21; and the A08 Monostable Multivibrator, Figure 3.1.28.

Tests on the gates consisted of measuring pulse amplitude, pulse width, rise time, fall time, delay time, storage time, and propagation delay. These measurements were made with fan-outs of 1, 5, and maximum, at bias voltages (V_{cc}) of 4, 5 and 6 volts, and temperatures of -55, -40, 25, 85 and 125°C. A block diagram of the test set-up is shown in Figure 3.1.5 Definition of the measured parameters (rise time etc.) is given in Figure 3.1.6.

Tests on the flip-flop consisted of measuring the same parameters as measured on the gates with the exception of set-up time which was determined instead of propagation delay. These measurements were again determined at the various values of fan-out, bias voltage, and temperature. Figure 3.1.14 shows a block diagram of the test set-up and Figure 3.1.15 defines the measured parameters.

The A08 monostable multivibrator was tested by measuring pulse amplitude, pulse width, rise time, fall time and delay time. These measurements were made with external capacitances from D-D' to ground of 113 and 226 pico-farads. Measurements for each value of capacitance were obtained at bias voltages of 4, 5, and 6 volts and temperatures of -55, -40, 25, 85 and 125°C. The minimum pulse widths at the complimentary outputs (open circuit from D-D' to ground) were measured for each condition of bias voltage and temperature. All tests were performed at a fan-out of one from each output. Figure 3.1.32 shows a block diagram of the test set-up and Figure 3.1.33 defines the measured parameters.

III. Circuit Performance.

A. General observations made while performing tests on Siliconix "A" Series LCDTL integrated circuits are listed below together with any comments.

1. From the block diagrams of the test set-ups shown in Figures 3.1.5, 3.1.14 and 3.1.32 it can be seen that the test circuitry consisted of essentially three Siliconix A type circuits in series. The first circuit is termed the driver unit, the second the test unit, and the third the load unit(s). It will be noted that all units were enclosed in the temperature chamber and hence changes noted in the test circuit performance as a function of temperature (all data was acquired from the "test circuit") were due in part to changes in the associated circuitry. This is also true for changes due to bias supply, variations, i.e., all units were connected to the same supply and were subjected to the same variations. It is felt that testing in this manner produces results more typical to system performance than if isolated circuits were tested.

2. A characteristic of the LCDTL circuits was ringing on the lower voltage level of the output pulse. See oscillographs accompanying the data sheets. This ringing, which is attributed to the diode D_3, of Figure 3.1.1, was found to increase with decreasing temperature. It was also noted to decrease with increasing fan-out or with decreasing bias supply, V_{CC}. The ringing is a noticeable characteristic of the circuits when viewed on an oscilloscope but it did not have any apparant adverse effect on circuit operation. The ringing is not propagated from one circuit to another but is generated in each individual circuit. This is shown by the fact that in a NAND Gate a low voltage input (with ringing) produces a high voltage output with no ringing.

During the discussion of the data in this report with Siliconix engineers it was learned that a mask change and a process change has been introduced to reduce the ringing noted above. The results are shown in Figure 3.1.9.

3. As has been the case in several previous issues of μ-NOTES, the definitions of the various time parameters used by this facility and those used by the manufacturer have been different. Siliconix uses definitions shown in Figure 3.1.36 for the dynamic parameters.

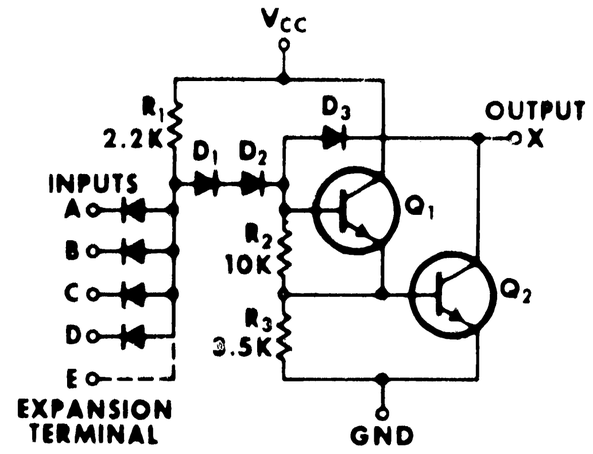
The waveforms used in this report are defined in Figures 3.1.6, 3.1.15 and 3.1.33. Generally speaking, the time definitions used for the gate circuits are more severe than those imposed by Siliconix and those used for the flip-flop are less severe. Comparison of data published by the manufacturer and that shown in this report should be done with the above mentioned differences in mind.

4. Data on circuit performance as a function of fan-in was not acquired. It was found that differences in circuit performance with fan-ins ranging from one to four (the A01 and A06 were not tested) was negligible.

Multiple fan-ins from circuits not utilizing pull up resistors in the output transistor collector circuits, produce the result that no output can go to its high voltage level unless all outputs connected to that particular fan-in array are also high. This is true for all DTL circuits, not only the A series of Siliconix. This fact is mentioned because of the effect noted on the performance of the flip-flop and one-shot circuits which are arrays of NAND Gates. In the case of the flip-flop, the SI logic input which was supplied by a type A02 gate would not go high until after the clock pulse went low if the clock pulse was present during the transient of the logic input from its low to its high state. See Figures 3.1.11, 3.1.14 and 3.1.18. In the case of the one-shot, the $\overline{T}$ input, which was also supplied by an A02 gate, would not go high until after the $\overline{Q}$ output went high. See Figures 3.1.28, 3.1.32 and 3.1.34. If any undesireable results were found because of the above mentioned characteristics they could be easily corrected by using the A05 units (with pull up resistors in the output transistor collector circuits) in place of the A02 units as driver circuits to the devices in question (A03 and A08).

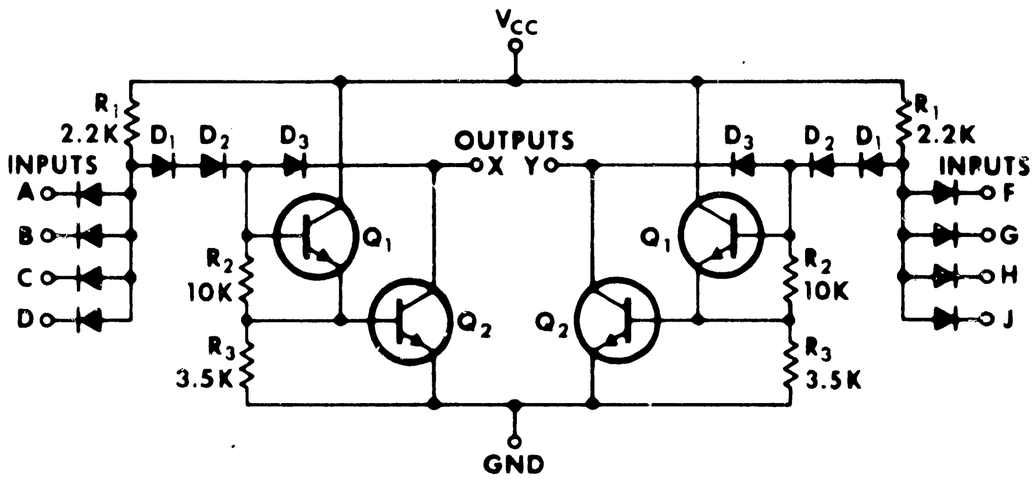
AO2 Dual Power Gate
Characteristic Data and Graphs

CIRCUIT DIAGRAMS



A01 & A06

SINGLE GATE



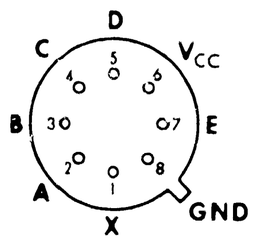
A02 & A07

DUAL GATE

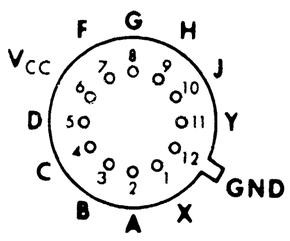
Figure 3.1.1

PIN DIAGRAMS

A01A & A06A



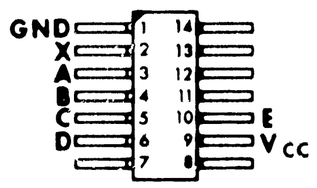
A02A & A07A



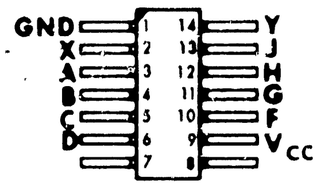
BOTTOM VIEWS

MODIFIED TO-5

A01F & A06F



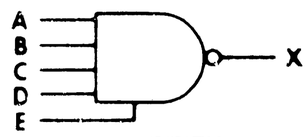
A02F & A07F



TOP VIEWS

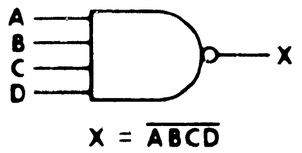
FLATPAC

LOGIC DIAGRAMS

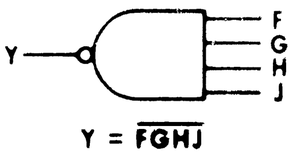


$X = \overline{ABCD}$

SINGLE GATE



$X = \overline{ABCD}$



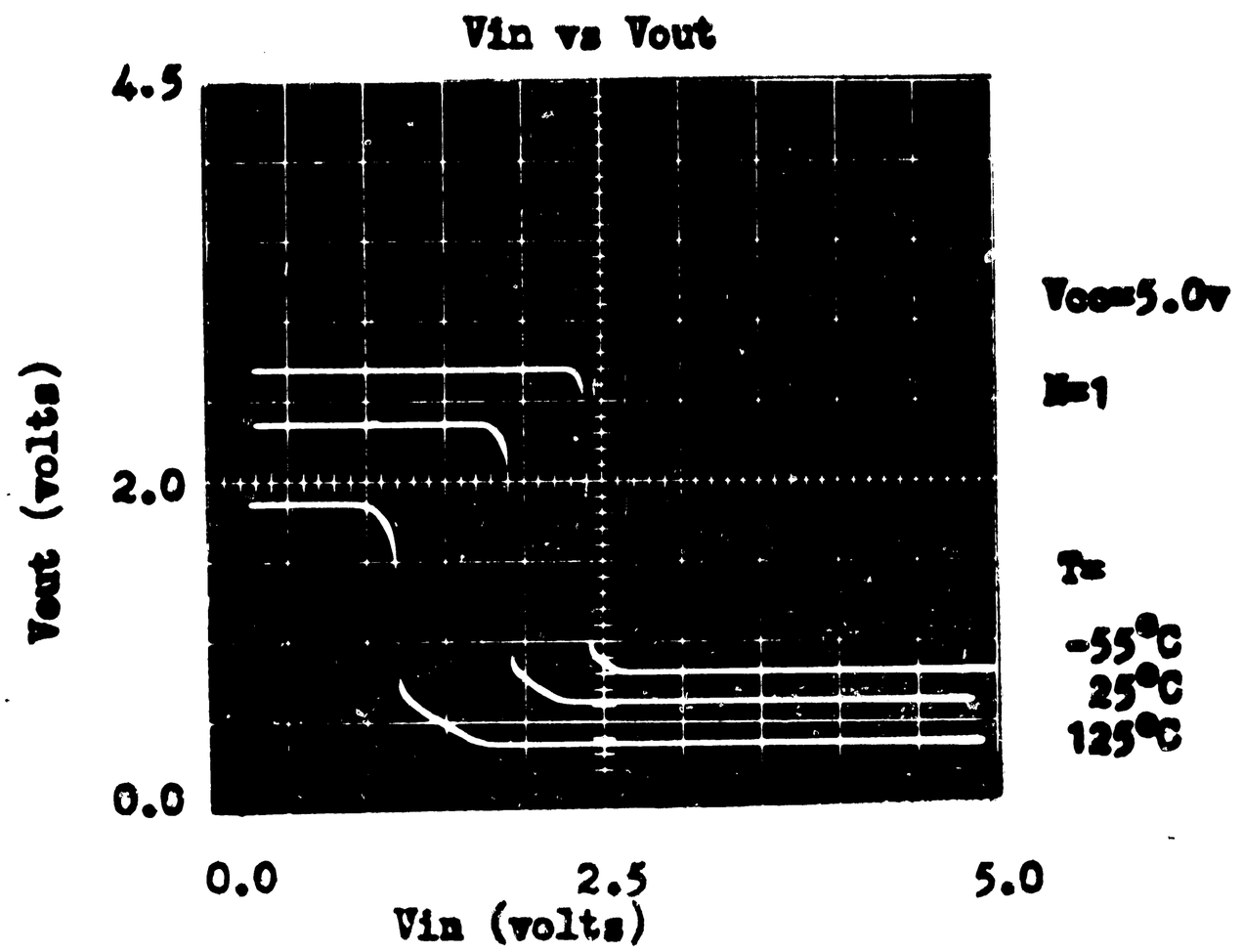
$Y = \overline{FGHJ}$

DUAL GATE

ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC}	6 v
Input Voltage BV_i	6 v
Output Voltage BV_o	6 v
Operating Temperature Range T_A	−55 to +125°C
Storage Temperature Range T_S	−65 to +150°C
Output Current	50 ma

Voltage at any pin must be positive with respect to the common terminal.


Vin vs Vout
4.5
2.0
0.0
Vout (volts)
0.0
2.5
5.0
Vin (volts)
Vcc=5.0v
N=1
Tc
-55°C
25°C
125°C

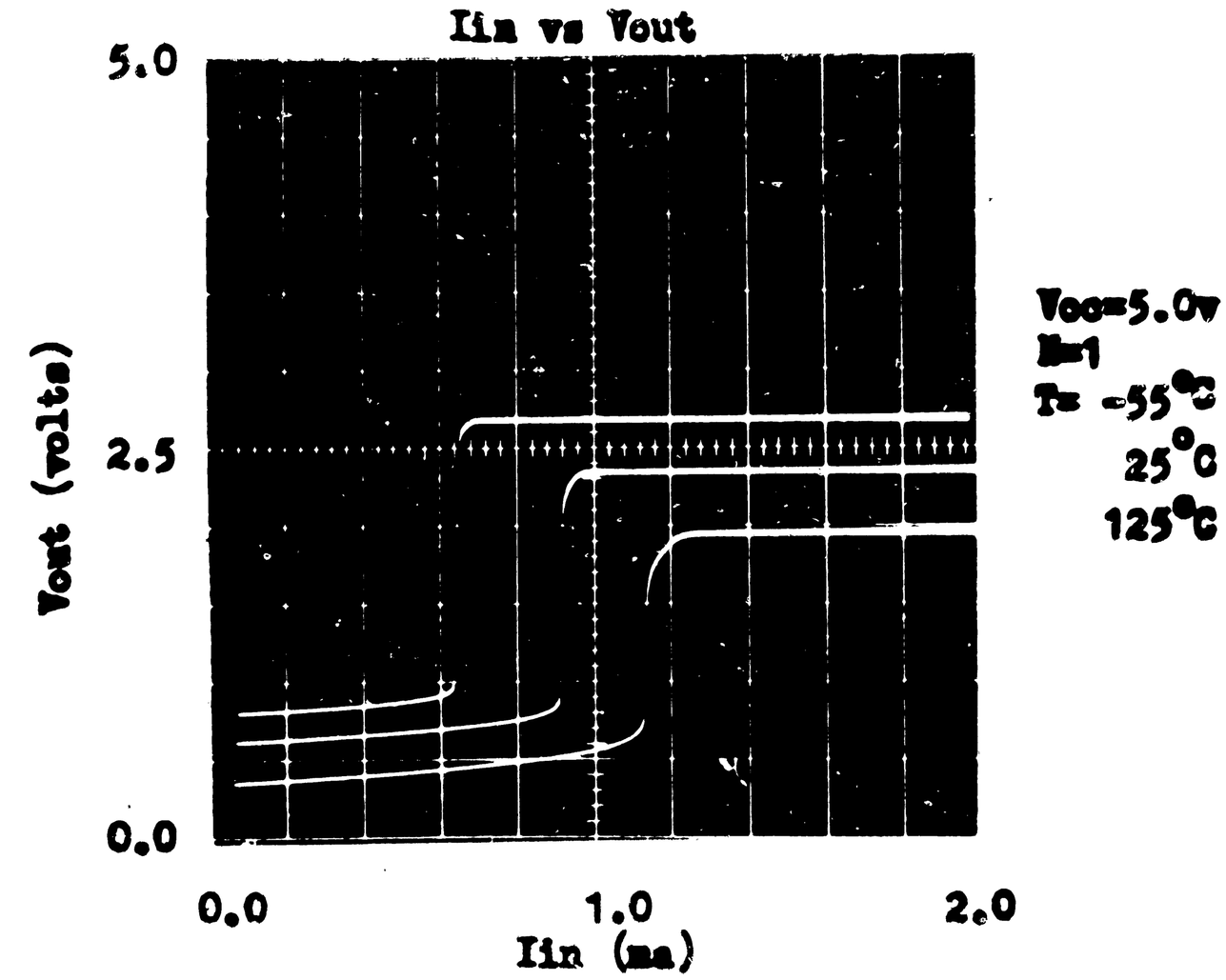
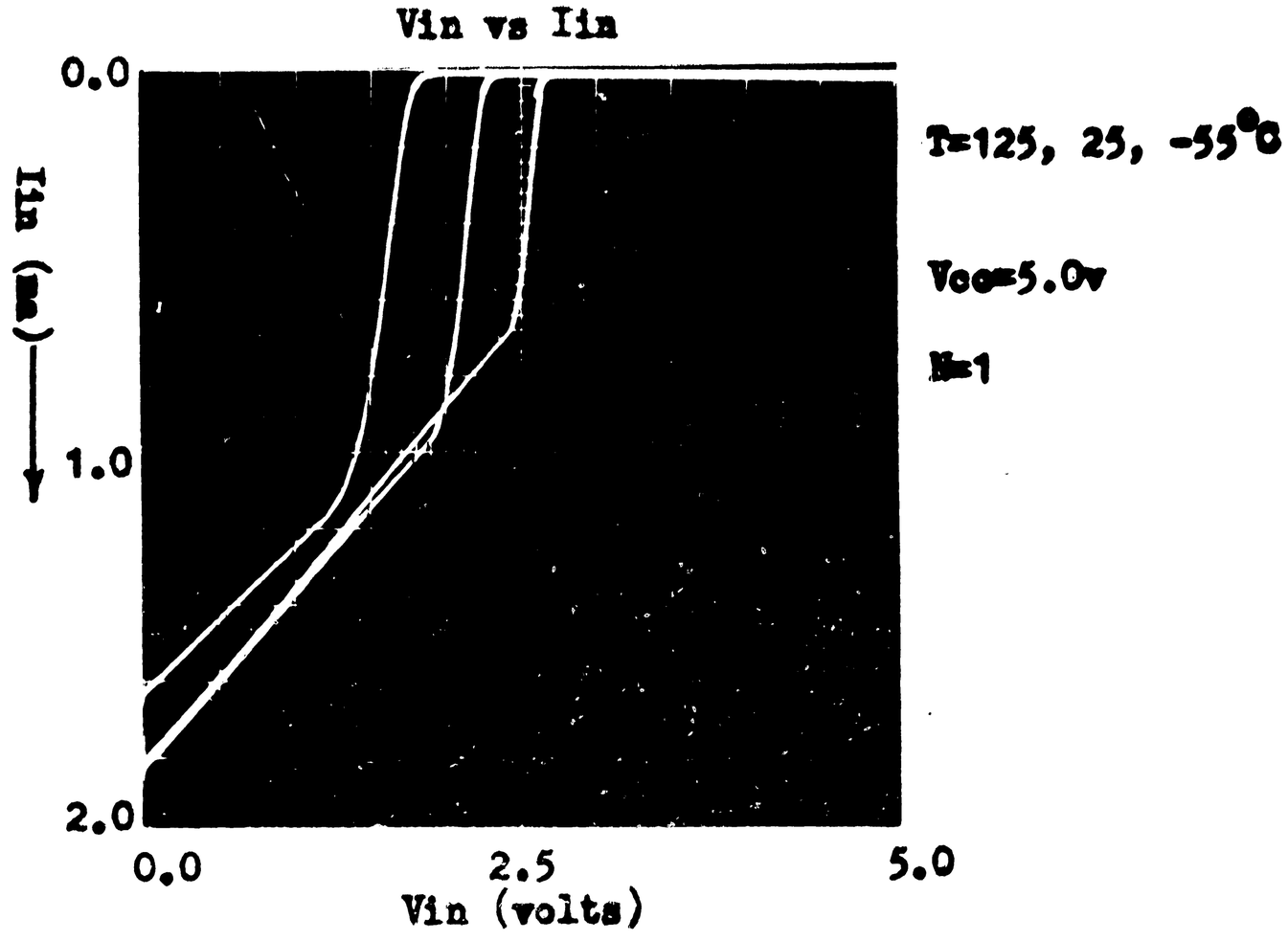

Iin vs Vout
5.0
2.5
0.0
Vout (volts)
0.0
1.0
2.0
Iin (ma)
Vcc=5.0v
N=1
Tc -55°C
25°C
125°C

Figure 3.1.2

AO2 DUAL NAND/NOR GATE



Note: The Vin vs Iin curve also represents a Vout vs Iout characteristic for Vin=0.0 and N>0.

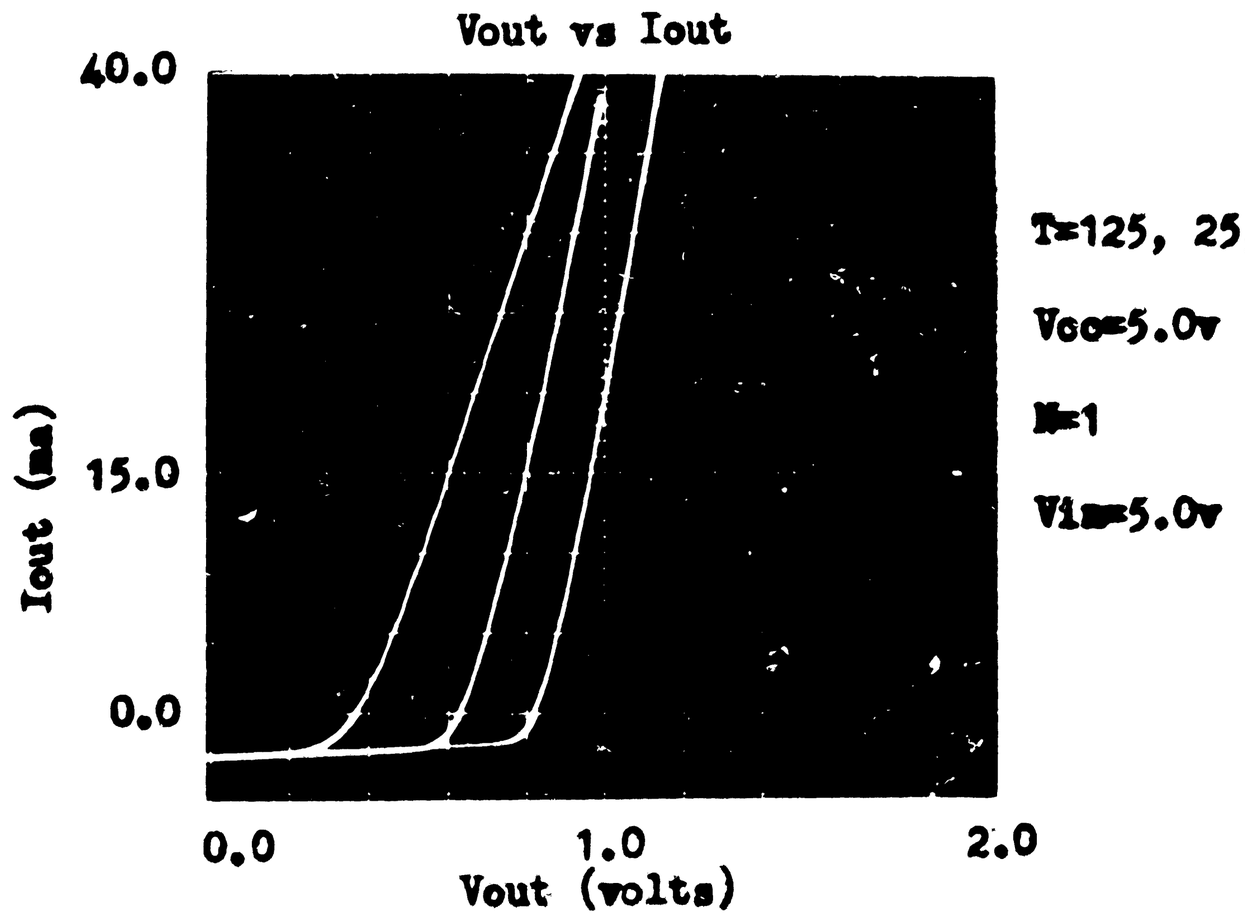
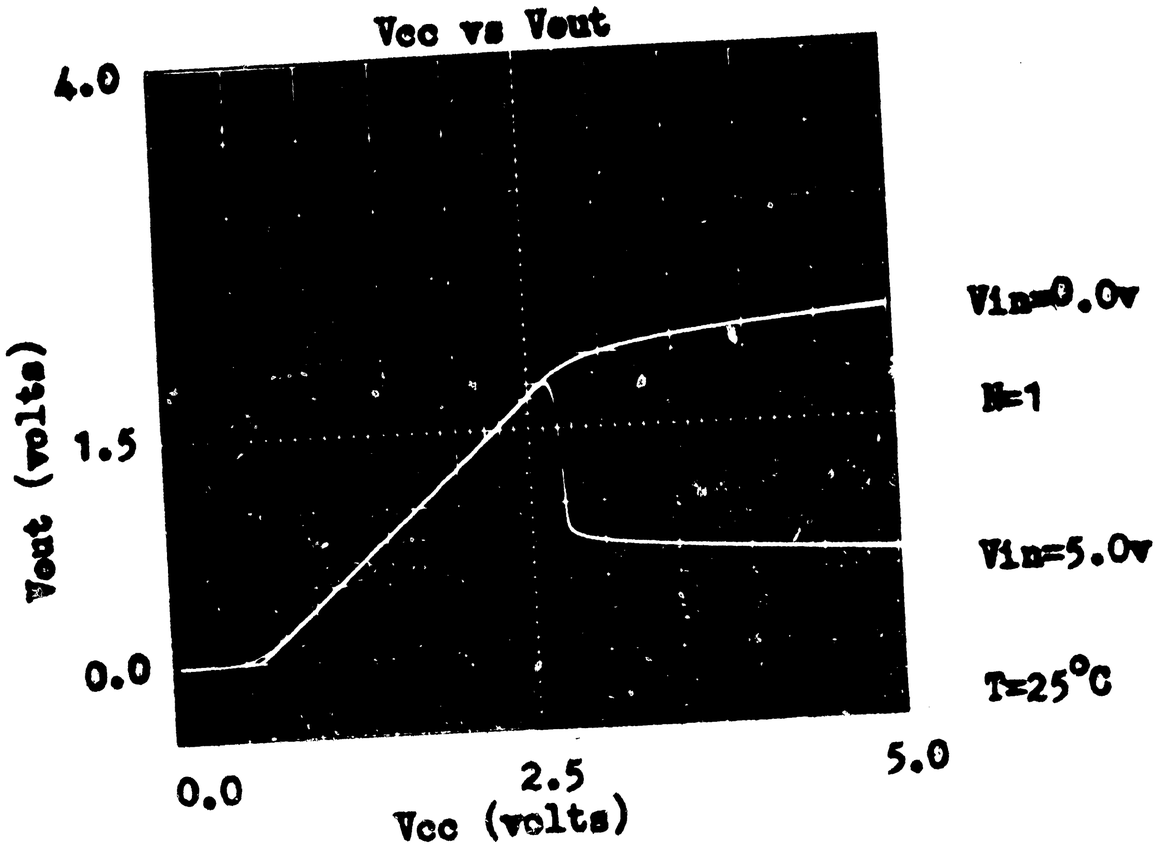
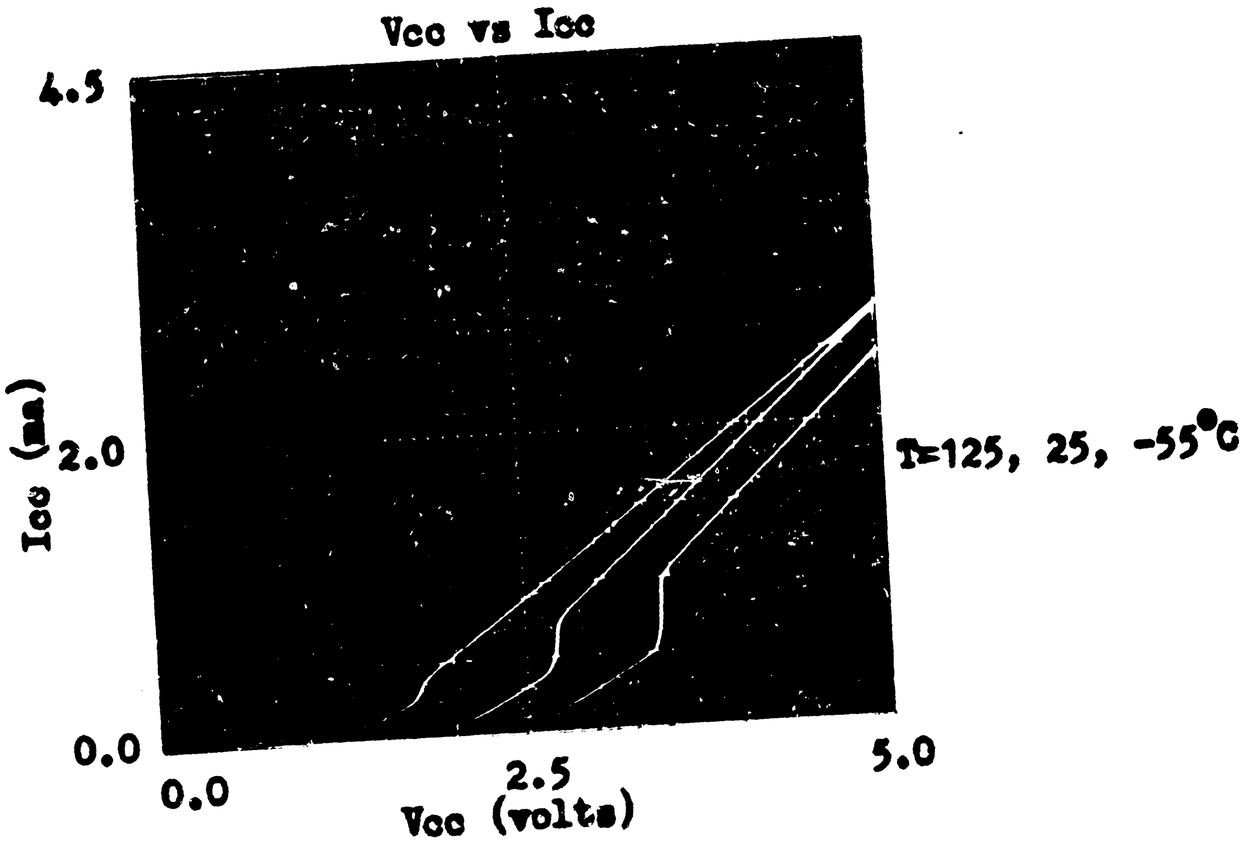


Figure 3.1.3

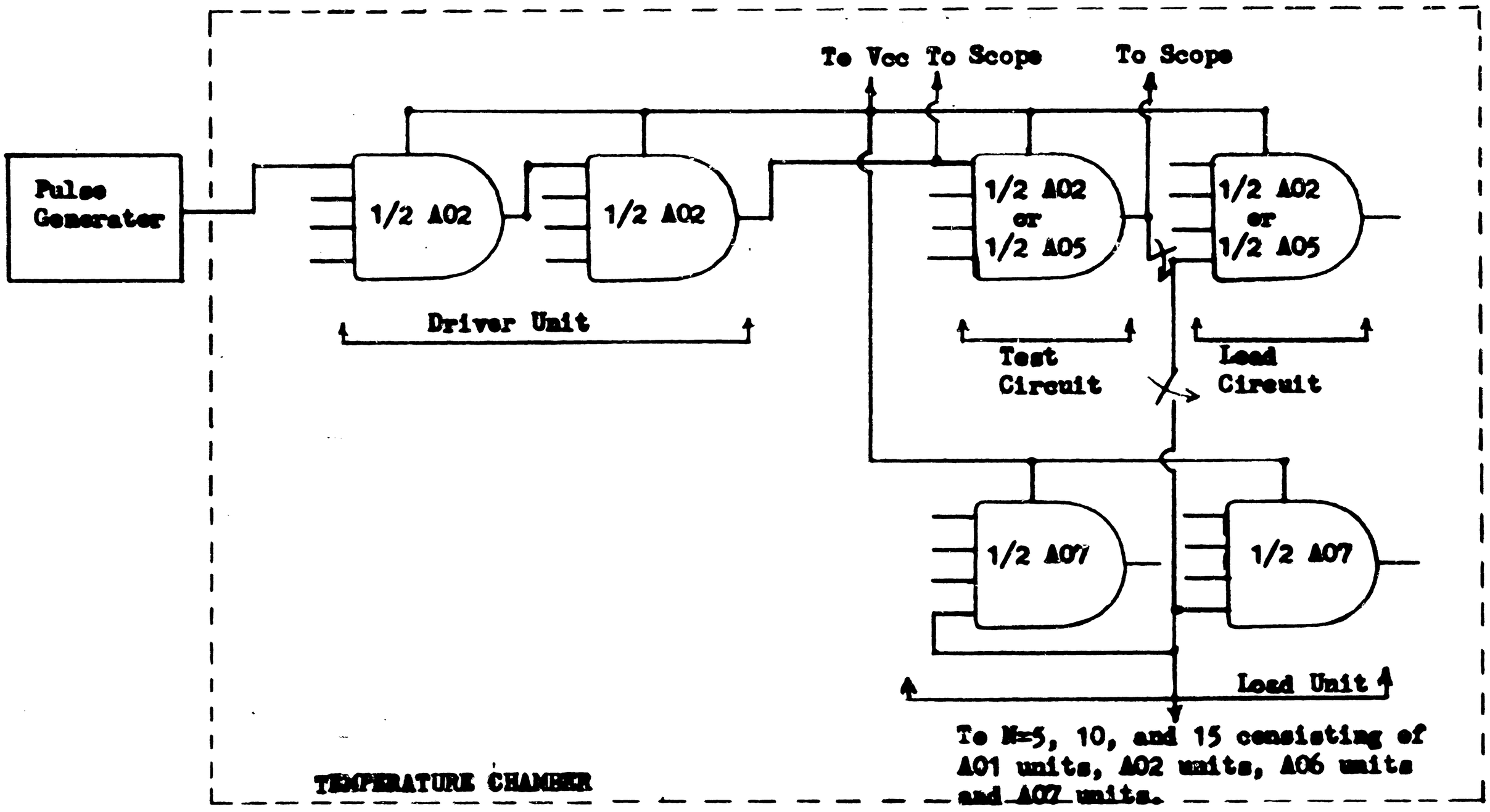
AO2 DUAL NAND/NOR GATE





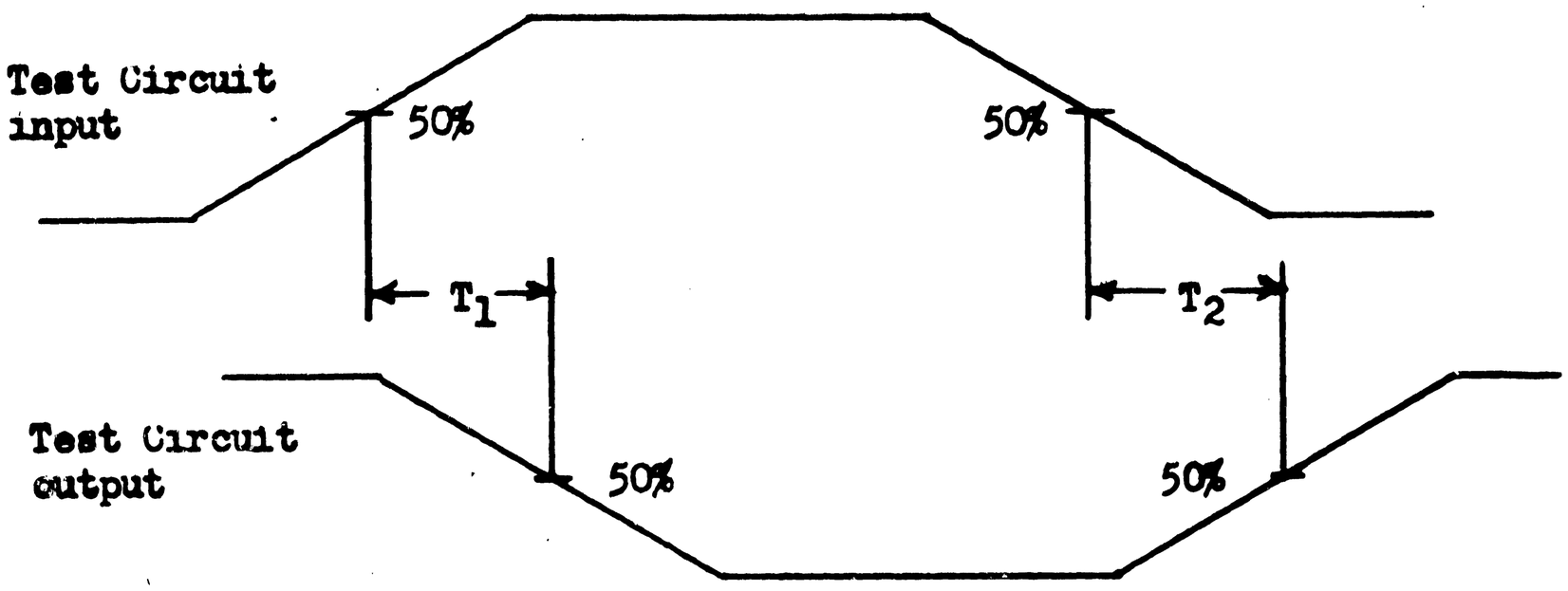
The power dissipation curve, Vcc vs Icc, shown above was obtained by loading one circuit of the dual NAND unit with the other. The inputs to the first circuit were left open simulating a high level input. This produced a low output which was coupled to the input of second circuit. In this manner a 50% duty cycle power dissipation curve (one circuit "on" and one circuit "off") is obtained for the complete unit. Power dissipation for one circuit is obtained by dividing the product of Vcc and Icc shown on the above curve by two.

Figure 3.1.4



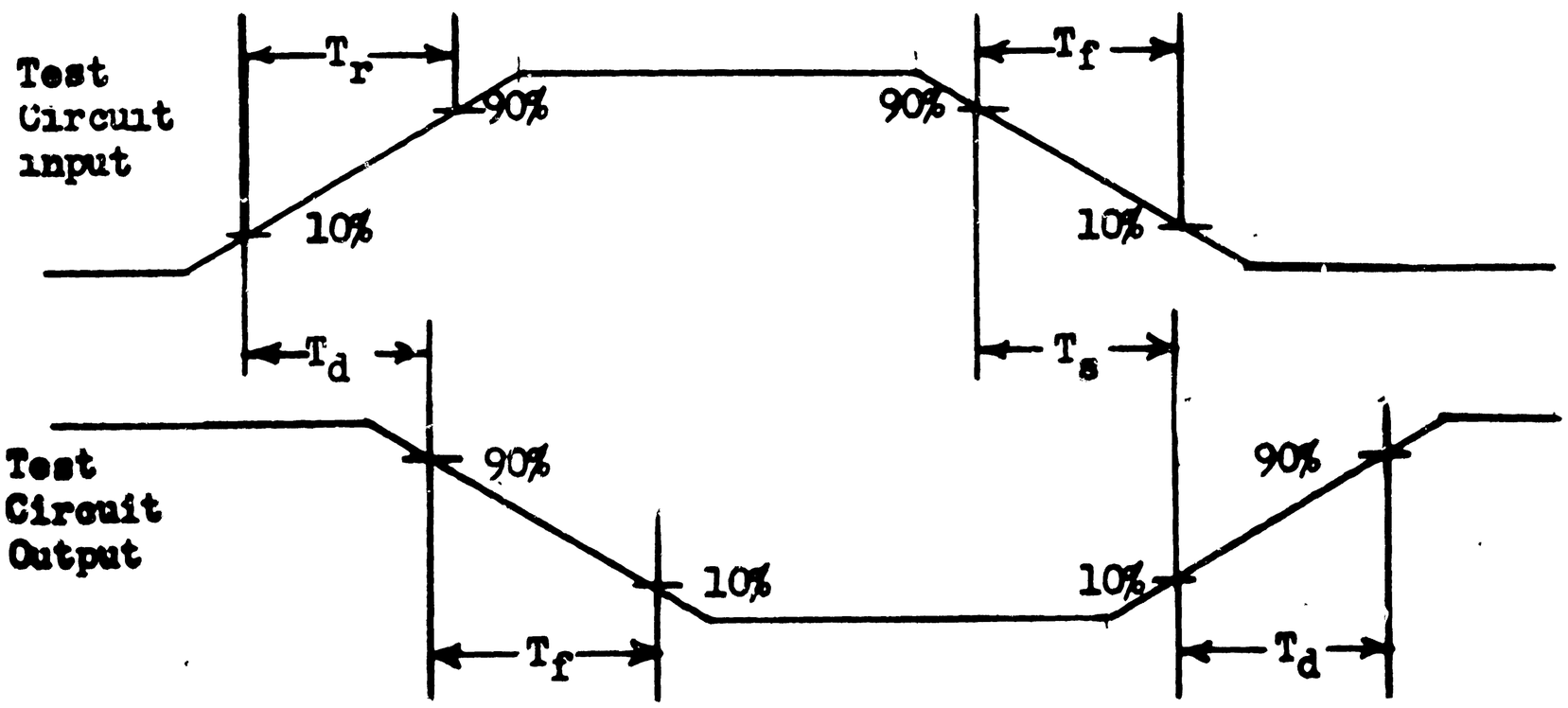
Test set-up for the A02 dual NAND/NOR gate and the A05 dual Line Driver.

Figure 3.1.5



$$T_{pd} = \frac{T_1 + T_2}{2}$$

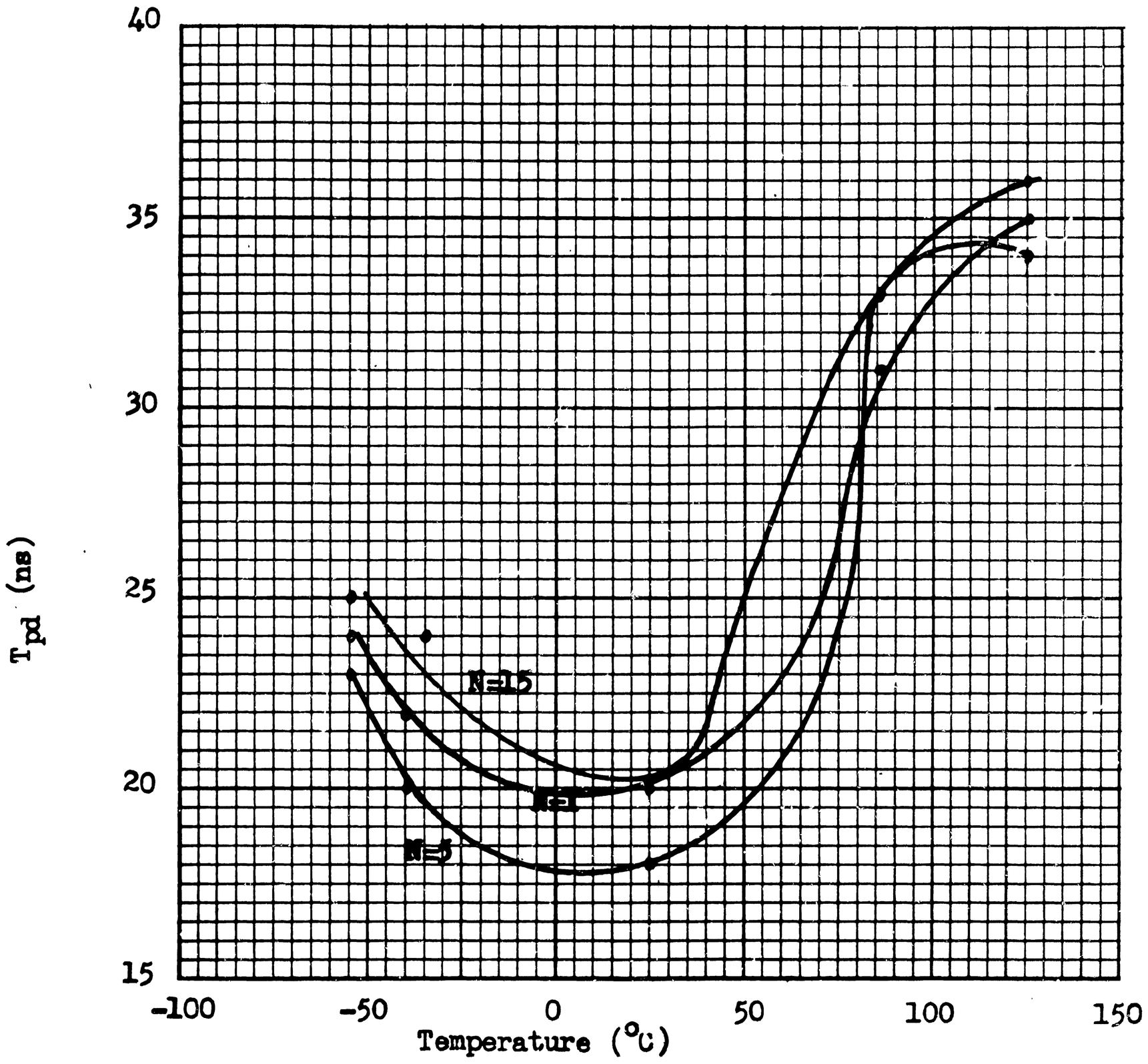
Propagation Delay



Rise time (T_r), Fall time (T_f), Delay time (T_d), Storage time (T_s).

A02 and A05 NAND/NOR Gate waveform definitions.

Figure 3.1.6

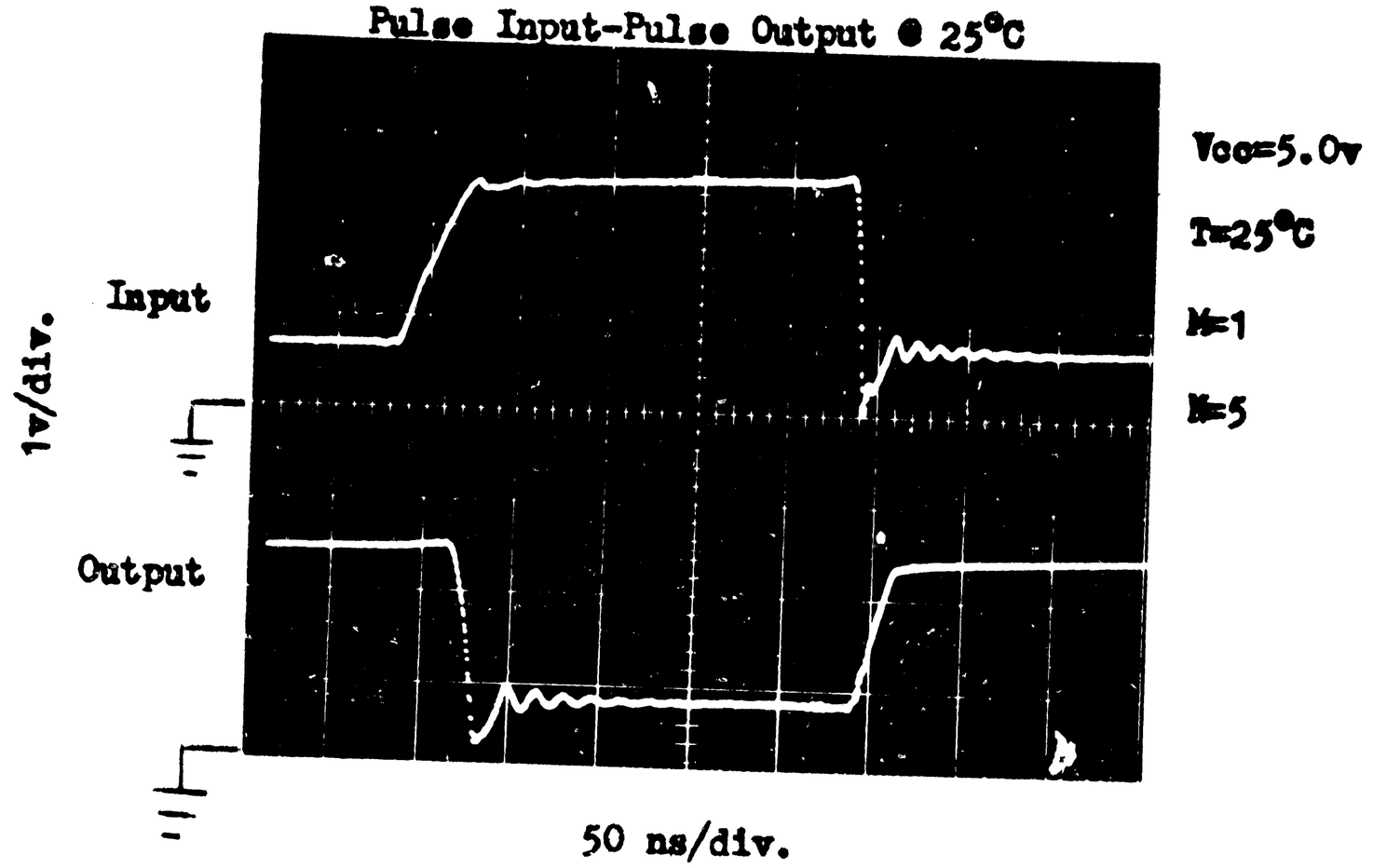


AO2 NAND/NOR Power Gate. Propagation delay vs temperature with the number of loads (N) as a parameter. Vcc=5.0v

Figure 3.1.7

A02 DUAL NAND/NOR GATE

Pulse Input-Pulse Output @ 25°C



Pulse Input-Pulse Output @ -55°C

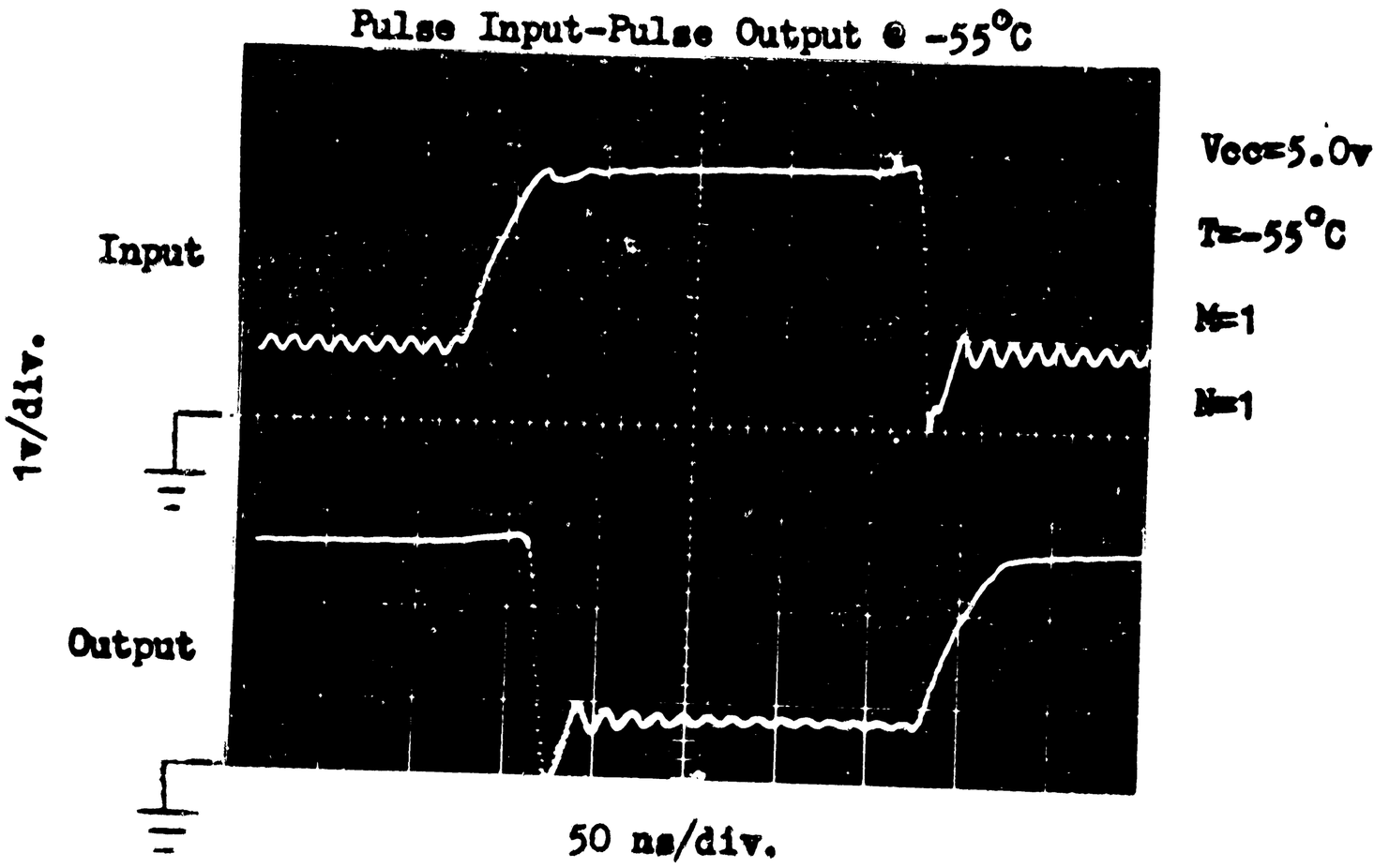
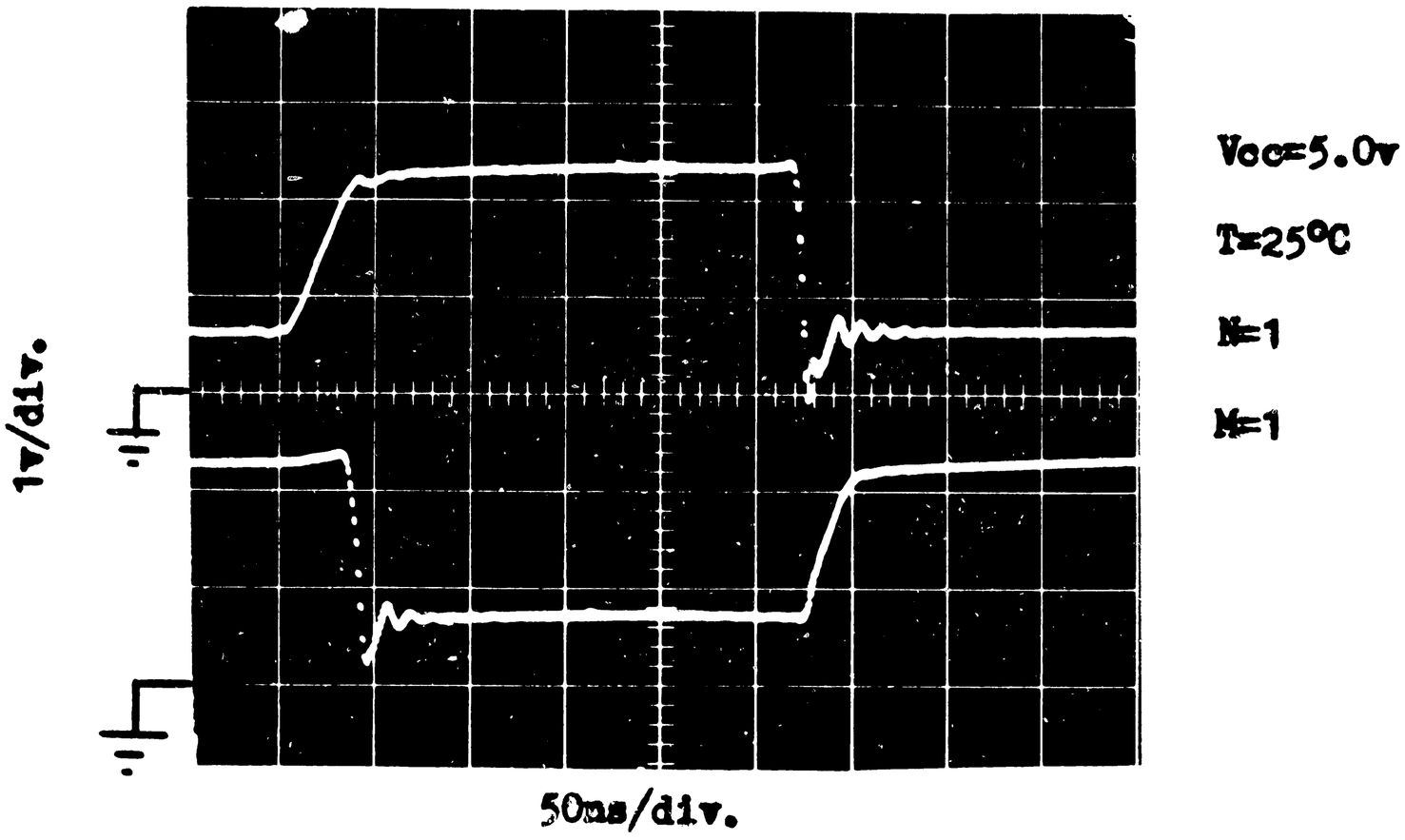


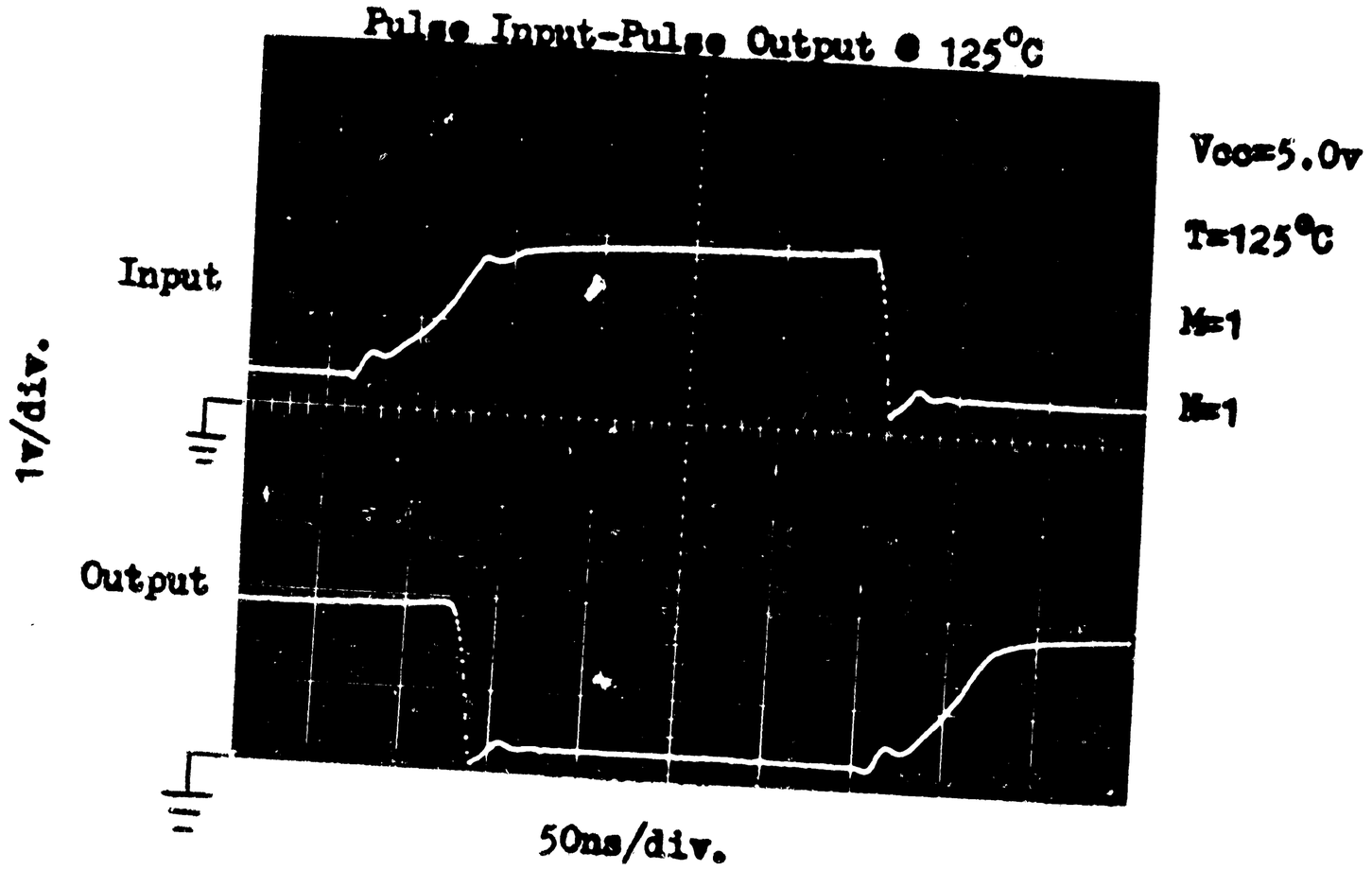
Figure 3.1.8

A02 Dual NAND/NOR Gate driving a A07 Dual NAND/NOR Gate



This oscillograph demonstrates the difference in output pulses between an "old" circuit and a "new" circuit. The top trace is the output of an A02 before changes were made in the production process. This trace is also the input to an A07 circuit which was manufactured under the new process. The output of the A07 is shown in the bottom trace. Note the reduction in the duration of the ringing as well as the peak amplitude.

Figure 3.1.9


Pulse Input-Pulse Output @ 125°C
Input
Output
1v/div.
Vcc=5.0v
T=125°C
M=1
M=1
50ns/div.

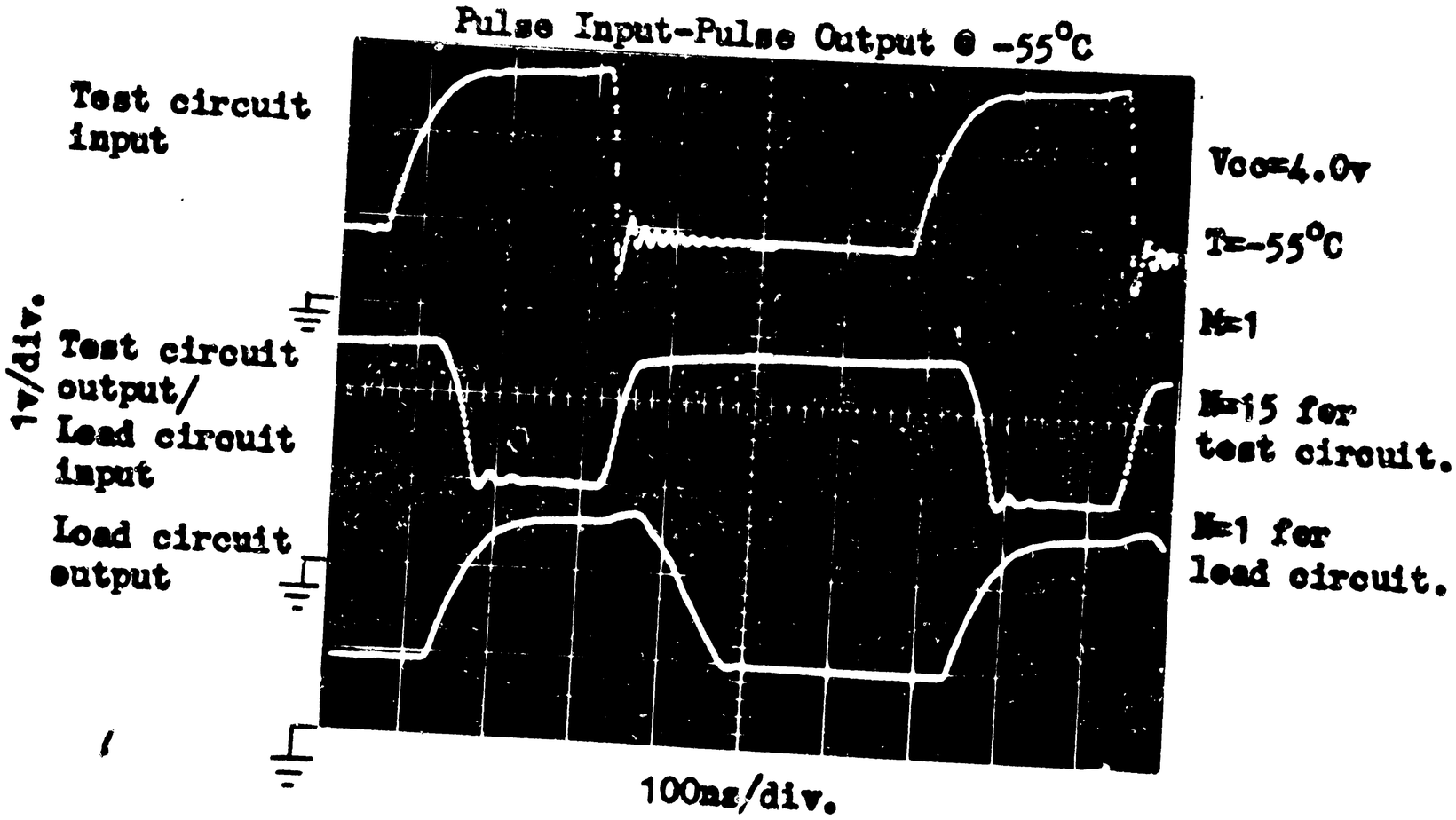

Pulse Input-Pulse Output @ -55°C
Test circuit input
Test circuit output/ Load circuit input
Load circuit output
1v/div.
Vcc=4.0v
T=-55°C
M=1
M=15 for test circuit.
M=1 for load circuit.
100ns/div.

Figure 3.1.10

Circuit Designation A02 , Fan-In 1 , Vcc 4.0 Volts, Input Pulse Rep. Rate 1 MC

Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	1.8	1.8	1.6	1.5	1.8	1.7	1.7	1.5	1.7	1.7	1.6	1.4
Pulse Width (ns)	250	219	199	184	250	230	210	202	250	245	232	230
T_r (ns)	64	83	42	34	58	71	36	31	45	55	31	27
T_f (ns)	9	13	21	38	8	11	17	29	5	8	12	18
T_d (ns)		73	76	84		62	65	70		42	43	45
T_s (ns)		8	8	9		10	8	9		10	8	9
T_{pd} (ns)		44	39	48		38	34	41		27	24	27

Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	1.6	1.5	1.4	1.2	1.5	1.4	1.3	1.1
Pulse Width (ns)	250	251	244	245	250	285	280	275
T_r (ns)	41	54	45	49	87	79	84	82
T_f (ns)	5	8	12	17	7	8	12	18
T_d (ns)		35	53	46		58	60	60
T_s (ns)		10	10	10		15	12	15
T_{pd} (ns)		25	22	25		37	37	36

Circuit Designation A02 , Fan-In 1 , Vcc 5.0 Volts, Input Pulse Rep. Rate 1 MC

Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	2.0	1.9	1.8	1.7	1.9	1.9	1.8	1.7	1.8	1.8	1.7	1.5
Pulse Width (ns)	250	247	232	228	250	245	236	232	250	250	243	243
T_r (ns)	36	40	21	22	32	38	19	21	31	37	22	28
T_f (ns)	5	6	10	17	4	6	9	16	4	6	9	14
T_d (ns)		38	39	41		34	36	38		42	29	30
T_s (ns)		8	8	8		9	8	8		9	8	8
T_{pd} (ns)		24	23	26		22	20	24		20	18	20

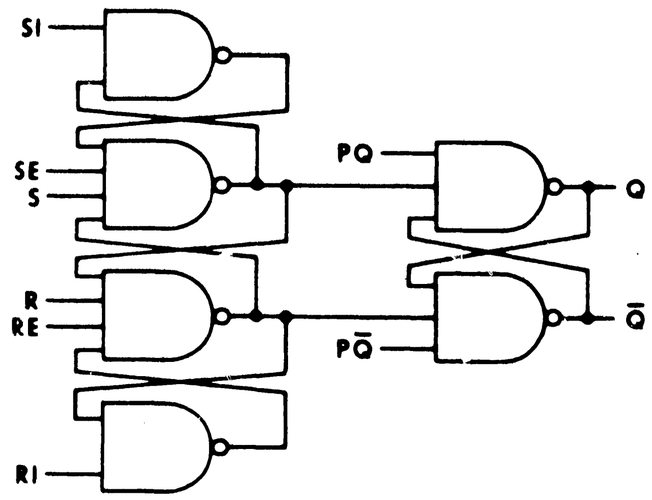
Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	1.7	1.7	1.5	1.3	1.6	1.5	1.4	1.1
Pulse Width (ns)	250	276	276	277	250	284	280	281
T_r (ns)	52	63	66	75	87	73	86	91
T_f (ns)	4	5	9	15	7	8	12	19
T_d (ns)		49	50	50		59	60	61
T_s (ns)		10	9	9		14	12	18
T_{pd} (ns)		31	33	33		35	34	36

Circuit Designation A02 , Fan-In 1 , Vcc 6.0 Volts, Input Pulse Rep. Rate 1MC												
Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	2.2	2.0	1.9	1.8	2.0	1.9	1.9	1.7	2.0	1.9	1.8	1.5
Pulse Width (ns)	250	247	238	236	250	250	242	240	250	269	264	258
T_r (ns)	25	30	16	18	24	27	16	18	28	47	46	50
T_f (ns)	4	5	8	14	4	5	8	13	3	5	8	13
T_d (ns)		27	29	30		26	27	27		28	29	28
T_s (ns)		9	6	8		9	8	7		8	8	7
T_{pd} (ns)		19	17	20		18	17	19		25	25	23

Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	15		1	5	15
Pulse Amplitude (V_{pp})	1.8	1.8	1.6	1.3	1.7	1.6	1.5	1.2
Pulse Width (ns)	250	278	275	280	250	292	286	279
T_r (ns)	49	56	69	81	90	77	92	90
T_f (ns)	4	5	9	16	7	8	12	21
T_d (ns)		45	52	52		63	65	65
T_s (ns)		10	9	14		14	13	23
T_{pd} (ns)		30	31	33		37	35	33

AC3 Counter,Shift-Register Circuit
Characteristic Data and Graphs

BLOCK DIAGRAM



TRUTH TABLE

SE	RE	SI	RI	Q^{n+1}
1	1	1	1	Q^n
1	1	1	0	0
1	1	0	1	1
1	1	0	0	*
1	0	1	1	Q^n
1	0	1	0	Q^n
1	0	0	1	1
1	0	0	0	1
0	1	1	1	Q^n
0	1	1	0	0
0	1	0	1	Q^n
0	1	0	0	0
0	0	1	1	Q^n
0	0	1	0	Q^n
0	0	0	1	Q^n
0	0	0	0	Q^n

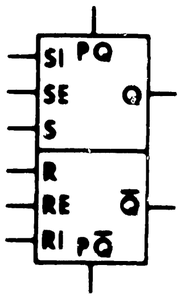
* INDETERMINATE

Each block in the diagram represents a single NAND gate.
Truth table assumes clock input to R and S.

A03 COUNTER, SHIFT-REGISTER CIRCUIT

LOGIC DIAGRAM

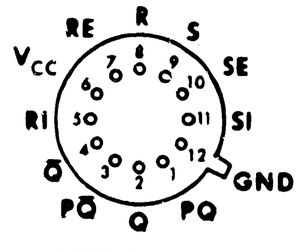
Figure 3.1.11



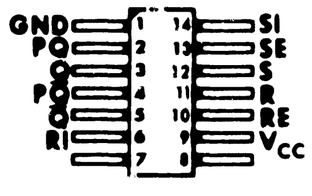
TERMINAL IDENTIFICATION

SI – SET INHIBIT
SE – SET ENABLE
S – SET
R – RESET
RE – RESET ENABLE
RI – RESET INHIBIT
PQ – PRESET Q
PQ̄ – PRESET Q̄
Q, Q̄ – COMPLEMENTARY OUTPUTS

PIN DIAGRAMS



BOTTOM VIEW



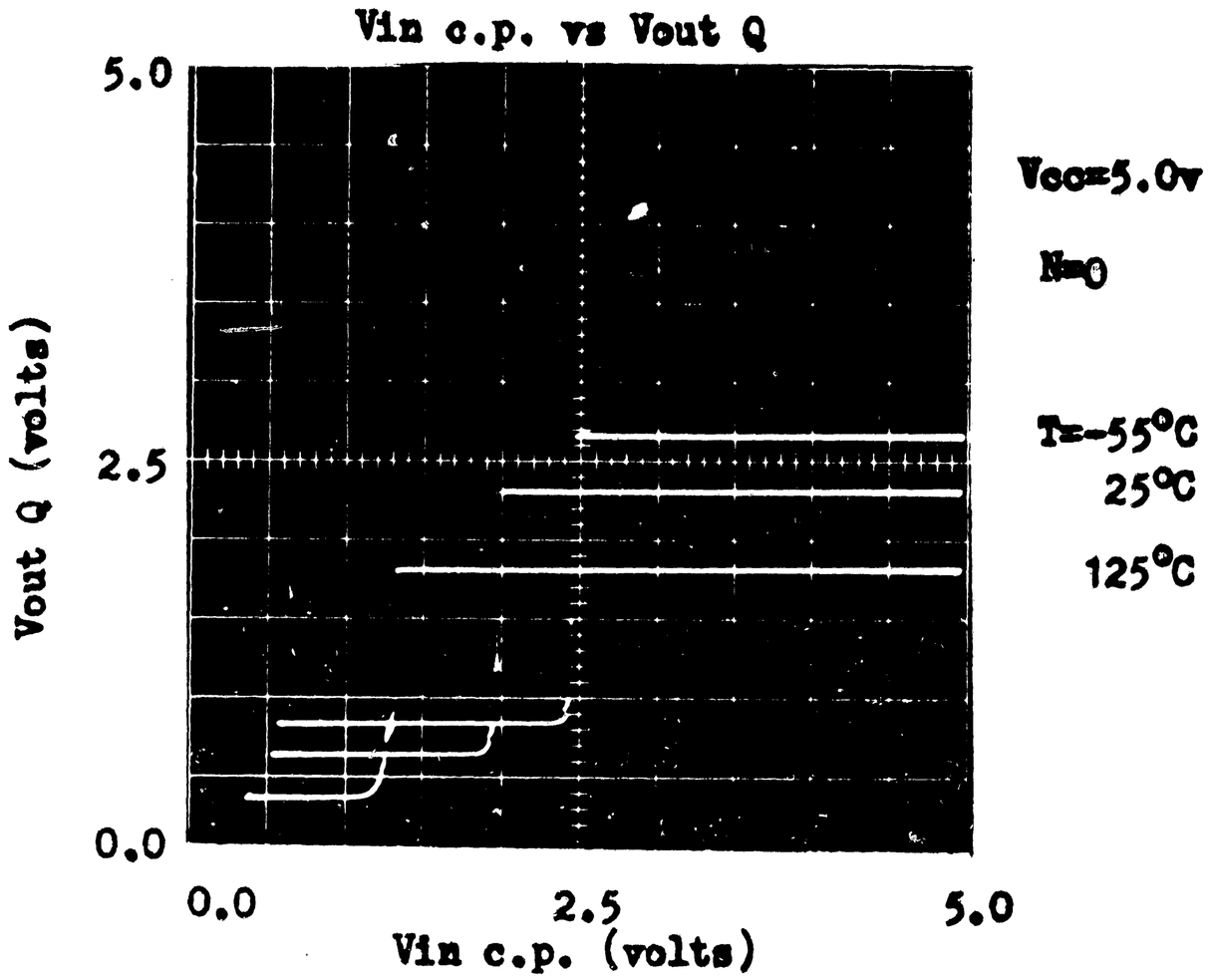
TOP VIEW

MODIFIED TO-5 FLATPAC

ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC} . . . . . 6 v
Input Voltage BV_i . . . . . 6 v
Output Voltage BV_o . . . . . 6 v
Operating Temperature Range T_A . . . . . −55 to +125°C
Storage Temperature Range T_S . . . . . −65 to +150°C
Output Current . . . . . 50 ma

Voltage at any pin must be positive with respect to the common terminal.


Vin c.p. vs Vout Q
5.0
2.5
0.0
Vout Q (volts)
0.0
2.5
5.0
Vin c.p. (volts)
Vcc=5.0v
N=0
T=-55°C
25°C
125°C

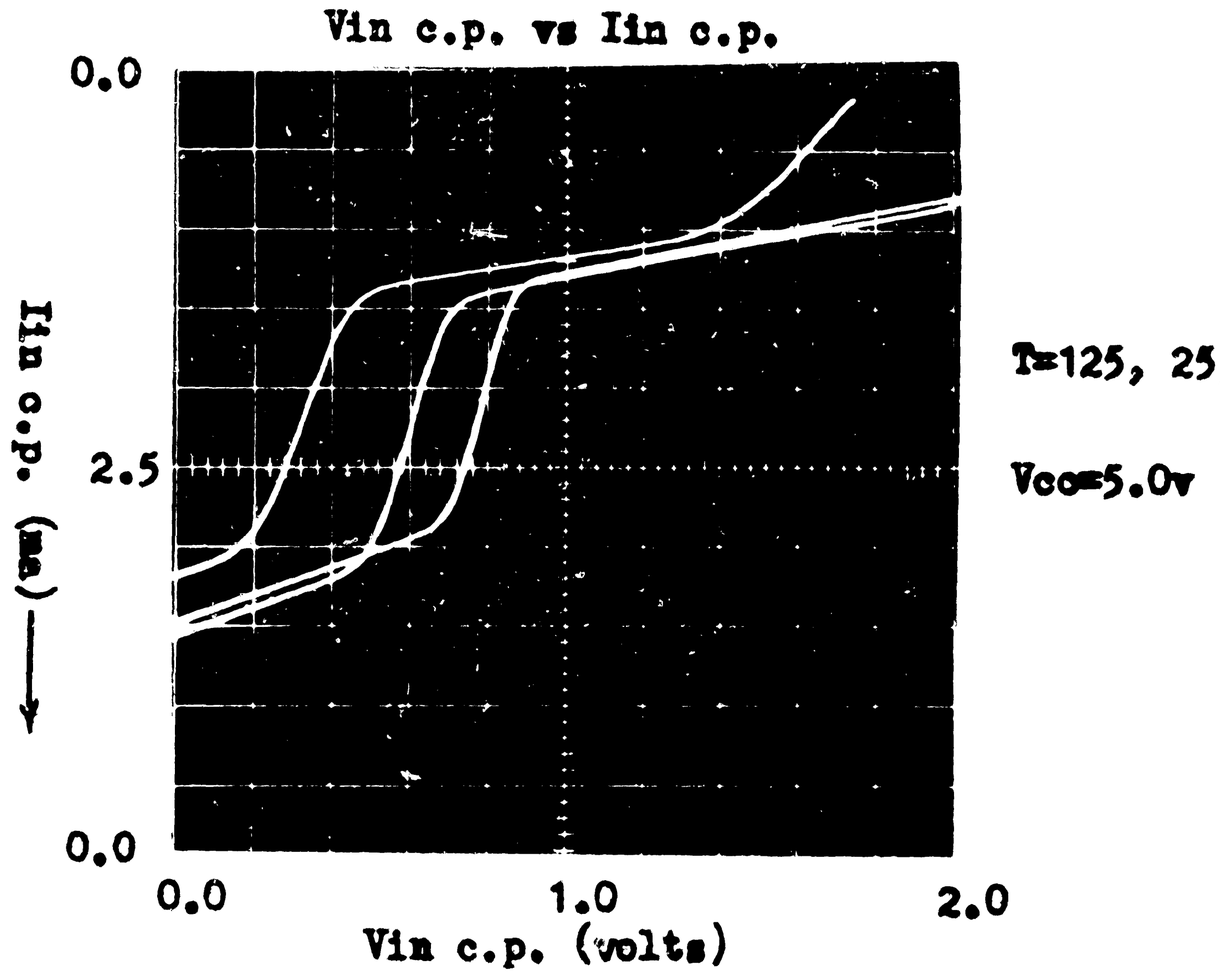
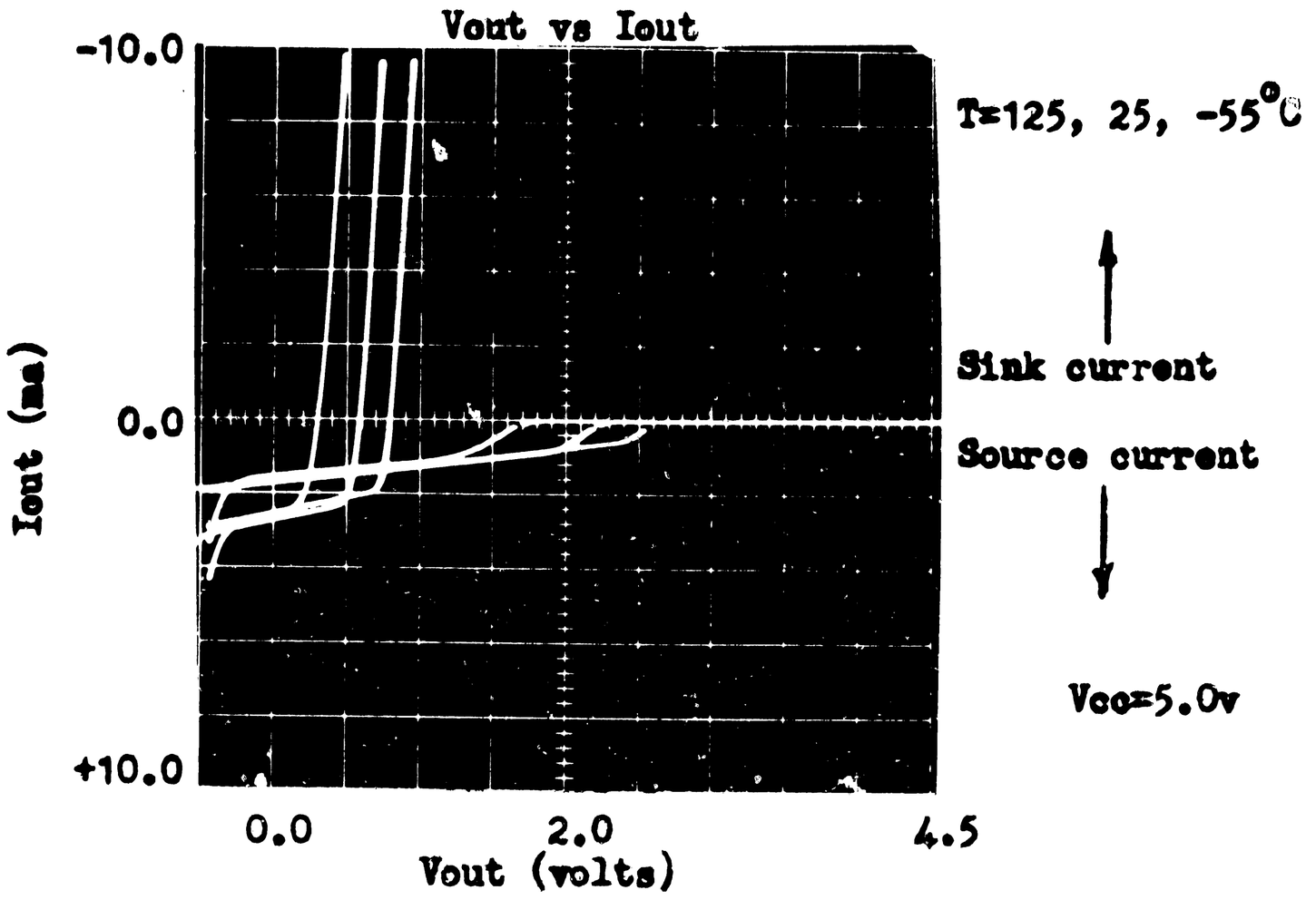

Vin c.p. vs Iin c.p.
0.0
2.5
0.0
Iin c.p. (mA)
0.0
1.0
2.0
Vin c.p. (volts)
T=125, 25, -55°C
Vcc=5.0v

Figure 3.1.12

A03 COUNTER SHIFT-REGISTER CIRCUIT



Both Q and $\bar{Q}$ outputs are shown. Q, in this case, is in the "on" state.

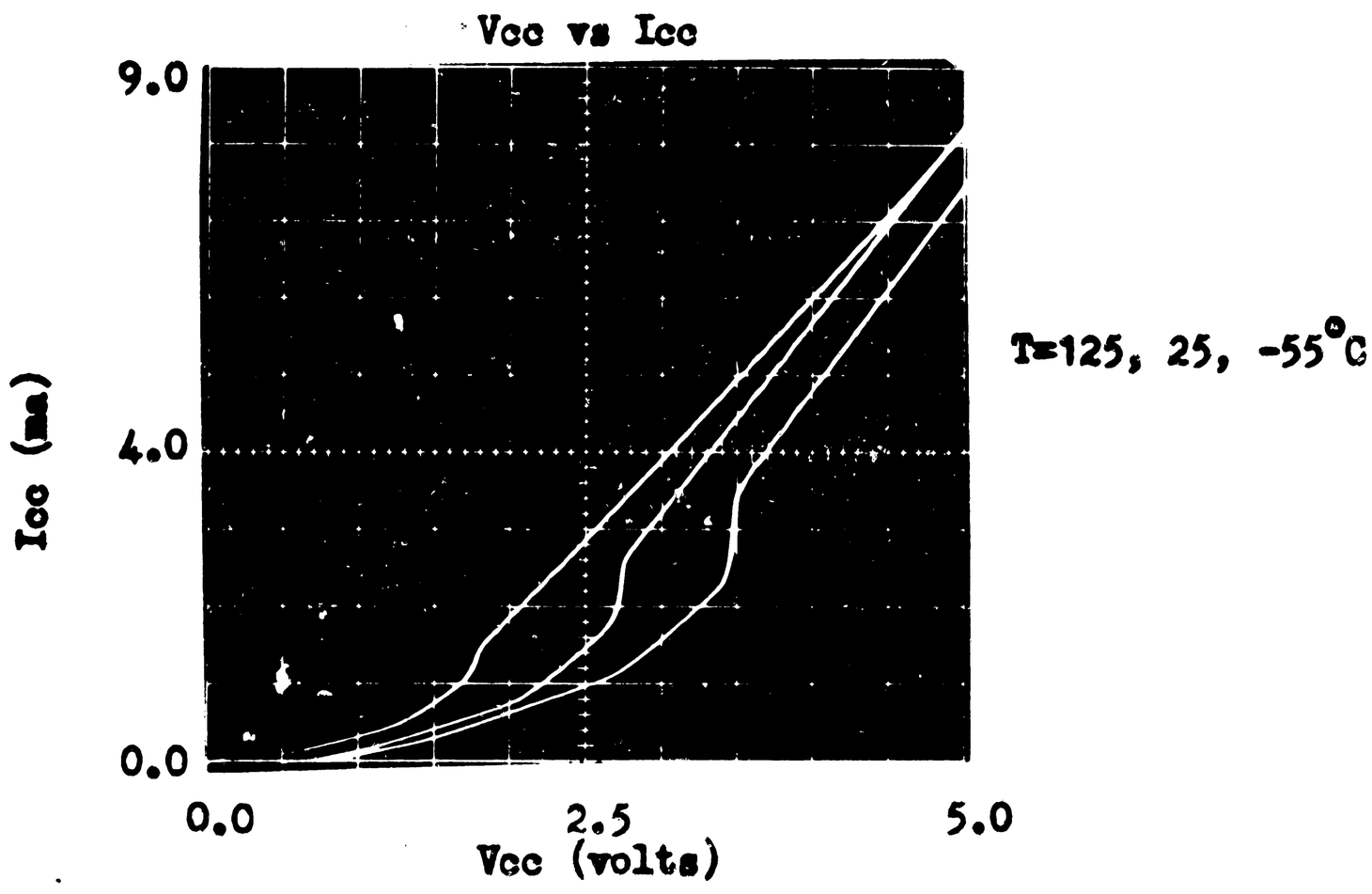
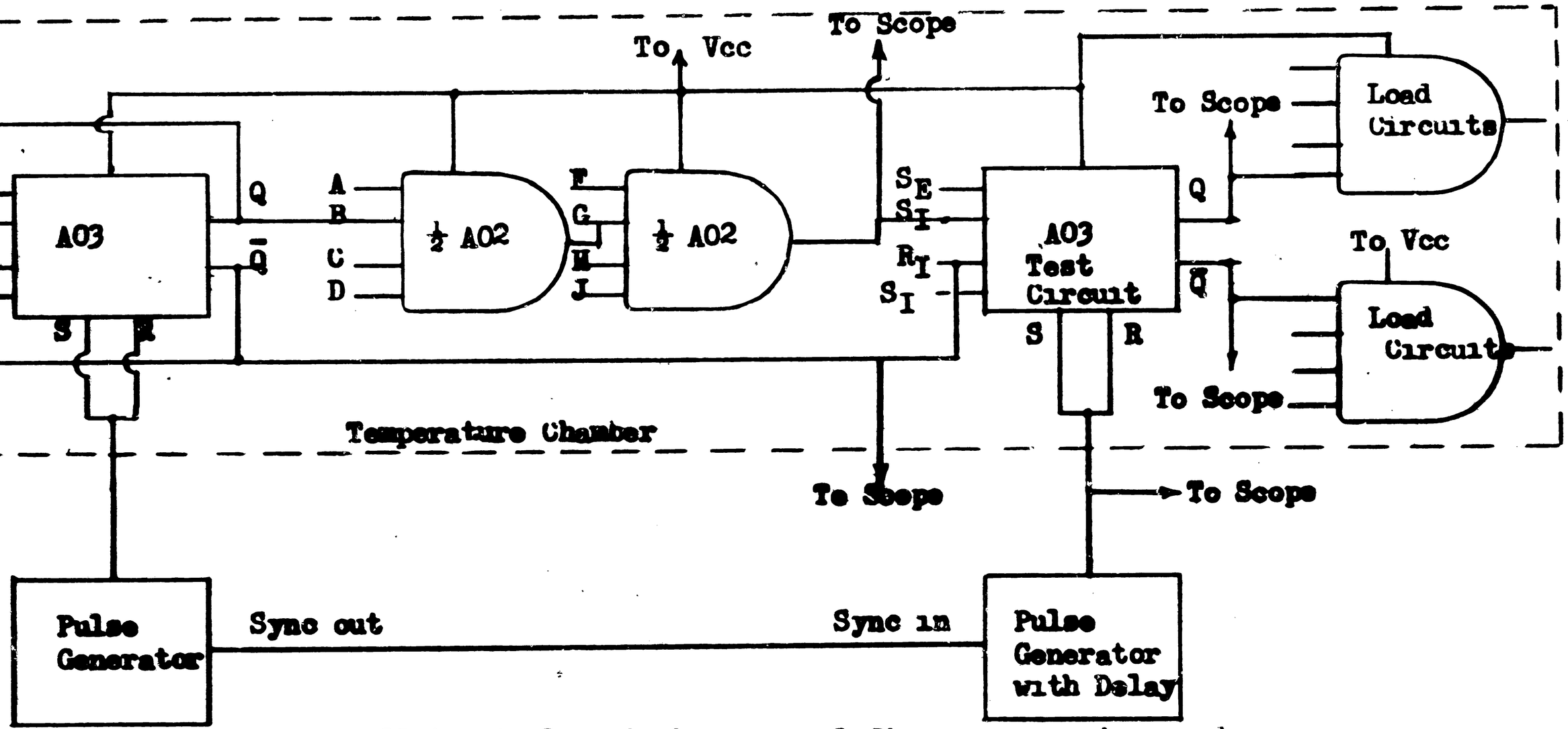


Figure 3.1.13

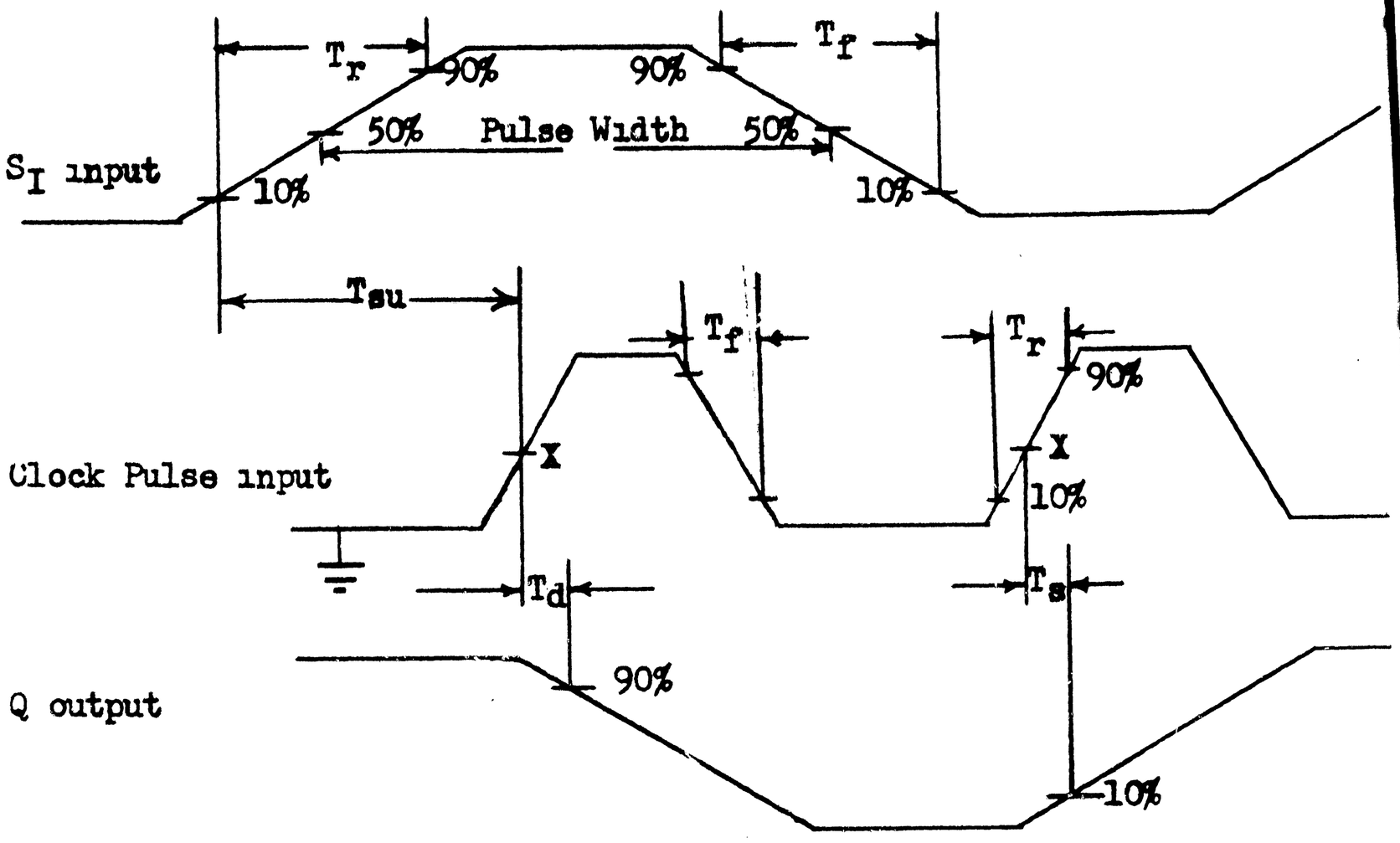


All terminals not shown were left open, except ground.

Test set-up for the A03 counter, shift-register circuit.

Figure 3.1.14

3.1.23



Rise time (T_r), Fall time (T_f), Delay time (T_d),
Storage time (T_s), Set-up time (T_{su})

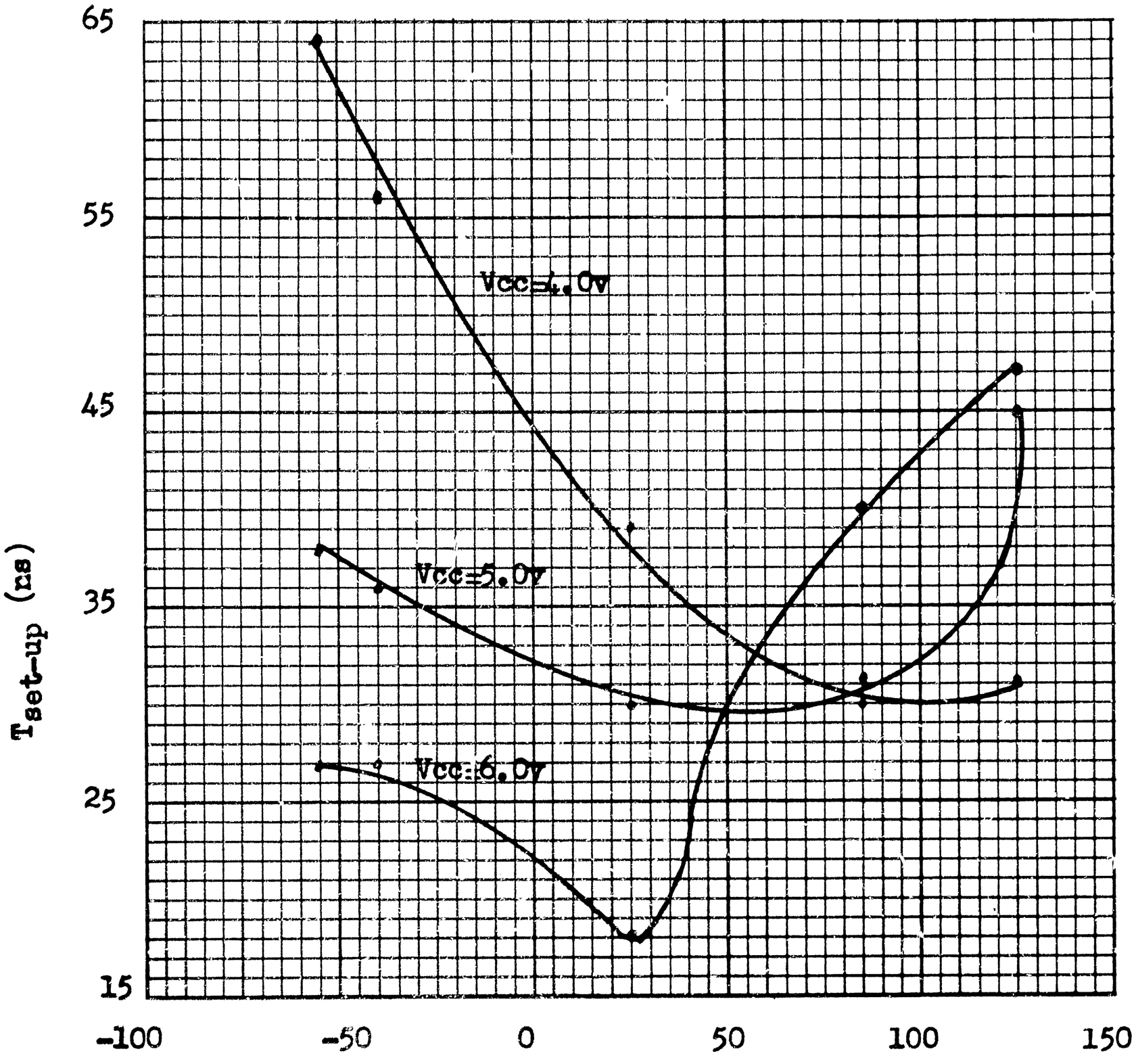
T°C	-55	-40	25	85	125
X volts	2.5	2.5	2.0	1.3	1.3

A03 Counter-Shift Register Waveform Definition. See notes below.

Figure 3.1.15

NOTE 1: The X voltage points were used instead of percentage points on the clock pulse. This was done because the clock pulse was swinging from ground and not from an offset voltage as would be the case if it had been supplied through a Siliconix driver circuit. The points were determined from the static clock pulse input vs. Q output voltage curves of Figure 12. It should be noted however, that the rise time of the clock pulse was less than 10 ns and therefore the points from which the measurements were made were not critical.

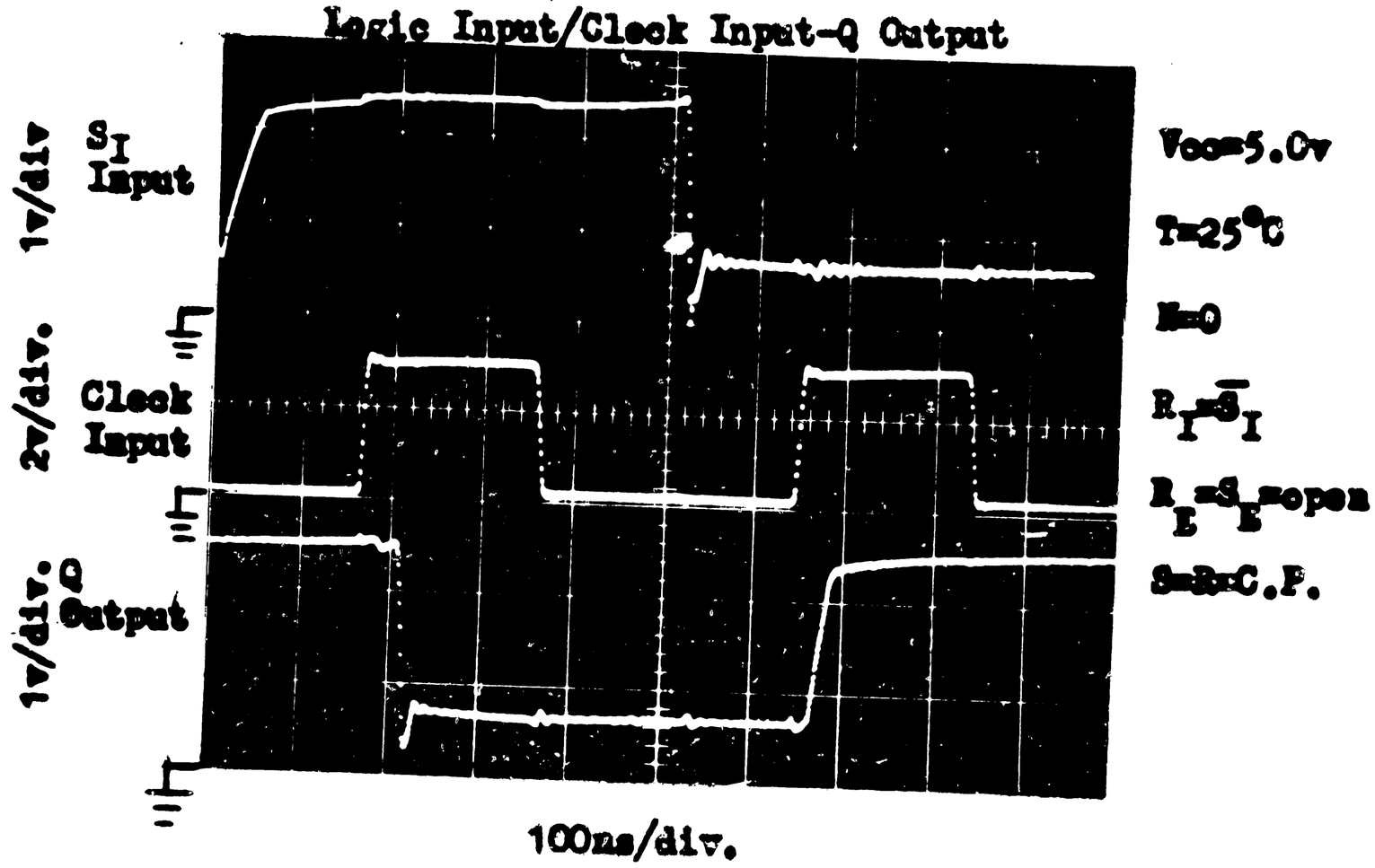
NOTE 2: The criteria used to measure the setup time was as follows. Refer to Figure 13 for the test setup and to Figures 16 and 17 for actual pulse data oscillographs. The clock pulse was moved to the left until a steady state (no toggeling) output was observed. At this point the logic and clock pulse input was similar to that shown in Figure 18. The clock pulse was then slowly moved to the right until toggeling was observed and the discontinuity in the logic input vanished. The setup time was measured at this point.



AOj Counter, Shift-Register. Set-up time vs temperature with Vcc as a parameter. M=1.

Figure 3.1.16

A03 COUNTER, SHIFT-REGISTER CIRCUIT



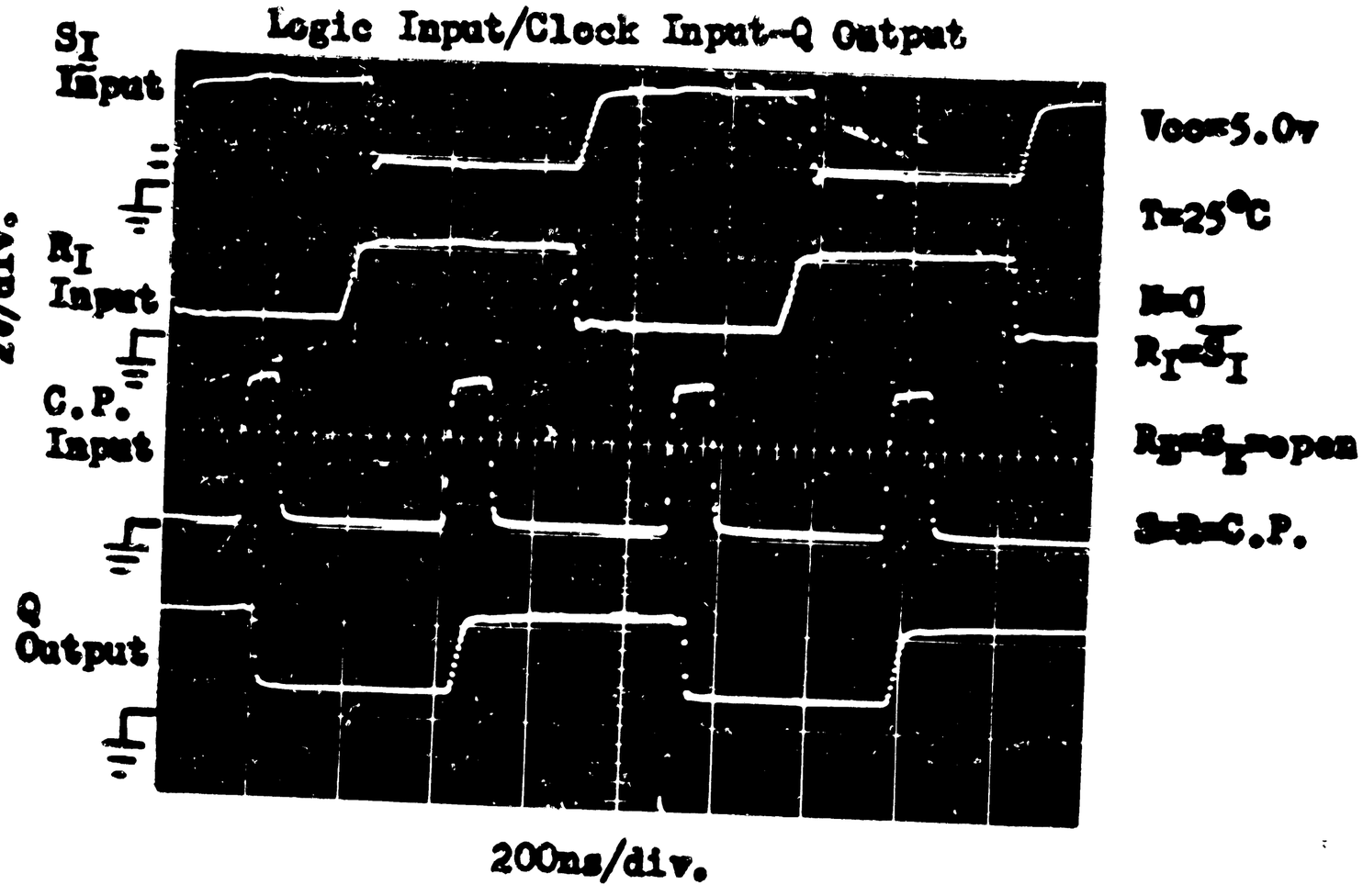
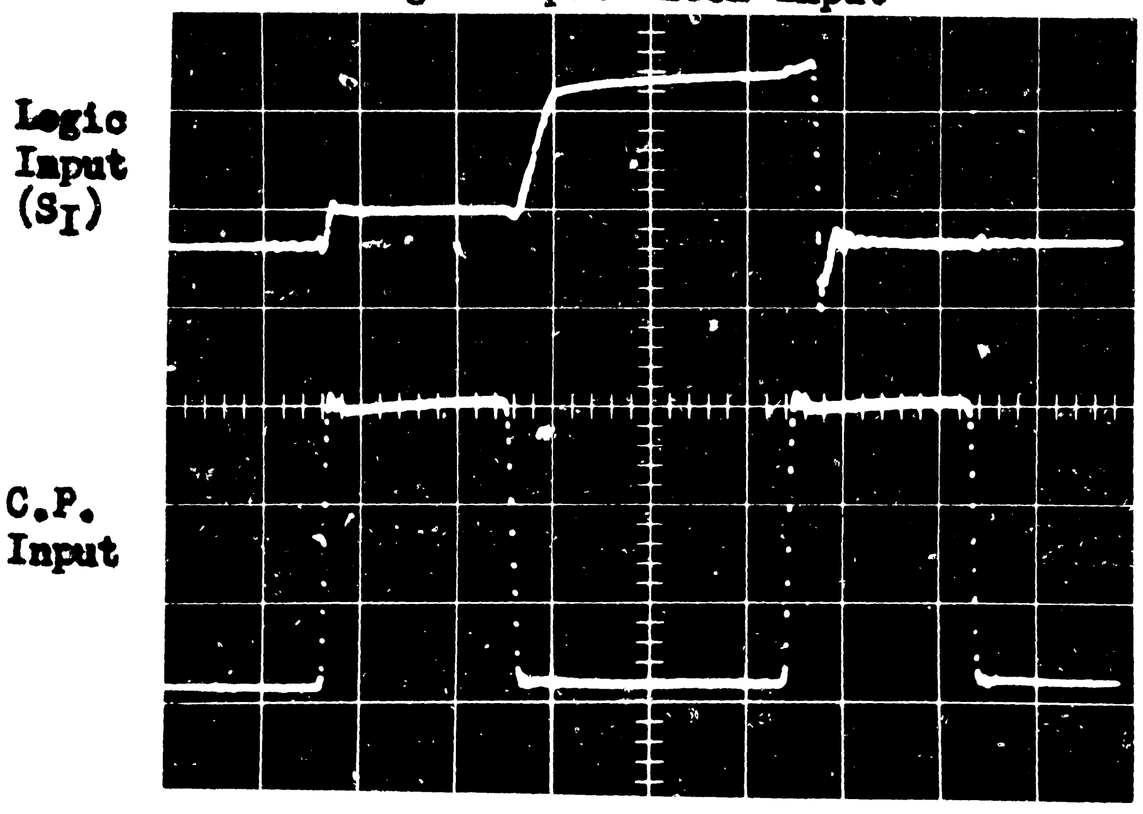


Figure 3.1.17

A03 COUNTER,SHIFT REGISTER CIRCUIT

Logic Input-Clock Input



50ns/div.

Oscillograph shows the effect of applying the clock pulse too soon after the logic input.
See paragraph III.A.4.

Figure 3.1.18

Circuit Designation A03					Vcc 4.0 Volts, Clock Pulse Rep. Rate 2 MC							
Temperature	-55°C				-40°C				25°C			
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5
Pulse Amplitude (V_{pp})	1.8	3.0	1.7	1.7	1.8	3.0	1.7	1.7	1.6	3.0	1.6	1.6
Pulse Width (ns) 50-50%	546	200	454	455	539	200	458	459	526	200	478	478
T_r (ns) 10 to 90%	101	7	48	45	77	7	42	36	64	7	34	32
T_f (ns) 90 to 10%	10	8	22	55	8	8	16	41	6	7	8	16
Td (ns) X to 10%			104	101			89	88			64	63
T_s (ns) X to 90%			51	52			48	46			31	31
T Set Up 10% to X		64				56				39		

Temperature	85°C				125°C				Minimum Vcc=4.0 at -55°C =3.5 at 25°C =2.7 at 125°C N=5 Minimum clock pulse width =65ns at -55°C =34ns at 25°C =48ns at 125°C N=5 The minimum parameter measurements were taken at the point just above that necessary to produce toggeling on the output. X_{cp}=2.5v at -40 and -55°C =2.0v at 25°C =1.3v at 85 and 125°C
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	
Pulse Amplitude (V_{pp})	1.5	3.0	1.5	1.4	1.4	3.0	1.4	1.4	
Pulse Width (ns) 50-50%	515	200	468	476	520	200	498	505	
T_r (ns) 10 to 90%	65	7	32	28	18	6	46	46	
T_f (ns) 90 to 10%	5	7	7	12	7	7	7	15	
T_d (ns) X to 10%			55	54			55	53	
T_s (ns) X to 90%			26	26			24	23	
T Set Up 10% to X		30				31			

Circuit Designation A03 , Vcc 5.0 Volts, Clock Pulse Rep. Rate 2 MC												
Temperature	-55°C				-40°C				25°C			
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5
Pulse Amplitude (V_{pp})	1.9	3.0	1.9	1.8	1.9	3.0	1.9	1.8	1.7	3.0	1.7	1.7
Pulse Width (ns) 50-50%	512	200	474	469	512	200	477	474	506	200	480	478
T_r (ns) 10 to 90%	52	6	25	22	49	6	24	22	40	6	23	19
T_f (ns) 90 to 10%	5	8	8	17	5	8	7	15	4	8	6	11
Td (ns) X to 10%			58	58			54	54			45	45
T_s (ns) X to 90%			29	29			27	27			21	21
T Set Up 10% to X		38				36				30		

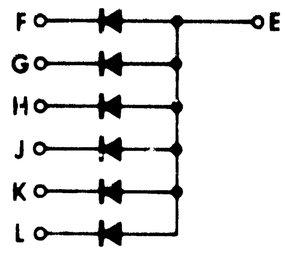
Temperature	85°C				125°C				
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	
Pulse Amplitude (V_{pp})	1.6	3.0	1.6	1.5	1.5	3.0	1.5	1.5	Minimum clock pulse width =31ns at -55°C. =<23ns at 25°C = 53 ns at 125°C N=5
Pulse Width (ns) 50-50%	518	200	480	476	520	200	477	476	X_{cp} =2.5vp at -40 and -55°C =2.0vp at 25°C =1.3vp at 85 and 125°C
T_r (ns) 10 to 90%	61	6	31	28	75	6	51	57	
T_f (ns) 90 to 10%	5	8	6	12	6	8	8	15	
T_d (ns) X to 10%			47	47			54	52	
T_s (ns) X to 90%			21	21			19	20	
T Set Up 10% to X		31				45			

Circuit Designation A03	Vcc 6.0 Volts, Clock Pulse Rep. Rate 2 MC											
Temperature	-55°C				-40°C				25°C			
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5
Pulse Amplitude (V_{pp})	2.1	3.0	2.0	1.9	2.0	3.0	2.0	1.9	1.9	3.0	1.8	1.7
Pulse Width (ns) 50-50%	511	200	493	477	509	200	481	478	507	200	472	.489
T_r (ns) 10 to 90%	37	6	19	16	35	7	19	15	32	7	19	18
T_f (ns) 90 to 10%	4	7	6	13	3	7	5	11	3	8	5	11
T_d (ns) X to 10%			41	41			38	39			36	36
T_s (ns) X to 90%			26	28			15	17			14	14
T Set Up 10% to X		27				27			18			

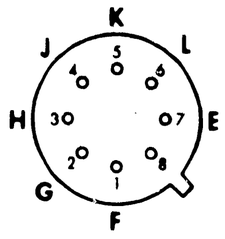
Temperature	85°C				125°C				Minimum clock pulse width = <23ns at -55°C = <23ns at 25°C = 53ns at 125°C N=5 X_{cp} =2.5vp at -40and -55°C =2.0vp at 25°C =1.3vp at 85 and 125°C
Test Circuit:	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	Logic Input	C.P. Input	Q Output N =1	Q Output N =5	
Pulse Amplitude (V_{pp})	1.8	3.0	1.7	1.7	1.6	3.0	1.6	1.6	
Pulse Width (ns) 50-50%	515	200	497	477	519	200	467	481	
T_r (ns) 10 to 90%	64	7	37	40	69	7	52	64	
T_f (ns) 90 to 10%	5	7	6	13	6	7	8	16	
T_d (ns) X to 10%			49	46			53	50	
T_s (ns) X to 90%			16	16			17	17	
T Set Up 10% to X		40				47			

AC4 Diode Array
Characteristic Data and Graphs

CIRCUIT DIAGRAM

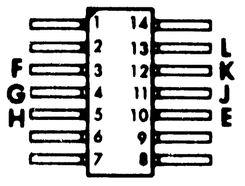


PIN DIAGRAMS



BOTTOM VIEW

MODIFIED TO-5

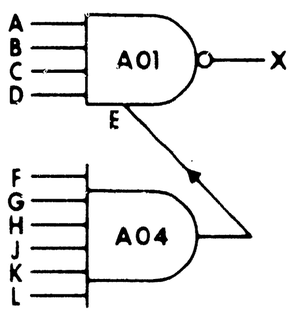


TOP VIEW

FLAT PAC

LOGIC DIAGRAM

The diode array is represented here in the normal application of expanding the inputs of a single NAND gate.



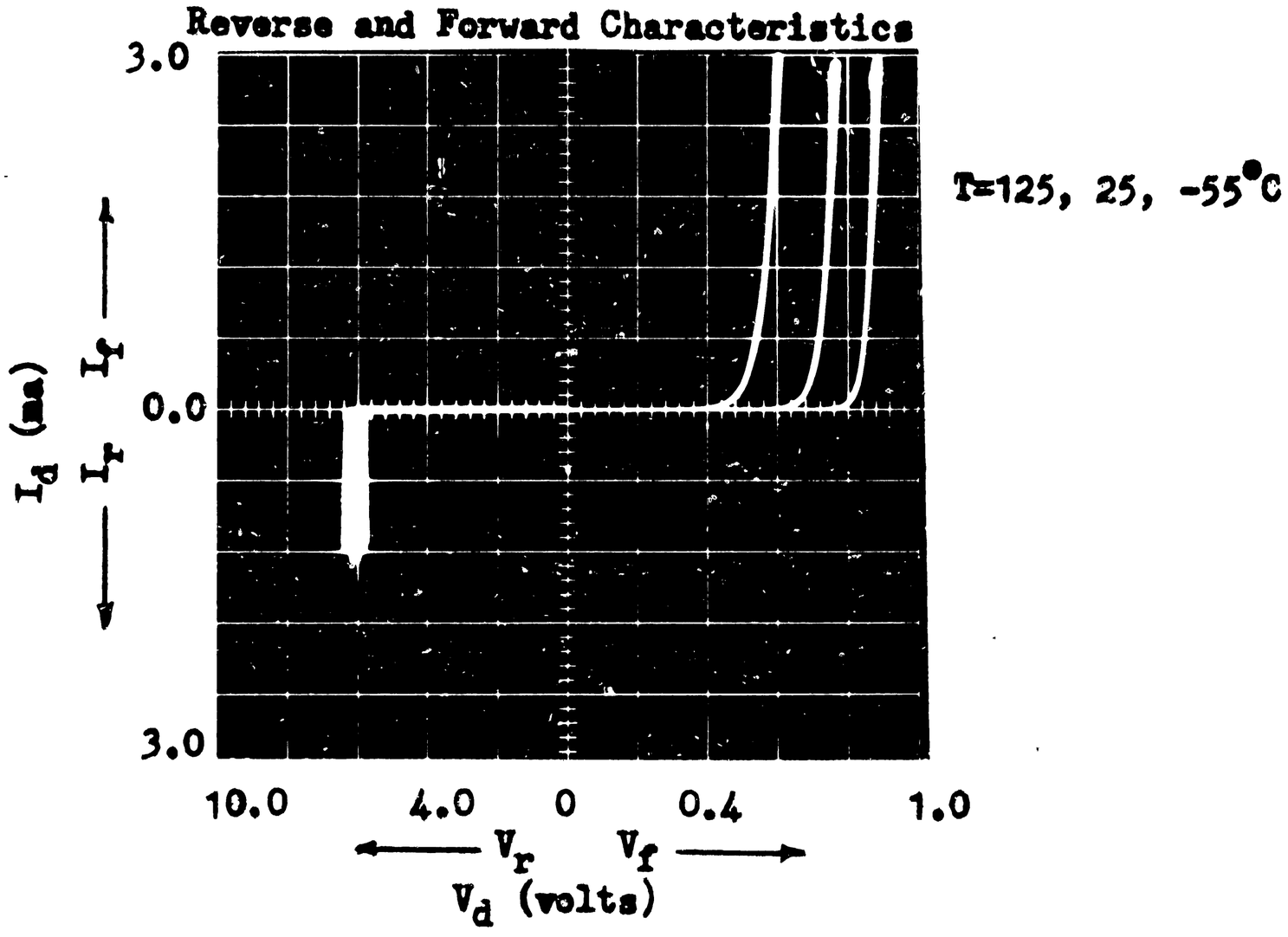
$X = \overline{ABCDFGHJKL}$

ABSOLUTE MAXIMUM RATINGS

Breakdown Voltage BV −55 to 125°C	6 v
Operating Temperature Range T_A	−55 to +125°C
Storage Temperature Range T_S	−65 to +150°C

Figure 3.1.19

AO4 DIODE ARRAY

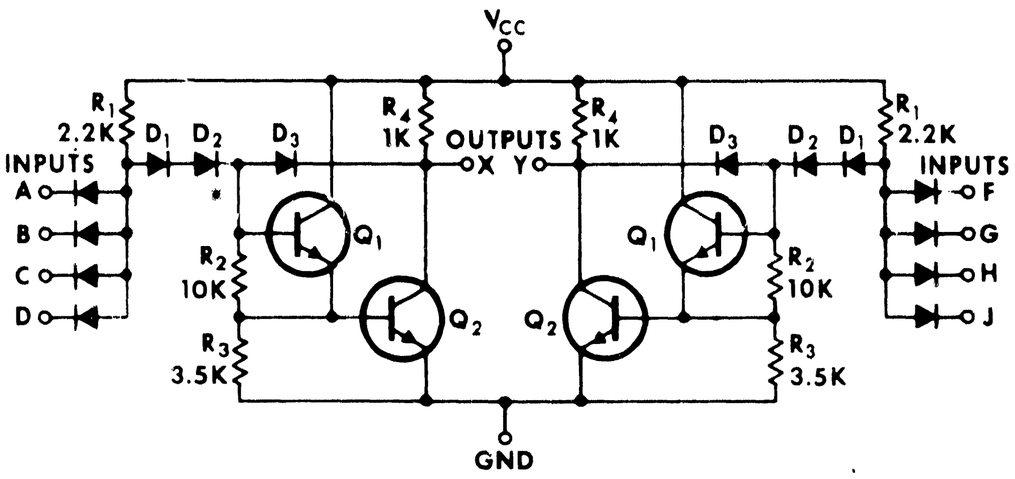


This is the only data obtained for this device.

Figure 3.1.20

AO5 Dual Line Driver
Characteristic Data and Graphs

CIRCUIT DIAGRAM

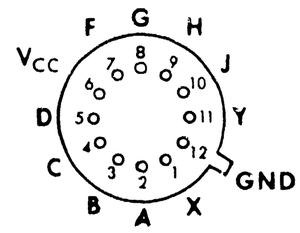


DUAL GATE

A05 Dual Line Driver

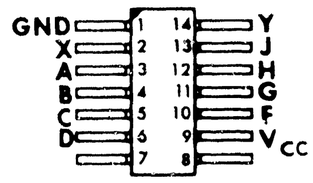
Figure 3.1.21

PIN DIAGRAMS



BOTTOM VIEW

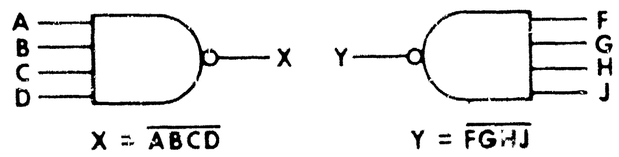
MODIFIED TO-5



TOP VIEW

FLATPAC

LOGIC DIAGRAM



$X = \overline{ABCD}$ $Y = \overline{FGHJ}$

ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC} . . . . . 6 v

Input Voltage BV_i . . . . . 6 v

Output Voltage BV_o . . . . . 6 v

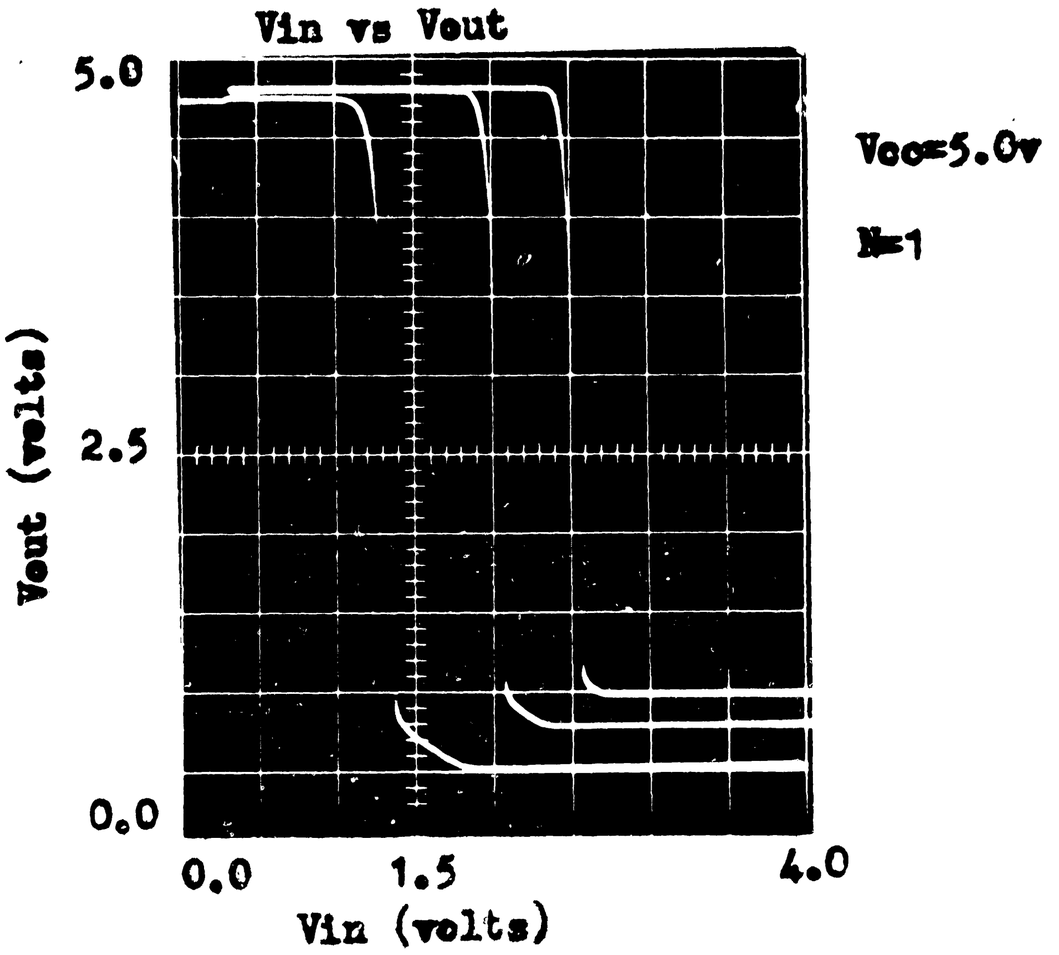
Operating Temperature Range T_A . . . . . −55 to +125°C

Storage Temperature Range T_S . . . . . −65 to +150°C

Output Current . . . . . 50 ma

Voltage at any pin must be positive with respect to the common terminal.

AO5 DUAL LINE DRIVER



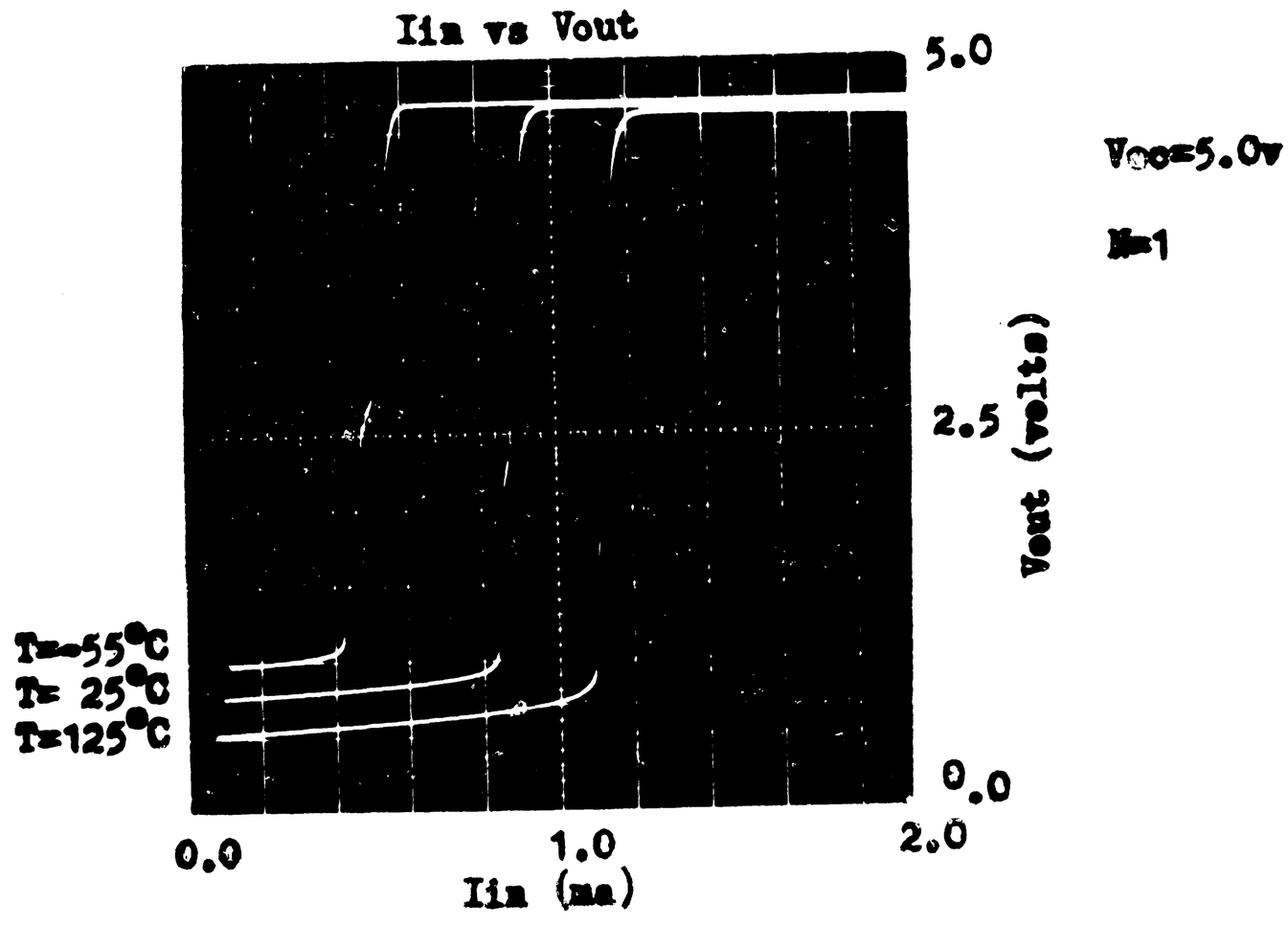
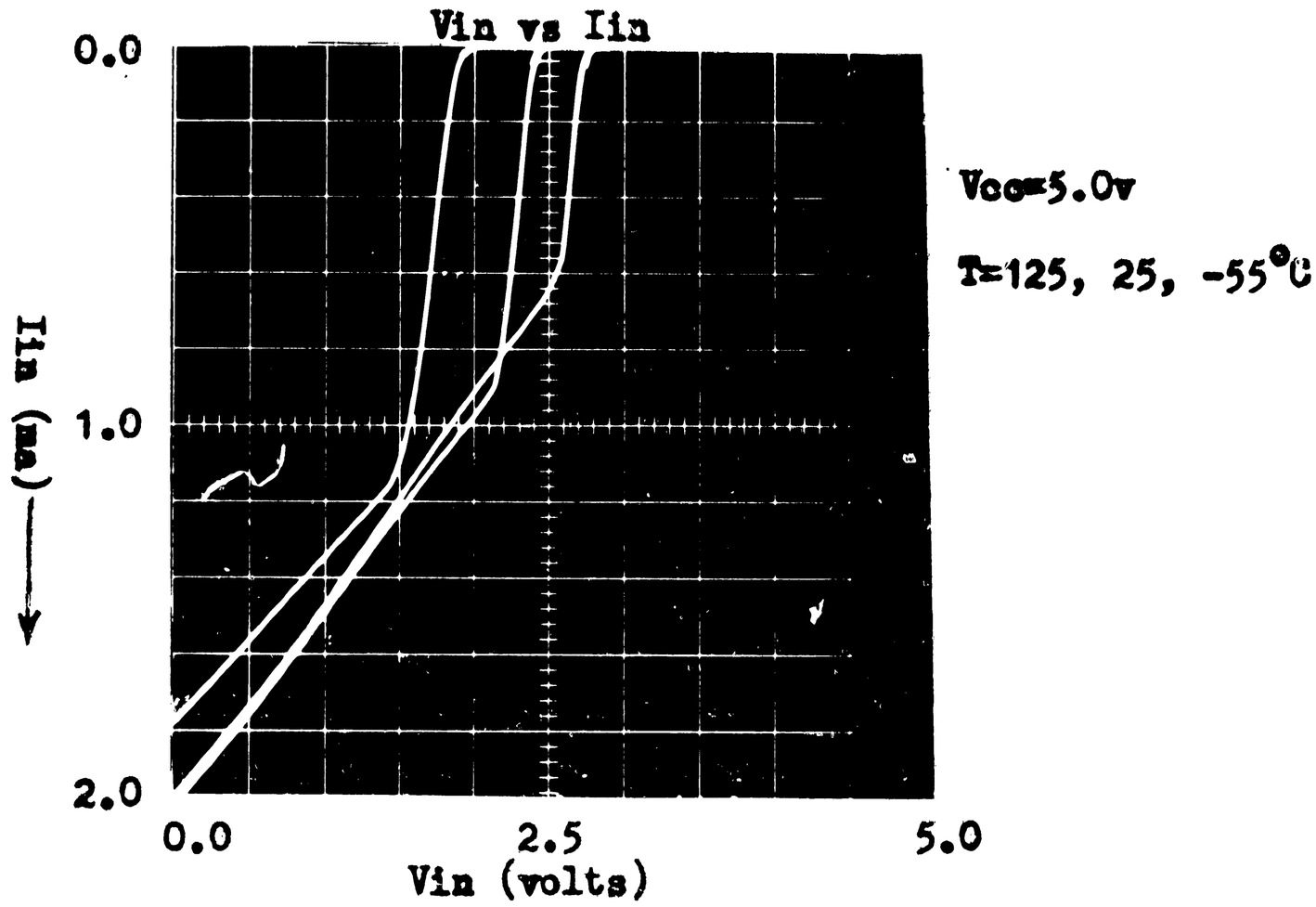


Figure 3.1.22


Vin vs Iin
0.0
1.0
2.0
Iin (ma)
0.0
2.5
5.0
Vin (volts)
Vcc=5.0v
T=125, 25, -55°C

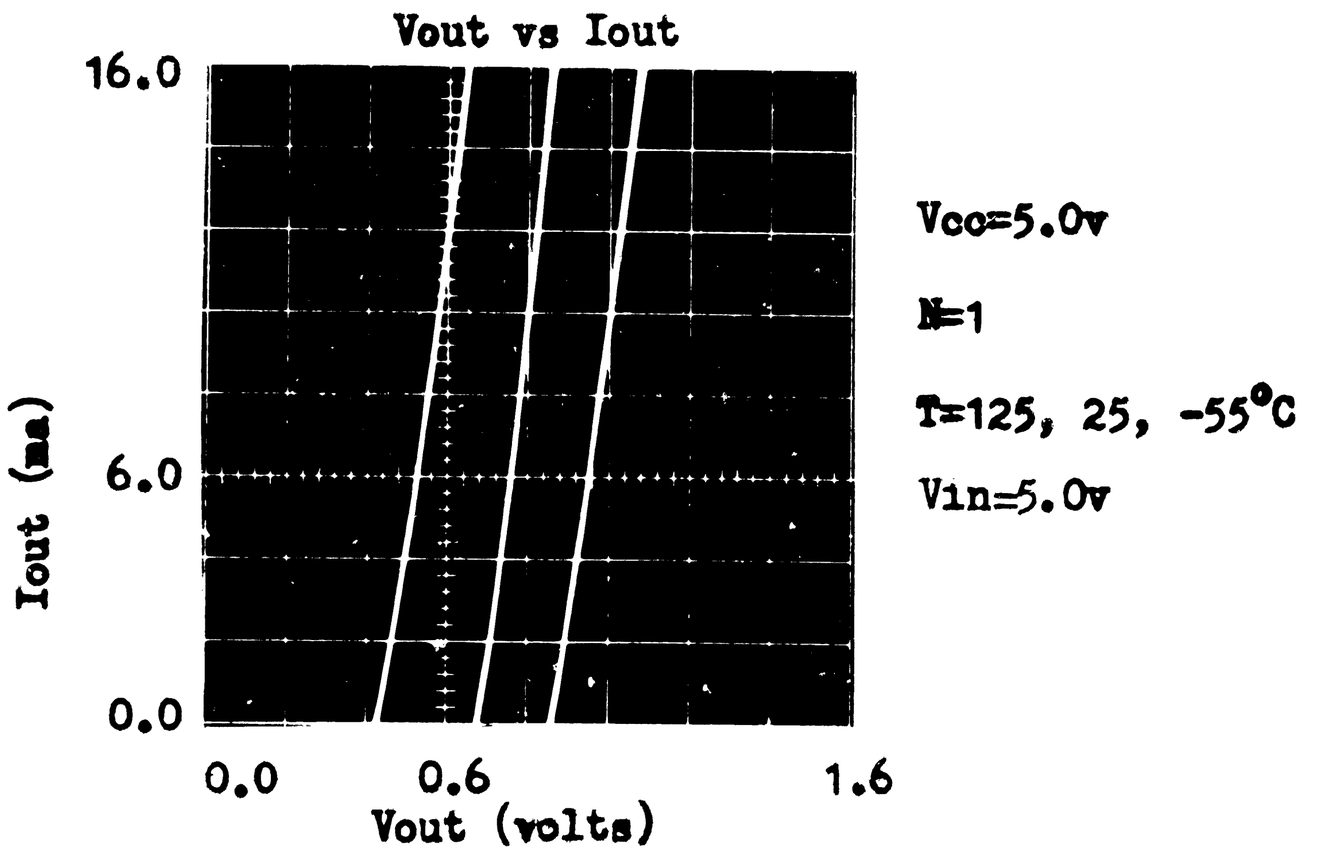
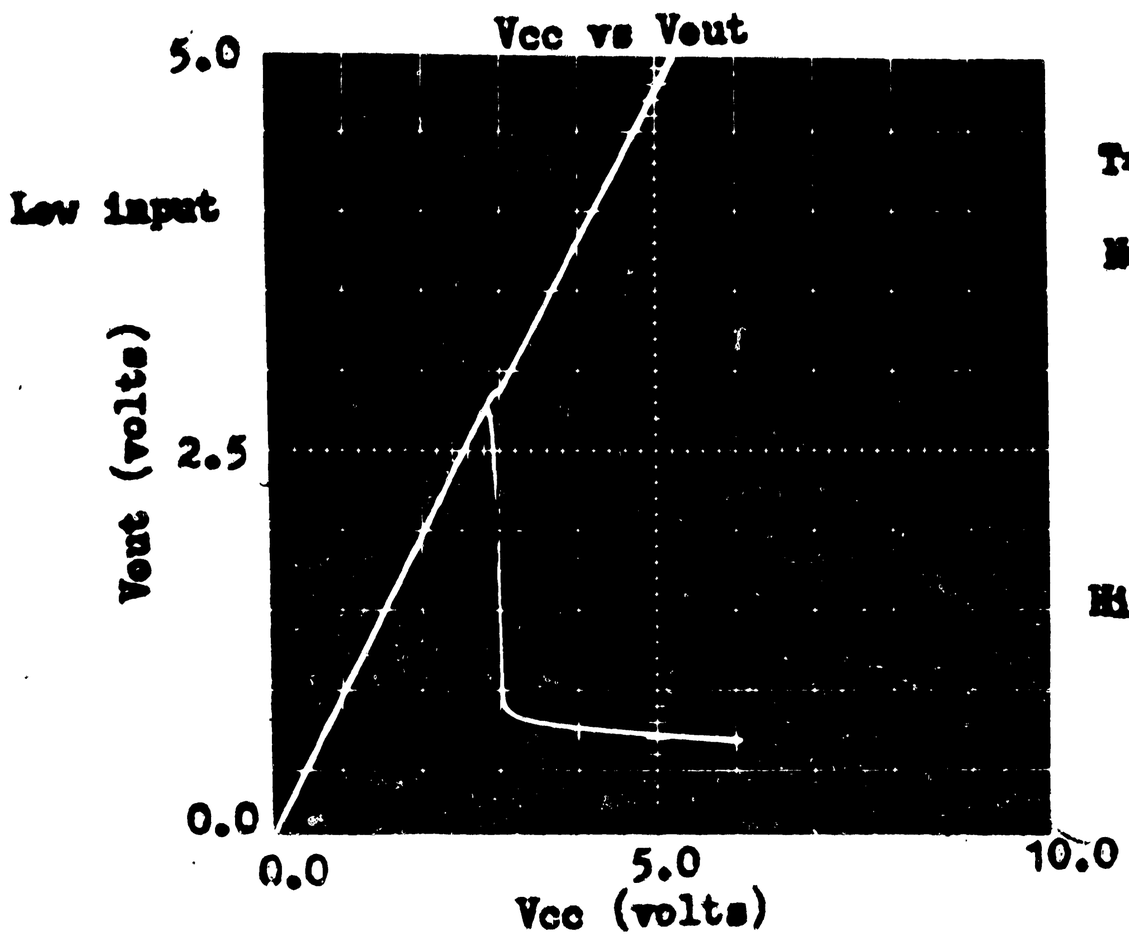
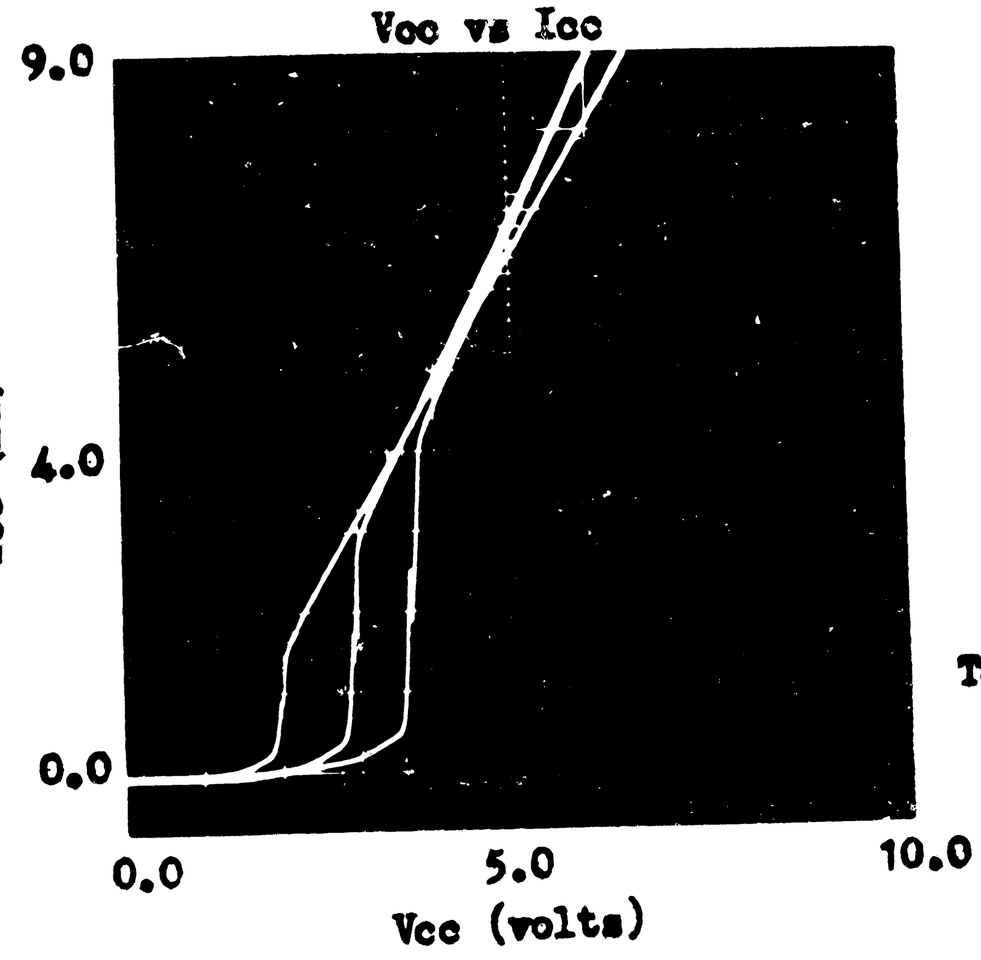

Vout vs Iout
16.0
6.0
0.0
Iout (ma)
0.0
0.6
1.6
Vout (volts)
Vcc=5.0v
N=1
T=125, 25, -55°C
Vin=5.0v

Figure 3.1.23

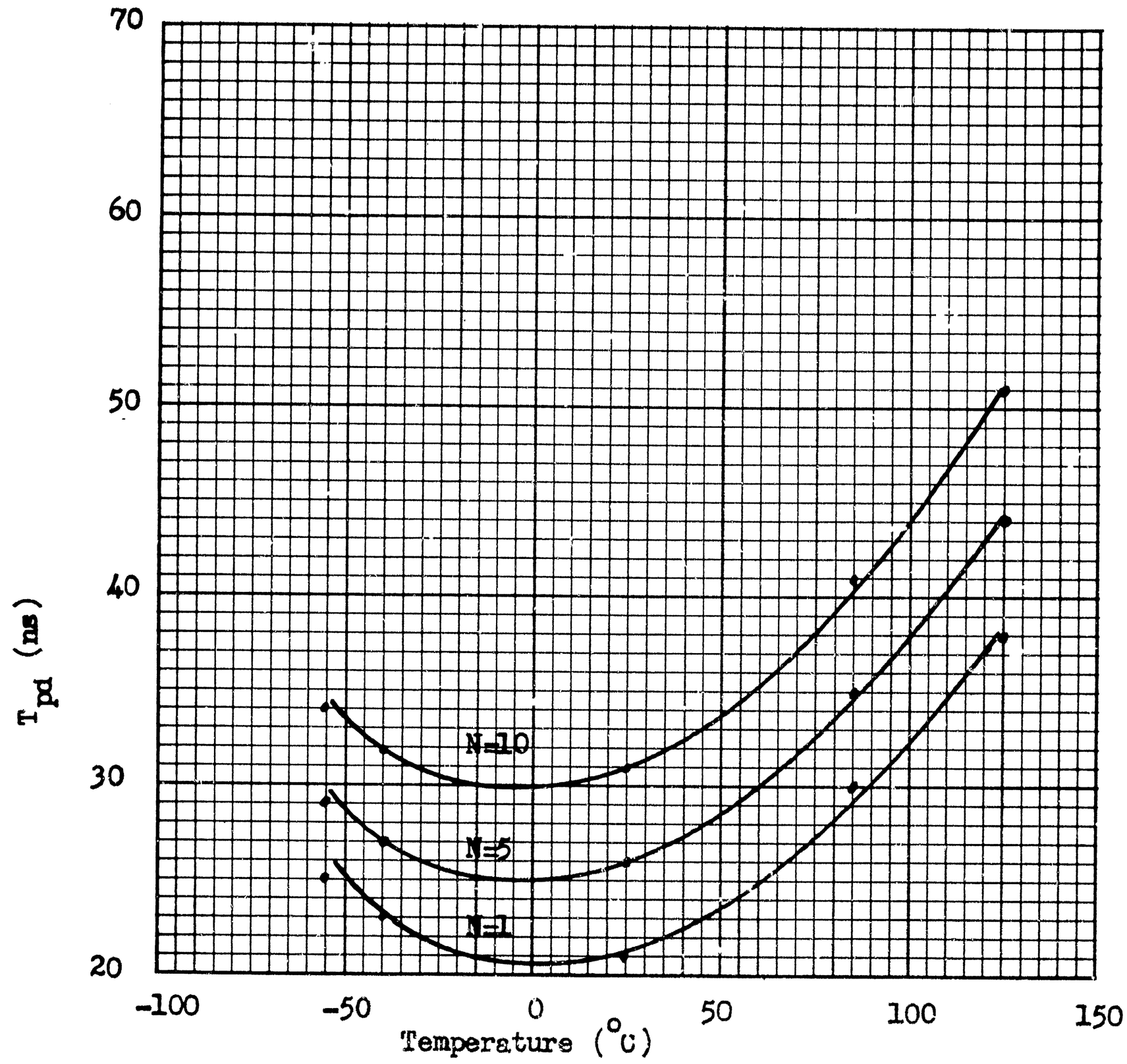
A05 DUAL LINE DRIVER





See the Vcc vs Ico curve of the A02 circuit for an explanation of the above curve.

Figure 3.1.24



A05 Dual Line Driver. Propagation delay vs temperature with the number of loads (N) as a Parameter. Vcc=5.0v

Figure 3.1.25

AO5 DUAL LINE DRIVER

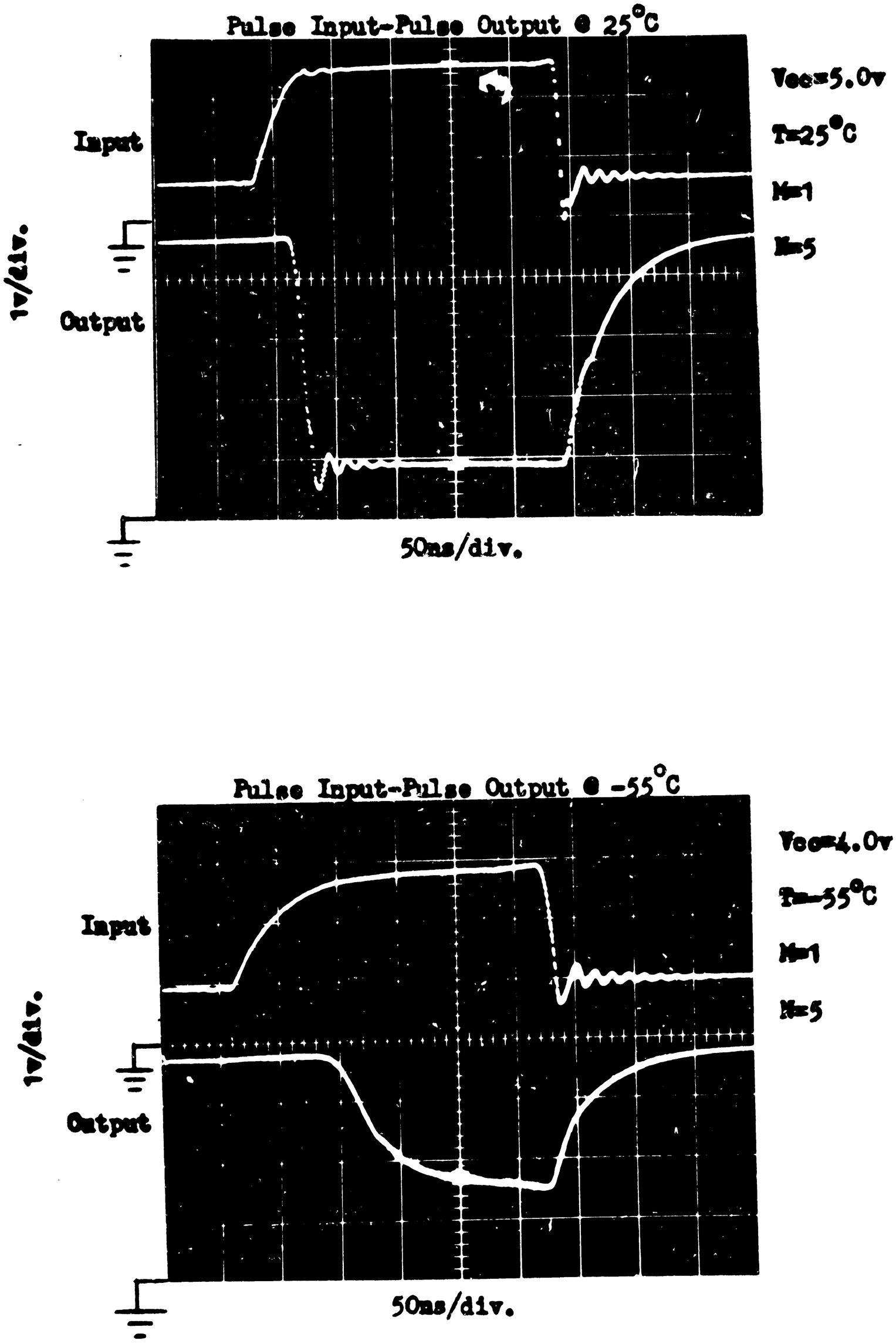
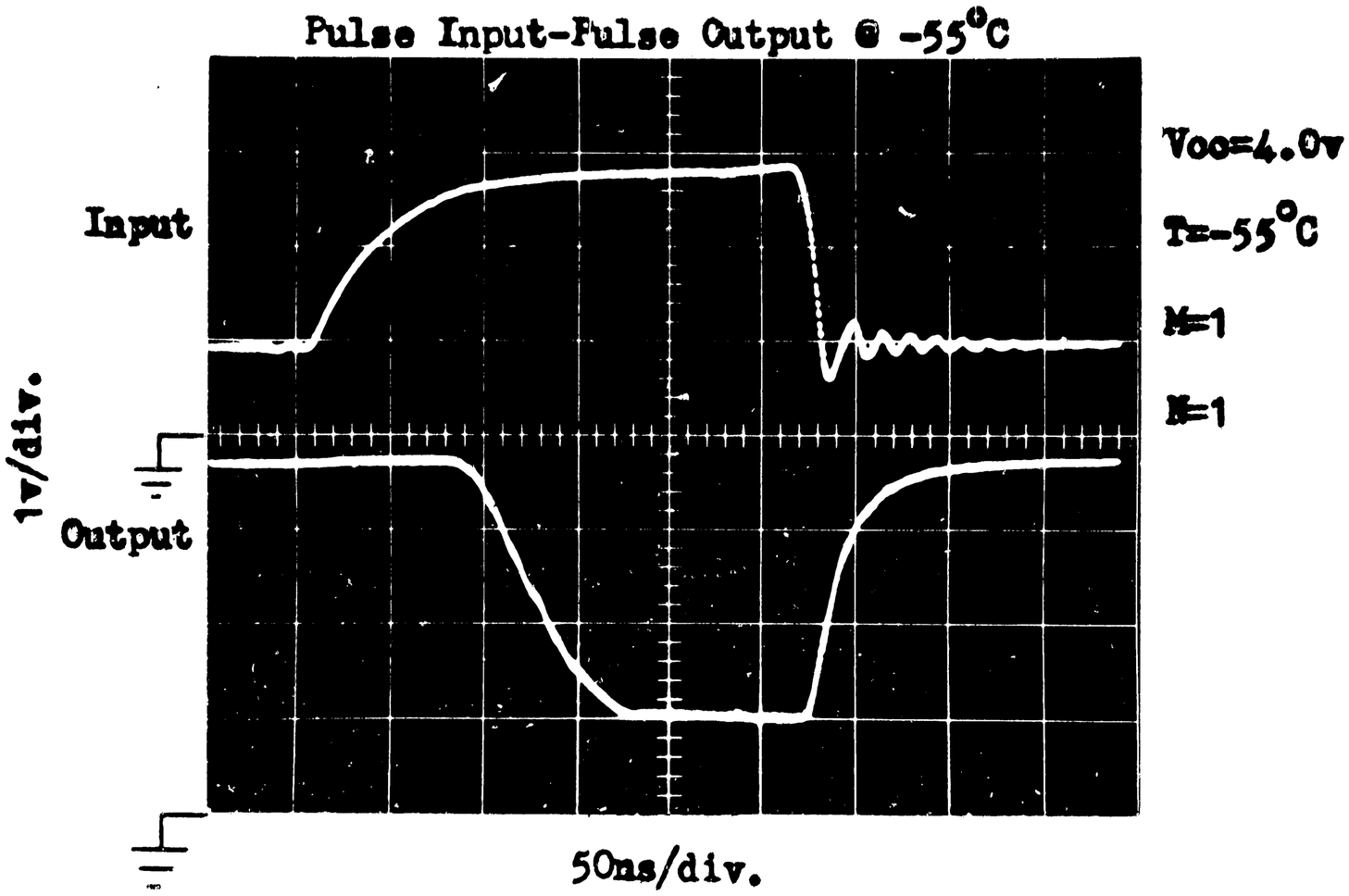


Figure 3.1.26

AO5 DUAL LINE DRIVER



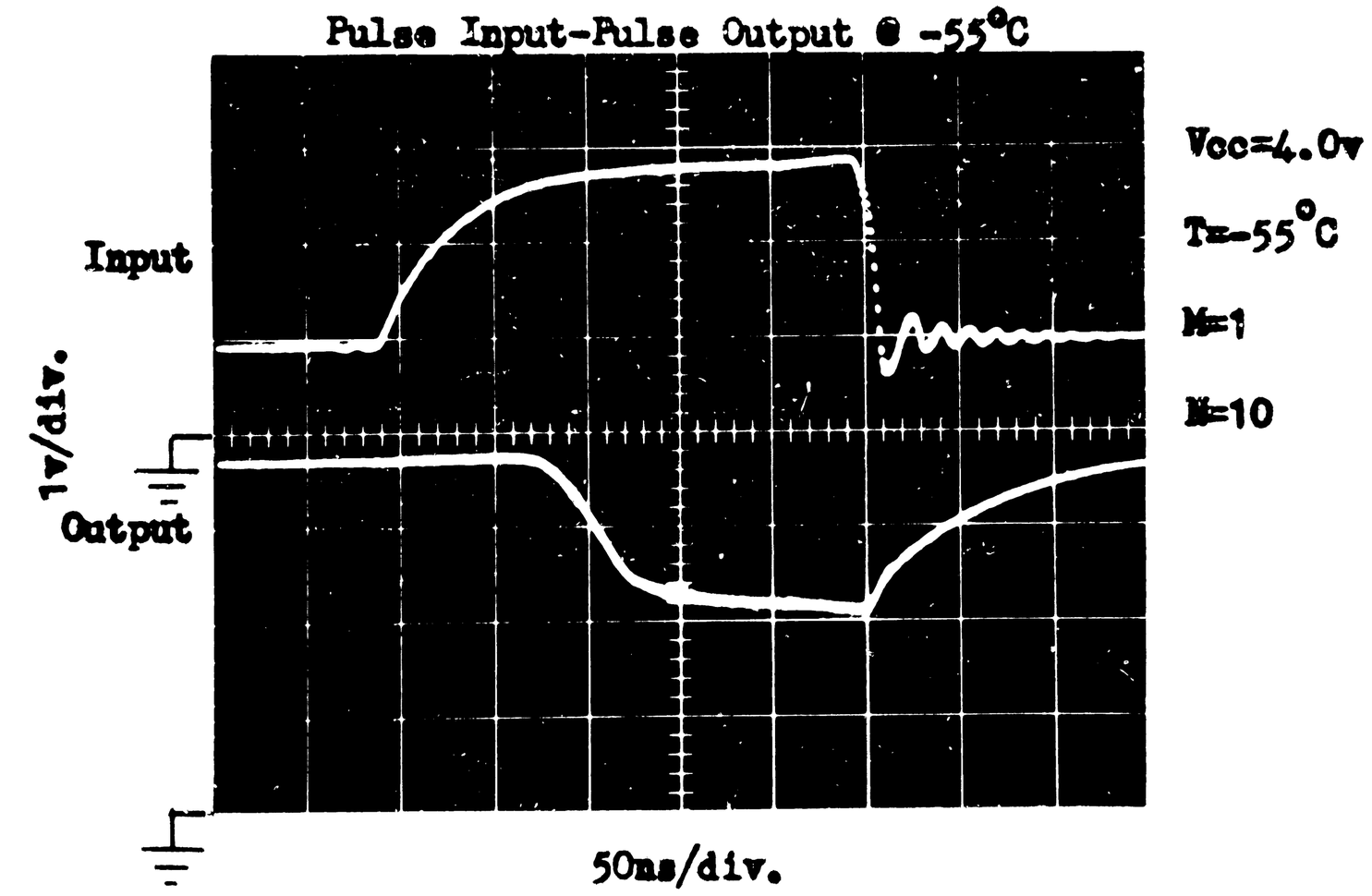


Figure 3.1.27

Circuit Designation 405 , Fan-In 1 , Vcc 4.0 Volts, Input Pulse Rep. Rate 1 MC												
Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	1.9	2.8	2.	1.8	1.9	2.8	2.7	2.2	1.8	3.0	2.9	2.9
Pulse Width (ns)	250	171	179	192	250	191	200	200	250	232	235	242
T_r (ns)	82	44	85	119	73	45	80	119	50	50	83	121
T_f (ns)	9	60	84	62	8	35	52	77	6	14	18	23
T_d (ns)		90	92	90		75	73	77		44	45	46
T_s (ns)		6	6	7		6	7	7		8	8	9
T_{pd} (ns)		56	57	65		42	44	50		25	26	34

Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	1.7	1	3.0	3.0	1.6	3.2	3.1	3.0
Pulse Width (ns)	250	248	256	264	250	268	275	285
T_r (ns)	66	55	94	138	72	74	112	157
T_f (ns)	6	11	14	17	6	11	14	15
T_d (ns)		59	60	60		62	61	62
T_s (ns)		9	10	10		12	13	15
T_{pd} (ns)		25	29	35		33	36	43

Circuit Designation A05 , Fan-In 1 , Vcc 5.0 Volts, Input Pulse Rep. Rate 1 MC

Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	2.1	3.9	3.8	3.7	2.0	3.9	3.8	3.7	1.9	4.1	4.0	3.9
Pulse Width (ns)	250	232	239	244	250	235	242	250	250	248	257	264
T_r (ns)	40	47	82	119	37	46	79	118	32	50	85	124
T_f (ns)	5	14	20	30	5	12	17	23	4	9	12	14
T_d (ns)		41	40	42		37	38	38		30	30	30
T_s (ns)		7	8	8		7	8	8		8	8	9
T_{pd} (ns)		25	29	34		23	27	32		21	26	31

Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	1.8	4.0	4.1	4.0	1.6	4.2	4.1	4.0
Pulse Width (ns)	250	271	278	287	250	283	296	308
T_r (ns)	54	68	105	150	69	68	109	167
T_f (ns)	5	8	10	12	6	10	11	13
T_d (ns)		50	51	52		63	63	64
T_s (ns)		12	13	13		31	33	27
T_{pd} (ns)		30	35	41		38	44	51

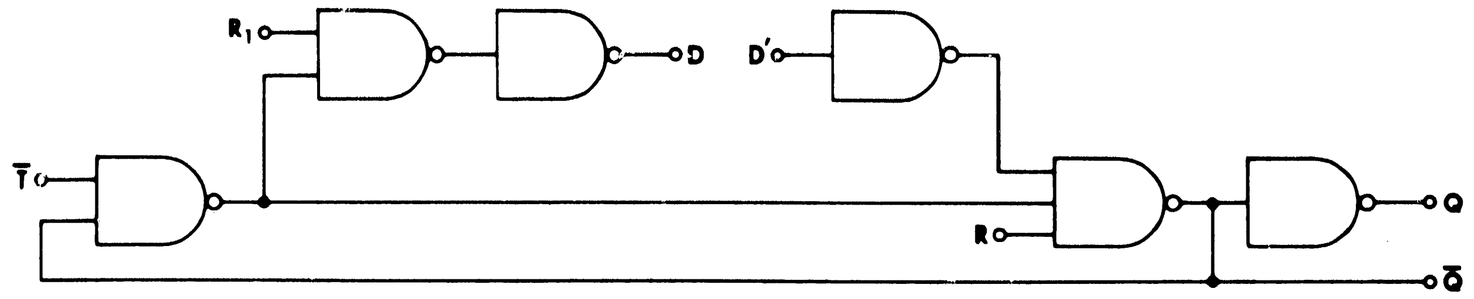
Circuit Designation A05 , Fan-In 1 , Vcc 6.0 Volts, Input Pulse Rep. Rate 1 MC

Temperature	-55°C				-40°C				25°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	2.3	4.8	4.8	4.7	2.2	4.9	4.8	4.7	2.0	5.0	4.9	4.8
Pulse Width (ns)	250	244	248	261	250	246	252	262	250	260	257	277
T_r (ns)	27	46	80	119	25	46	79	118	30	60	89	128
T_f (ns)	4	10	14	19	4	9	12	16	4	7	9	10
T_d (ns)		29	30	30		27	28	28		30	30	28
T_s (ns)		7	8	8		7	8	8		8	8	10
T_{pd} (ns)		20	26	31		20	25	30		23	28	33

Temperature	85°C				125°C			
Test Circuit:	Input	Output @ N =			Input	Output @ N =		
		1	5	10		1	5	10
Pulse Amplitude (V_{pp})	1.9	5.1	4.1	5.0	1.7	5.1	4.1	5.0
Pulse Width (ns)	250	281	292		250	289	303	319
T_r (ns)	57	61	99	151	73	71	112	164
T_f (ns)	5	8	9	10	7	10	11	12
T_d (ns)		53	53	54		66	67	68
T_s (ns)		28	30	23		34	34	35
T_{pd} (ns)		33	35	46		39	47	55

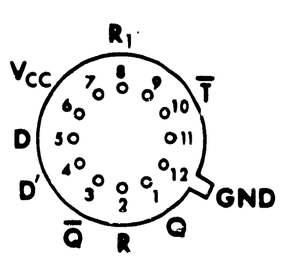
AO8 Monostable Multivibrator
Characteristic Data and Graphs

BLOCK DIAGRAM



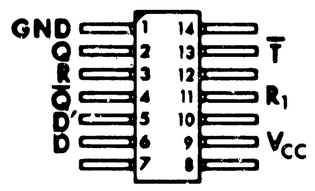
A08 Monostable Multivibrator

PIN DIAGRAMS



BOTTOM VIEW

MODIFIED TO-5

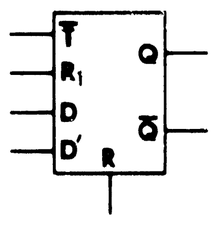


TOP VIEW

FLAT PAC

Figure 3.1.28

LOGIC DIAGRAM



TERMINAL IDENTIFICATION

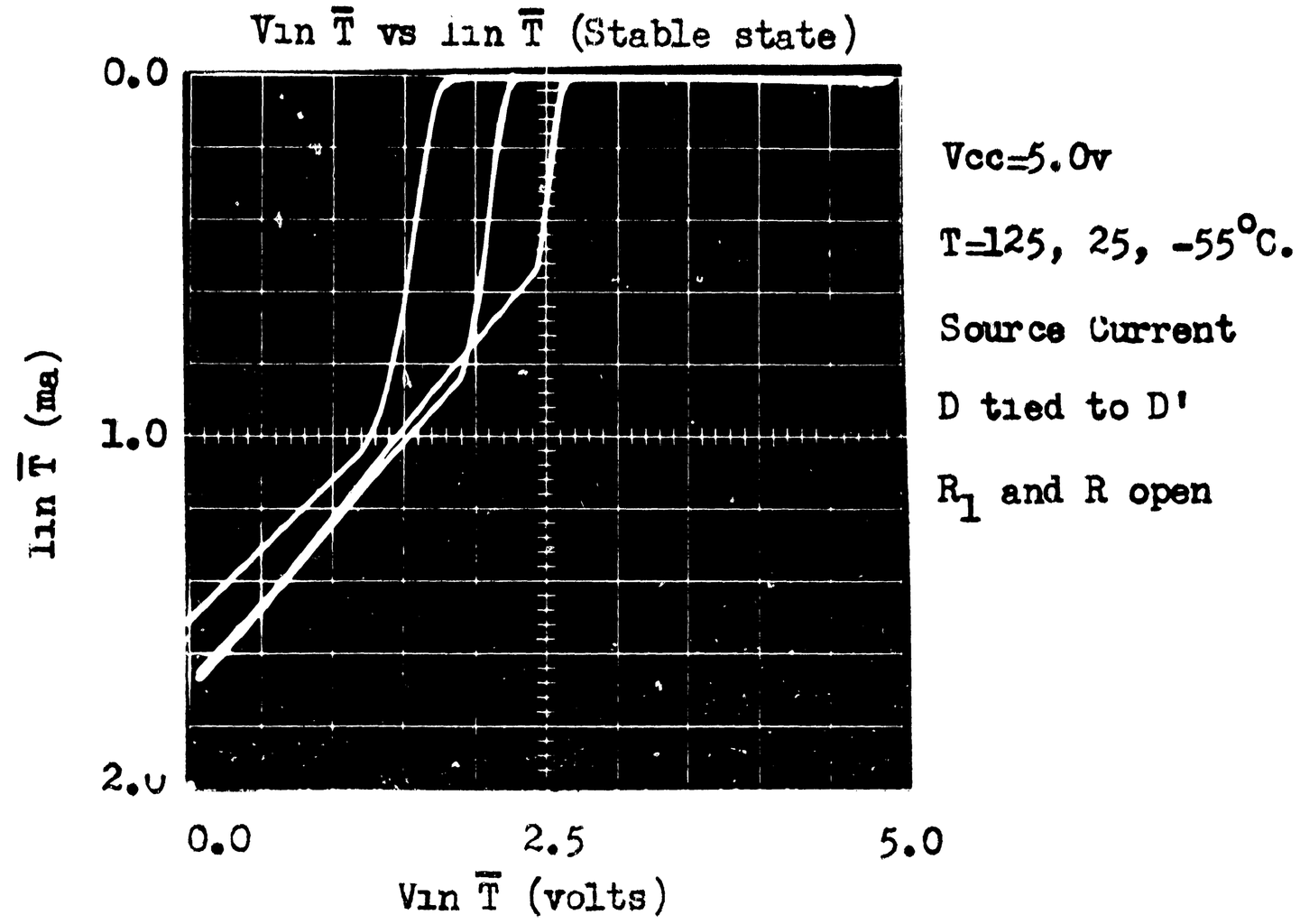
$\overline{T}$ – INPUT
R_1 – TIMING ENABLE TERMINAL
R – RESET TERMINALS
D, D′ – DELAY TERMINALS
Q, $\overline{Q}$ – COMPLEMENTARY OUTPUTS

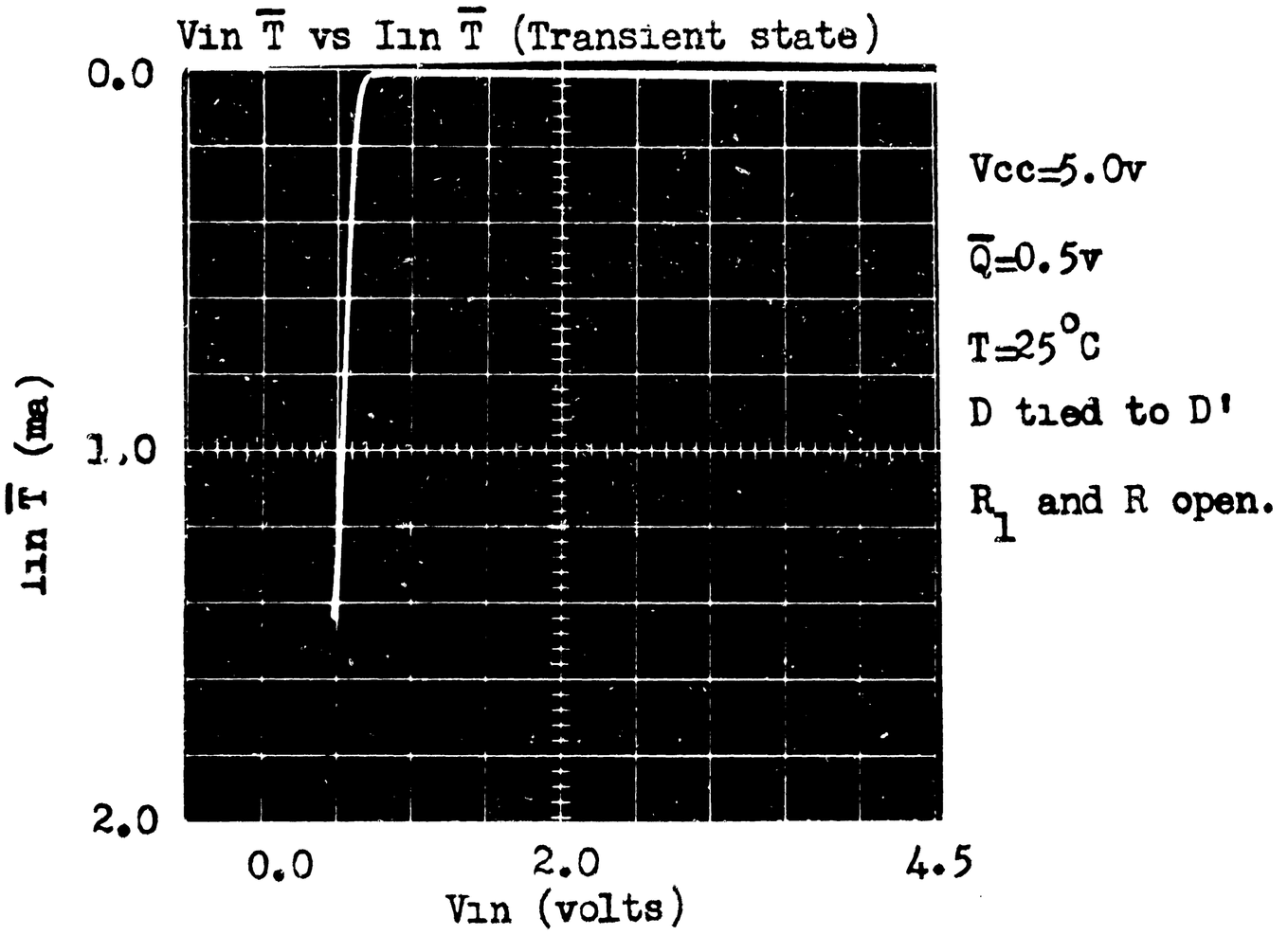
ABSOLUTE MAXIMUM RATINGS AT 25°C

Power Supply Voltage V_{CC} . . . . . 6 v
Input Voltage BV_i . . . . . 6 v
Output Voltage BV_o . . . . . 6 v
Operating Temperature Range T_A . . . . . −55 to +125°C
Storage Temperature Range T_s . . . . . −65 to +150°C
Output Current . . . . . 50 ma

Voltage at any pin must be positive with respect to the common terminal.

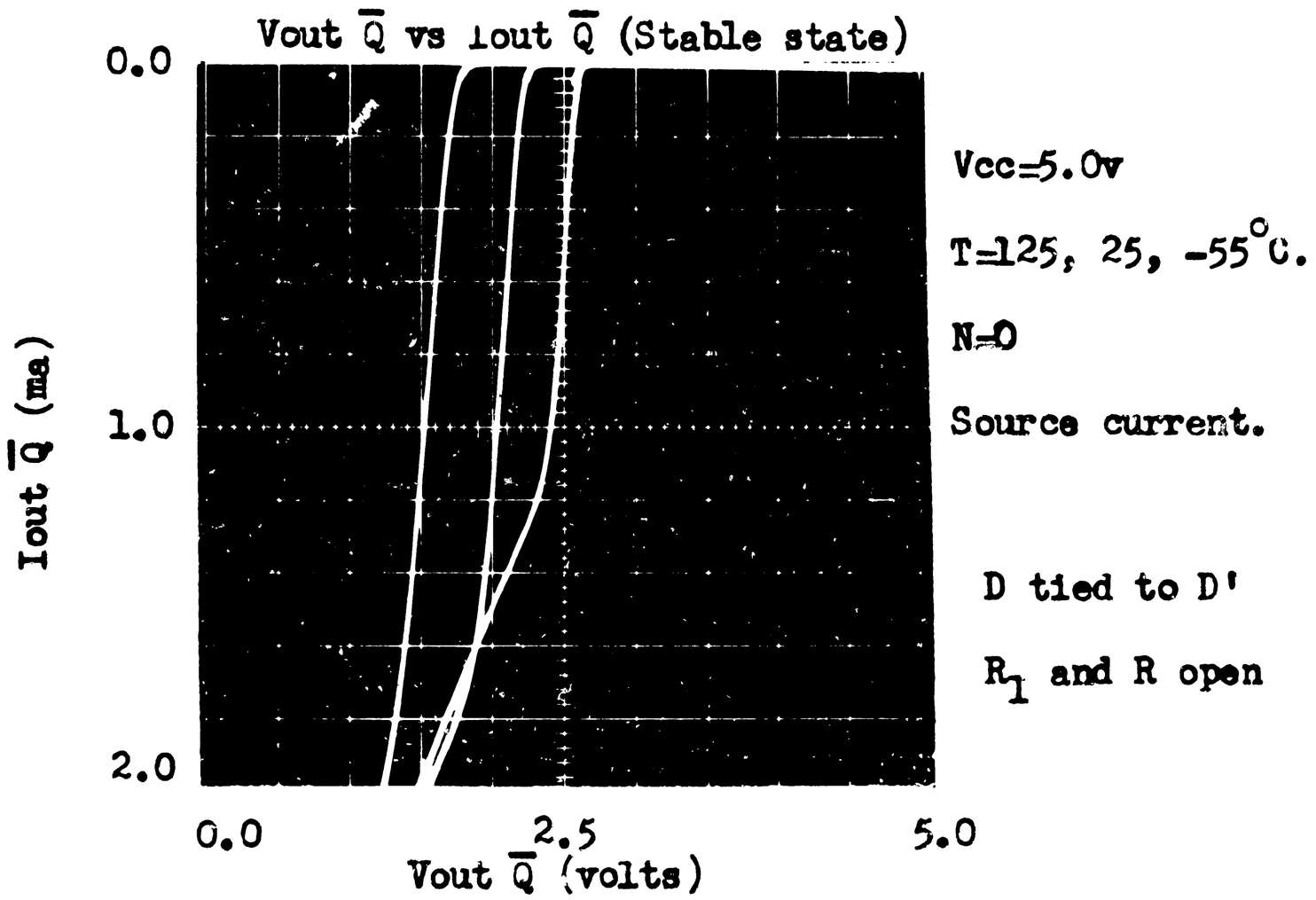
A08 MONOSTABLE MULTIVIBRATOR





Note: To obtain the above curve $\overline{Q}$ was tied to a 0.5v supply. In actual operation Vin would approach the voltage $\overline{Q}$ assumes in its transient state. **Figure** 3.1.29

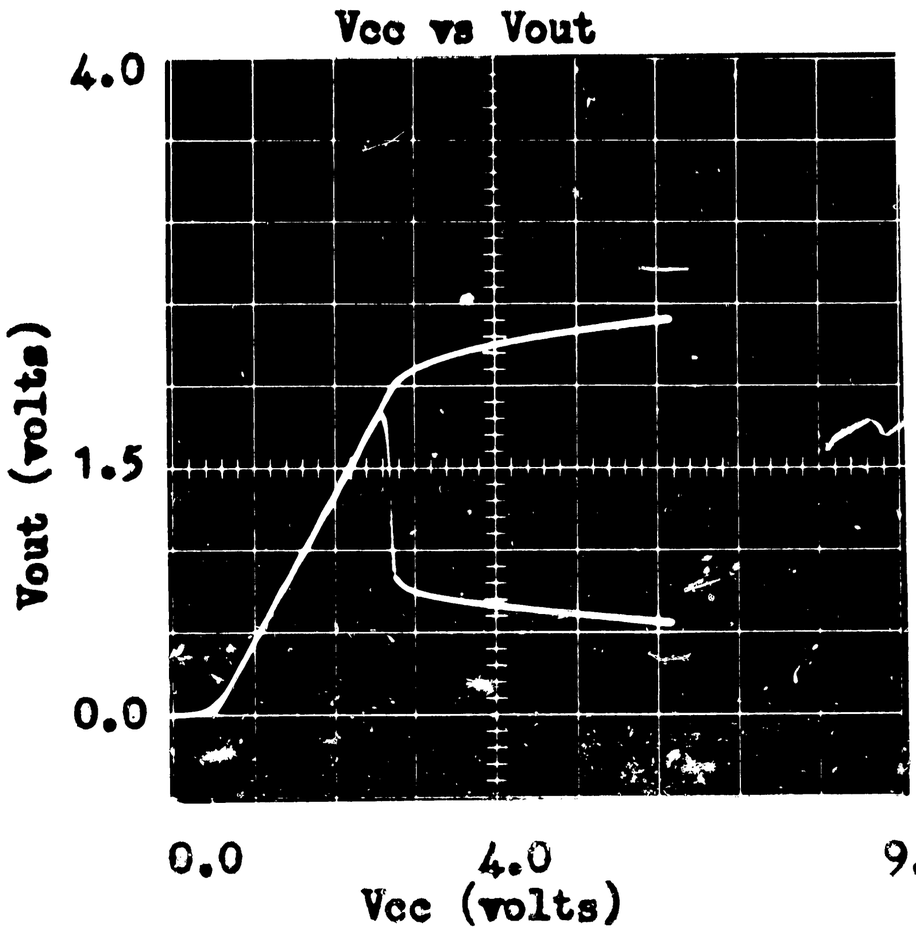
A08 MONOSTABLE MULTIVIBRATOR



Note: Refer to the Vout vs Iout curve for the A02 if the stable state Vout Q vs Iout Q curve for the A08 is desired. The two curves are identical.

Figure 3.1.30

AO8 MONOSTABLE MULTIVIBRATOR

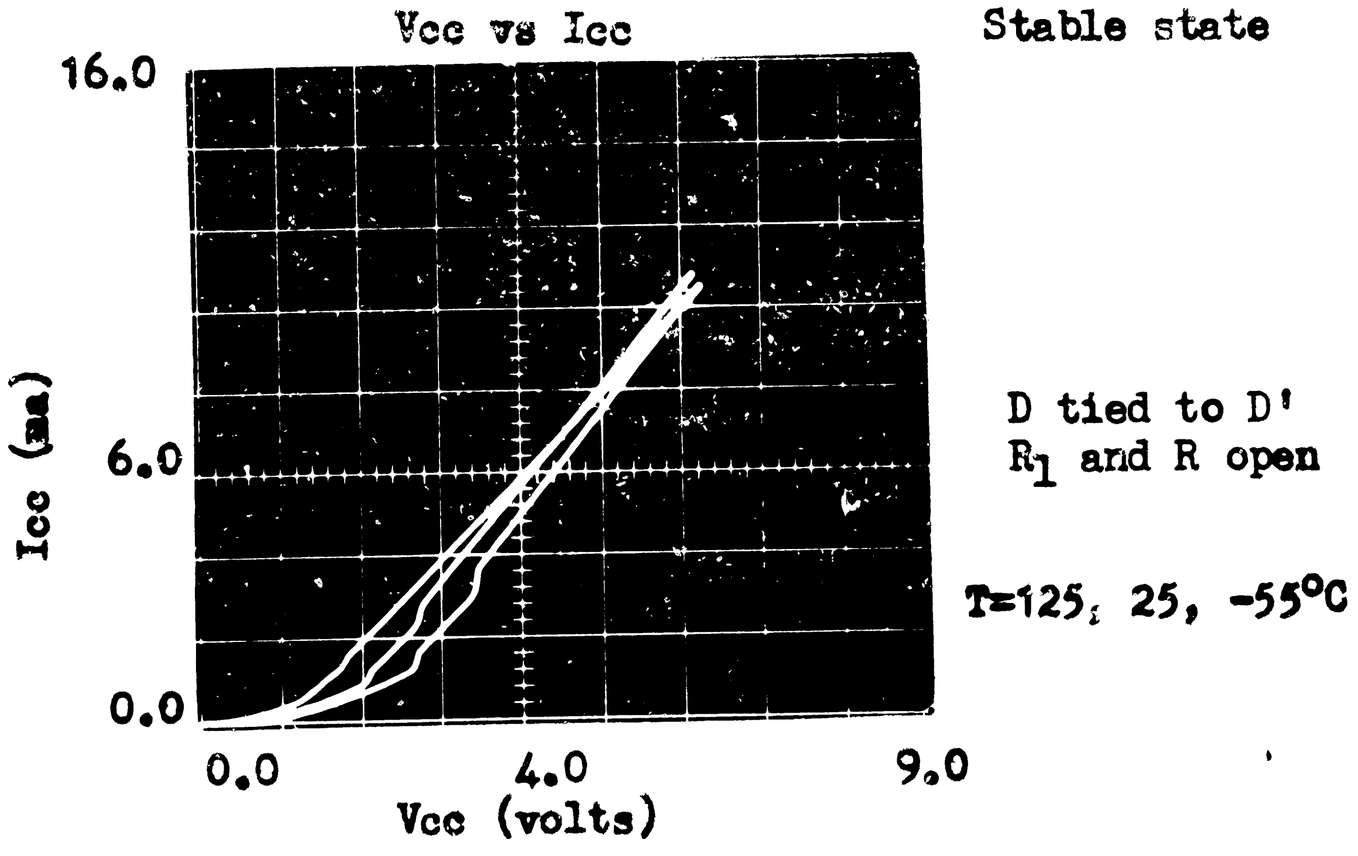


Stable state

—

Q output
N=1
Vcc=5.0v
T=25°C

Q output
N=1
D tied to D'
R_1 and R open

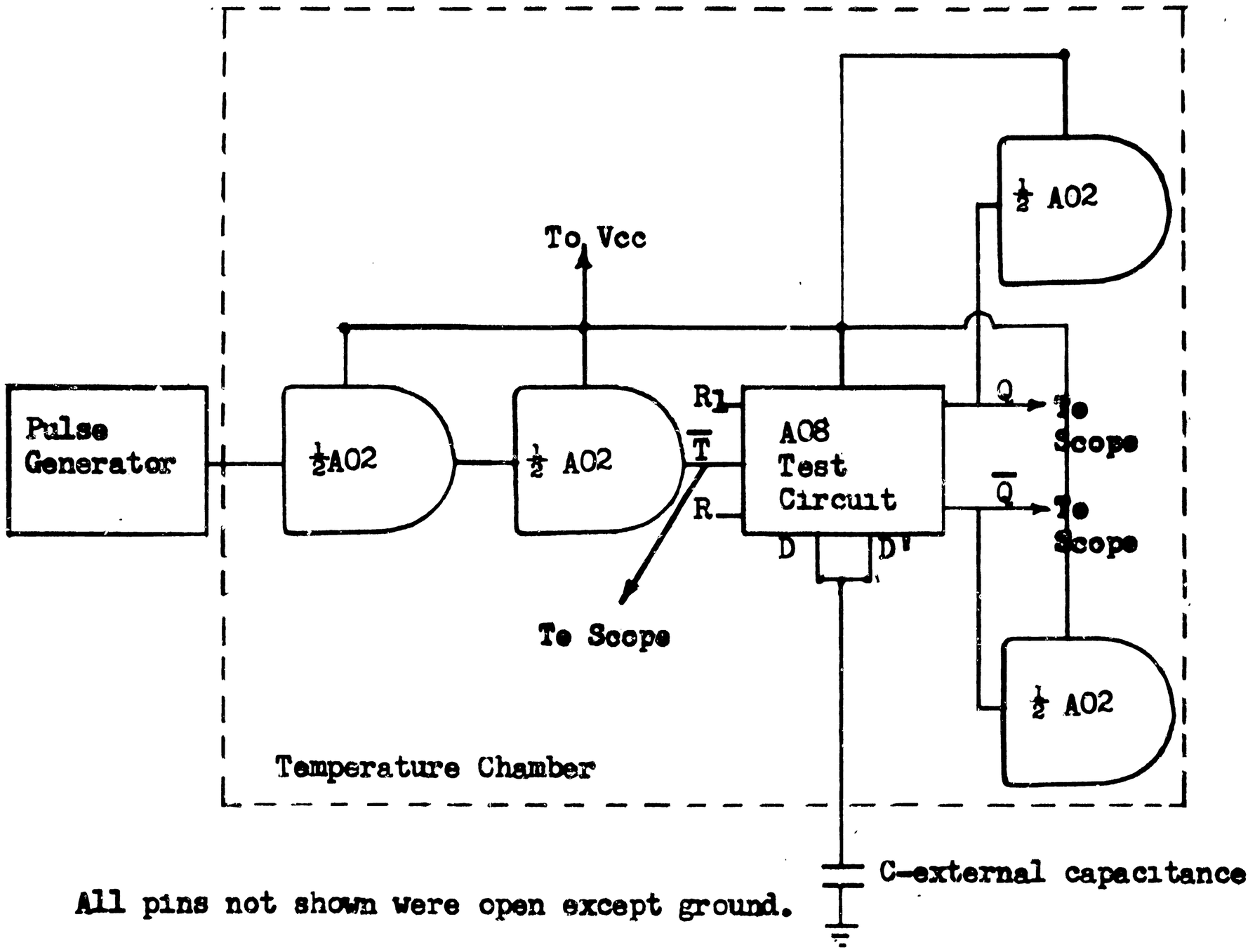


Stable state

D tied to D'
R_1 and R open

T=125, 25, -55°C

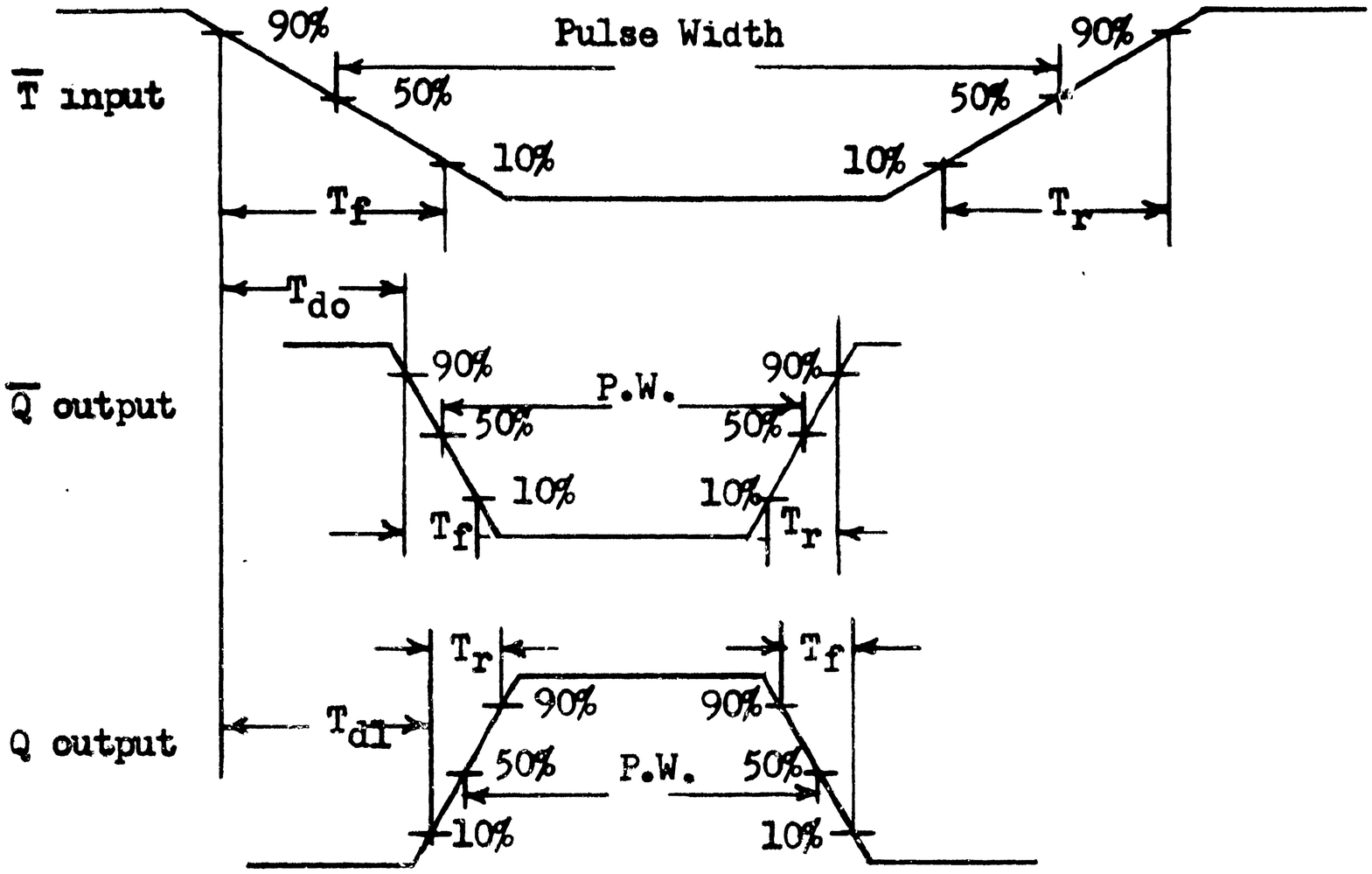
Figure 3.1.31



All pins not shown were open except ground.

Test Set-Up for the A08 one-shot multivibrator.

Figure 3.1.32



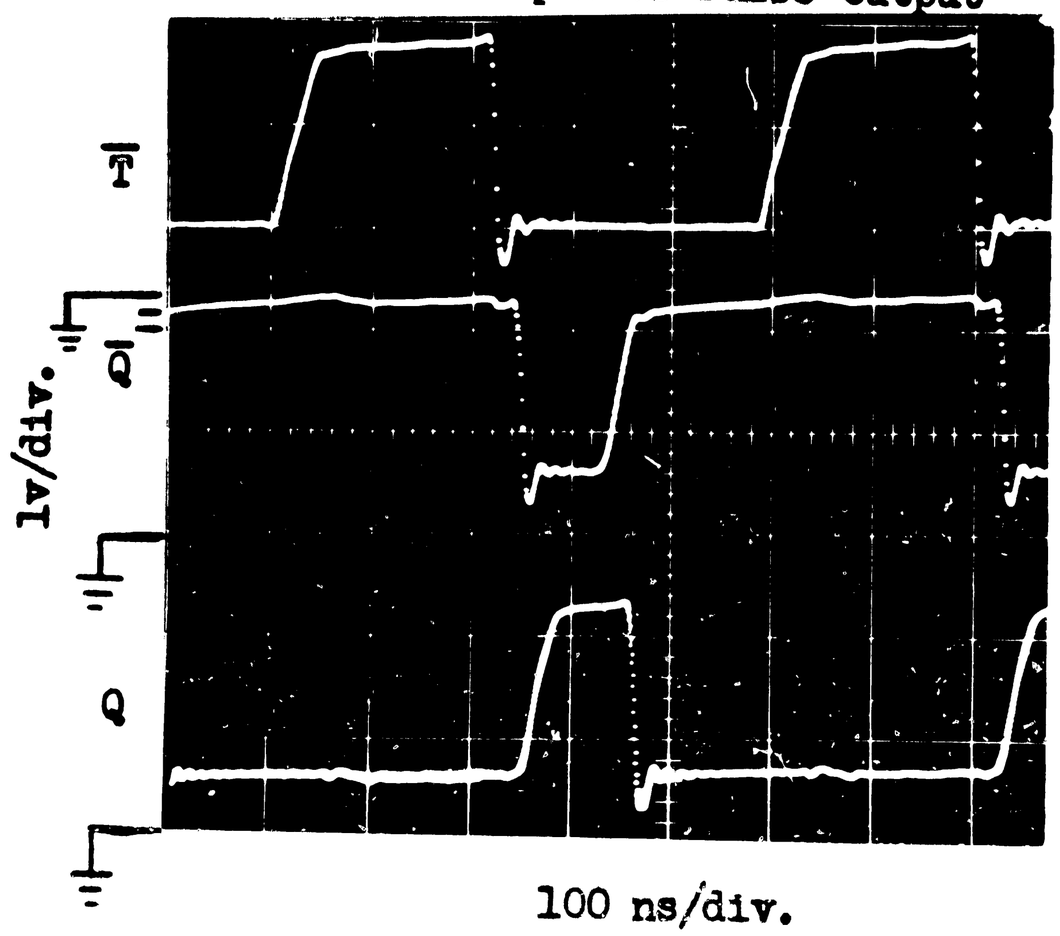
A08 One-Shot Multivibrator Waveform Definition.

Rise time (T_r), Fall time (T_f), Delay time of the $\overline{Q}$ output, one to zero transient (T_{do}), Delay time of the Q output, zero to one transient (T_{d1}).

Figure 3.1.33

A08 MONOSTABLE MULTIVIBRATOR

Pulse Input vs Pulse Output



Vcc=5.0v

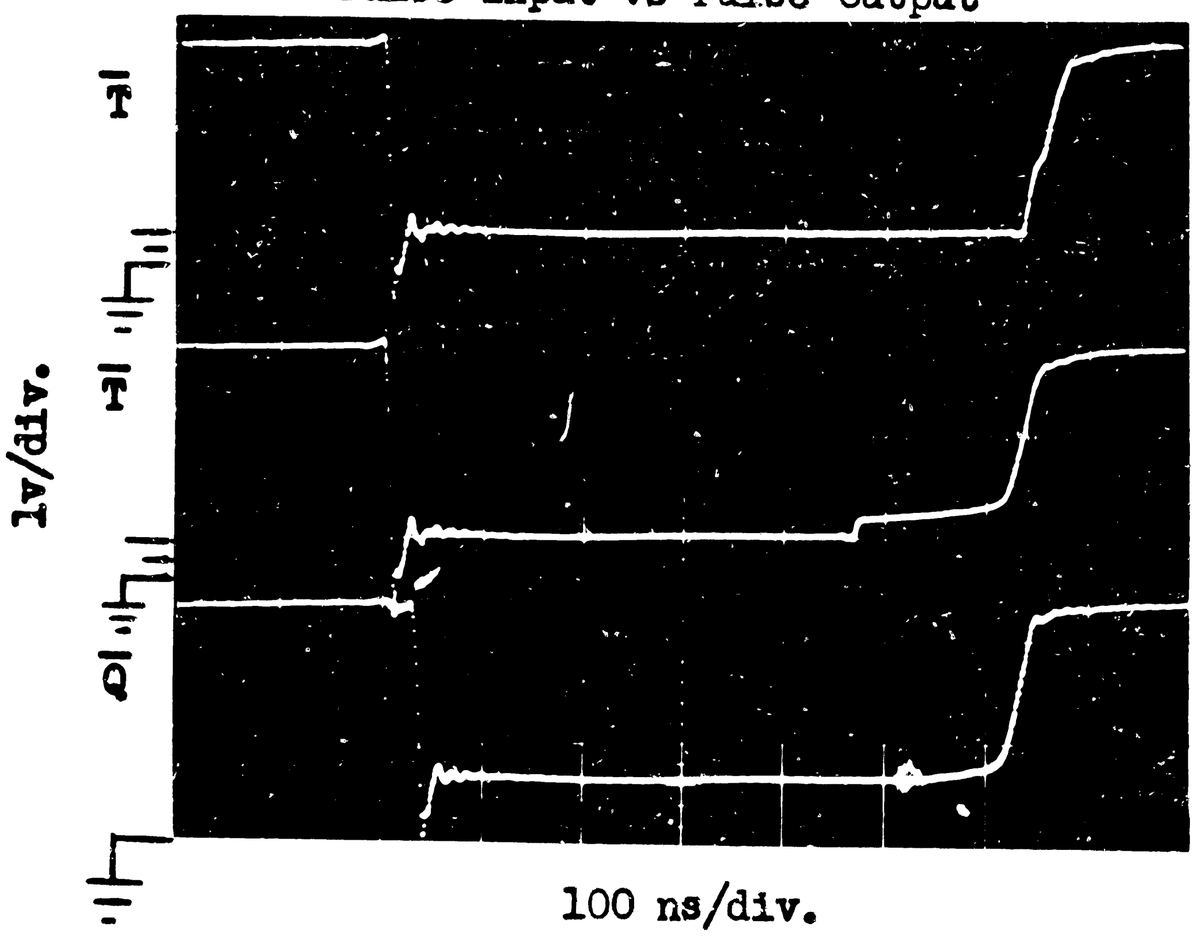
C=0 ie.,D tied to D'

T=25°C

N=1

$\overline{T}$ is the output of an A02 Dual NAND/NOR Gate.

Pulse Input vs Pulse Output



Vcc=5.0v

T=25°C

N=1

The bottom oscillograph was obtained using the output of an A02 Dual NAND/NOR gate to furnish the $\overline{T}$ input and a value of capacitance from D-D' to ground to produce the $\overline{Q}$ output shown. The oscillograph illustrates (center trace) that the $\overline{T}$ input will remain at a low voltage level as long as the $\overline{Q}$ output is low ie., in its transient state. This would not occur if a pull up resistor were used on the output of the driving circuit. The top trace shows an input pulse width of sufficient duration so as not to be affected by the output.

Figure 3.1.34

Circuit Designation A08				Fan-out 1		Vcc 4.0v		Pulse Rep. Rate 1M							
Temperature	-55°C					-40°C					25°C				
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf	
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$
Pulse Amplitude (Vpp)	1.9	1.7	1.8	1.7	1.8	1.9	1.7	1.7	1.7	1.8	1.7	1.6	1.6	1.6	1.6
Pulse Width (ns)	500	212	185	350.	321	500	189	171	316	296	500	141	136	231	227
Tr (ns)	84	85	66	84	64	75	73	60	73	60	55	46	41	45	40
Tf (ns)	9	18	21	17	19	8	14	14	14	15	6	8	9	8	9
Td (ns)		62	52	61	53		55	47	55	45		41	34	41	34
Min. Pulse Width,C=0		79	38				61	36				41	31		

Temperature	85°C					125°C				
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf	
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$
Pulse Amplitude (Vpp)	1.7	1.5	1.4	1.5	1.5	1.6	1.4	1.4	1.4	1.4
Pulse Width (ns)	500	109	110	180	183	500	94	102	153	160
Tr (ns)	77	42	37	43	41	95	42	49	43	49
Tf (ns)	6	7	7	7	7	7.	8	8	7	8
Td (ns)		41	32	41	32		43	32	43	33
Min. Pulse Width,C=0		37	34				39	42		

The input pulse width ($\overline{T}$) can be varied without affecting the pulse widths of the outputs. This was verified for pulse widths varying from 100 to 900 ns.

Circuit Designation A08				Fan-out 1		Vcc 5.0v		Pulse Rep. Rate 1MC							
Temperature	-55°C					-40°C					25°C				
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf	
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$
Pulse Amplitude (Vpp)	2.1	1.9	1.9	1.9	1.9	2.0	1.9	1.9	1.9	1.9	1.9	1.8	1.8	1.8	1.8
Pulse Width (ns)	500	143	138	227	220	500	128	124	210	205	500	99	99	166	166
Tr (ns)	46	39	34	39	34	42	37	32	36	32	43	31	28	31	32
Tf (ns)	5	7	8	7	8	5	7	7	7	7	4	6	6	6	6
Td (ns)		36	29	36	29		35	28	34	28		32	26	33	26
Min. Pulse Width, C=0		39	29				38	29				32	29		

Temperature	85°C					125°C				
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf	
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$
Pulse Amplitude (Vpp)	1.8	1.6	1.6	1.6	1.6	1.7	1.5	1.5	1.5	1.5
Pulse Width (ns)	500	87	91	142	146	500	79	89	124	134
Tr (ns)	67	32	25	33	29	95	40	42	43	44
Tf (ns)	5	6	6	6	6	7	8	9	6	9
Td (ns)		36	28	36	28		43	32	44	32
Min. Pulse Width, C=0		35	35				39	44		

The input pulse width ($\overline{T}$) can be varied without affecting the pulse widths of the outputs. This was verified for input pulse widths ranging from 100 to 900 ns.

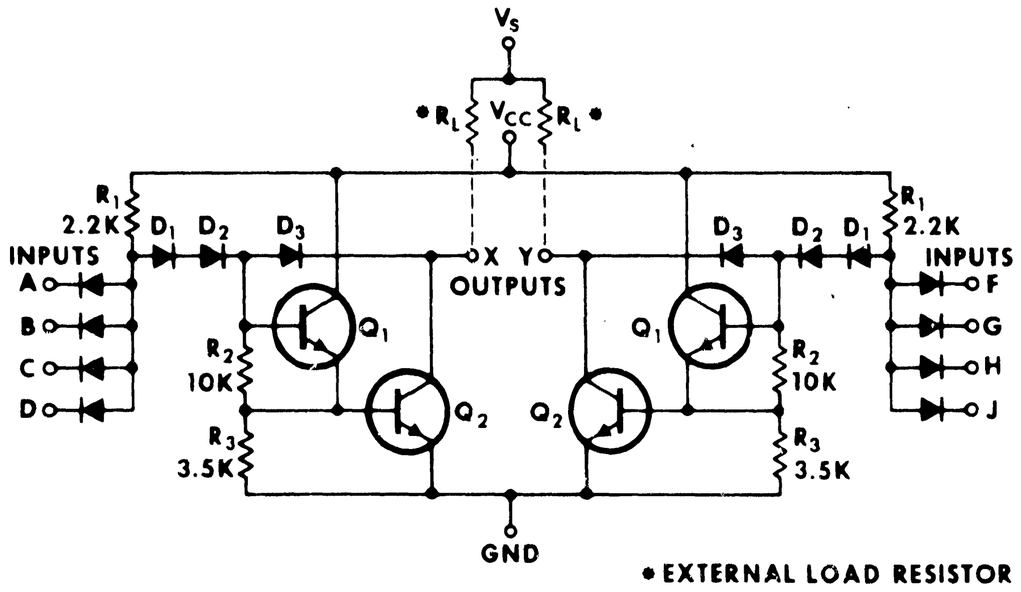
Circuit Designation A08						Fan-out 1					Vcc 6.0					Pulse Rep. Rate 1MC				
Temperature	-55°C					-40°C					25°C									
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf						
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$					
Pulse Amplitude (Vpp)	2.2	2.0	2.0	2.0	2.0	2.0	1.9	1.9	2.0	2.0	2.0	1.9	1.9	1.9	1.9					
Pulse Width (ns)	500	103	101	178	174	500	96	96	161	160	500	84	89	139	141					
Tr (ns)	32	27	23	27	23	30	27	21	26	24	47	25	21	25	24					
Tf (ns)	4	6	6	6	6	3	5	5	5	5	4	5	5	5	5					
Td (ns)		29	23	29	23		28	23	28	23		29	23	29	23					
Min. Pulse Width, C=0		30	27				30	27				29	29							
Temperature	85°C					125°C														
Test Circuit:	Input $\overline{T}$	C=113pf		C=226pf		Input $\overline{T}$	C=113pf		C=226pf											
		Q	$\overline{Q}$	Q	$\overline{Q}$		Q	$\overline{Q}$	Q	$\overline{Q}$										
Pulse Amplitude (Vpp)	1.9	1.7	1.8	1.7	1.8	1.8	1.5	1.6	1.6	1.6										
Pulse Width (ns)	500	75	82	120	126	500	70	78	105	117										
Tr (ns)	59	32	25	32	26	99	39	42	47	42										
Tf (ns)	5	6	8	5	7	7	9	10	6	10										
Td (ns)		37	29	38	30		51	41	52	41										
Min. Pulse Width, C=0		36	38				41	47												

The input pulse width ($\overline{T}$) can be varied without affecting the pulse widths of the outputs. This was verified for input pulse widths ranging from 100 to 900 ns.

1. A20 Dual NAND/NOR Gate Equivalent Circuit

2. Siliconix Test Circuits and Waveform Definitions

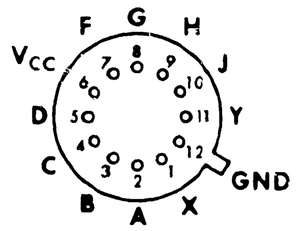
CIRCUIT DIAGRAM



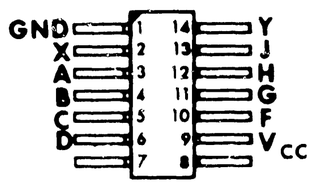
A20 Dual NAND/NOR Gate
UNIFET Commutator Driver and Buffer

Figure 3.1.35

PIN DIAGRAMS

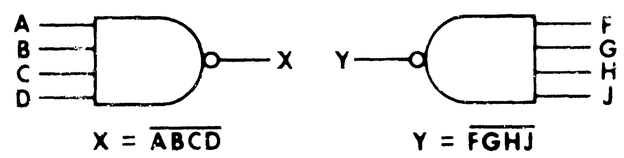


Modified TO-5



FlatPac

LOGIC DIAGRAMS

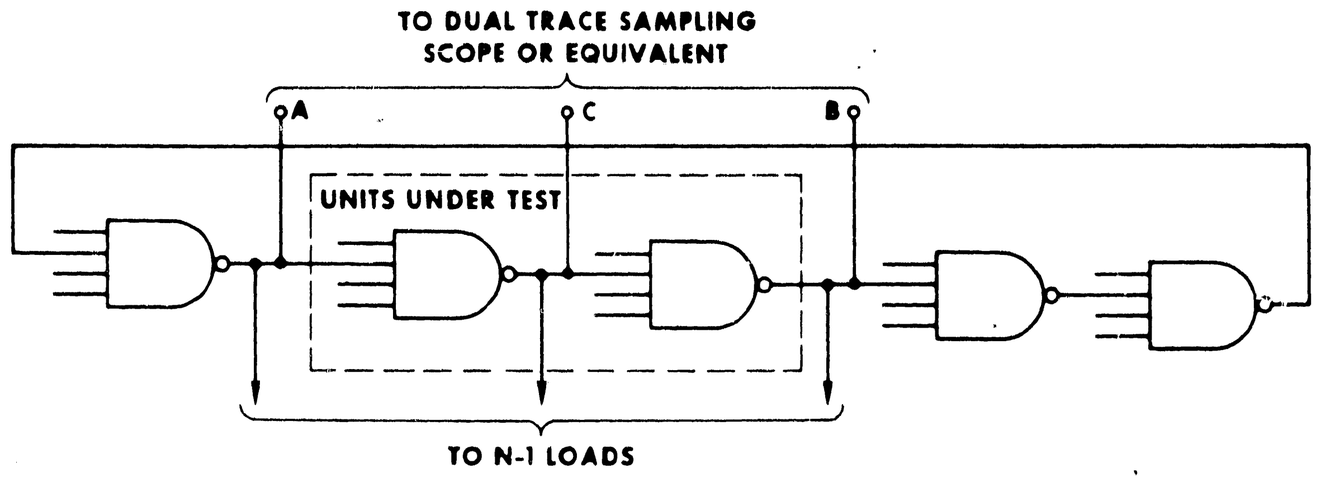


ABSOLUTE MAXIMUM RATINGS AT 25°C

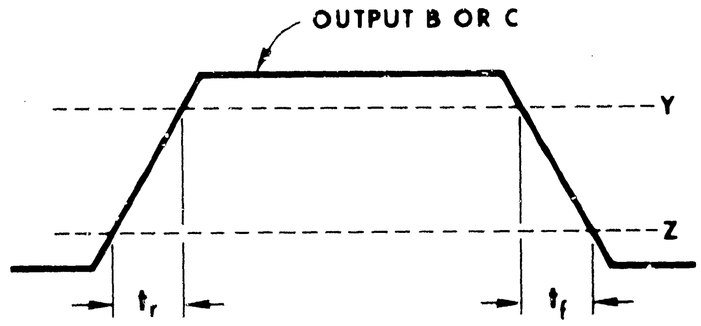
External Source Voltage V_S . . . . . 18 v
Circuit Power Supply Voltage V_{CC} . . . . . 6 v
Input Voltage BV_i . . . . . 6 v
Output Voltage BV_{CEX} at 1 μa . . . . . 18 v
Sustaining Output Voltage LV_{CEX} at 1 ma . . . . . 18 v
Operating Temperature Range T_A . . . . . -55 to +125°C
Storage Temperature Range T_S . . . . . -65 to +150°C
Output Current . . . . . 35 ma

Voltage at any pin must be positive with respect to the common terminal.

This circuit was not tested because of its similarity with the A02 Dual NAND/NOR Gate.

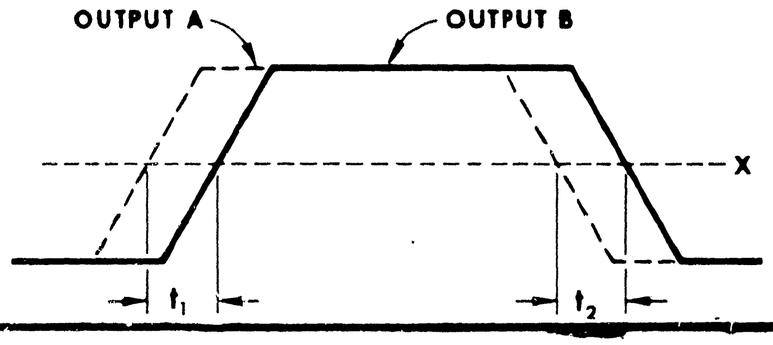


Rise time t_r and fall time t_f
When an internal or external load resistor is connected to a gate, the Y level of the output voltage waveform will be 4.0 volts for rise- and fall-time measurements.

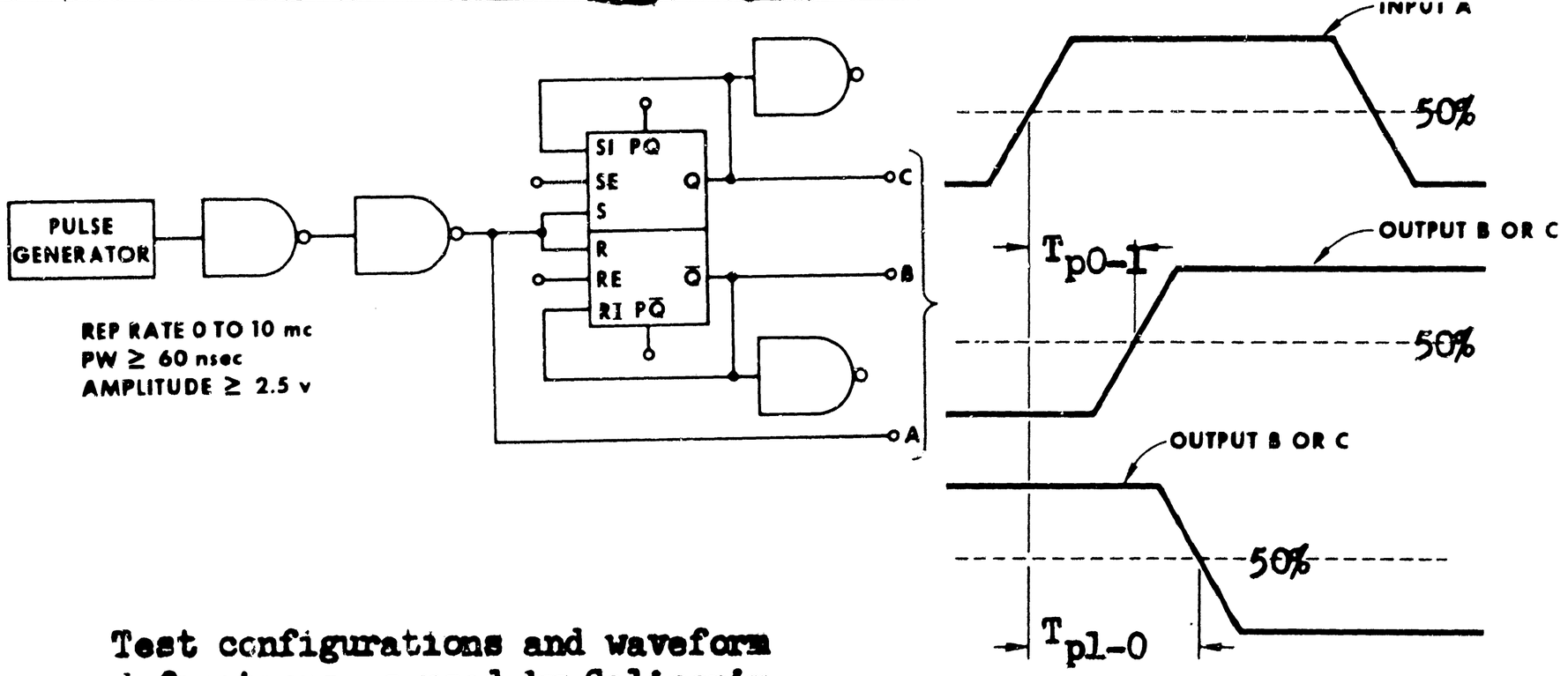


LEVEL	TEMP—°C		
	-55	+25	+125
Y	2.5 v	2.0 v	1.6 v
Z	1.4 v	1.1 v	0.9 v

$$t_p = \frac{t_1 + t_2}{4}$$



LEVEL	TEMP—°C		
	-55	+25	+125
X	2.0 v	1.6 v	1.3 v



Test configurations and waveform definitions as used by Siliconix.

Figure 3.1.36

NOTES #9.3.2

EVALUATION OF GENERAL MICRO-ELECTRONICS FUNCTIONAL DEVICES

TABLE OF CONTENTS

	Page
Circuit List	3.2.1
Waveform Definitions	3.2.2, 3.2.3
Equipment List	3.2.4
RTL Line (Low Power) General Information	3.2.5
G Element	3.2.7
E Element	3.2.32
D_2 Element	3.2.34
D_3 Element	3.2.39
B Element	3.2.44
H Element	3.2.59
A Element	3.2.66
R Element	3.2.83
RTL Line (Hi Power) $153D_3$ Dual Gate	3.2.87
DTL Line - General Information	3.2.92
$254G_4$ Gate	3.2.94
264P Gate	3.2.110
$264D_2$ Dual Gate	3.2.117
$254G_6$ Gate	3.2.123
$254D_3$ Dual Gate	3.2.125
CML Line - General Information	3.2.140
$543G_5$ Gate	3.2.142
TTL Line - General Information	3.2.155
$365D_4$ - Dual Gate	3.2.156
$365G_8$ - Gate	3.2.164

CIRCUITS WHICH COMPRISE GENERAL MICROELECTRONICS LINE

Low-Power RTL

1. G, 4 input OR/NOR Gate
2. D_2, Dual 2 input NOR Gate
3. D_3, Dual 3 input NOR Gate
4. E, Dual 2 input Expander Gate
5. B, 2 input Buffer Element
6. H, Exclusive or Element, Half Adder
7. A, Adder Element
8. R, Register Element

High-Power RTL

1. Dual 3 input NOR Gate

CML

1. 543G5 5 input OR/NOR Gate

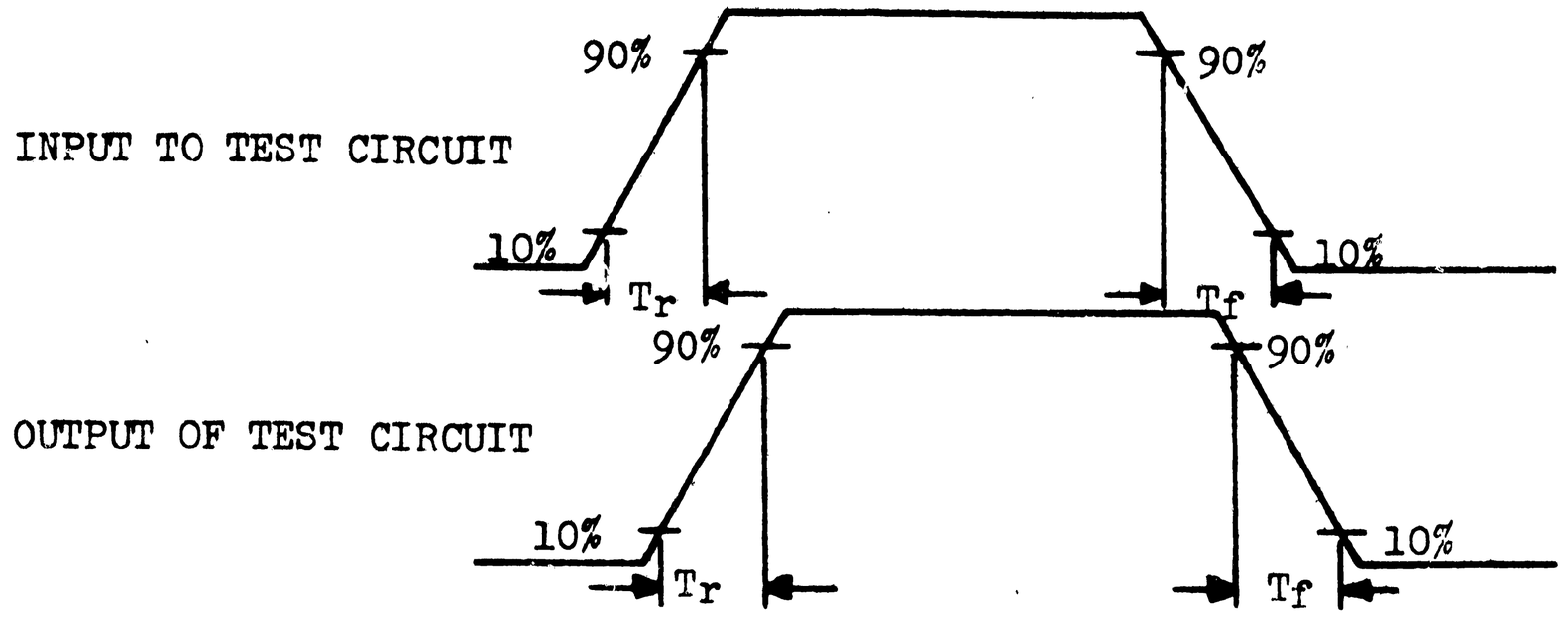
TTL

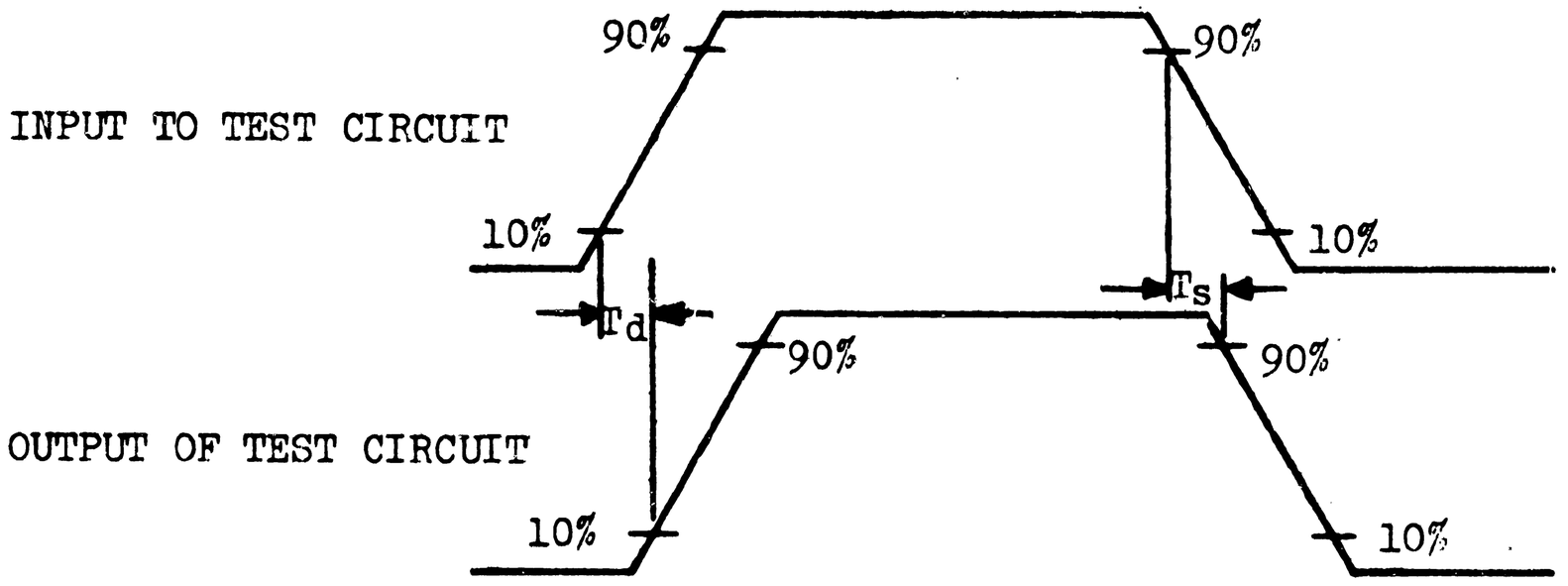
1. 365D4 Dual 4 input Gate
2. 365G8 8 input Gate

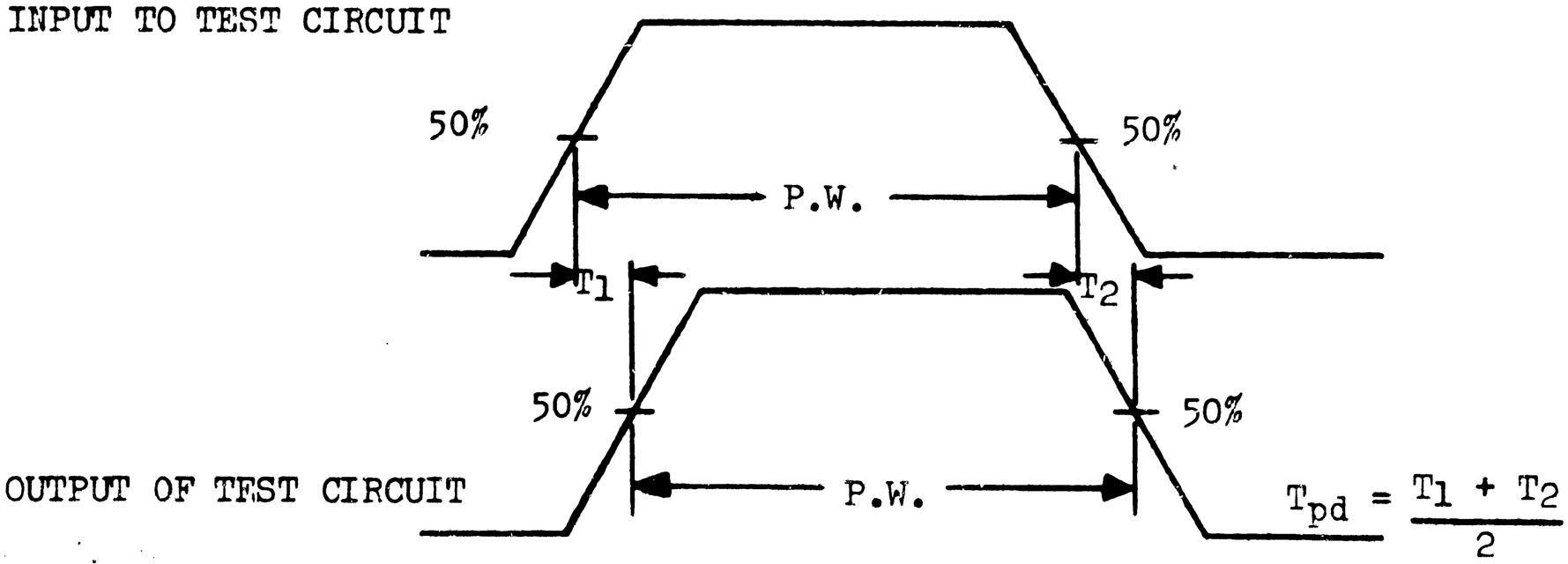
DTL

1. 254G4 4 input NOR Gate
2. 254G3 3 input NOR Gate
3. 254G6 6 input Diode and Gate
4. 254P 3 input Power Gate
5. 264D_2 Dual 2 input Gate
6. 264B Binary Element
7. 254D_3 Dual 3 input Diode and Gate

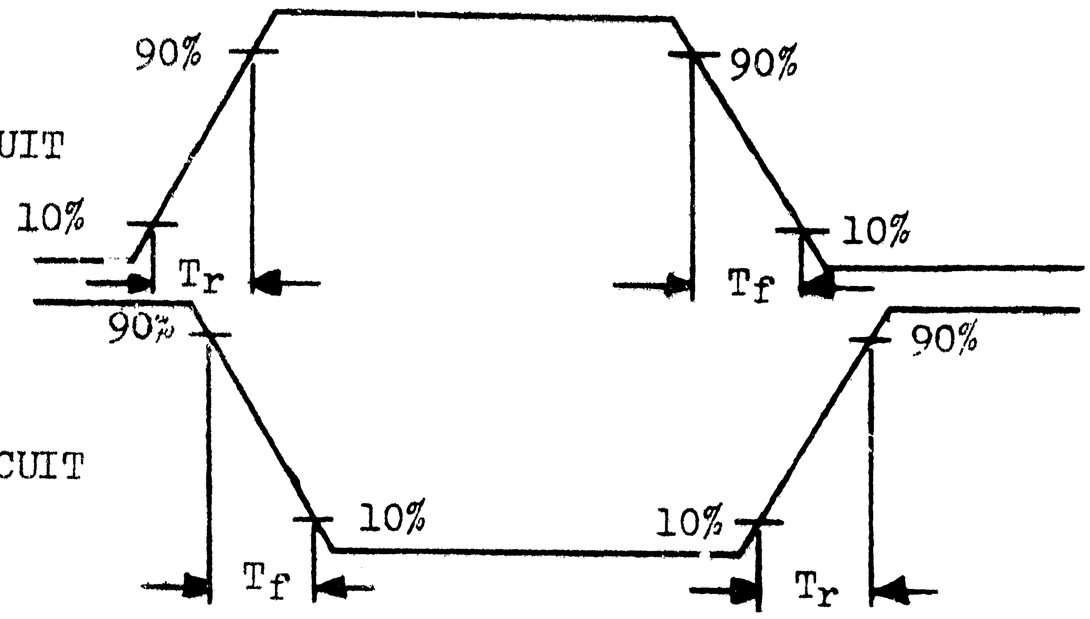
WAVEFORM DESCRIPTION AND TIME MEASUREMENT DEFINITION FOR A POSITIVE INPUT WAVE AND A POSITIVE OUTPUT WAVE

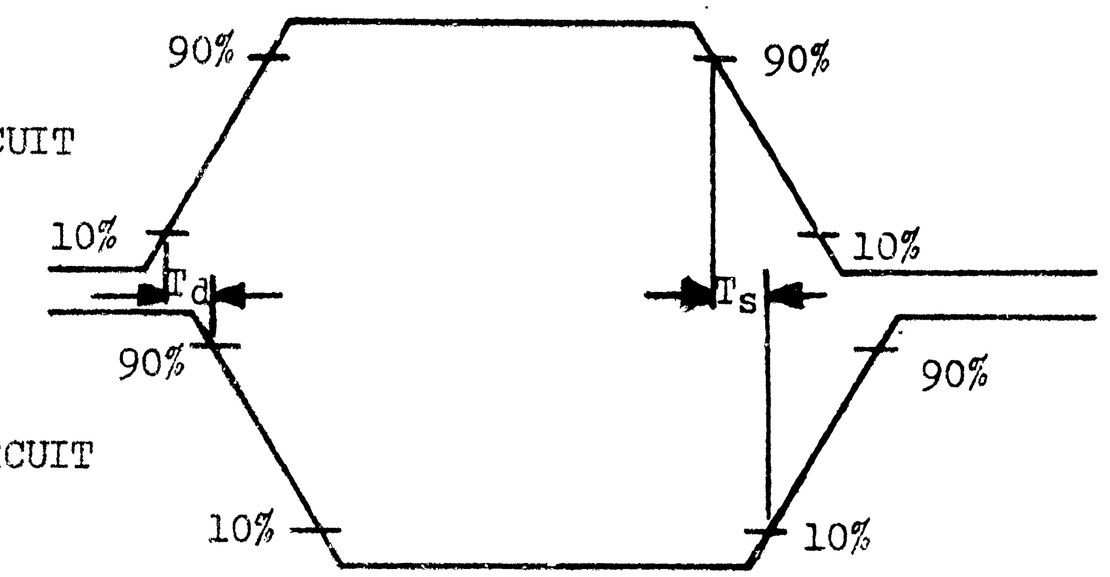


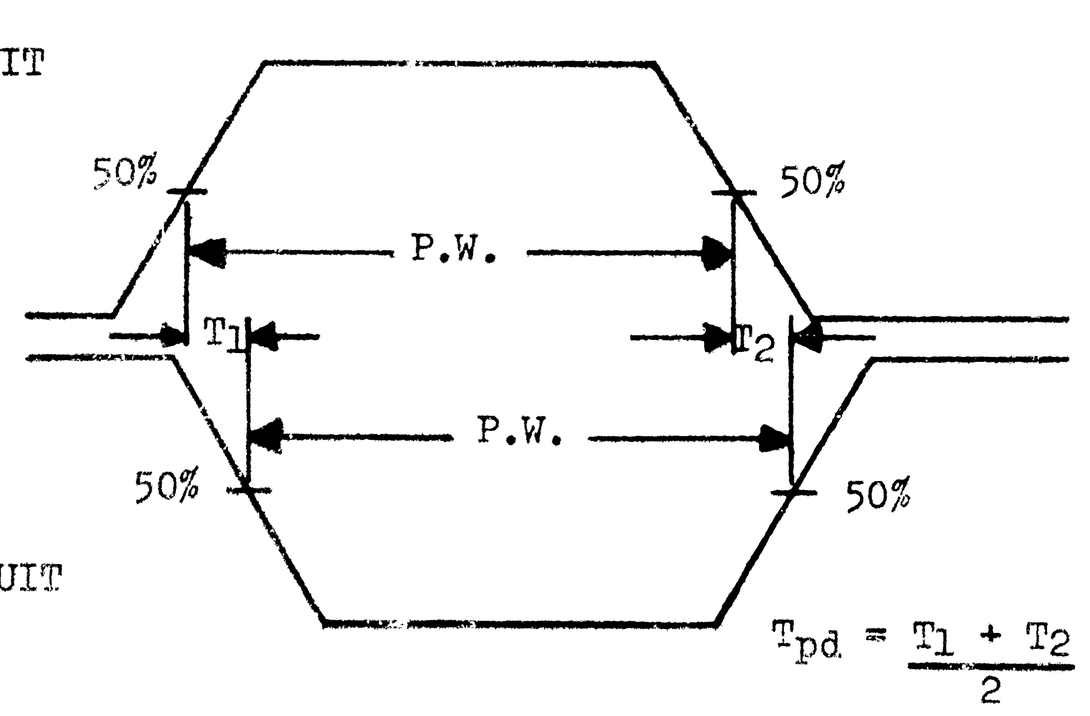




WAVEFORM DESCRIPTION AND TIME MEASUREMENT DEFINITION FOR A POSITIVE INPUT WAVE AND A NEGATIVE OUTPUT WAVE







EQUIPMENT LIST FOR EVALUATION OF GENERAL MICROELECTRONIC

1. Oscilloscope:

   Tektronix, Model 567 with: 3S76 Sampling dual trace
   3T77 Sampling Sweep
   6R1 Digital plug-in units
   P6032 Probes

2. Pulse Generators:

   Texas Instruments, Model 6611
   Texas Instruments, Model 6303

3. Power Supplies:

   Trygon Model HR40-750
   Harrison Laboratories, Model 802B
   Harrison Laboratories, Model 6204A

4. Transistor Curve Tracer:

   Tektronix, Model 575

5. Voltmeter:

   Hewlett Packard, Model 412A

6. Temperature Chamber:

   Stratham, Model SD-6

EVALUATION

The General Microelectronic RTL line is a series of monolithic, planar, epitaxial devices which are packaged in a flat pack or TO-5 can. The family consists of the following elements:

G, D_2, D_3	Basic NAND Gates
$153D_3$	A basic higher power NAND Gate
E	Contains 2 sets of 2 input transistors used to extend the fan-in of the basic gates
B	Primarily a driver circuit to extend the fan-out capabilities of the basic gates
A	Provides the sum and carry outputs for two inputs to be added
H	Generates an exclusive OR function
R	Functions as a shift register or delay flip-flop

The circuits were tested on a transistor curve tracer to obtain demonstrative circuit static characteristics. The only circuit not tested statically was the R element due to the nature of the time spacing requirements between the clock and the data inputs.

The same circuits used to obtain the static curves were tested dynamically and only representative circuits were tested. The G element, for instance, gives a good indication of the performance of the D_2, D_3, and $153D_3$. The Buffer Element was tested because of the additional circuitry to obtain the high output drive. The A element should give a performance profile of the H element also. The R element was tested dynamically because of its unique circuit function.

DYNAMIC TEST PROCEDURE:

1. The block diagram for each circuit is given preceeding the data for that circuit.

2. The load supply was held constant at the manufacturers rated for all tests.

3. The temperature was regulated at 25°C.

4. The test circuit supply was set at 2.0 volts, the frequency at 1MC and the pulse width to the test circuit at 500 ns and load of 1.

5. The supply was increased to 3.0 with all else constant. Data and a picture were taken.

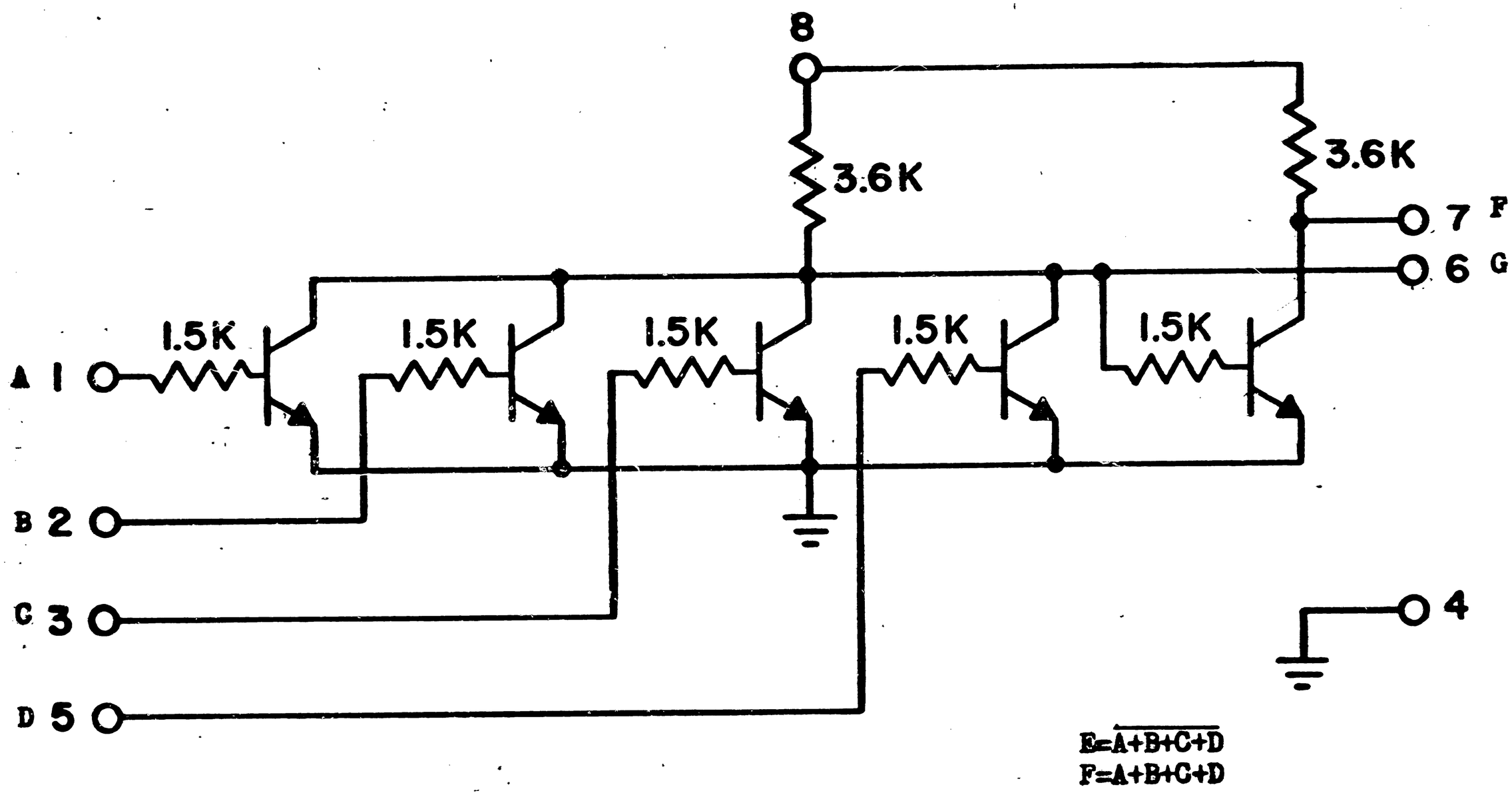
6. The Supply was increased to 4.0 volts and full data was again taken.

7. The above procedure from 2 to 6 was repeated at -40°C, -55°C, +85°C, +125°C.

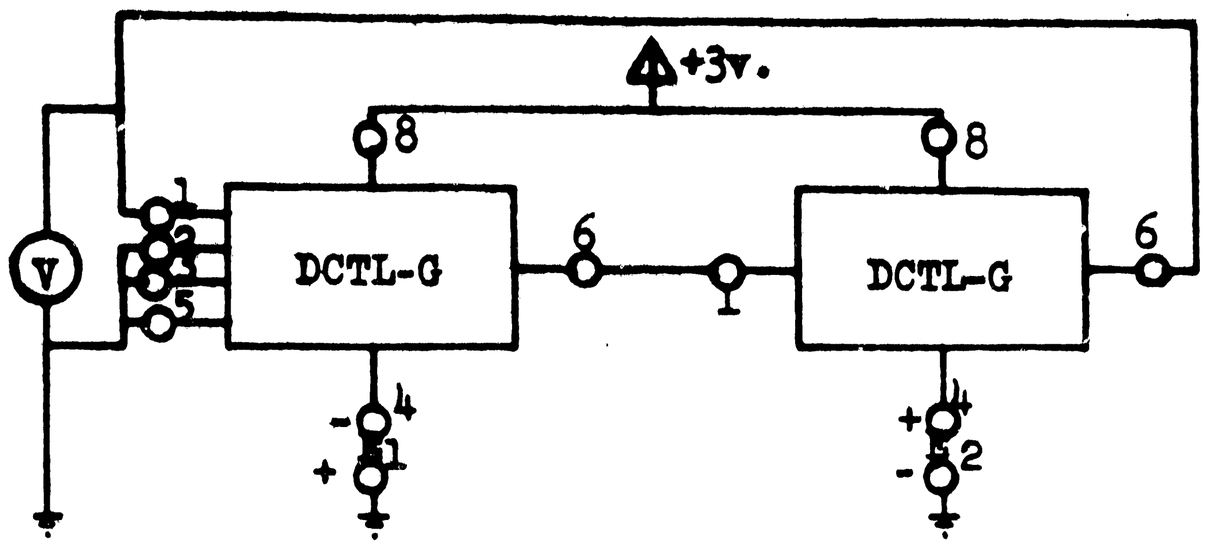
8. The procedure from 2 to 7 was repeated for loads of 3 and 5.

9. In the case of the buffer the load values were 2, 6 and 10.

10. The test procedure for the R element is included with the data.



4 - INPUT DCTL GATE ELEMENT, G



NOISE TEST

Procedure:

1. The circuits were connected as in the above block diagram.
2. E_2 was replaced by a short.
3. E_1 was increased until V indicated a change of state.
4. The system was reset by disconnecting the negative terminal of E_1 which set V to zero.
5. E_1 was replaced by a short.
6. E_2 was increased until V indicated a change of state.
7. The system was reset by disconnecting E_1's short which set V to zero.

Data:

The average of five test runs was:

E_1 at system change of state -0.596

E_2 at system change of state +0.603

The noise margin of the DCTL elements used was 0.596v.

Equipment:

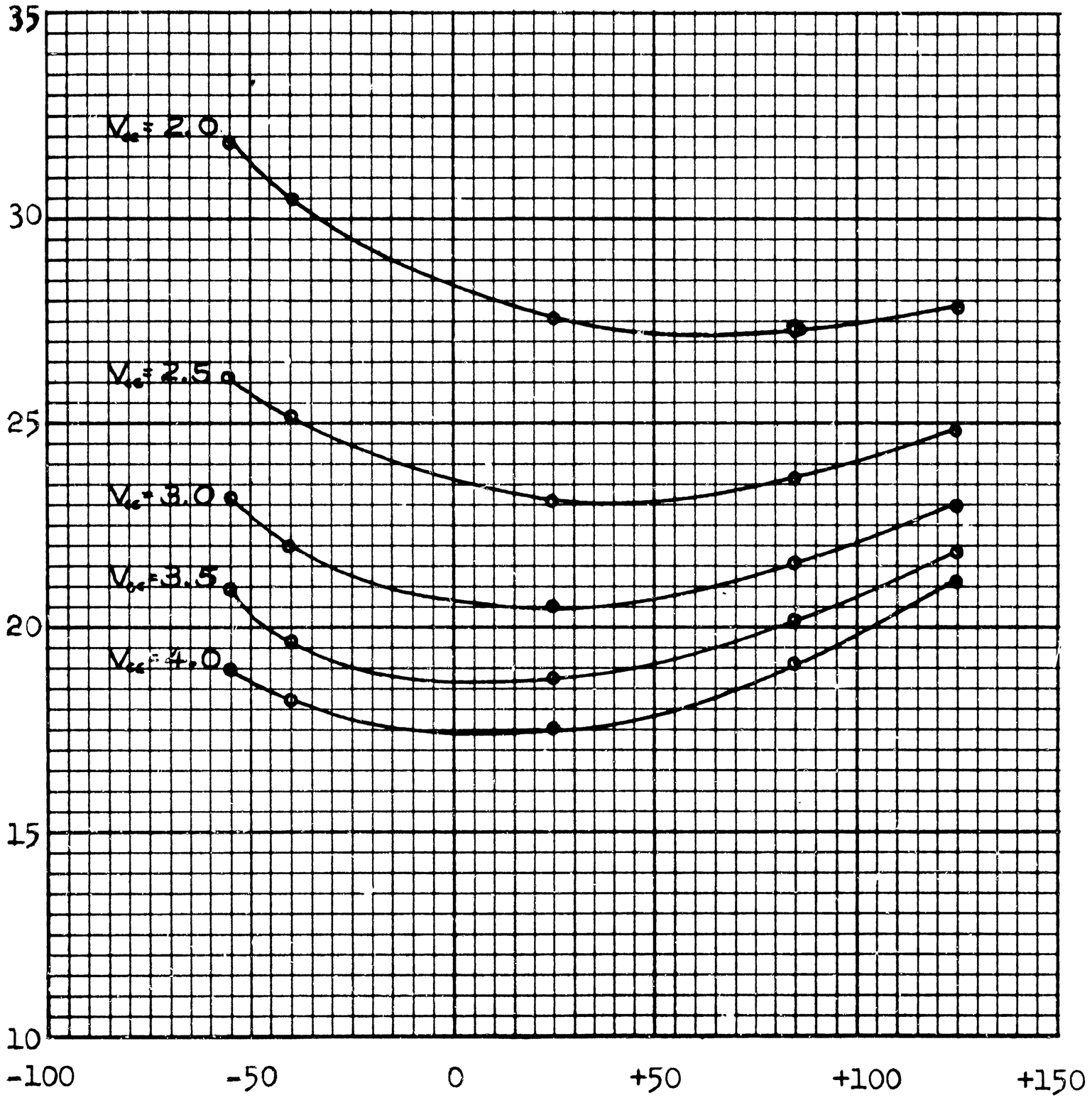
Voltmeter; Hewlett Packard, Model 412A
Power supply; Trygon Electronics, Model HR40-750
E_1 and E_2; Harrison Laboratories, Model 6204A

TEMP.-^{O}C	V_{cc}-VOLTS	PERIOD-NS	AMPL.-VOLTS	T_{pd}-NS
-55	2.0	446	0.94	31.8
	2.5	365	1.02	26.1
	3.0	323	1.11	23.1
	3.5	291	1.20	20.8
	4.0	264	1.30	18.9
-40	2.0	427	0.91	30.5
	2.5	353	1.00	25.2
	3.0	308	1.08	22.0
	3.5	275	1.19	19.6
	4.0	253	1.28	18.1
+25	2.0	387	0.80	27.6
	2.5	325	0.90	23.2
	3.0	287	1.00	20.5
	3.5	262	1.10	18.7
	4.0	245	1.20	17.5
+85	2.0	383	0.70	27.3
	2.5	332	0.78	23.7
	3.0	302	0.84	21.6
	3.5	282	0.92	20.2
	4.0	269	1.00	19.2
+125	2.0	389	0.64	27.8
	2.5	347	0.74	24.8
	3.0	322	0.84	23.0
	3.5	306	0.93	21.8
	4.0	297	1.02	21.2

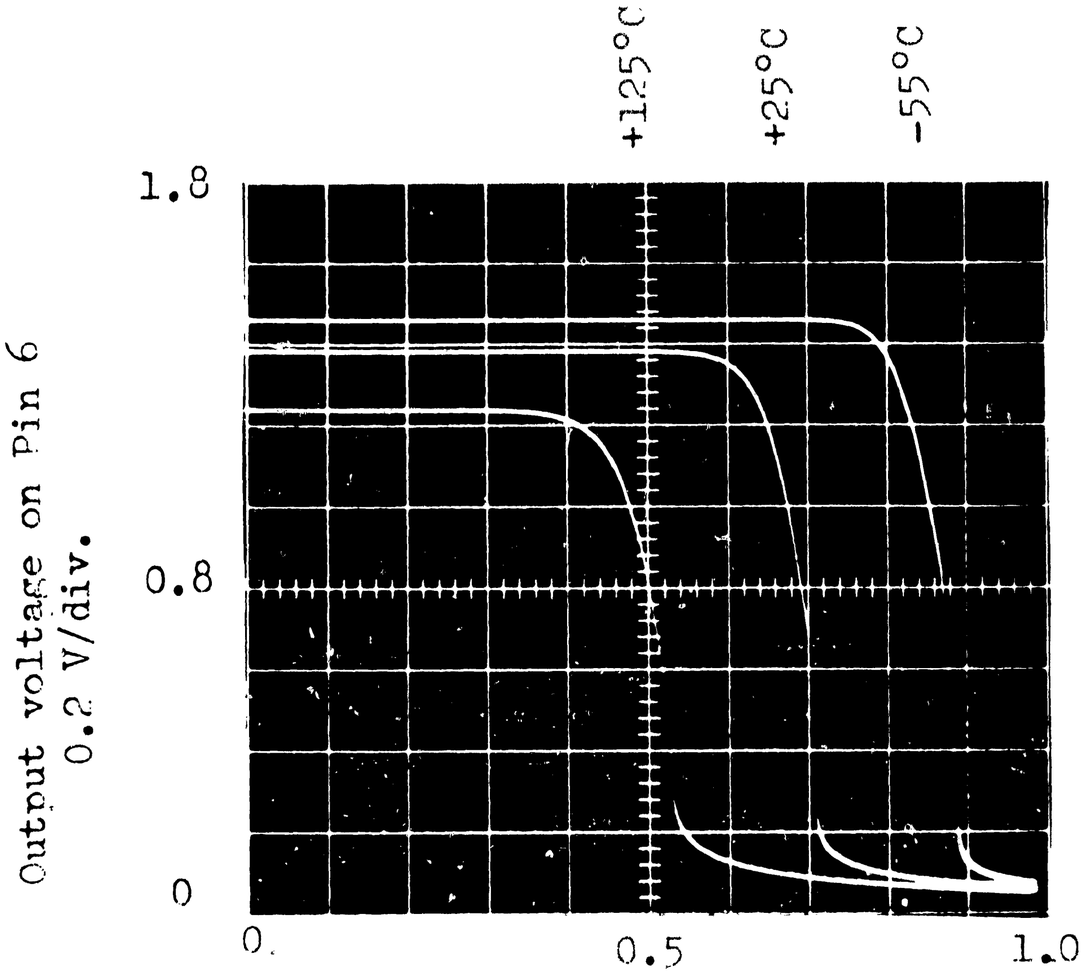
TABLE FOR PROPAGATION DELAY VERSUS TEMPERATURE CURVES

DCTL - G ELEMENT

PROPAGATION DELAY versus TEMPERATURE

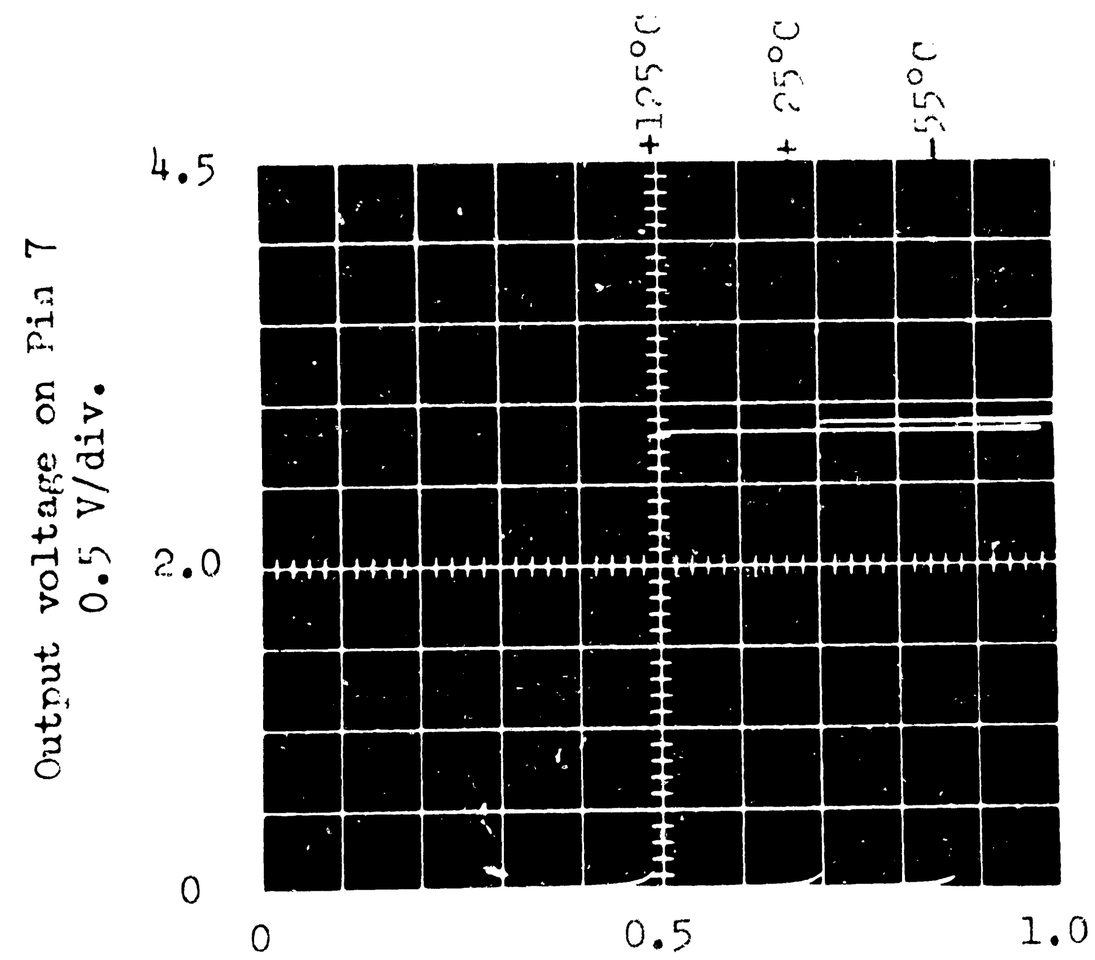


TEST CONDITIONS: Seven Low Power RTL G elements connected in a ring oscillator with a variable common supply voltage.



V_{cc} = 3.0

0.1 V/div.
Input Voltage on Pin 1

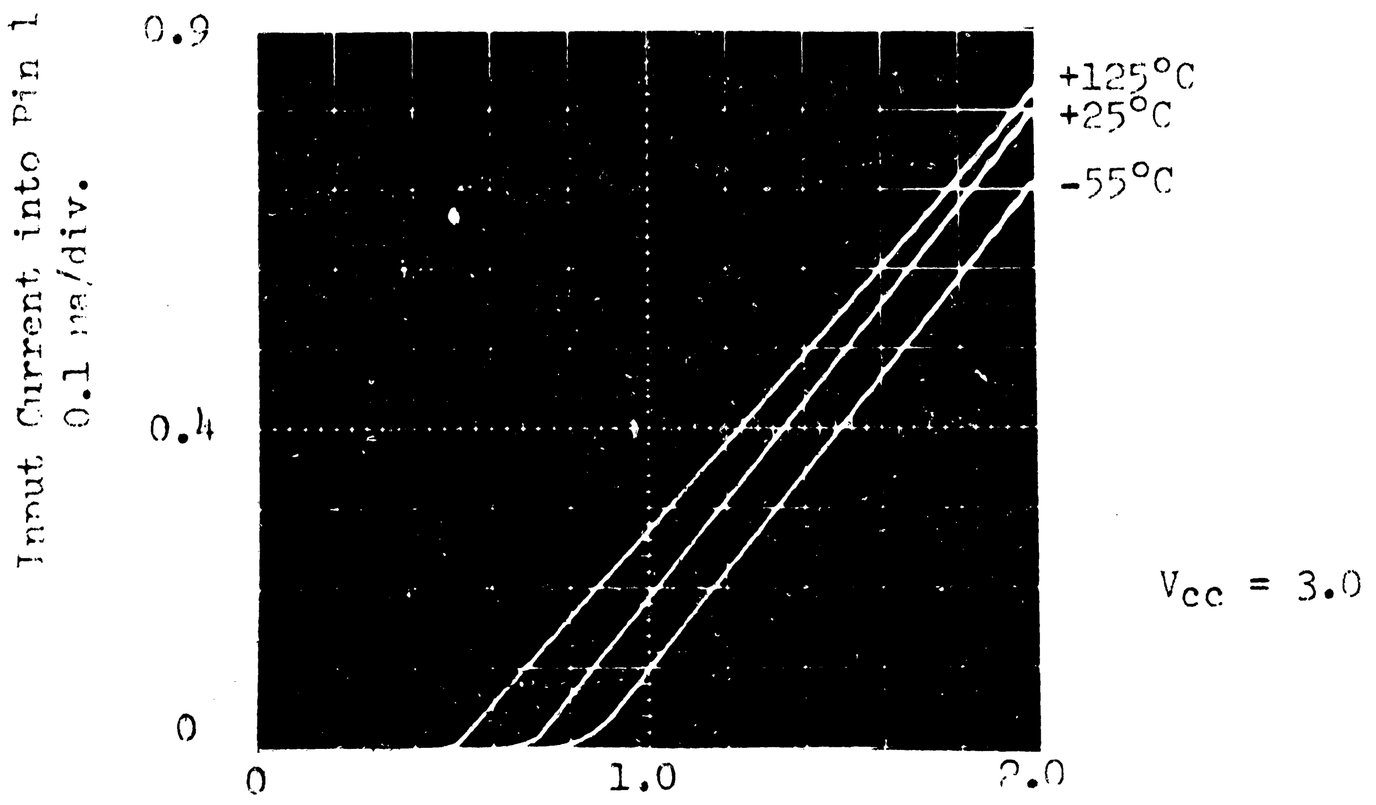


V_{cc} = 3.0

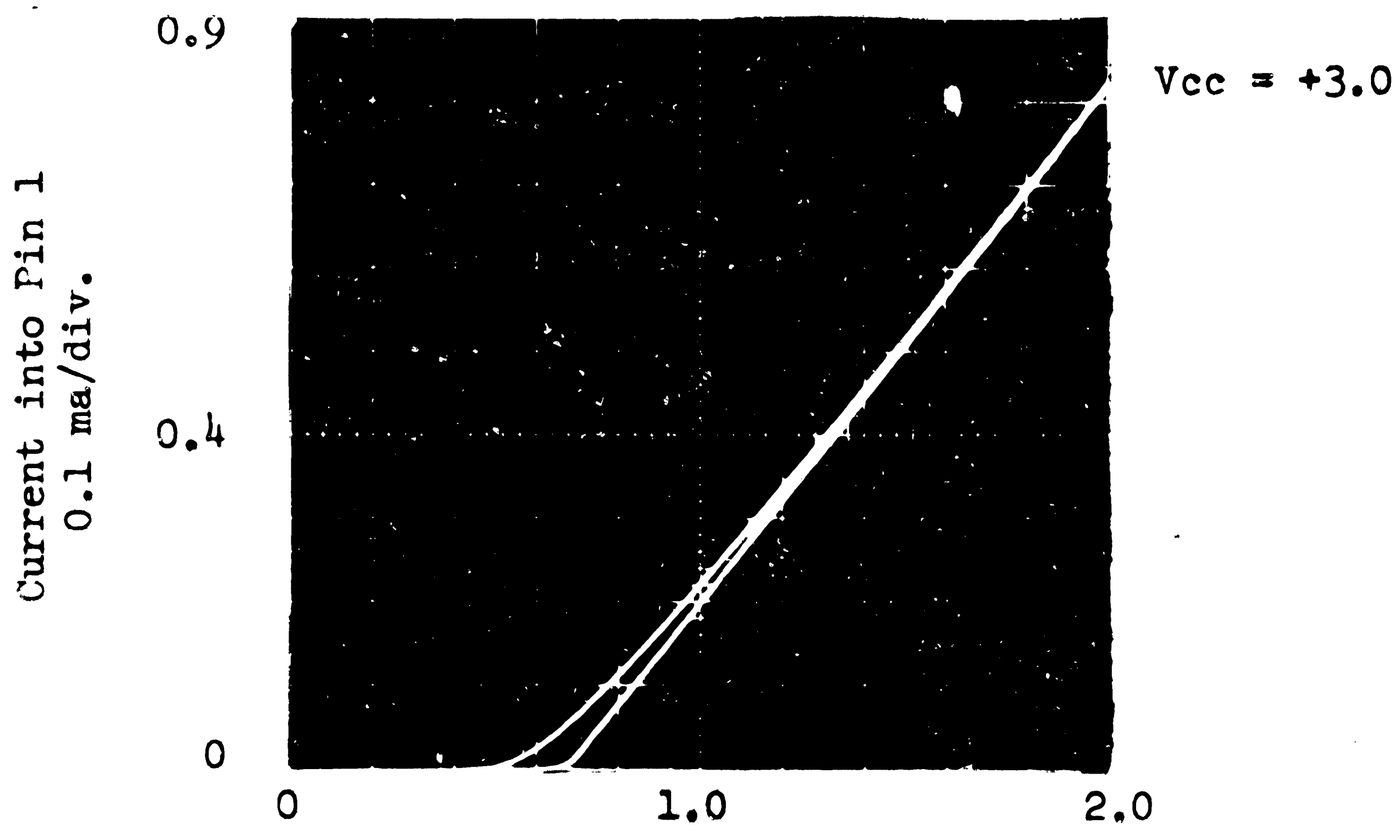
0.1 V/div.
Input Voltage on Pin 1

INPUT OUTPUT CHARACTERISTICS
DCTL G ELEMENT

3.2.11

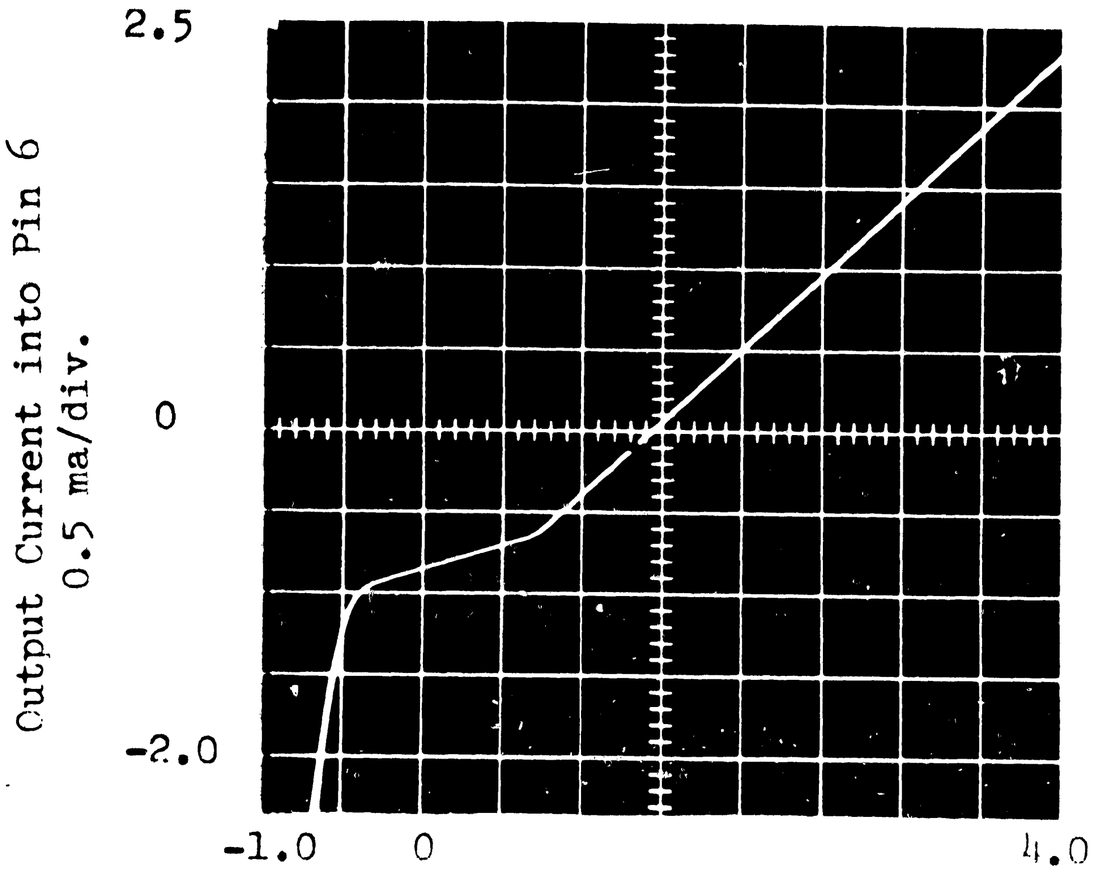


INPUT CHARACTERISTICS
DCTL G ELEMENT

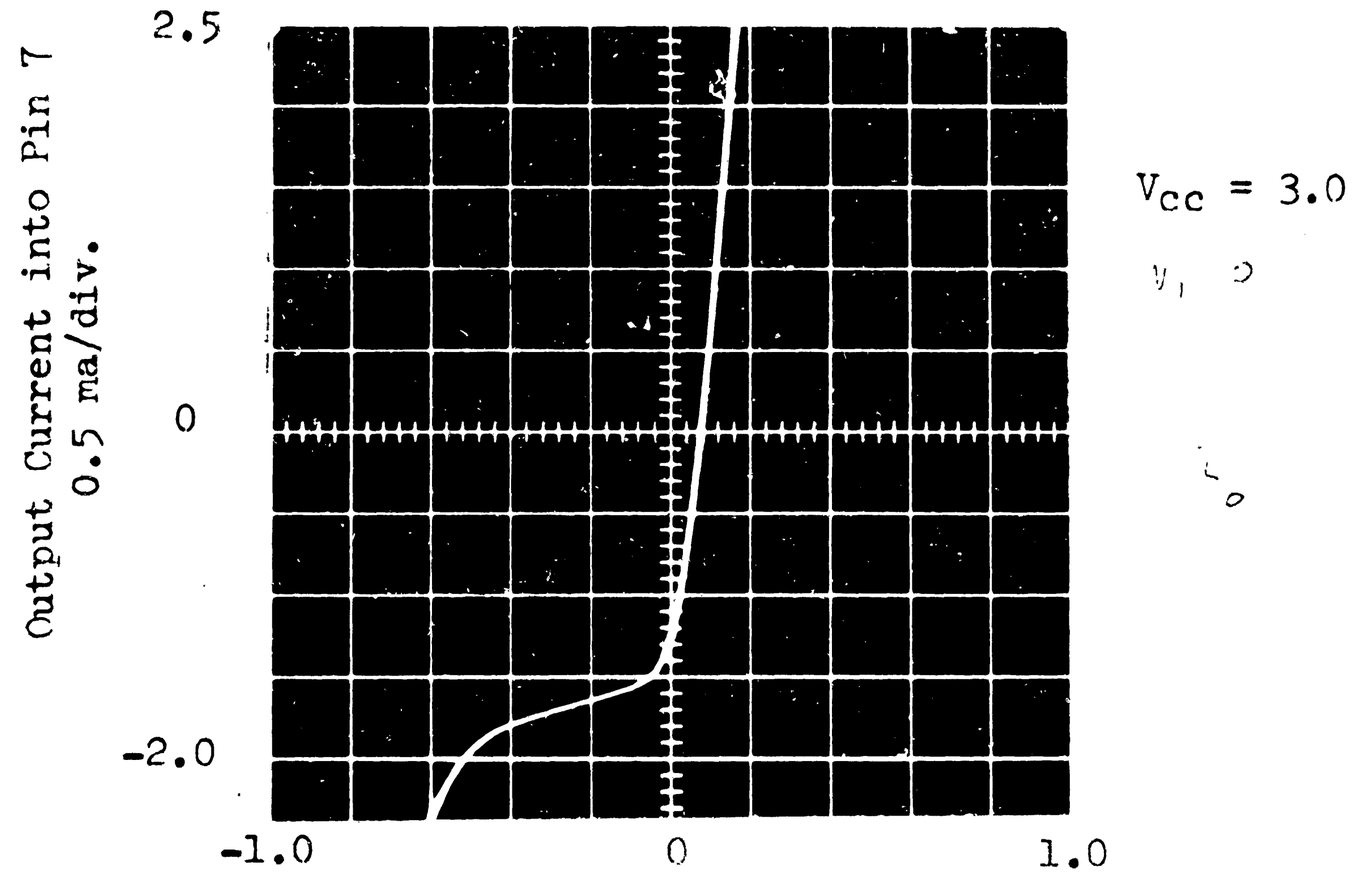


NOTE: Bottom curve is with pins 2, 3, and 5 open.
Top curve is with pins 2, 3 and 5 at +3.0

INPUT CHARACTERISTICS
DCTL G ELEMENT

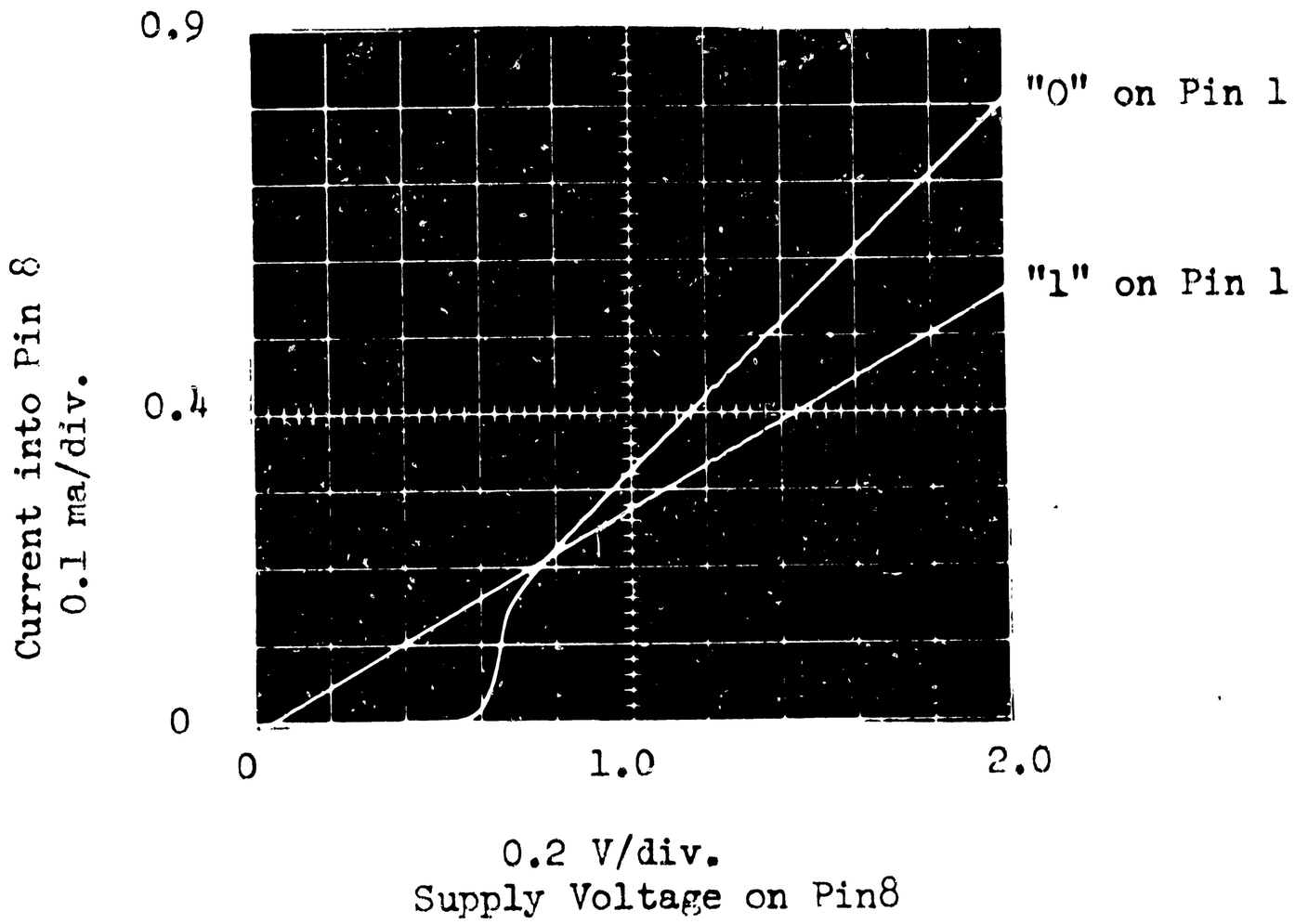


0.5 V/div.
Output Voltage on Pin 6

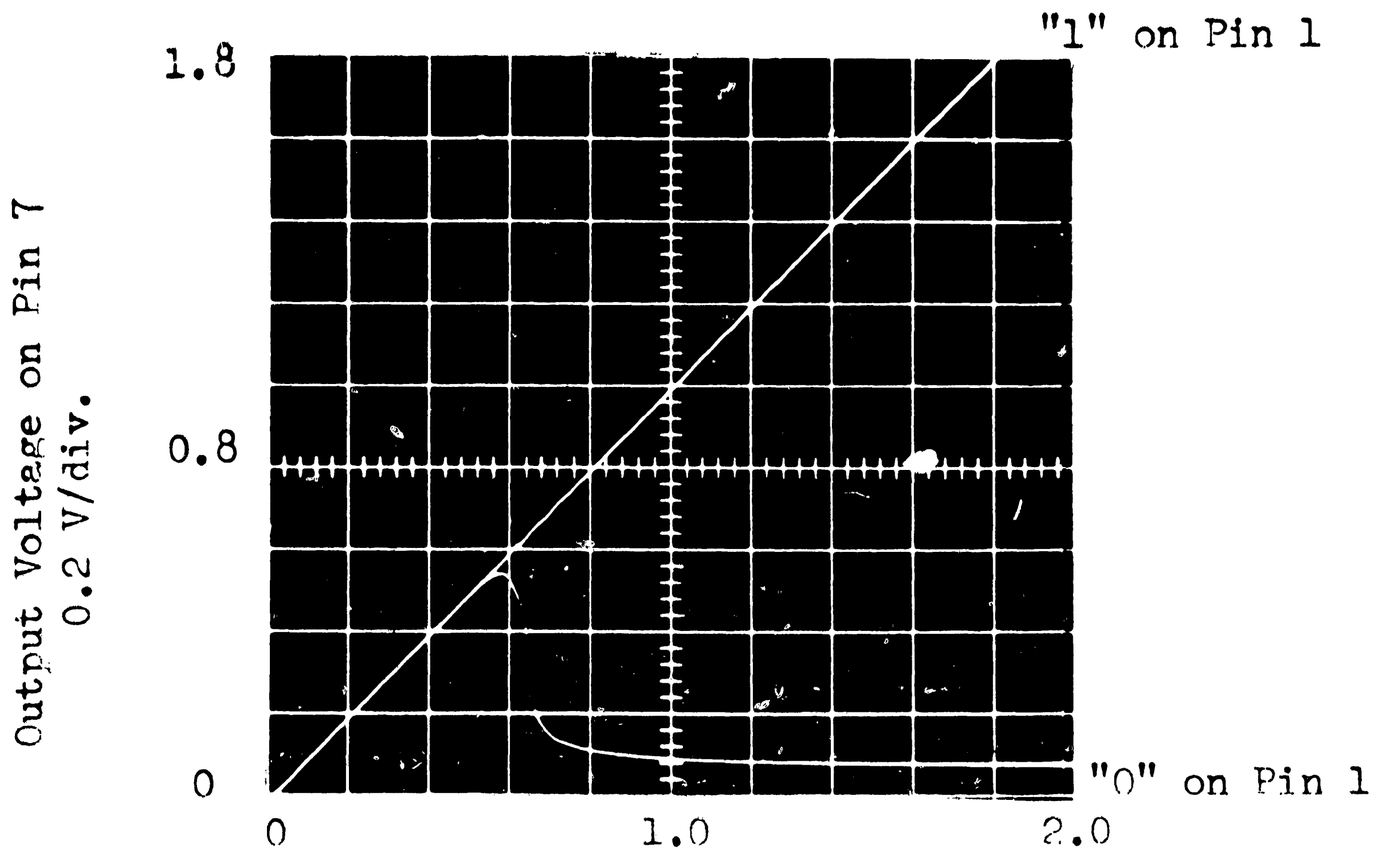


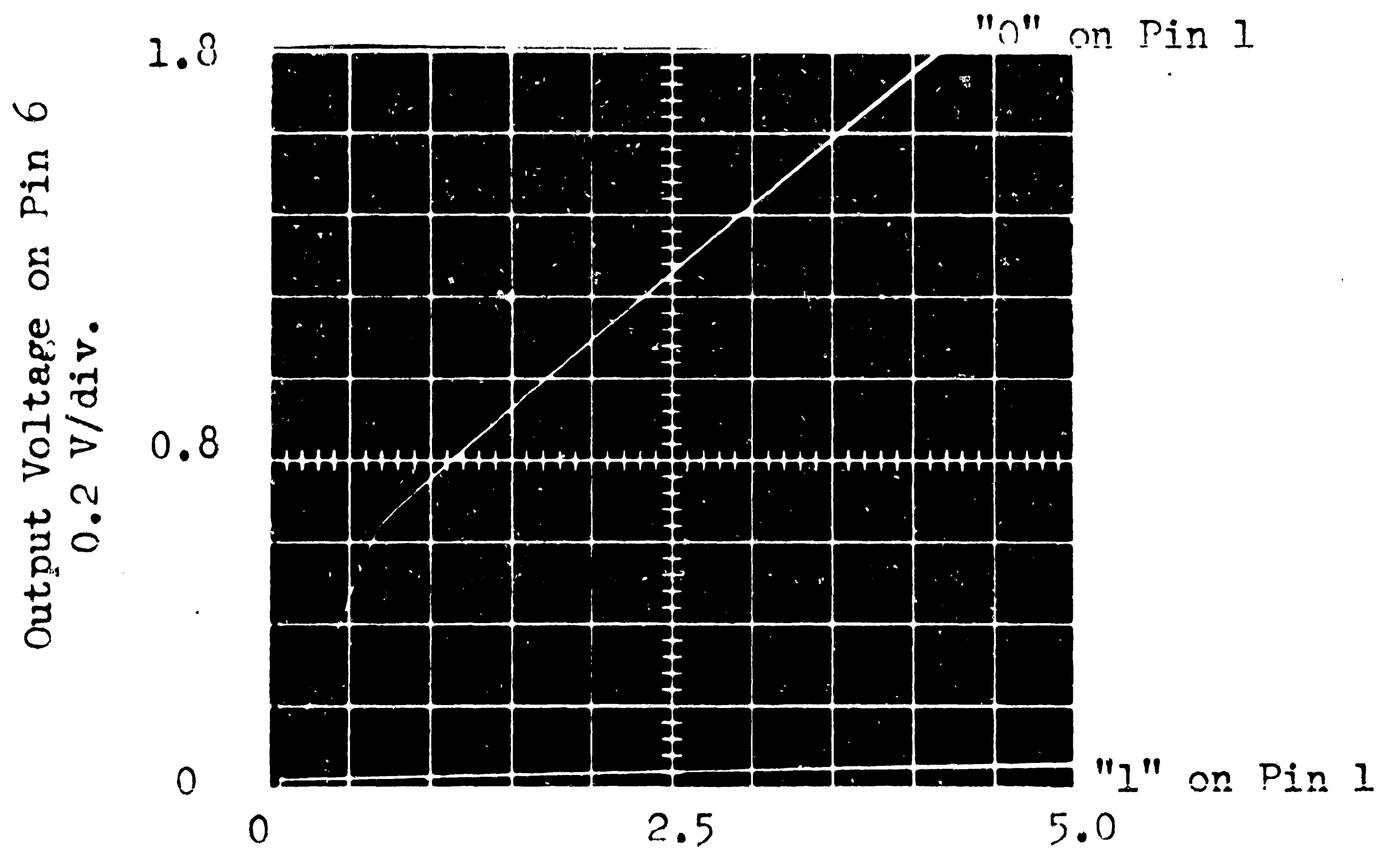
0.2 V/div.
Output Voltage on Pin 7

OUTPUT CHARACTERISTICS
DCTL G ELEMENT

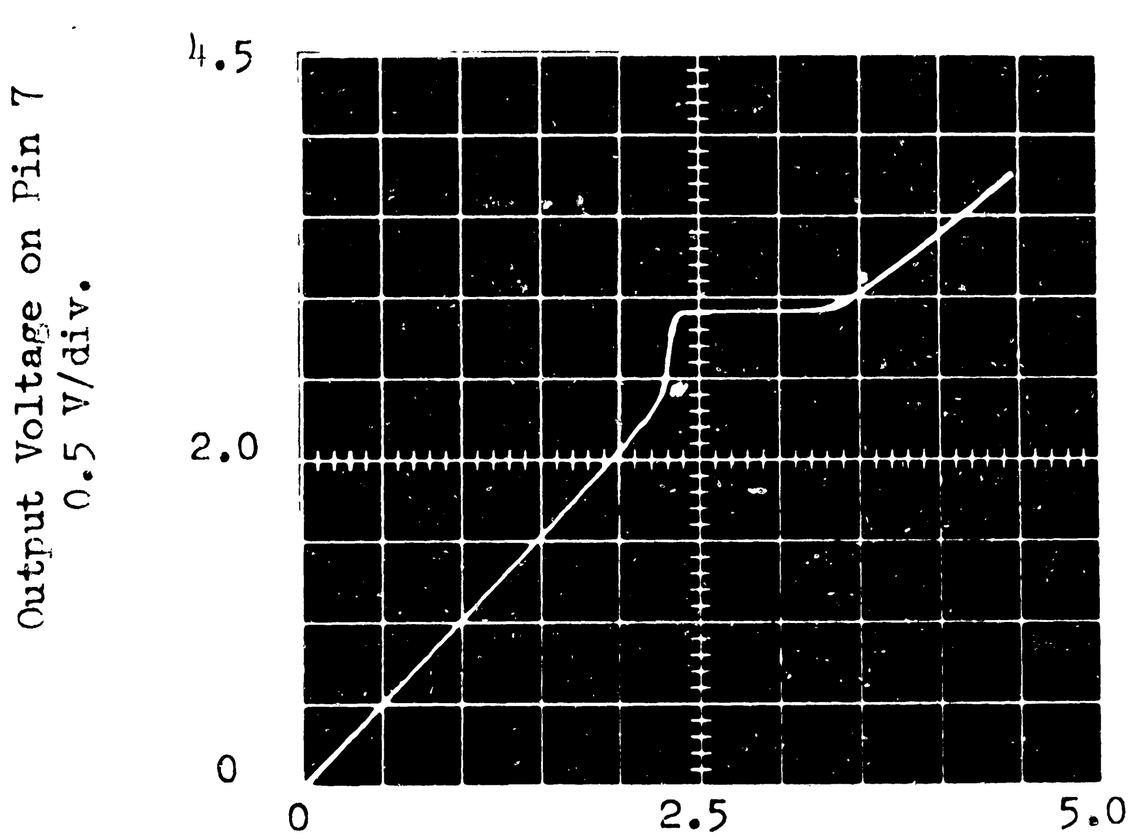


POWER DISSIPATION
DCTL G ELEMENT



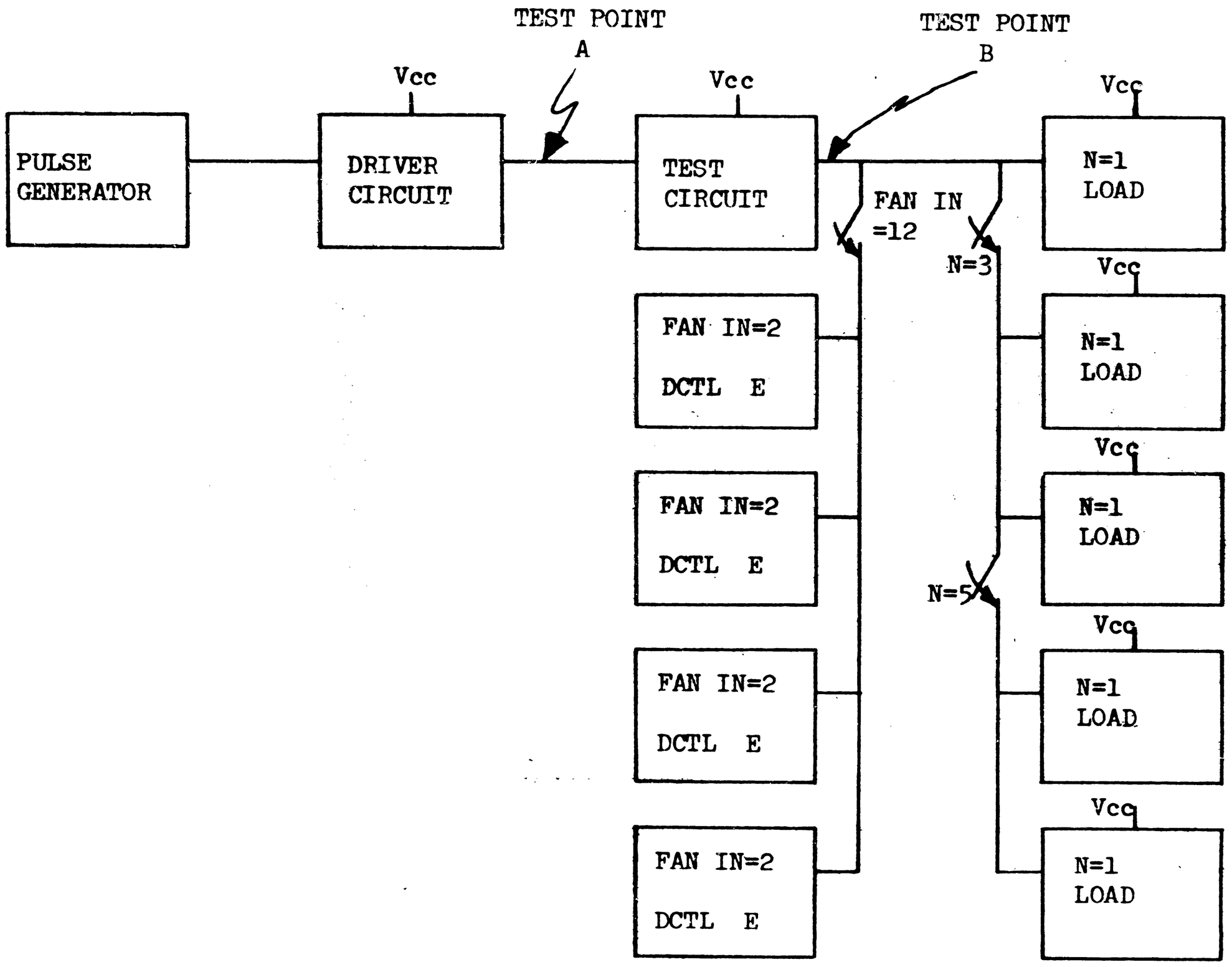


OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL G ELEMENT

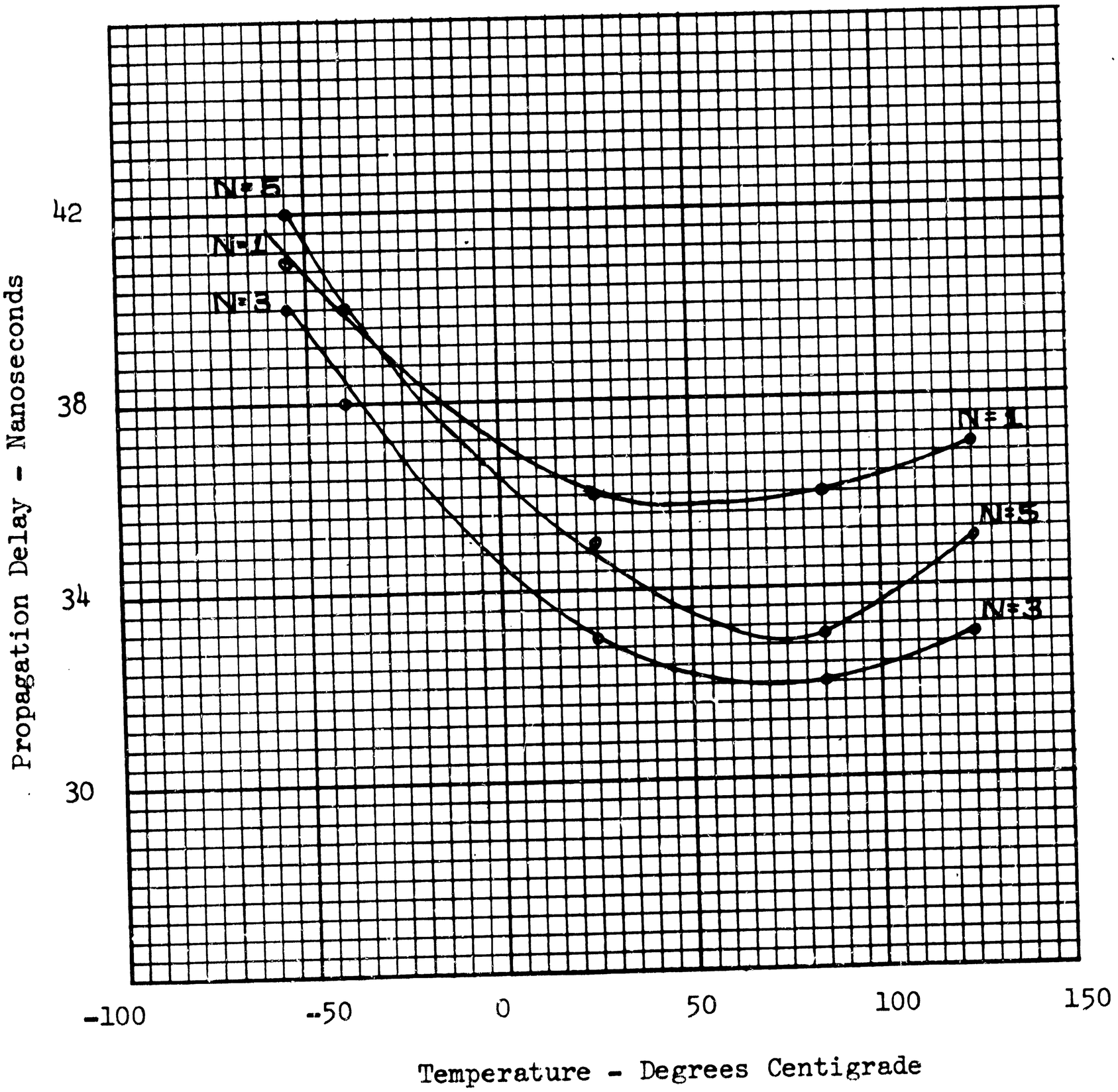


V_{cc} = 3.0

OUTPUT VOLTAGE versus NOISE VOLTAGE
DCTL G ELEMENT



TEST CIRCUIT FOR DCTL G GATE



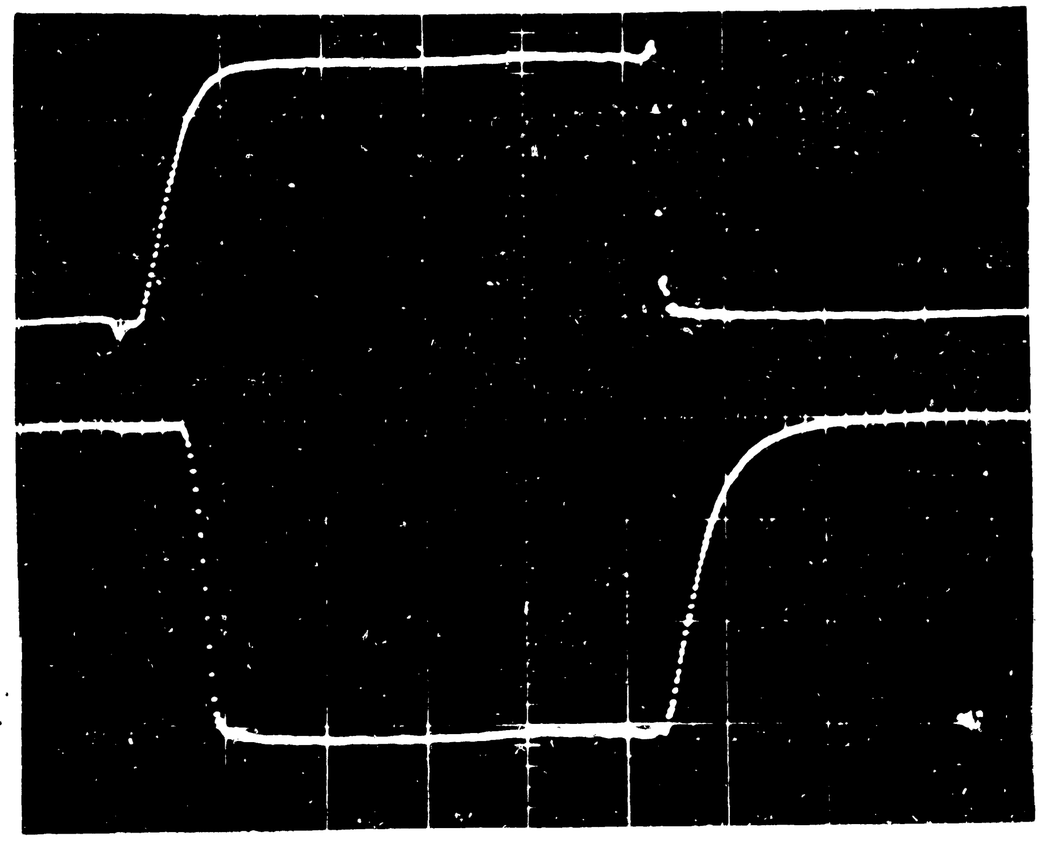
TEST CONDITIONS:
DATA FOR GRAPH TAKEN WI'H SUPPLY TO LOAD AND TEST
CIRCUITS HELD CONSTANT AT 3.0 V

DCTL - G ELEMENT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	517.	506.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.06	1.0	1.39	1.58
T_r	57.	98.	87.	83.
T_f	11.6	20.	21.	23.
T_d		44.	44.	45.
T_s	16.5	14.	13.	
T_{pd}	40.	36.	35.	



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	508.	497.	491.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.15	1.08	1.37	1.66
T_r	58.	93.	82.	78.
T_f	11.	22.	24.	27.
T_d		51.	51.	52.
T_s		15.	13.	12.
T_{pd}		42.	40.	38.

Type RTL No. G Temp. -55°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	506.	494.	492.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.16	1.10	1.39	1.69
T_r	58.	95.	84.	79.
T_f	12.	23.	26.	28.
T_d		52.	53.	52.
T_s		14.	11.	11.
T_{pd}		44.	41.	38.

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	524.	513.	508.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.0	0.94	1.23	1.52
T_r	59.	100.	91.	88.
T_f	12.	21.	22.	23.
T_d		40.	41.	41.
T_s		19.	16.5	15.
T_{pd}		39.	36.	35.

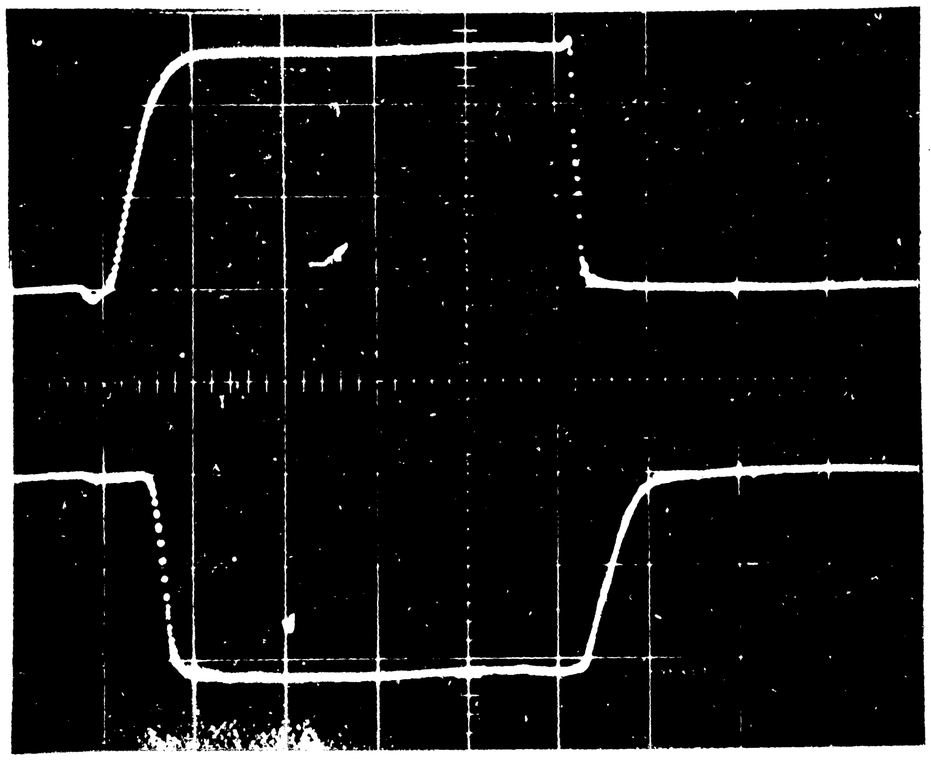
Type RTL No. G Temp. +125°C Vcc +3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	529.	518.	512.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.91	0.85	1.09	1.30
T_r	64.	103.	89.	82.
T_f	17.	25.	25.	25.
T_d		39.	40.	40.
T_s		23.	20.	18.
T_{pd}		40.	37.	35.

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	518.	503	497.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.08	0.78	0.90	1.02
T_r	56.	85.	62.	53.
T_f	12.	23.	24.	24.
T_d		43.	43.	43.
T_s		18.	14.	13.
T_{pd}		40.	33.	31.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	518.	500.	494.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.13	0.88	0.98	1.10
T_r	56.	90.	64.	54.
T_f	11.	25.	27.	27.
T_d		50.	51.	51.
T_s		16.	12.	10.
T_{pd}		45.	38.	35.

Type RTL No. G Temp. -55°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	518.	502.	495.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.18	0.90	1.02	1.12
T_r	57.	92.	65.	55.
T_f	11.	25.	26.	28.
T_d		53.	52.	53.
T_s		15.	11.	10.
T_{pd}		46.	40.	37.

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	524.	512.	506.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	.99	0.70	0.82	0.934
T_r	60.	83.	62.	55.
T_f	11.	27.	26.	26.
T_d		38.	38.	39.
T_s		18.	16.	14.
T_{pd}		38.	32.	31.

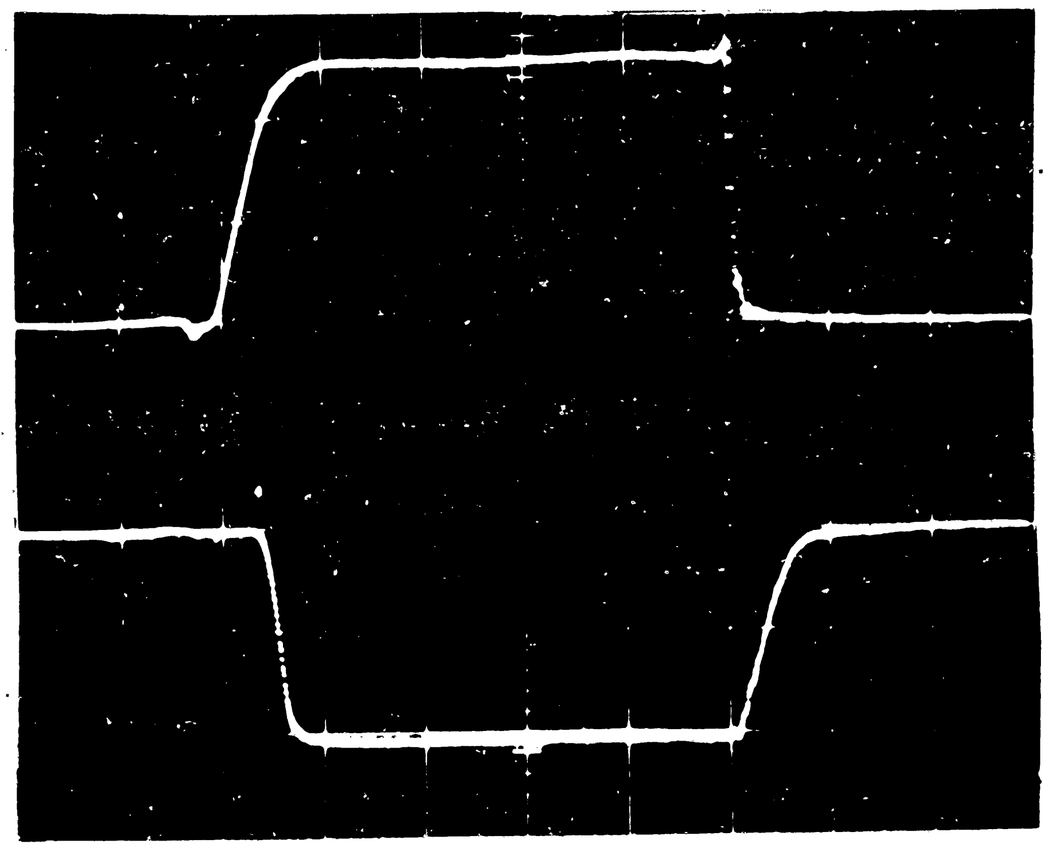
Type RTL No. G Temp. +125°C Vcc +3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	530.	517.	508.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.89	0.62	0.72	0.83
T_r	63.	84.	65.	58.
T_f	12.	32.	30.	29.
T_d		37.	37.	37.
T_s		22.	18.	16.
T_{pd}		39.	33.	31.

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	523.	506.	497.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.06	0.74	0.80	0.87
T_r	56.	95.	64.	53.
T_f	11.	26.	26.	26.
T_d	43.	43.	43.	43.
T_s	15.	12.	12.	10.
T_{pd}	43.	35.	35.	32.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	518.	500.	490.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.16	0.86	0.93	1.0
T_r	58.	107.	72.	58.
T_f	14.	29.	29.	29.
T_d		49.	49.	50.
T_s		18.	11.	10.
T_{pd}		50.	40.	37.

Type RTL No. G Temp. -55°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	515.	496.	487.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.18	0.88	0.95	1.02
T_r	59.	113.	77.	60.
T_f	12.	29.	30.	32.
T_d		51.	51.	51.
T_s		16.	10.	9.
T_{pd}		52.	42.	38.

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	527.	510.	503.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.98	0.64	0.71	0.78
T_r	59.	97.	63.	51.
T_f	12.	40.	37.	36.
T_d		40.	40.	40.
T_s		17.	15.	12.
T_{pd}		42.	33.	31.

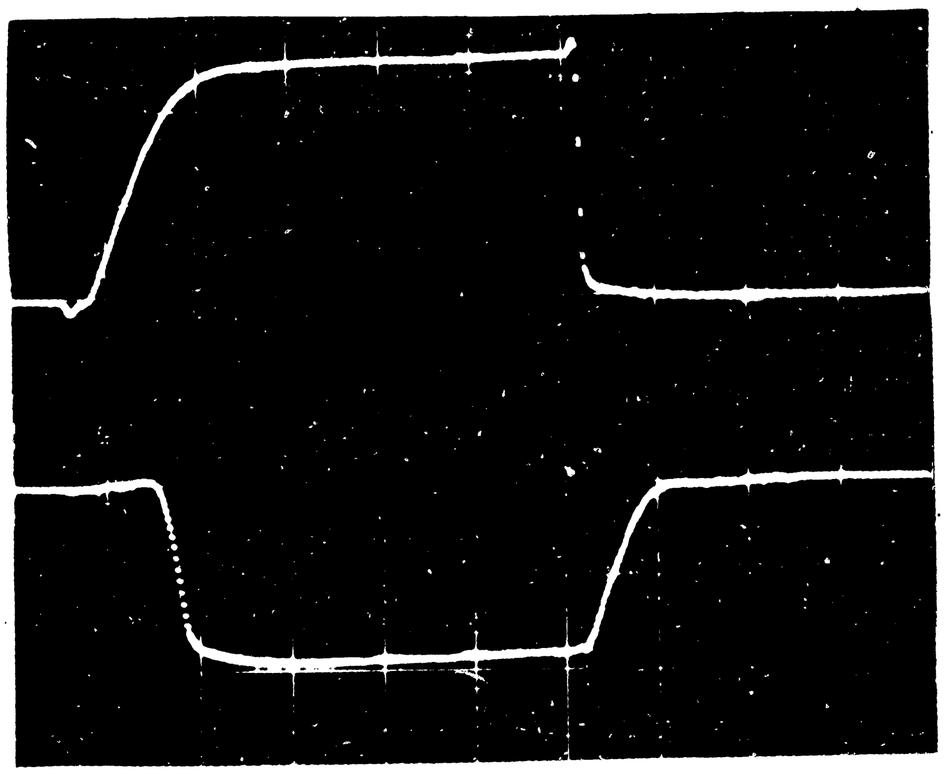
Type RTL No. G Temp. +125°C Vcc +3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	527.	513.	507.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.91	0.56	0.62	0.79
T_r	63.	92.	68.	54.
T_f	17.	50.	44.	42.
T_d		39.	39.	39.
T_s		18.	16.	16.
T_{pd}		40	35	32

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +25°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	508.	492.	484.
Repetition Rate	1MC	1MC	1MC	1MC
Pulse Amplitude	1.08	0.73	0.80	0.87
T_r	97.	97.	67.	53.
T_f	13.	34.	34.	35.
T_d		67.	67.	67.
T_s		15.	11.	10.
T_{pd}		49.	41.	38.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. -40°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	499.	481.	473.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.19	0.85	0.918	0.98
T_r	97.	106.	71.	56.
T_f	12.	33.	35.	36.
T_d		76.	75.	76.
T_s		15.	10.	9.
T_{pd}		56.	47.	44.

Type RTL No. G Temp. -55°C Vcc 3.0 N = 5 FAN IN = 12

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	498.	477.	468.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.18	0.87	0.94	1.01
T_r	97.	115.	73.	57.
T_f	12.	35.	37.	40.
T_d		80.	79.	78.
T_s		15.	10.	9.
T_{pd}		60.	50.	46.

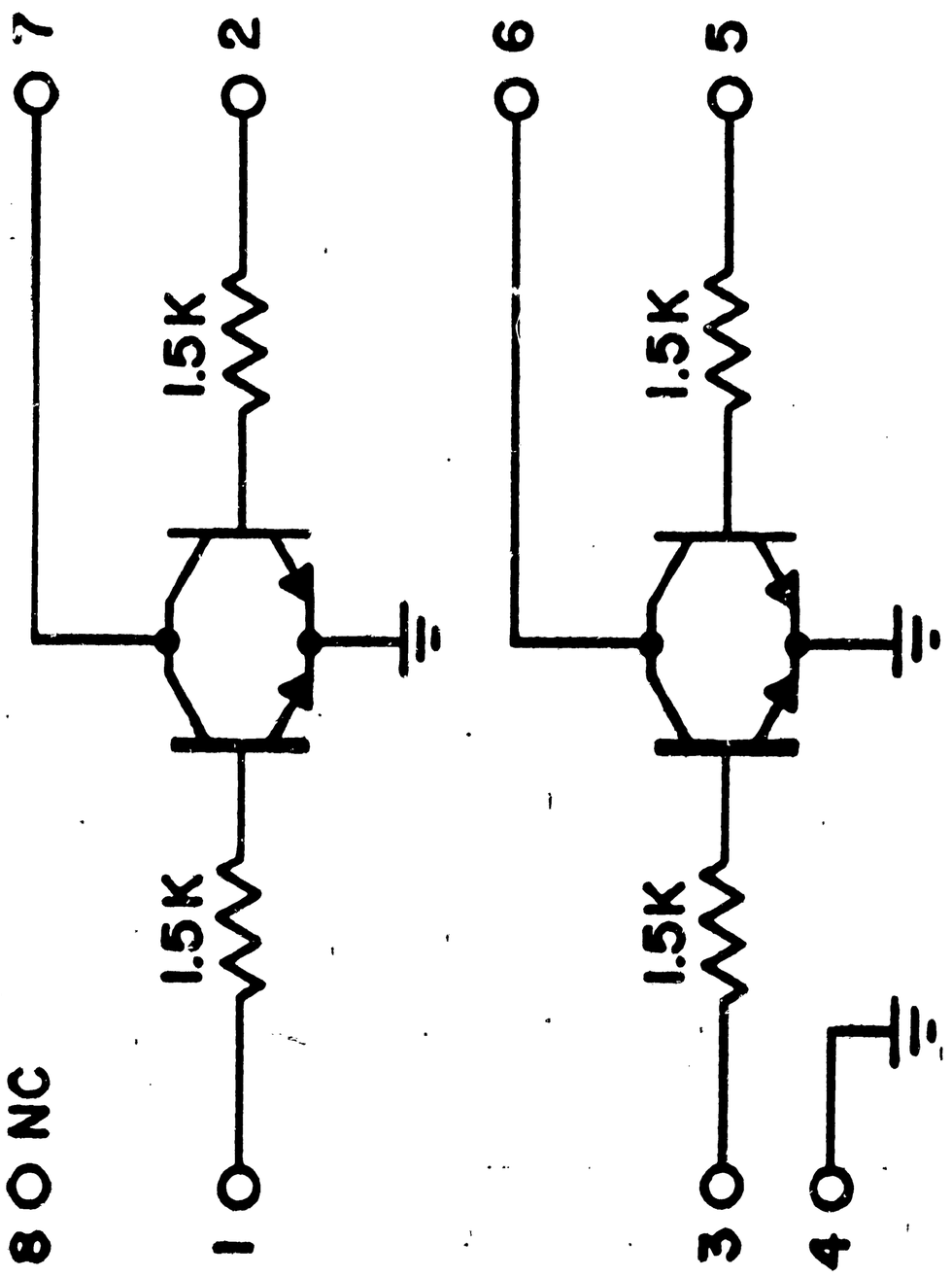
GENERAL MICRO-ELECTRONICS

Type RTL No. G Temp. +85°C Vcc 3.0 N = 5 FAN IN = 12

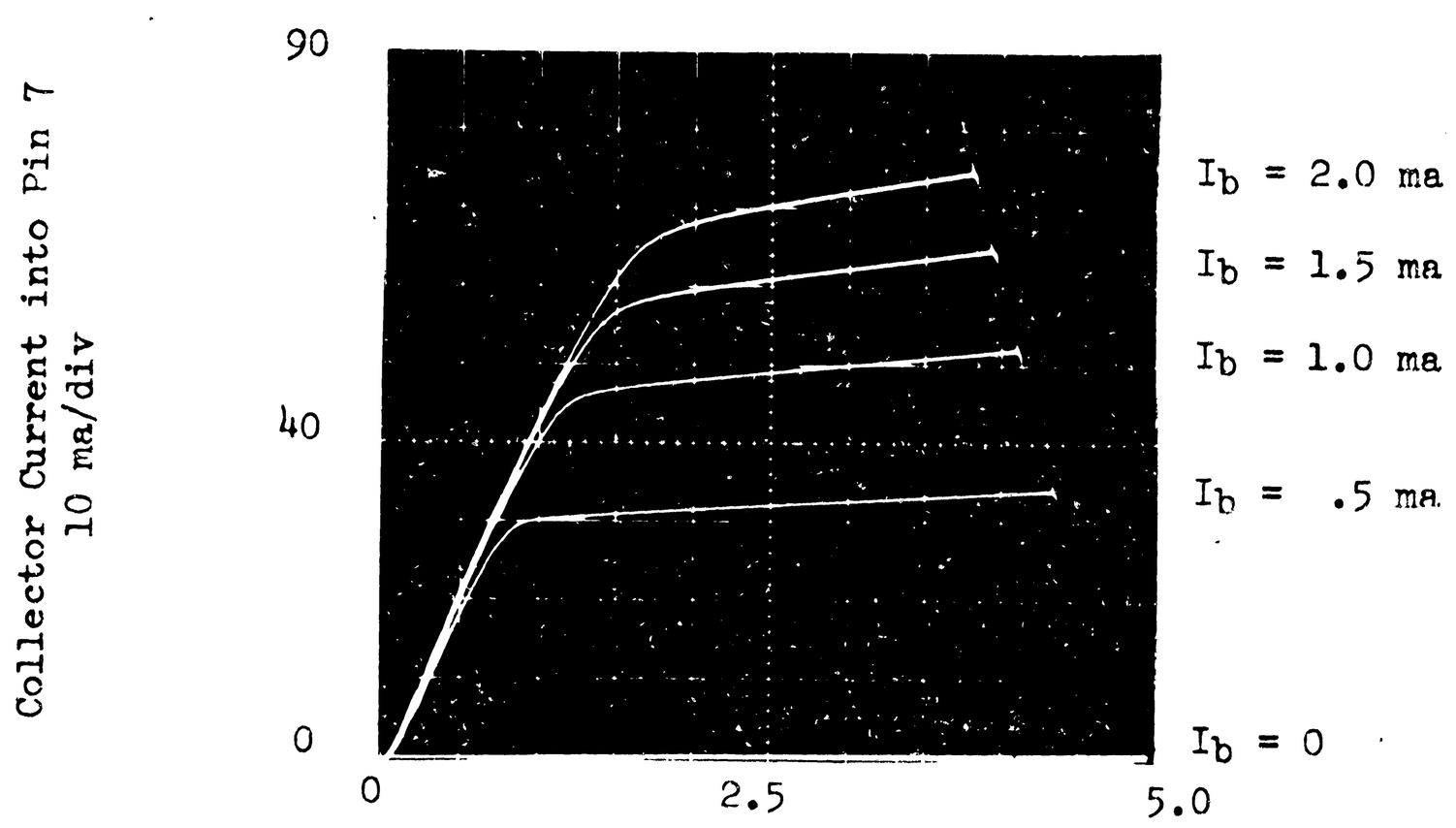
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	517.	502.	495.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.99	0.62	0.69	0.76
T_r	106.	95.	65.	52.
T_f	14.	44.	42.	41.
T_d		60.	60.	60.
T_s		18.	15.	13.
T_{pd}		45.	38.	35

Type RTL No. G Temp. +125°C Vcc 3.0 N = 5 FAN IN = 12

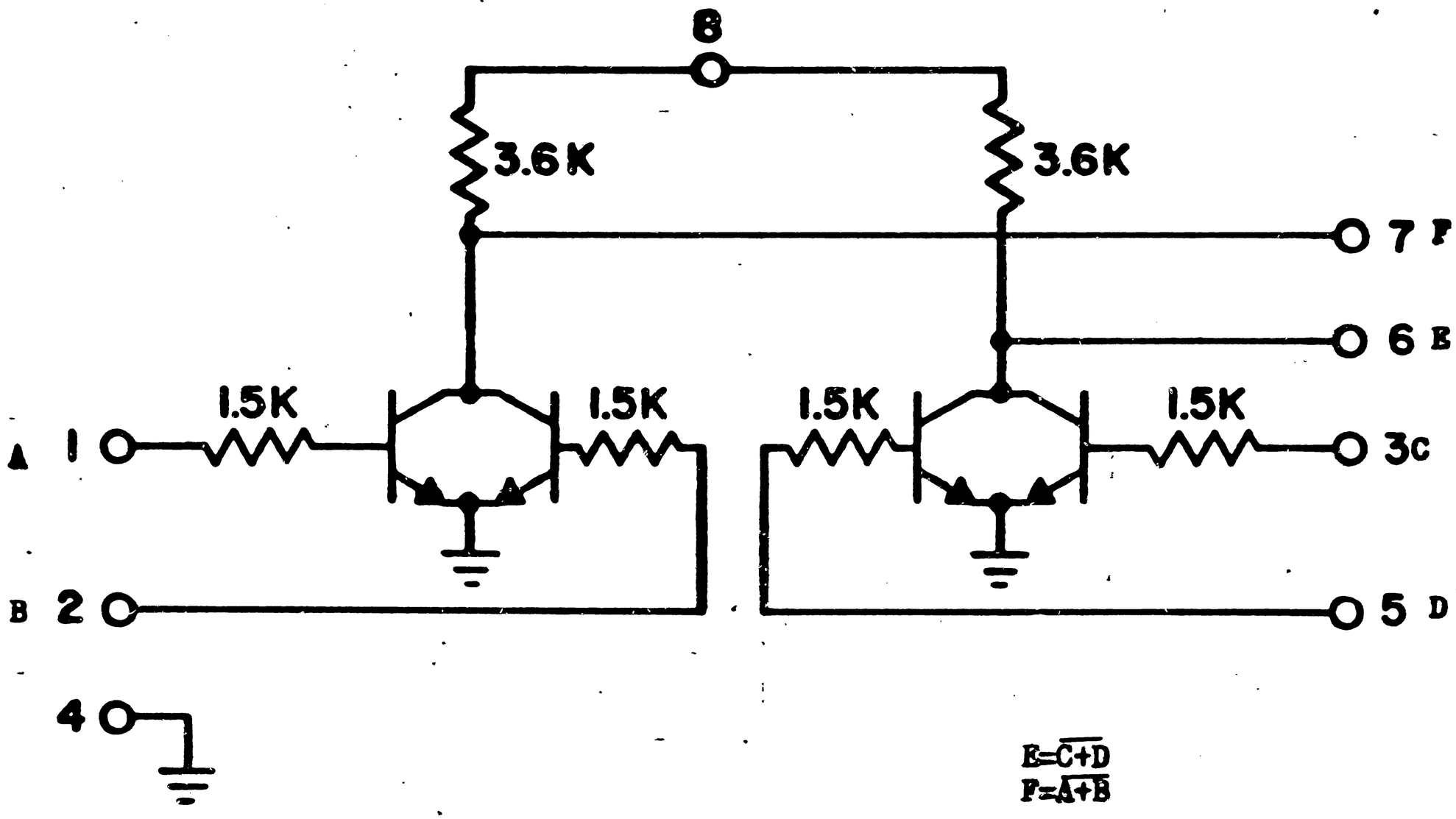
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	522.	507.	499.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.90	0.54	0.60	0.67
T_r	118.	98.	67.	54.
T_f	16.	55.	53.	52.
T_d		59.	59.	54.
T_s		21.	17.	15.
T_{pd}		45.	37.	35.



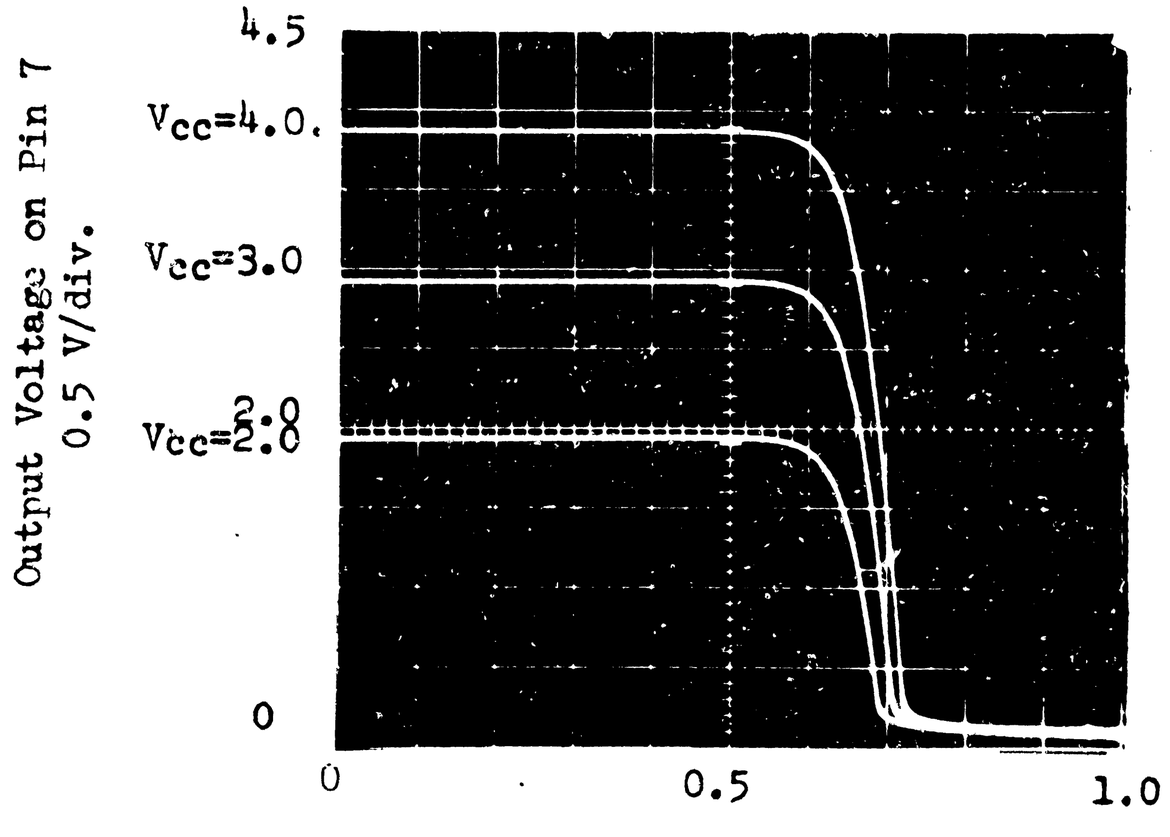
DUAL 2 - INPUT DCTL EXPANDER GATE, E



TRANSISTOR CHARACTERISTICS
DCTL E ELEMENT

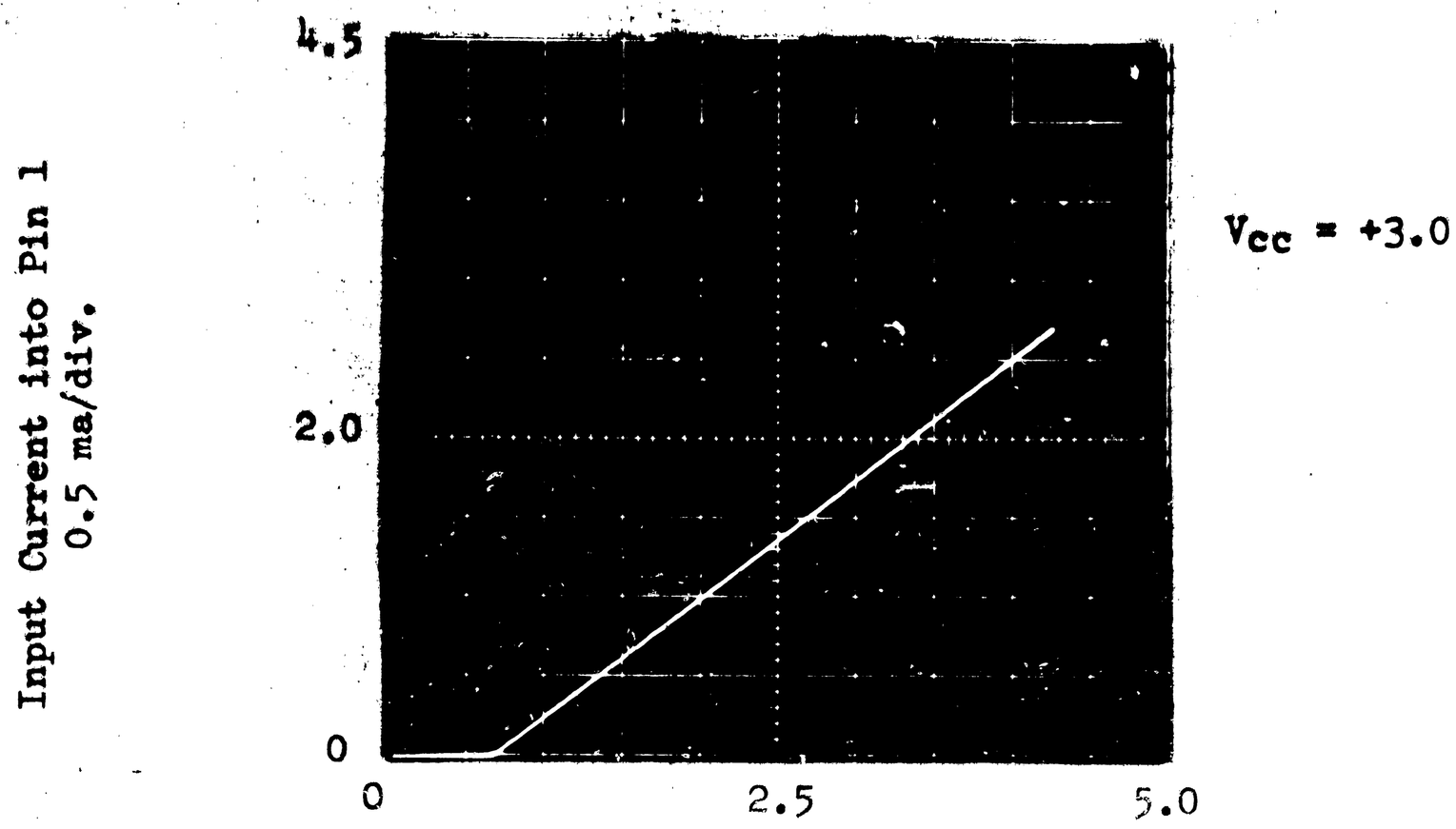


DUAL 2 - INPUT DCTL GATE, D_2

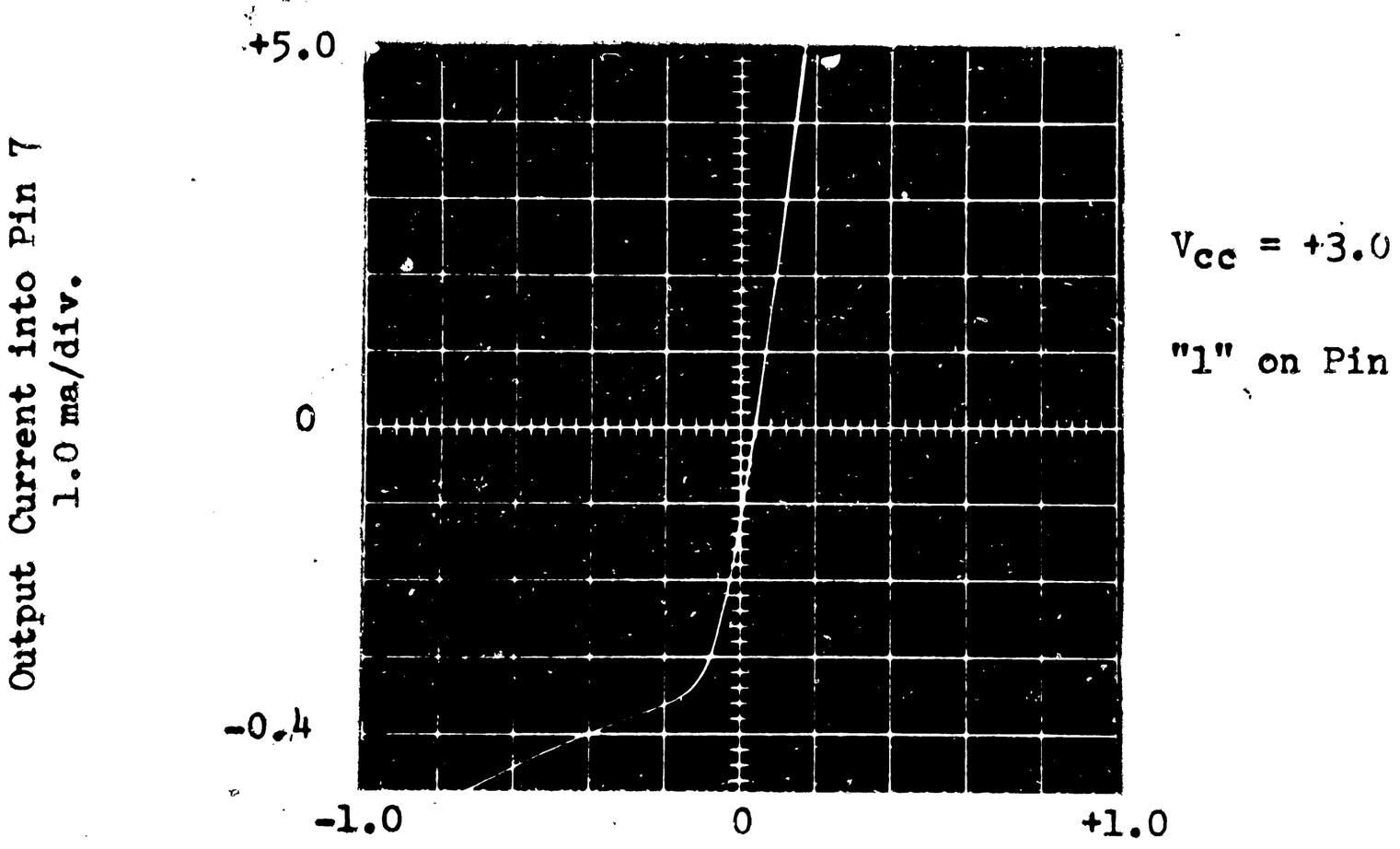


INPUT OUTPUT CHARACTERISITCS
DCTL D_2 ELEMENT

3.2.35

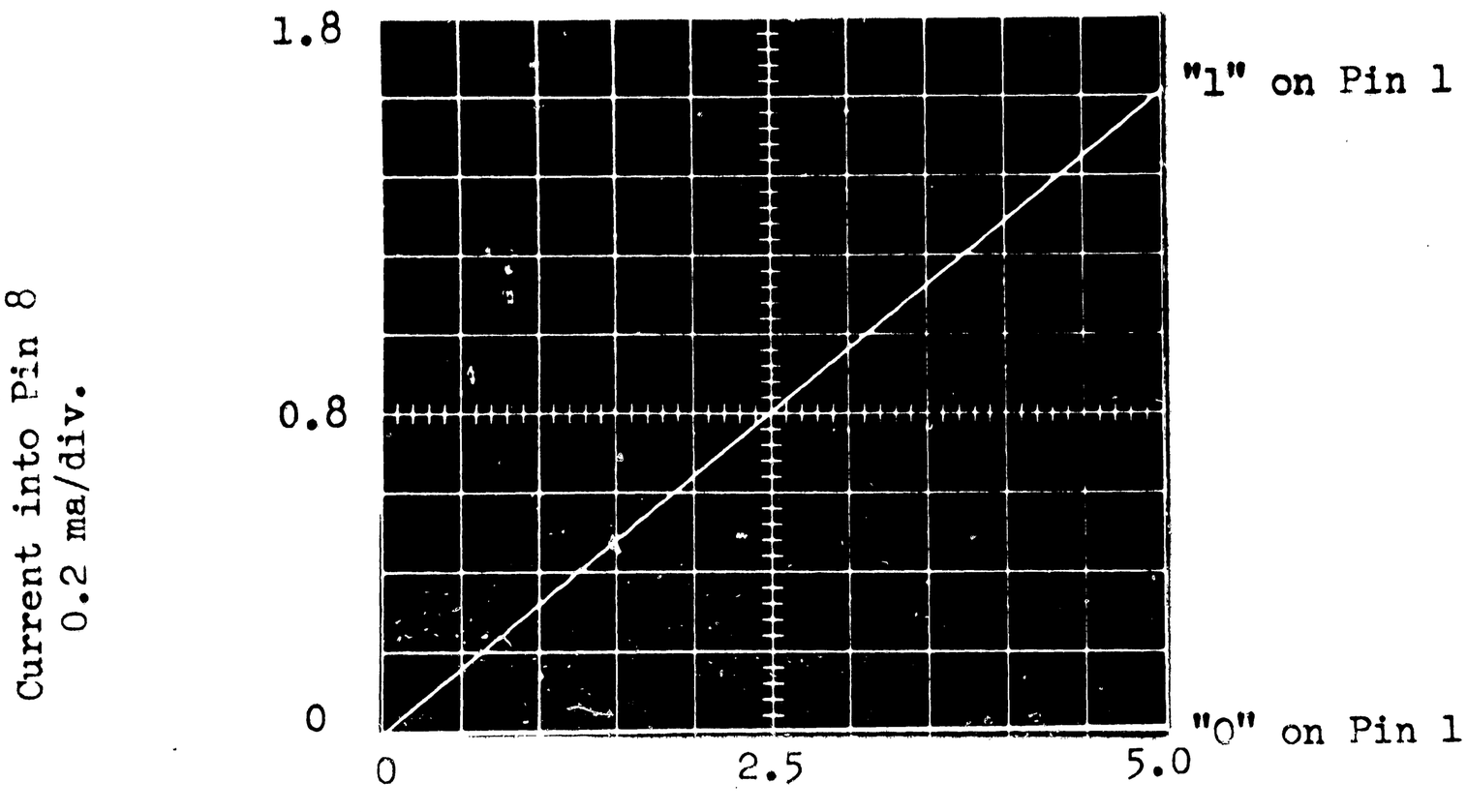


INPUT CHARACTERISITCS

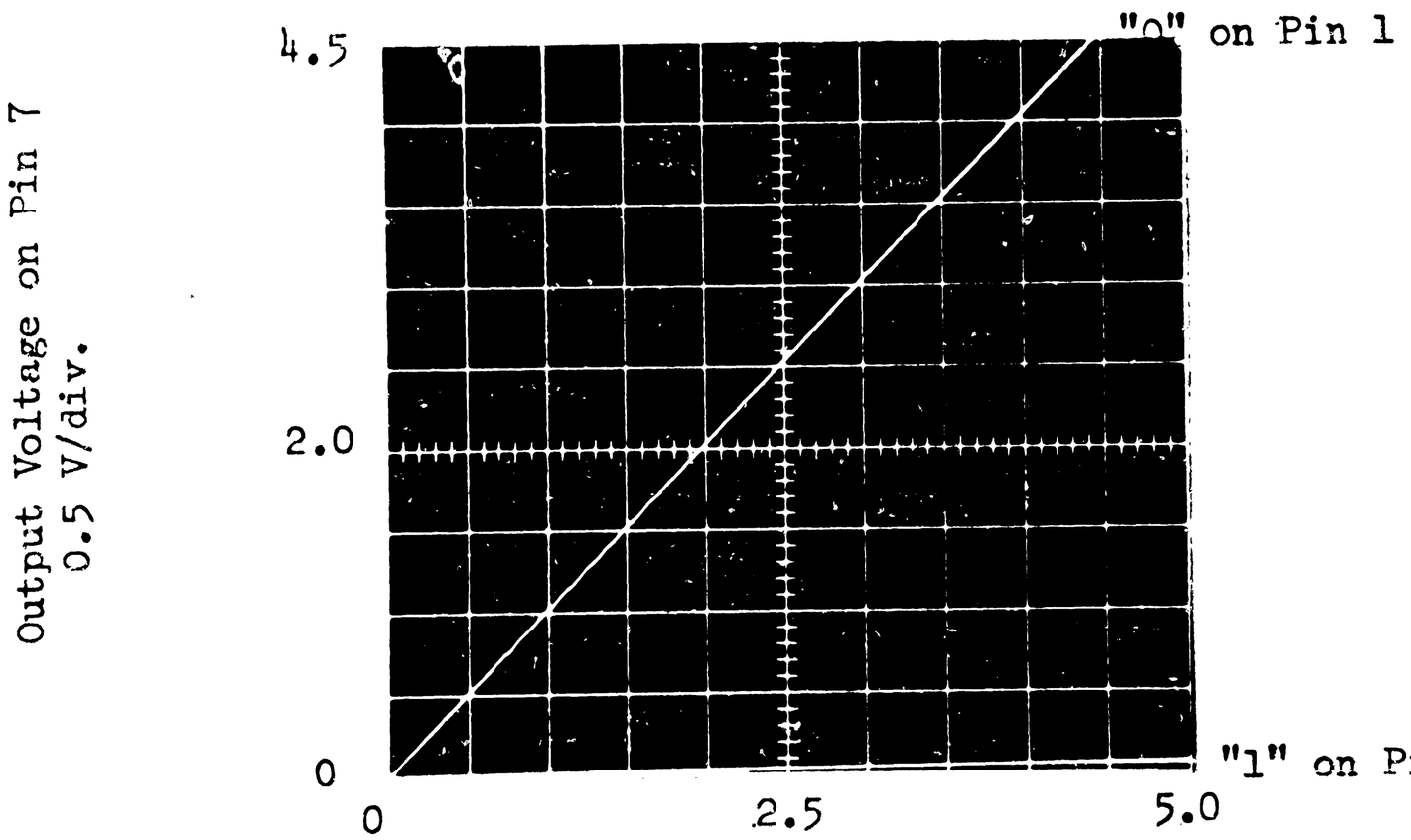


OUTPUT CHARACTERISTICS
DCTL D_2 ELEMENT

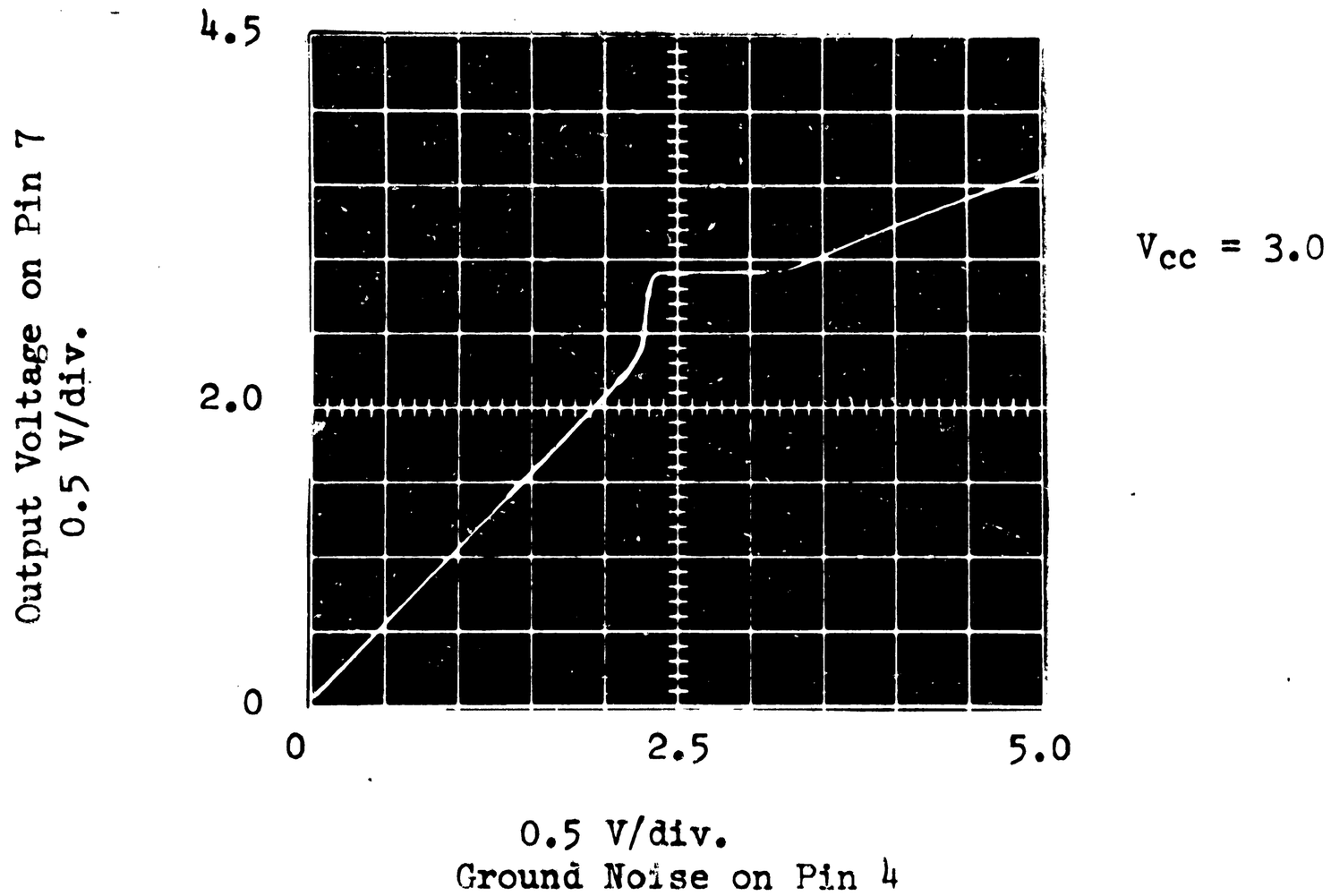
3.2.36



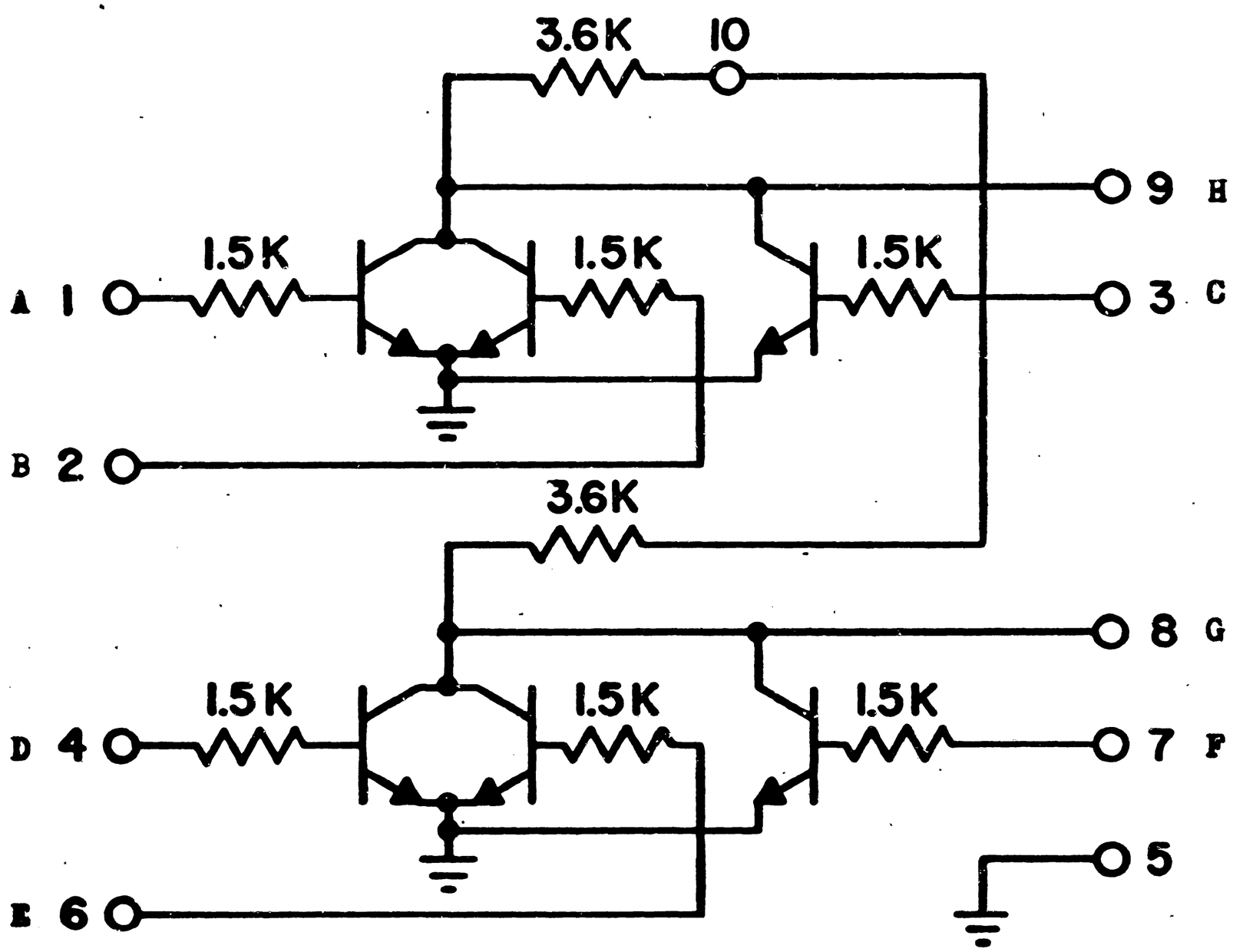
POWER DISSIPATION



OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL D_2 ELEMENT

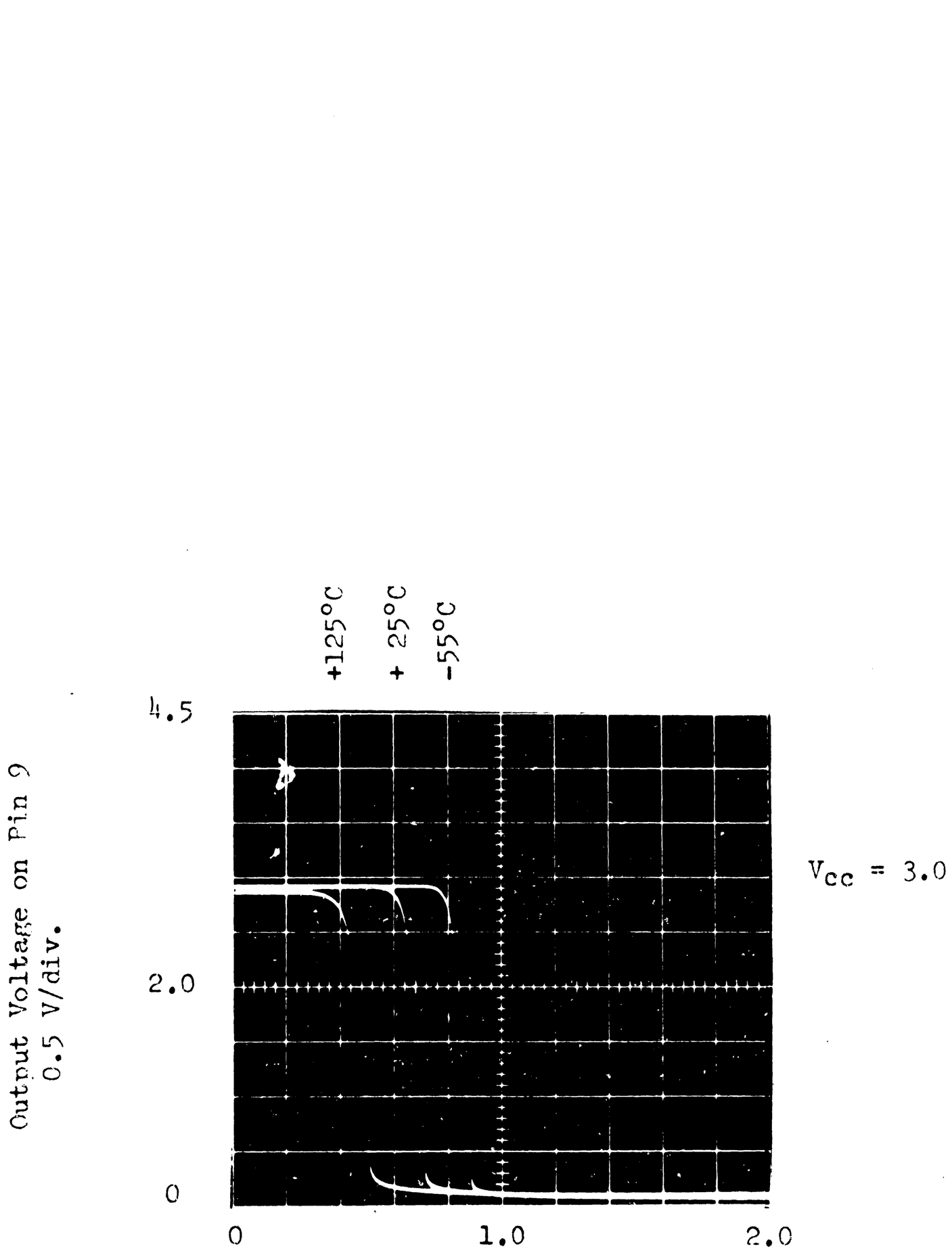


OUTPUT VOLTAGE versus NOISE VOLTAGE
DCTL D_2 ELEMENT

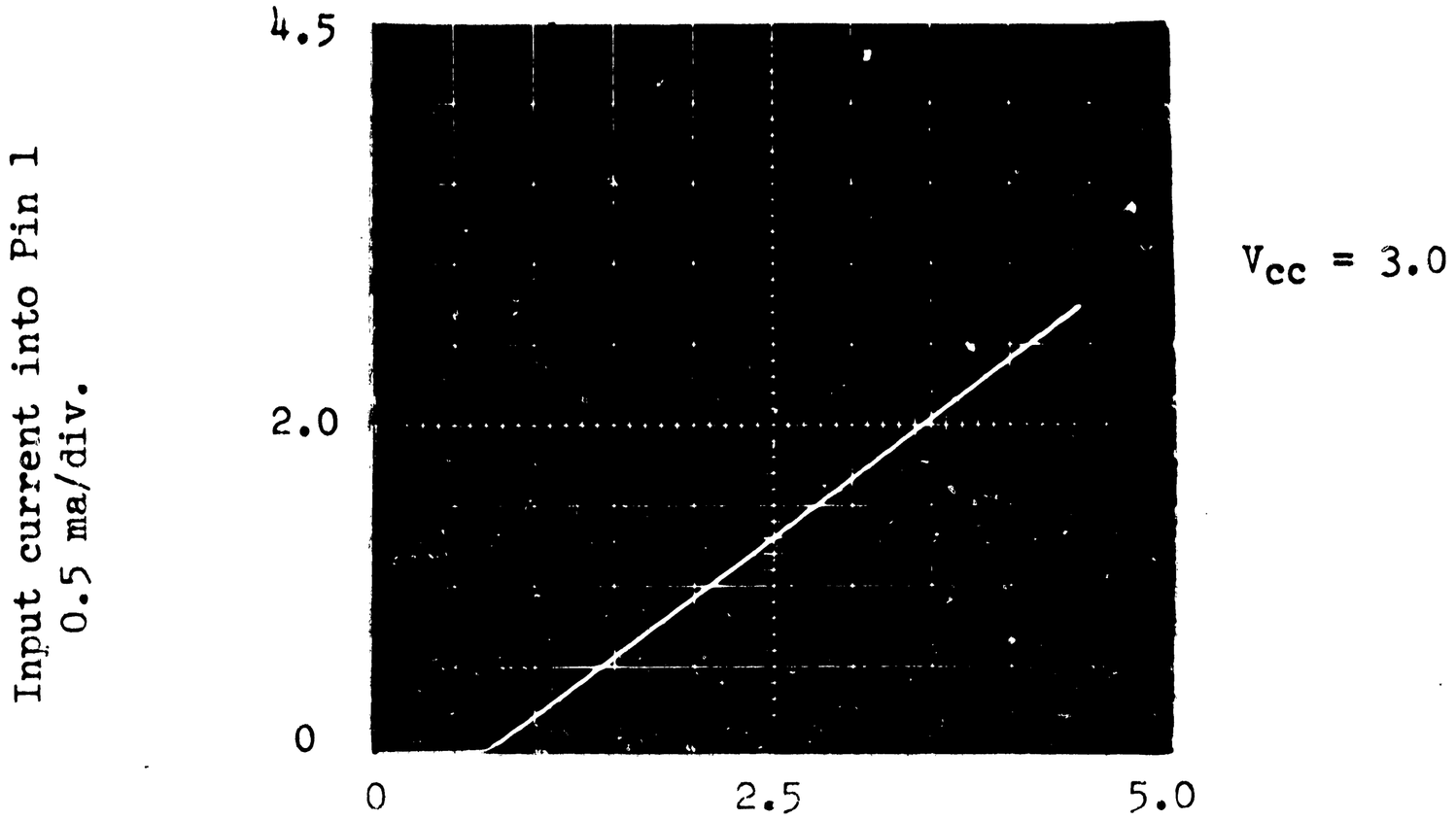


$H=\overline{A+B+C}$
$G=\overline{D+E+F}$

DUAL 3 - INPUT DCTL GATE, D_3

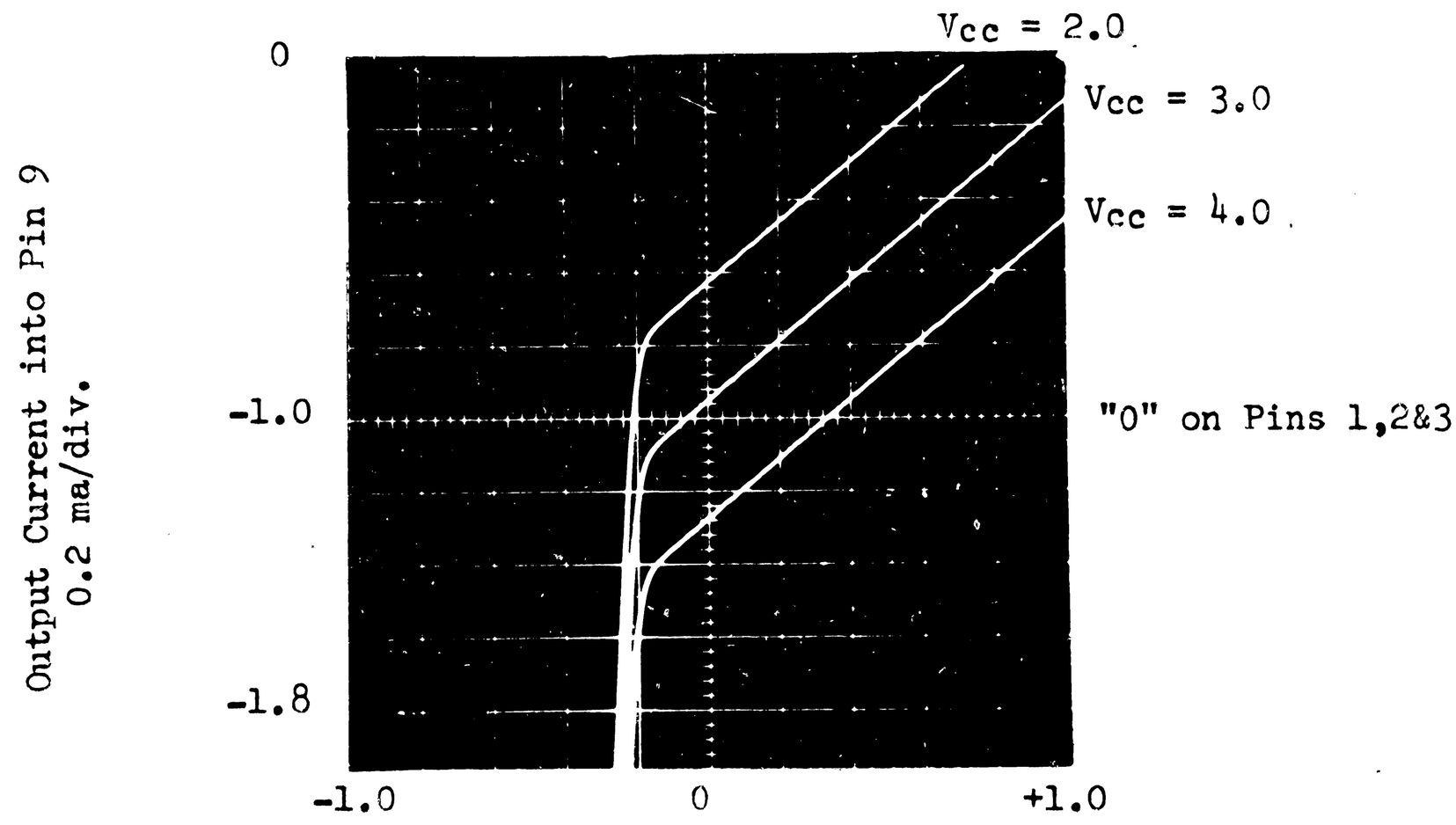


INPUT OUTPUT CHARACTERISTICS
DCTL D_3 ELEMENT



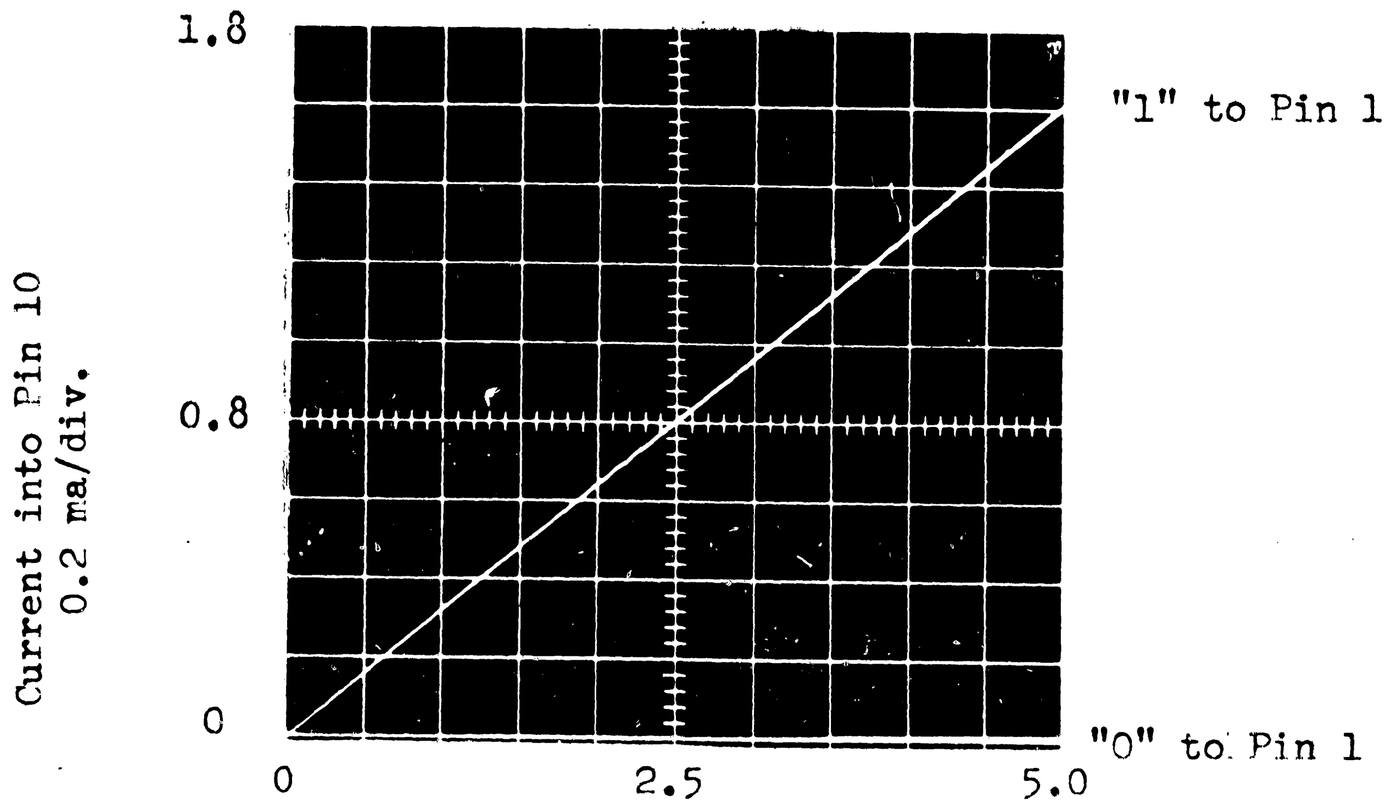
0.5 V/div.
Input Voltage on Pin 1

INPUT CHARACTERISTICS



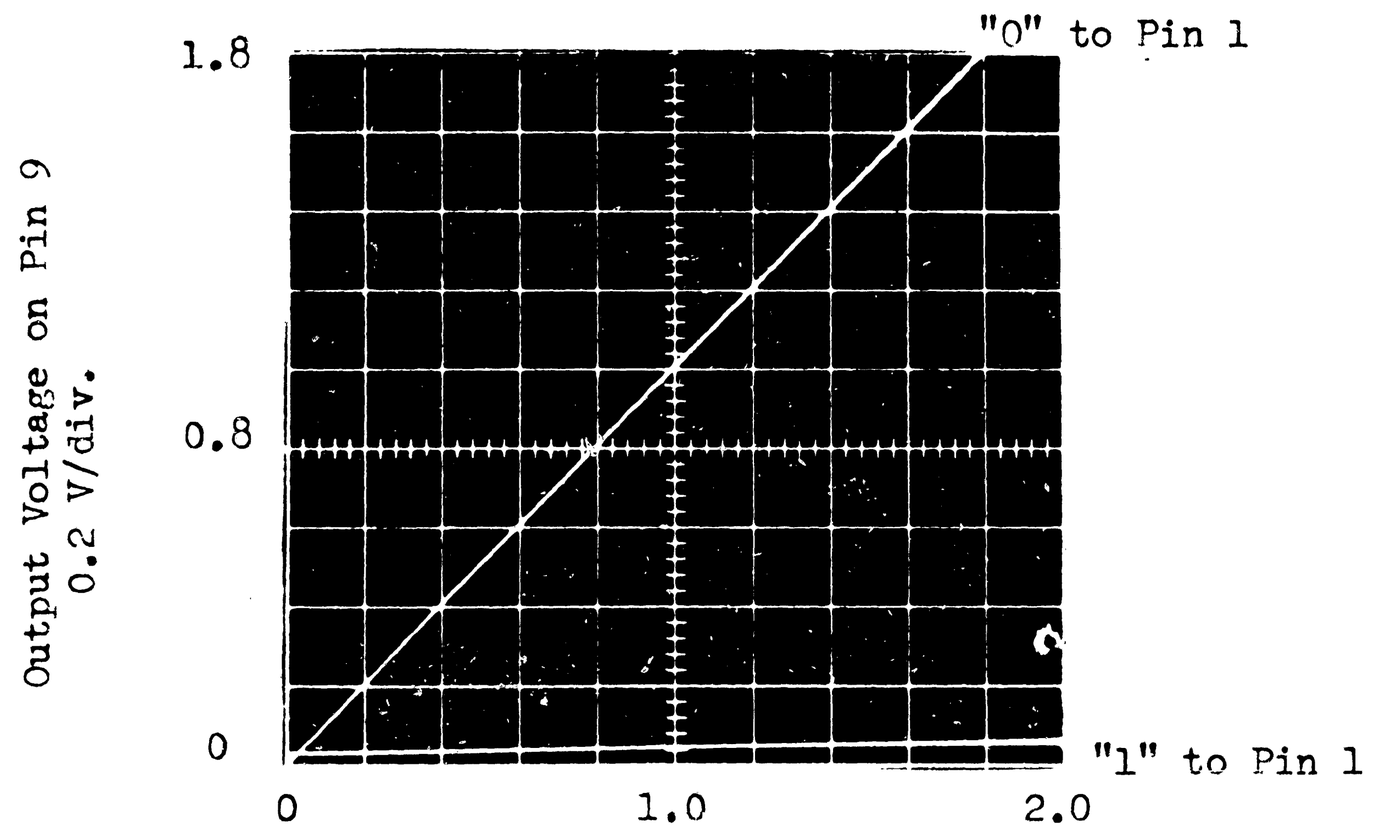
0.5 V/div.
Output Voltage on Pin 9

OUTPUT CHARACTERISTICS
DCTL D_3 ELEMENT



0.5 V/div.
Supply Voltage on Pin 10

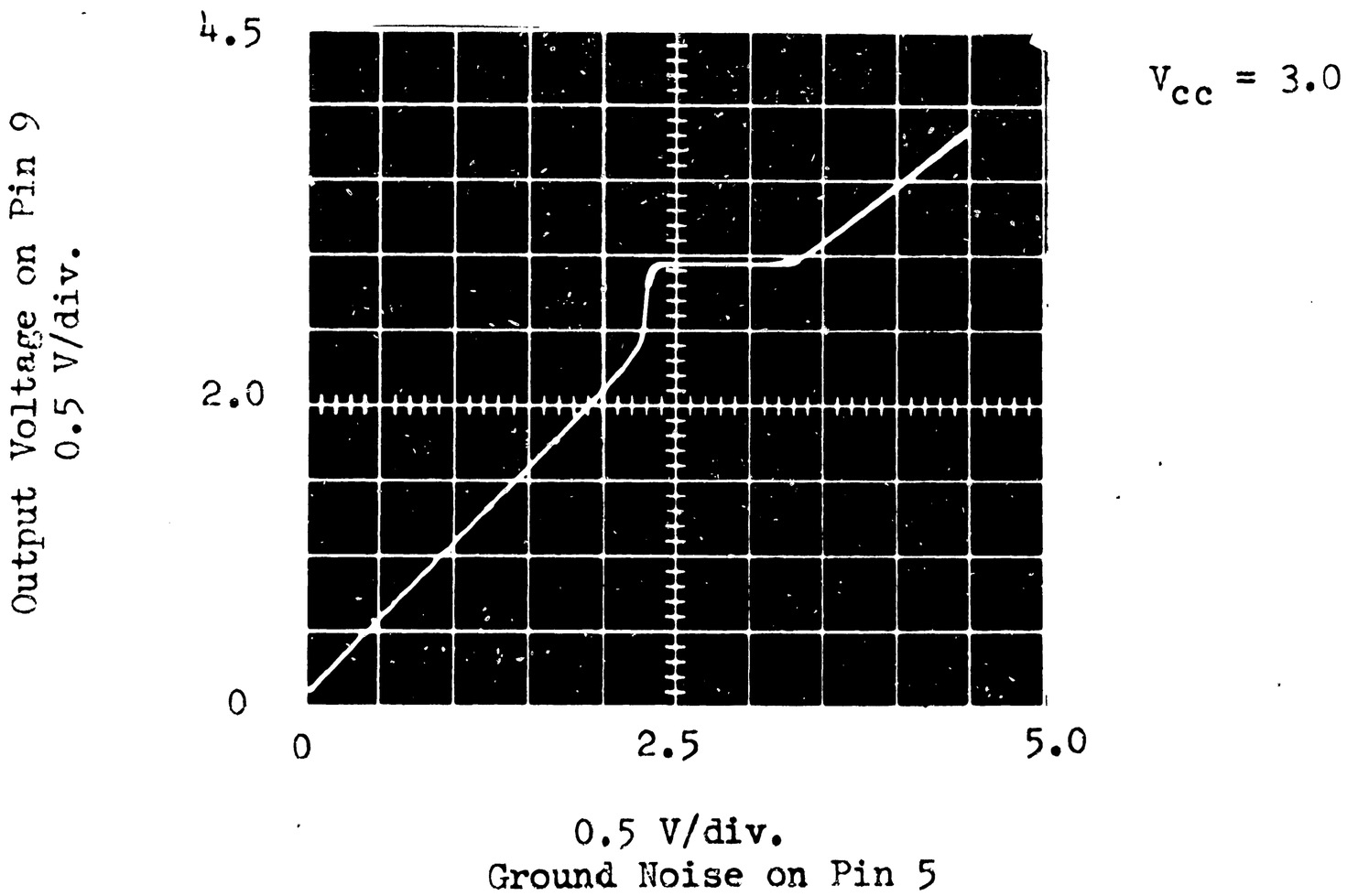
POWER DISSIPATION



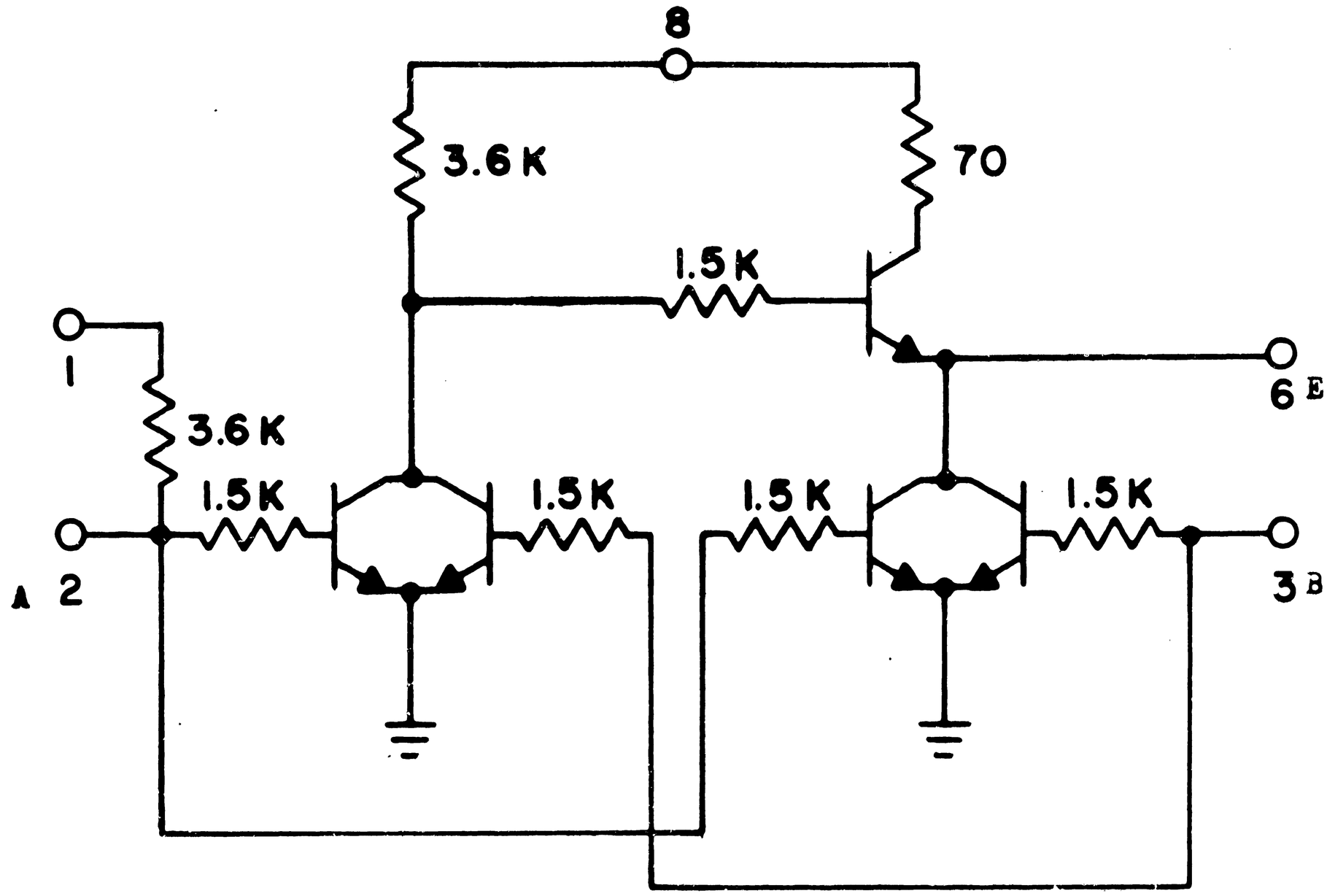
0.2 V/div.
Supply Voltage on Pin 10

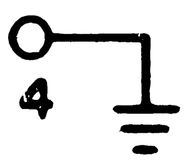
OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL D_3 ELEMENT

3.2.42



OUTPUT VOLTAGE versus GROUND NOISE VOLTAGE
DCTL D_3 ELEMENT





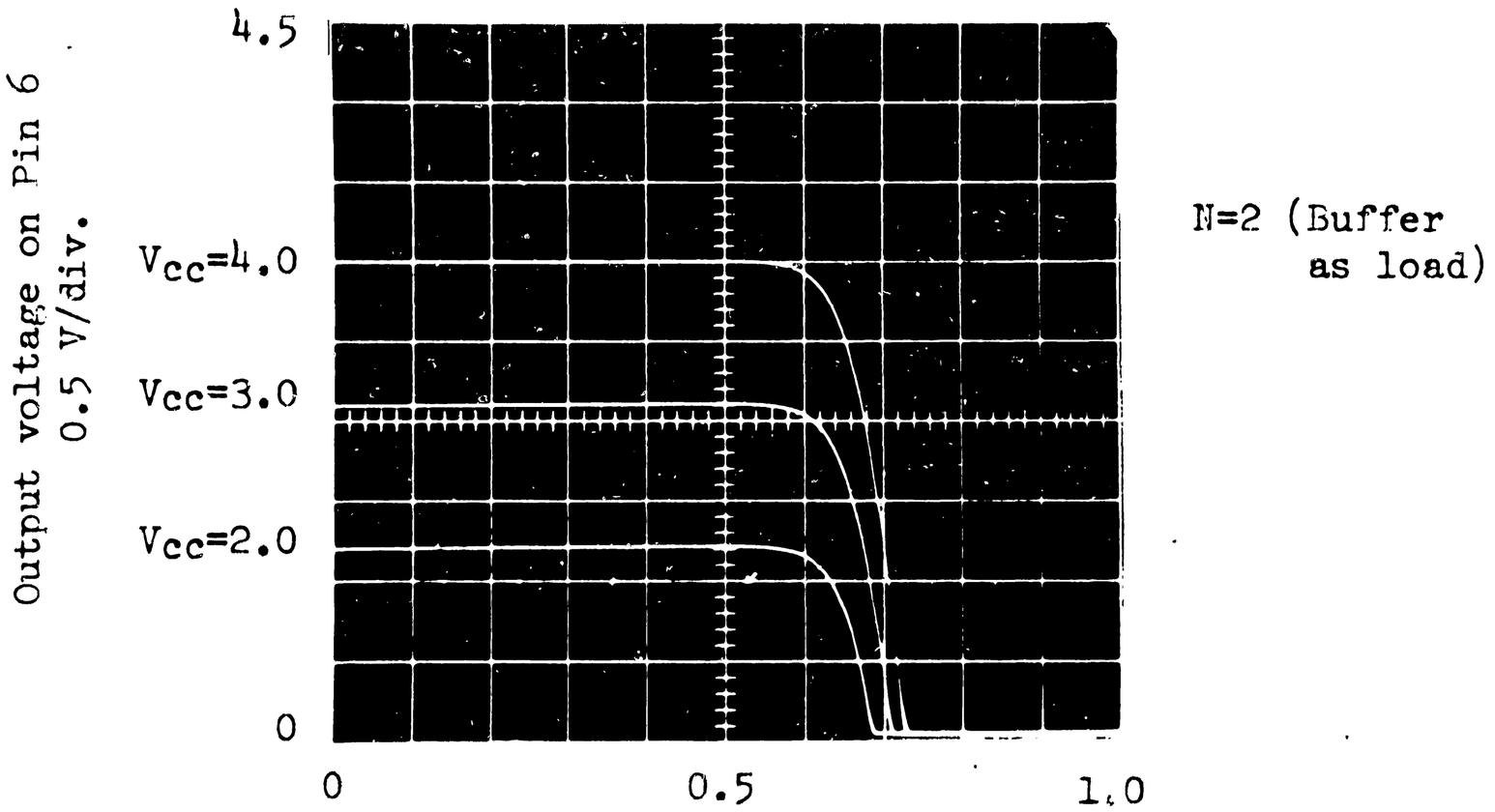
NC 5

NC 7

$E=\overline{A+B}=\overline{A}\,\overline{B}$

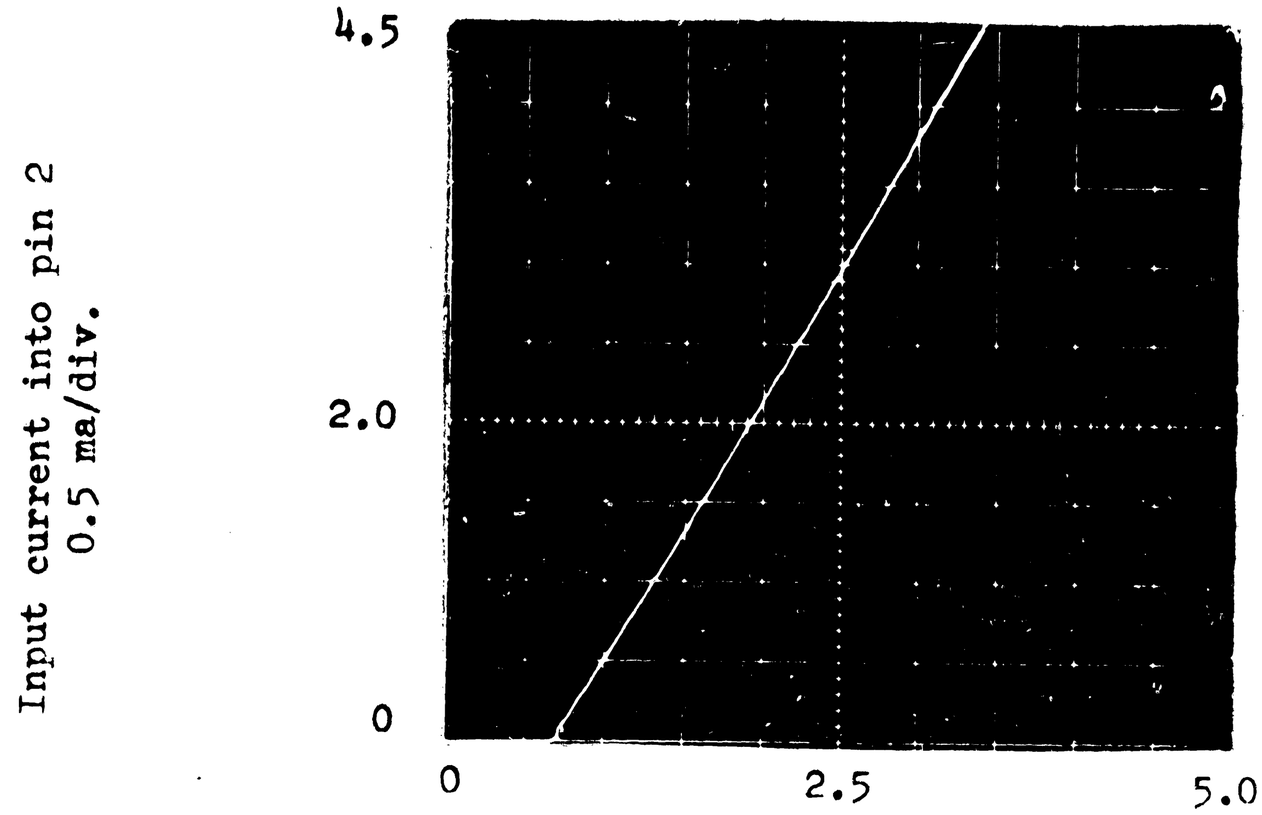
DCTL BUFFER ELEMENT, B

3.2.44

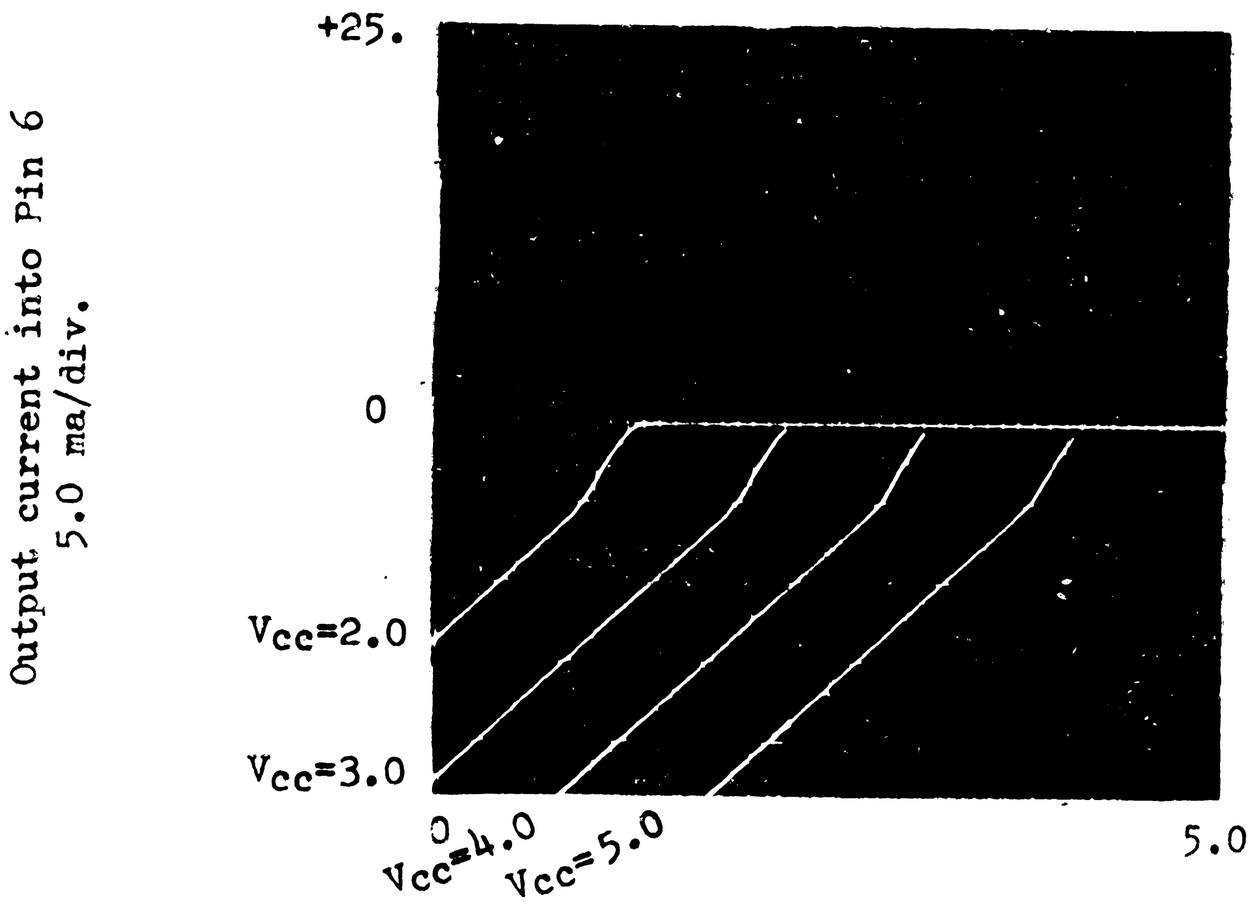


INPUT OUTPUT CHARACTERISTICS

DCTL B ELEMENT

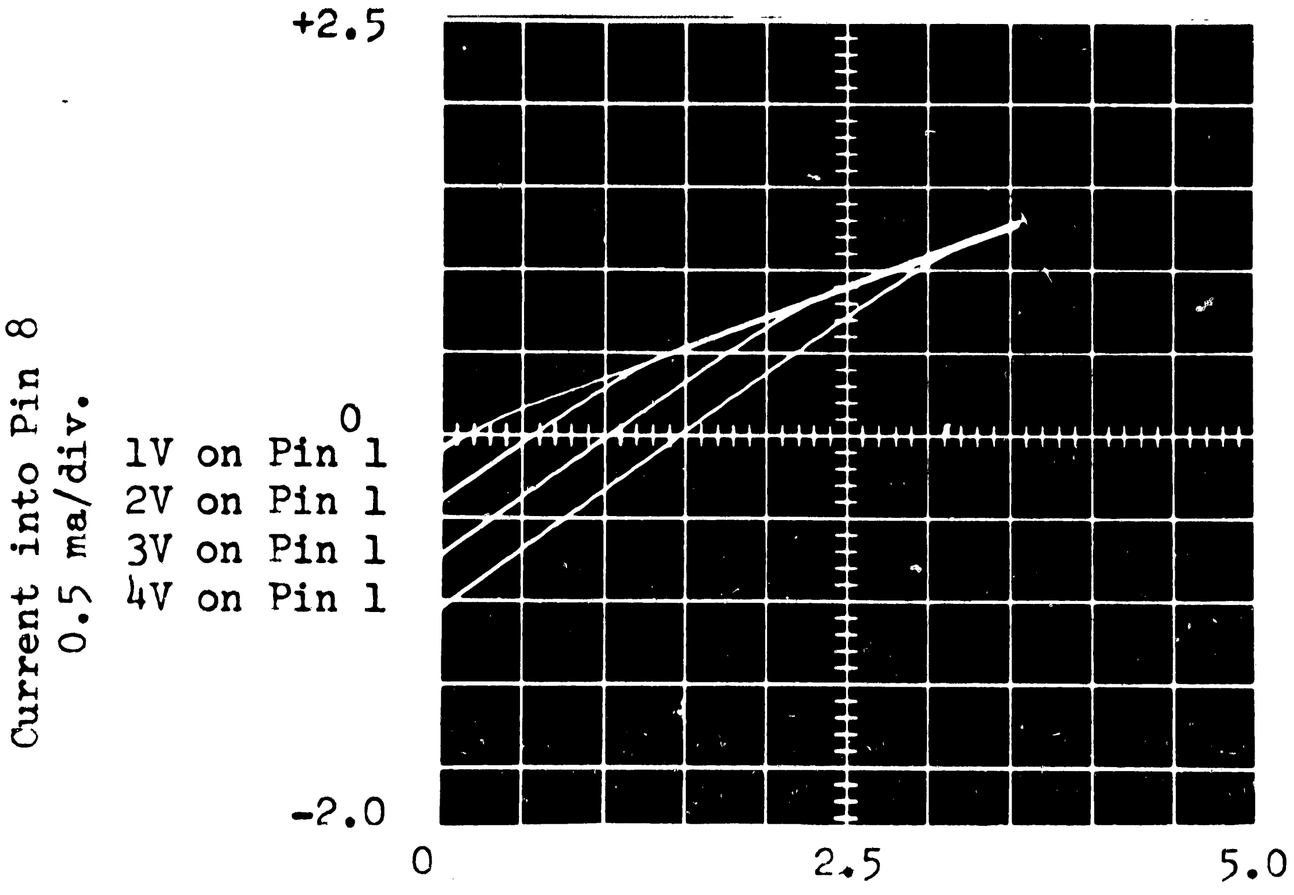


INPUT CHARACTERISTICS



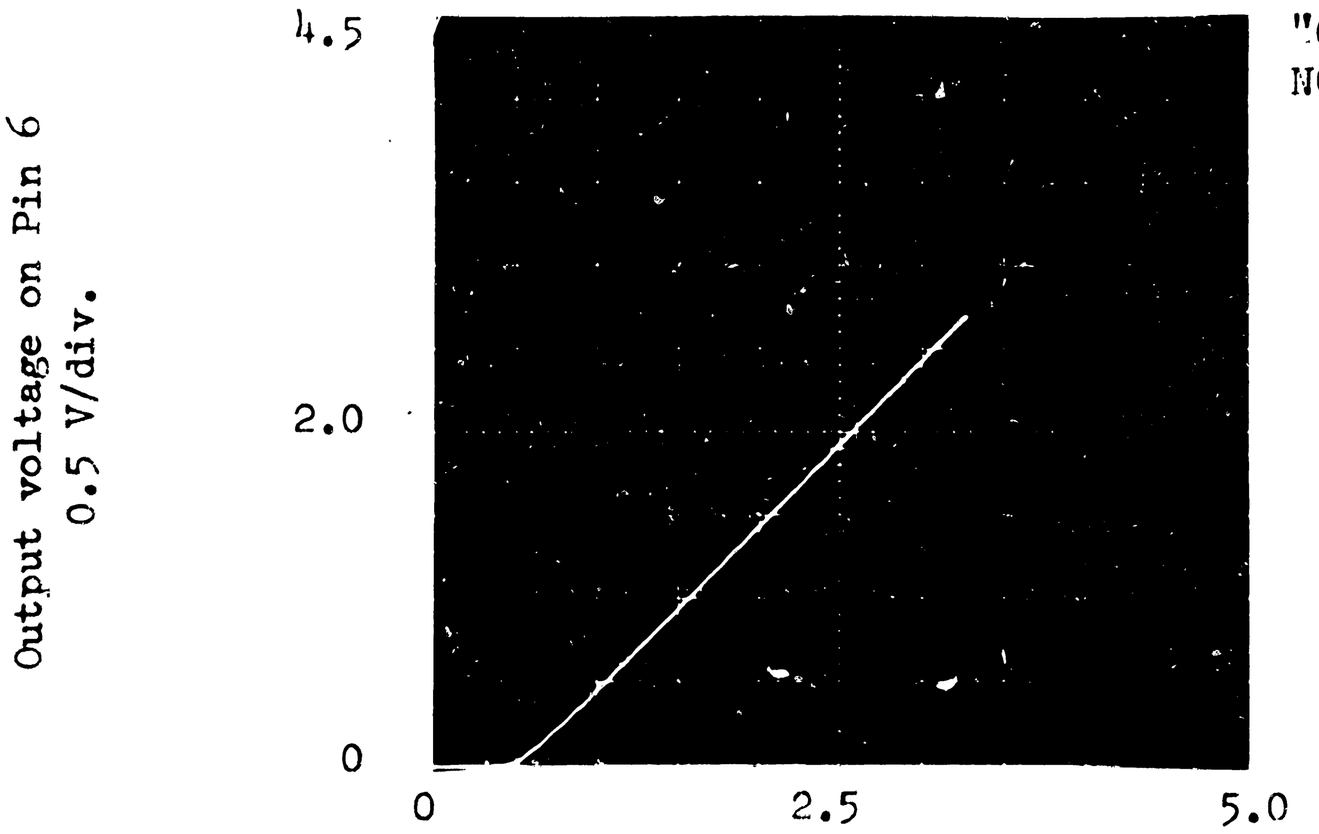
OUTPUT CHARACTERISTICS
DCTL B ELEMENT

3.2.46



0.5 V/div.
Supply Voltage on Pin 8

POWER DISSIPATION

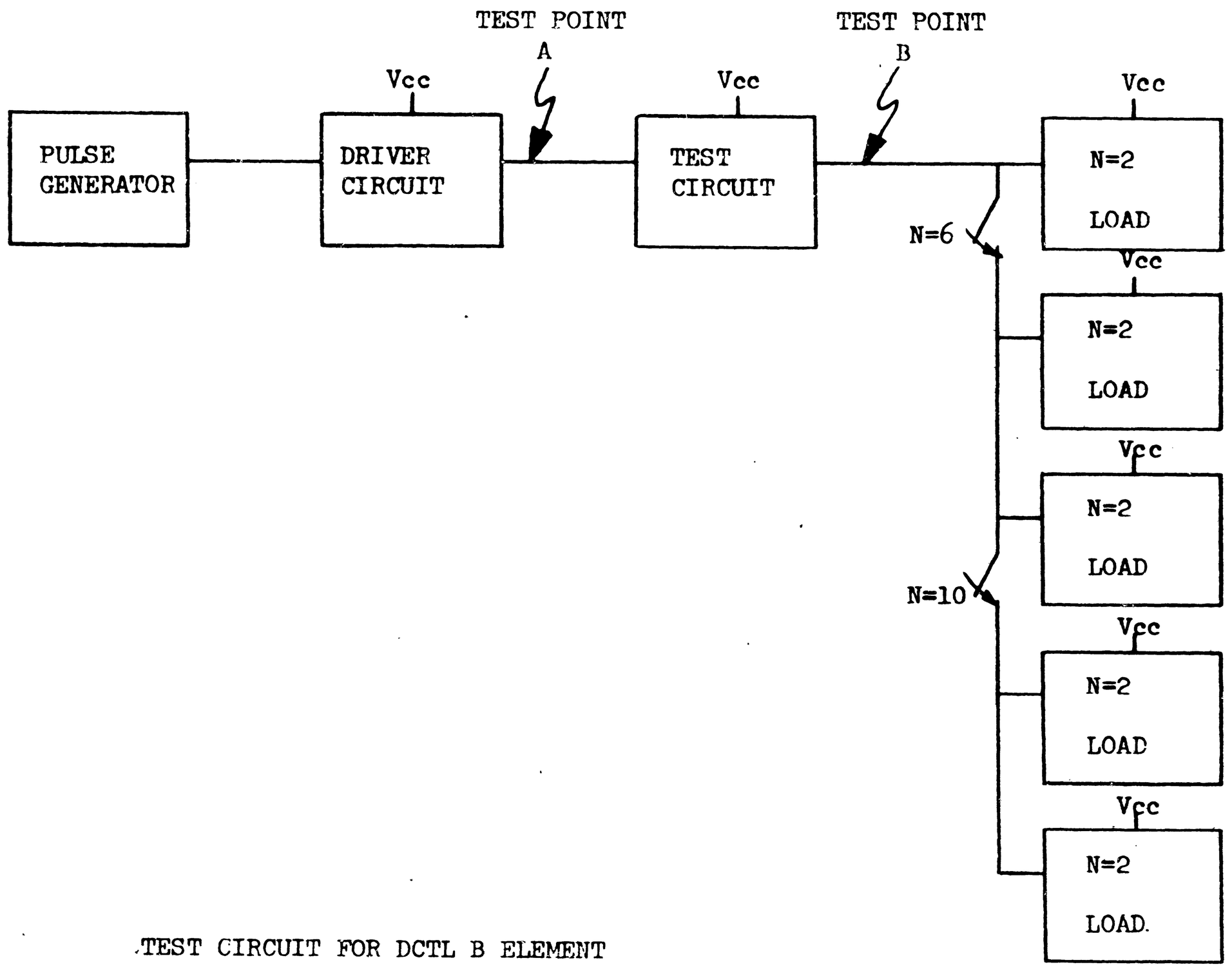


"0" to pin 2 and 3
NOTE: 100K resistor between pin 6 and pin 4

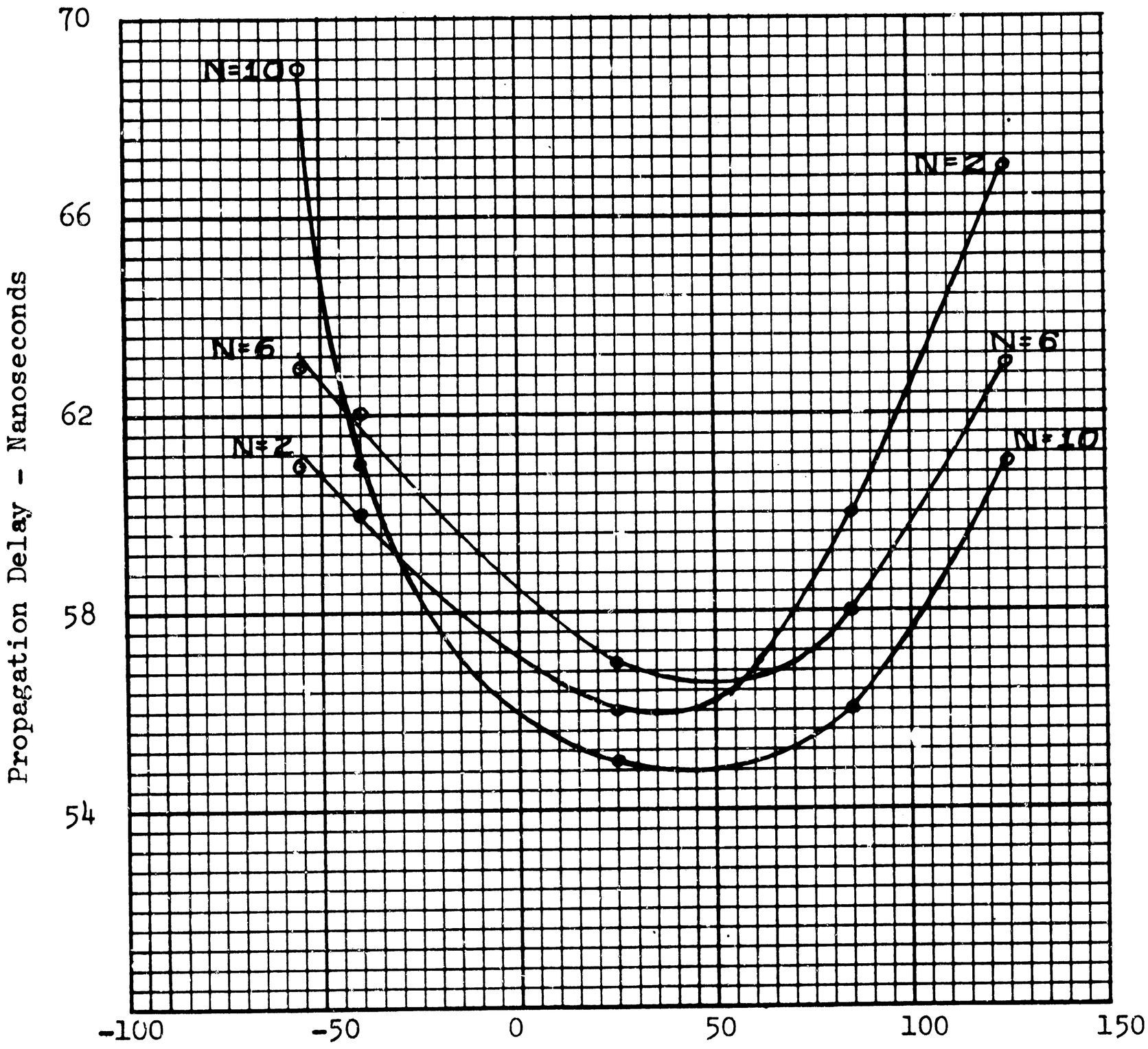
0.5 V/div.
Supply Voltage on Pin 8

OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL B ELEMENT

3.2.47



TEST CIRCUIT FOR DCTL B ELEMENT



READINGS TAKEN WITH SUPPLY VOLTAGES AT +3.0

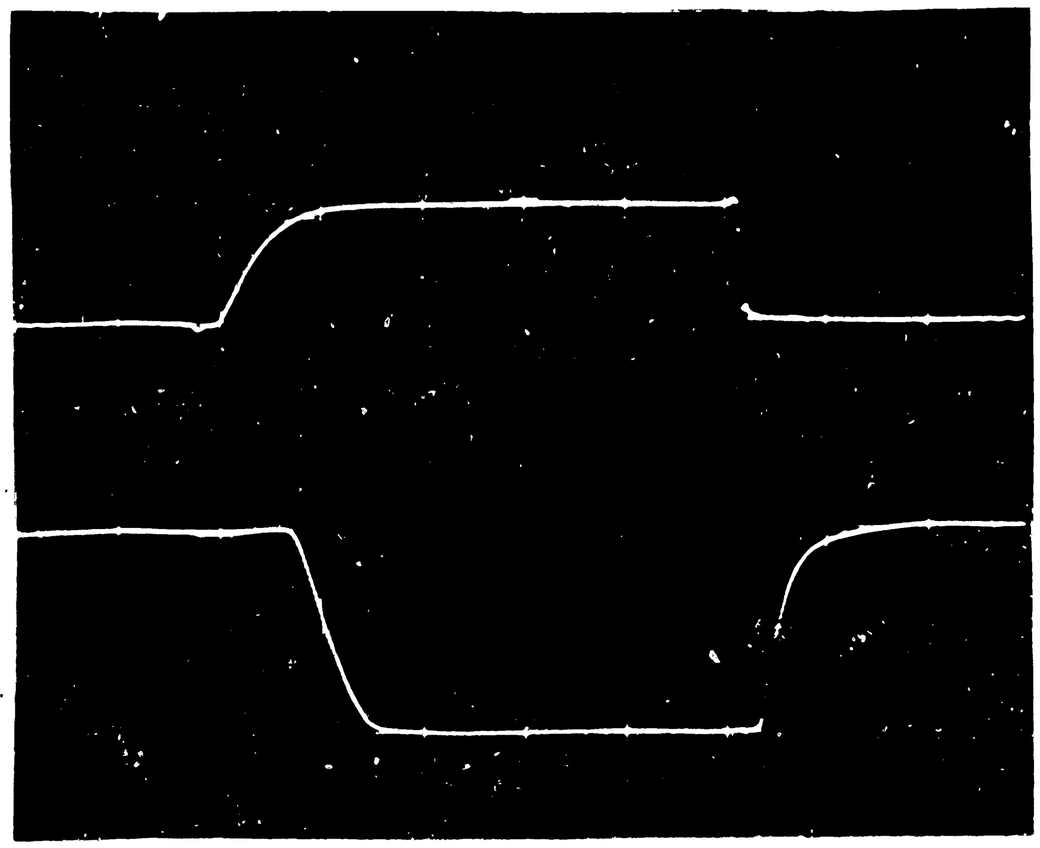
DCTL B ELEMENT

3.2.49

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	469.	462.	458.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.20	1.12	2.06	3.0
T_r	71.	48.	58.	64.
T_f	11.	46.	60.	76.
T_d		75.	75.	76.
T_s		28.	23.	21.
T_{pd}		55.	56.	62.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	456.	446.	438.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.27	1.02	1.88	2.79
T_r	74.	42.	45.	49.
T_f	11.	50.	67.	89.
T_d		85.	85.	88.
T_s		28.	23.	21.
T_{pd}		61.	60.	65

Type RTL No. B Temp. -55°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	451.	440.	430.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.28	0.97	1.85	2.74
T_r	76.	41.	45.	48.
T_f	11.	52.	71.	96.
T_d		89.	88.	90.
T_s		29.	24.	19.
T_{pd}		64.	61.	66.

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +85 Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	476.	472.	468.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.11	1.20	2.08	2.98
T_r	77.	54.	63.	68.
T_f	11.	46.	57.	71.
T_d		73.	74.	75.
T_s		30.	26.	24.
T_{pd}		55.	60.	65.

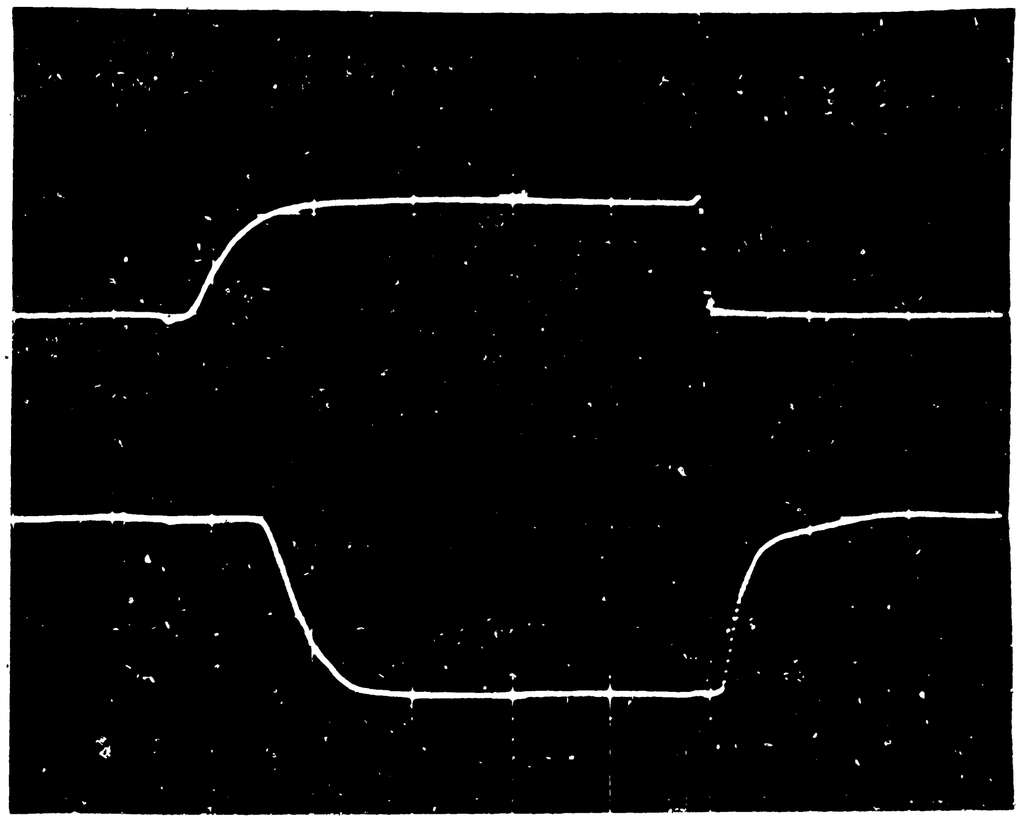
Type RTL No. B Temp. +125°C Vcc 3.0 N = 2

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	477.	477.	475.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.03	1.24	2.22	3.11
T_r	83.	69.	84.	90.
T_f	11.	54.	71.	86.
T_d		75.	73.	74.
T_s		31.	27.	25.
T_{pd}		60.	67.	73.

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	467.	459.	453.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.19	1.06	1.82	2.52
T_r	74.	54.	68.	61.
T_f	11.	59.	69.	79.
T_d		76.	77.	79.
T_s		29.	24.	22.
T_{pd}		57.	57.	61.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

3.2.53

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	446.	444.	434.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.27	0.93	1.65	2.38
T_r	77.	40.	53.	64.
T_f	11.	68.	82.	98.
T_d		86.	87.	88.
T_s		29.	24.	21.
T_{pd}		67.	62.	65.

Type RTL No. B Temp. -55°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	438.	439.	427.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.30	0.92	1.62	2.35
T_r	77.	41.	50.	60.
T_f	11.	74.	88.	105.
T_d		91.	90.	92.
T_s		30.	24.	19.
T_{pd}		73.	63.	65.

3.2.54

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +85°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	476.	469.	464.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.11	1.12	1.84	2.51
T_r	76.	63.	60.	66.
T_f	11.	64.	67.	74.
T_d		72.	74.	75.
T_s		30.	26.	23.
T_{pd}		55.	58.	62.

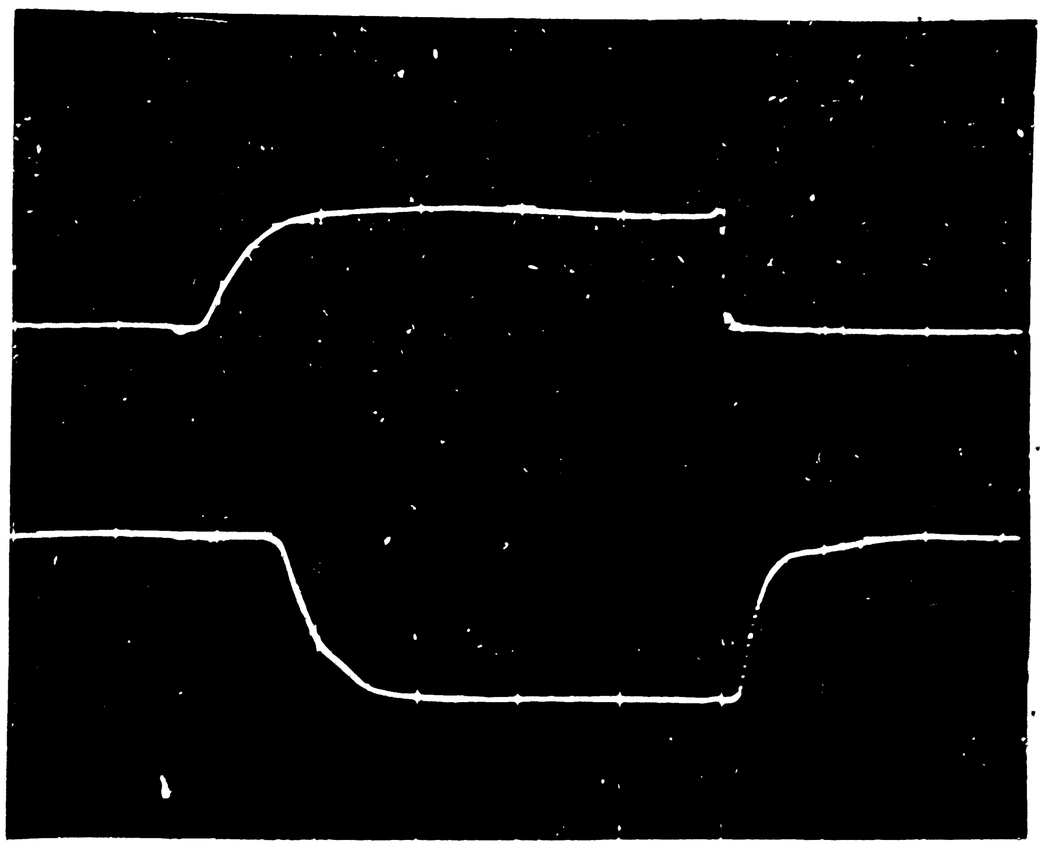
Type RTL No. B Temp. +125°C Vcc 3.0 N = 6

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	478.	473.	469.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.02	1.12	1.78	2.46
T_r	82.	70.	76.	87.
T_f	11.	78.	75.	82.
T_d		74.	75.	75.
T_s		32.	27.	25.
T_{pd}		60.	63.	69.

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +25°C Vcc +3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	464.	458.	451.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.20	0.98	1.64	2.20
T_r	76.	48.	55.	69.
T_f	11.	72.	79.	87.
T_d		77.	78.	79.
T_s		29.	24.	22.
T_{pd}		58.	55.	59.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

3.2.56

GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. -40°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	430.	443.	433.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.29	0.86	1.52	212.
T_r	80.	34.	48.	69.
T_f	12.	84.	94.	109.
T_d		88.	86.	87.
T_s		30.	24.	22.
T_{pd}		75.	61.	63.

Type RTL No. B Temp. -55°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	419.	438.	426.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.31	0.86	1.47	2.03
T_r	83.	34.	42.	61.
T_f	12.	90.	103.	116.
T_d		92.	92.	92.
T_s		31.	25.	21.
T_{pd}		81.	69.	65.

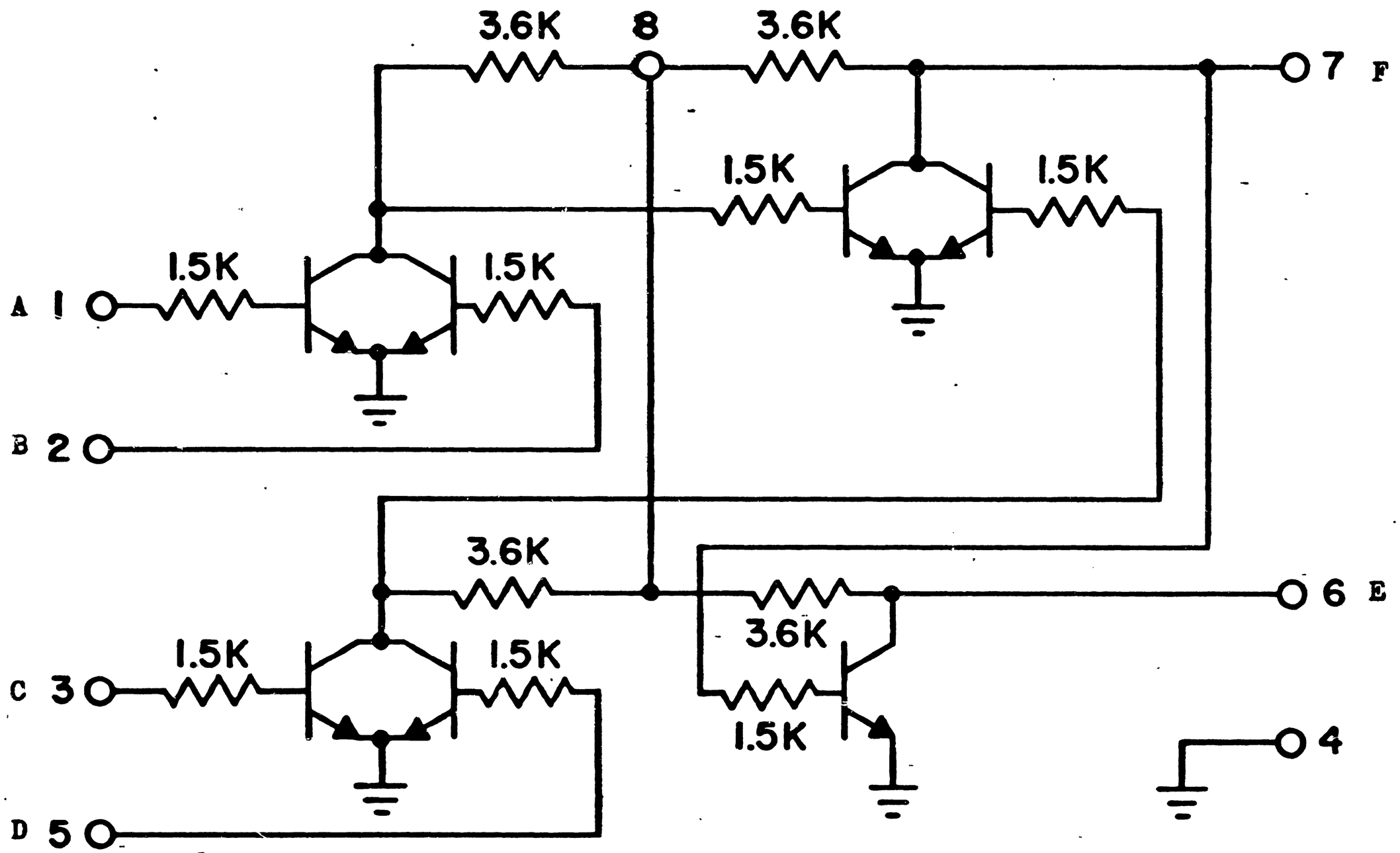
GENERAL MICRO-ELECTRONICS

Type RTL No. B Temp. +85°C Vcc 3.0 N = 10

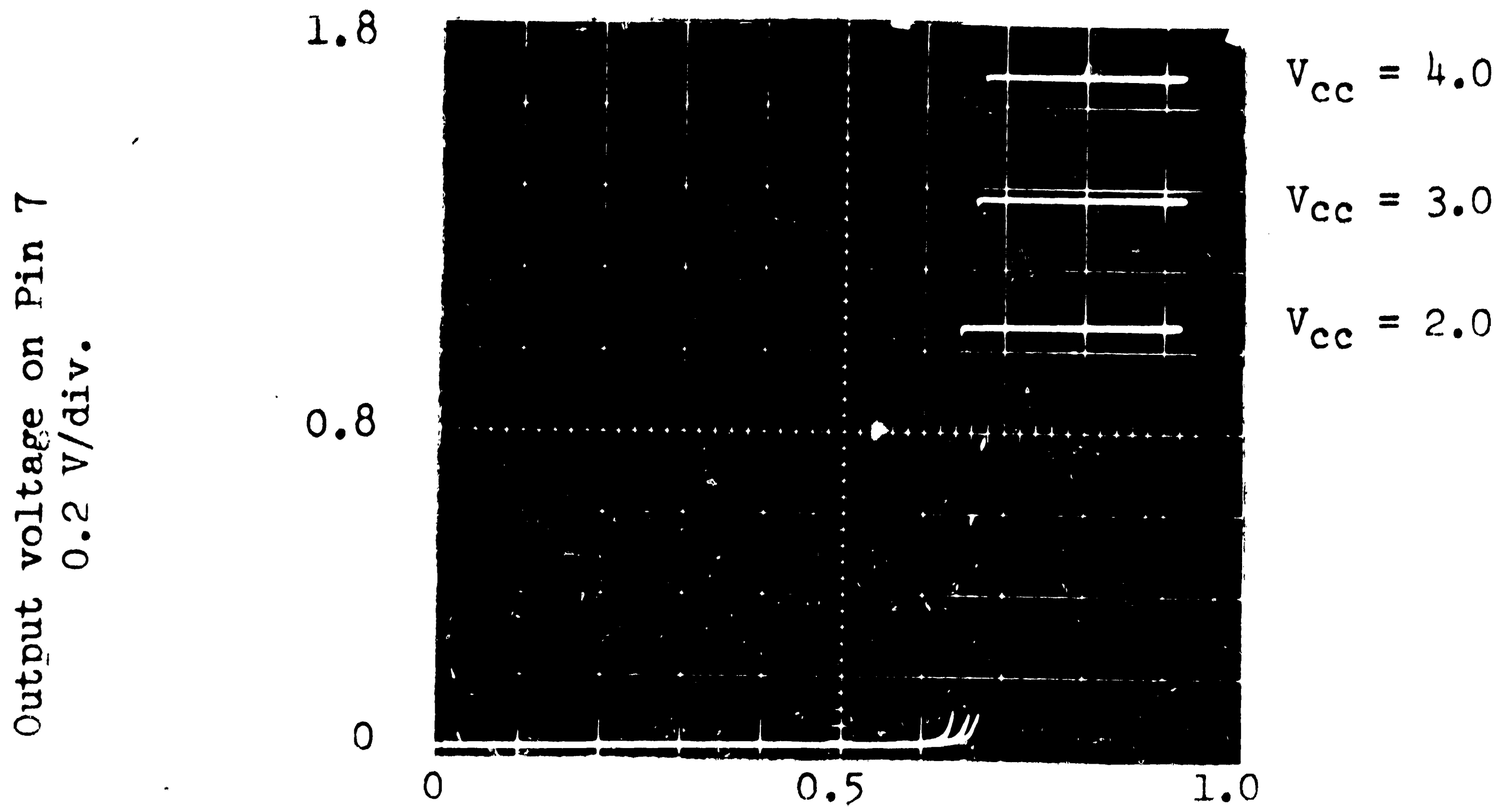
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	477.	468.	464.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.10	1.02	1.60	2.15
T_r	80.	54.	65.	90.
T_f	11.	81.	83.	85.
T_d		72.	73.	73.
T_s		31.	26.	23.
T_{pd}		55.	56.	65.

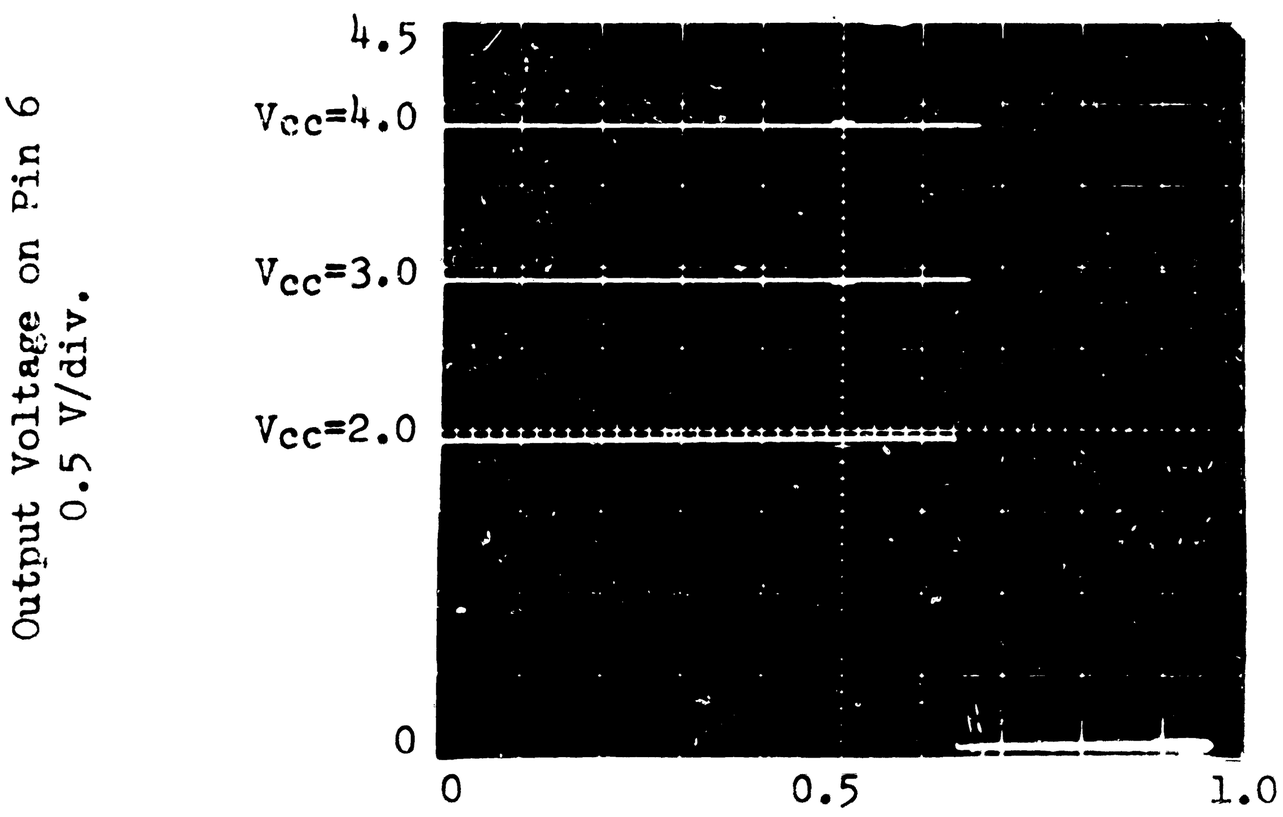
Type RTL No. B Temp. +125°C Vcc 3.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	476.	469.	467.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	51.	0.98	1.54	2.10
T_r	87.	61.	82.	102.
T_f	11.	99.	97.	91.
T_d		74.	73.	73.
T_s		32.	27.	25.
T_{pd}		58.	61.	66.



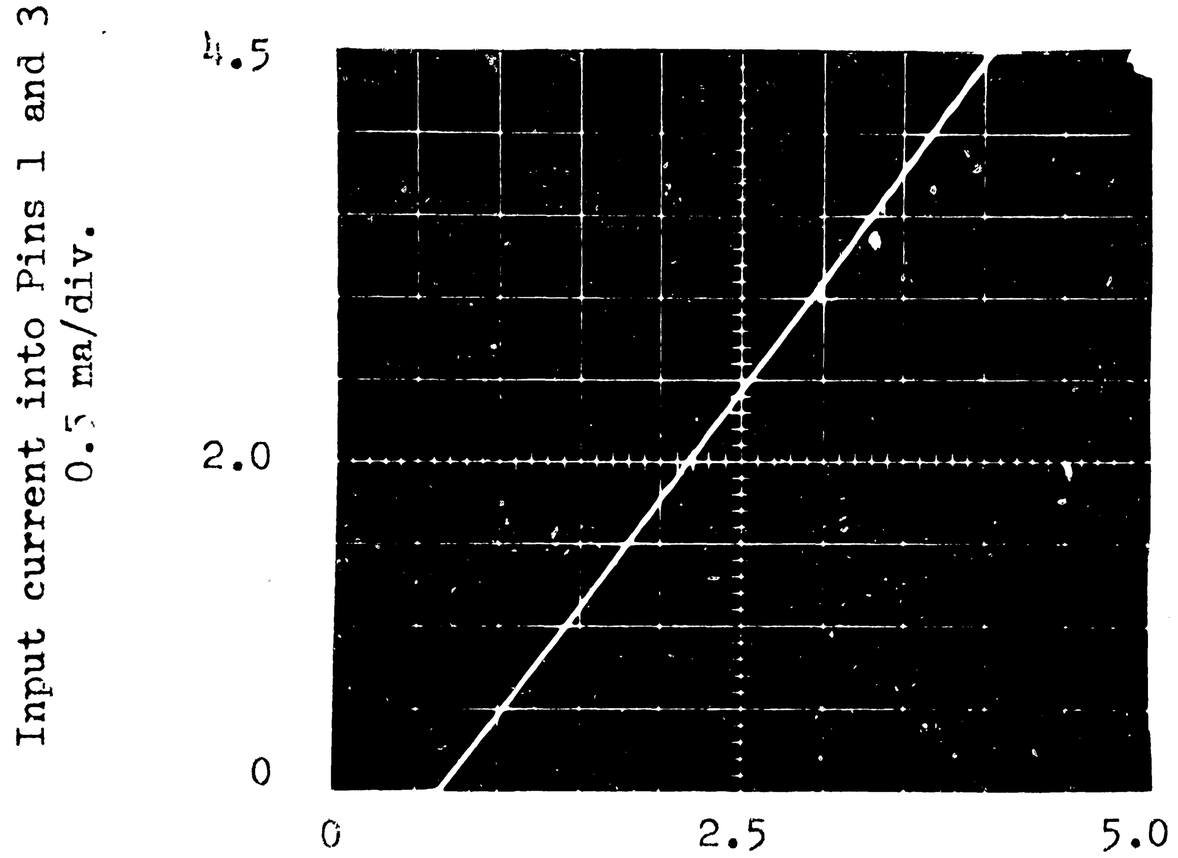
DCTL EXCLUSIVE OR ELEMENT, HALF ADDER, H



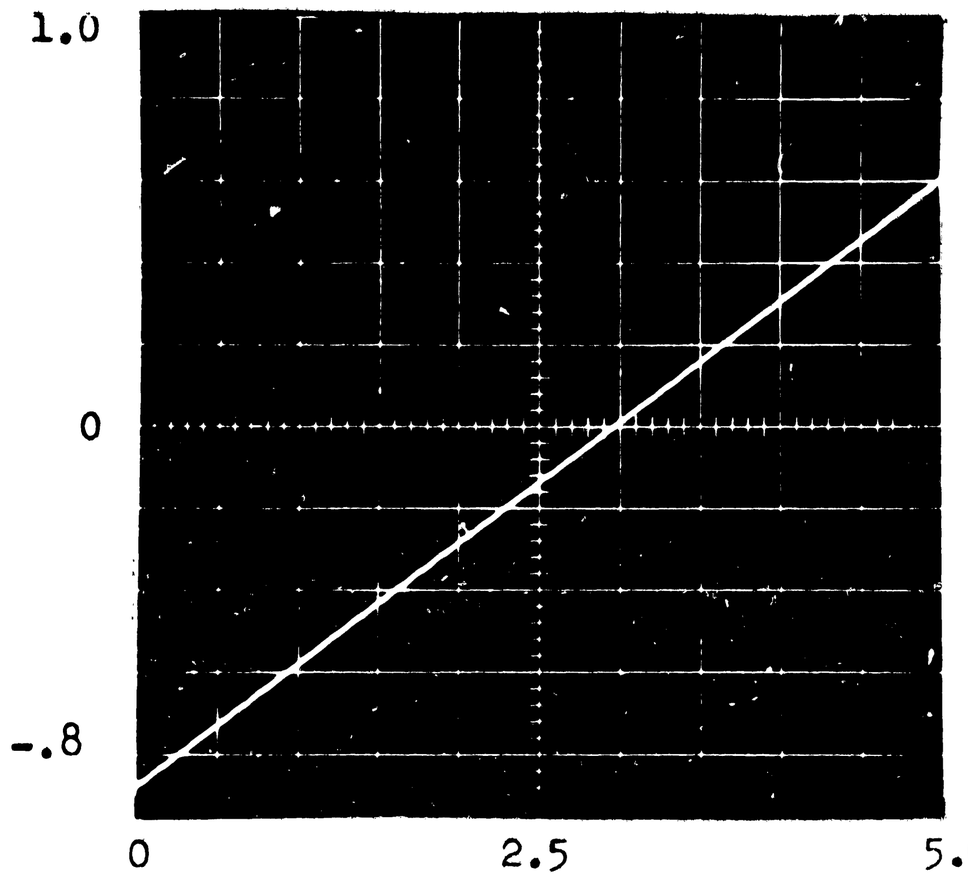


INPUT - OUTPUT CHARACTERISTICS
DCTL H ELEMENT

3.2.60

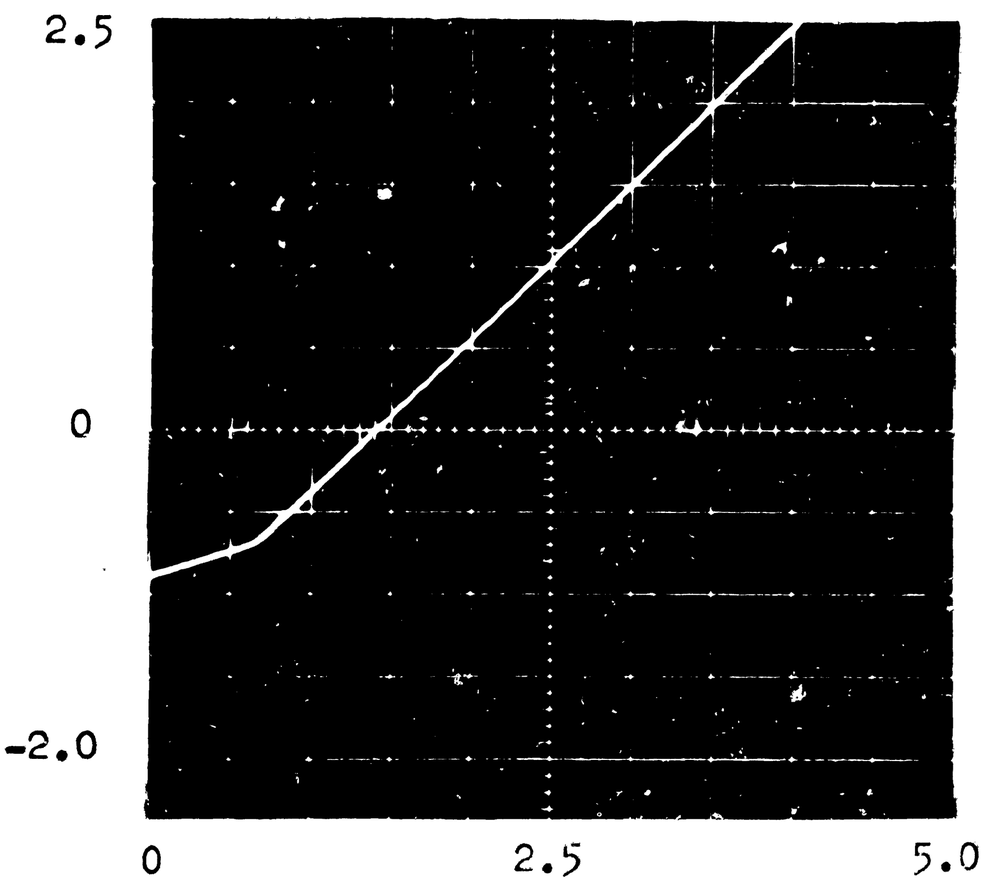


INPUT CHARACTERISTICS
DCTL H ELEMENT



Output current into Pin 6
0.2 ma/div.

0.5 V/div
Output Voltage on Pin 6

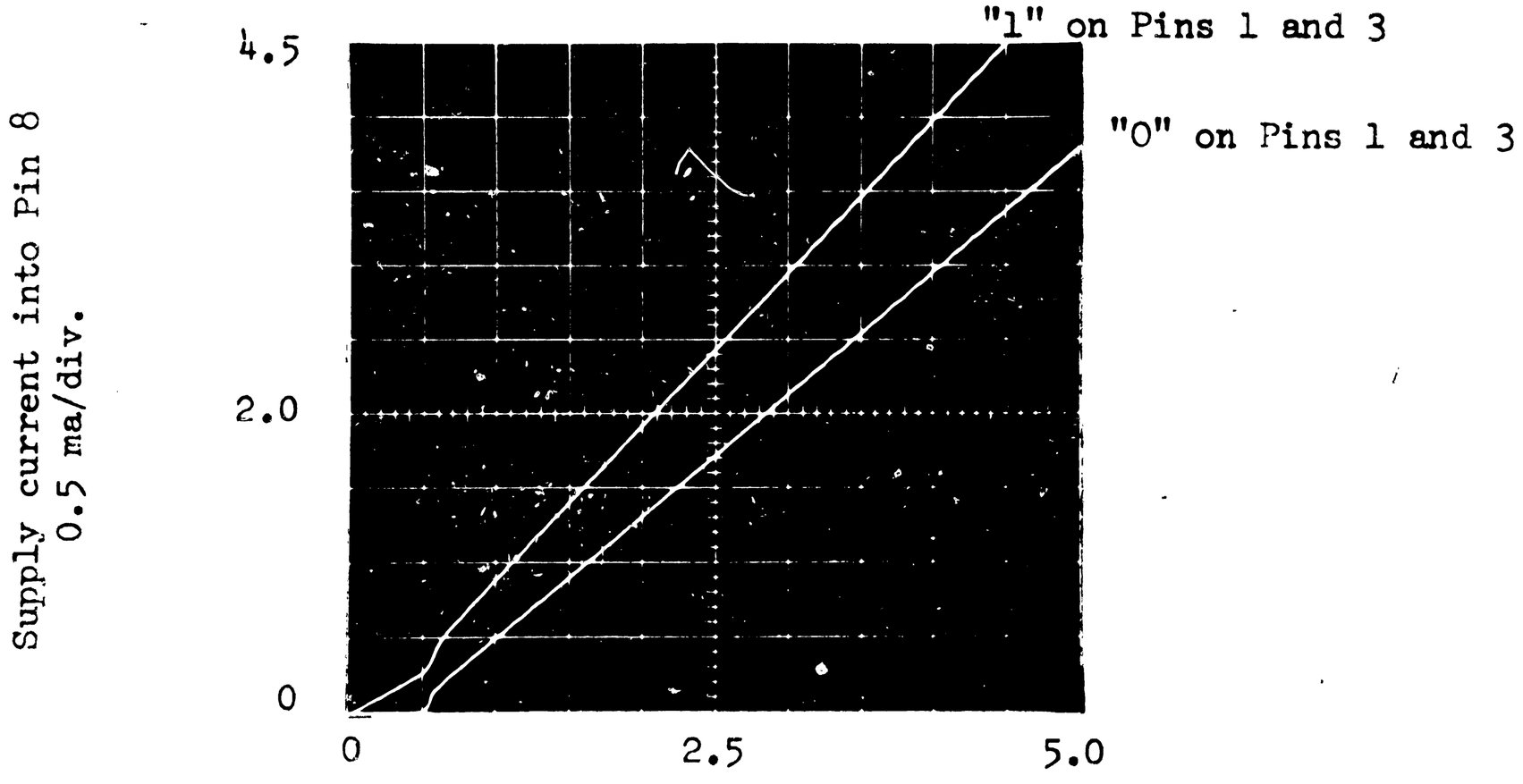


Output current into Pin 7
0.5 ma/div.

0.5 V/div.
Output Voltage on Pin 7

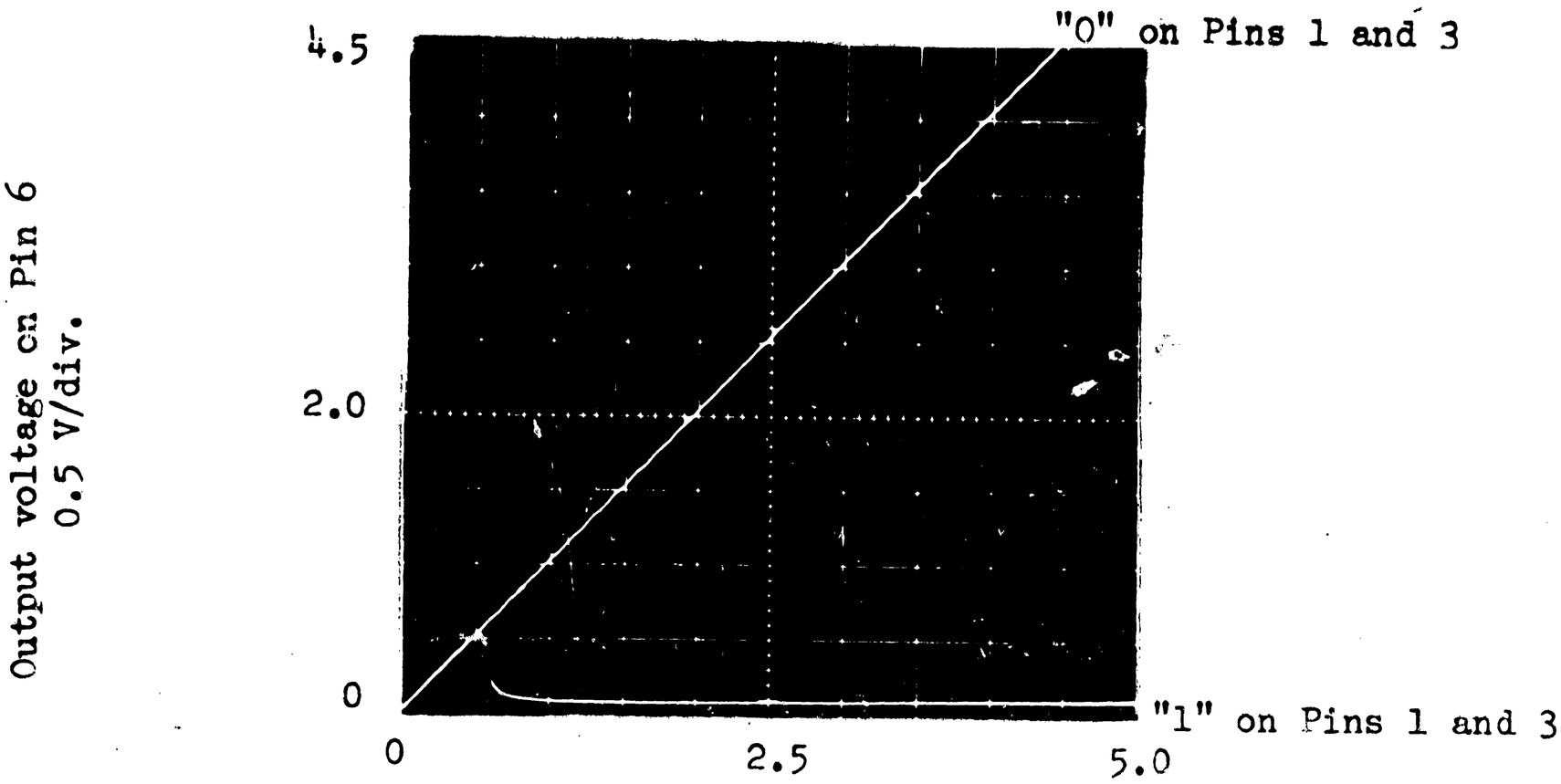
OUTPUT CHARACTERISTICS
DCTL H ELEMENT

3.2.62

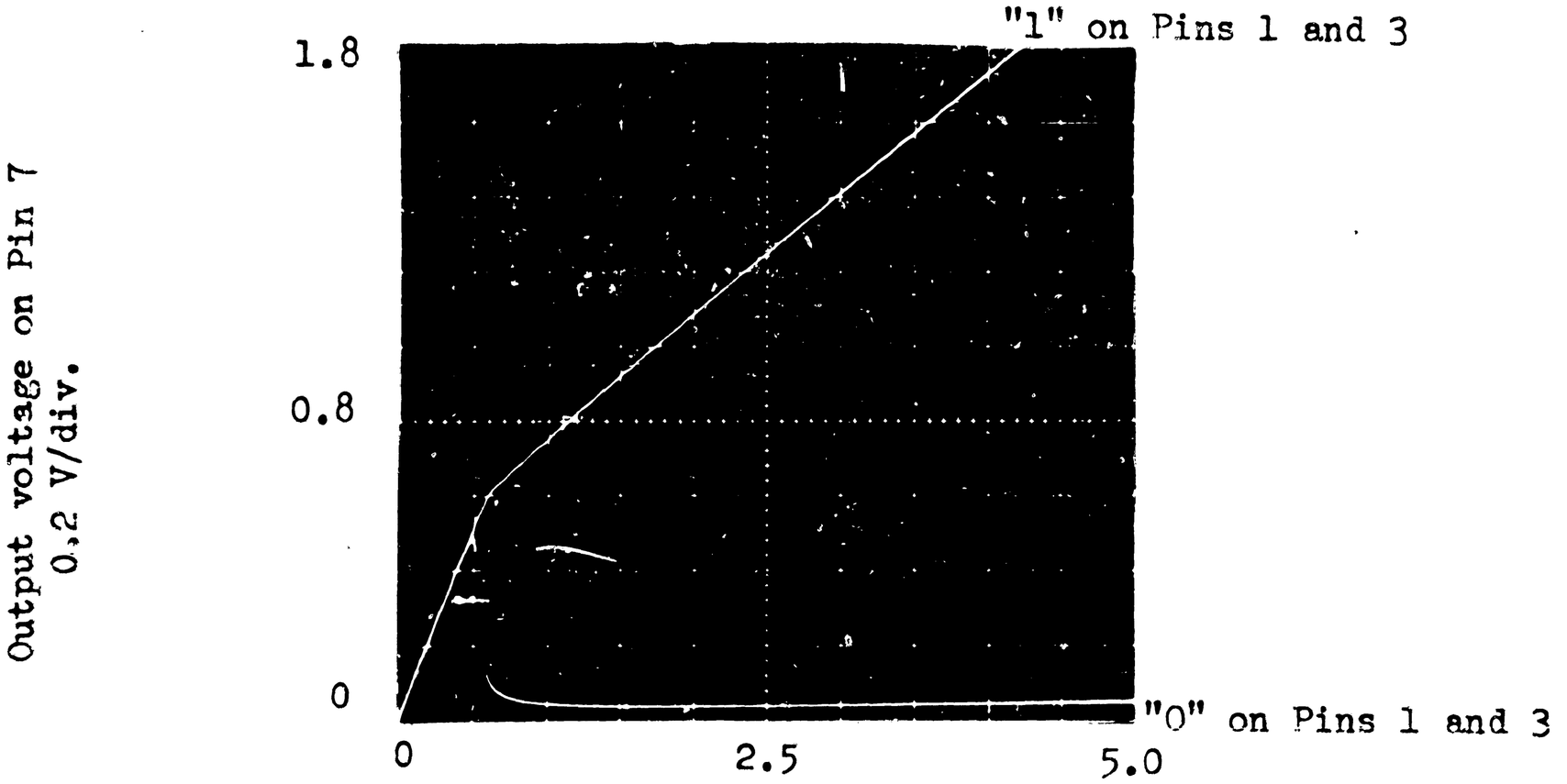


POWER DISSIPATION
DCTL H ELEMENT

3.2.63



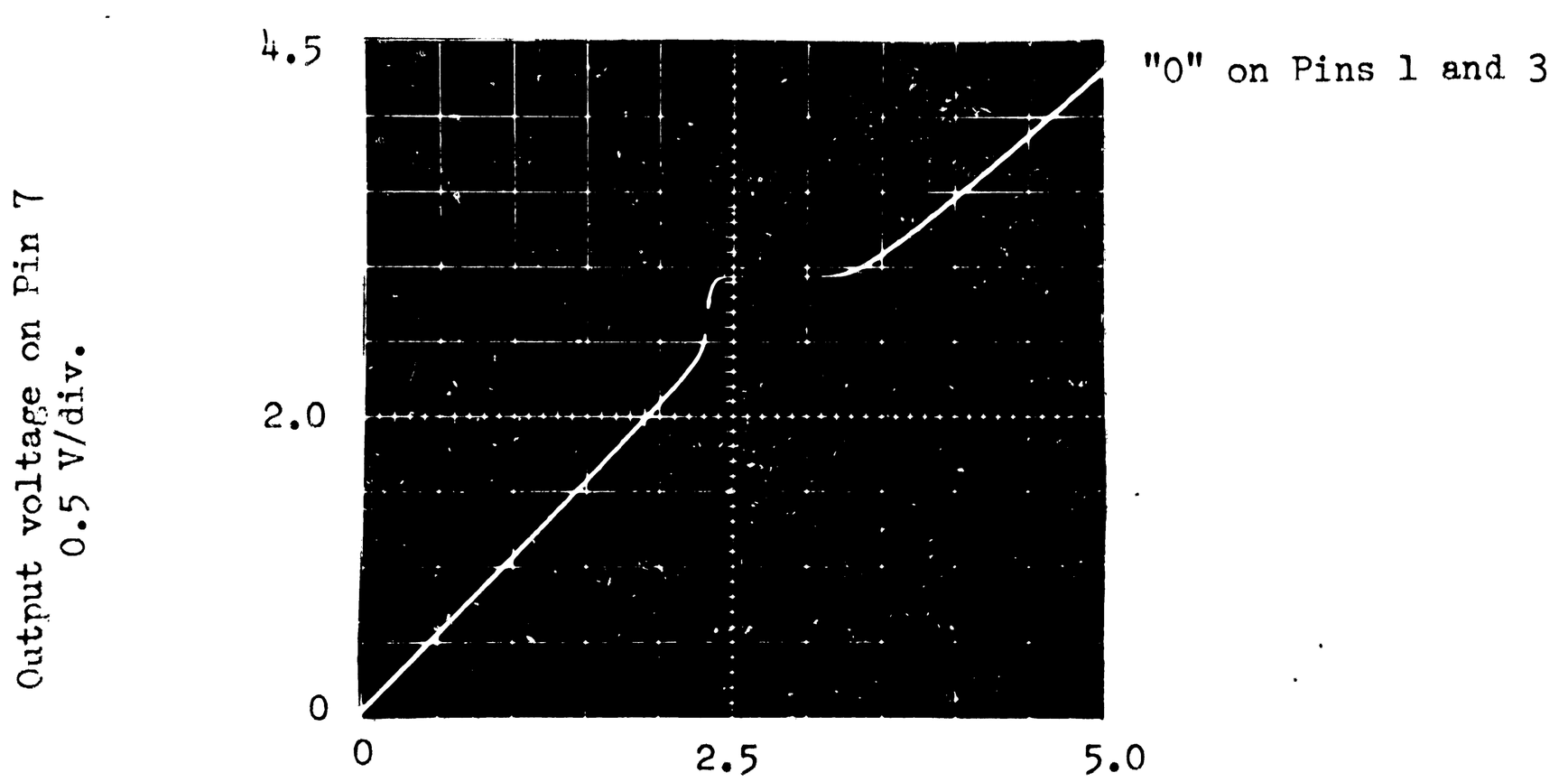
0.5 V/div.
Supply Voltage on Pin 8



0.5 V/div.
Supply Voltage on Pin 8

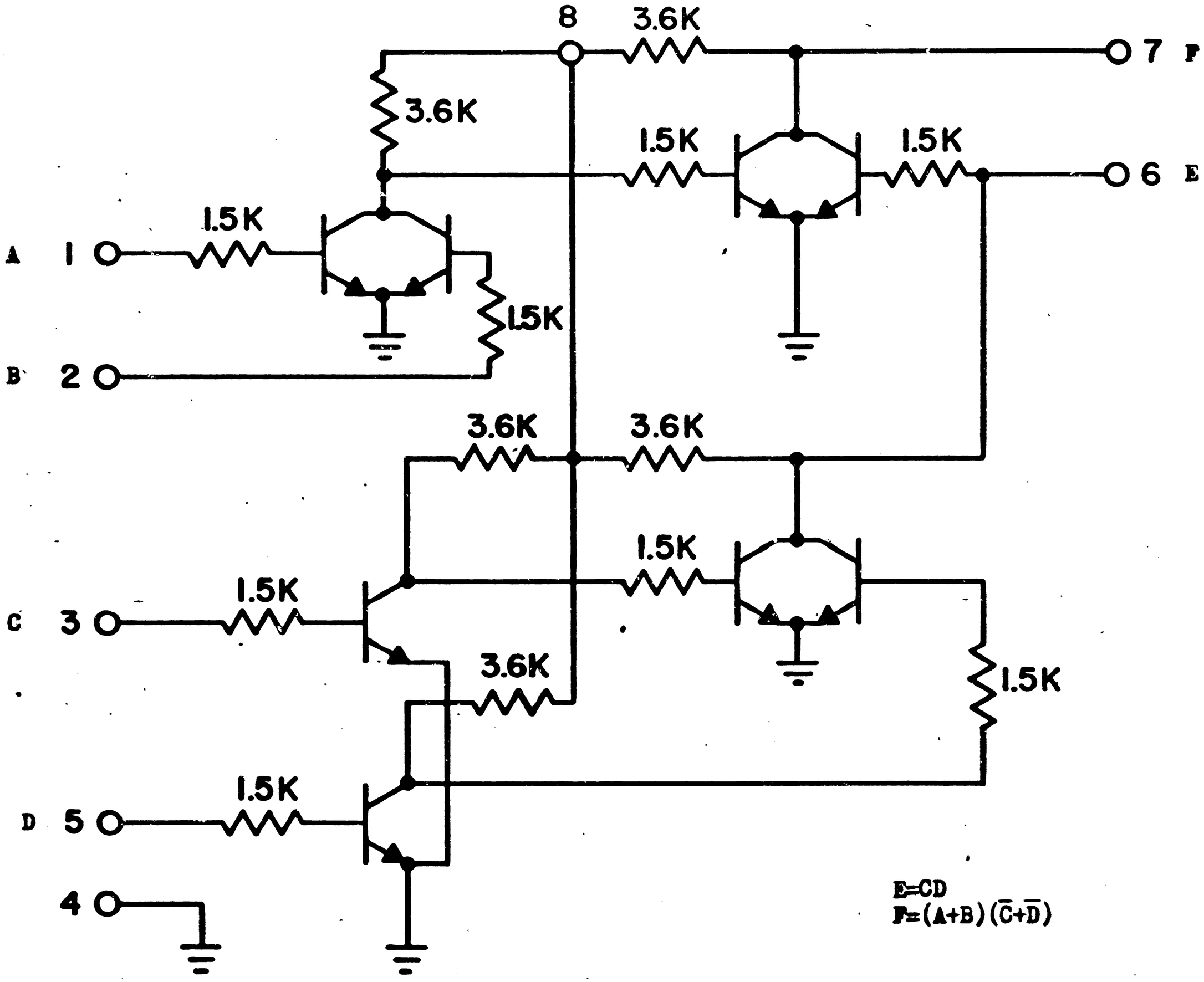
OUTPUT VOLTAGE versus SUPPLY VOLTAGES
DCTL H ELEMENT

3.2.64



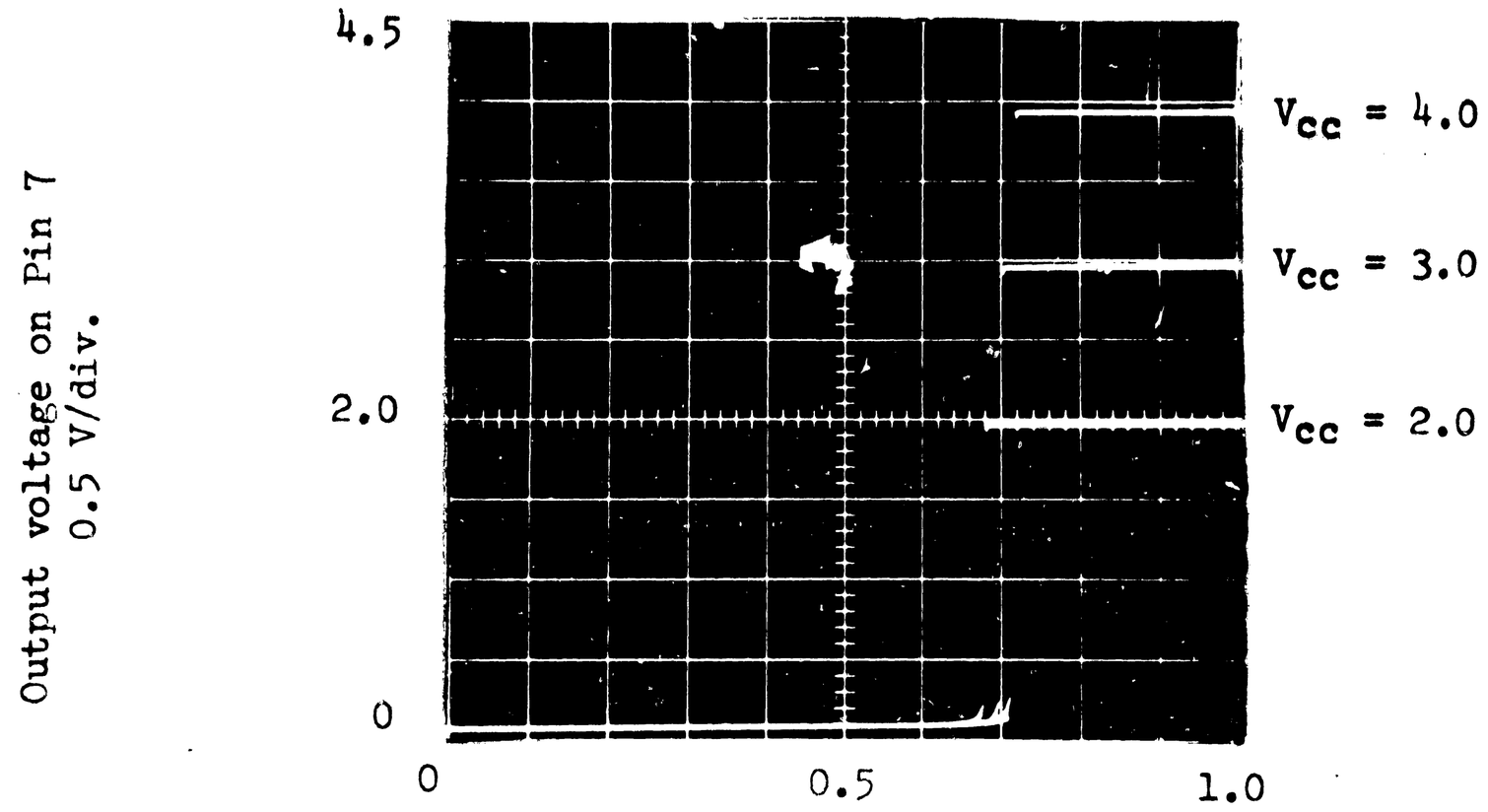
OUTPUT VOLTAGE versus GROUND NOISE VOLTAGE
DCTL II ELEMENT

3.2.65

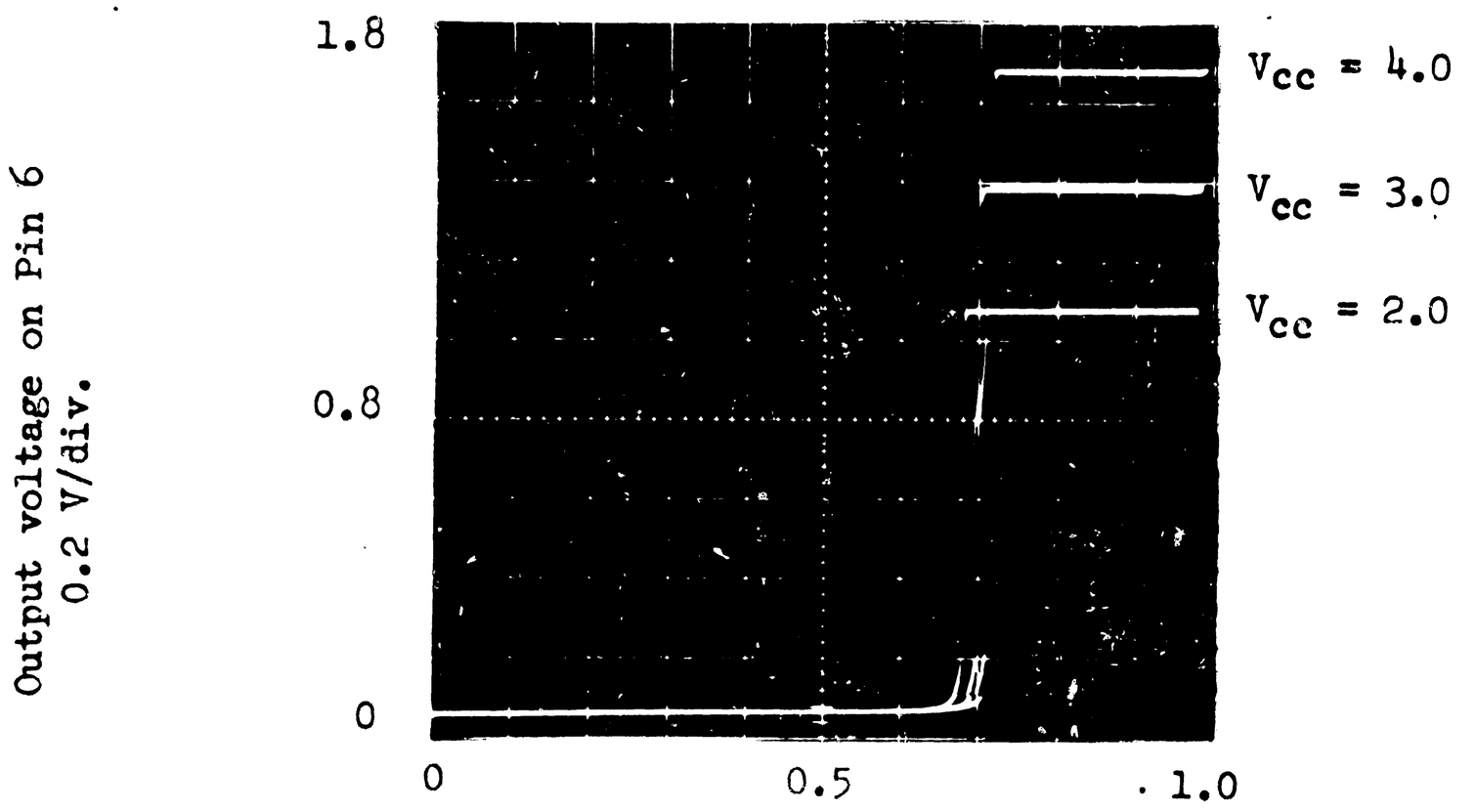


3.2.66

DCTL ADDER ELEMENT, A



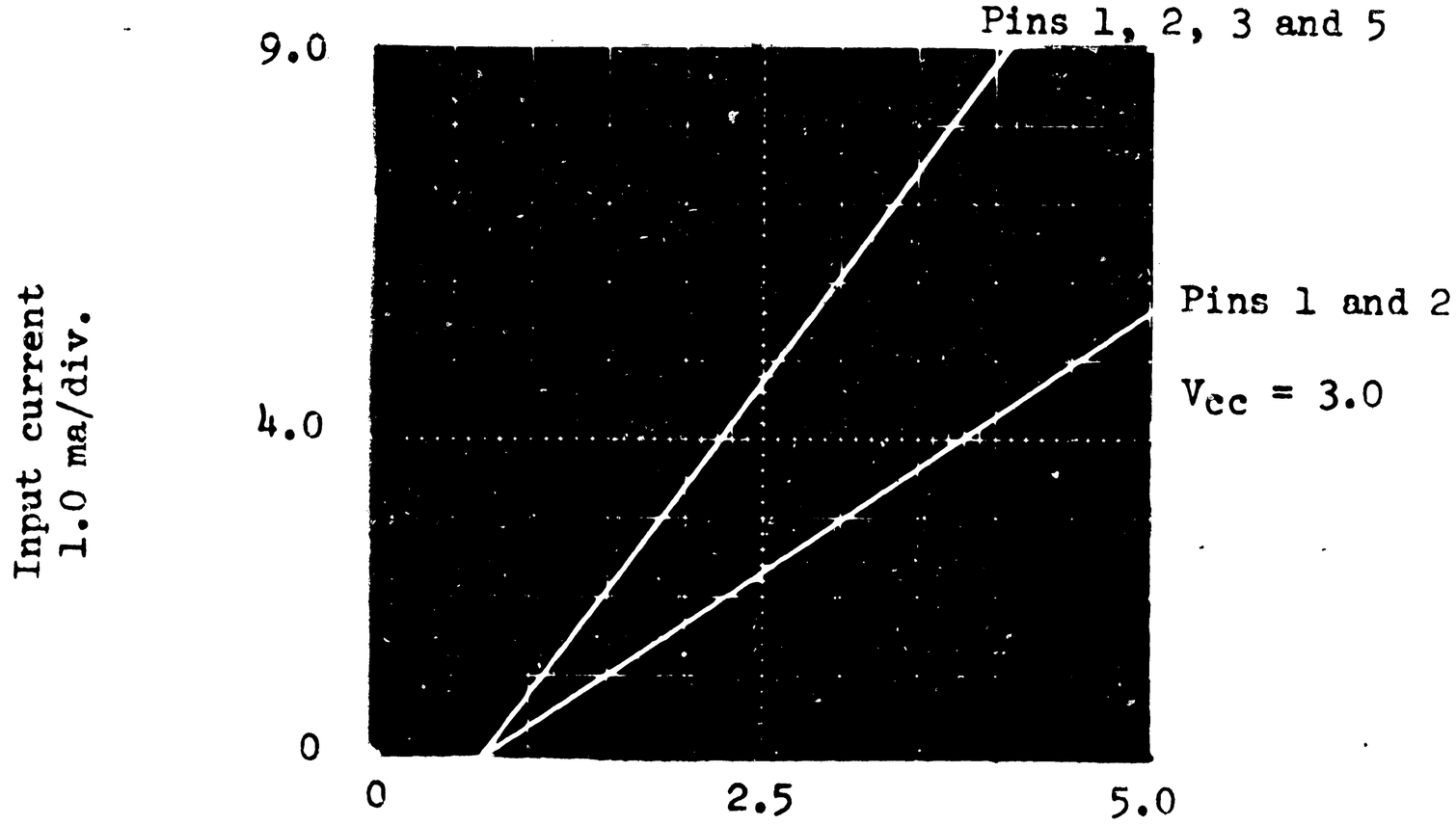
0.1 V/div.
Input Voltage on Pins 1 and 3



0.1 V/div.
Input Voltage on Pins 1, 2, 3 and 5

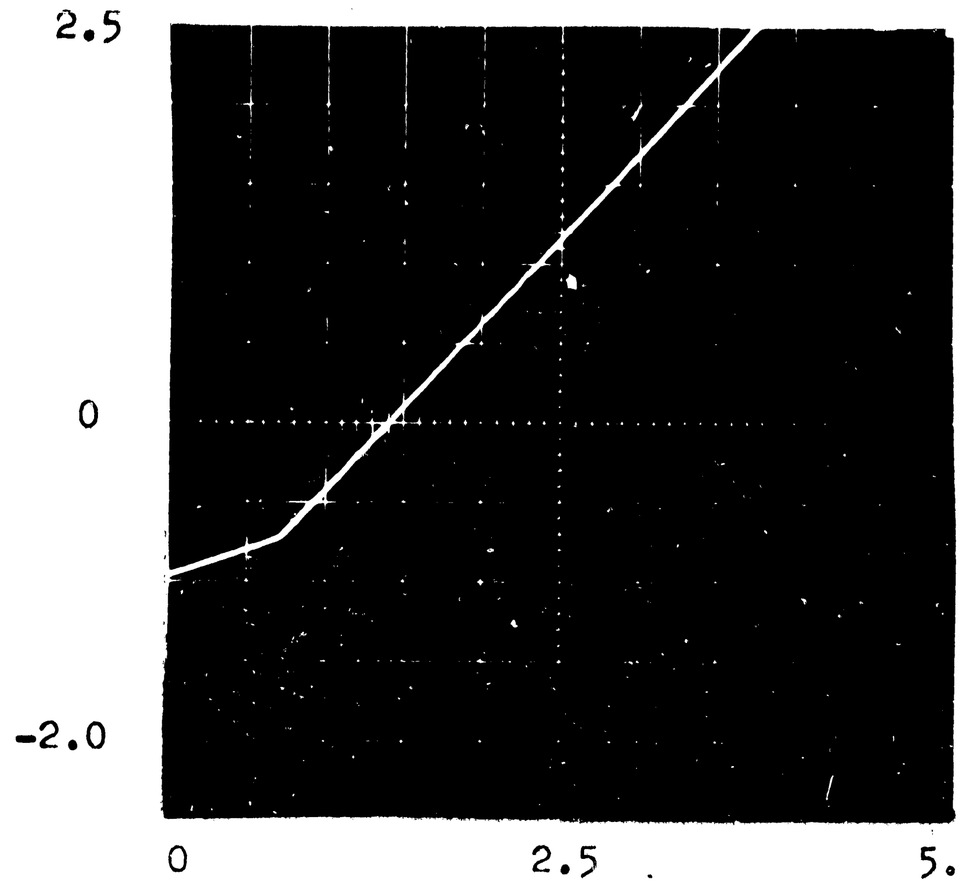
INPUT - OUTPUT CHARACTERISTICS
DCTL A ELEMENT

3.2.67

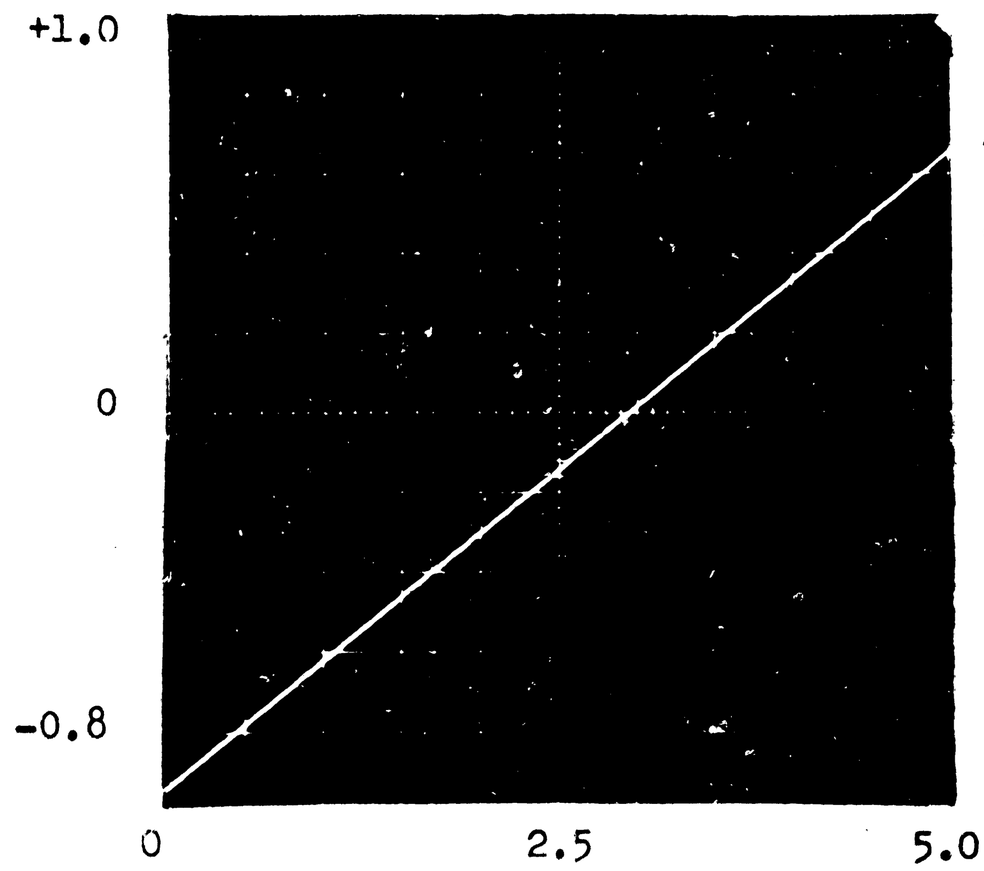


INPUT CHARACTERISTICS
DCTL A ELEMENT

3.2.68



0.5 V/div.
Output Voltage on Pin 6



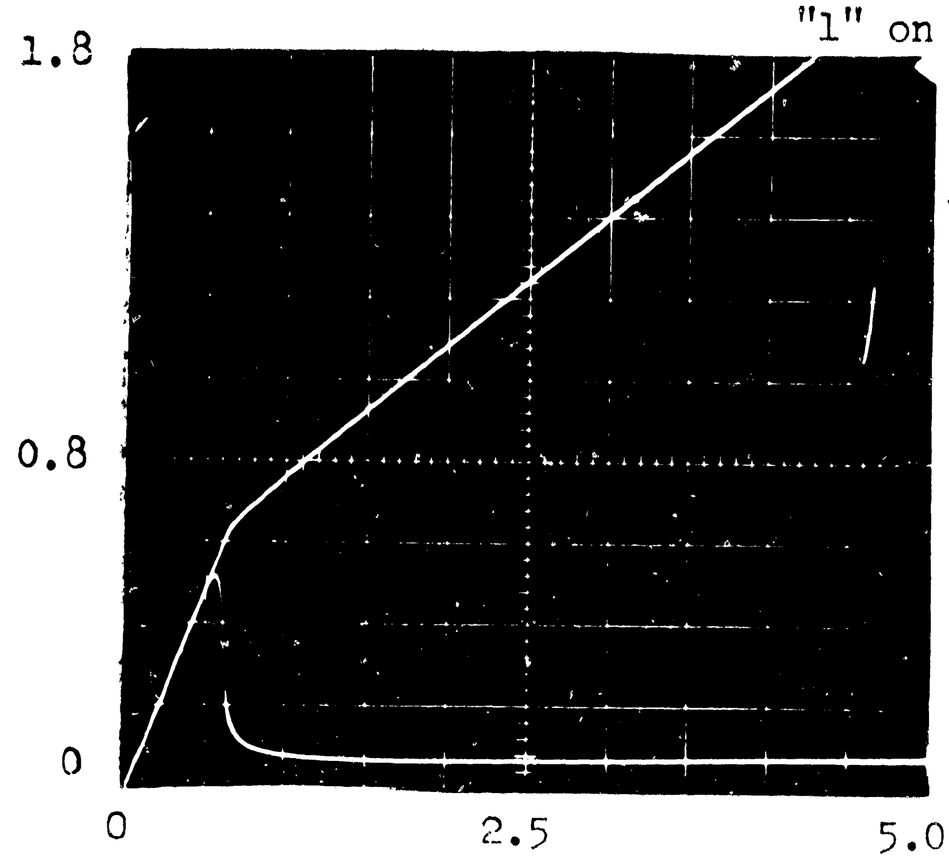
0.5 V/div.

Output Voltage on Pin 7

OUTPUT CHARACTERISITCS
DCTL A ELEMENT

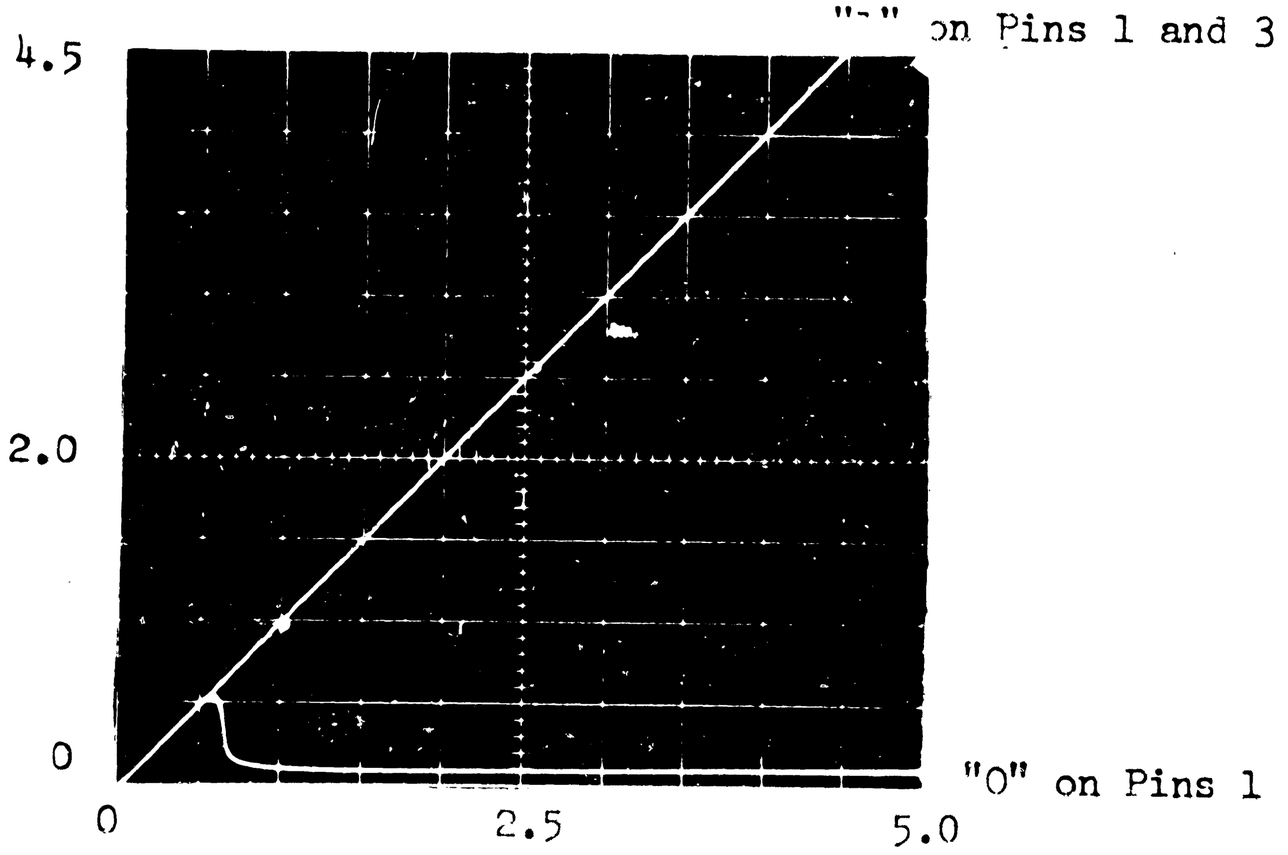
3.2.69

Output voltage on Pin 6
0.2 V/div.



0.5 V/div.
Supply Voltage on Pin 8

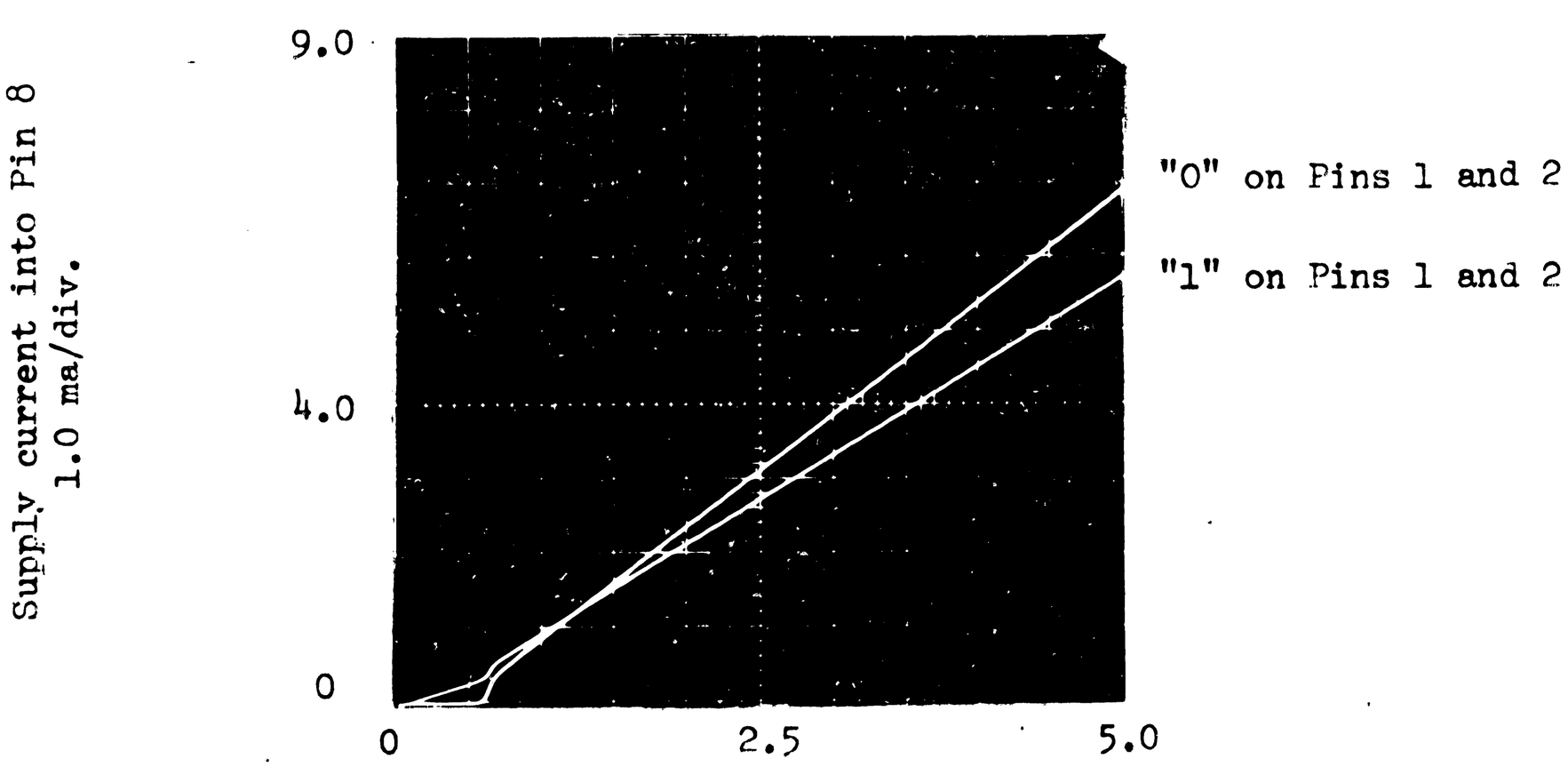
Output voltage on Pin 7
0.5 V/div.



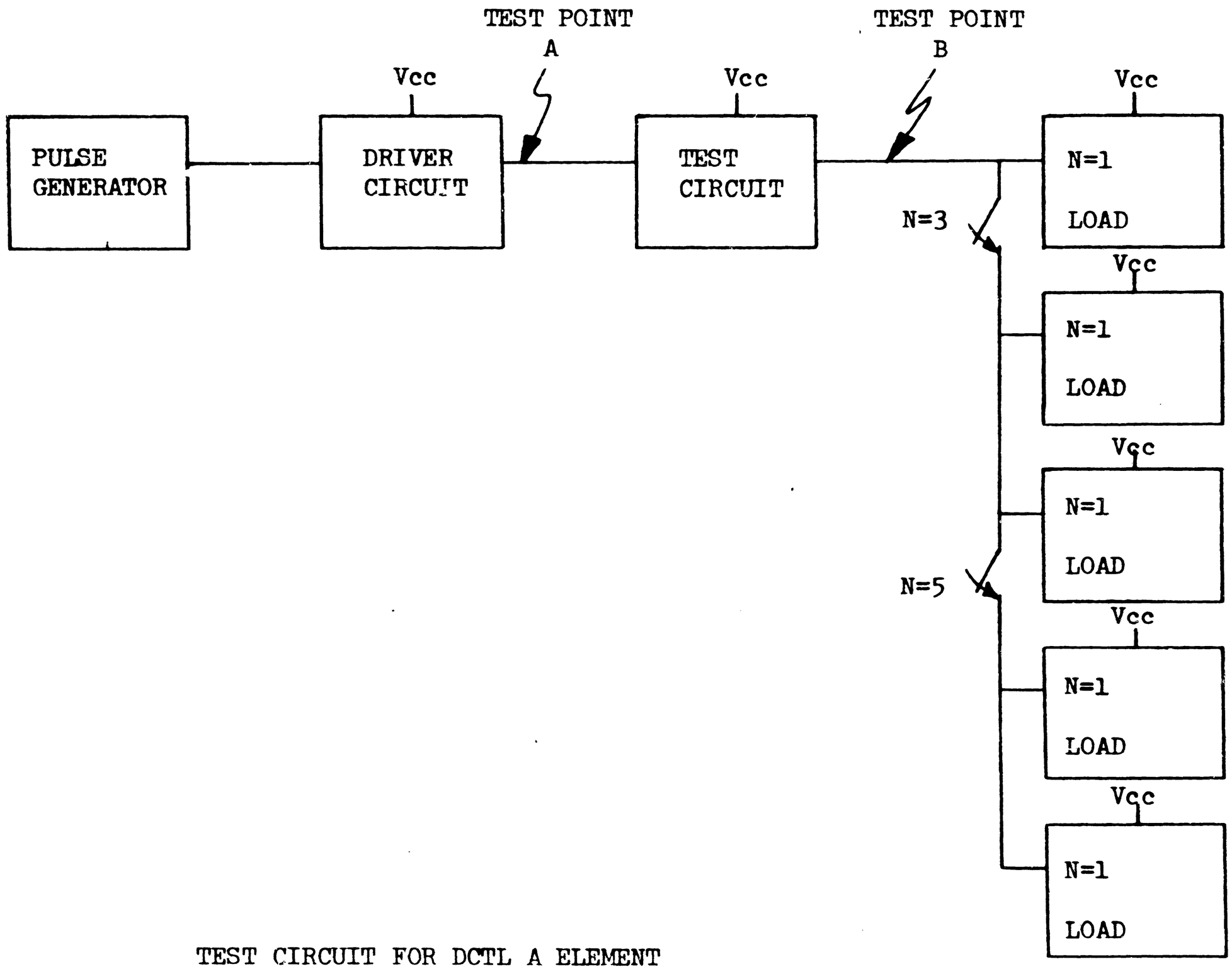
0.5 V/div.
Supply Voltage on Pin 8

OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DCTL A ELEMENT

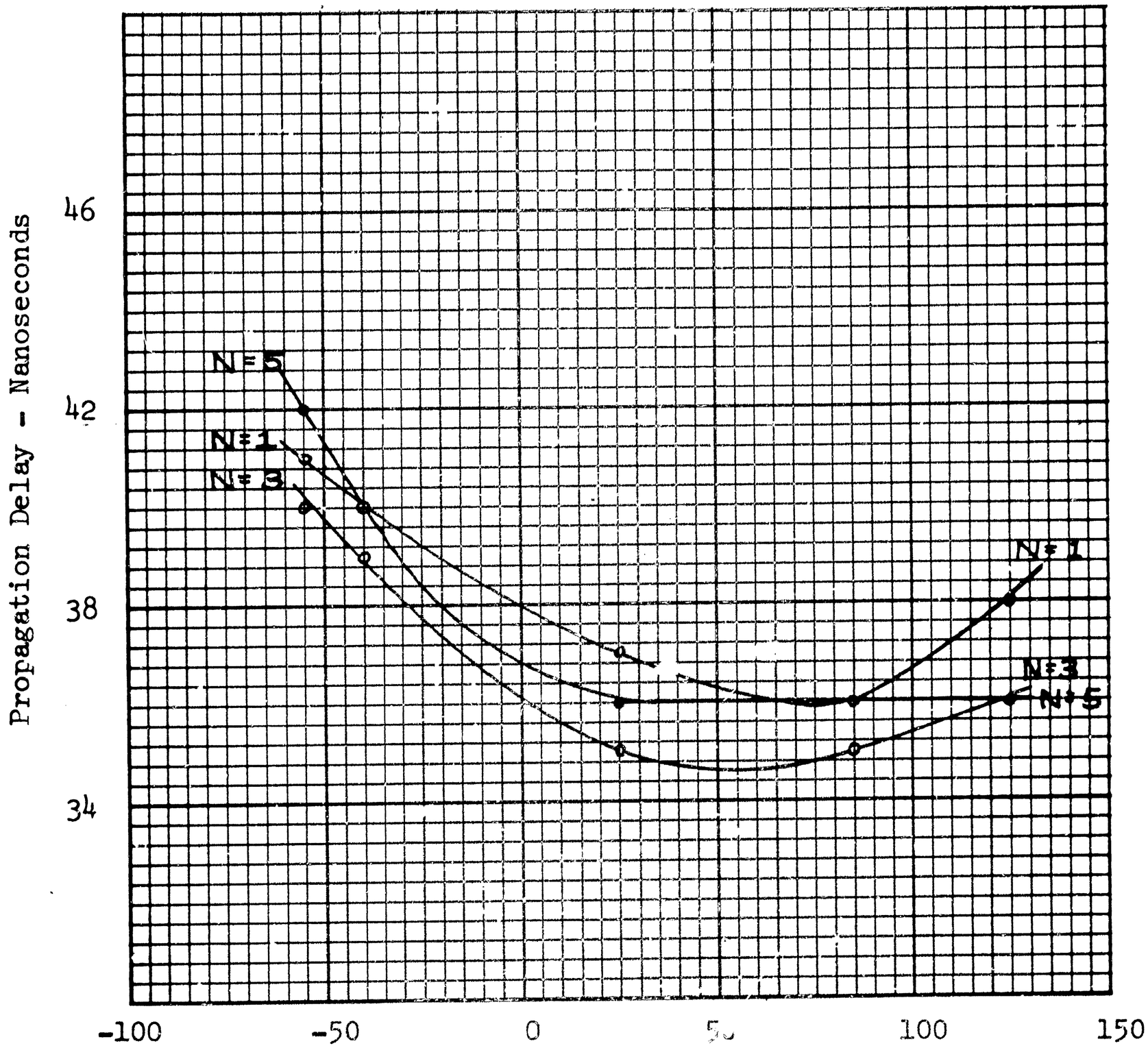
3.2.70



POWER DISSIPATION
DCTL A ELEMENT



TEST CIRCUIT FOR DCTL A ELEMENT



DATA FOR GRAPH TAKEN WITH TEST CIRCUIT AND LOAD SUPPLY AT 3.0 V

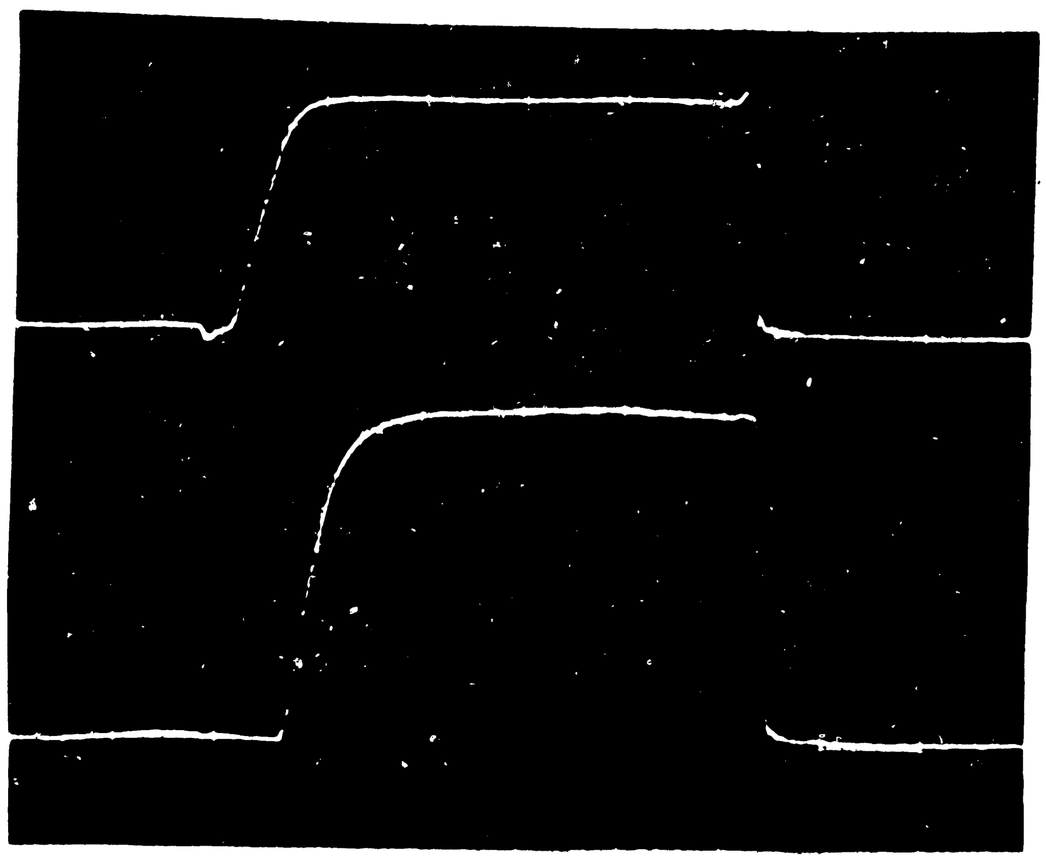
DCTL A ELEMENT

3.2.73

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	463.	450.	448.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.94	1.02	1.38	1.72
T_r	51.	80.	73.	66.
T_f	11.	16.	13.	12.
T_d		59.	60.	62.
T_s		20.	15.	12.
T_{pd}		42.	37.	35.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	460.	455.	452.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.04	1.10	1.40	1.72
T_r	53.	75.	65.	61.
T_f	11.	12.	9.	8.
T_d		61.	63.	65.
T_s		21.	15.	12.
T_{pd}		45.	40.	38.

Type RTL No. A Temp. -55°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	459.	454.	451.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.06	1.12	1.42	1.72
T_r	54.	76.	65.	61.
T_f	12.	13.	9.	9.
T_c		64.	65.	67.
T_s		22.	16.	12.
T_{pd}		42.	41.	40.

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	465.	460.	457.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.35	0.97	1.28	1.60
T_r	53.	76.	70.	67.
T_f	11.	13.	12.	12.
T_d		54.	56.	58.
T_s		20.	15.	13.
T_{pd}		40.	36.	35.

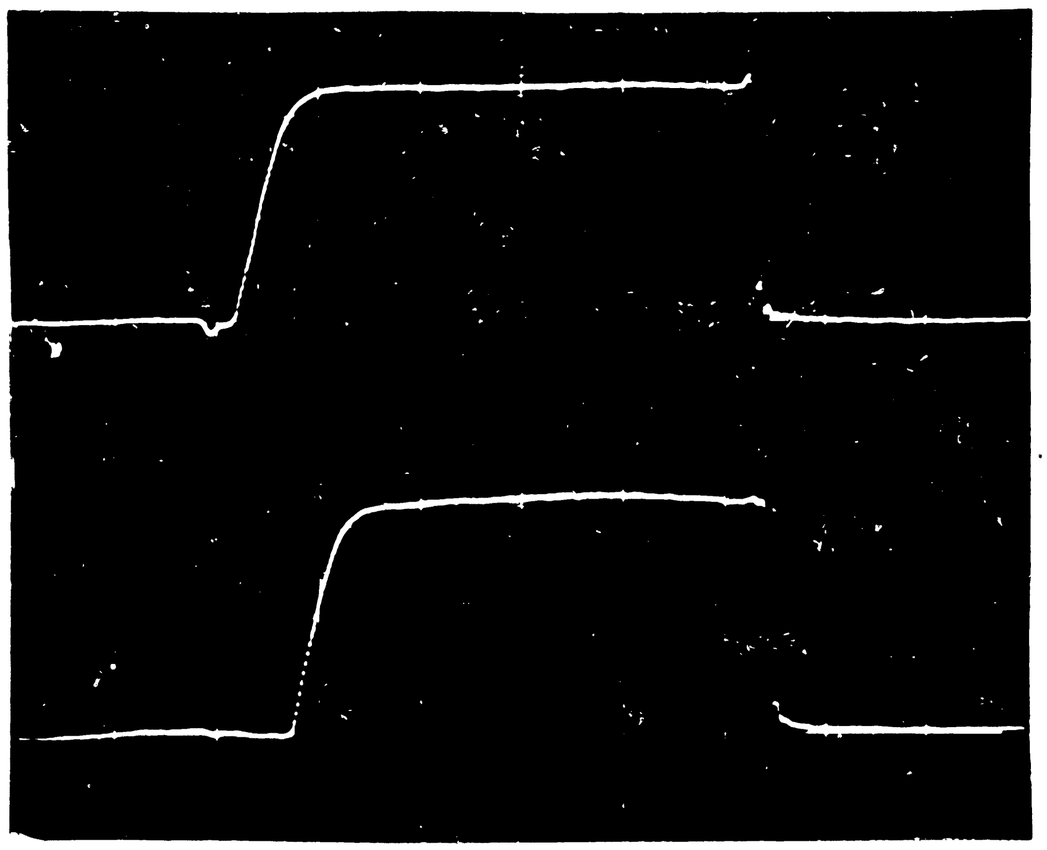
Type RTL No. A Temp. +125°C Vcc 3.0 = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	467.	462.	459.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.77	0.90	1.22	1.56
T_r	57.	81.	75.	72.
T_f	14.	14.	12.	12.
T_d		54.	57.	60.
T_s		21.	17.	15.
T_{pd}		40.	38.	37.

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	464.	463.	461.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.96	0.80	0.95	1.09
T_r	51.	71.	53.	46.
T_f	11.	15.	12.	12.
T_d	54.	56.	57.	
T_s	20.	15.	12.	
T_{pd}	41.	35.	32.	



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

3.2.77

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	458.	458.	456.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.06	0.92	1.06	1.20
T_r	52.	76.	56.	48.
T_f	11.	15.	14.	12.
T_d		59.	60.	62.
T_s		22.	15.	13.
T_{pd}		46.	39.	35.

Type RTL No. A Temp. -55°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	458.	456.	454.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.09	0.94	1.08	1.22
T_r	55.	79.	58.	49.
T_f	12.	14.	13.	13.
T_d		61.	63.	65.
T_s		23.	16.	13.
T_{pd}		49.	40.	37.

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	466.	464.	463.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.87	0.71	0.86	1.0
T_r	54.	69.	53.	48.
T_f	11.	15.	13.	12
T_d		53.	55.	57.
T_s		20.	15.	13.
T_{pd}		40.	35.	33.

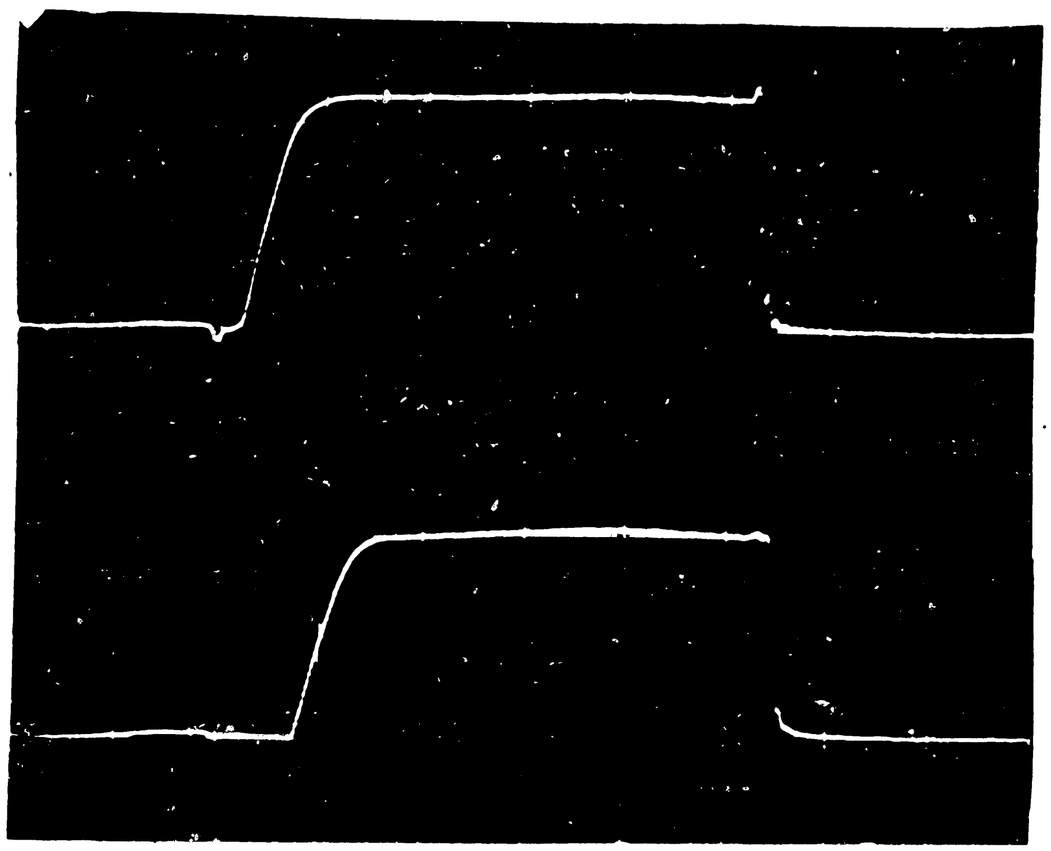
Type RTL No. A Temp. +125°C Vcc 3.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	467.	465.	463.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.79	0.63	0.78	0.92
T_r	58.	68.	54.	50.
T_f	14.	15.	13.	12.
T_d		54.	56.	58.
T_s		21.	17.	15.
T_{pd}		40.	36.	34.

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +25°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	458.	459.	458.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.95	0.74	0.83	0.92
T_r	52.	80.	55.	45.
T_f	10.	15.	13.	12
T_d	55.	56.		57.
T_s	19.	13.		11.
T_{pd}	44.	36.		33.



TEST CIRCUIT OUTPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. -40°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	453.	454.	455.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.06	0.84	0.95	1.04
T_r	54.	89.	61.	49.
T_f	11.	15.	14.	12.
T_d		61.	61.	63.
T_s		22.	15.	13.
T_{pd}		50.	40.	37.

Type RTL No. A Temp. -55°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	451.	453.	452.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	1.08	0.88	0.97	1.06
T_r	55.	92.	63.	50.
T_f	11.	16.	14.	13.
T_d		63.	64.	66.
T_s		22.	16.	13.
T_{pd}		53.	42.	39.

GENERAL MICRO-ELECTRONICS

Type RTL No. A Temp. +85°C Vcc 3.0 N = 5

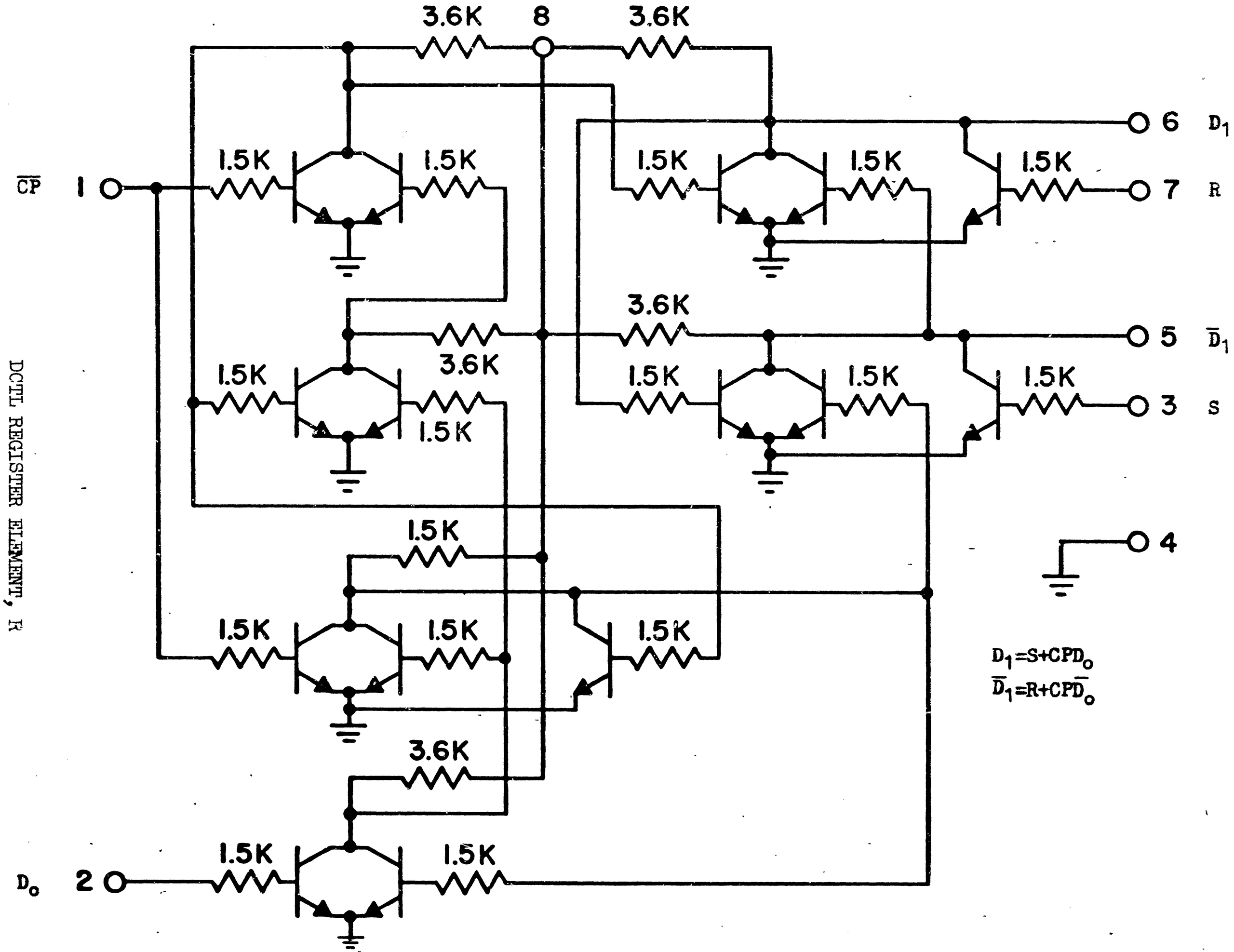
	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	461.	462.	462
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.85	0.64	0.73	0.82
T_r	53.	77.	55.	46.
T_f	10.	17.	13.	13.
T_d		54.	55.	57.
T_s		19.	15.	12.
T_{pd}		42.	36.	34.

Type RTL No. A Temp. +125°C Vcc 3.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 2.0	Vcc 3.0	Vcc 4.0
Pulse Width	500.	462.	464.	461.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	0.78	0.57	0.66	0.75
T_r	57.	77.	56.	47.
T_f	12.	19.	16.	14.
T_d		54.	56.	58.
T_s		20.	16.	14.
T_{pd}		42.	36.	35.

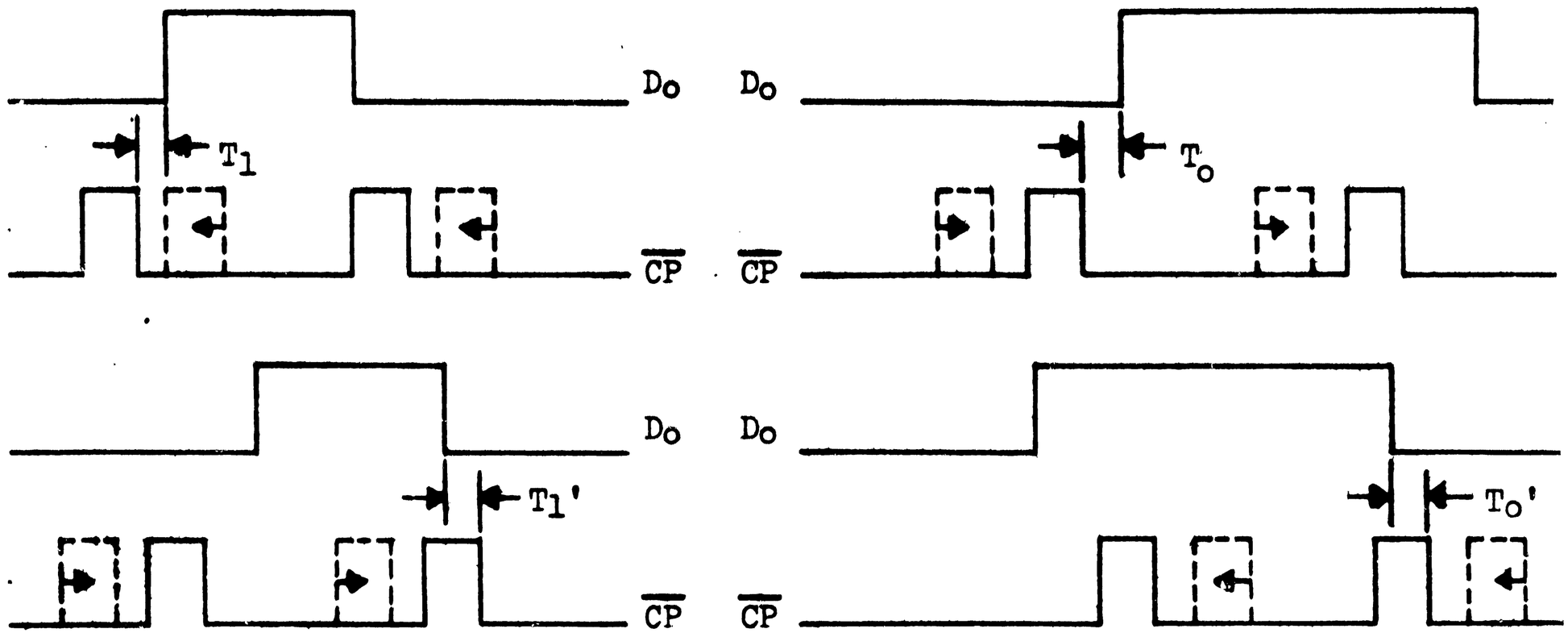
3.2.83

DCTL REGISTER ELEMENT, R



$D_1 = S + CPD_o$

$\overline{D}_1 = R + CP\overline{D}_o$



---- Condition 1

——— Condition 2

PROCEDURE FOR DETERMINING MINIMUM TIME RELATIONSHIPS BETWEEN $\overline{CP}$ INPUT AND D_o INPUT

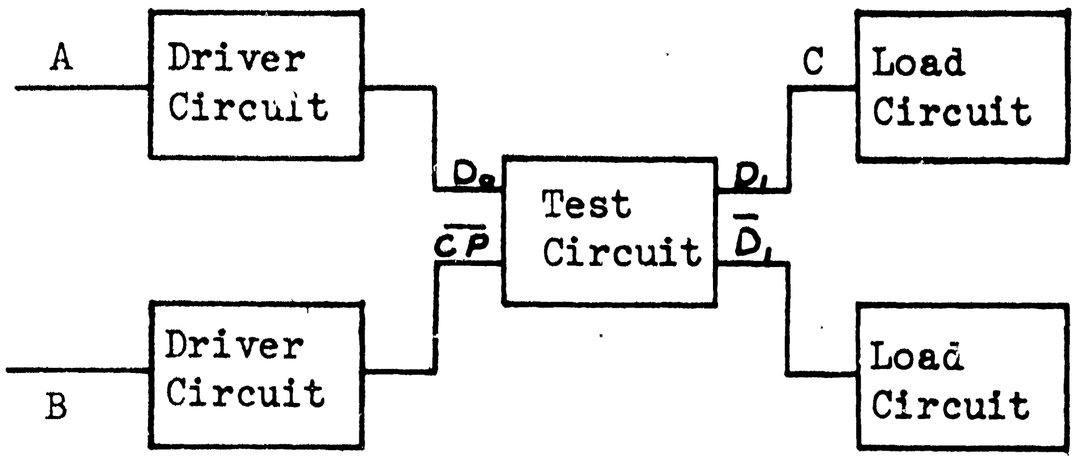
PROCEDURE:

1. The inputs were time orientated as shown in the above diagrams as condition 1.

2. The input clock pulse $\overline{CP}$ was delayed in the direction of the arrows until the circuit ceased to operate as viewed at D_1.

3. The pulse train $\overline{CP}$ was then reversed until the circuit began to toggel and the time indicated for each case was recorded between the 50% points.

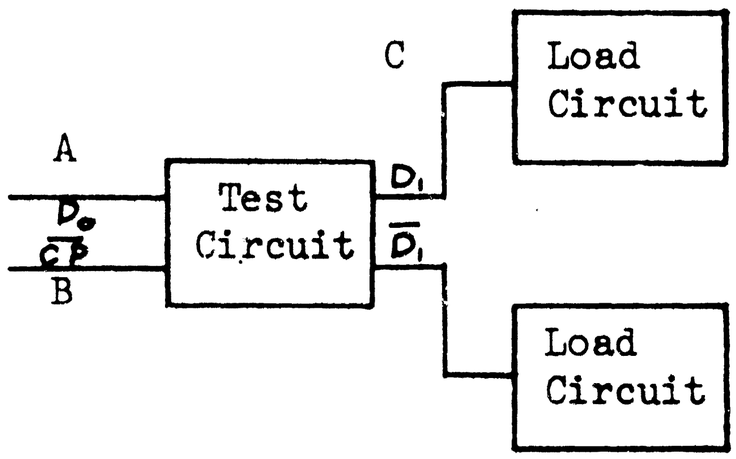
NOTE: The threshold voltage of the clock pulse is approximately 0.6 volts. That is, the trigger point is at .6 volts on the negative slope of the clock pulse. The measuring point is at 50% or 1.5 V on the 1.5 V and 0.6 V on a 20 ns fall time pulse should account for the apparent pre-trigger when setting the output high.



CONDITION 1

	25°C	-55°C	+125°C
T_1	6.57	6.3	10.4
T_1'	2.97	1.5	15.3
T_o	6.85	6.7	12.9
T_o'	7.17	1.5	18.

The table of data is an average of 4 readings for each temperature and read at the driver inputs.



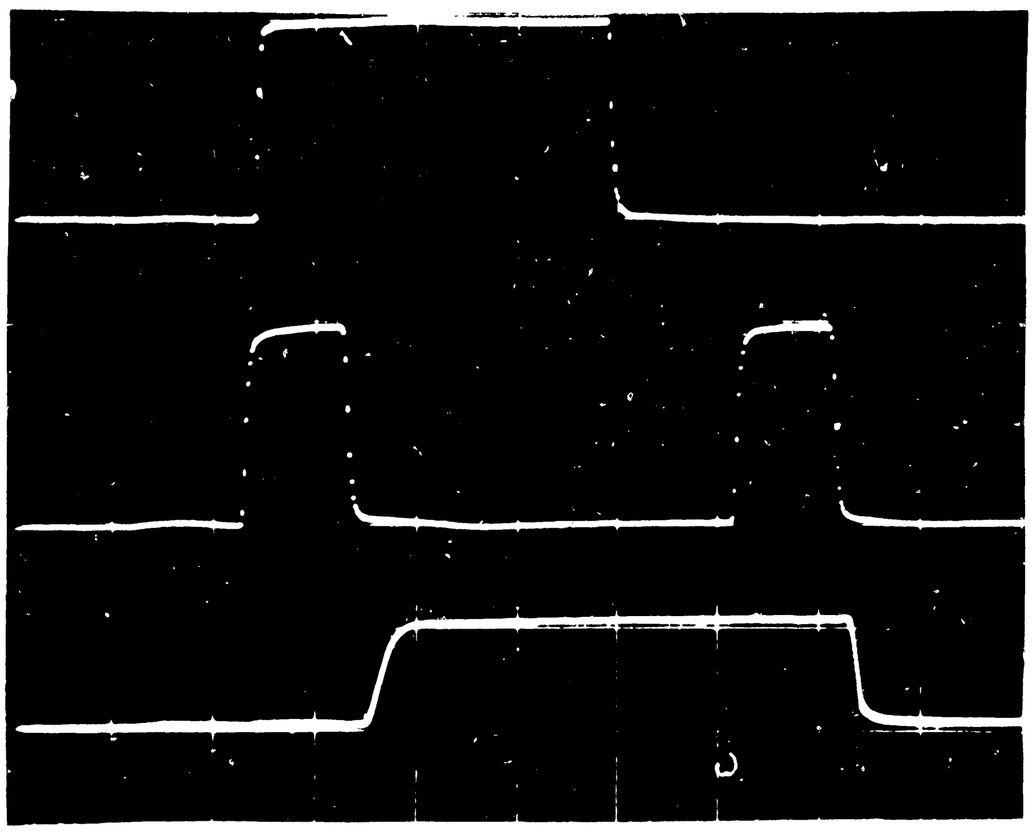
CONDITION 2

	25°C	-55°C	+125°C
T_1	5.45	5.0	7.73
T_1'	2.1	4.4	1.0
T_o	5.9	4.9	8.1
T_o'	0	2.4	1.0

The table of data is an average of 2 readings for each temperature and read at test circuit input.

NOTE: All readings in nanoseconds

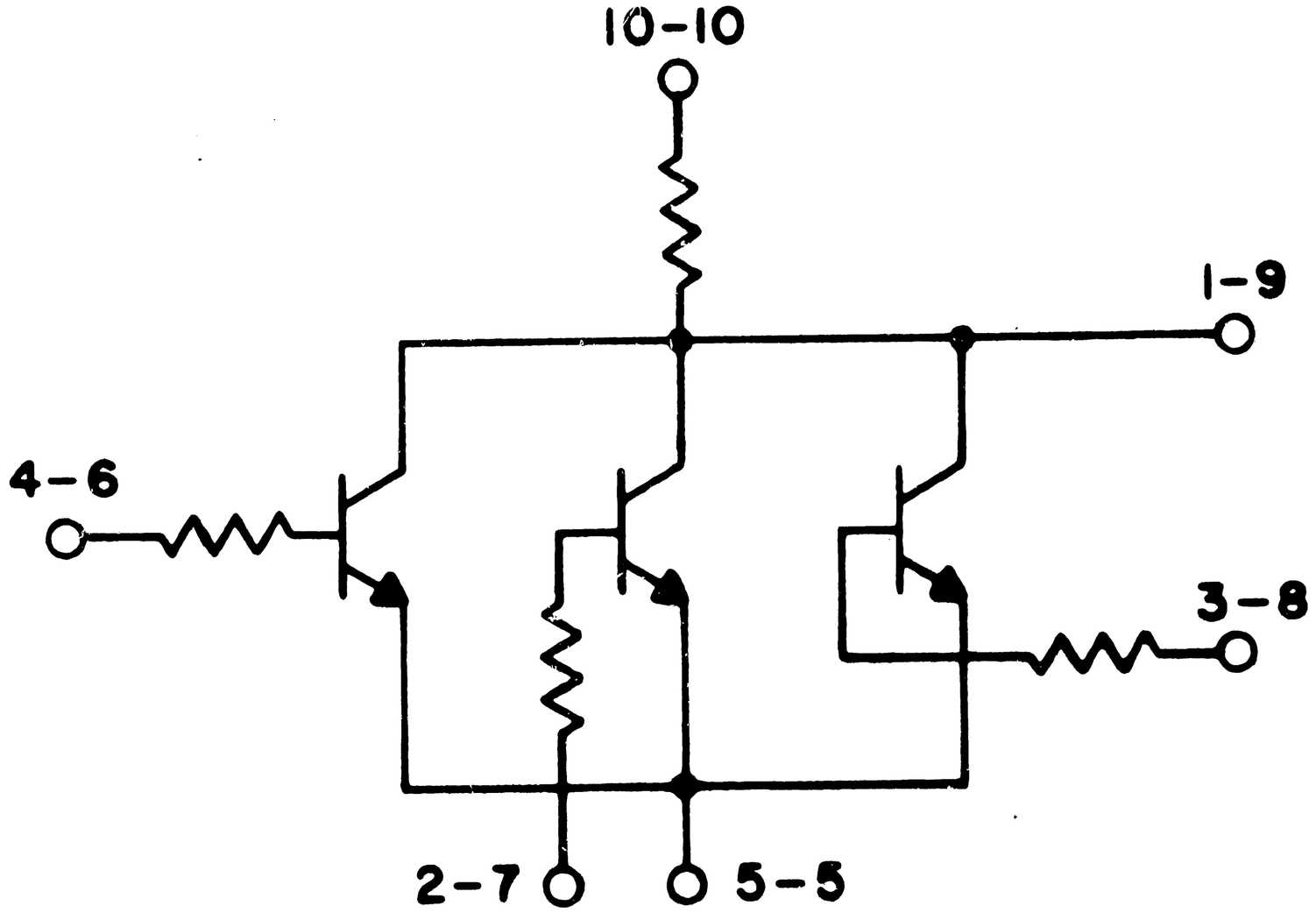
	TEST CKT INPUT CLOCK	TEST CIRCUIT OUTPUTS FOR TEMPERATURES OF				
		25°C	-40°C	-55°C	+85°C	+125°C
Amplitude	3.0	1.03	1.14	1.16	0.94	0.85
Pulse Width	200.	992.	994.	995.	983.	984.
T_r	18.	56.	58.	58.	56.	57.
T_f	19.	37.	45.	48.	42.	48.
T_d		48.	50.	52.	50.	50.
T_s		42.	46.	49.	42.	45.
T_{pd}		56.	64.	68.	56.	59.



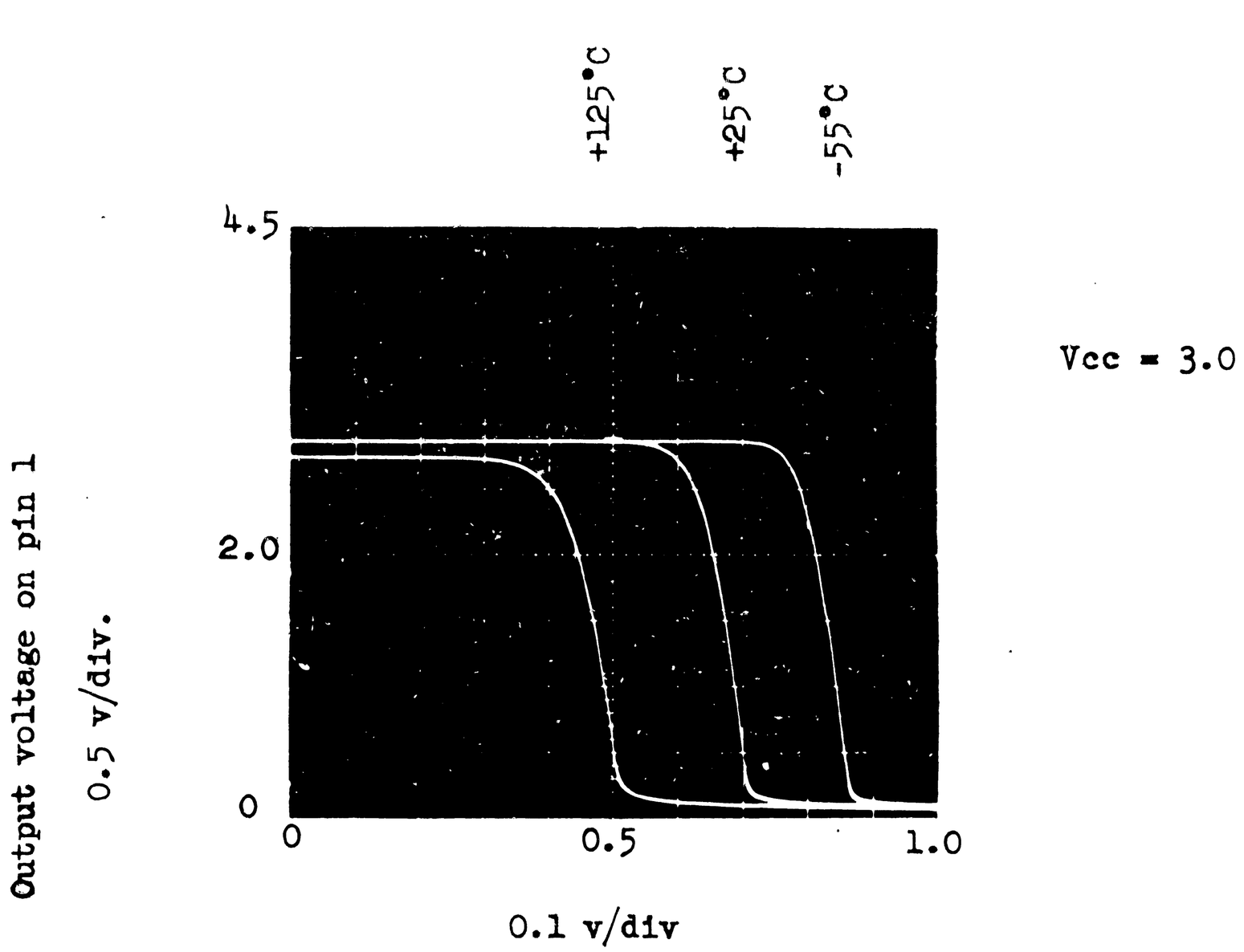
INPUT D_o

INPUT CLOCK $\overline{CP}$

OUTPUT D_1



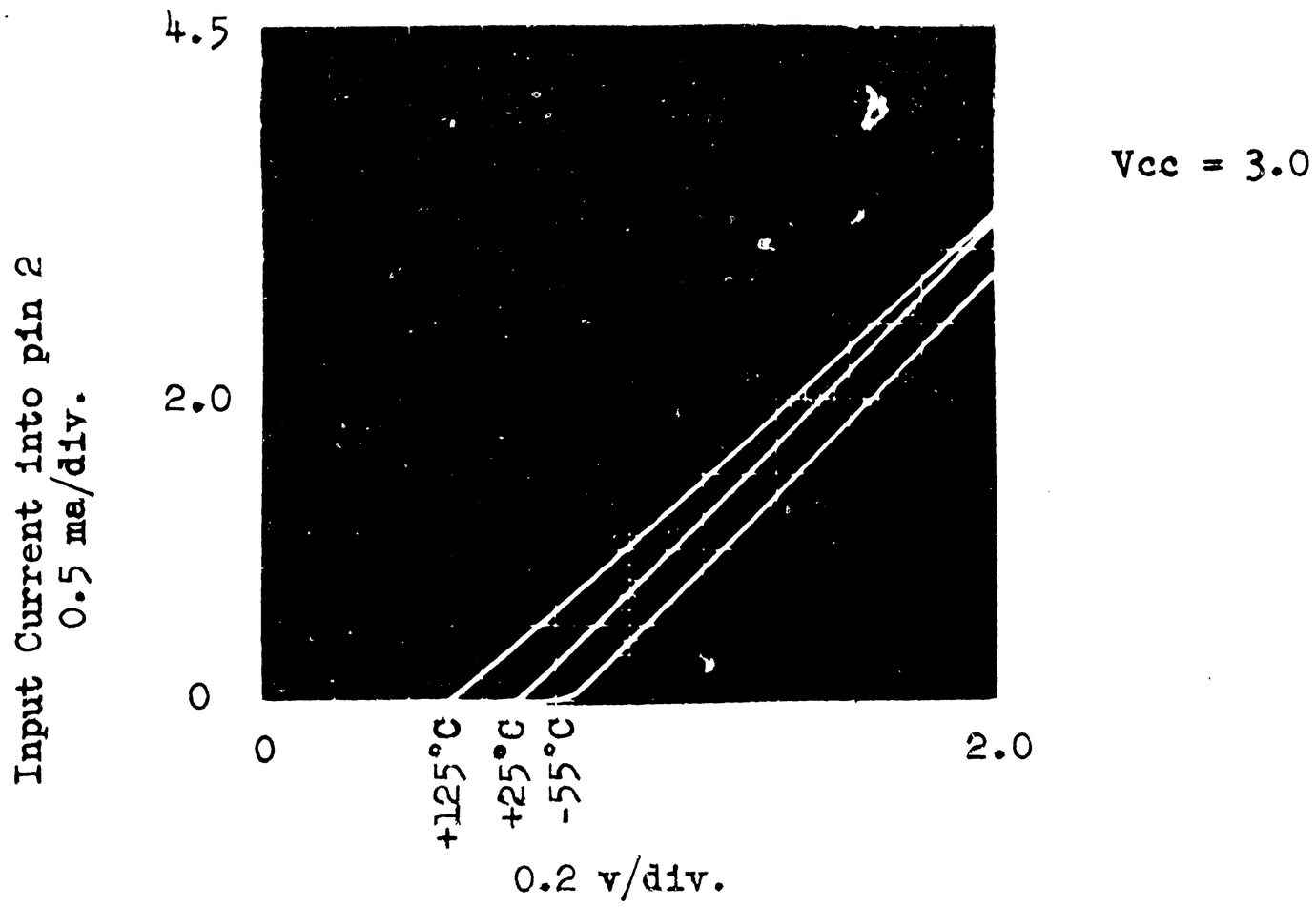
DUAL 3 - INPUT DCTL HIGH POWER GATE ELEMENT



INPUT OUTPUT CHARACTERISTICS

RTL $153D_3$

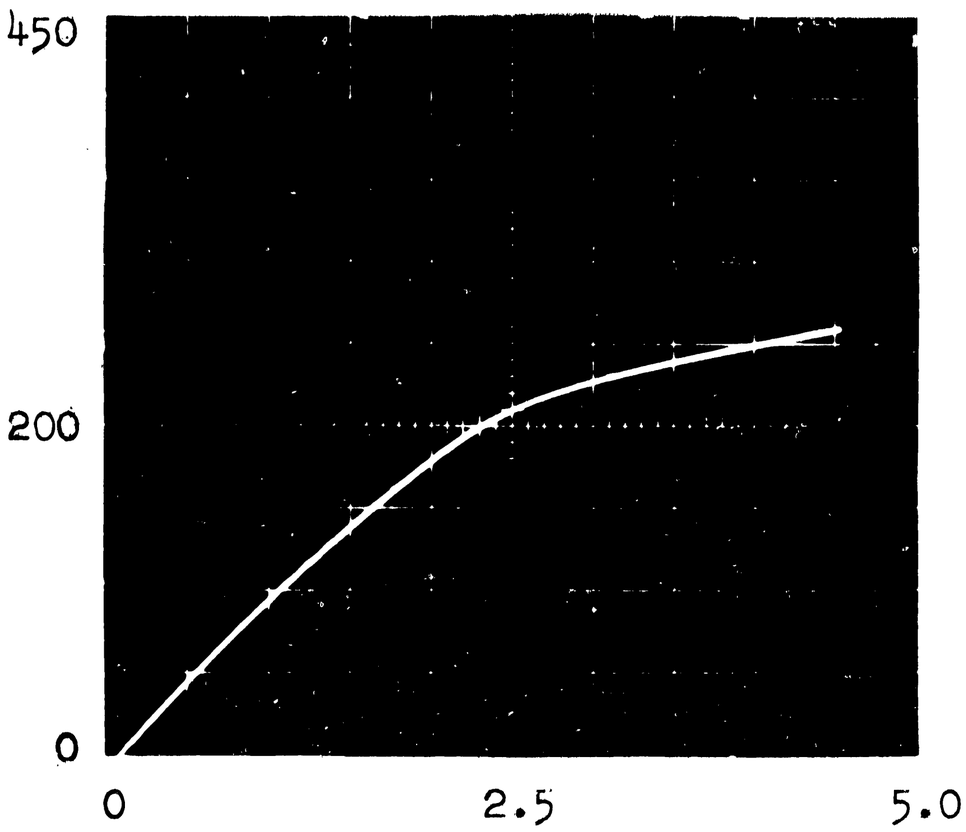
3.2.88



INPUT CHARACTERISTICS

RTL $153D_3$

3.2.89



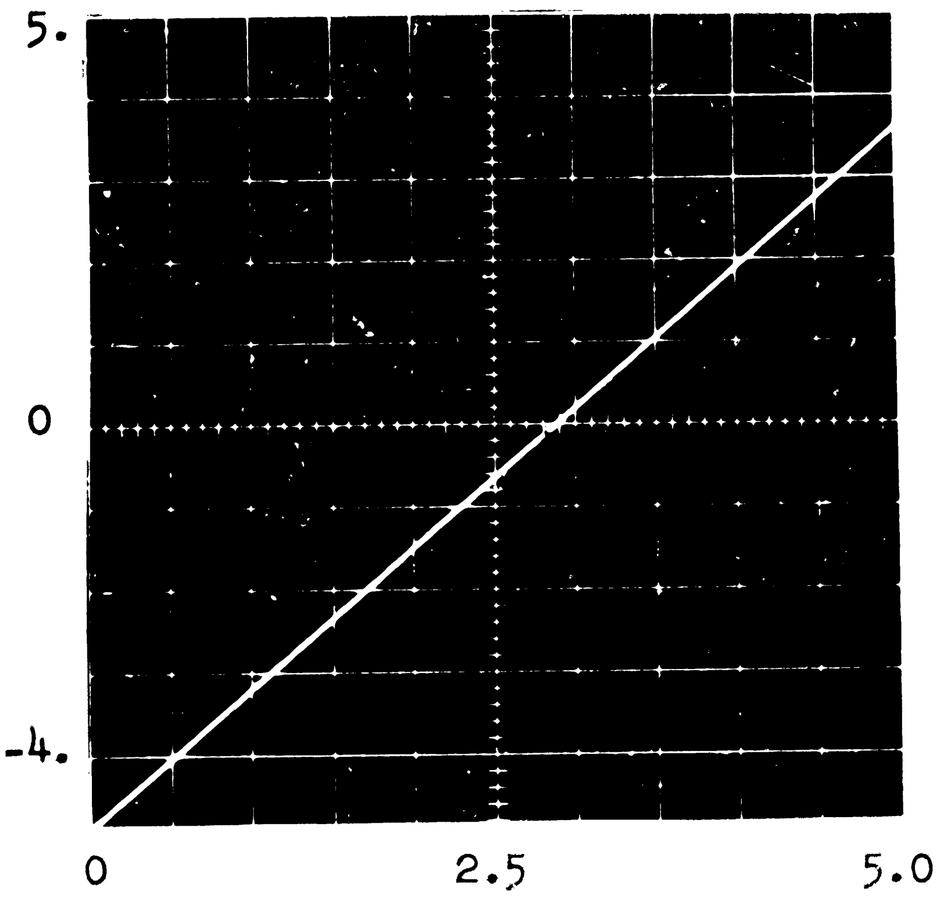
Output current into pin 1

50 ma/div.

Vcc = 3.0
"1" on pin 2

0.5 v/div.

Output voltage on pin 1



Output current into pin 1

1 ma/div.

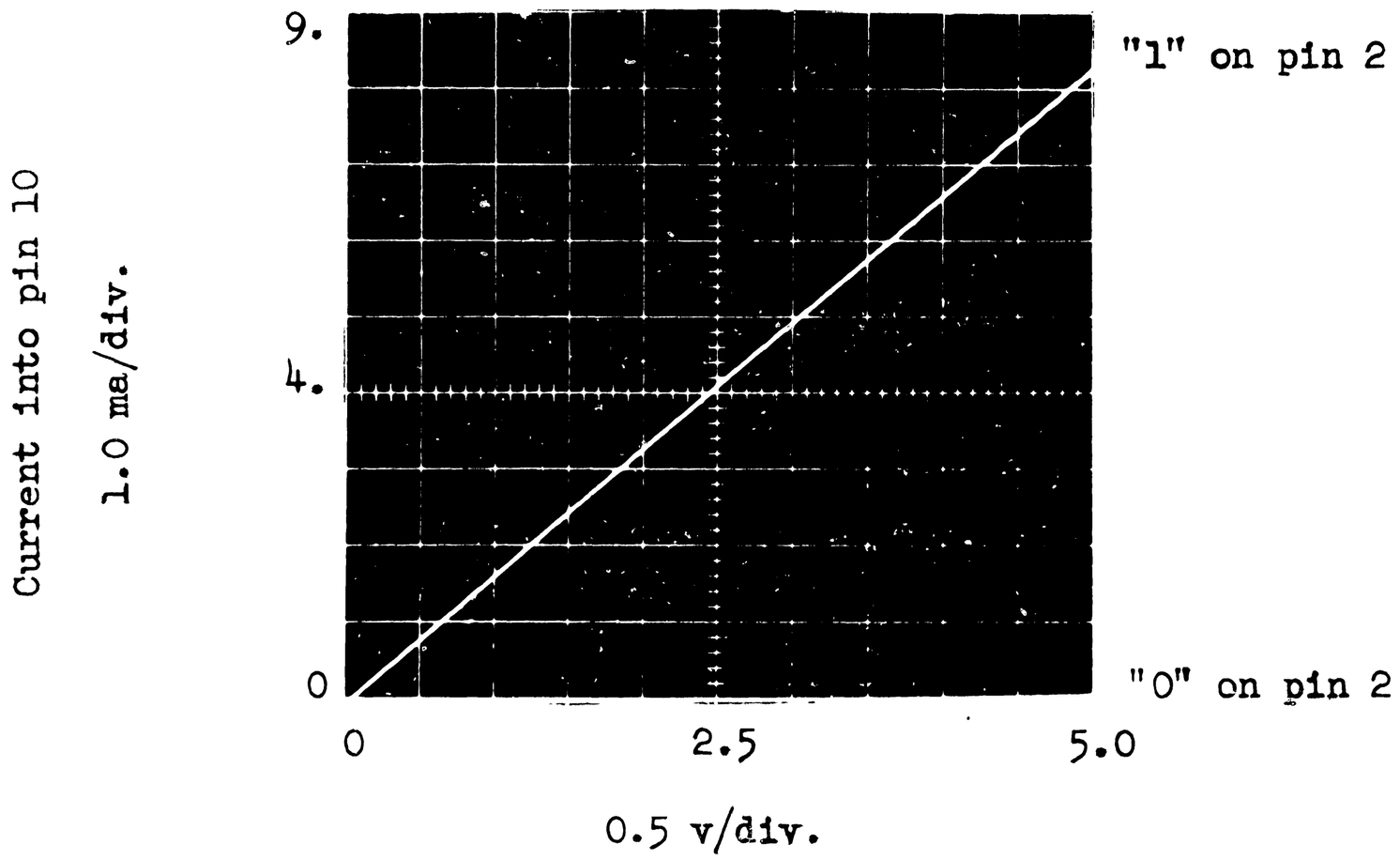
Vcc = 3.0
"0" on pin 2

0.5 v/div.

Output voltage on pin 1

OUTPUT CHARACTERISTICS
RTL $153D_3$

3.2.90



POWER DISSIPATION CURVES

RTL $153D_3$

3.2.91

EVALUATION

The General Microelectronic DTL line is a family of monolithic, planar, epitaxial devices consisting of five DTL circuits and two diode AND Gates.

DTL 254G4 and 254G3 are identical DTL NAND/NOR Gates with the exception that 254G4 has an additional input diode. Both are provided with an optional internal pull-up resistor which may or may not be used according to the application. They also have an extra input terminal (without the input diode) to allow additional AND Gating or to permit OR-diode gating.

DTL 264P is a NAND/NOR Gate similar to the 254G3 except no pull-up resistor is provided and this circuit has higher dc fan-out capabilities.

DTL 264D2 is a Dual 2 input DTL NAND/NOR gate with a pull-up resistor provided. There are no spare inputs provided on this circuit. The circuit will generate the exclusive OR function when pins 2 and 10 are tied together.

DTL 264B is a DTL set reset flip-flop with provisions for clock operation. The circuit was designed for ripple counting and shifting. The clock pulse, when operating in the clock mode, must have a fall time described by:

$$\frac{T_F}{V_{CP}} = <50 \ \frac{nSec}{volt}$$

where T_F is fall time
and V_{CP} is the clock pulse amplitude

Also, the minimum clock pulse width is determined by the time constant of the charging circuit which is influenced by the fan-out of the gate driving the clocked set (or reset) inputs and the output impedance of the clock driver.

The output are buffered for high d-c fan out and driving of capacitive loads. This element can be used in either double or single power supply systems.

The truth table for the 264B for positive logic is:

CLOCKED		SET-RESET	DIRECT SET		RESET	
S_c	R_c	Q	S_d	R_d	Q	$\overline{Q}$
0	0	?	0	0	*	1
0	1	1	0	1	1	0
1	0	0	1	0	0	1
1	1	No Change	1	1	No Change	

DTL 254G6 and DTL 254D3 are Diode AND Gates; the 254G6 is designed to be used as a 6 input AND Gate but the supply resistor is not connected internally to the output terminal. The 254D3 is a Dual 3-input Diode AND Gate with the supply connected internally to the output pin.

All circuits with the exception of the 254G3 were tested statically on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

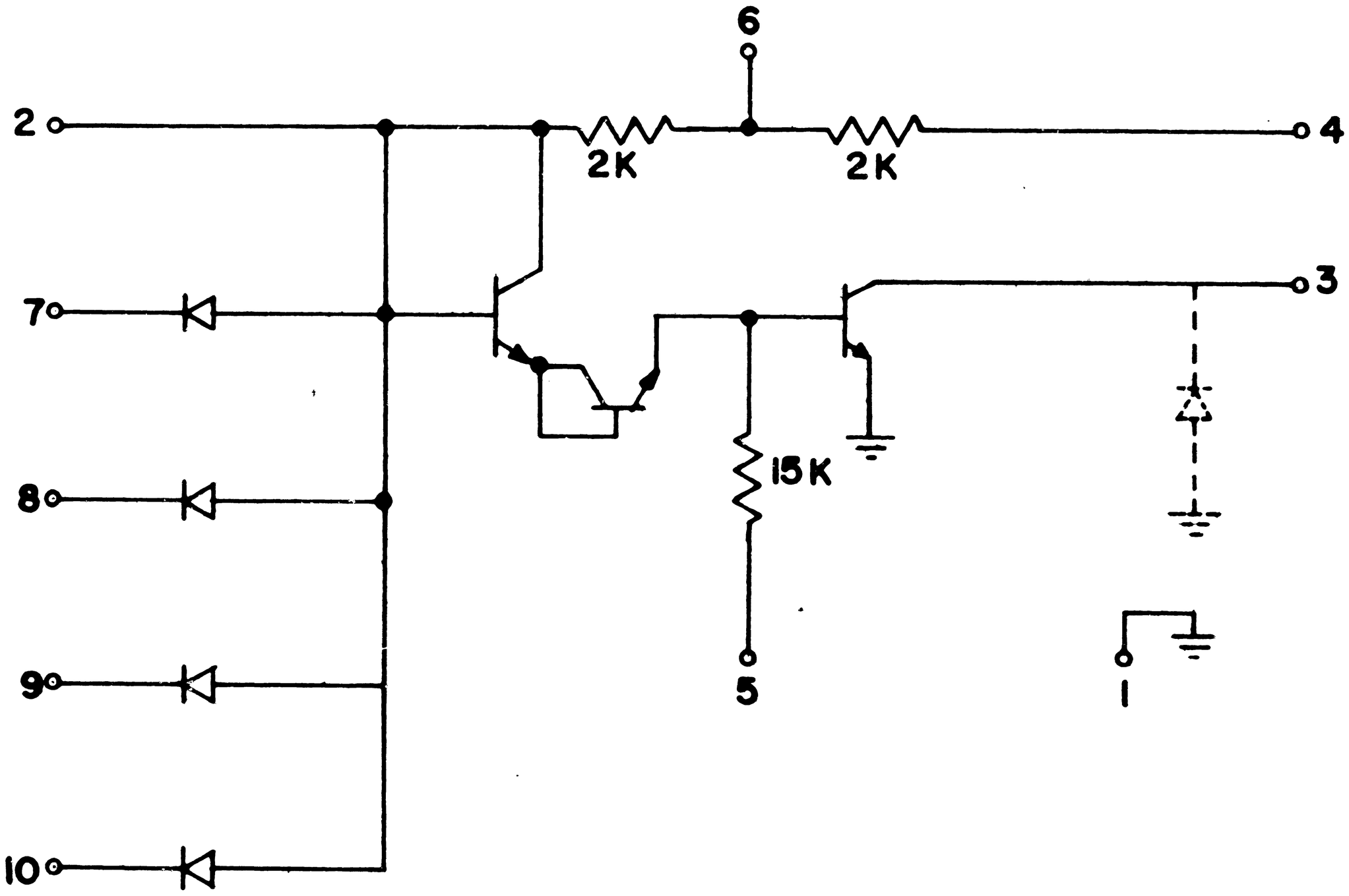
1. The block diagram for each test precedes the data for that circuit.

2. The temperature was regulated at 25°C the pulse repetition rage was set at 1 MC with a pulse width of 500 ns. The supply voltages for the 254G4 and 264B were set at: V_6 = +4.0, V_5 = -2.0. The load for the 254G4 and 264B was 1.

3. Data was taken for the 254D3 at supply voltages of 3.0V, 4.0V and 5.0V with a load of 1.

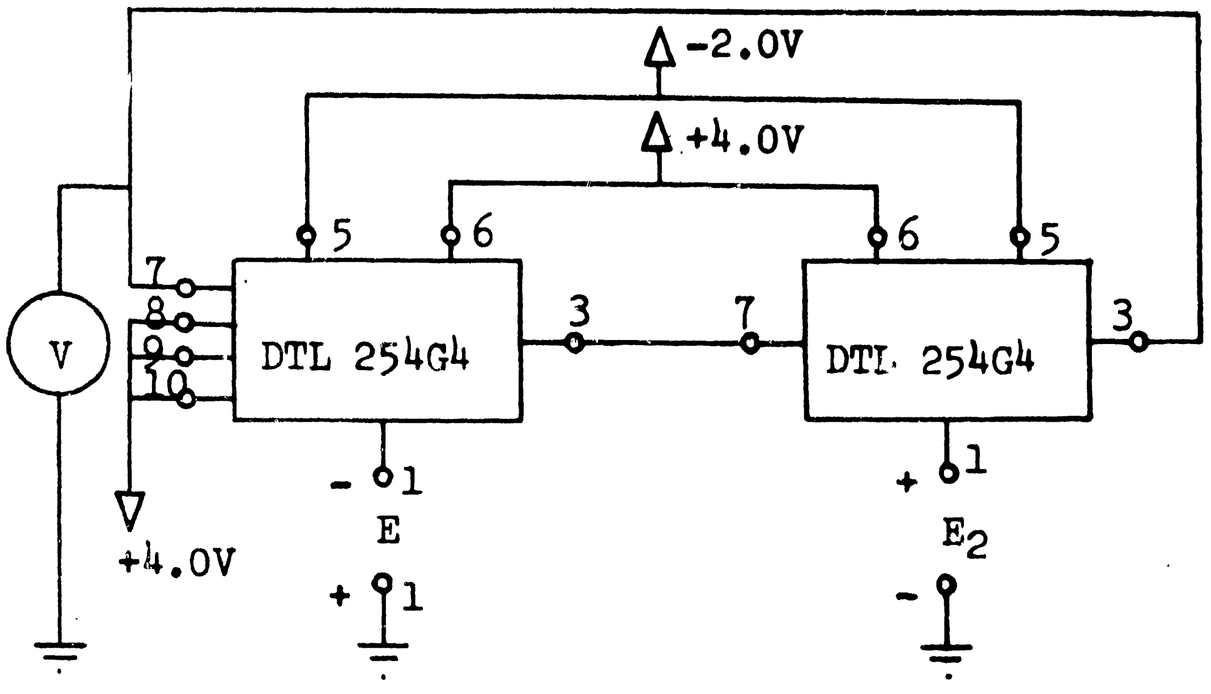
4. The above was repeated for temperatures of -40°C, -55°C, +85°C and +125°C.

5. The above was repeated for varying loads of 3 and 5 for the 254G4 and the 254D3.



3.2.94

254G4 4-INPUT DTL NOR GATE



NOISE TEST

PROCEDURE:

1. The circuits were connected as in the above block diagram.

2. E_2 was replaced by a short.

3. E_1 was increased until V indicated a change of state.

4. The system was reset by opening the negative terminal of E_1 which set V to zero.

5. E_1 was replaced by a short.

6. E_2 was increased until V indicated a change of state.

7. The system was reset by disconnecting E_1's short which set V to zero.

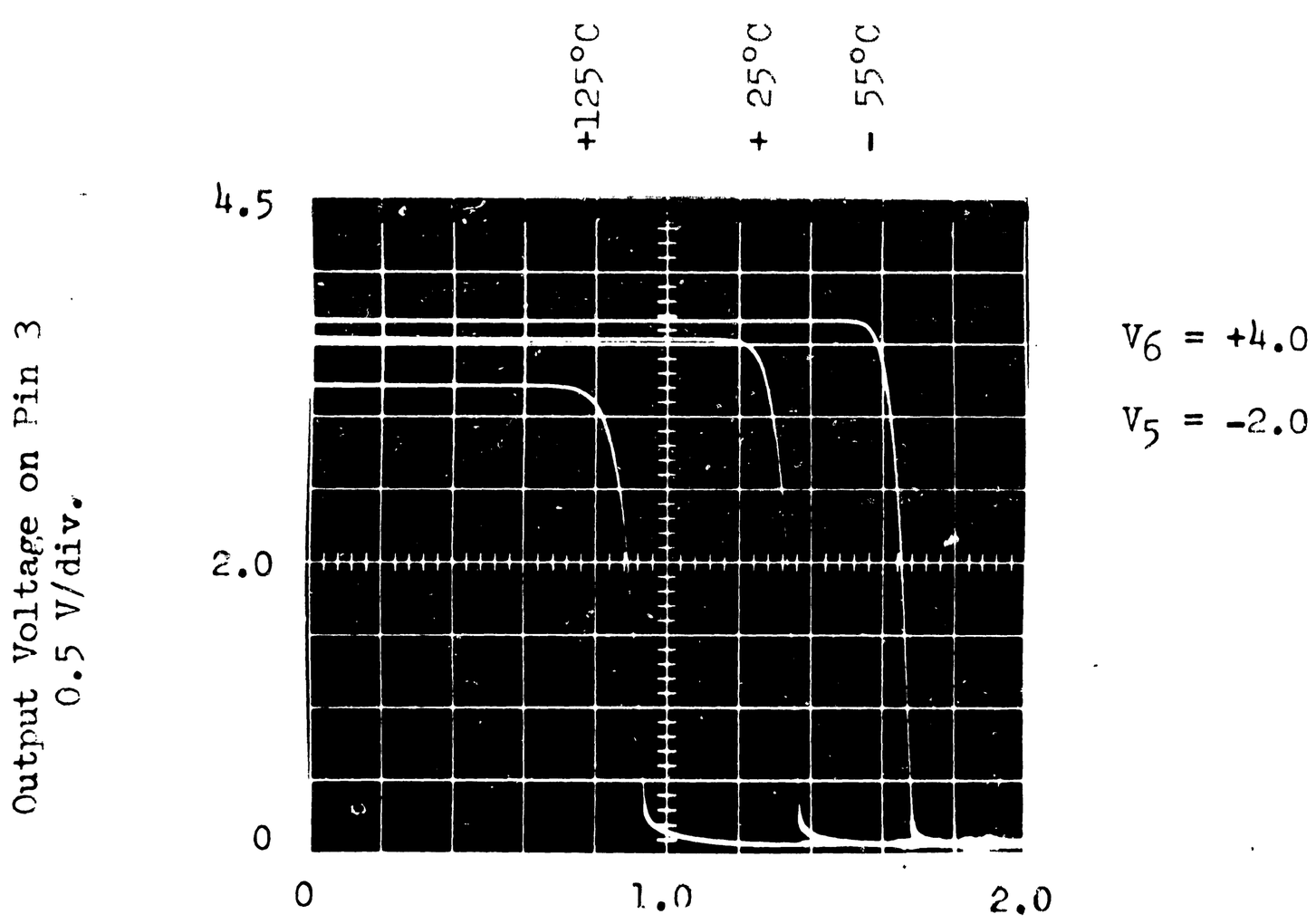
DATA:

The average of five test runs was:
E_1 at system change of state -1.208
E_2 at system change of state +1.18

The noise margin of the DTL elements used was 1.18 V.

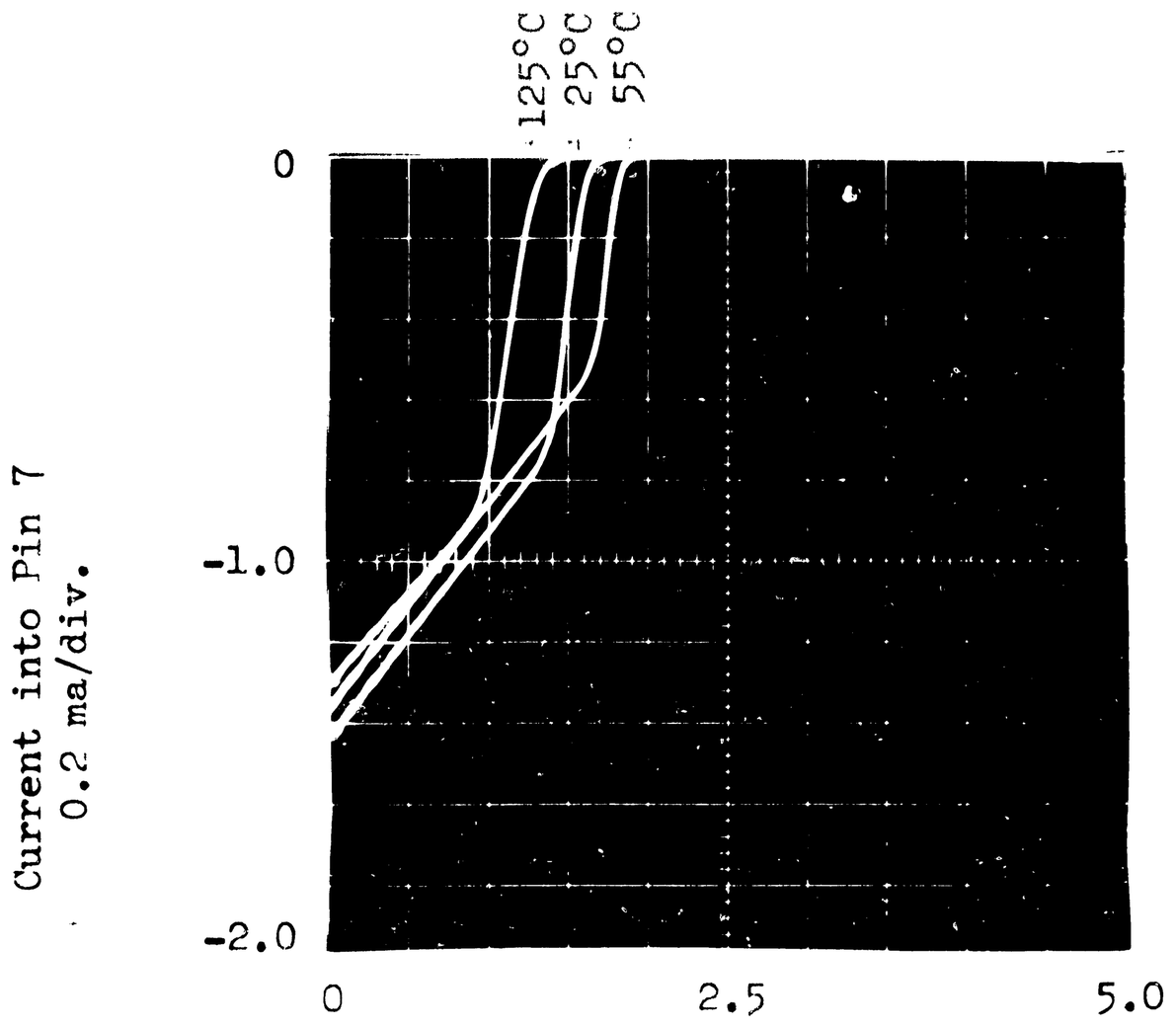
EQUIPMENT:

Voltmeter; Hewlett Packard, Model 412A
Power Supplies; Harrison Laboratories, Model 6204A
E_1 and E_2; Harrison Laboratories, Model 865B



NOTE: All curve tracer tests for this circuit were performed with the pull-up resistor provided internally.

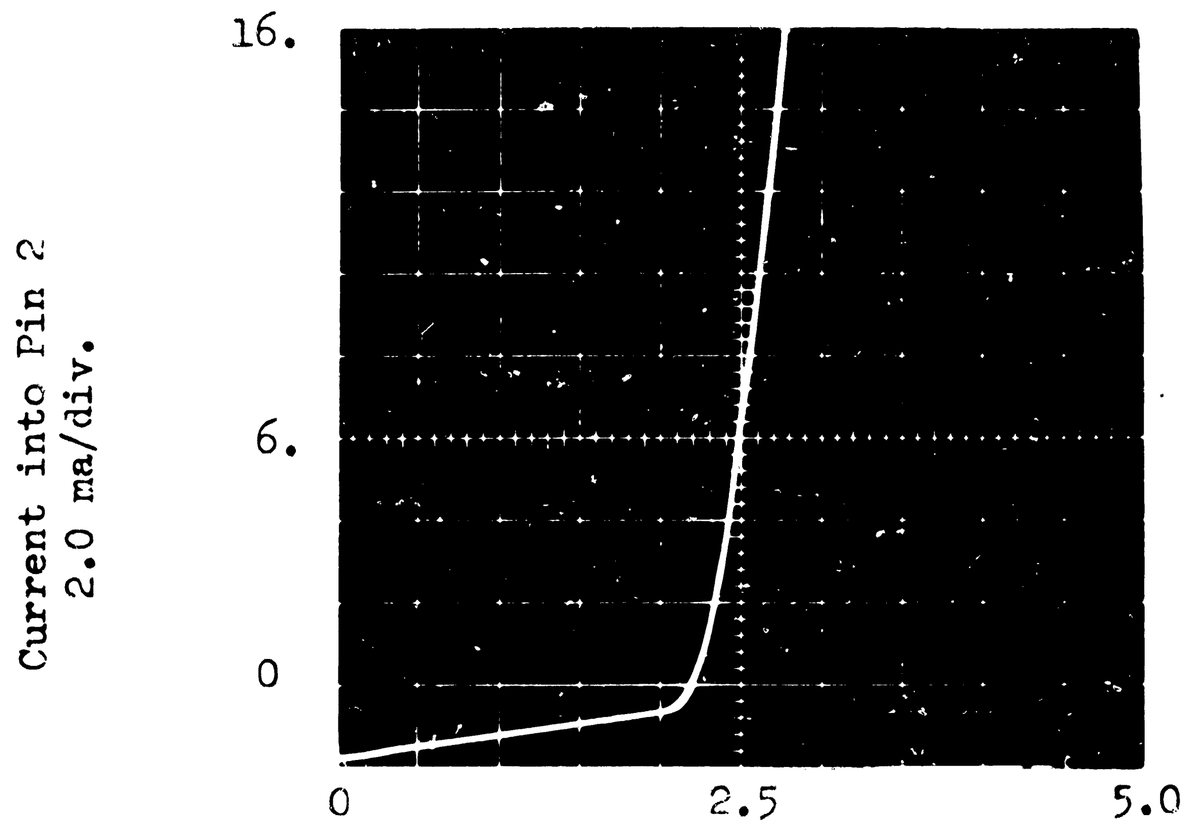
INPUT - OUTPUT CHARACTERISTICS
DTL 254G4



$V_6 = +4.0$

$V_5 = -2.0$

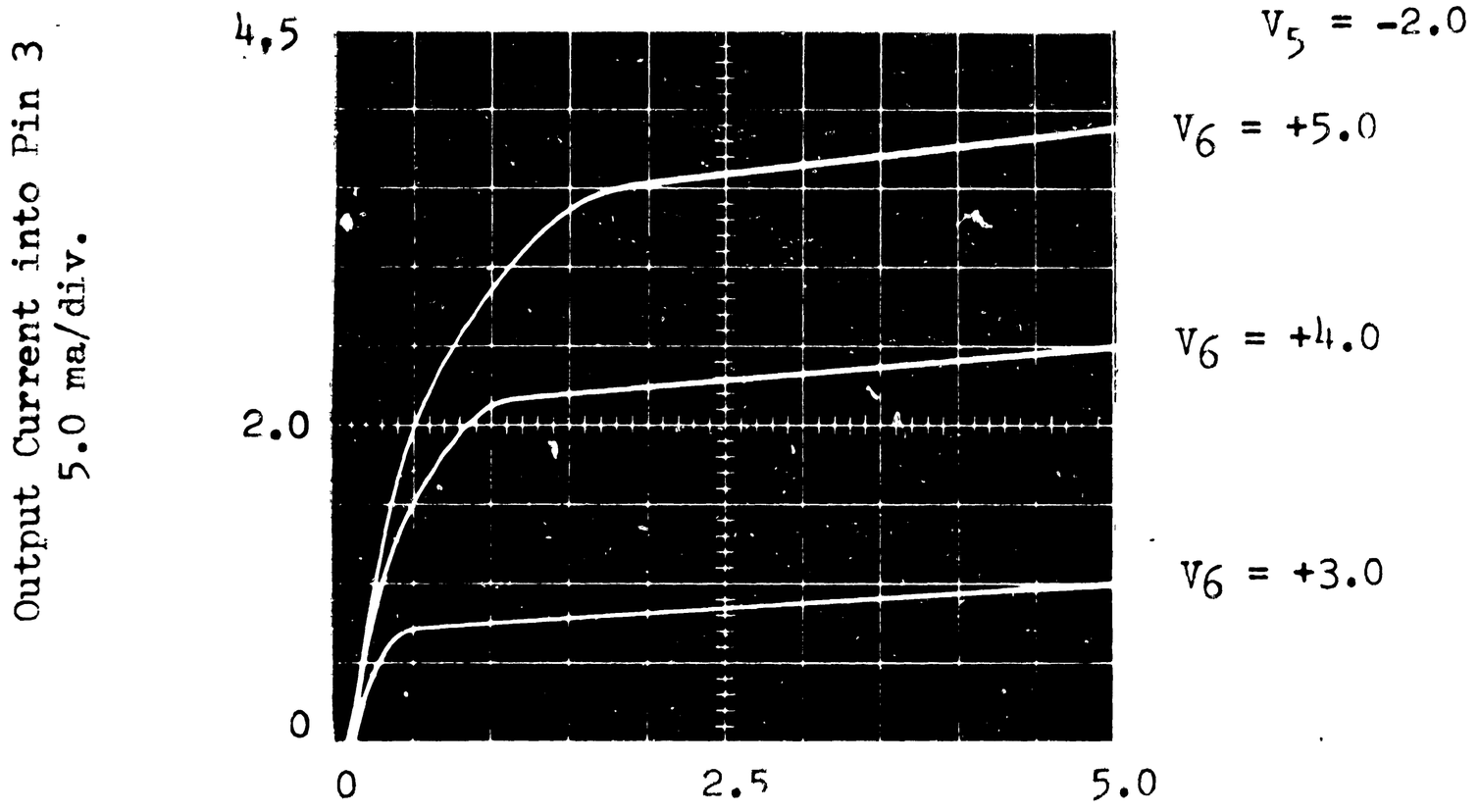
0.5 V/div.
Input Voltage on Pin 7



0.5 V/div.
"Direct" Input Voltage on Pin 2
(No input diode)

INPUT CHARACTERISTICS
DTL 2546

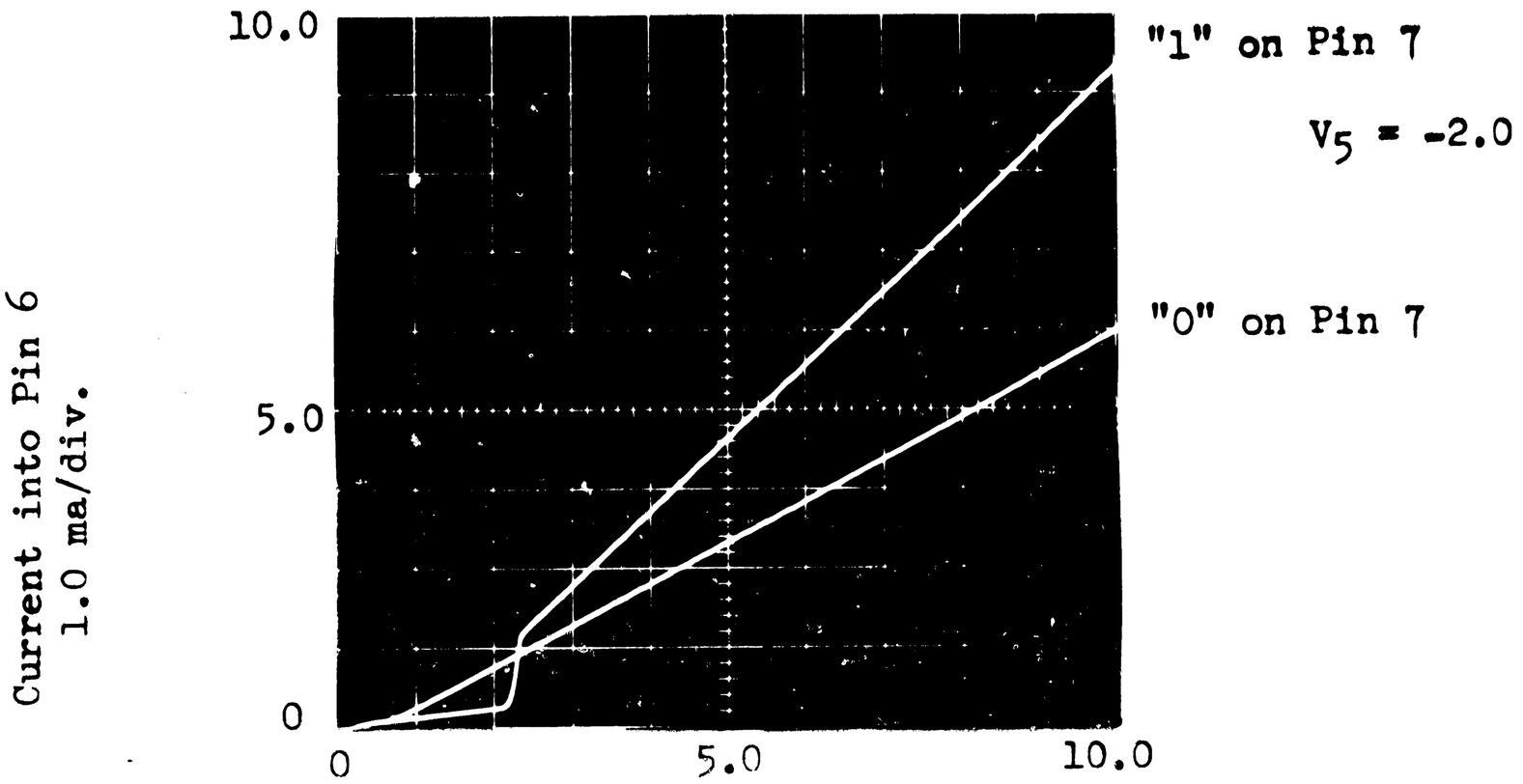
3.2.97



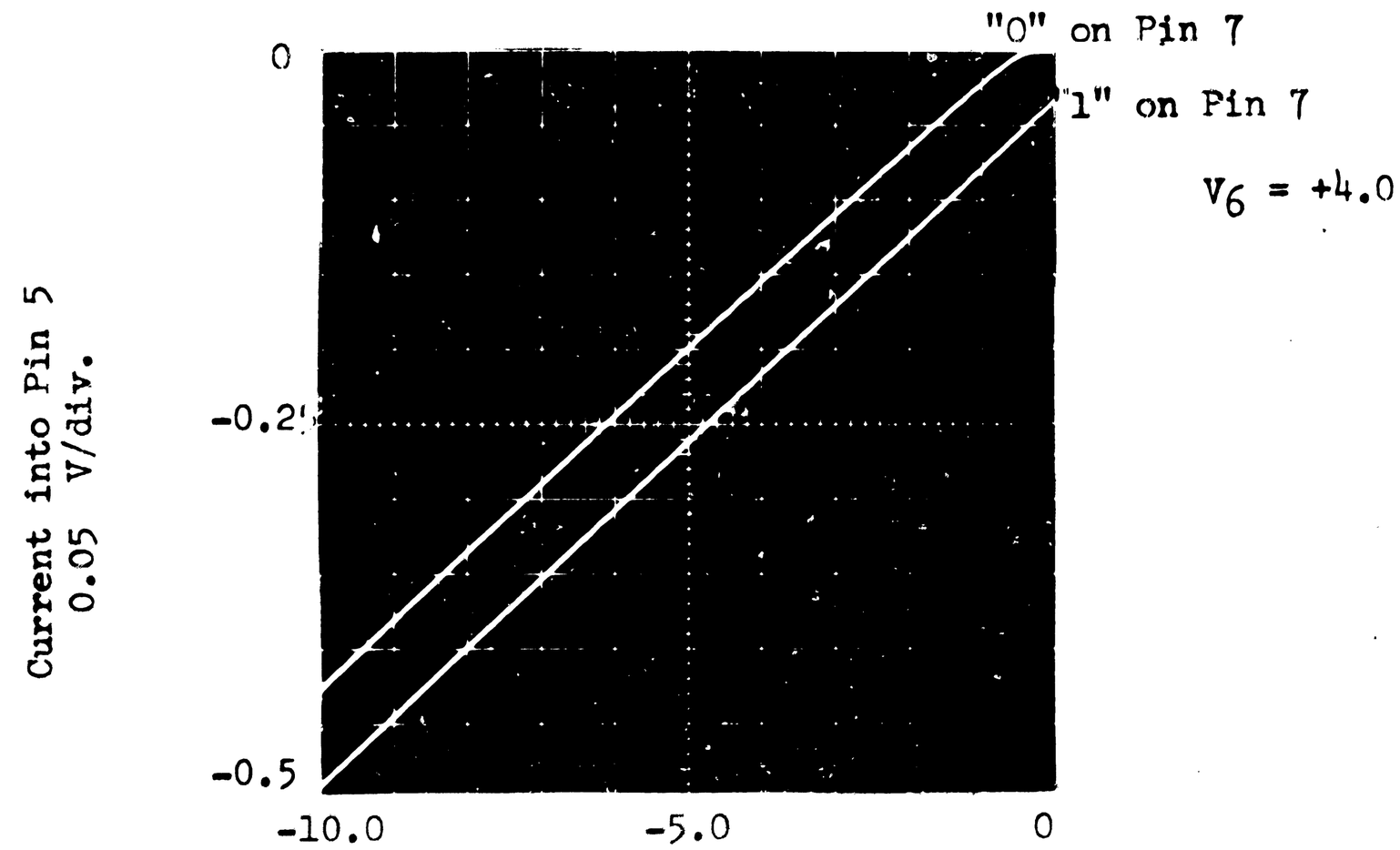
OUTPUT CHARACTERISTICS

DTL 254G4

3.2.98



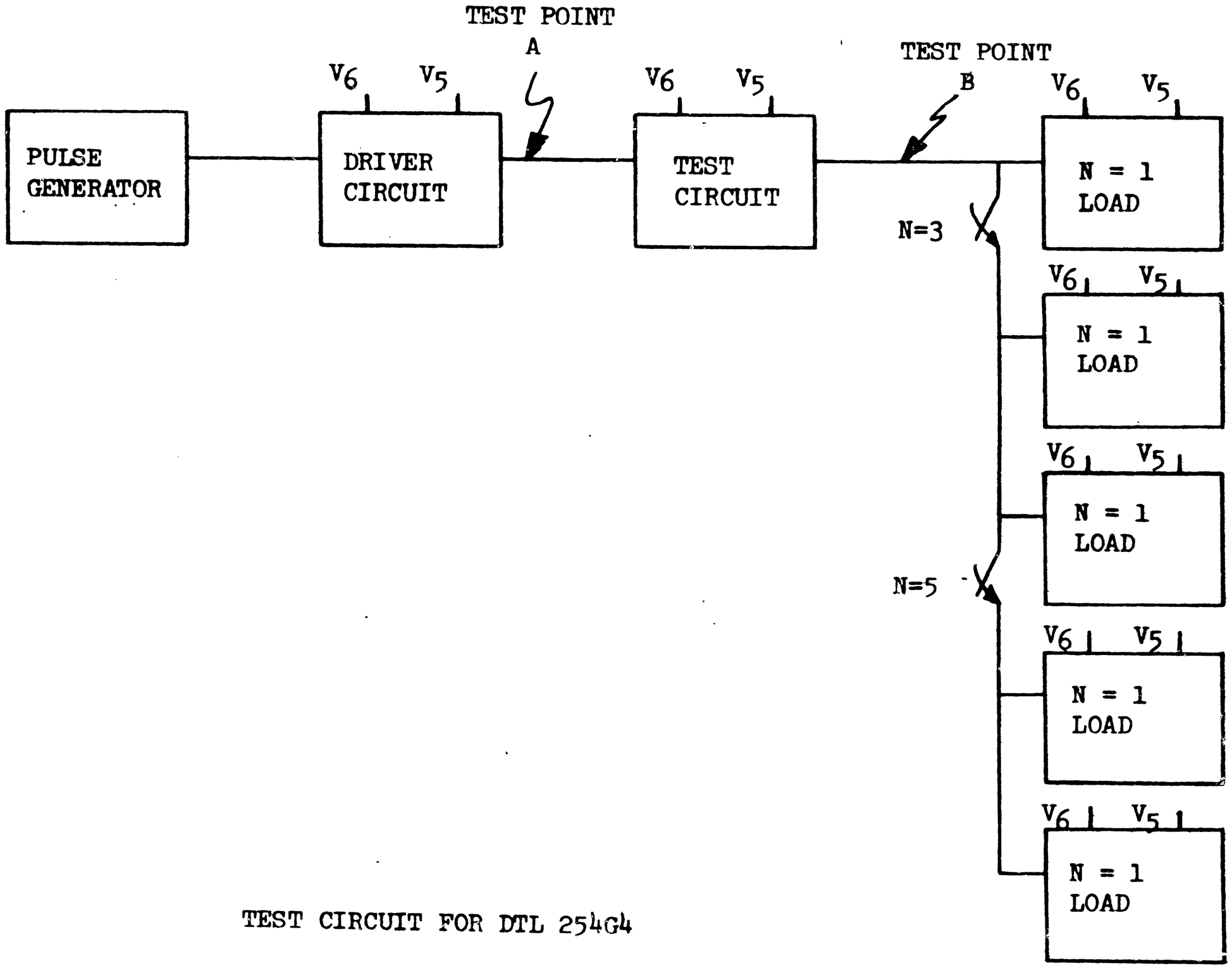
1.0 V/div.
Supply Voltage on Pin 6



1.0 V/div.
Supply Voltage on Pin 5

POWER DISSIPATION CURVES
DTL 254G4

3.2.99

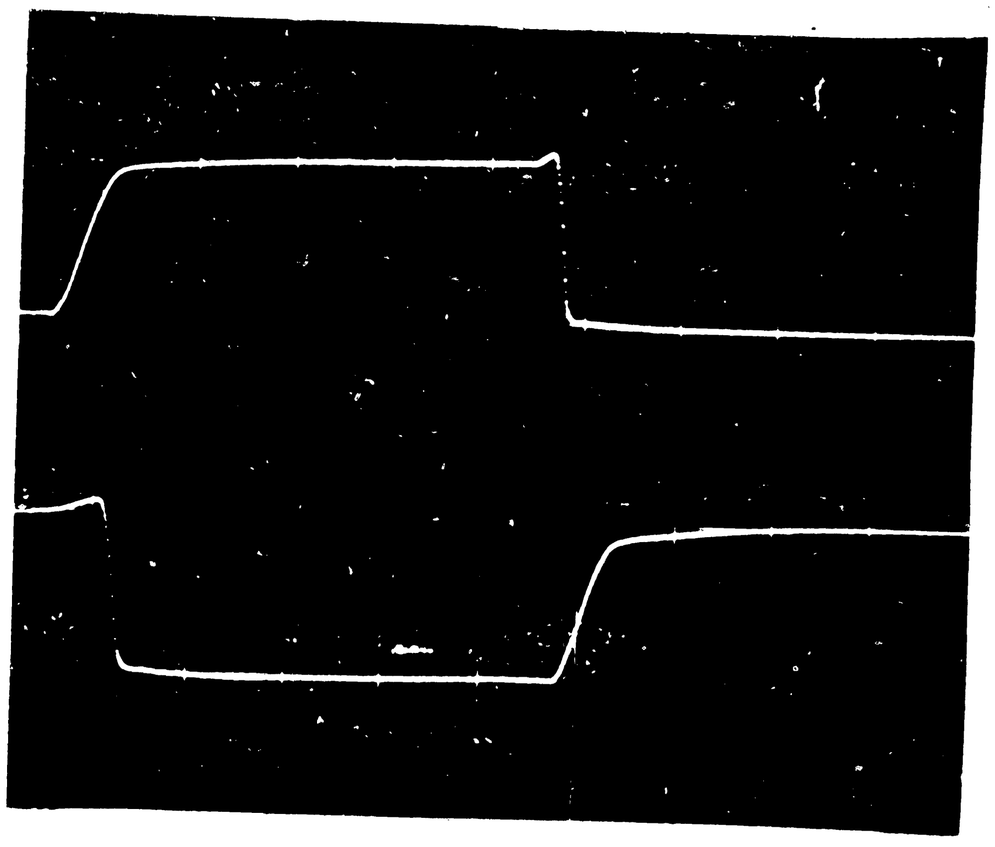


TEST CIRCUIT FOR DTL 254G4

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT. INPUT	TEST CKT. OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	500.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.70	1.68
T_r	56.	60.
T_f	13.	16.
T_d		50.
T_s		17.
T_{pd}		34.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	478.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.84	1.86
T_r	58.	55.
T_f	16.	19.
T_d		60.
T_s		12.
T_{pd}		36.

Type DTL No. 254G4 Temp -55 V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	471.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.89	1.90
T_r	59.	57.
T_f	18.	21.
T_d		64.
T_s		11.
T_{pd}		39.

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +85°C V6 +4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 4.0 V5 -2.0
Pulse Width	500	519
Repitition Rate	1MC	1MC
Pulse Amplitude	1.52	1.50
T_r	59.	70.
T_f	13.	15.
T_d		44.
T_s		27.
T_{pd}		36.

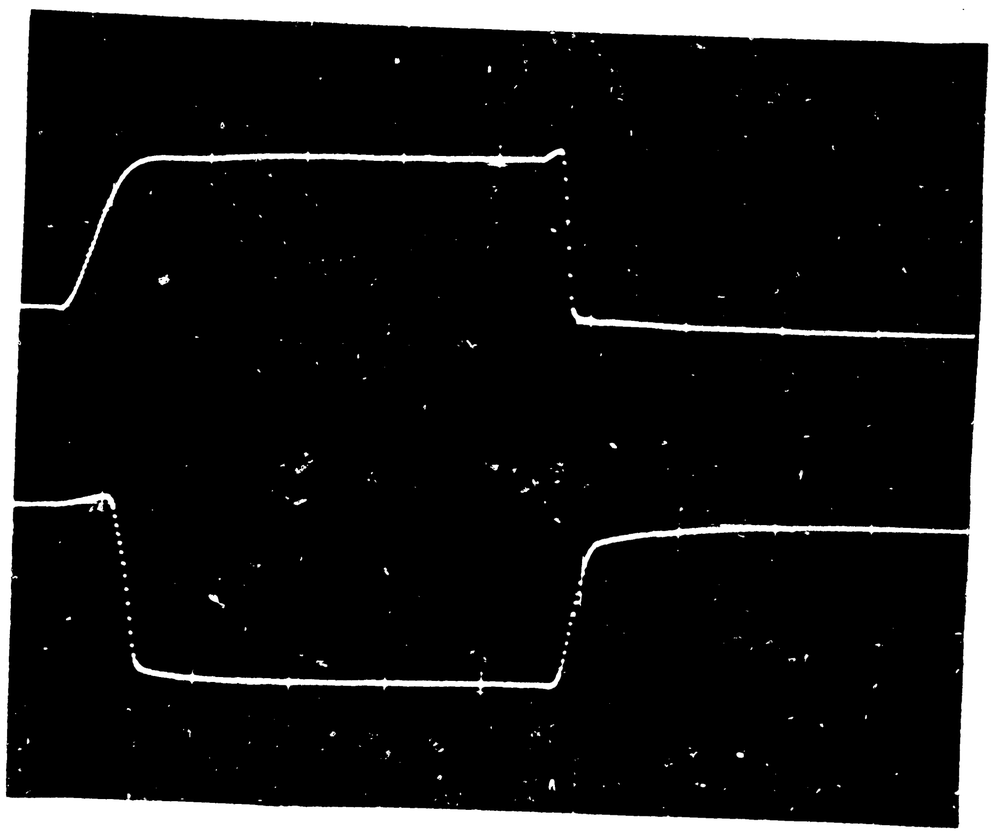
Type DTL No. 254G4 Temp +125°C V6 4.0 V5 -2.0 N = 1

	TEST CKT INPUT	TEST CKT OUTPUT V6 4.0 V5 -2.0
Pulse Width	500.	531.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.38	1.36
T_r	66.	76.
T_f	14.	16.
T_d		42.
T_s		35.
T_{pd}		39.

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT. INPUT	TEST CKT. OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	480.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.72	1.80
T_r	59.	52.
T_f	13.	25.
T_d		51.
T_s		12.
T_{pd}		30.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	451.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.88	1.94
T_r	61.	36.
T_f	17.	35.
T_d		62.
T_s		8.
T_{pd}		36.

Type DTL No. 254G4 Temp -55°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	442.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.92	1.98
T_r	62.	35.
T_f	18.	39.
T_d		66.
T_s		7.
T_{pd}		40.

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +85°C V6 +4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 4.0 V5 -2.0
Pulse Width	500.	507.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.56	1.62
T_r	58.	65.
T_f	14.	22.
T_d		45.
T_s		21.
T_{pd}		32.

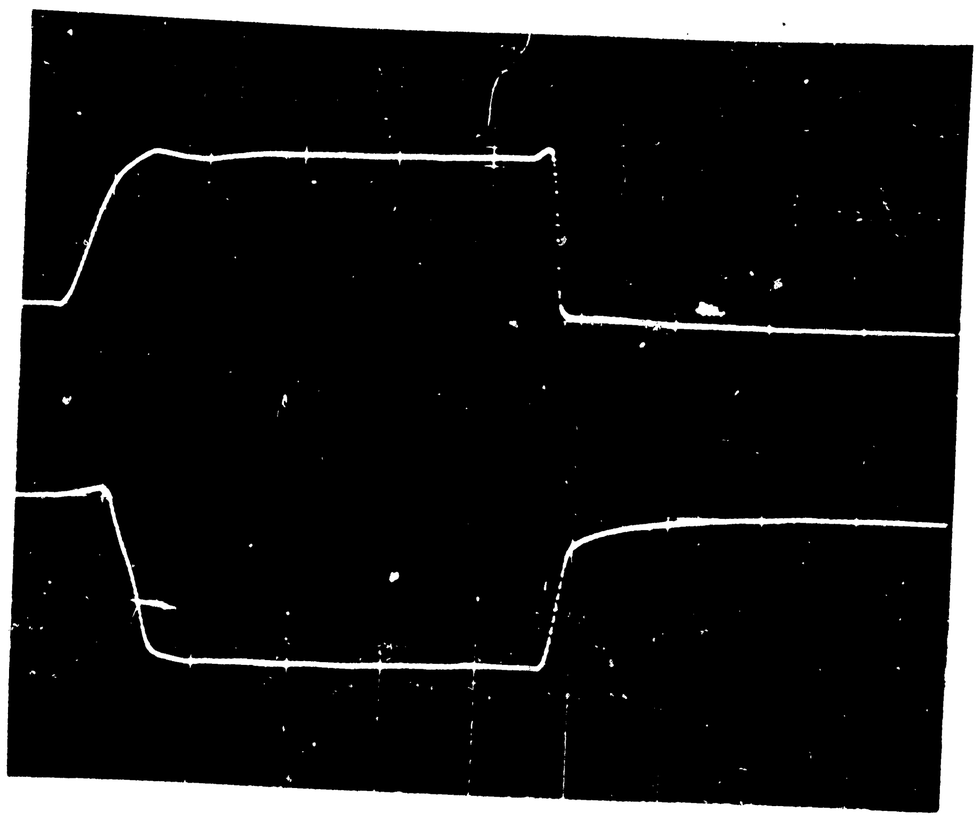
Type DTL No. 254G4 Temp +125°C V6 4.0 V5 -2.0 N = 3

	TEST CKT INPUT	TEST CKT OUTPUT V6 4.0 V5 -2.0
Pulse Width	500.	515.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.42	1.50
T_r	62.	71.
T_f	14.	24.
T_d		43.
T_s		28.
T_{pd}		35.

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. +25°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT. INPUT	TEST CKT. OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	465.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.76	1.75
T_r	61.	70.
T_f	13.	43.
T_d		52.
T_s		9.
T_{pd}		34.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DTL No. 254G4 Temp. -40°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	425.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.90	1.86
T_r	63.	56.
T_f	16.	57.
T_d		62.
T_s		5.
T_{pd}		45.

Type DTL No. 254G4 Temp -55°C V6 +4.0 V5 -2.0 N = 5

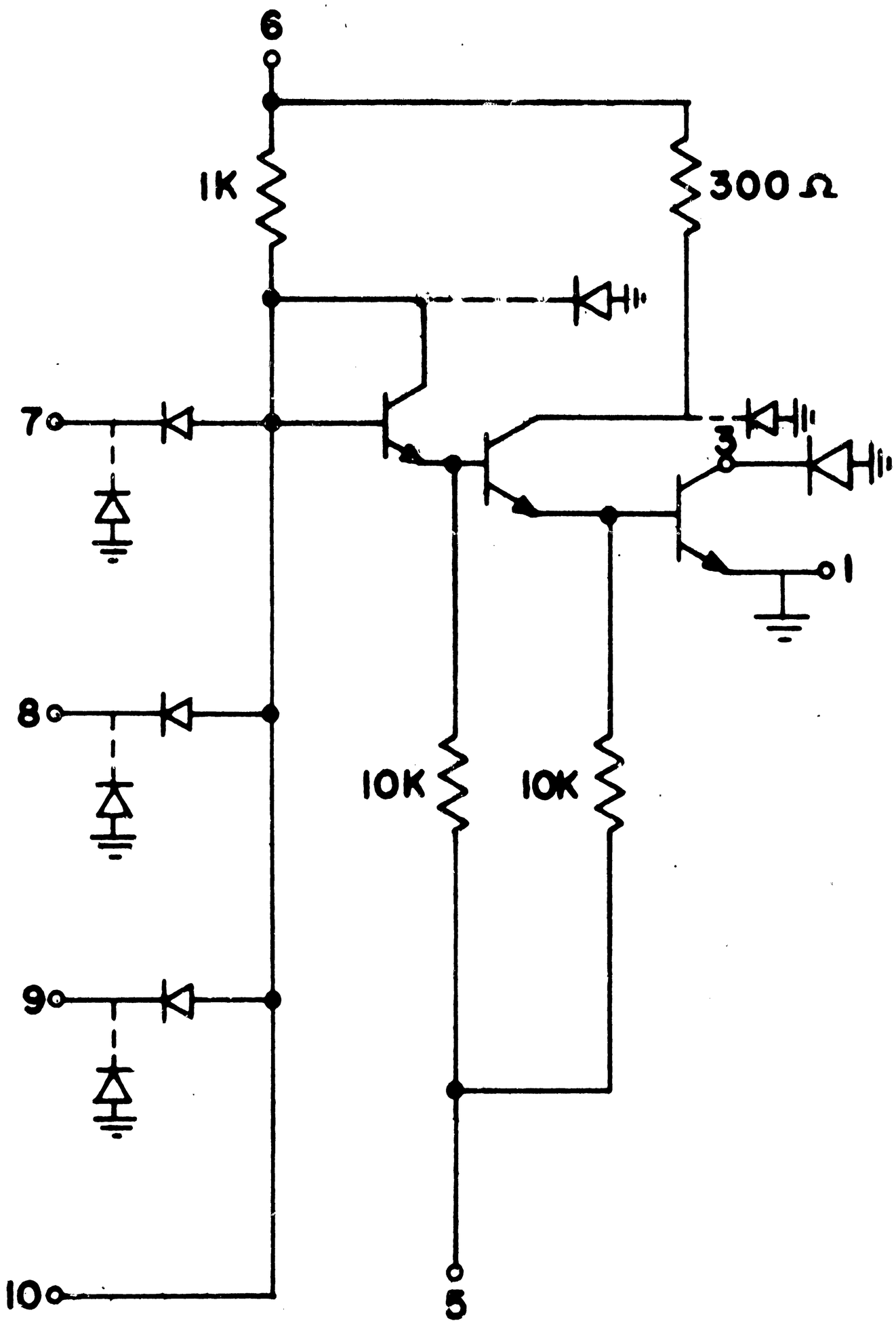
	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	411.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.94	1.83
T_r	64.	55.
T_f	18.	69.
T_d		67.
T_s		5.
T_{pd}		50.

Type DTL No. 25434 Temp. +85°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	492.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.58	1.56
T_r	60.	78.
T_f	14.	46.
T_d		45.
T_s		16.
T_{pd}		31.

Type DTL No. 254G4 Temp +125°C V6 +4.0 V5 -2.0 N = 5

	TEST CKT INPUT	TEST CKT OUTPUT V6 +4.0 V5 -2.0
Pulse Width	500.	505.
Repitition Rate	1MC	1MC
Pulse Amplitude	1.44	1.44
T_r	62.	84.
T_f	14.	54.
T_d		43.
T_s		23.
T_{pd}		33.



264P 3-INPUT DTL POWER NOR GATE

3.2.110

TABLE FOR PROPAGATION DELAY versus TEMPERATURE CURVE

(Temperature -°C)	T_{pd} NS[1]	Period-NS	T_{pd} - NS[2]
-55	41	599	42.7
-40	40	614	43.9
+25	47	717	50.5
+85	58	905	64.6
+125	66	1000	71.4

TEST CONDITIONS: Nine DTL Power Gates Connected in a Ring Oscillator
$V_6 = +4.0$ $V_5 = -2.0$ $V_1 = 0$

NOTES:

1. Measured as defined in data section:

$$T_{pd} - \frac{T_1 + T_2}{2}$$

T_1 = Time between 50% of input leading edge and 50% of output leading edge.

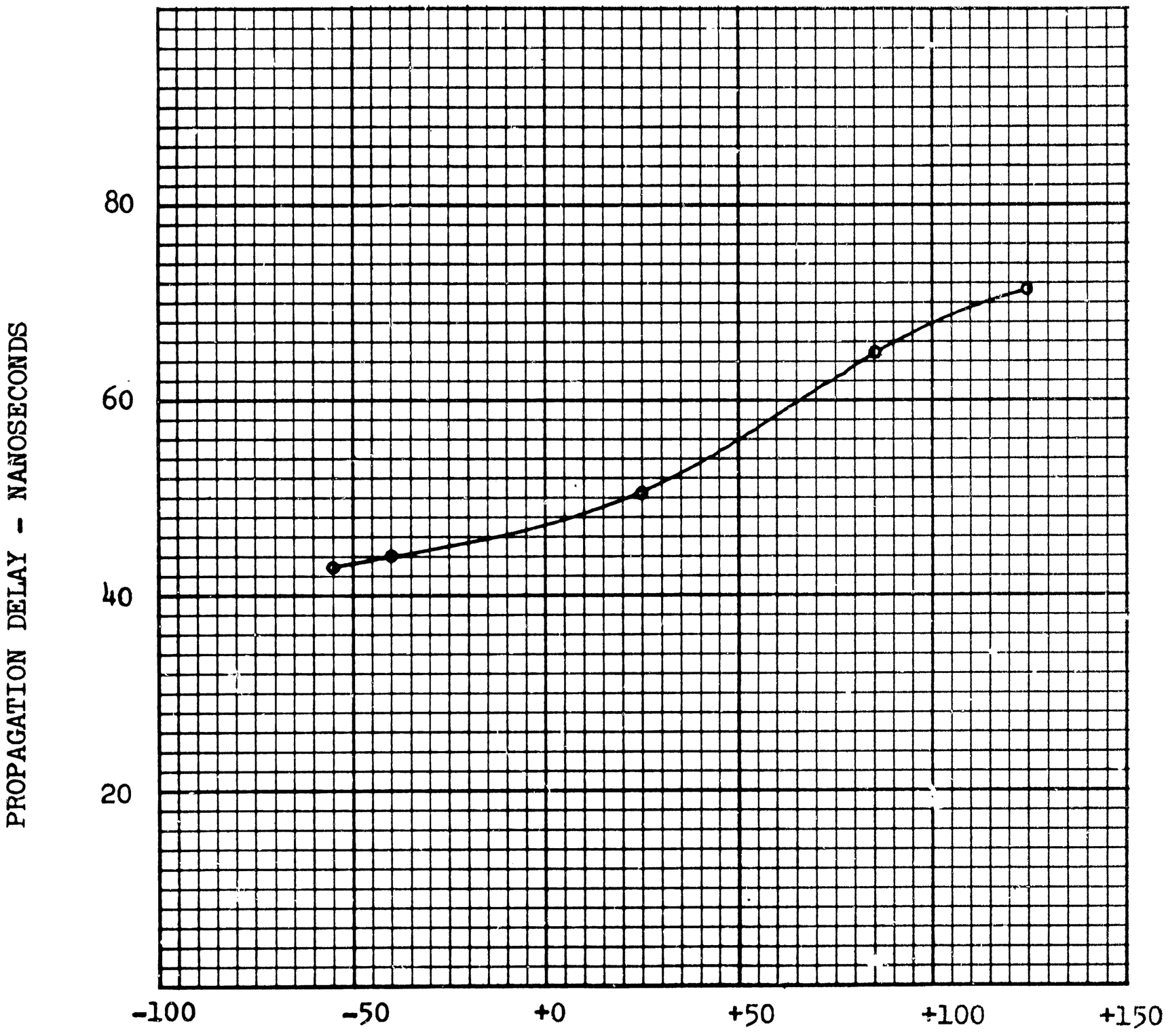
T_2 = Time between 50% of input trailing edge and 50% of output trailing edge.

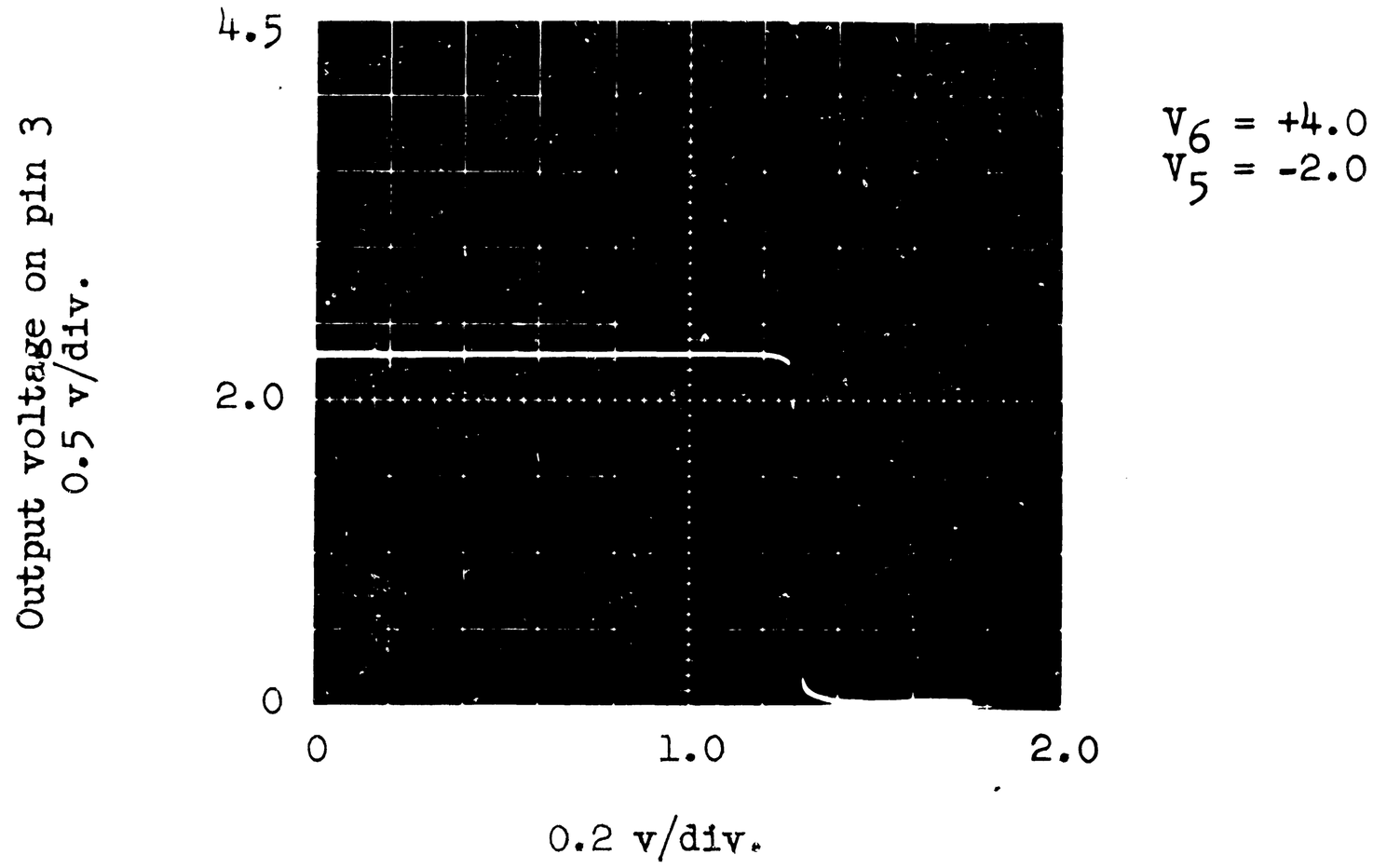
2. Defined as:

$$T_{pd} = \frac{\text{Period}}{2N}$$

N is total number of circuits in the ring oscillator.

PROPAGATION DELAY versus TEMPERATURE

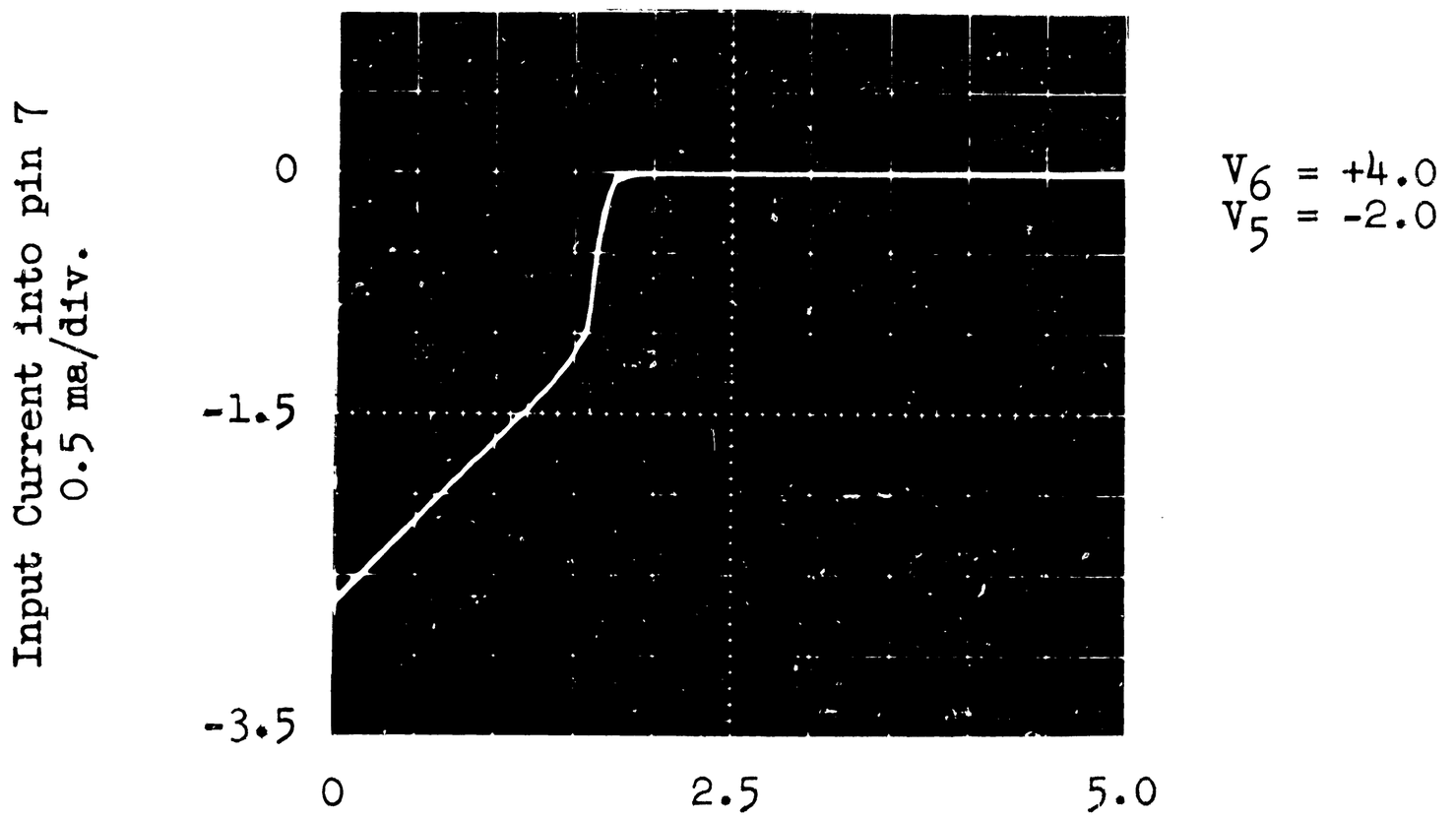




NOTE: The test gate was connected to drive the direct input of a similar gate for proper biasing conditions.

INPUT - OUTPUT CHARACTERISTICS

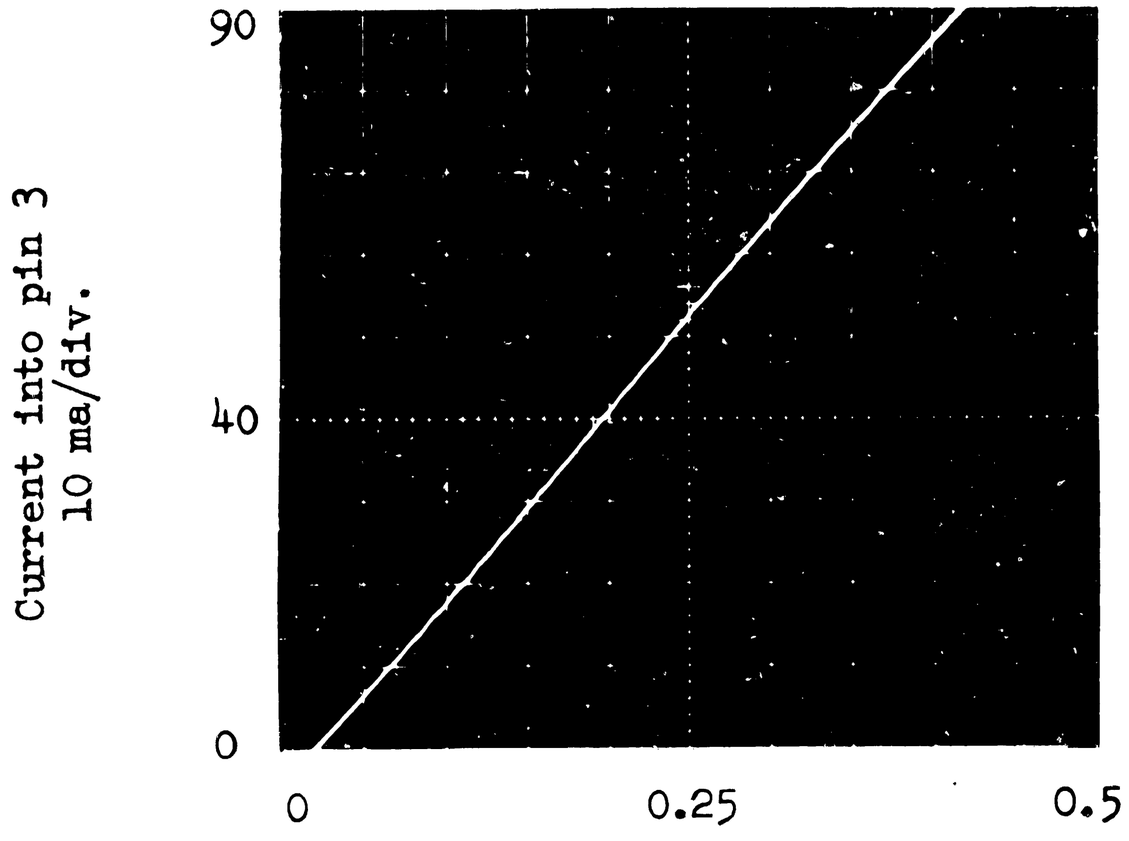
DTL - 264P



NOTE: Refer to note on Input Output Characteristics.

INPUT CHARACTERISTICS

DTL - 264P

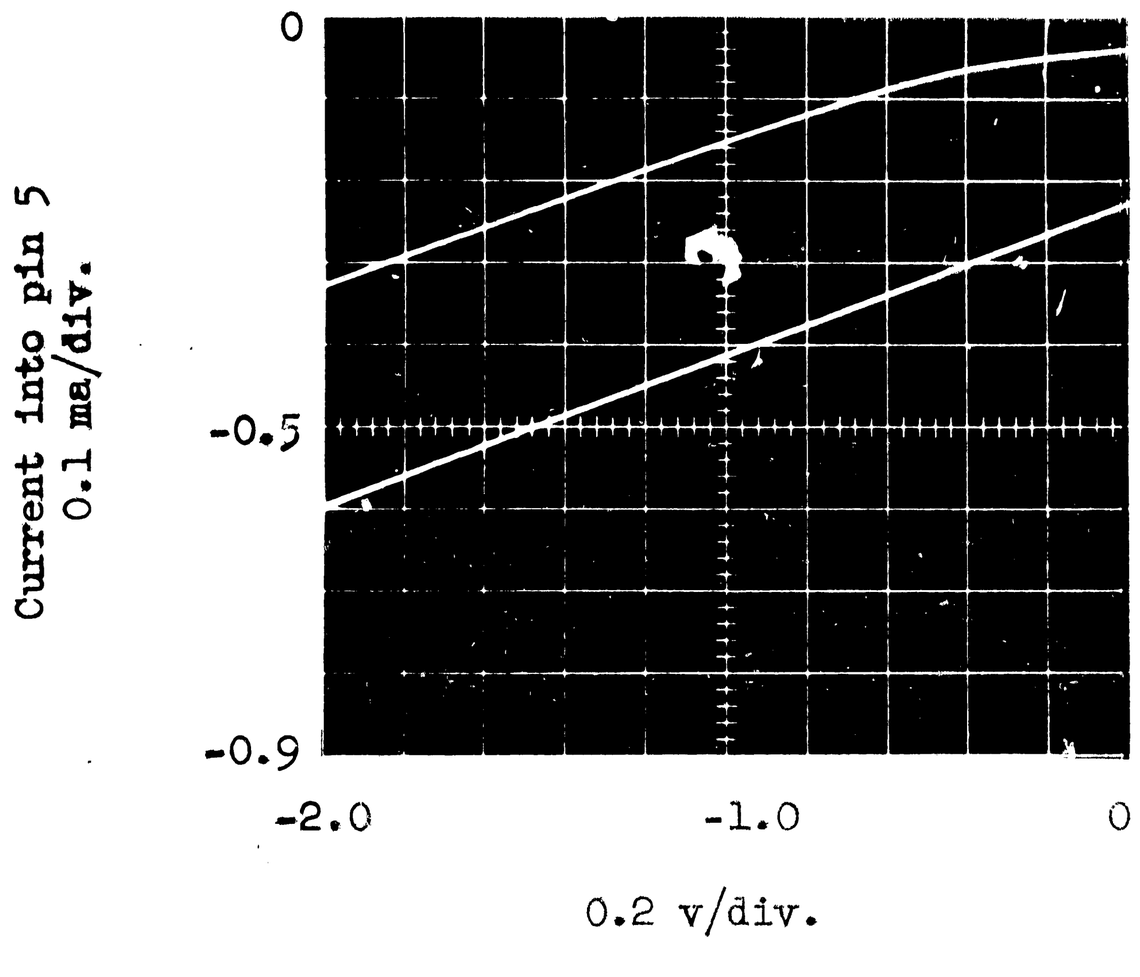


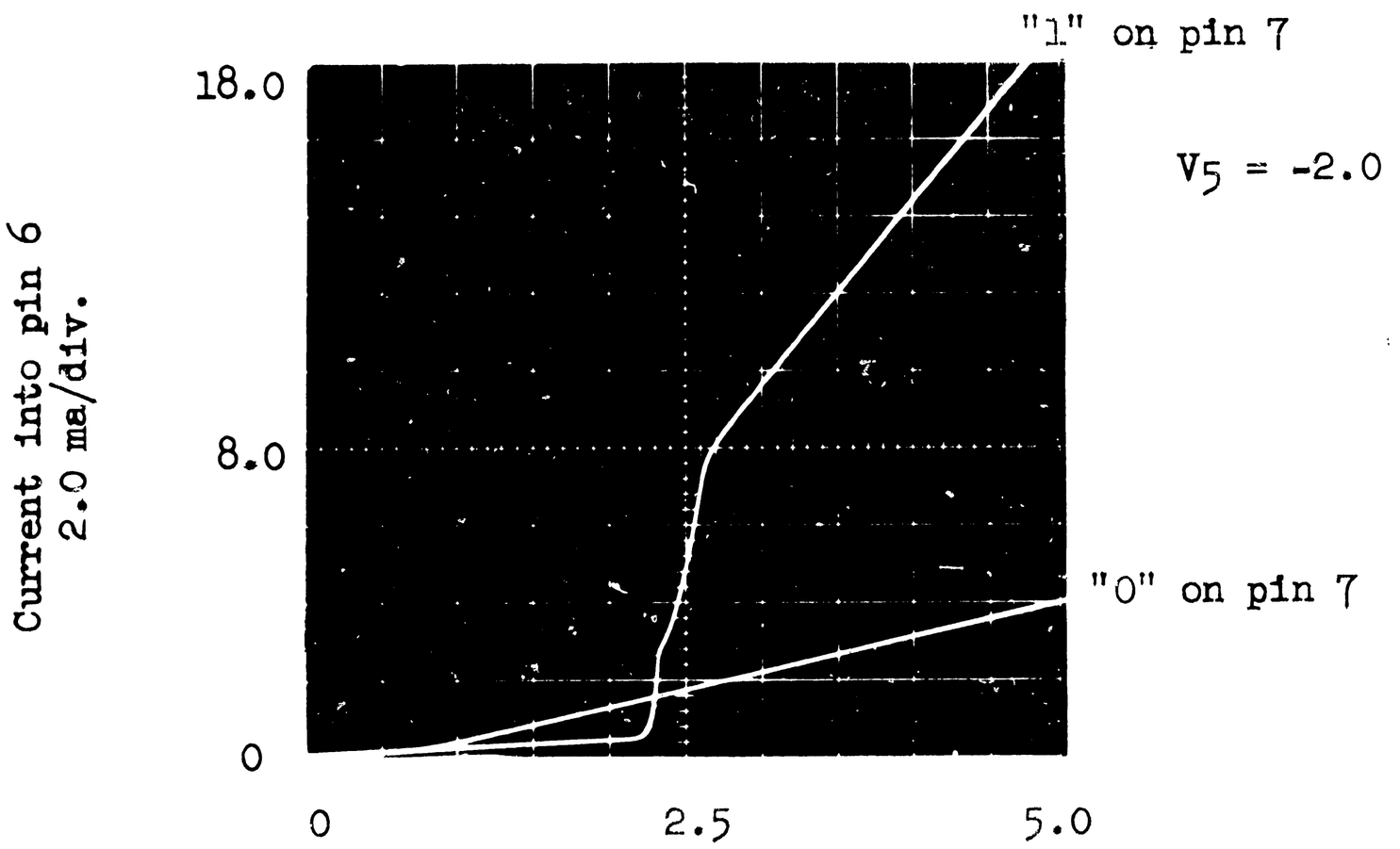
V_6 = +4.0
V_5 = -2.0
V_7 = +2.0

NOTE: Test ran "unloaded".

OUTPUT CHARACTERISTICS

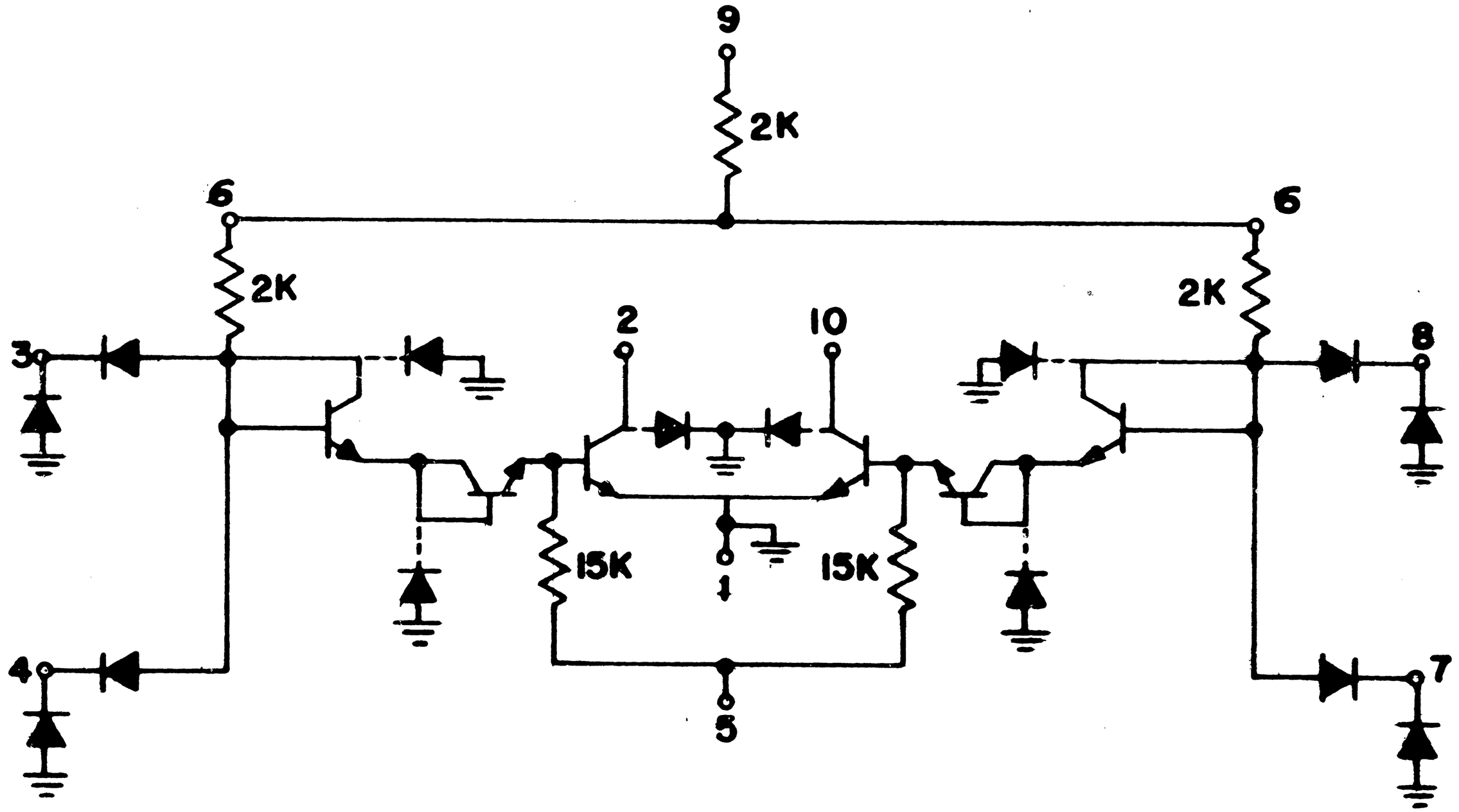
DTL - 264P



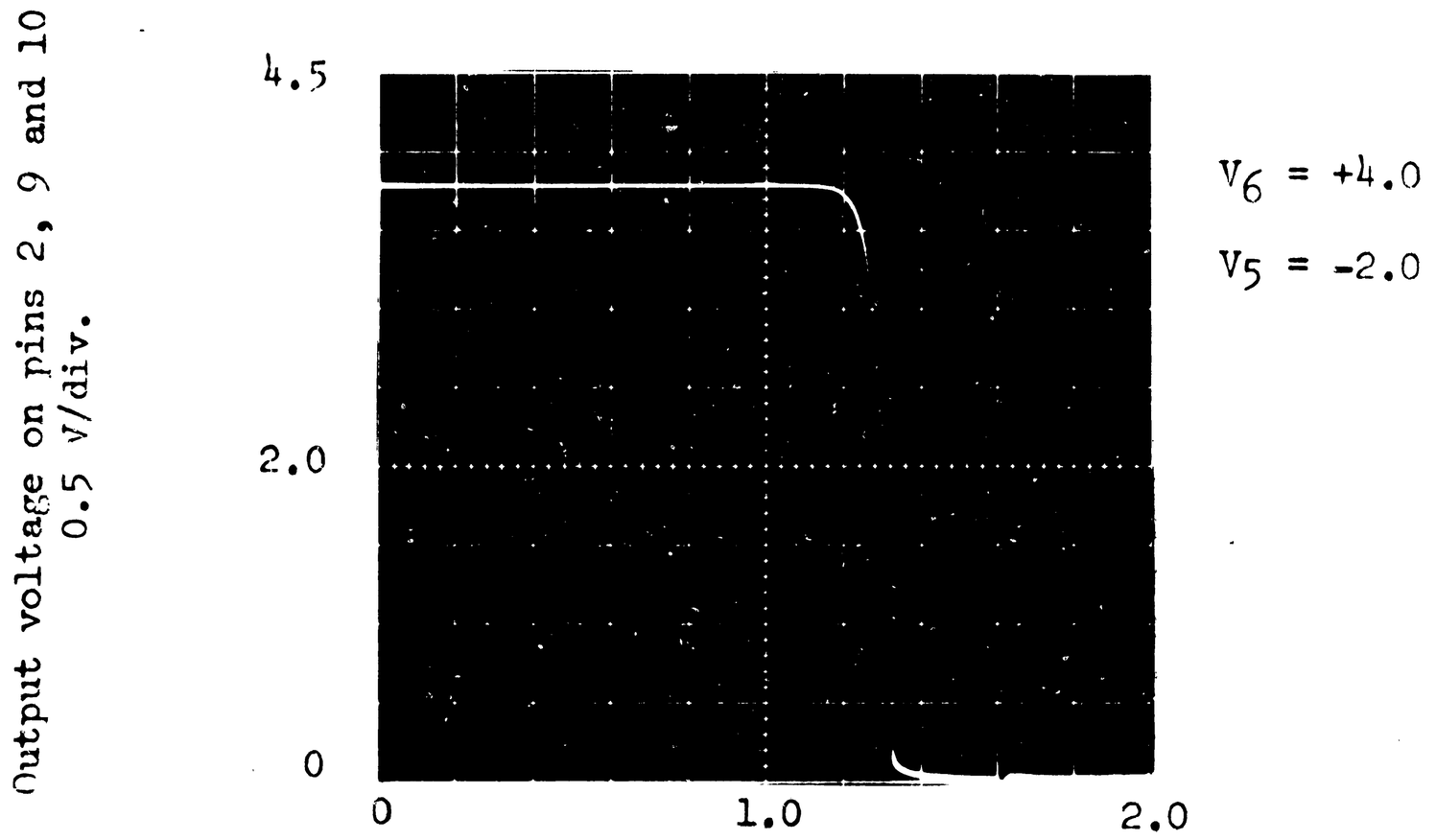


NOTE: Tests performed with 1K ohm pull-up resistor between pin 6 and pin 3.

POWER DISSIPATION CURVES
DTL - 264P

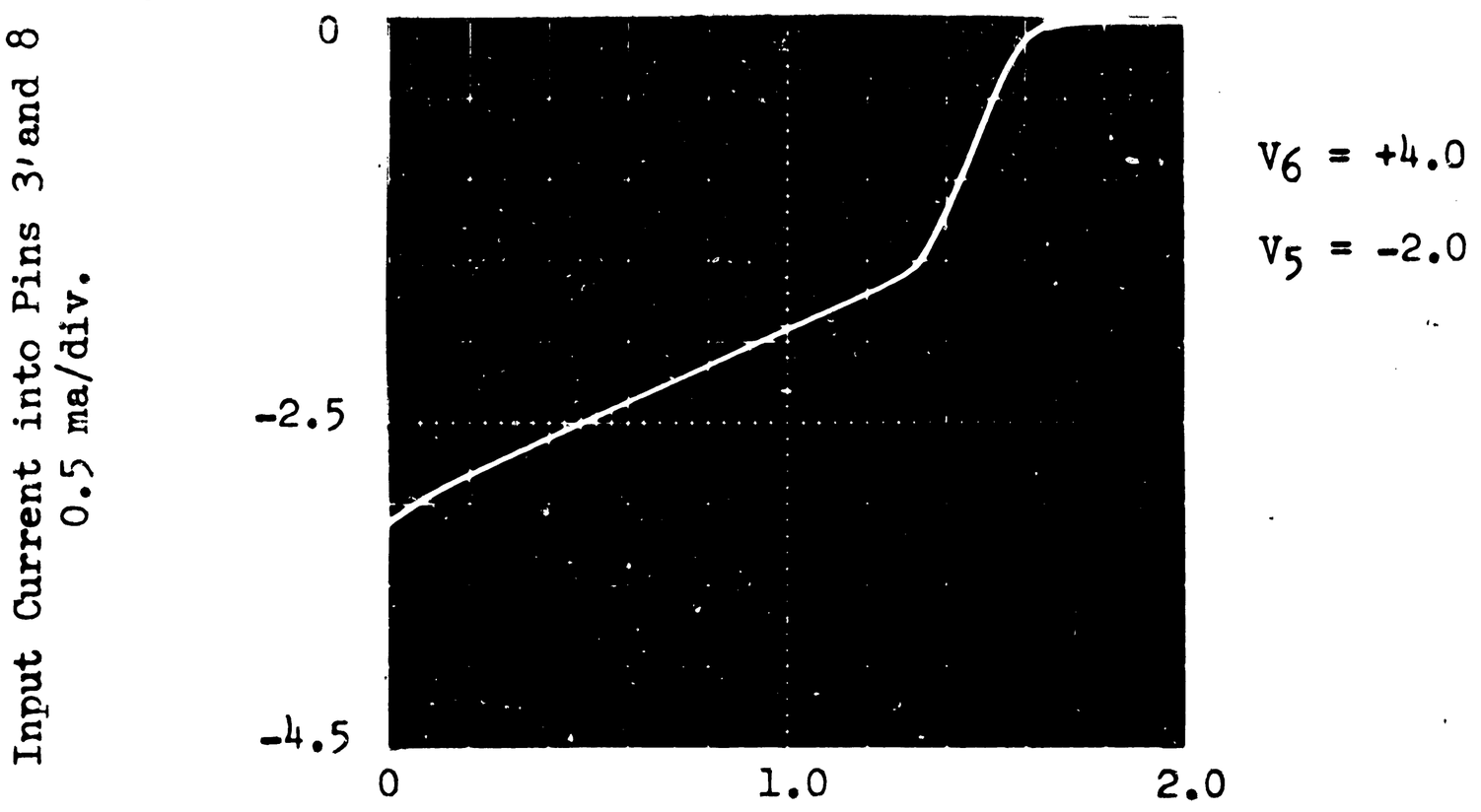


$264D_2$ DUAL 2-INPUT DTL GATE/EXCLUSIVE OR ELEMENT

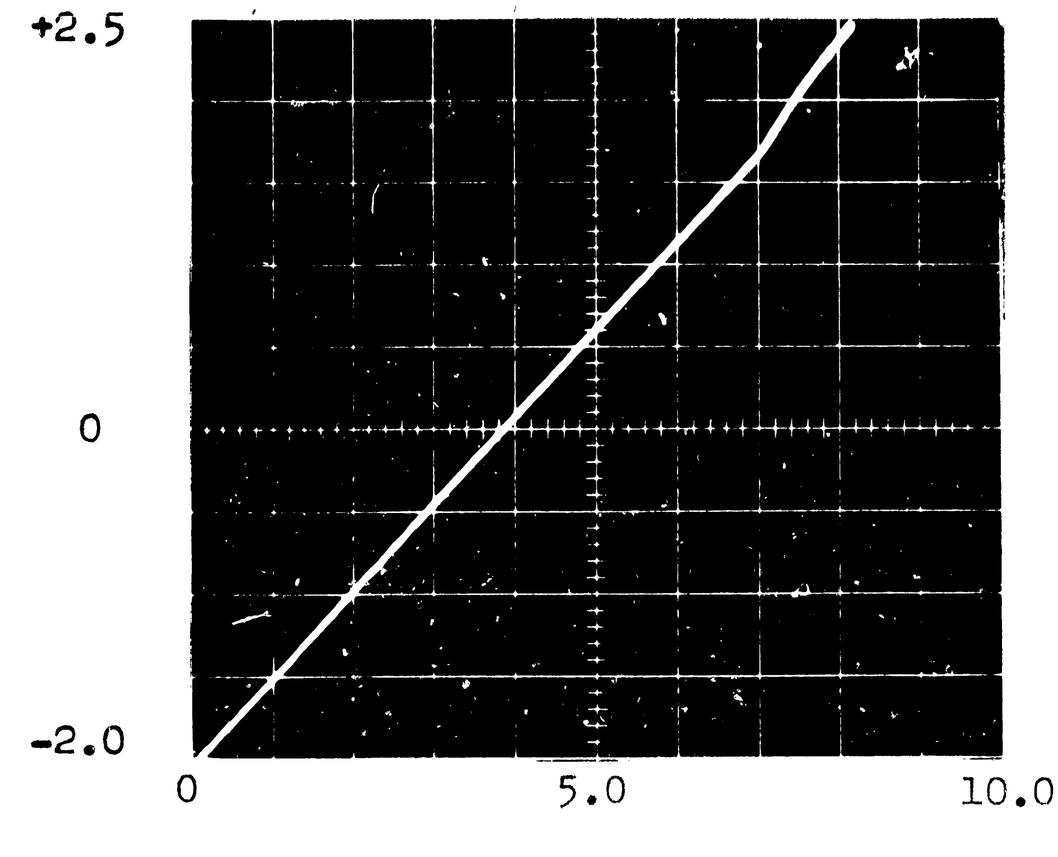


NOTE: Input pins 3 and 8 tied common.
Output pins 2 and 10 tied to pin 9
to utilize the pull up resistor

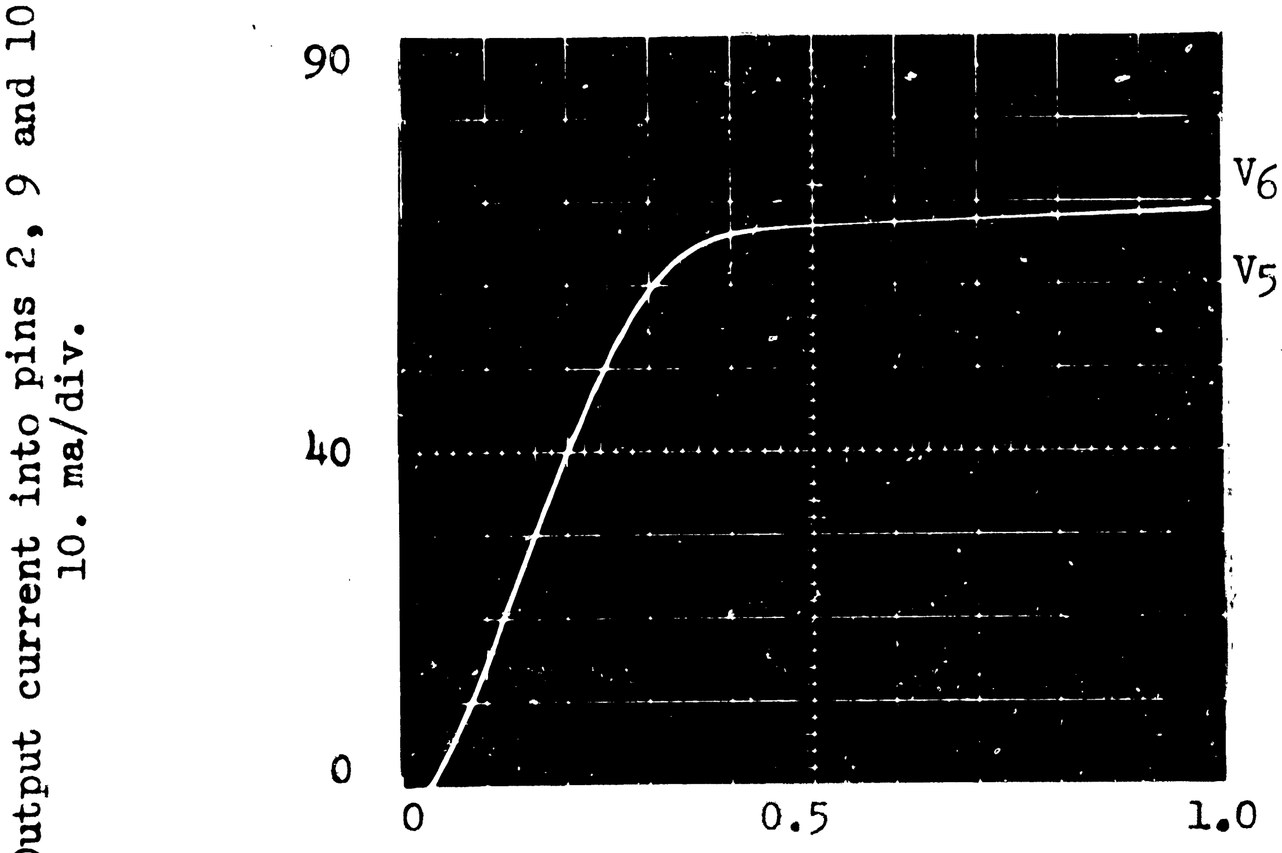
INPUT OUTPUT CHARACTERISTICS
DTL-264D2



INPUT CHARACTERISTICS
DTL 264D2

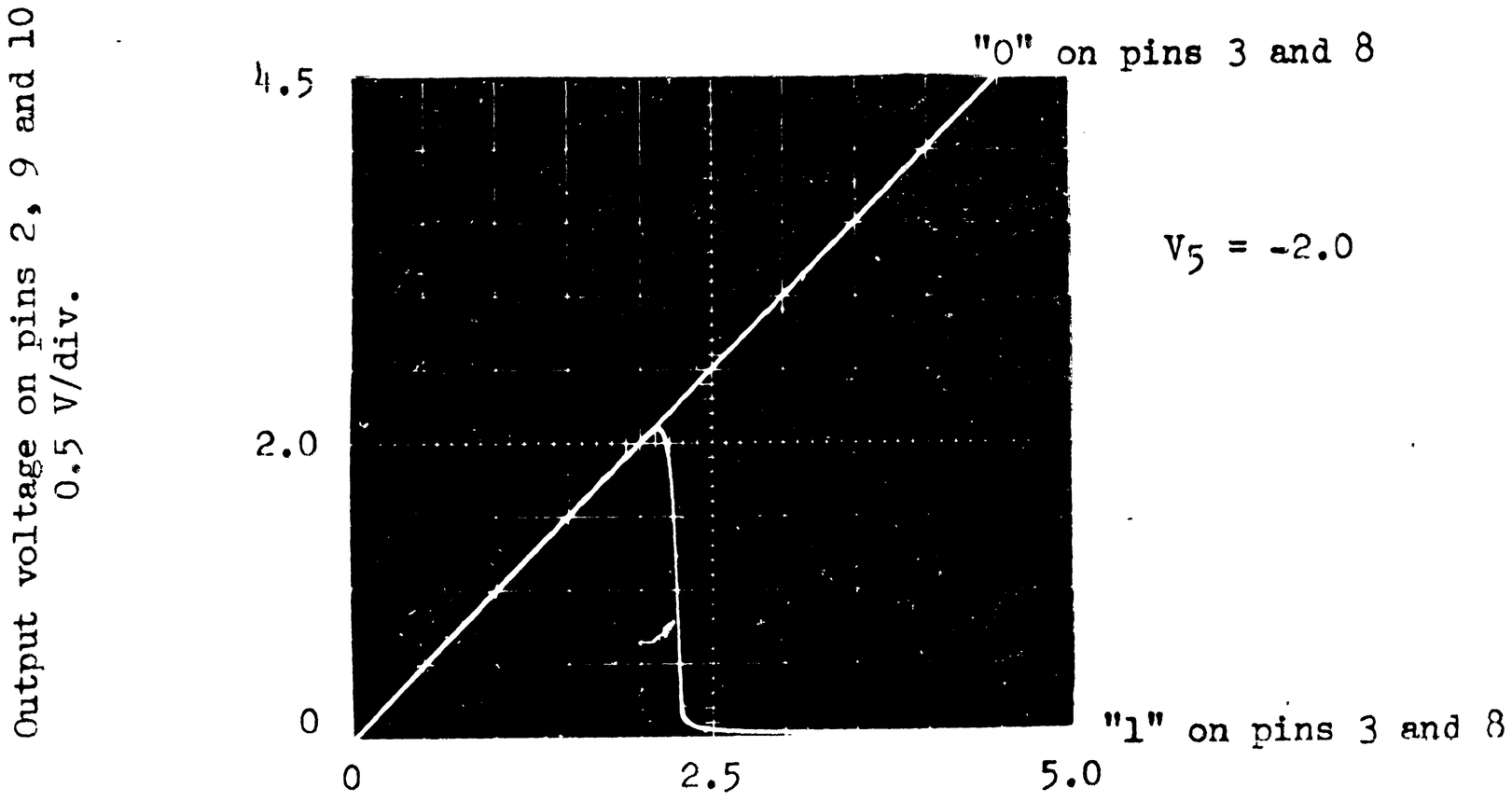


1.0 V/div.
Output Voltage on Pins 2, 9 and 10

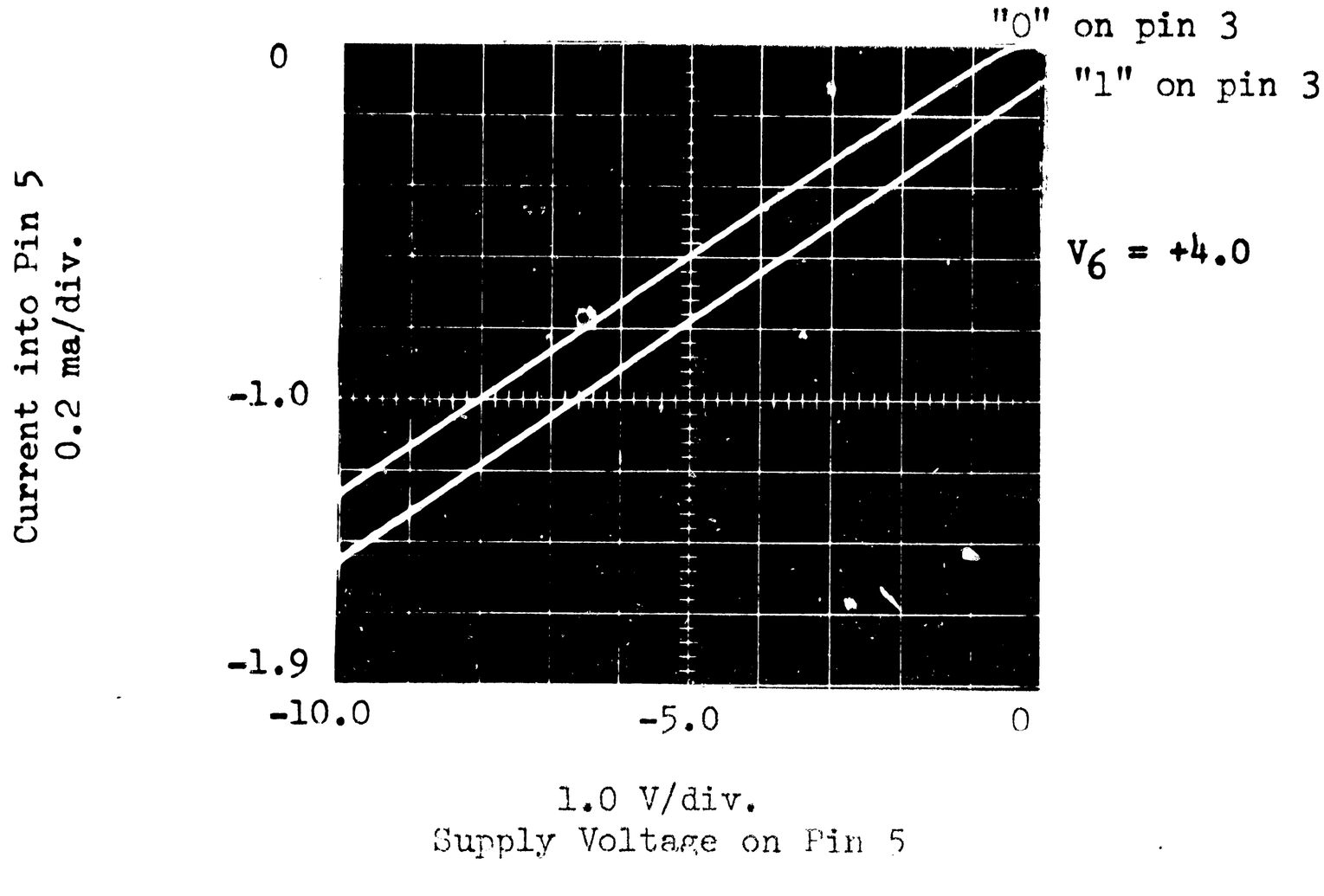


0.1 V/div.
Output Voltage on Pins 2, 9 and 10

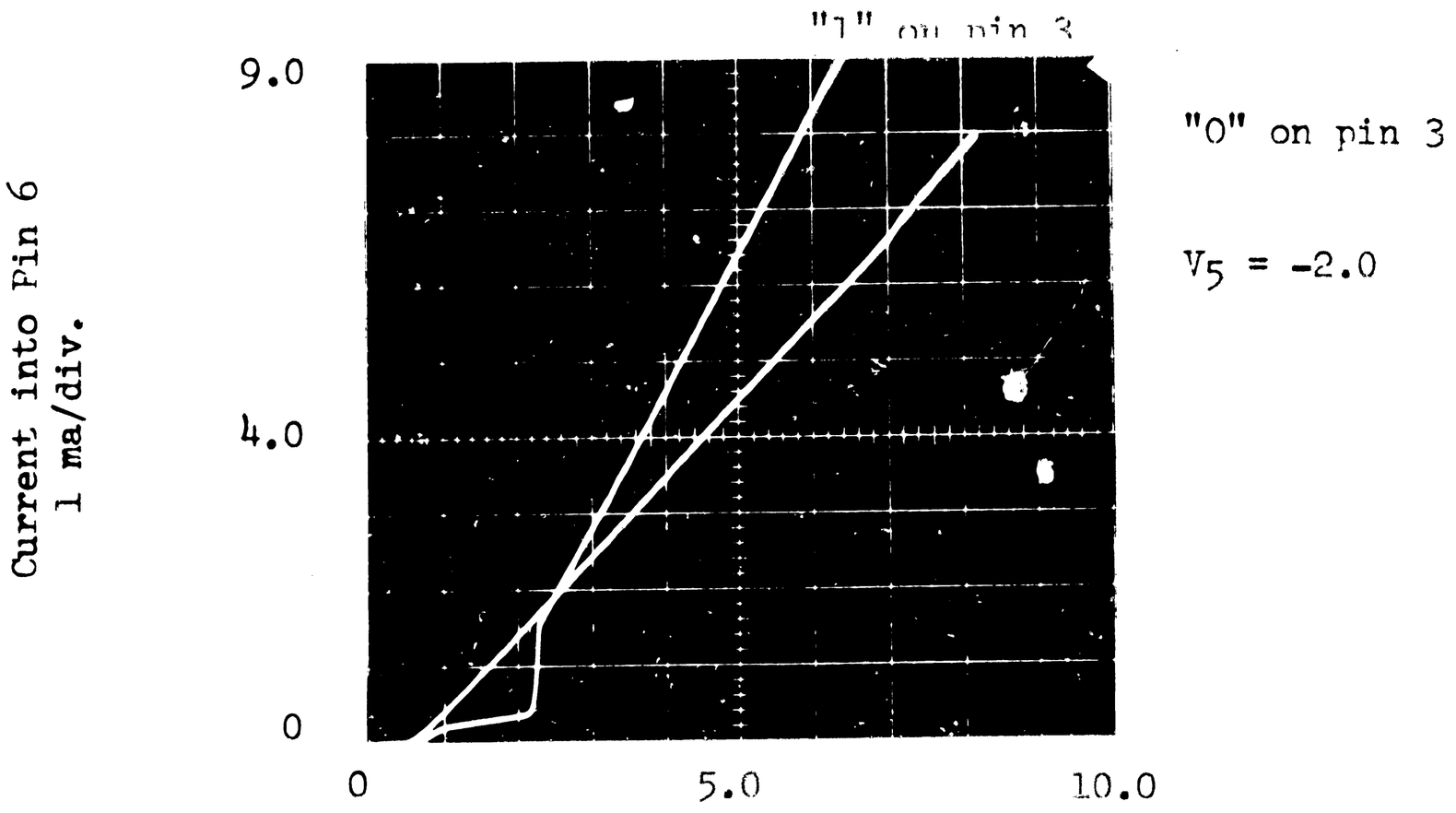
OUTPUT CHARACTERISTICS
DTL 264D2



OUTPUT VOLTAGE versus SUPPLY VOLTAGE
DTL 264D2

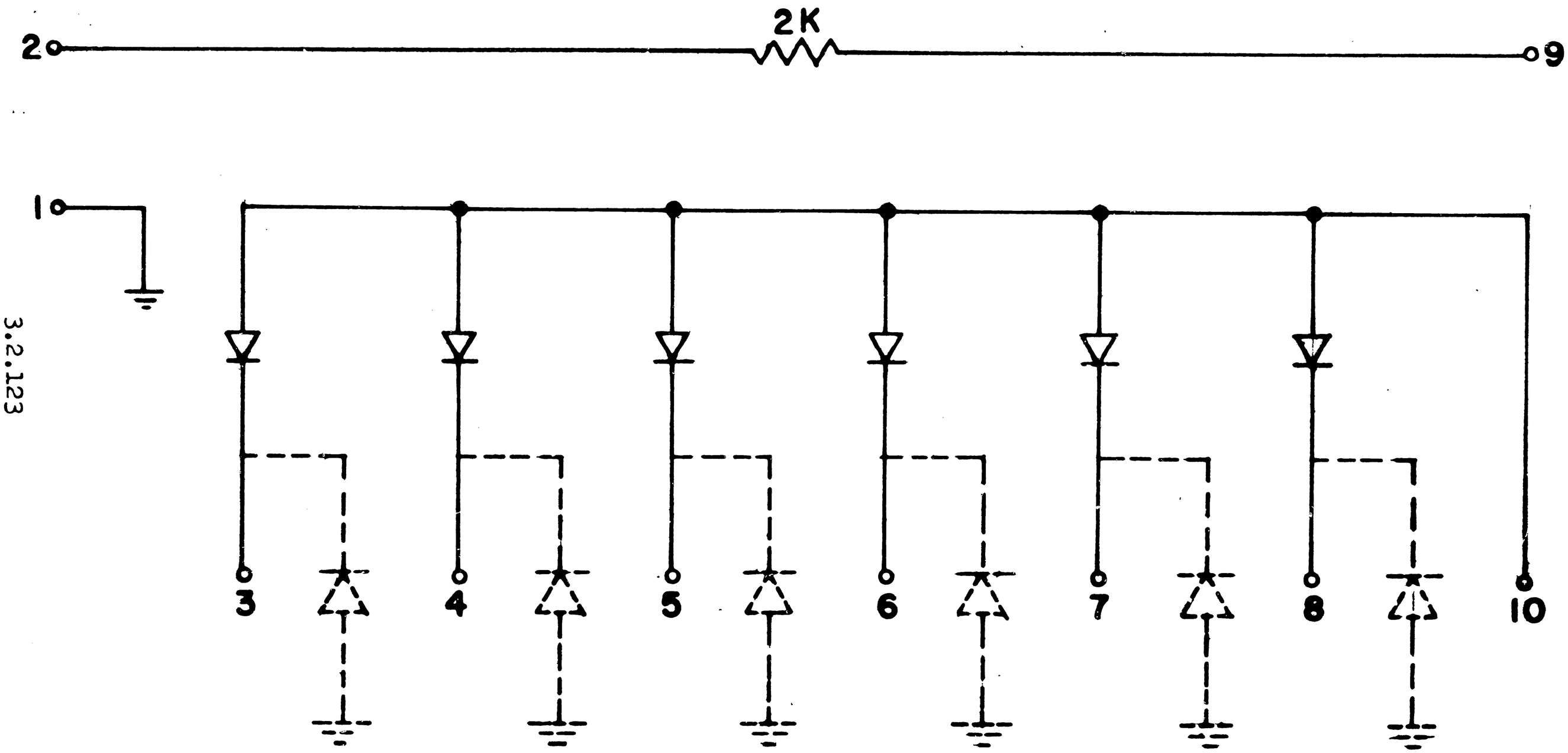


1.0 V/div.
Supply Voltage on Pin 5

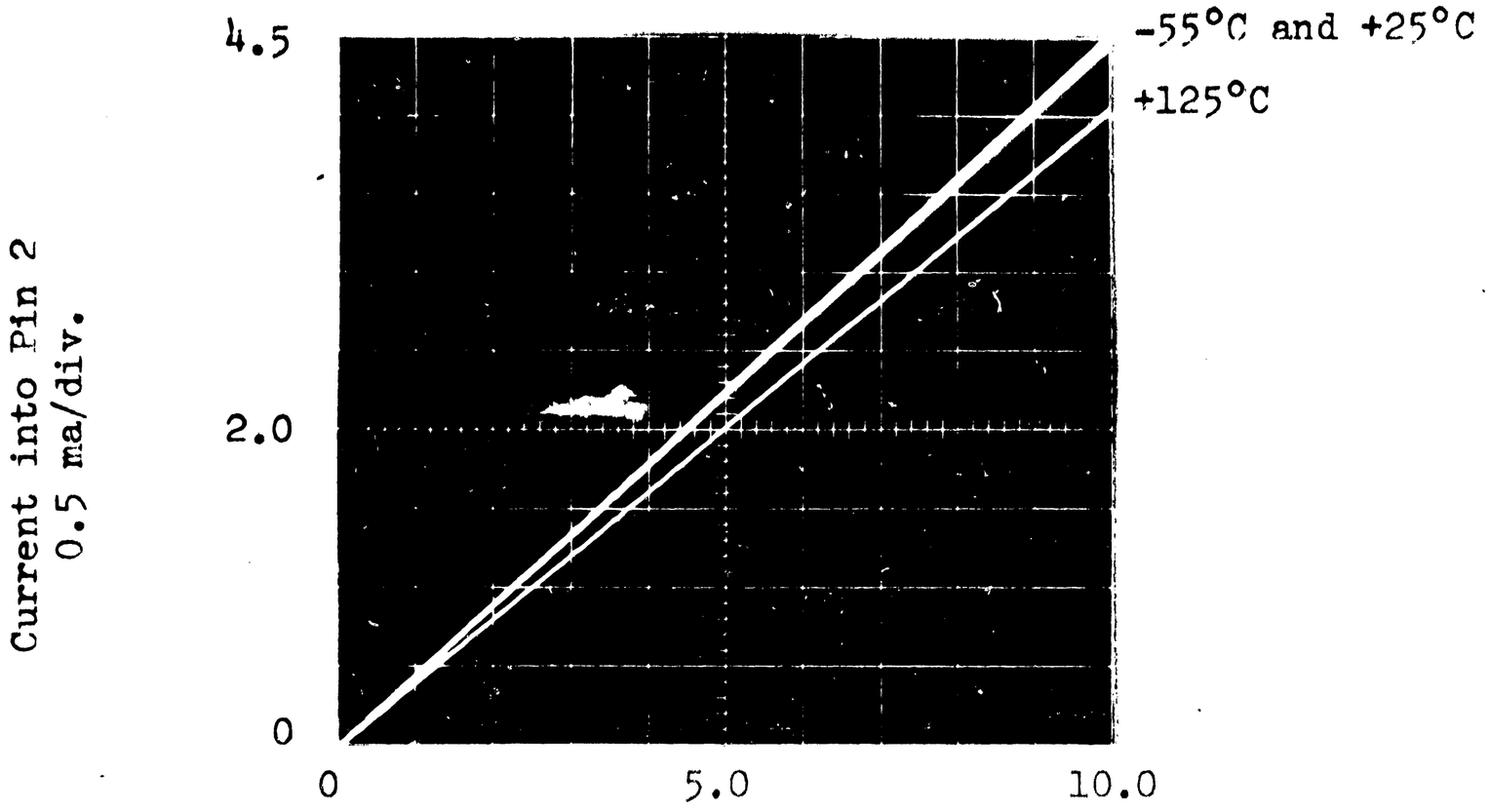


1 V/div.
Supply Voltage on Pin 6

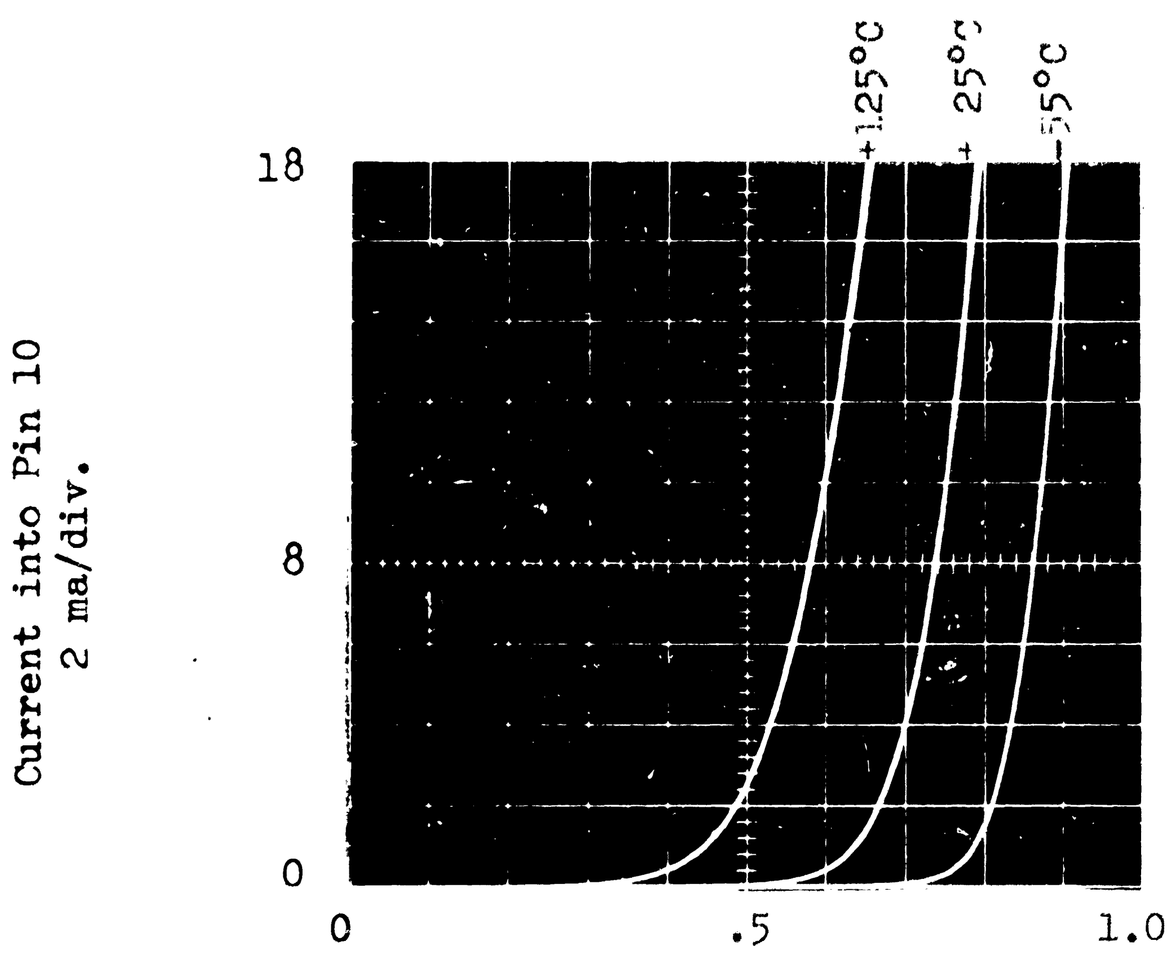
POWER DISSIPATION CURVES
DTL 264D?



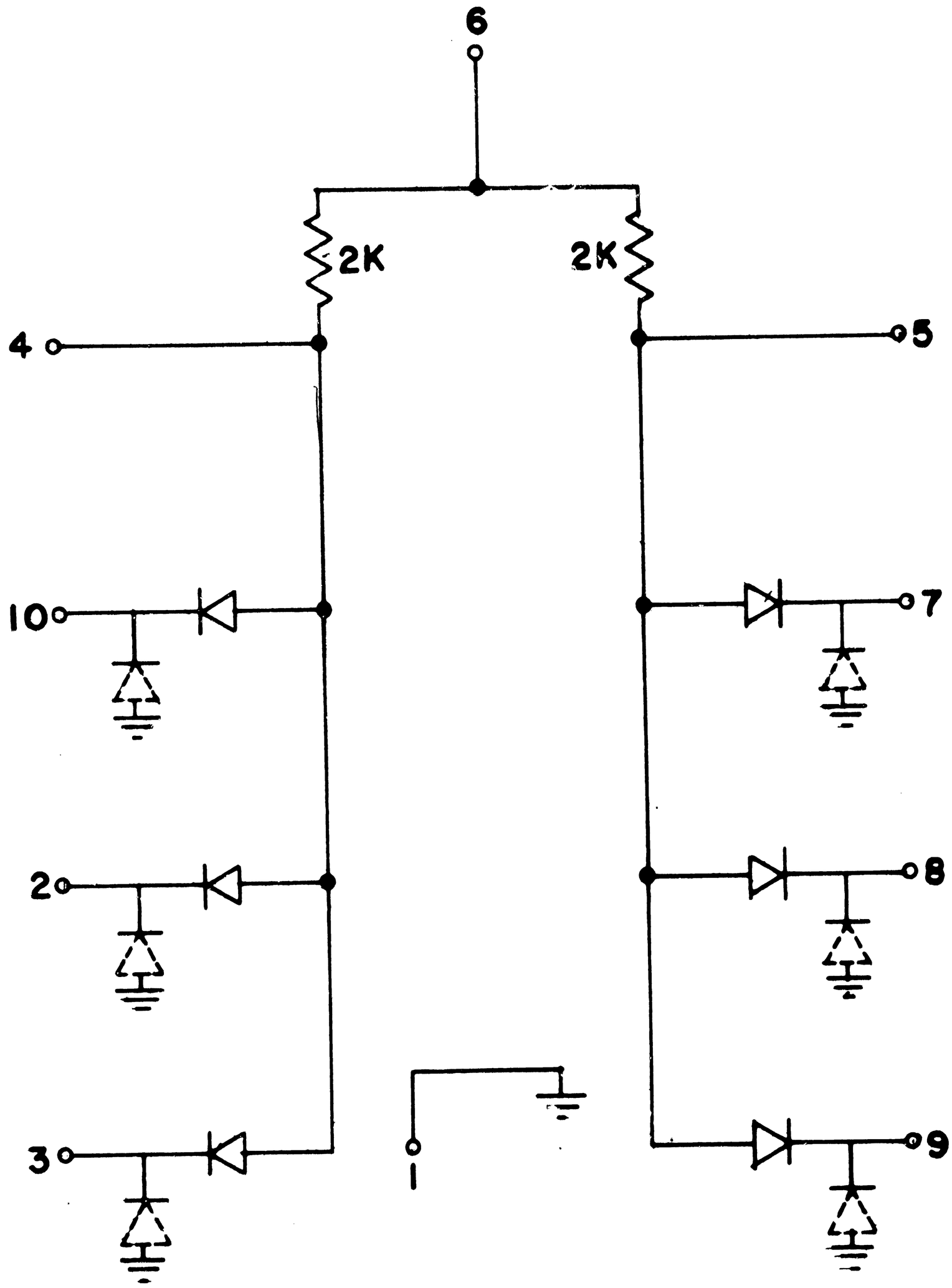
254G6 6-INPUT DIODE AND GATE



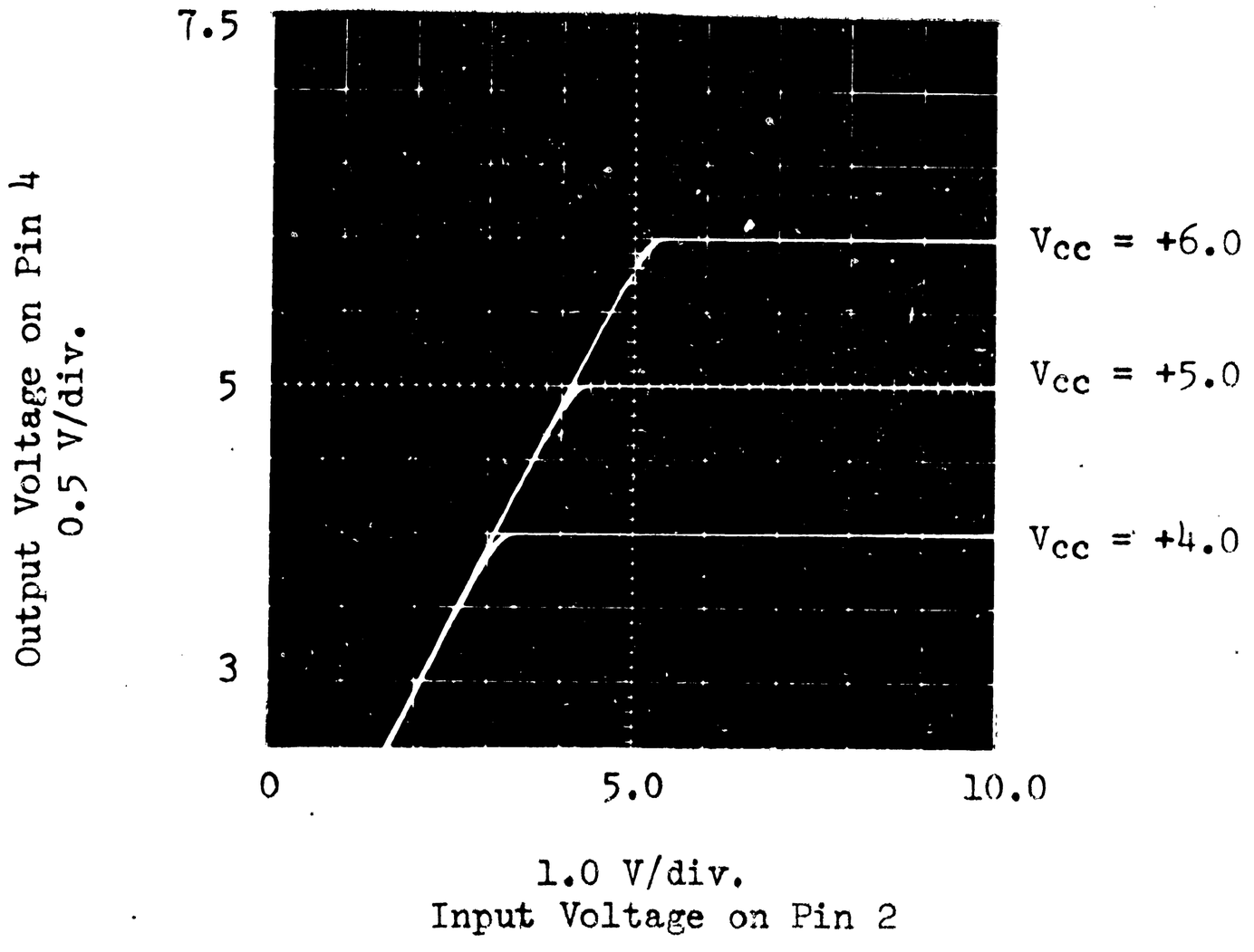
RESISTOR CHARACTERISTICS



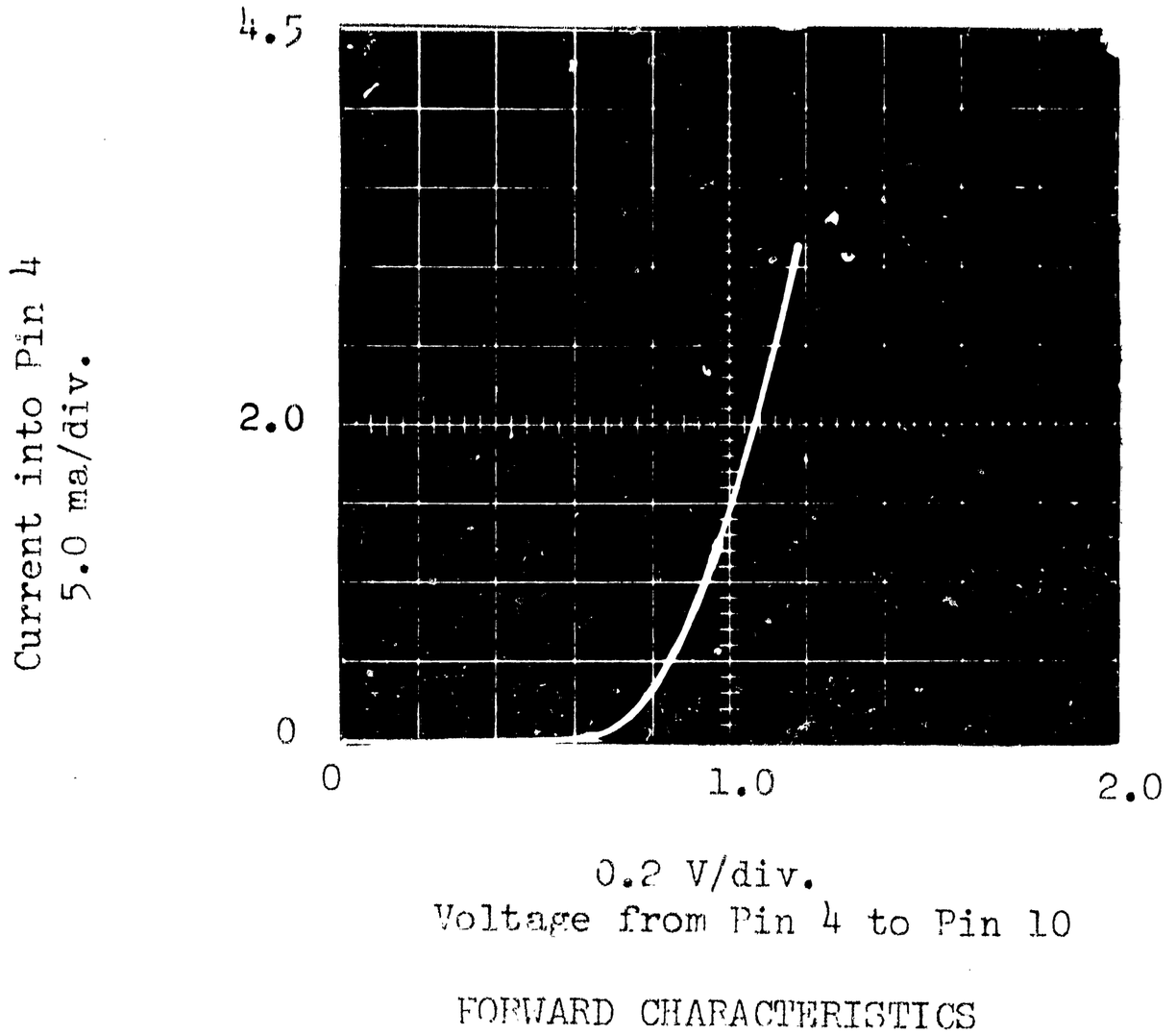
DIODE FORWARD CHARACTERISTICS
DTL 254G6



254D3 DUAL 3-INPUT DIODE AND GATE

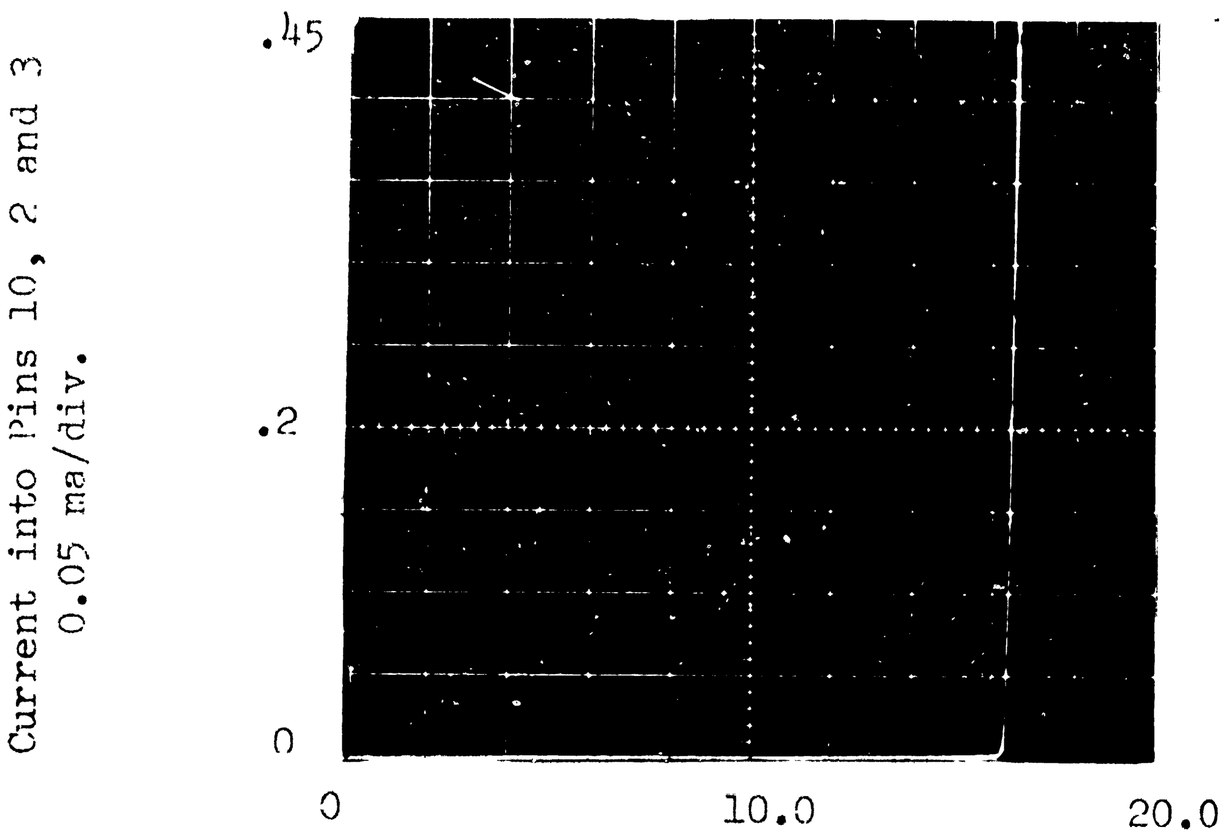


INPUT - OUTPUT CHARACTERISTICS
DTL 254D3



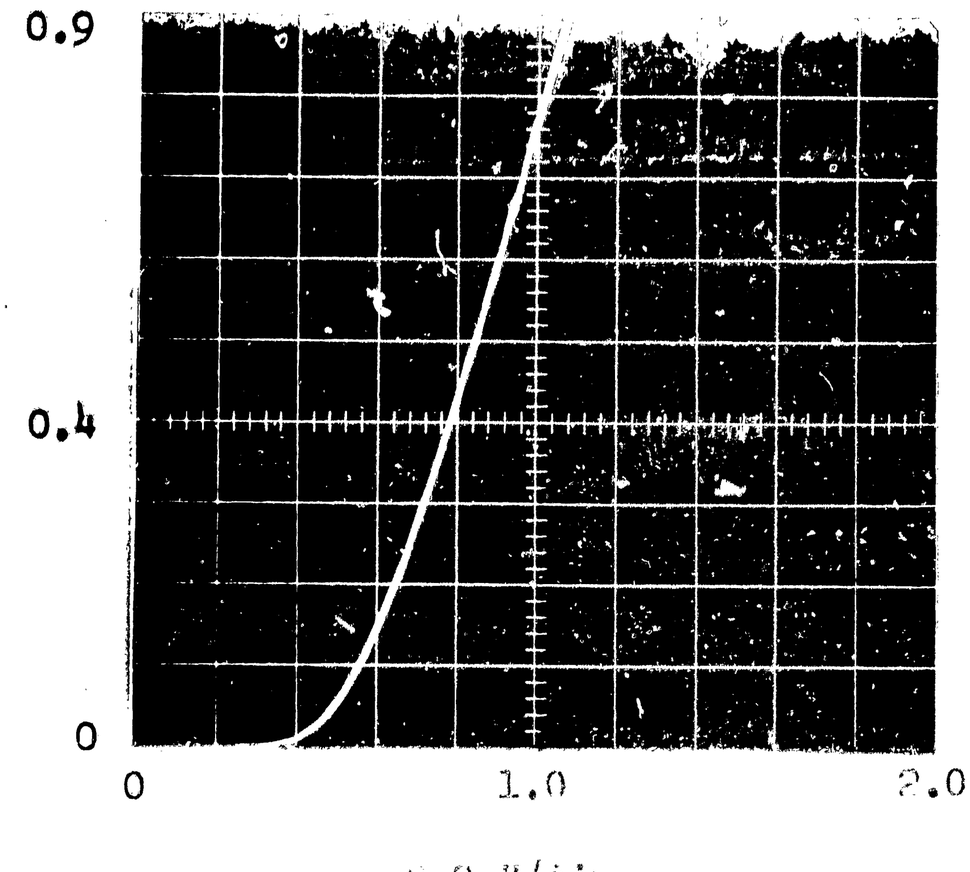
0.2 V/div.
Voltage from Pin 4 to Pin 10

FORWARD CHARACTERISTICS

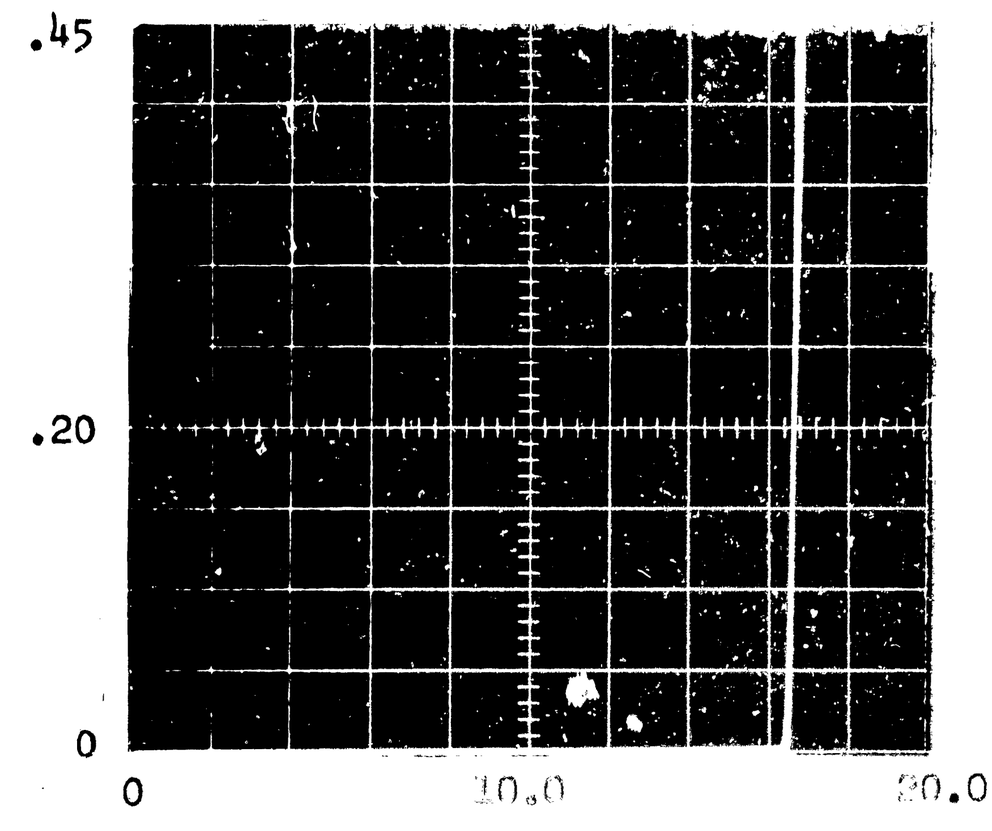


2.0 V/div.
Voltage from Common Input
Pins 10, 2 and 3 to Pin 4

REVERSE CHARACTERISTICS
INPUT DIODE CHARACTERISTICS
DTL 254D3



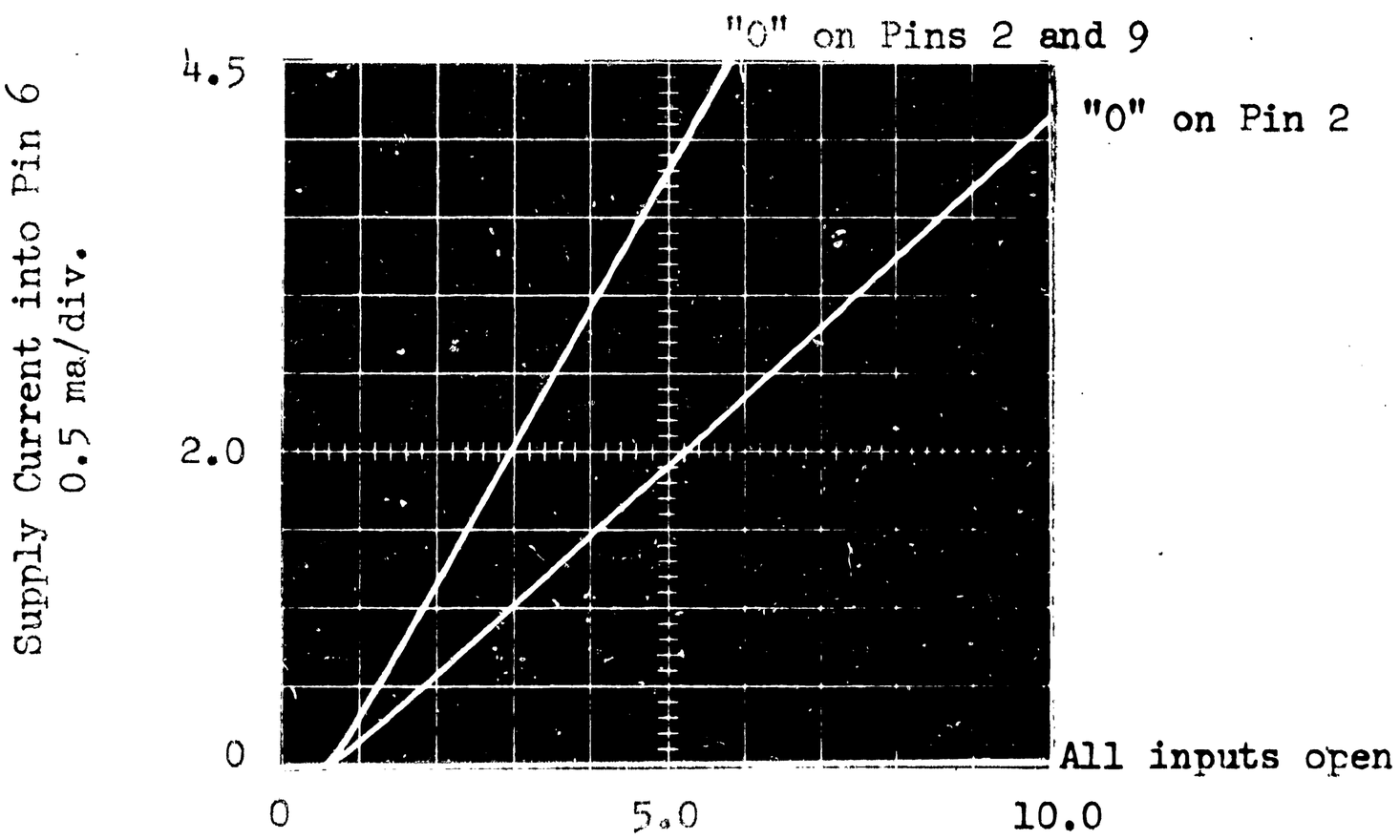
FORWARD CHARACTERISTICS



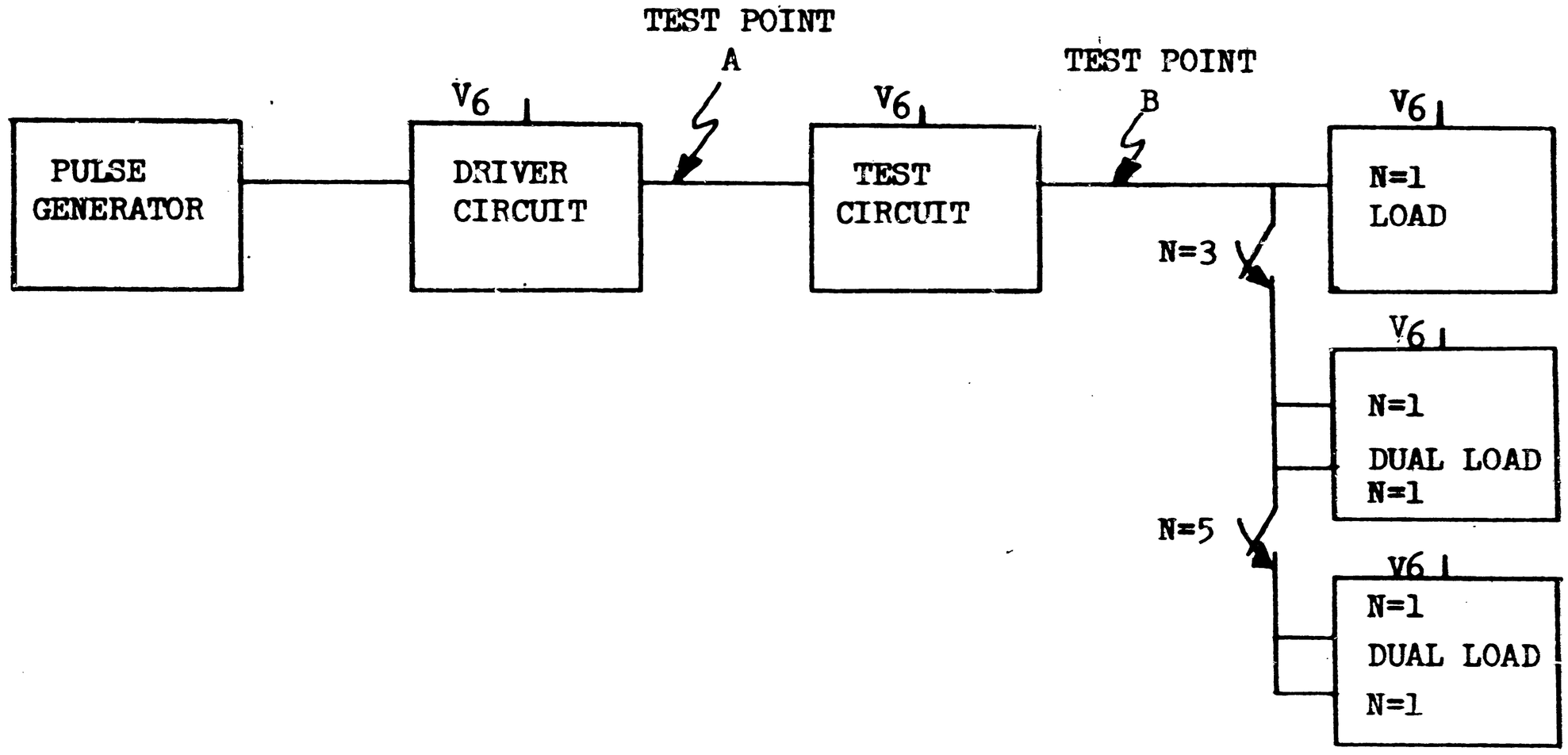
REVERSE CHARACTERISTICS

ISOLATION DIODE CHARACTERISTICS
MDL 25AD3

3.2.126



POWER DISSIPATION
DEL 25413



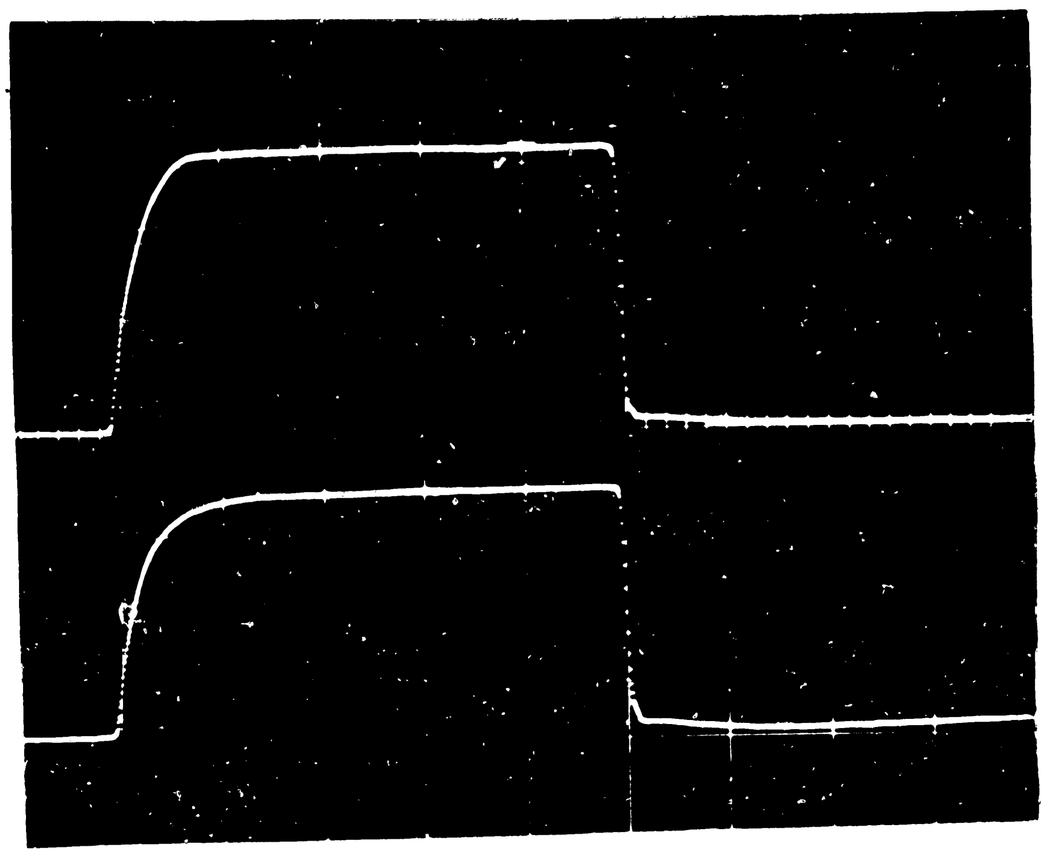
3.2.130

TEST CIRCUIT FOR DIODE AND GATE 254D3

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. +25°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	506.	501.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.84	1.60	2.40	2.82
T_r	53.	37.	60.	45.
T_f	12.	12.	11.	12.
T_d		0.	0.	2.
T_s		4.	2.	1.
T_{pd}		2.	1.5	2.0



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. $254D_3$ Temp. -40°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	508.	502.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.84	1.36	2.22	2.84
T_r	59.	33.	58.	52.
T_f	11.	11.	11.	11.
T_d		1.0	1.2	2.0
T_s		4.0	2.8	1.0
T_{pd}		2.0	1.4	1.5

Type DL No. $254D_3$ Temp. -55°C Vcc 4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	509.	503.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.90	1.31	2.22	2.90
T_r	64.	34.	61.	55.
T_f	11.	13.	11.	11.
T_d		1.0	1.0	1.6
T_s		4.6	3.0	1.0
T_{pd}		2.0	1.5	1.5

GENERAL MICRO-ELECTRONICS

Type DL No. $254D_3$ Temp. +85°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	505.	500.	501.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.85	1.87	2.61	2.82
T_r	56.	44.	66.	46.
T_f	13.	13.	13.	12.
T_d		1.0	1.5	1.0
T_s		4.0	1.0	1.0
T_{pd}		1.5	1.5	2.0

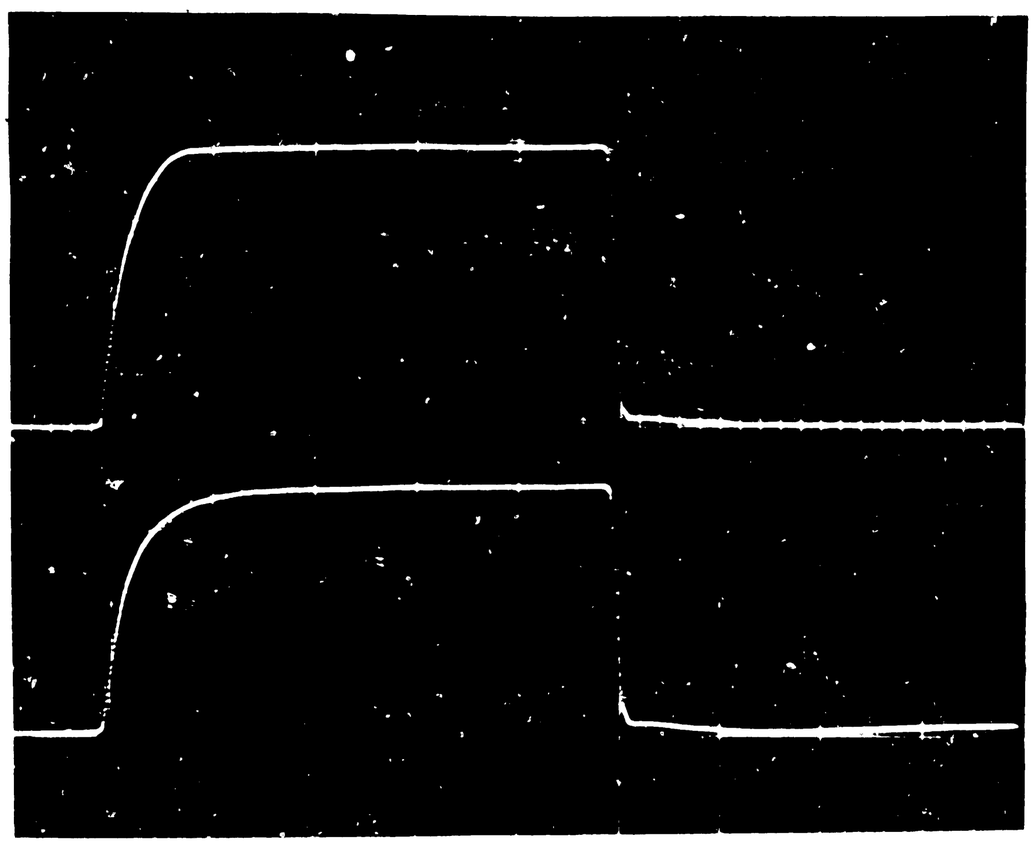
Type DL No. $254D_3$ Temp. +125°C Vcc +4.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	505.	502.	502.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.83	1.98	2.64	2.80
T_r	59.	51.	62.	47.
T_f	13.	14.	13.	13.
T_d		1.3	2.0	2.0
T_s		3.0	2.0	1.0
T_{pd}		2.0	2.5	2.0

GENERAL MICRO-ELECTRONICS

Type DL No. $254D_3$ Temp. +25°C Vcc 4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	505.	499.	500.
Repetition Rate	1MC	1MC	1MC	1MC
Pulse Amplitude	2.84	1.60	2.44	2.42
T_r	54.	40.	67.	49.
T_f	12.	12.	11.	12.
T_d		0.	2.0	2.0
T_s		4.0	3.0	1.2
T_{pd}		2.0	2.0	2.0



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. -40°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	507.	502.	499.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.82	1.34	2.24	2.86
T_r	58.	37.	66.	55.
T_f	11.	12.	11.	12.
T_d		1.0	1.8	2.0
T_s		4.0	2.9	1.0
T_{pd}		2.0	2.0	2.0

Type DL No. 254D3 Temp. -55°C Vcc 4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	508.	502.	499.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.88	1.30	2.16	2.83
T_r	59.	38.	67.	54.
T_f	11.	12.	11.	12.
T_d		1.0	1.0	2.0
T_s		4.6	3.0	1.0
T_{pd}		2.5	1.5	2.0

GENERAL MICRO-ELECTRONICS

Type DL No. $254D_3$ Temp. +85°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	505.	499.	501.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.75	1.83	2.56	2.76
T_r	54.	49.	70.	48.
T_f	12.	13.	13.	12.
T_d		1.2	2.0	1.6
T_s		4.0	1.5	1.0
T_{pd}		2.0	2.0	2.0

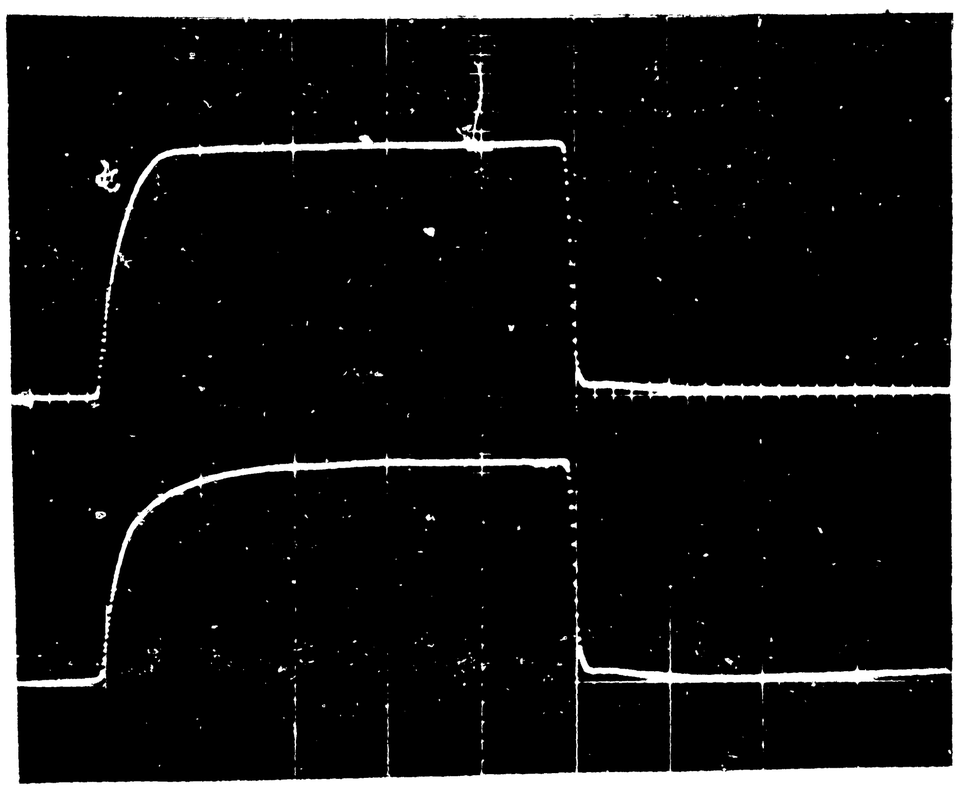
Type DL No. $254D_3$ Temp. +125°C Vcc +4.0 N = 3

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	502.	499.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.82	2.0	2.62	2.78
T_r	58.	54.	66.	49.
T_f	12.8	13.	13.	12.
T_d		2.0	2.0	2.0
T_s		4.0	1.0	1.6
T_{pd}		1.5	2.5	2.0

GENERAL MICRO-ELECTRONICS

Type DL No. 254D$_3$ Temp. +25°C Vcc 4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	505.	500.	497.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.84	1.58	2.26	2.68
T_r	51.	33.	84.	56.
T_f	13.	13.	13.	13.
T_d		0.	1.0	1.6
T_s		4.2	2.0	1.0
T_{pd}		2.0	2.0	2.5



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type DL No. 254D3 Temp. -40°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	509.	502.	497.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.92	1.37	2.12	2.82
T_r	60.	31.	86.	69.
T_f	12.	14.	12.	12.
T_d		1.0	1.0	2.0
T_s		4.0	3.5	1.0
T_{pd}		2.5	1.5	3.0

Type DL No. 254D3 Temp. -55°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	511.	503.	497.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.86	1.26	2 0	2.82
T_r	62.	29.	86.	74.
T_f	12.	12.	11.	12.
T_d		1.0	1.0	2.0
T_s		5.0	3.0	1.0
T_{pd}		2.5	1.9	3.5

GENERAL MICRO-ELECTRONICS

Type DL No. $254D_3$ Temp. +85°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	506.	503.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.80	1.87	1.32	1.72
T_r	55.	40.	62.	56.
T_f	13.	13.	12.5	13.
T_d		1.0	2.0	2.0
T_s		4.0	2.7	1.6
T_{pd}		2.0	2.0	2.3

Type DL No. $254D_3$ Temp. +125°C Vcc +4.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 3.0	Vcc 4.0	Vcc 5.0
Pulse Width	500.	504.	501.	500.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	2.78	2.02	2.50	2.70
T_r	57.	47.	71.	56.
T_f	13.	14.	14.	14.
T_d		2.0	2.0	2.0
T_s		3.0	2.0	2.0
T_{pd}		2.3	2.7	3.0

EVALUATION

The General Microelectronics CML Gate is a five-input OR/NOR Gate. The gate requires 3 power supplies for an input and output based on zero volts d-c. For this condition the supplies are: V9 - 2.0, V1, 13, 14 =-2.5, and V2 = +1.0. The circuit is packaged in a 14 lead flat-pack or a 10 pin TO-5 can.

Typical curves were plotted on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

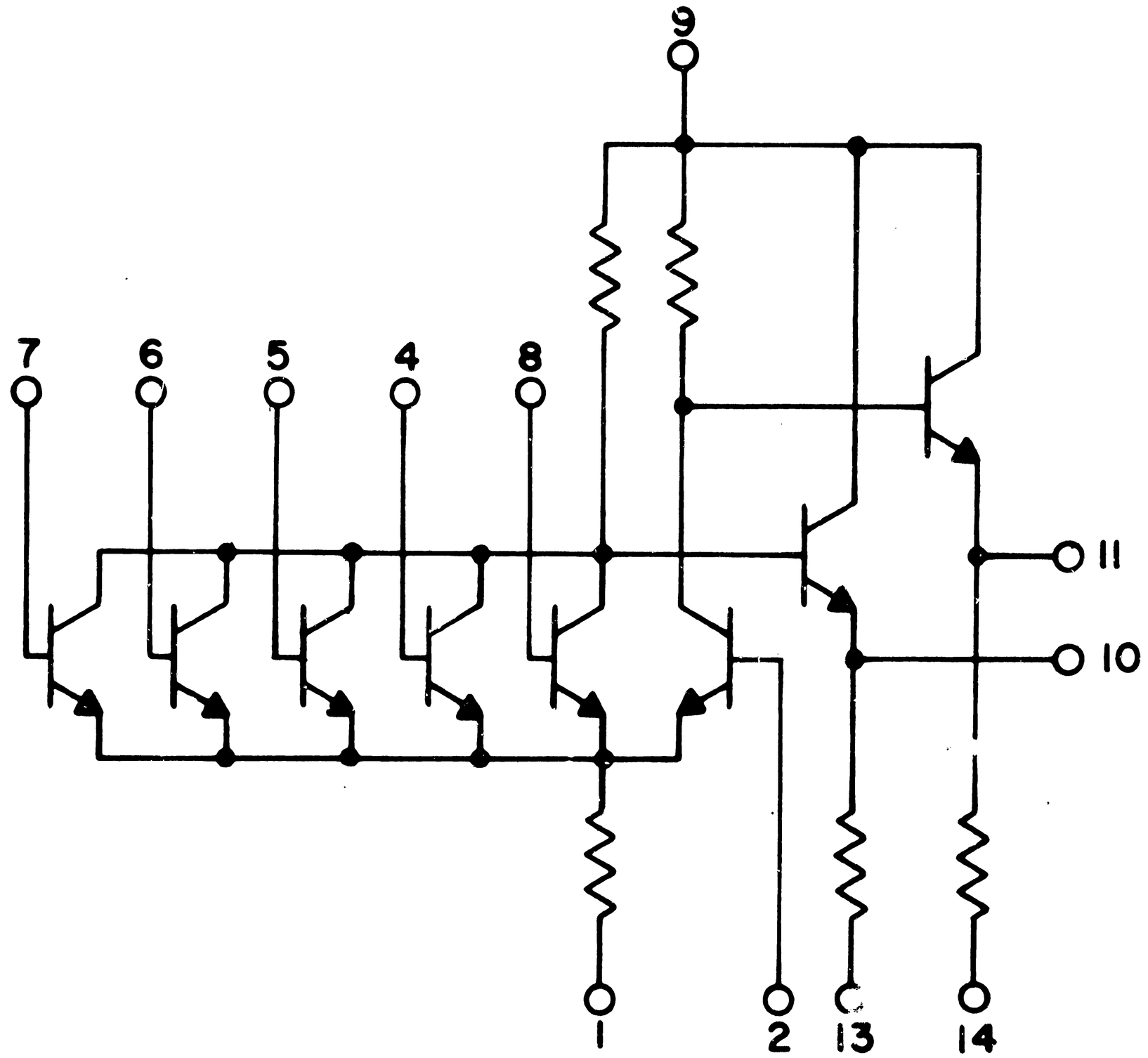
1. The testing circuit block diagram is shown preceeding the dynamic data.

2. The input pulse was set to have a repetition rate of 1 MC and a pulse width of 500 ns. The temperature was regulated at +25°C with a load of 1 on the test circuit.

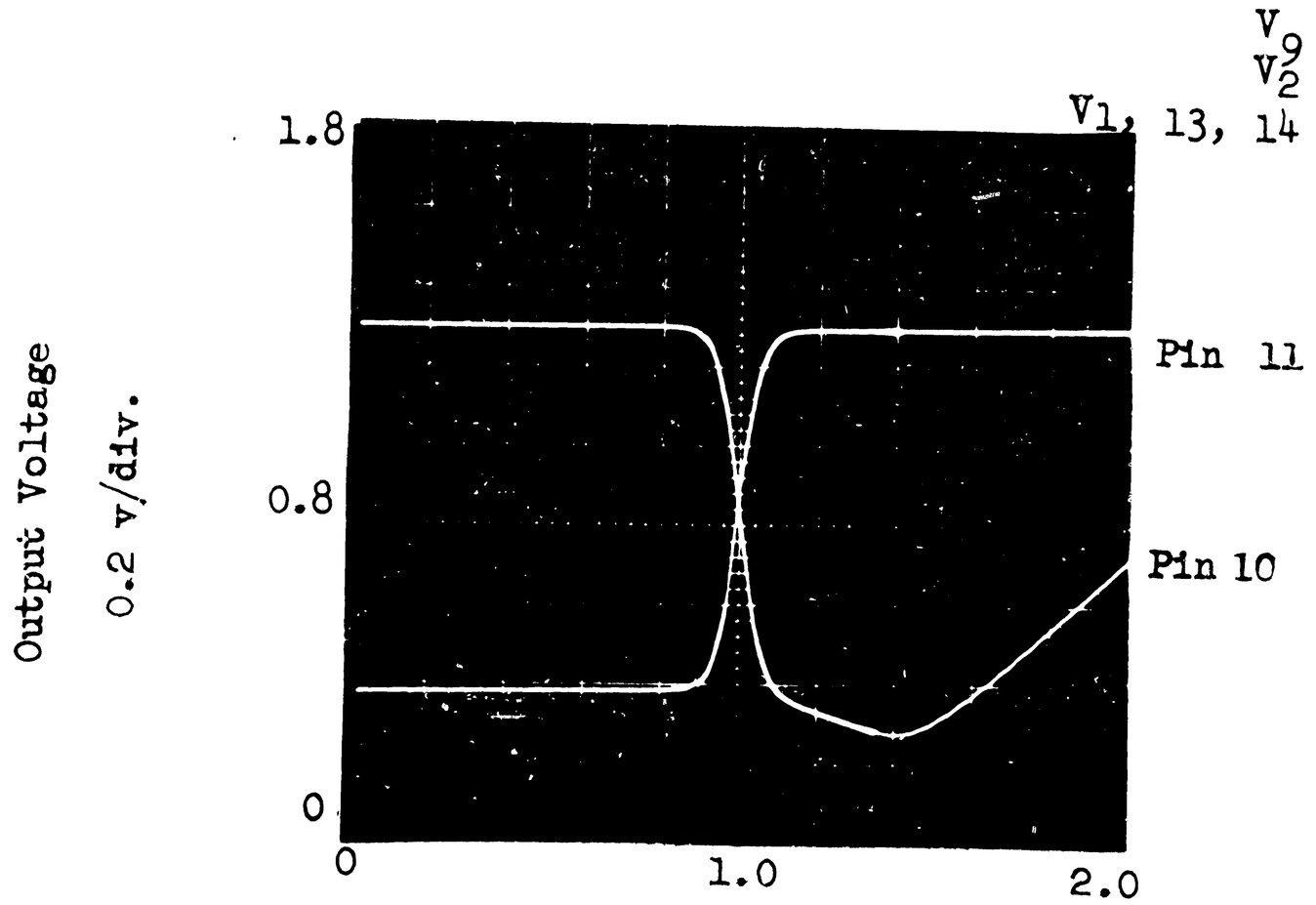
3. The supplies were set at V9 = +2.0, V1, 13, 14 = -2.5, and V2 = +1.0.

4. The above procedure was repeated for temperatures of -55°C, -40°C, +25PC, +85°C, and +125°C.

5. The above procedure was repeated for a load of 3.



543G5 5 - INPUT CML GATE ELEMENT



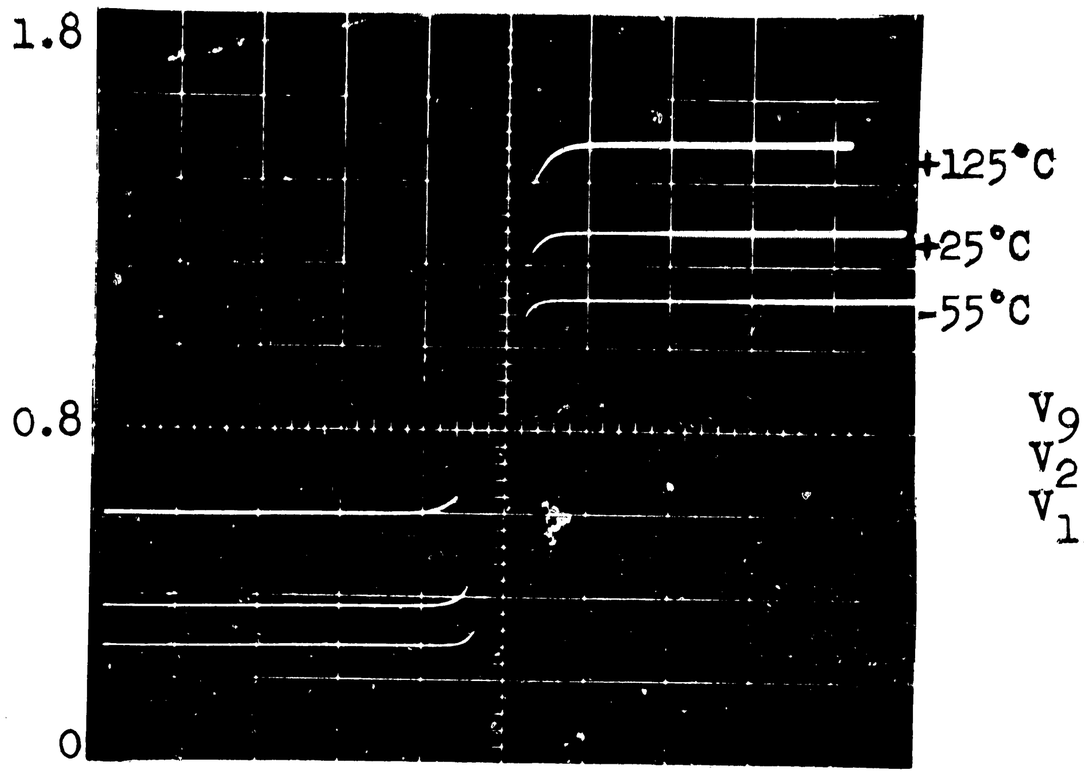
Input voltage on pin 4

INPUT OUTPUT CHARACTERISTICS

CML - 543G5

Output voltage on pin 11

0.2 v/div.

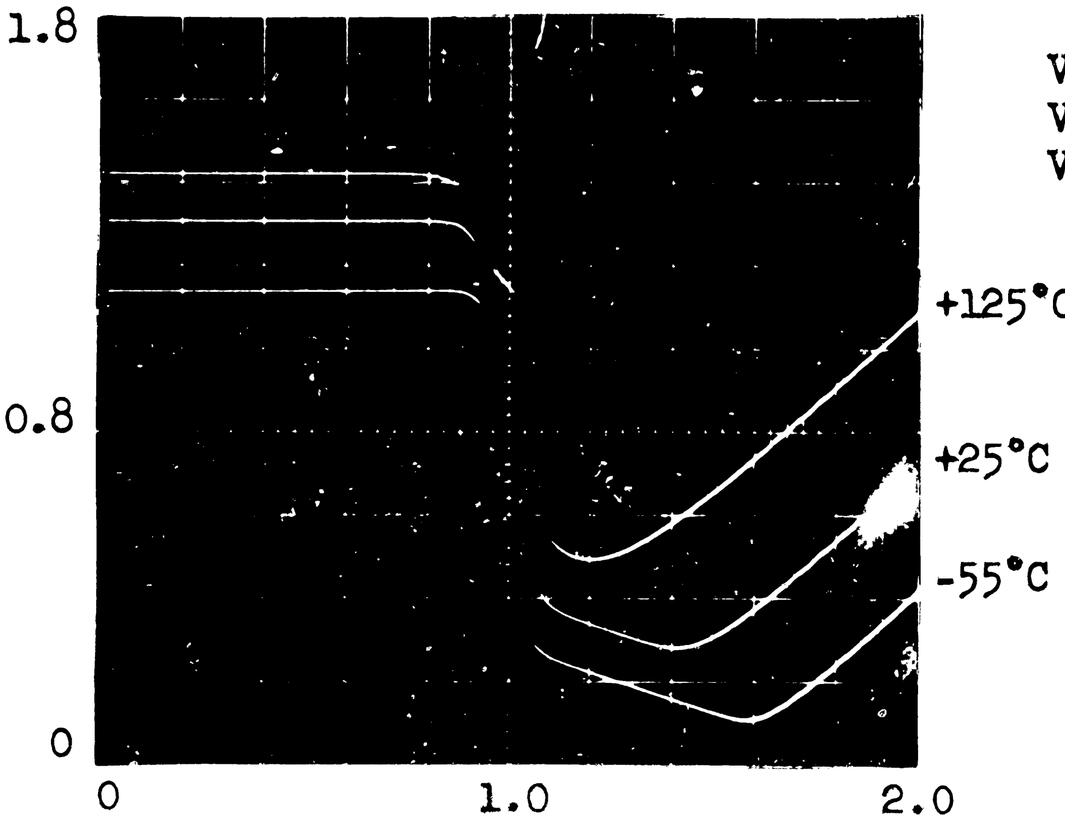


0.2 v/div.

Input voltage on pin 4

Output voltage on pin 10

0.2 v/div.



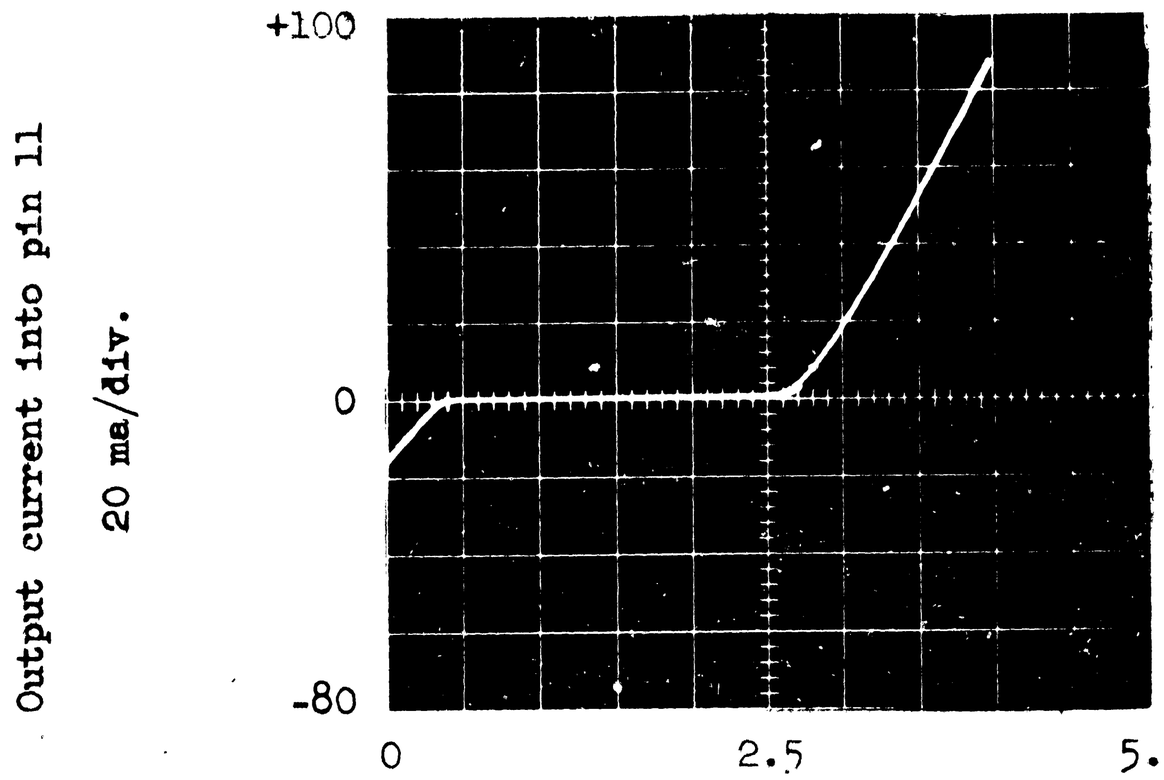
0.2 v/div.

Input voltage on pin 4

INPUT OUTPUT CHARACTERISTICS

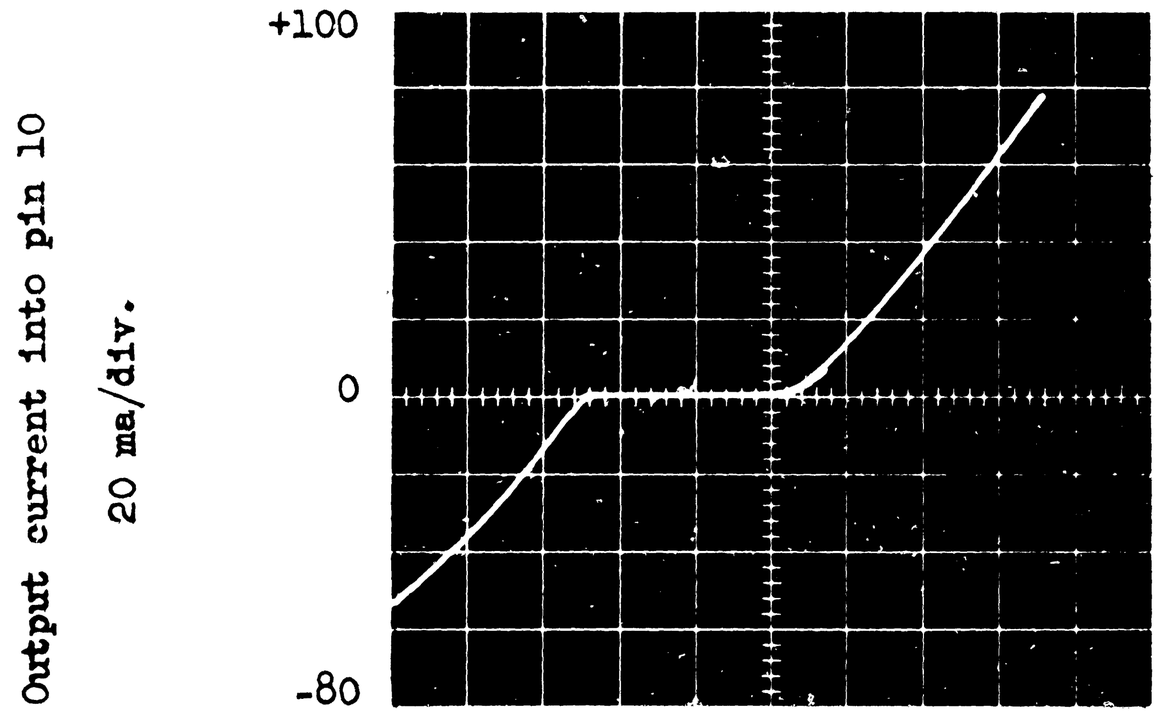
CML 543G5

3.2.144



$V_9 = 2.0$
$V_2 = 1.0$
$V_{1, 13, 14} = -2.5$

"0" on Inputs



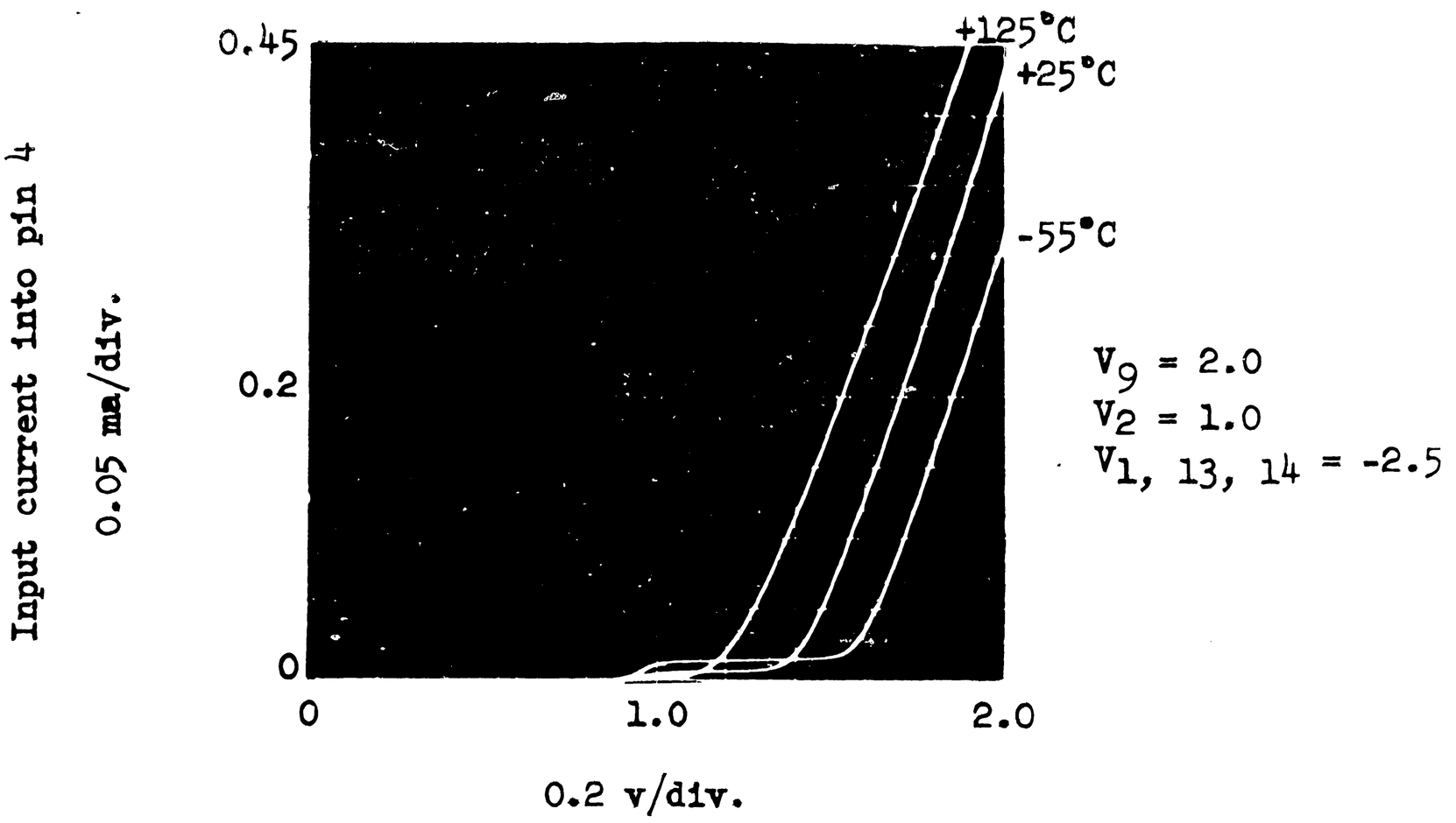
$V_9 = 2.0$
$V_2 = 1.0$
$V_{1, 13, 14} = -2.5$

"0" on Inputs

OUTPUT CHARACTERISTICS

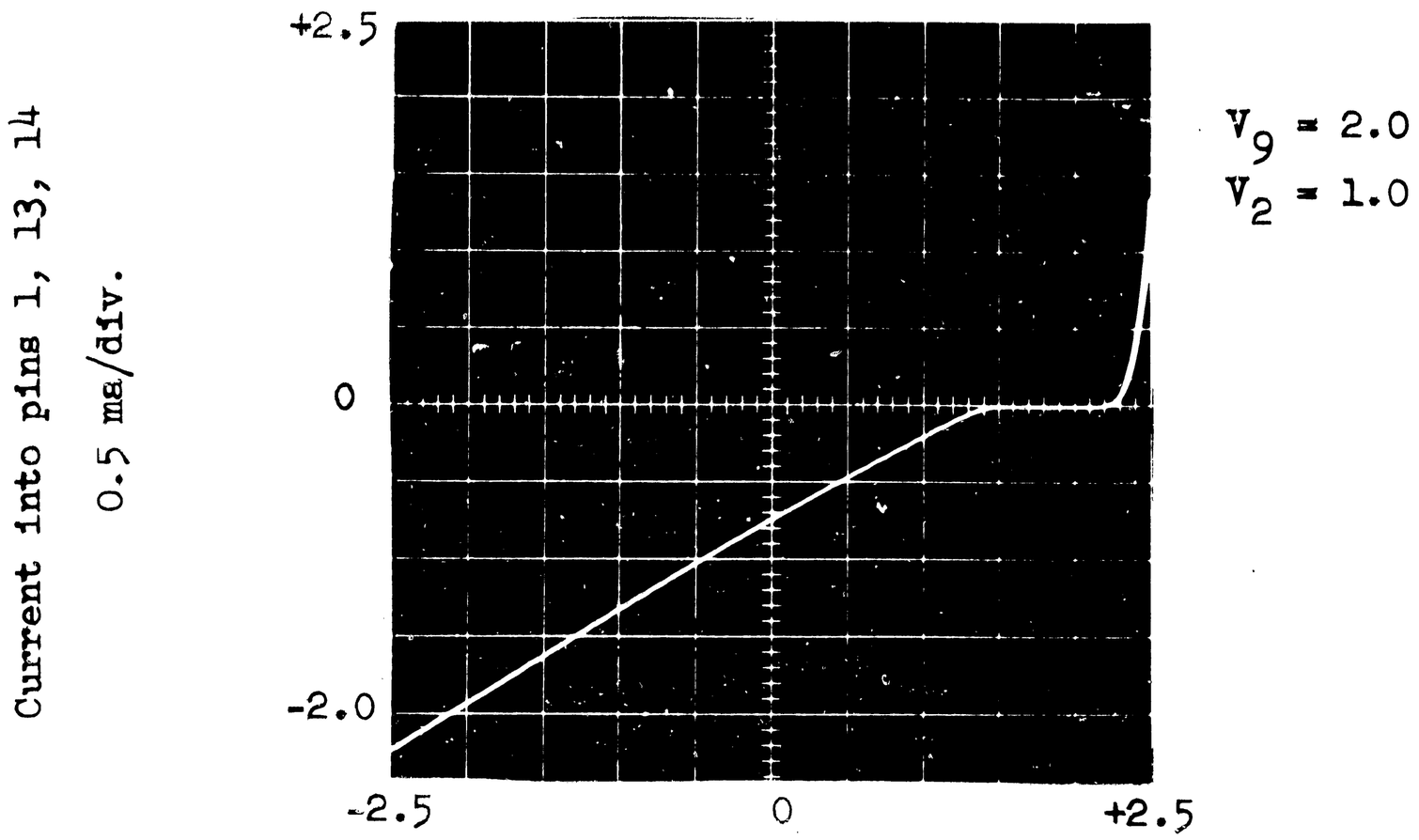
CML 543G5

3.2.145



INPUT CHARACTERISTICS

CML 543G5

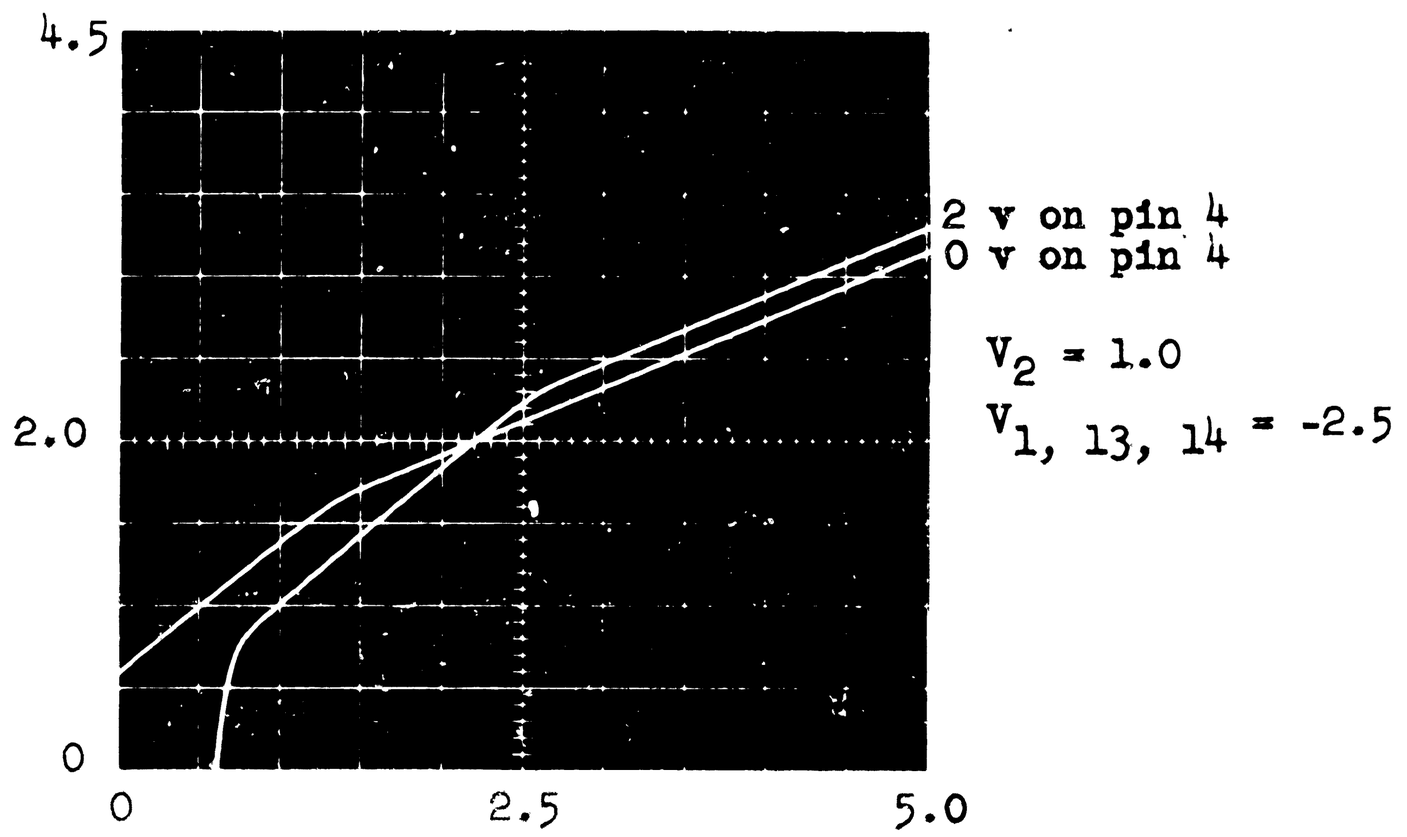


Current into pins 1, 13, 14

0.5 ma/div.

0.5 v/div.

Supply voltage on pins 1, 13, 14



Current into pin 9

0.5 ma/div.

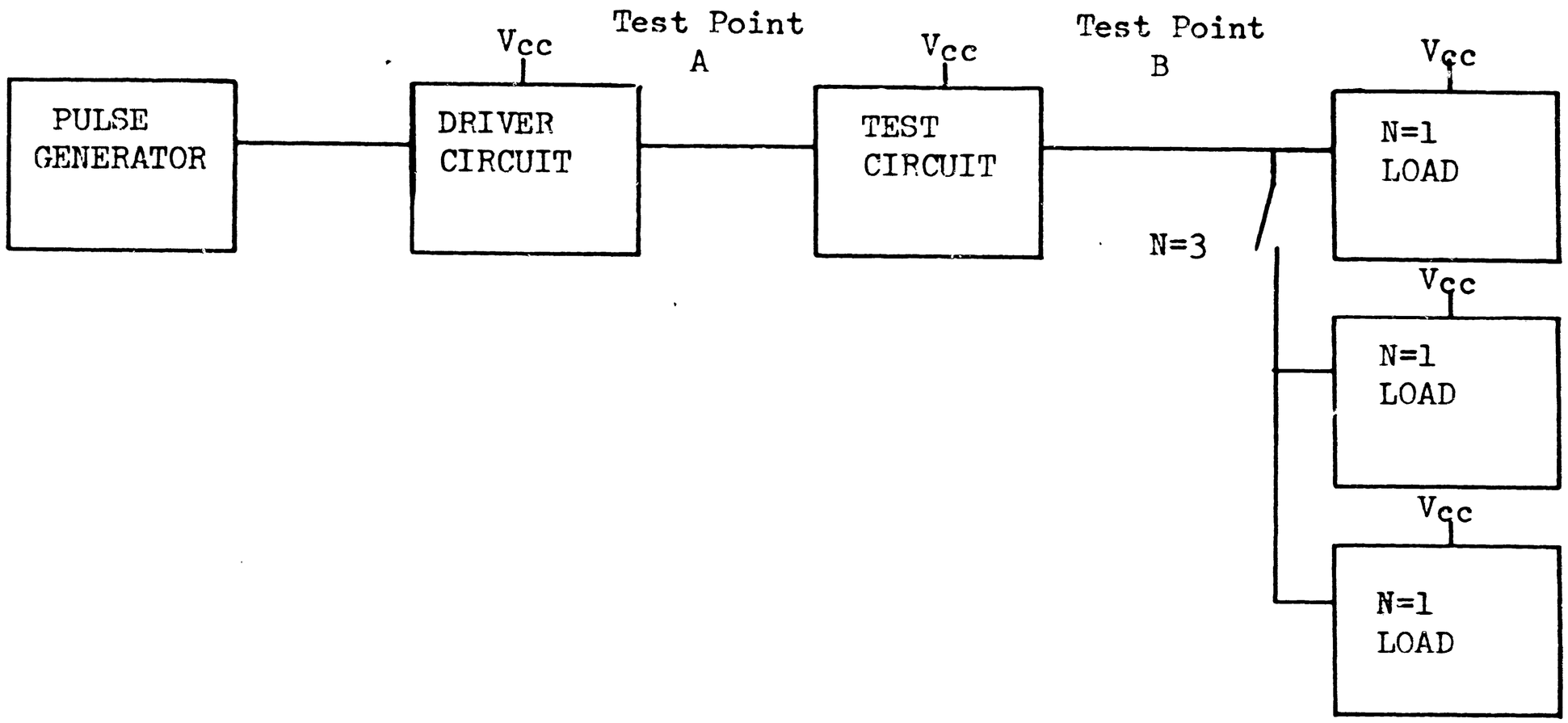
0.5 v/div.

Supply voltage on pin 9

POWER DISSIPATION CURVES

CML 543G5

3.2.147

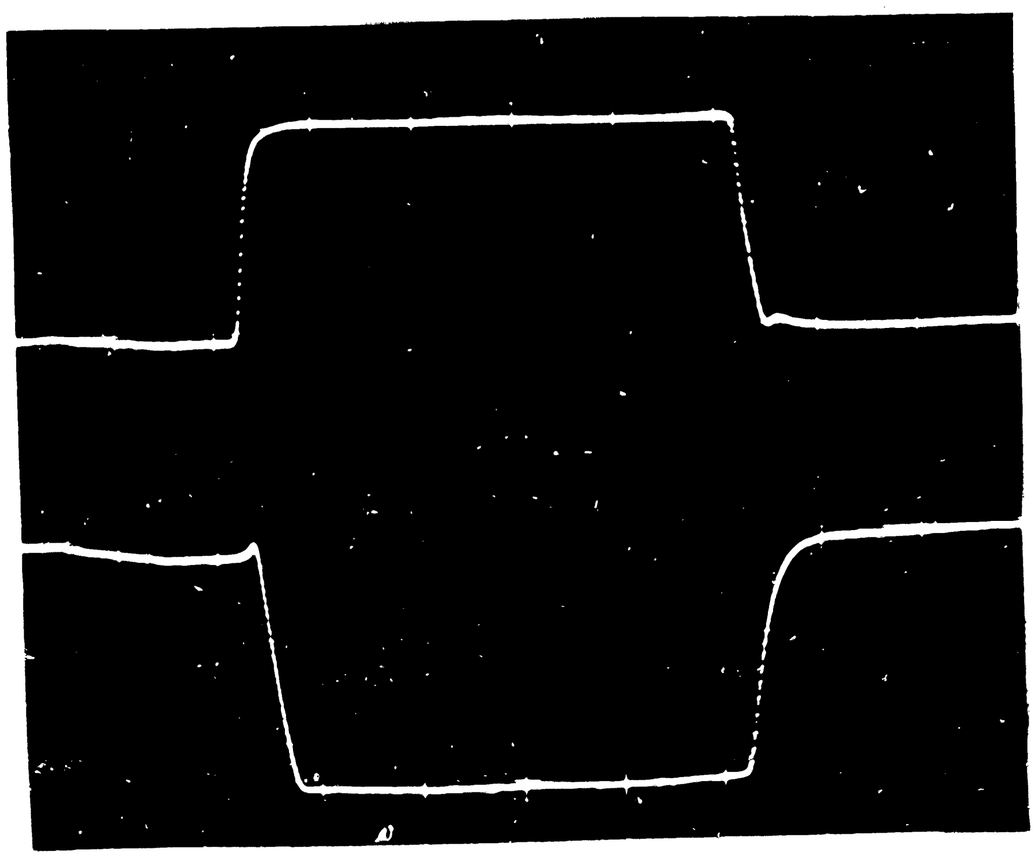


TEST CIRCUIT FOR CML 5436

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp. +25°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT. INPUT	TEST CKT. OUTPUT V_9 +2.0 V_2 -2.5 V_1 +1.0
Pulse Width	500.	487.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.83	1.06
T_r	16.6	55.
T_f	21.3	29.4
T_d		14.3
T_s		5.7
T_{pd}		15.



Test Circuit Input

Test Circuit Output

NOTE: Pins 1, 13 and 14 are tied common and referred to as Pin 1

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp [illegible] V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT V_9 +2.0 V_2 -2.5 V_1 +1.0
Pulse Width	500.	478.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.796	0.918
T_r	15.7	47.5
T_f	21.2	27.2
T_d		18.4
T_s		3.2
T_{pd}		15.5

Type CML No. 543G5 Temp [illegible] V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT V_1 +2.0 V_4 -2.5 V_5 +1.0
Pulse Width	1500.	474.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.76	0.86
T_r	15.5	50.
T_f	22.	46.
T_d	—	19.
T_s		3.0
T_{pd}		17.

Type CML No. 543G5 Temp +85°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT V_9 +2.0, V_2 -2.5, V_1 +1 0
Pulse Width	500.	497.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.872	1.08
T_r	19.	74.
T_f	24.	31.
T_d		14.
T_s		15.
T_{pd}		21.

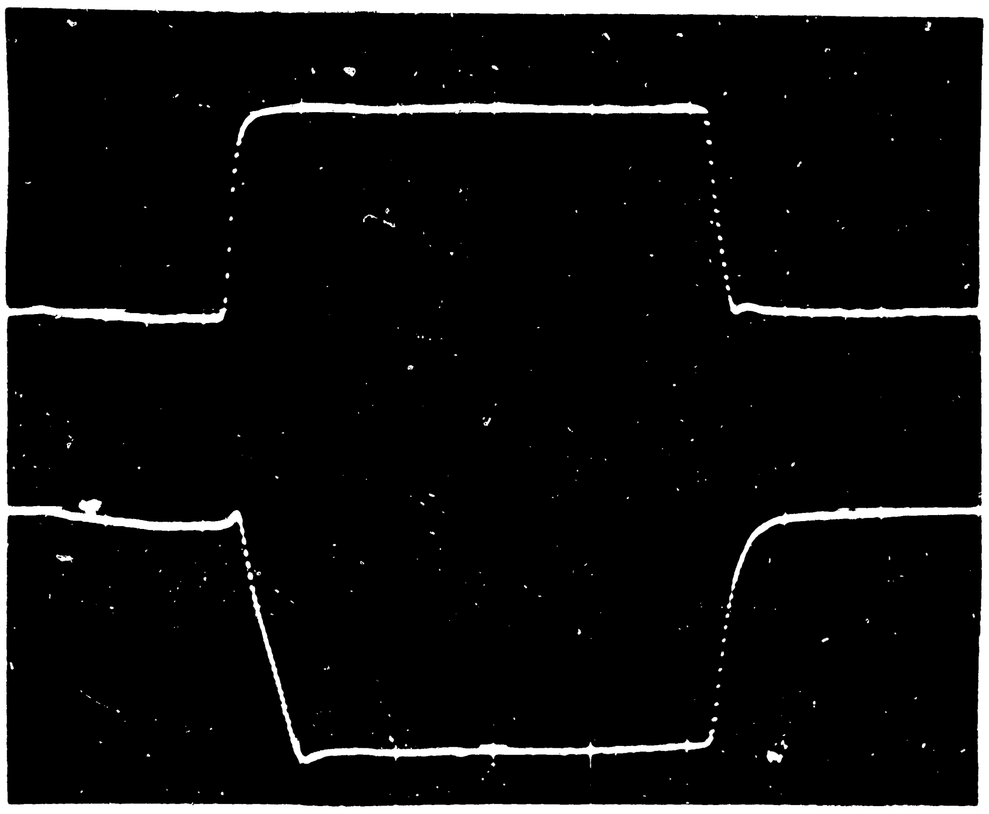
Type CML No. 543G5 Temp +125°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 1

	TEST CKT INPUT	TEST CKT OUTPUT V_1 +2.0, V_4 -2.5, V_5 +1.0
Pulse Width	500.	507.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.75	0.76
T_r	21.	72.
T_f	22.	25.
T_d		11.
T_s		24.
T_{pd}		21.

GENERAL MICRO-ELECTRONICS

Type CML No. 5436S Temp. +25°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT. INPUT	TEST CKT. OUTPUT V_9 +2.0 V_2 -2.5 V_1 +1.0
Pulse Width	500.	479.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.84	1.02
T_r	17.1	58.
T_f	21.7	47.8
T_d		15.
T_s		6.0
T_{pd}		21.



Test Circuit Input

Test Circuit Output

Type CML No. 543G5 Temp -40°C V_0 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT V_0 +2.0 V_2 -2.5 V_1 +1.0
Pulse Width	500.	470.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.792	0.912
T_r	15.7	50.
T_f	21.1	43.
T_d		19.7
T_s		3.5
T_{pd}		20.

Type CML No. 543G5 Temp -55°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT V_1 +2.0 V_4 -2.5 V_5 +1.0
Pulse Width	500.	468.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.774	0.872
T_r	16.	50.
T_f	21.5	41.
T_d		21.
T_s		3.0
T_{pd}		20.

GENERAL MICRO-ELECTRONICS

Type CML No. 543G5 Temp +85°C V_9 +2.0 V_2 -2.5 V_1 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT V_9 +2.0 V_2 -2.5 V_1 +1.0
Pulse Width	500.	489.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.88	1.04
T_r	18.6	75.
T_f	24.	52.
T_d		16.
T_s		17.
T_{pd}		25.

Type CML No. 543G5 Temp +125°C V_1 +2.0 V_4 -2.5 V_5 +1.0 N= 3

	TEST CKT INPUT	TEST CKT OUTPUT V_1 +2.0 V_4 -2.5 V_5 +1.0
Pulse Width	500.	504.
Repetition Rate	1MC	1MC
Pulse Amplitude	0.75	0.74
T_r	21.	66.
T_f	22.	42.
T_d		11.3
T_s		25.
T_{pd}		25.

EVALUATION

The General Microelectronics line of Transistor Transistor Logic (TTL) consists of two NAND Gates; the 265G8 which is an eight input gate and the 265D4 which is a dual four input gate. The circuits are typical TTL NAND Gates with an additional output non-inverting power stage enabling them to drive high fan-outs with high capacitive loading. Both circuits were tested statically on a transistor curve tracer.

DYNAMIC TEST PROCEDURE

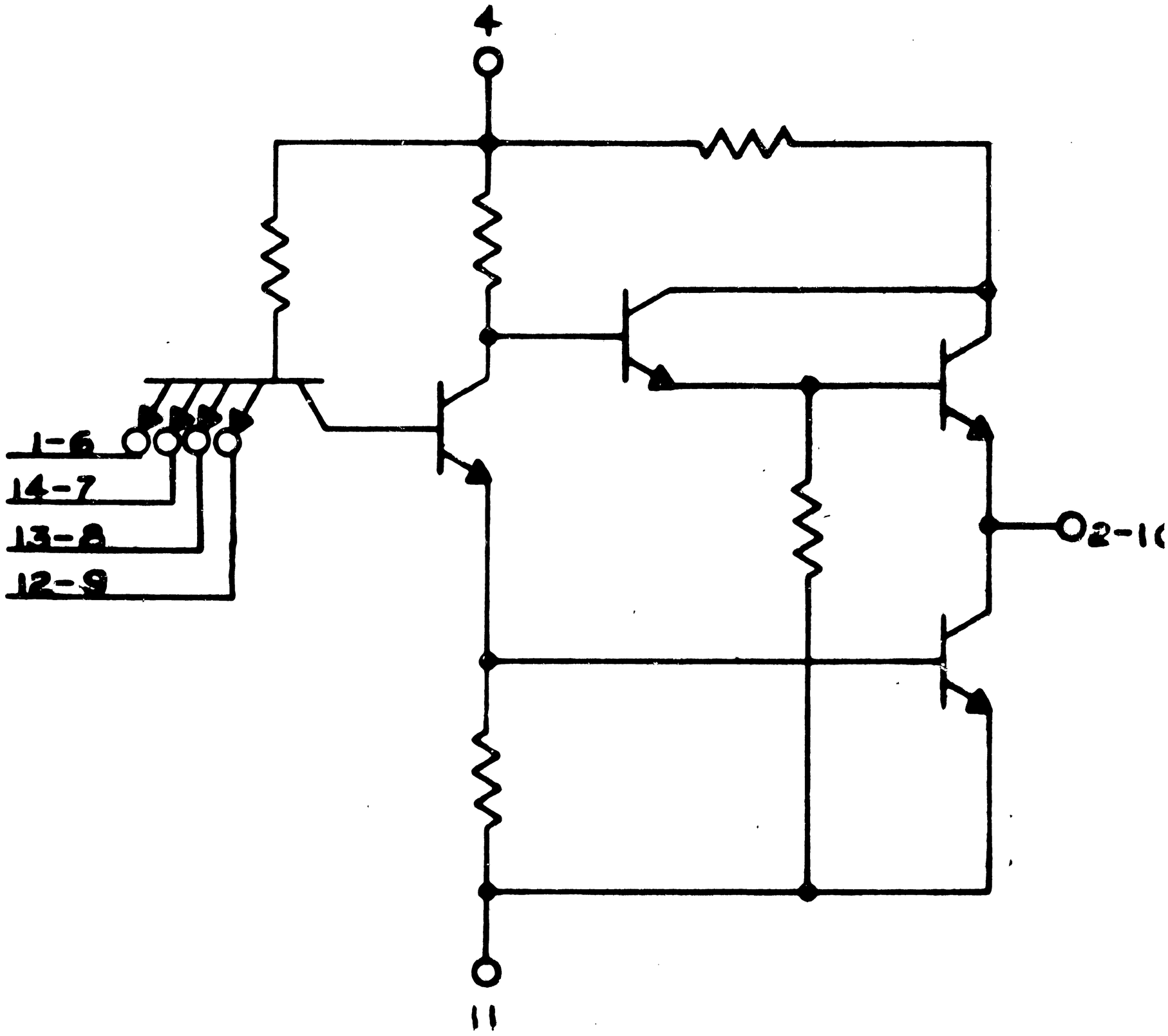
1. The testing circuit block diagram is shown preceding the dynamic data for the 365D4.

2. The input pulse was set to have a repetition rate of 1 MC and a pulse width of 500 ns. The temperature was regulated at +25°C with a load of 1 on the test circuit.

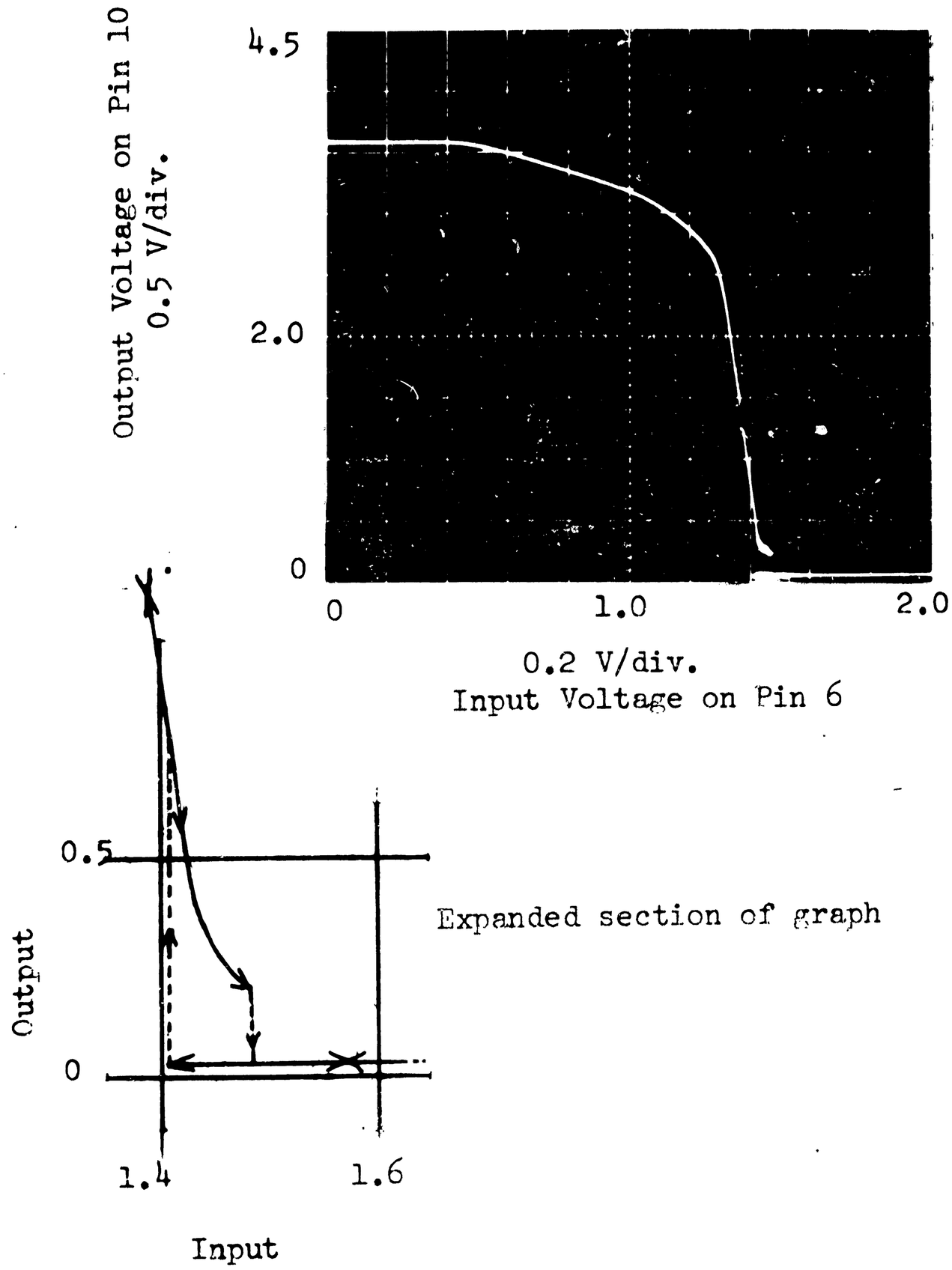
3. V_{cc} was set at +4.5 V and data taken. Data was also taken for V_{cc} of 5.0 V and 5.5 V.

4. The above procedure was repeated for temperatures of -40°C, -55°C, +85°C and +125°C.

5. The above procedure was repeated for test circuit loads of N = 5 and N = 10.



365D4 DUAL 4 - INPUT TTL GATE ELEMENT

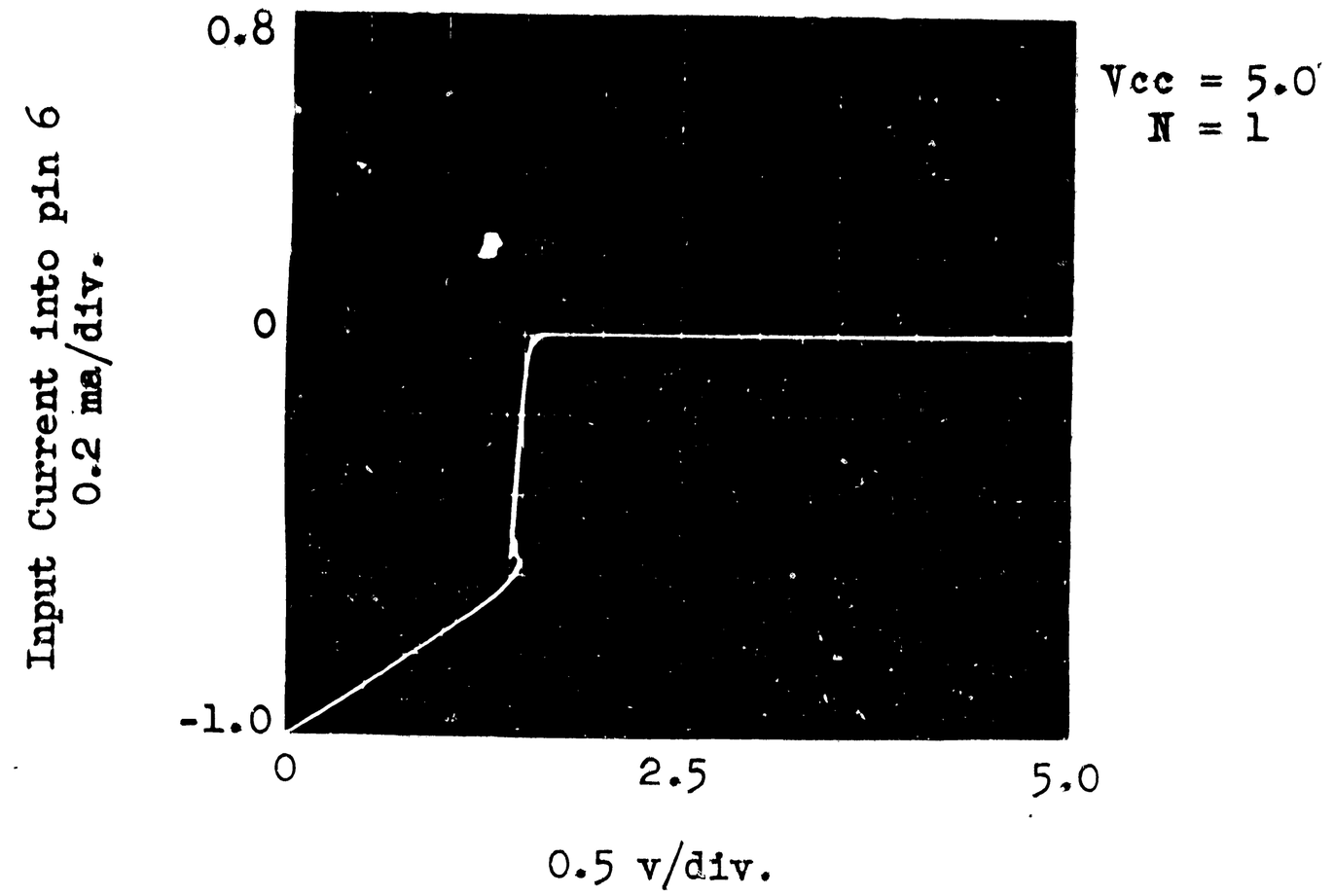


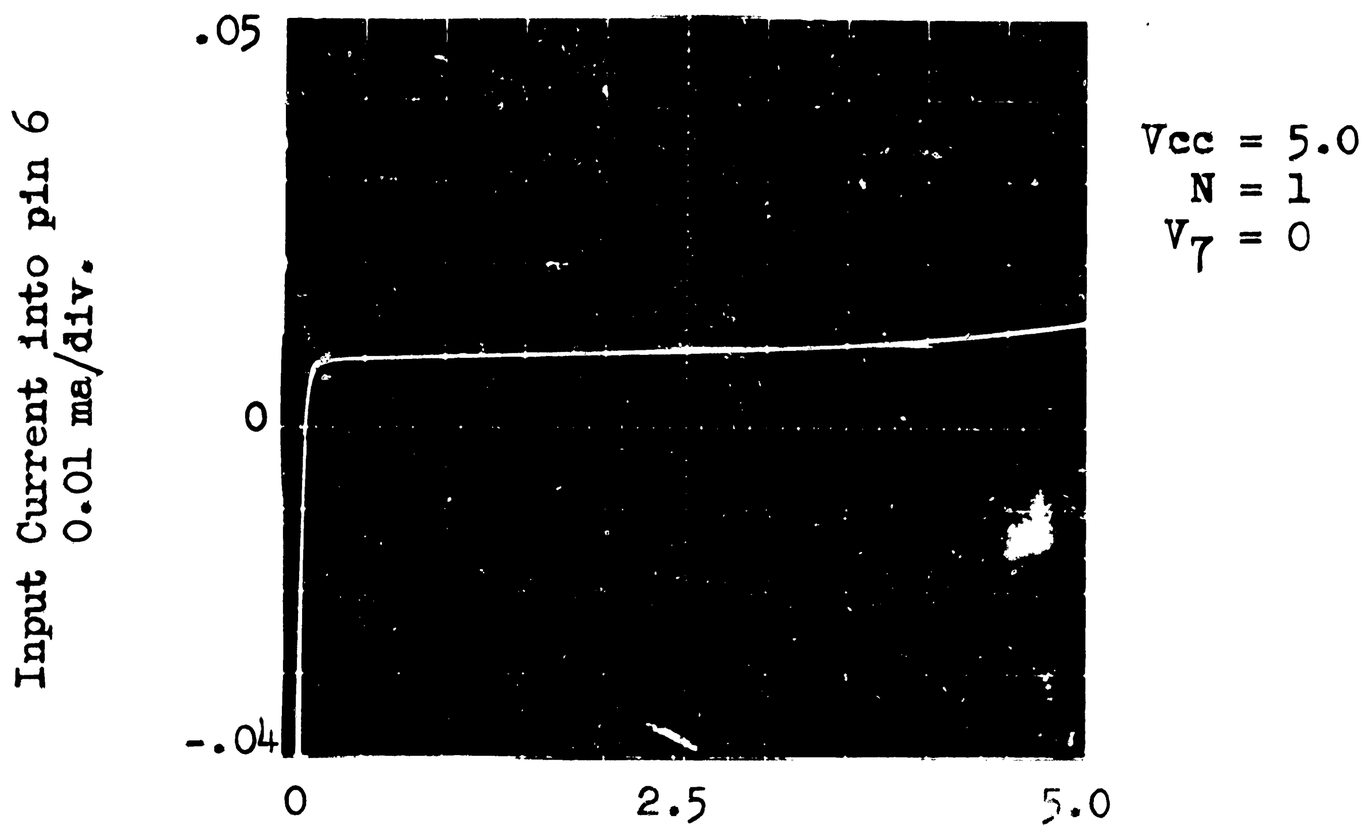
V_{cc} = +5.0
N = 1

Expanded section of graph

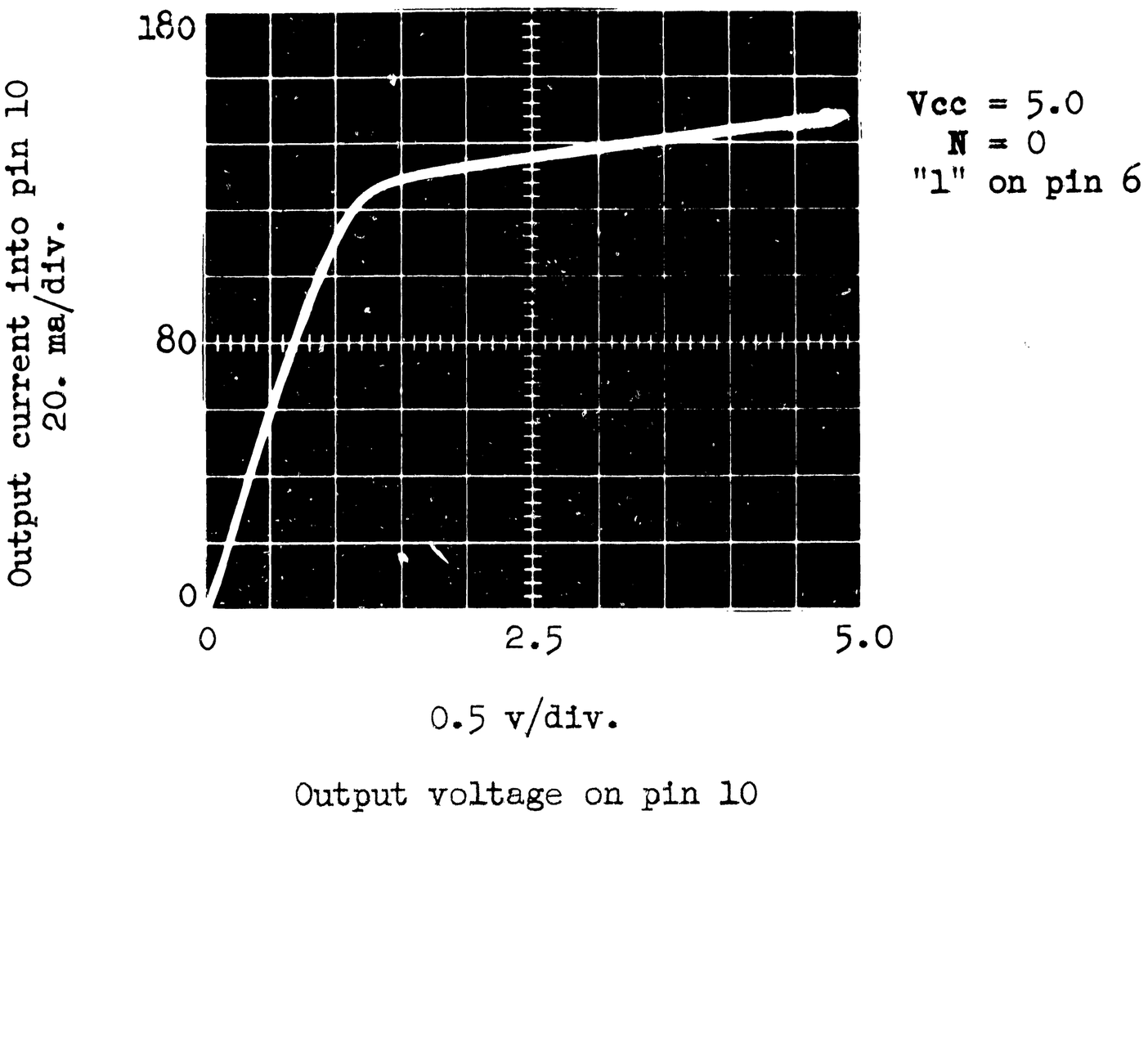
NOTE: In the above graph, the output voltage followed the curve down to the knee where the input was approximately 1.44V. The output then dropped to the lowest potential. On the retrace the output stayed low until the input was down to approximately 1.40V where it rose vertically to meet the trace going high.

INPUT - OUTPUT CHARACTERISTICS
TTL 365D4



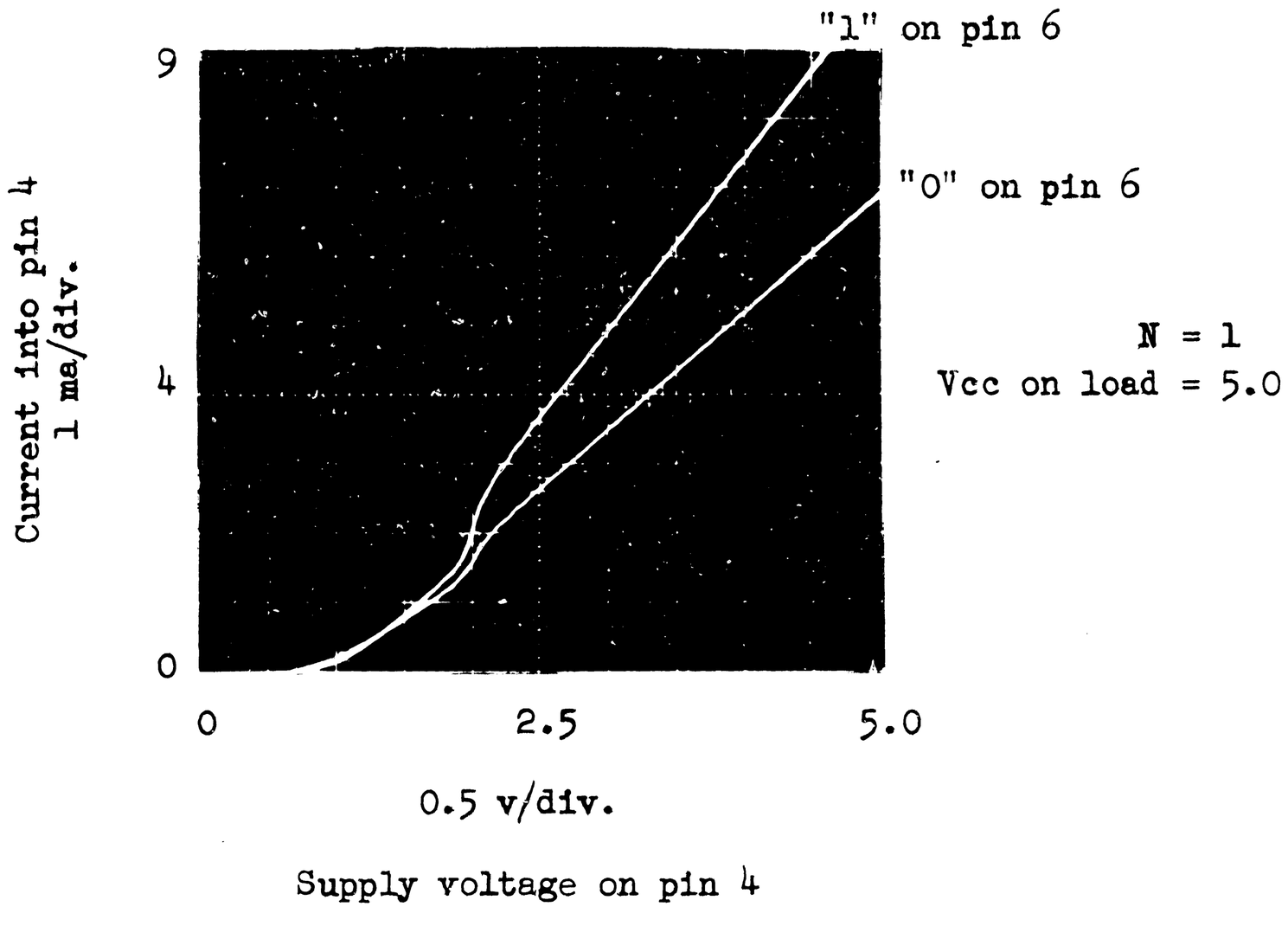


INPUT CHARACTERISTICS
TTL-365D4



OUTPUT CHARACTERISTICS
TTL 365D4

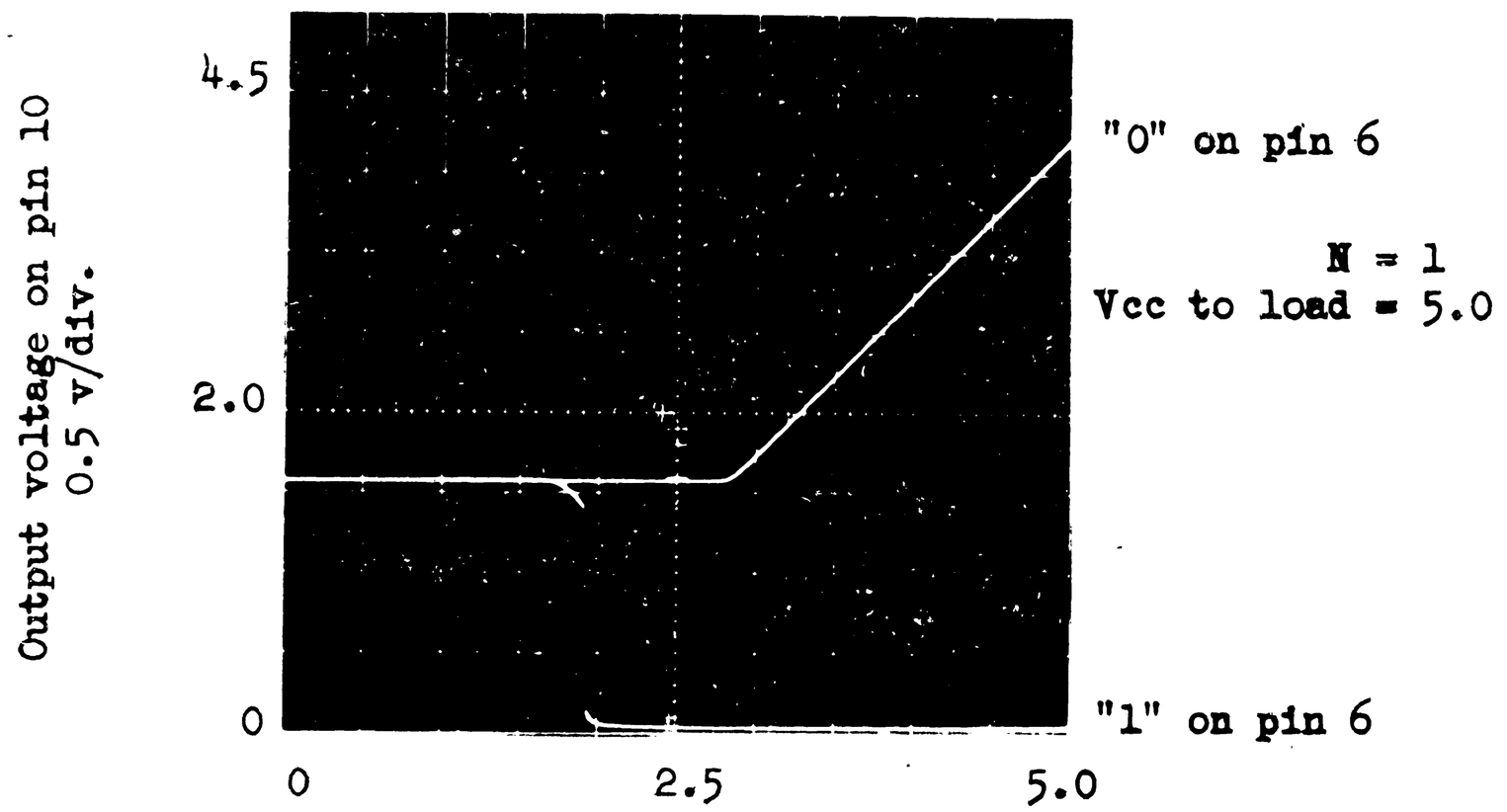
3.2.159



POWER DISSIPATION CURVES

TTL - 365D4

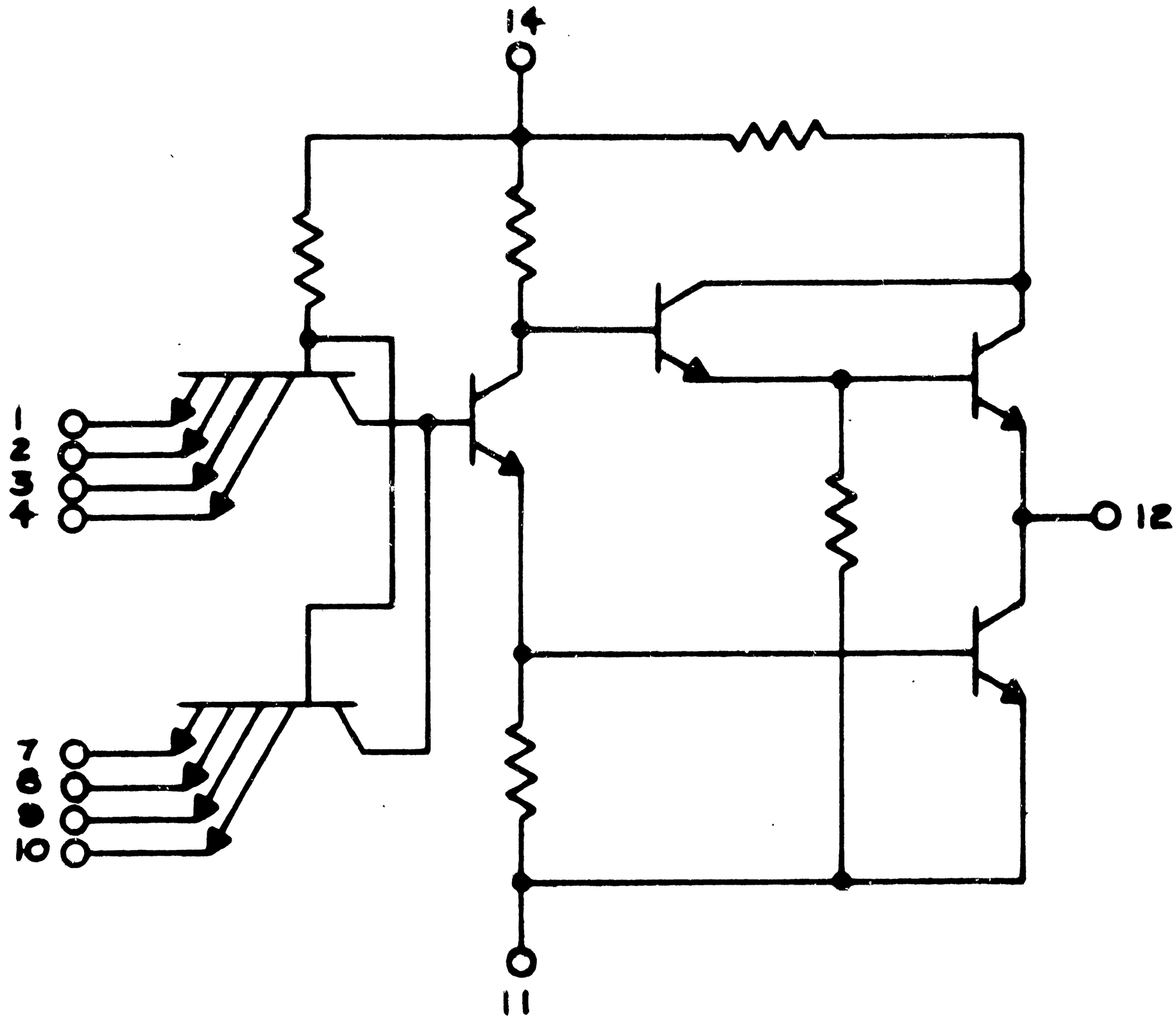
3.2.160



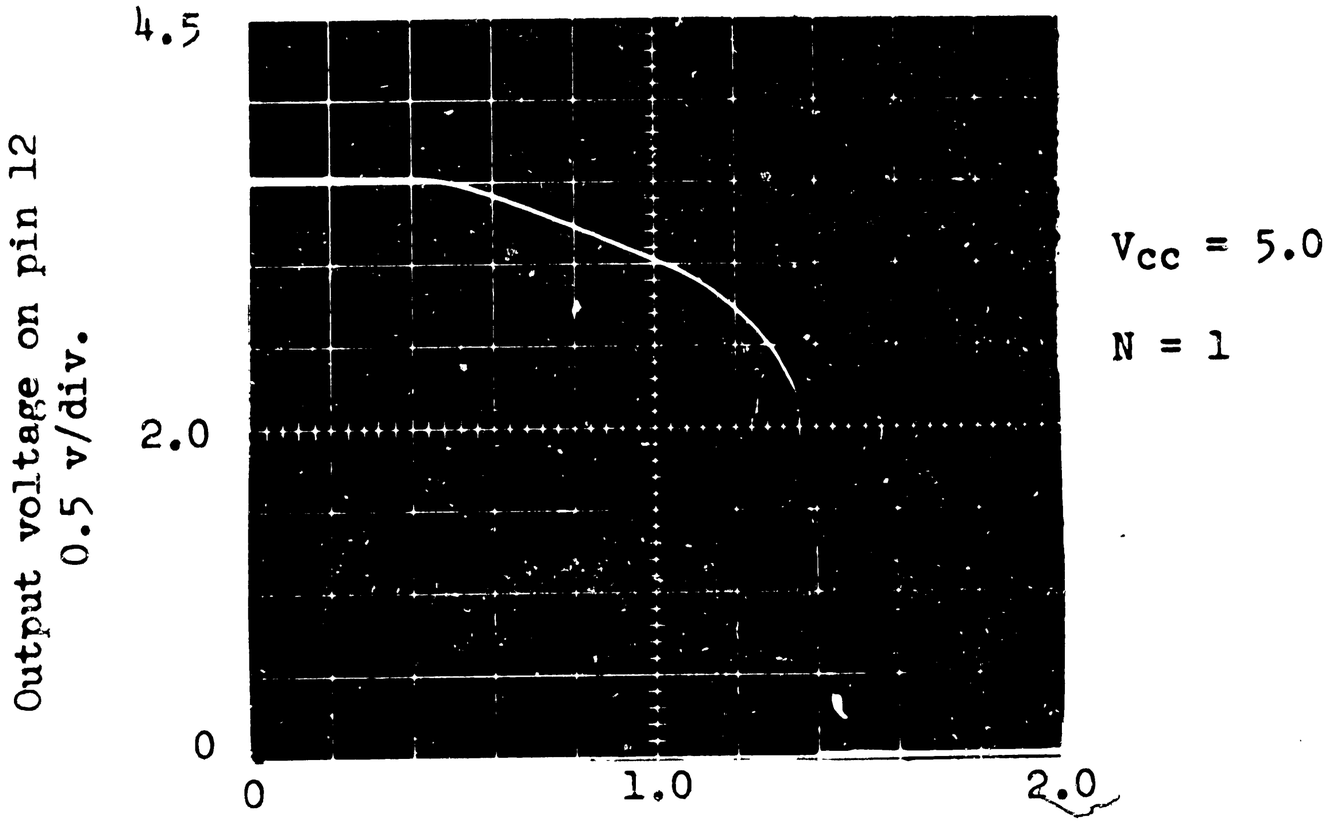
OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

TTL 365D4

3.2.161

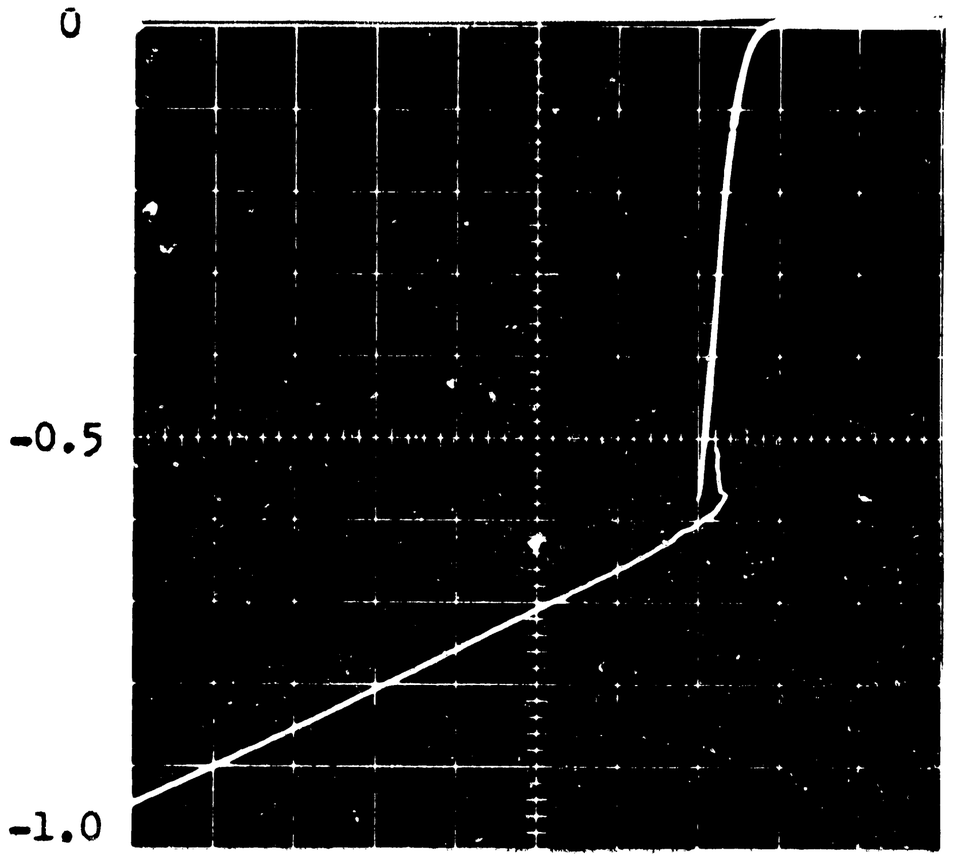


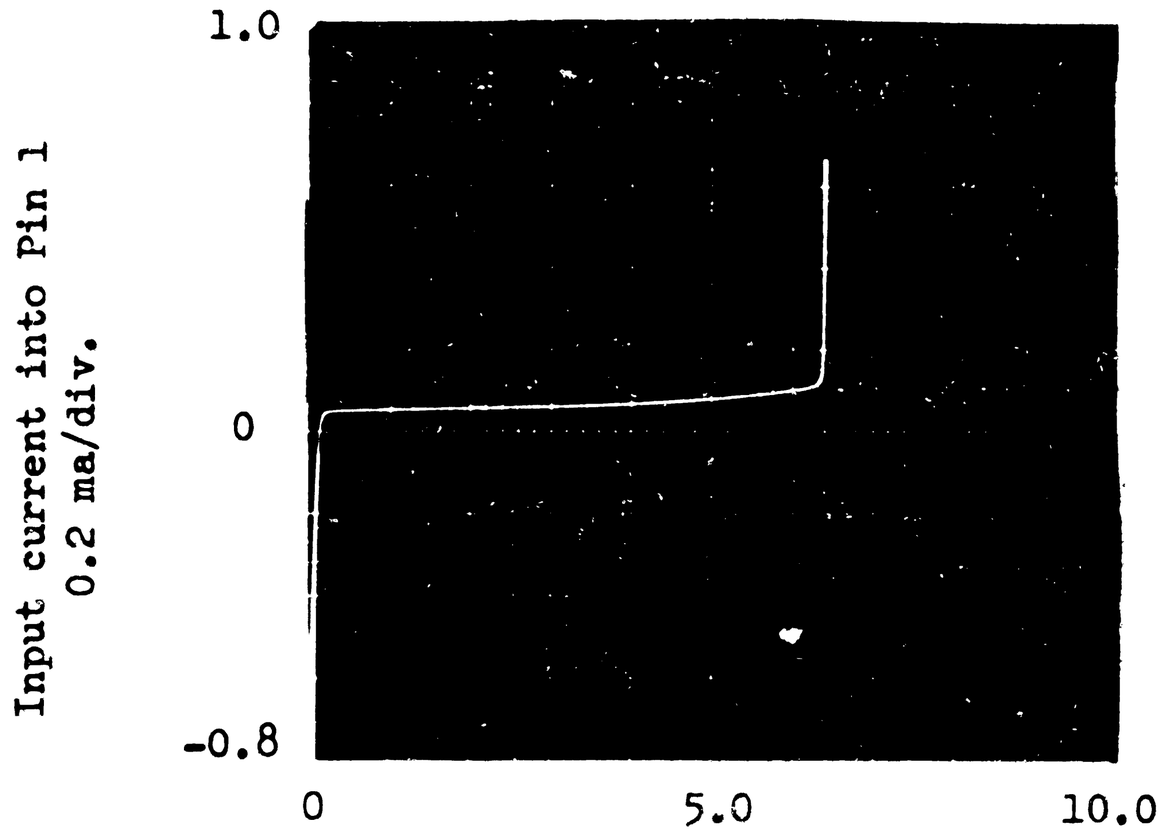
365G8 8 - INPUT TTL GATE ELEMENT



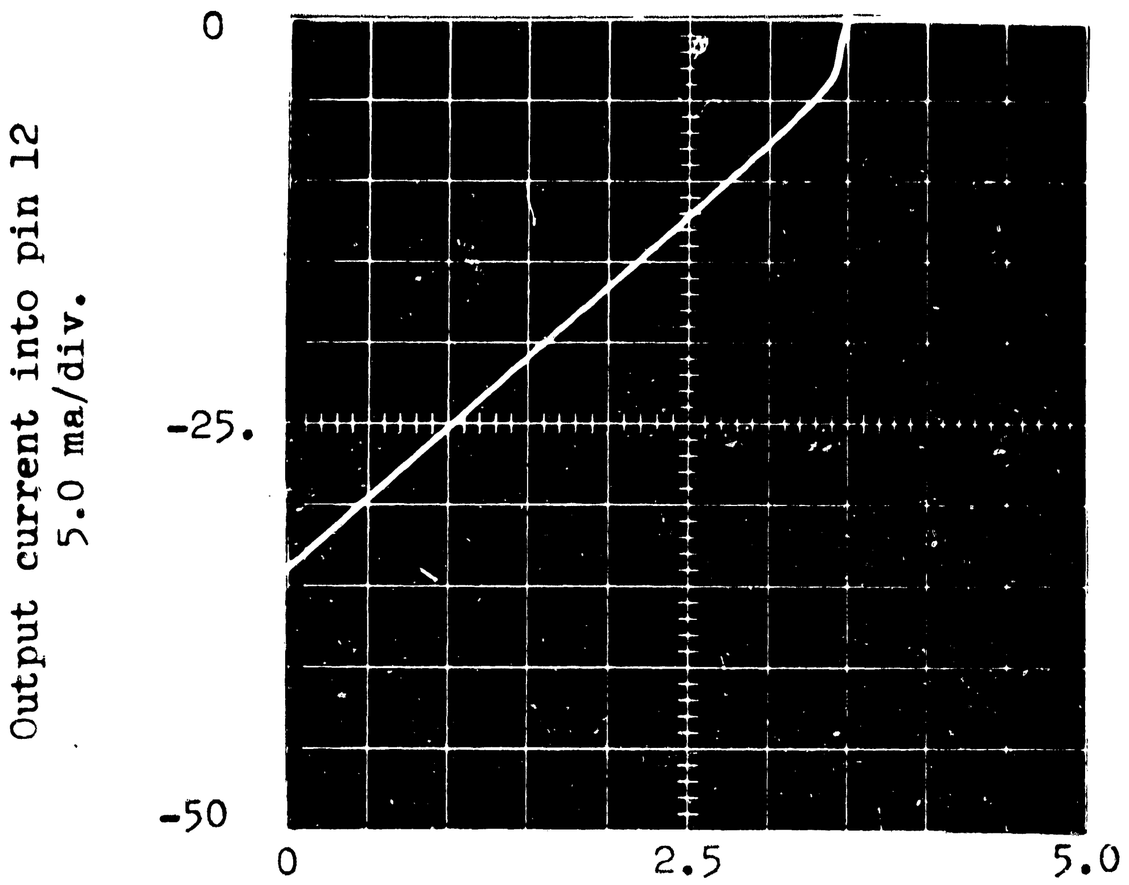
INPUT OUTPUT CHARACTERISTICS
TTL 365G8

3.2.163

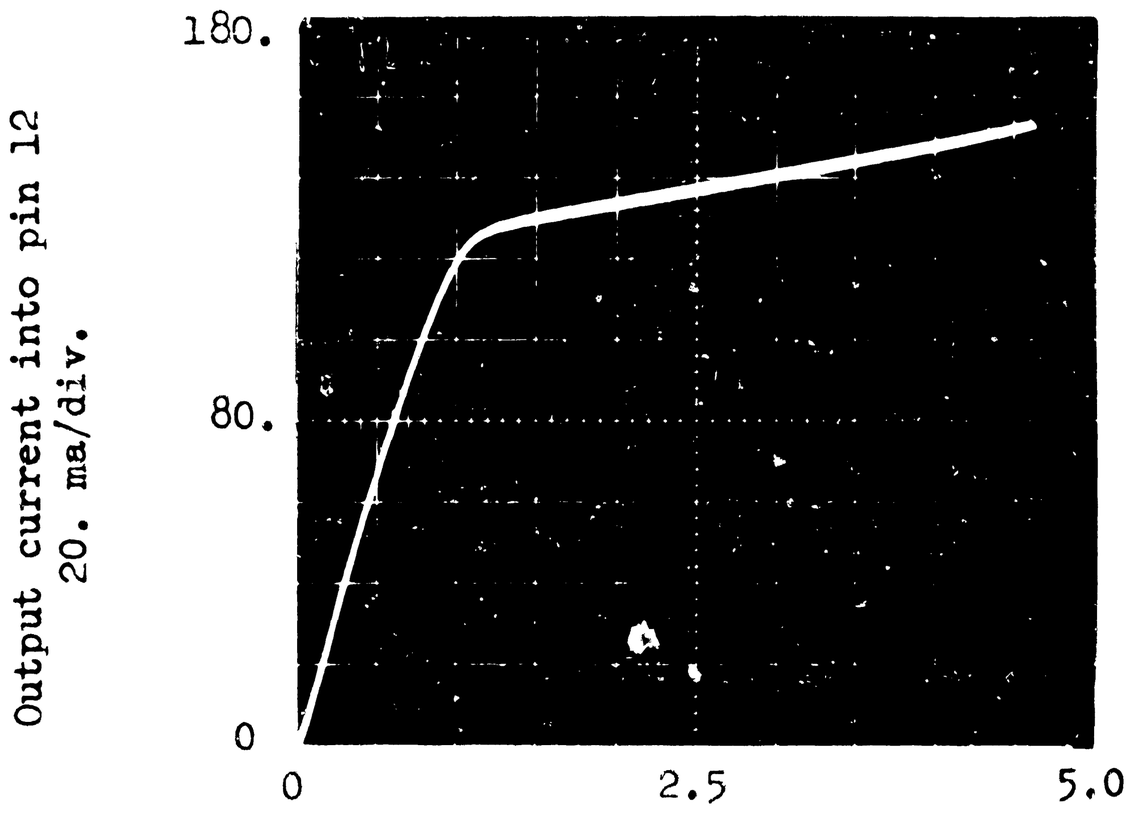




INPUT CHARACTERISTICS
TTL 365G8



0.5 v/div.
Output voltage on Pin 12

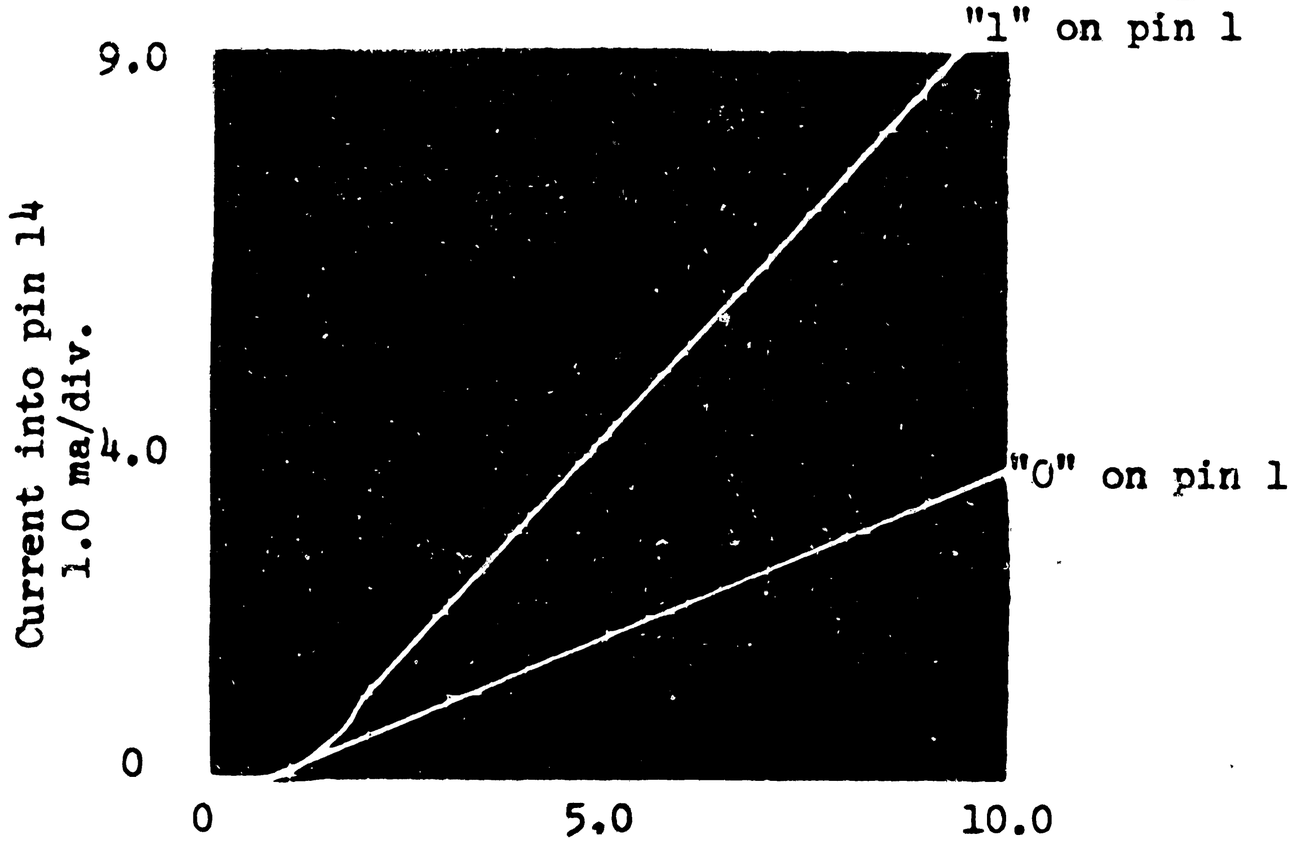


0.5 v/div.
Output voltage on Pin 12

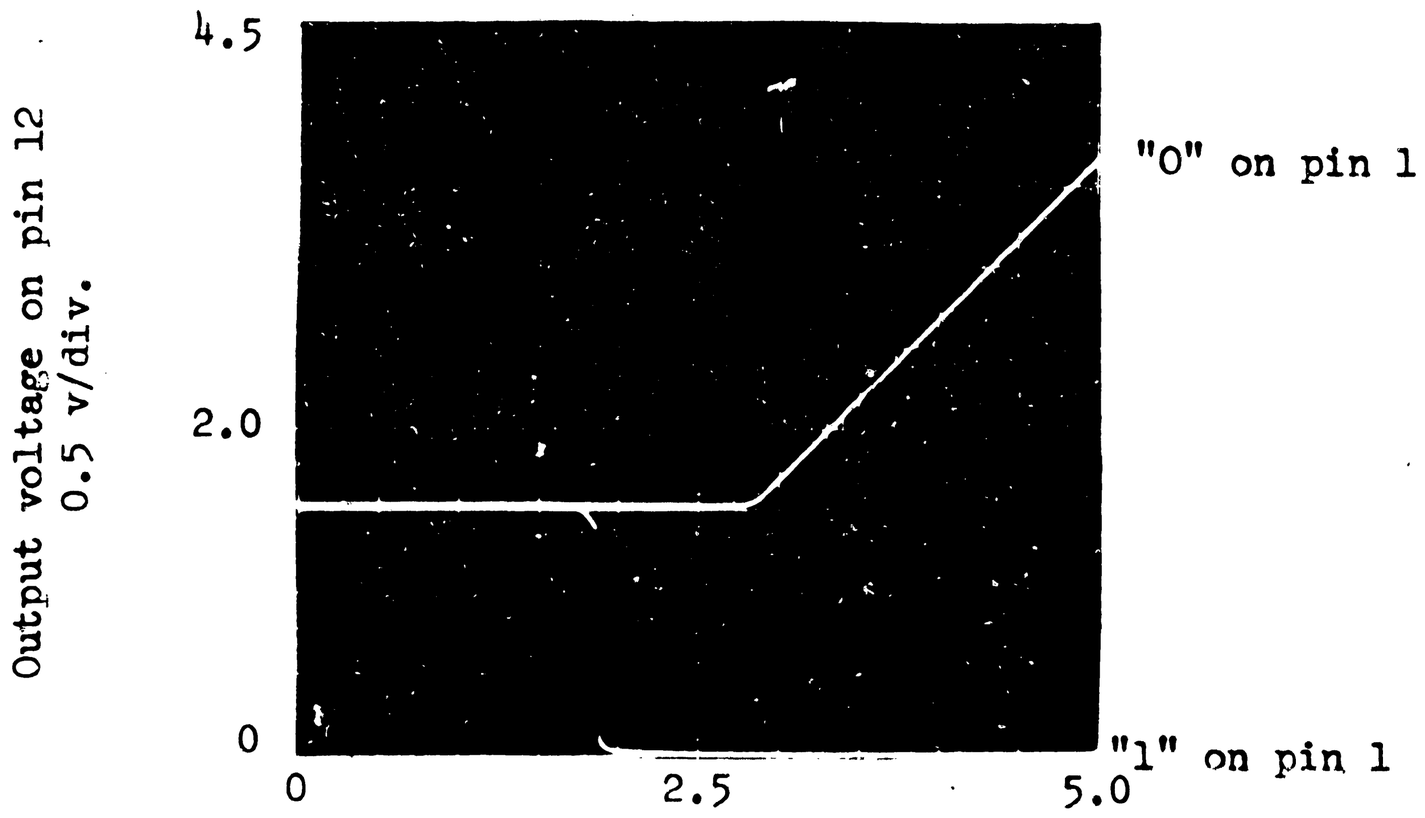
OUTPUT CHARACTERISTICS
TTL 365G8

V_{cc} to load = 5.0

N = 1

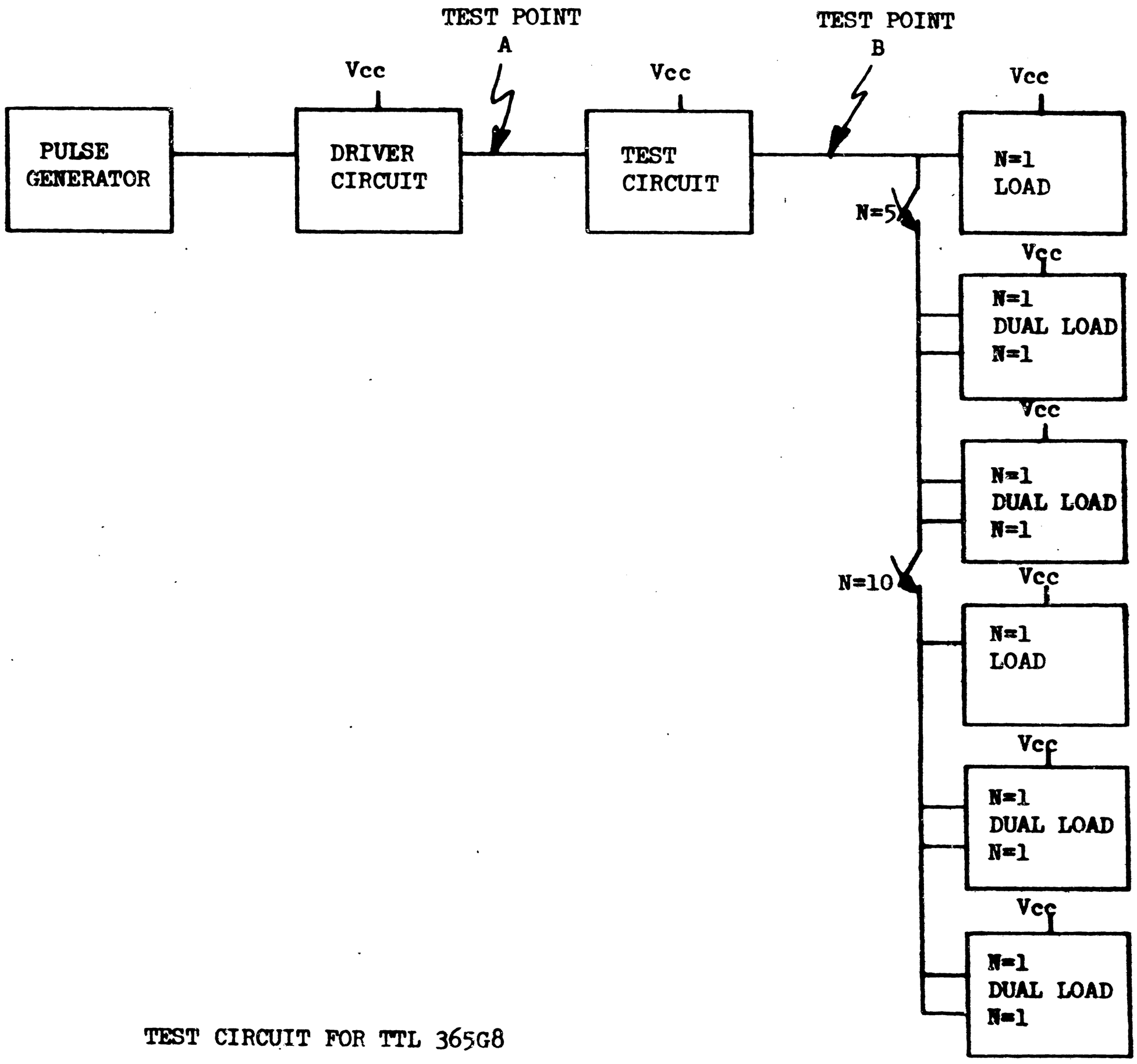


POWER DISSIPATION
TTL 365G8



OUTPUT VOLTAGE versus SUPPLY VOLTAGE
TTL 365G8

3.2.167

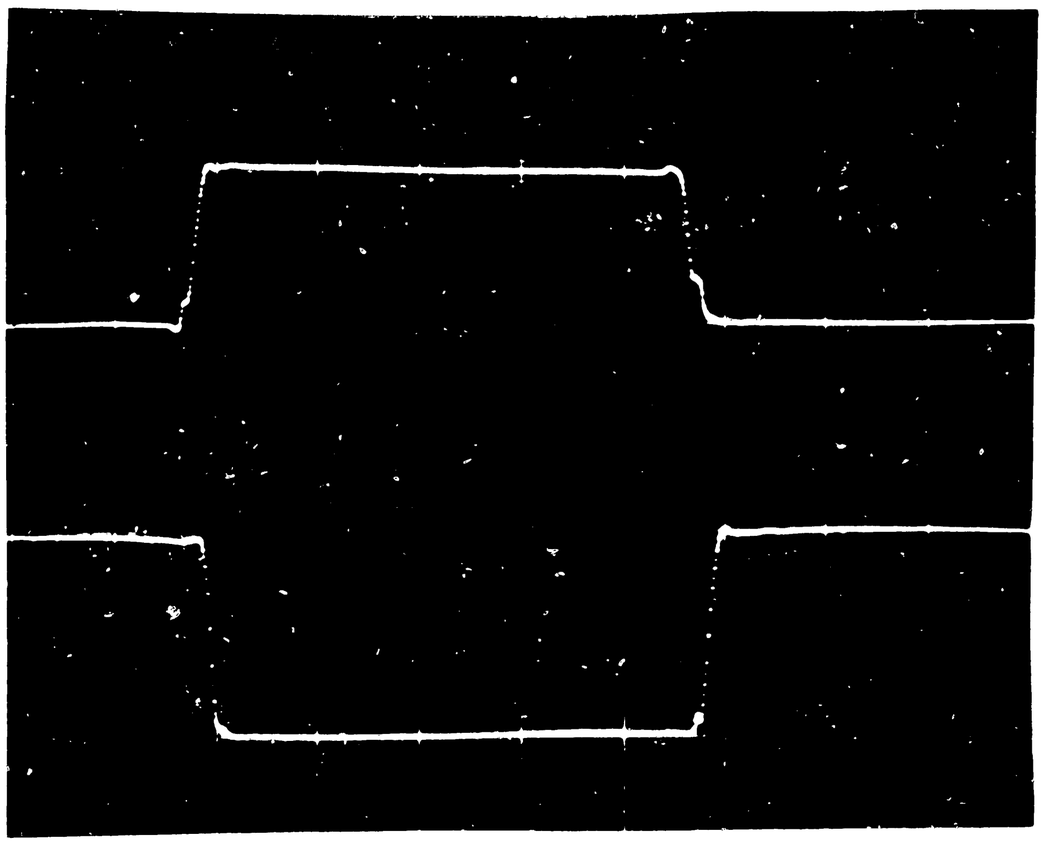


TEST CIRCUIT FOR TTL 365G8

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	502.	506.	508.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	3.6	4.25	4.95	5.65
T_r	21.	14.	14.	15.
T_f	22.	12.	11.	11.
T_d	23.	21.	21.	19.
T_s	16.	19.	19.	20.
T_{pd}	17.	17.	17.	17.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. -40°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	489.	494.	498.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	3.85	3.65	4.60	5.425
T_r	13.	14.	15.	16.
T_f	22.	15.	14.	13.
T_d		16.	19.	18.
T_s		10.	12.	12.8
T_{pd}		18.	17.	17.

Type TTL No. 365G8 Temp. -55°C Vcc 5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	486.	491.	495
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	3.735	375	4.35	5.25
T_r	12.	13.	15.	16.
T_f	22.	15.	15.	13.
T_d		22.	19.	18.
T_s		11.	11.	12.
T_{pd}		18.	17.	17.

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	511.	516.	520.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.0	4.30	4.90	5.50
T_r	31.	18.	20.	22.
T_f	23.	11.	11.0	12.
T_d		29.	28.	26.
T_s		22.	23.	25.
T_{pd}		19.	20.	20.

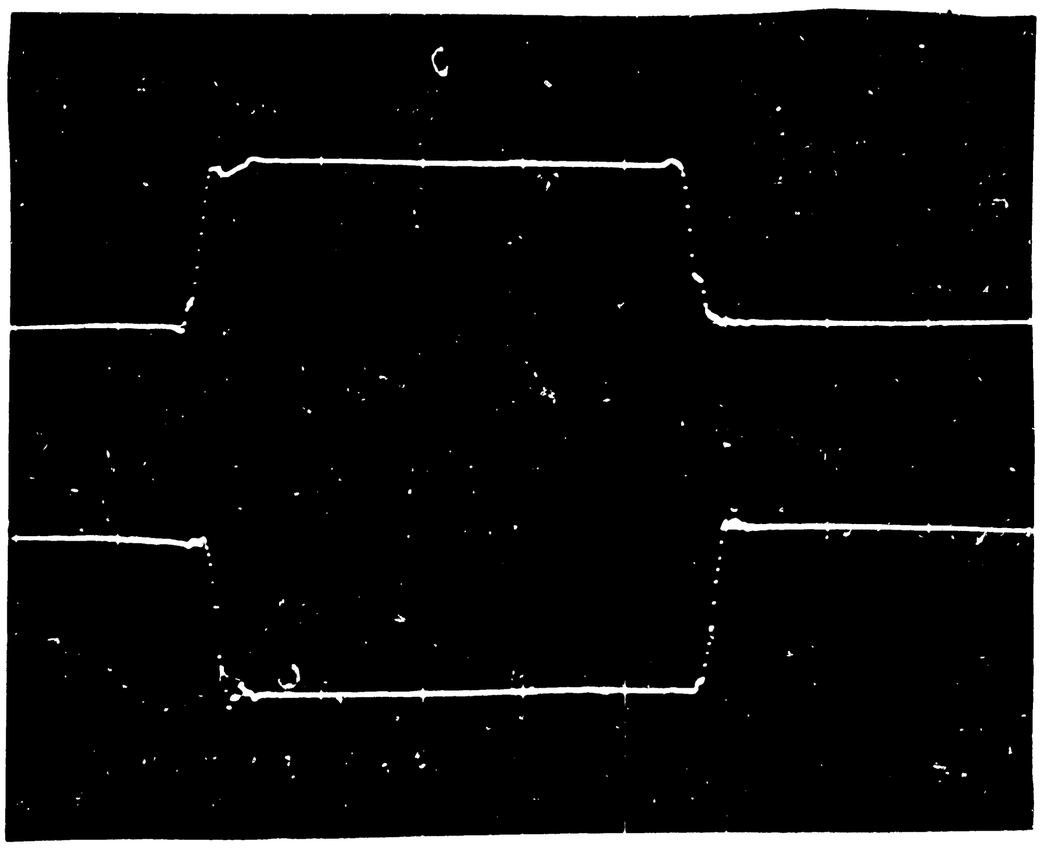
Type TTL No. 365G8 Temp. +125°C Vcc +5.0 N = 1

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	532.	536.	540.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.15	4.25	4.85	5.40
T_r	41.	23.	23.	24.
T_f	26.	15.	16.	16.
T_d		32.	31.	30.
T_s		35.	39.	41.
T_{pd}		25.	26.	27.

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	502.	505.	508.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.1	3.360	4.0	4.65
T_r	22.	15.	16.7	18.
T_f	22.	15.	16.	15.
T_d		23.	20.	20.
T_s		17.	18.	19.
T_{pd}		18.	18.	21.



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. -40°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.0
Pulse Width	500.	488.	493.	498.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	3.90	3.075	3.70	4.50
T_r	14.	15.	16.	17.
T_f	23.	18.	18.	17.
T_d		24.	20.	19.
T_s		12.	13.	14.
T_{pd}		20.	17.	19.

Type TTL No. 365G8 Temp. -55°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	484.	489.	492.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	3.775.	2.95	3.65	4.35
T_r	12.	14.	16.	17.
T_f	24.	18.	19.	18.
T_d		25.	21.	19.
T_s		11.	12.	13.
T_{pd}		20.	20.	19.

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	510.	516.	520.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.22	3.5	4.15	4.85
T_r	31.	20.	23.	27.
T_f	24.	16.5	16.	15.
T_d		29.	27.	27.
T_s		21.	23.	24.
T_{pd}		20.	20	22.

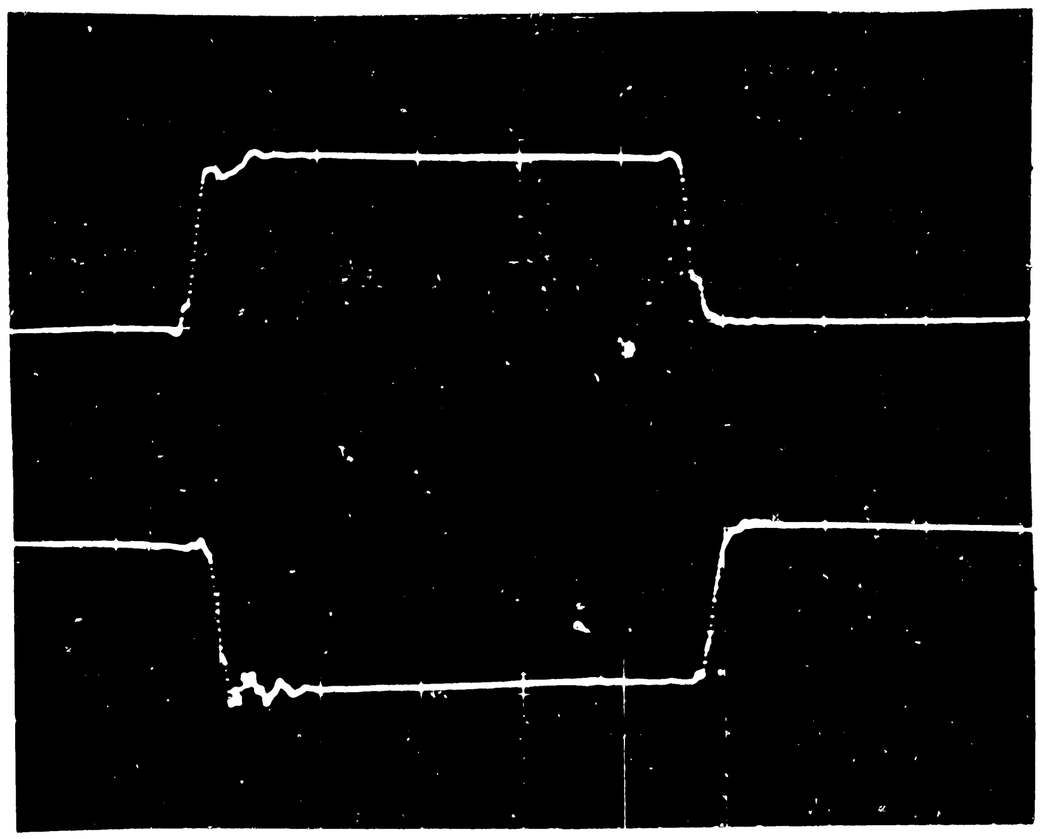
Type TTL No. 365G8 Temp. +125°C Vcc 5.0 N = 5

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	529.	535.	538.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.25	3.670	4.275	4.85
T_r	41.	28.	25.	26.
T_f	26.	18.	18	18.
T_d		32.	31.	30.
T_s		32.	39.	41.
T_{pd}		26.	28.	29.

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +25°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	501.	505.	508.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.3	3.16	3.75	4.35
T_r	22.	19.	20.	23.
T_f	23.	18.3	17.	18.
T_d	25.	23.	20.	
T_s	16.	19.	20.	
T_{pd}	20.	20.	21.	



TEST CIRCUIT INPUT

TEST CIRCUIT OUTPUT

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. -40°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	486.	494.	496.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.15	2.85	3.51	4.15
T_r	16.	19.	22.	20.
T_f	24.	19.	21.	21.
T_d		26.	19.	18.
T_s		12.	12.	15.
T_{pd}		22.	22.	21.

Type TTL No. 365G8 Temp. -55°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	483.	492.	495.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.05	2.80	3.35	3.95
T_r	14.	20.	20.	23.
T_f	24.	21.	21.	20.
T_d		18.	18.	17.
T_s		8.	9.	10.
T_{pd}		17.	19.	20.

GENERAL MICRO-ELECTRONICS

Type TTL No. 365G8 Temp. +85°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	511.	515.	519.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.4	3.325	3.85	4.45
T_r	34.	34.	32.	33.
T_f	24.	18.	18.	17.5
T_d		30.	29.	28.
T_s		26.	23.	23.
T_{pd}		23.	23.	24.

Type TTL No. 365G8 Temp. +125°C Vcc +5.0 N = 10

	TEST CKT. INPUT	TEST CIRCUIT OUTPUT FOR Vcc 4.5	Vcc 5.0	Vcc 5.5
Pulse Width	500.	529.	536.	541.
Repetition Rate	IMC	IMC	IMC	IMC
Pulse Amplitude	4.45	3.5	4.05	4.625
T_r	44.	35.	34.	35.
T_f	26.	19.	19.	18.
T_d		34.	33.	32.
T_s		31.	39.	42.
T_{pd}		27.	31.	32.

NOTES # 9.3.3

EVALUATION OF SYLVANIA DIGITAL INTEGRATED CIRCUITS

	Page
SNG-4B: Dual NAND/NOR Gate	3.3.3
SNG-5B: NAND/OR Gate	3.3.24
SNG-6B: High Fan-In NAND/NOR Gate	3.3.38
SNG-20: NAND/OR Gate (Voter Gate)	3.3.52
SFF-2B: Set-Reset Trigger Flip-Flop	3.3.61
SFF-3A: Set-Reset Trigger Flip-Flop	3.3.69

It is seldom that microcircuits are used individually, therefore testing was performed in a manner approaching system simulation.

1. Since the V_{cc} in a system is usually supplied by a single source, the question arises as to the amount of change in the circuit parameters which will be caused by a variation of V_{cc}. The three voltages selected for this test were 4.5, 5.0 and 5.5 since the manufacturer centered around 5.0 volts.

2. Loading was accomplished by means of dual SNG-4B units. In the standard test set-up for gates, the following two load conditions were imposed upon the test circuit: A load of "1" circuit and a load of "20" circuits. For this report, a load will be defined as that load presented by one input per each single gate circuit connected to the output of the circuit. Dual elements were used as loads, therefore each circuit represented a load of "2".

3. The input signals to the test circuit were produced by a driver circuit which was a dual element SNG-4B. This dual driver circuit which was driven from a pulse generator enabled a positive input to the test circuit since a negative going pulse was not available on the generator used.

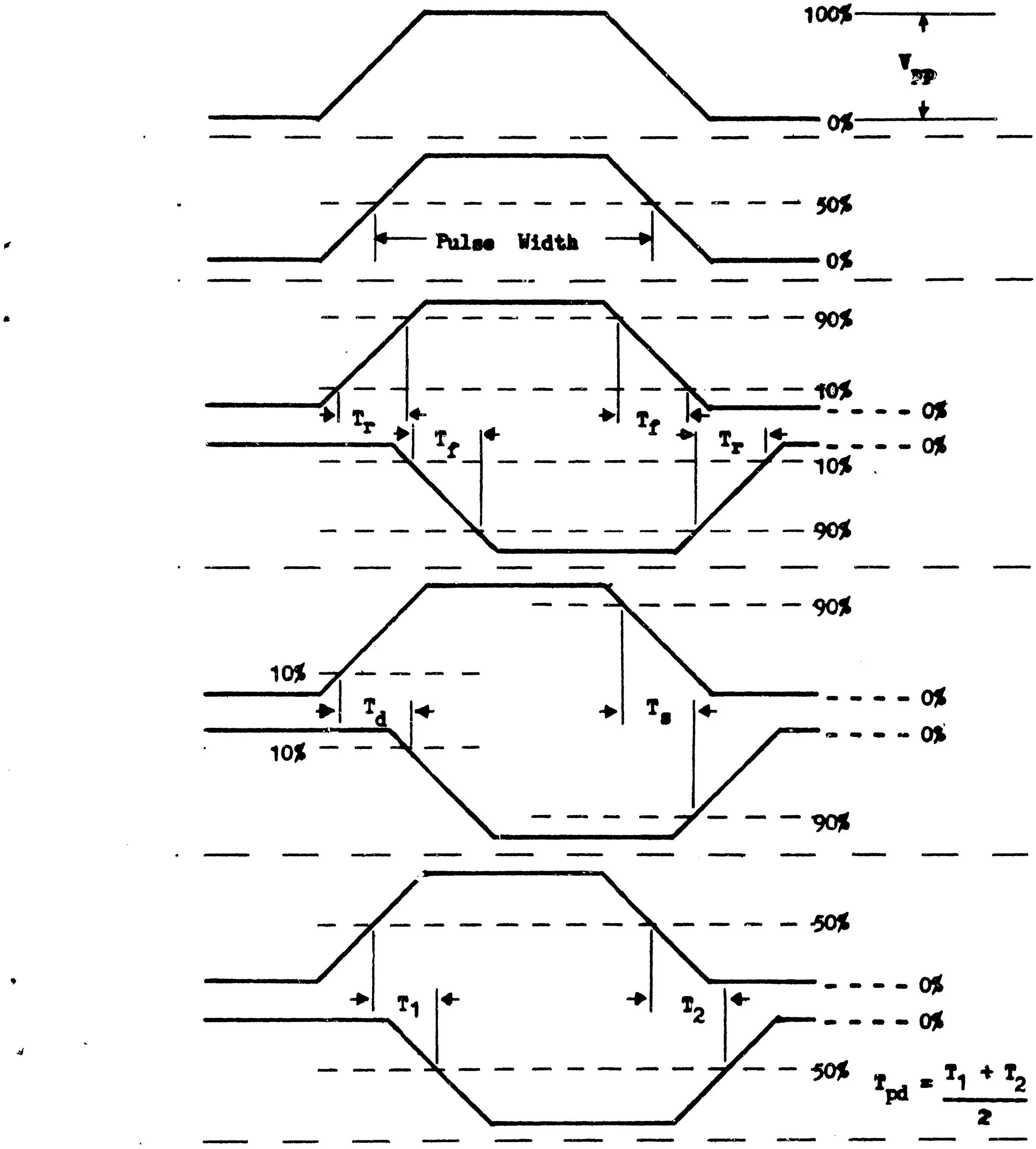
The driver circuit provided isolation between the generator and the test circuit as well as providing test circuit input variances as the V_{cc} to the entire system was varied.

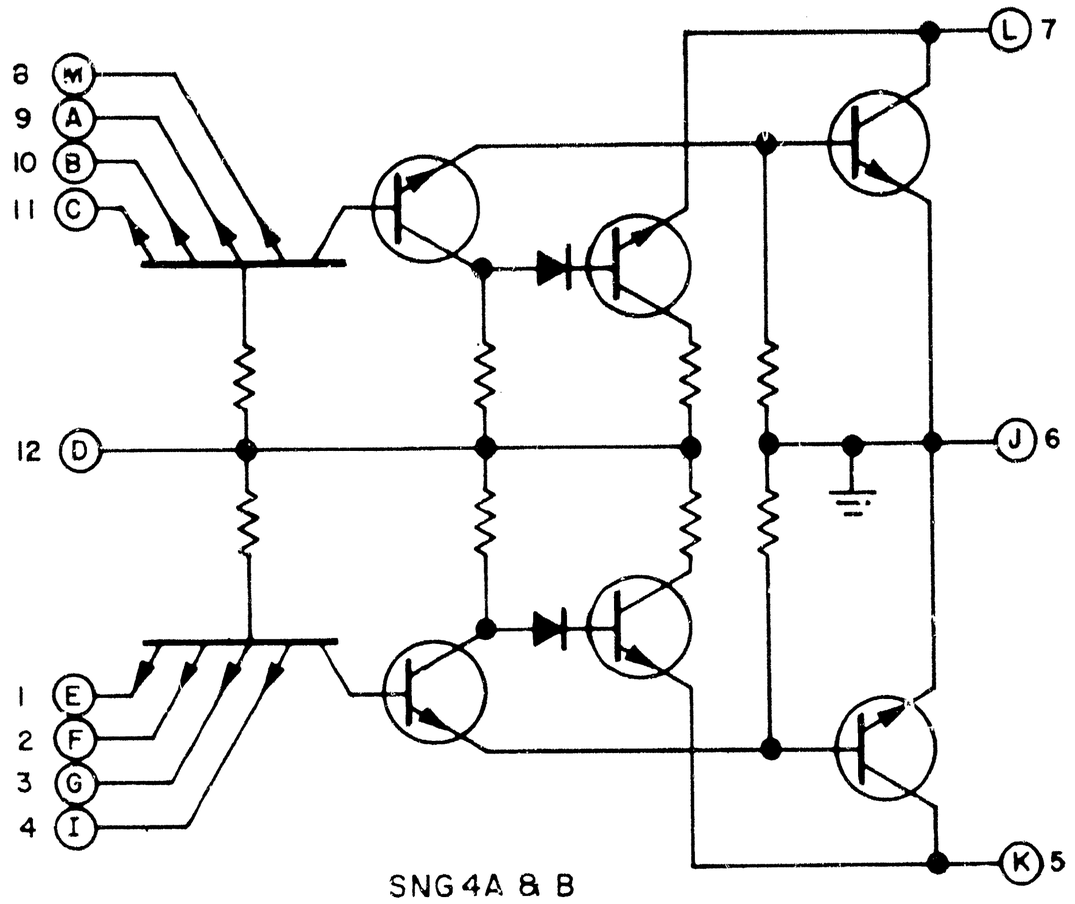
In the case of the flip-flops, which require alternate inputs, one signal was passed through a dual element for a positive input while the other was passed through a single element to produce a negative input. This provided alternate inputs with a time lag between them which was approximately equal to the propagation delay of "1" circuit. Measurements were made from the input traversing the most circuits before entering the test circuits. This ensured that the other input was already present and any effect on circuit operation was due to the input being monitored.

4. All of the elements of the system were subjected to the same temperature conditions. The temperatures used were: -55°C, -40°C, +25°C, +85°C, and +125°C.

5. The test fixture used was constructed from a glass epoxy sheet on which the wiring was kept at a minimum. A 1.0 mfd capacitor was used between V_{cc} and ground on the surface of the board. Signals were taken from B.N.C. connectors mounted as close to the circuit leads as possible. The probes used for measuring circuit parameters were of the cathode follower type and are approximately 10 megohms shunted by 2.6 pfd to ground.

6. The measurements made in this section are illustrated on the following page.


100%
V_{PP}
0%
50%
Pulse Width
0%
90%
10%
T_r
T_f
T_f
T_r
10%
0%
0%
90%
90%
10%
T_d
T_s
10%
0%
0%
90%
50%
T_1
T_2
0%
0%
50%
$T_{pd} = \frac{T_1 + T_2}{2}$



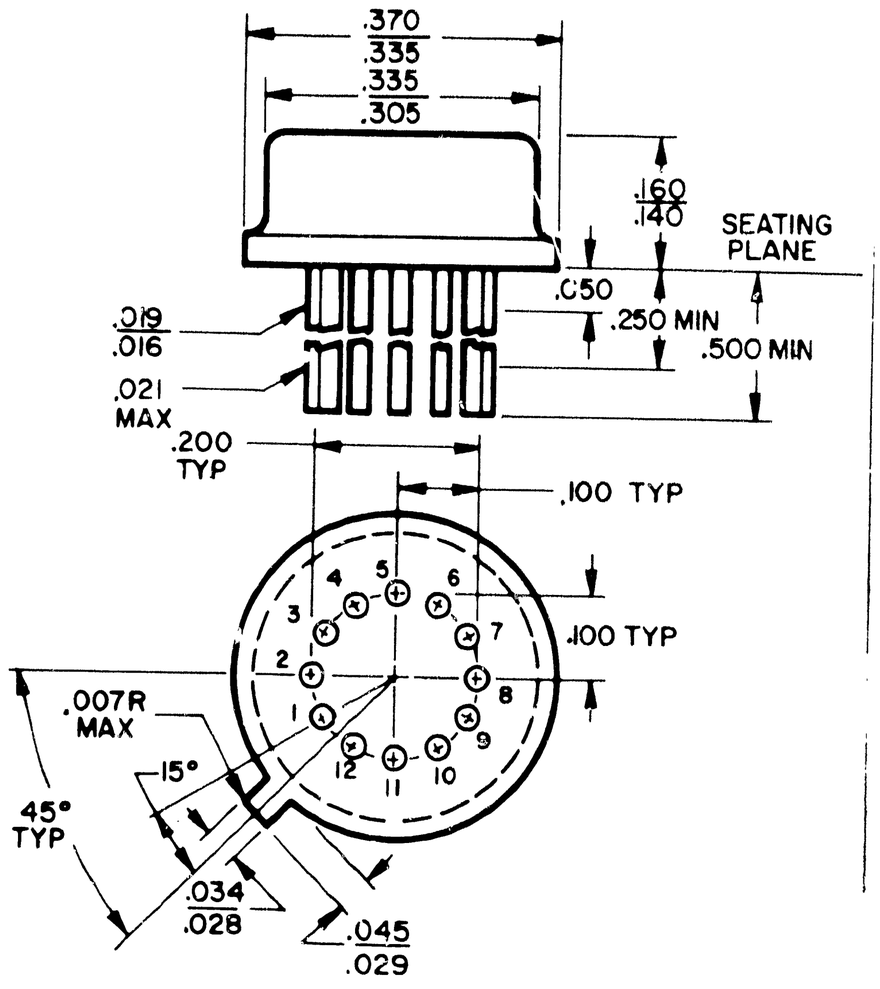
SNG 4A & B

(+) LOGIC	(−) LOGIC
$L = \overline{A \cdot B \cdot C \cdot M}$	$L = \overline{A+B+C+M}$
$K = \overline{E \cdot F \cdot G \cdot I}$	$K = \overline{E+F+G+I}$

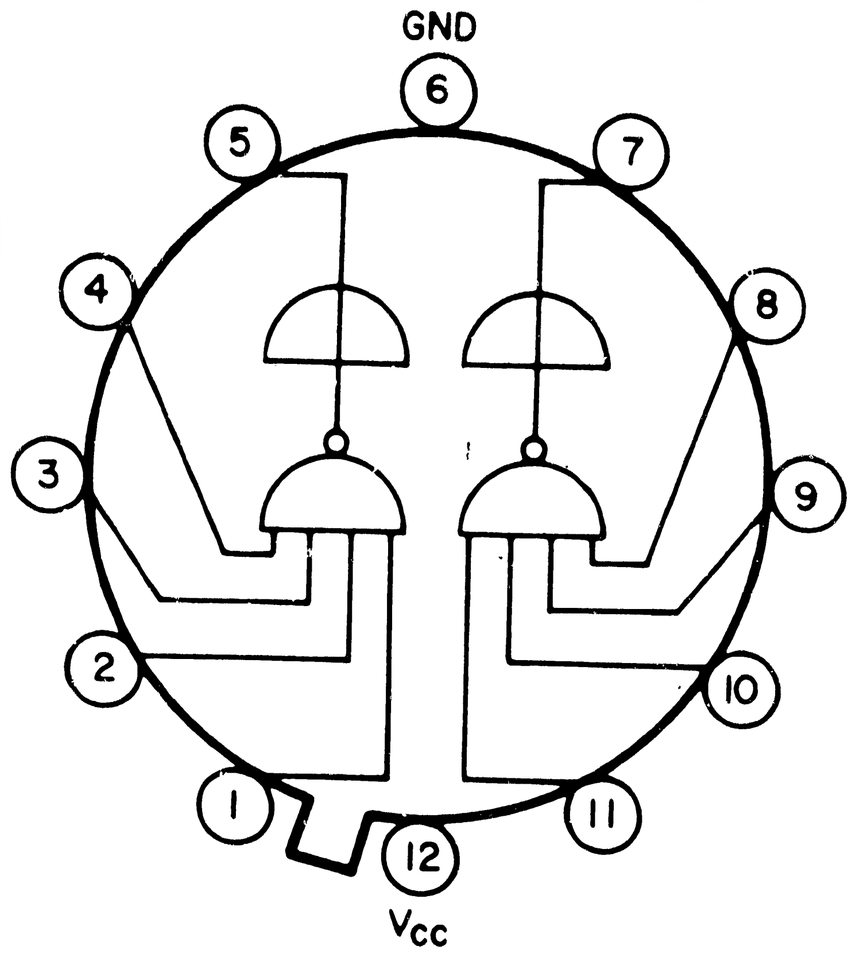
DUAL NAND/NOR GATE

The SNG-4A is a dual, three input AND gate, while the SNG-4B is a dual, four input AND gate. Both the "A" and the "B" versions are followed by an inverting amplifier. The circuits can function as NAND/NOR elements or, when cross-coupled, as set-reset flip-flops.

The "A" and "B" versions both require only one power supply and are members of the monolithic, epitaxial, and planar family.



12 LEAD TO-5



BOTTOM VIEW

SNG-4B

FOR SNG-4A INPUTS 9-A AND 3-G ARE NOT PRESENT

GENERAL GUIDE TO TESTING PROCEDURE USED FOR GATE CIRCUITS:

I. D.C. characteristics

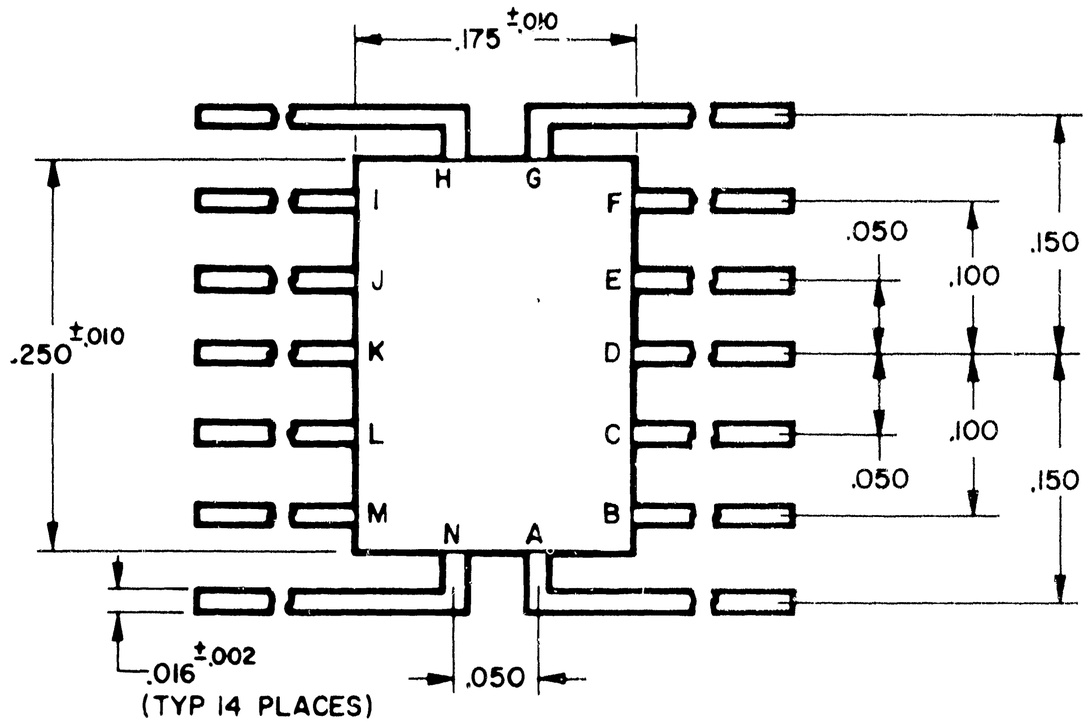
II. Dynamic characteristics

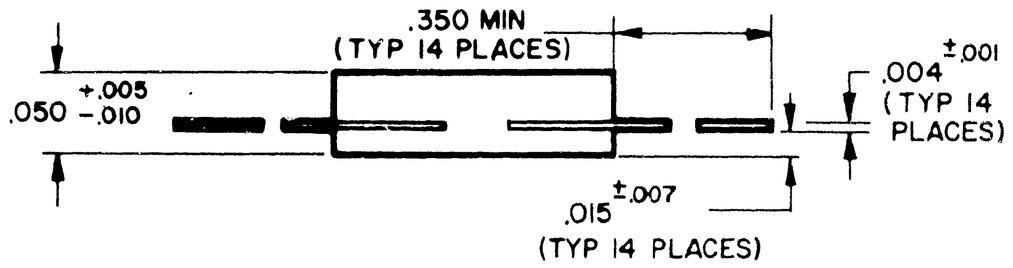
A. Generator driven

1. Variation of frequency
   a. Variation of V_{cc}
      (1.) Variation of temperature
2. Variation of loads

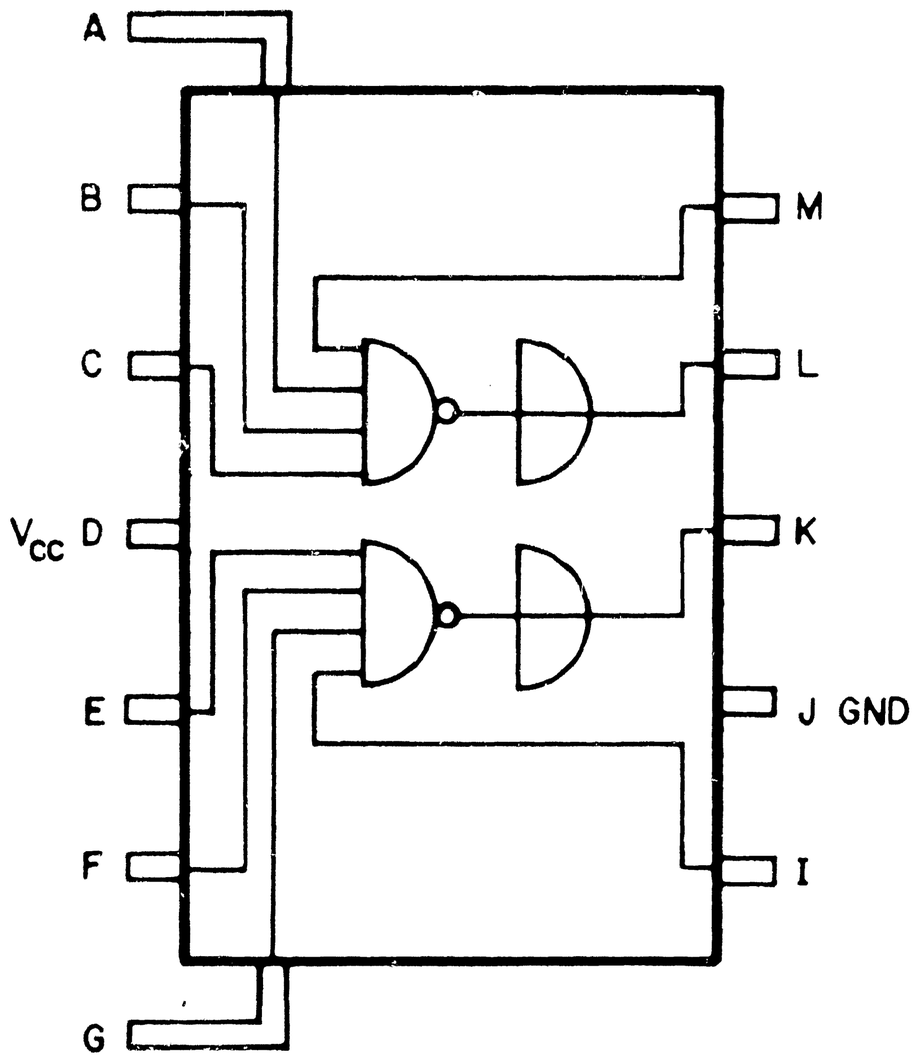
B. Ring counter driven

1. Variation of elements
   a. Variation of V_{cc}
      (1.) Variation of temperature





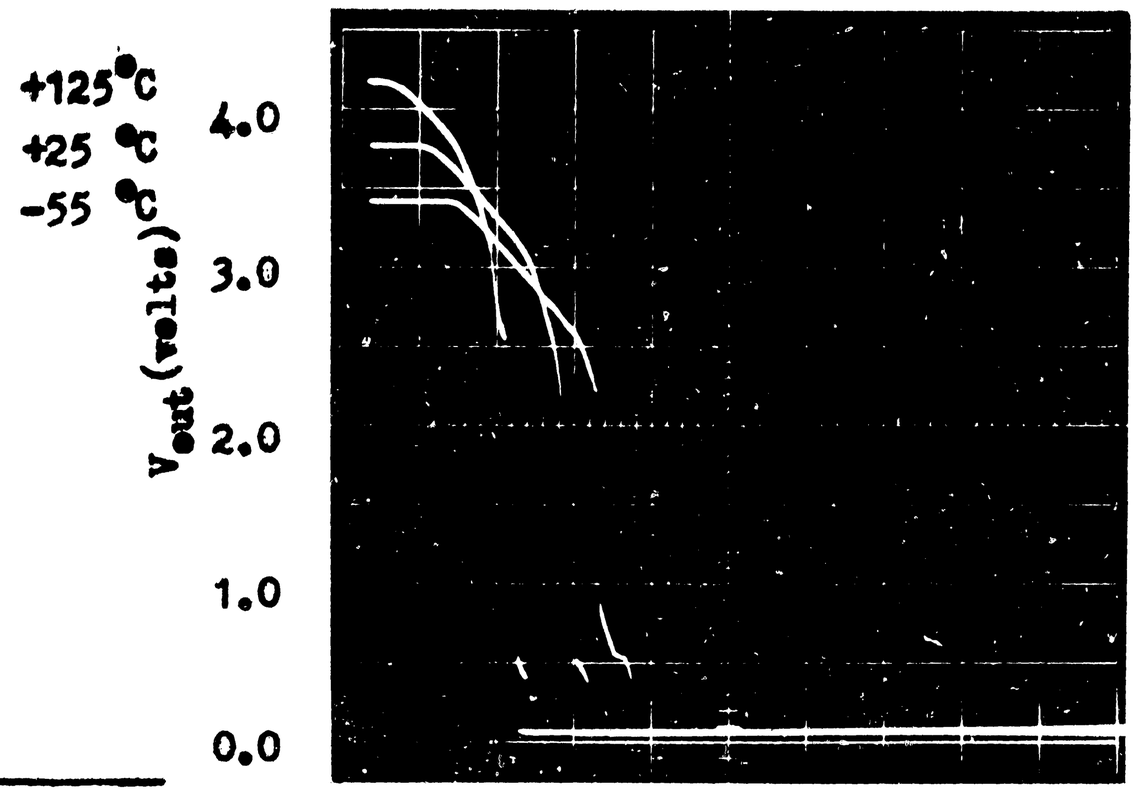
14-LEAD FLAT PACK



TOP VIEW

V_{in} vs. V_{out}

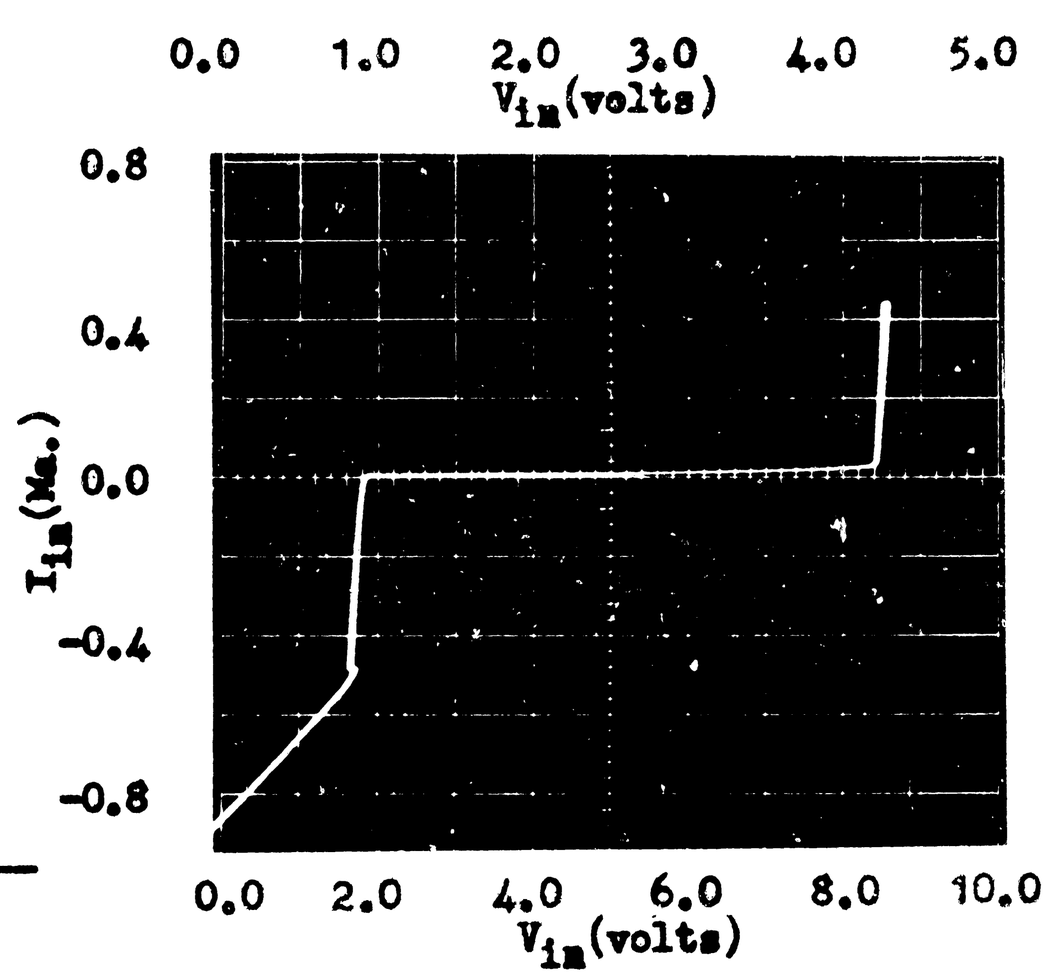
1.) V_{cc} = 5 v.



V_{in} vs. I_{in}

1.) V_{cc} = 5 v.

2.) T = 25°C

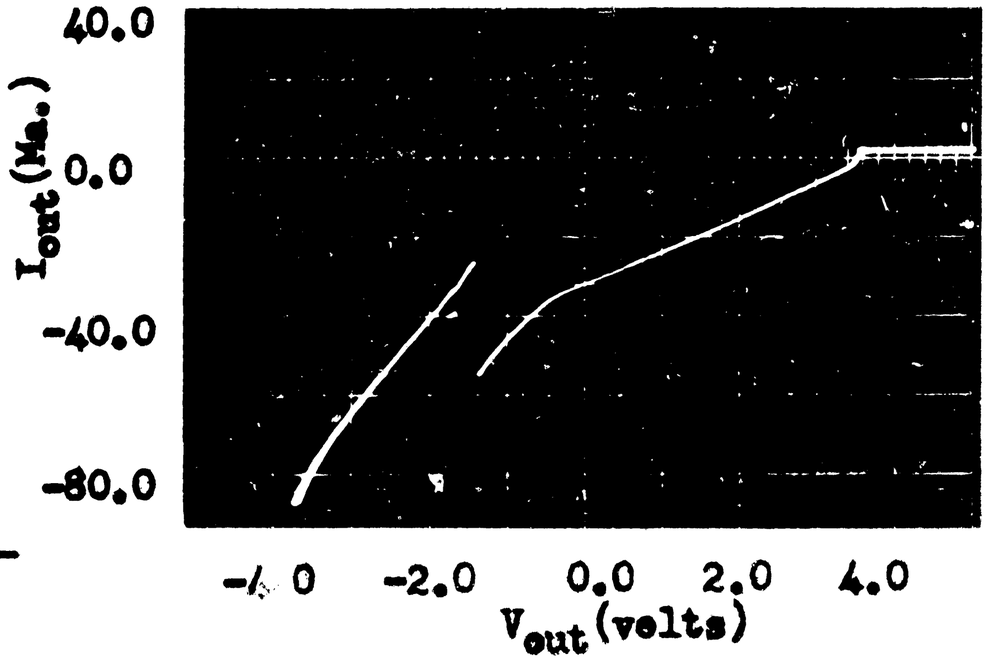


V_{out} vs. I_{out}

1.) V_{cc} = 5 v.

2.) T = 25°C

3.) Pin #3 & #10 @ ground.

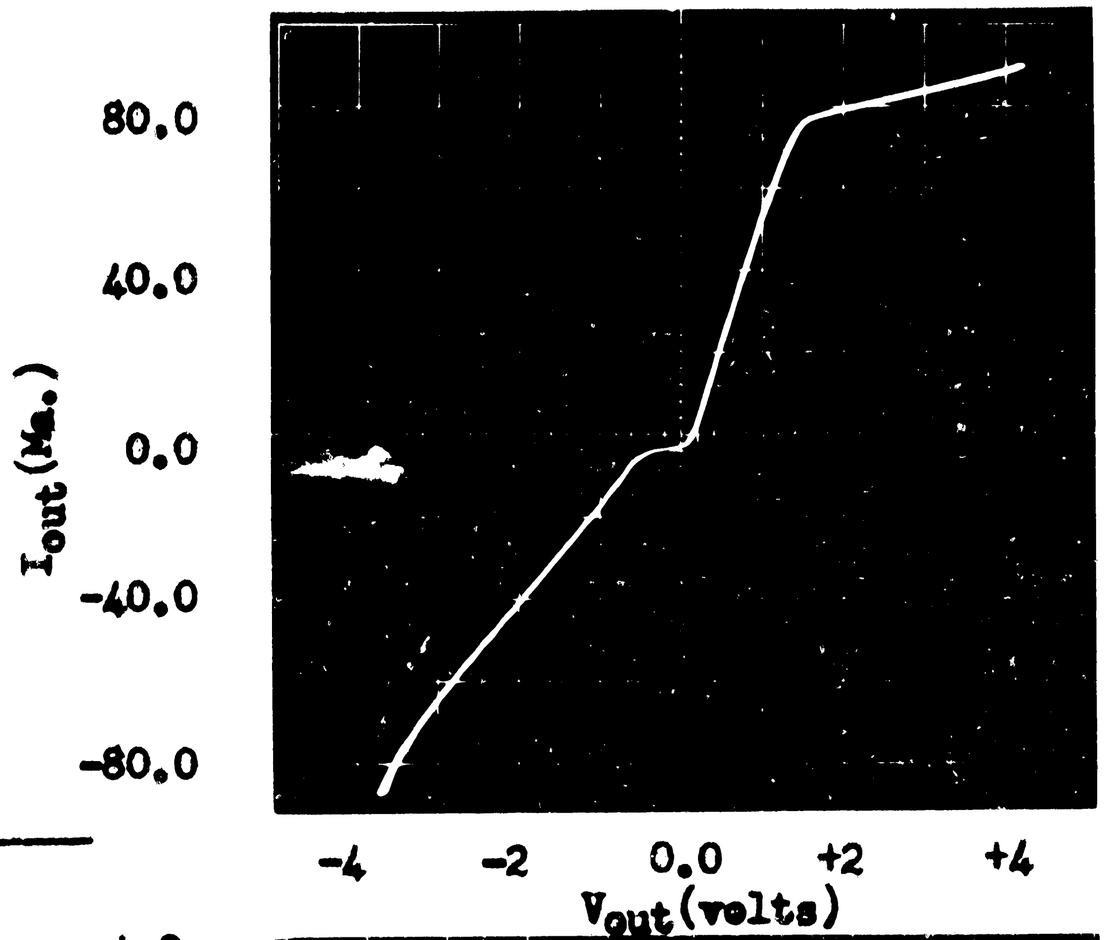


V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5.0 v.

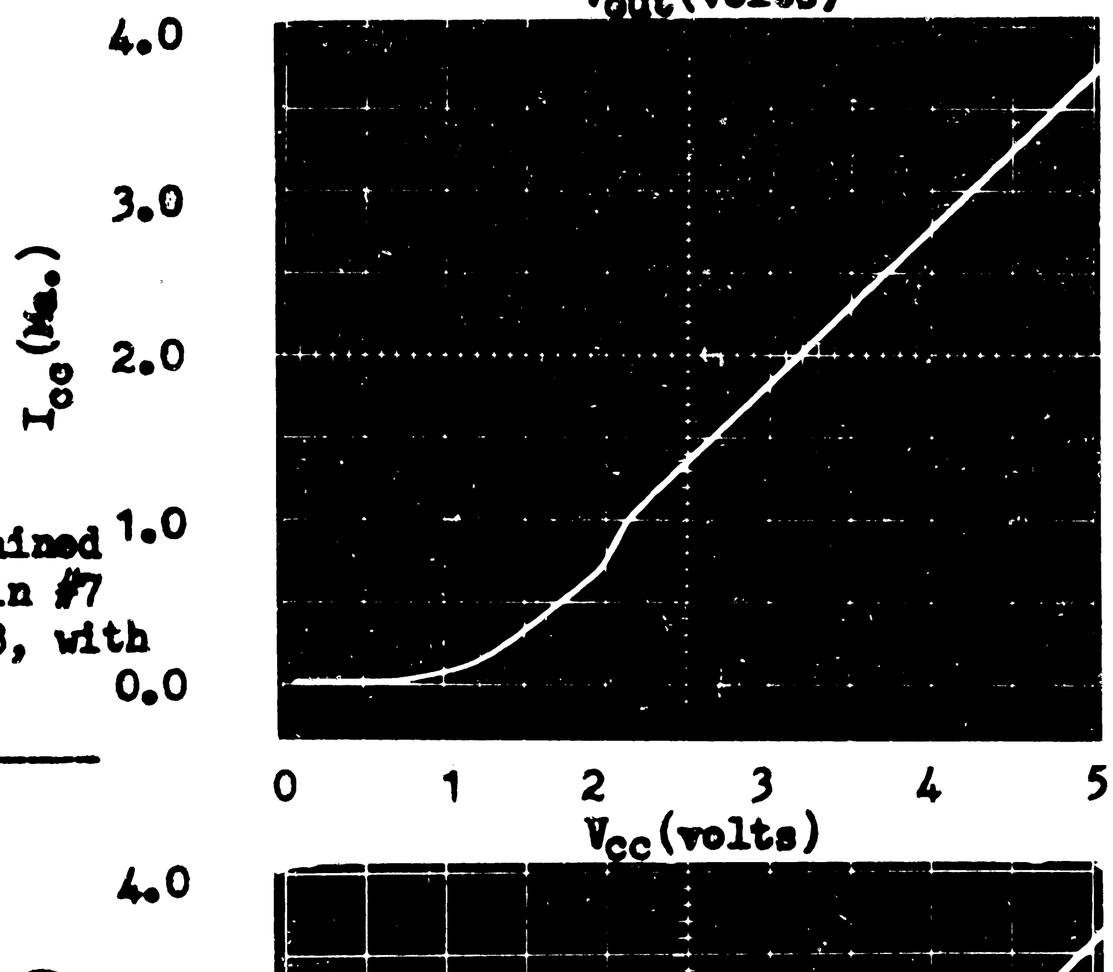
3.) All inputs high



V_{cc} vs. I_{cc}

1.) T = 25°C

2.) 50% duty cycle obtained with high output pin #7 connected to pin #3, with pin #10 grounded.

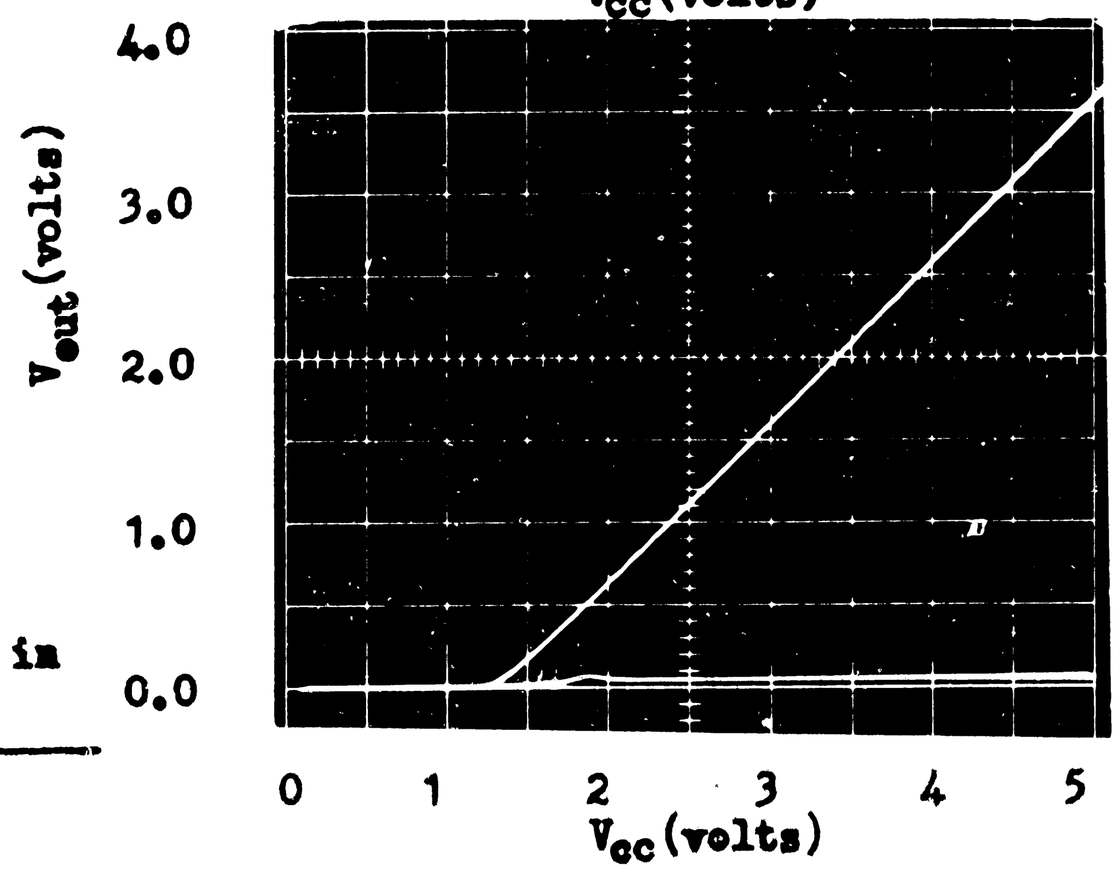


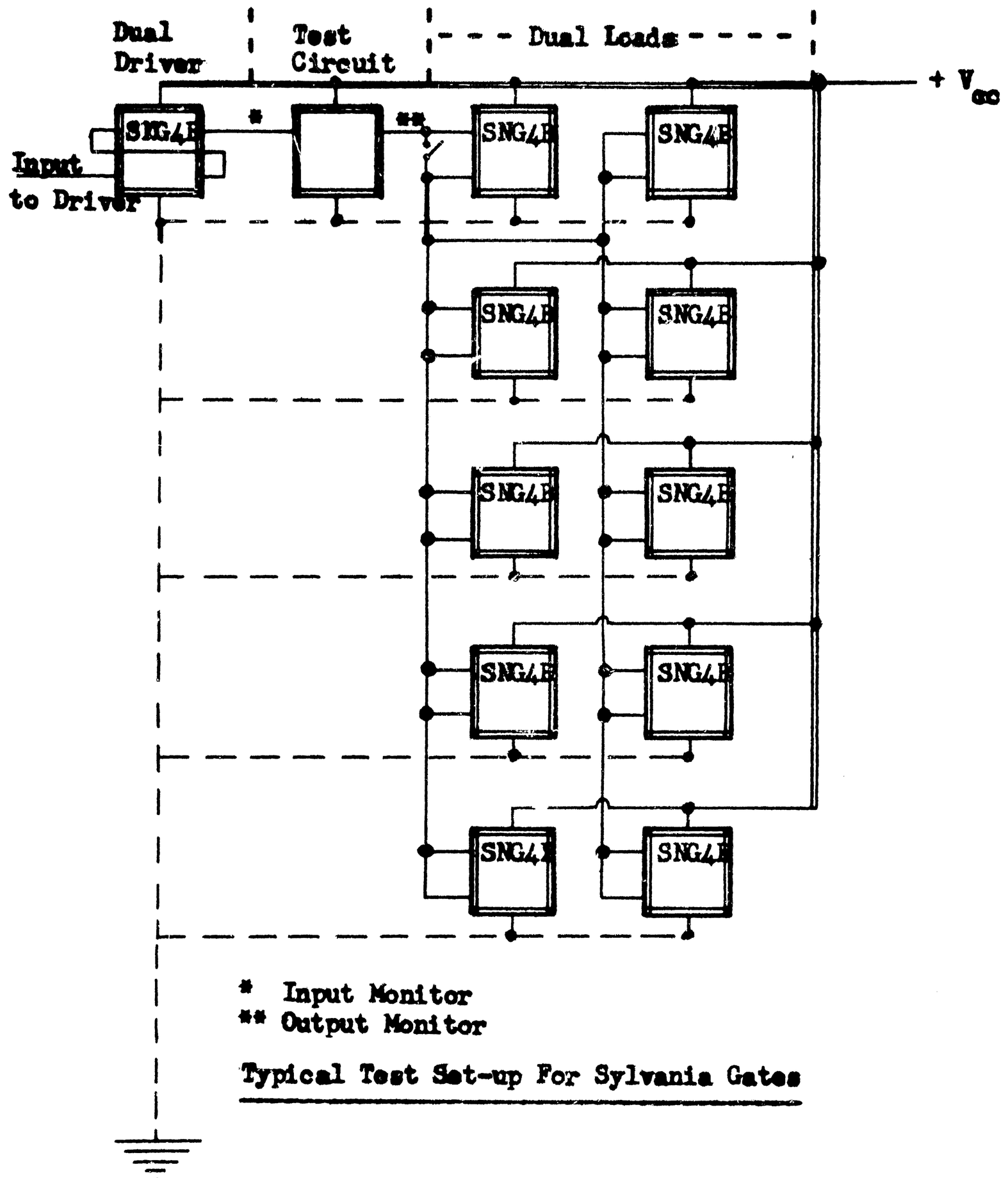
V_{cc} vs. V_{out}

1.) T = 25°C

2.) Top trace = "0" in

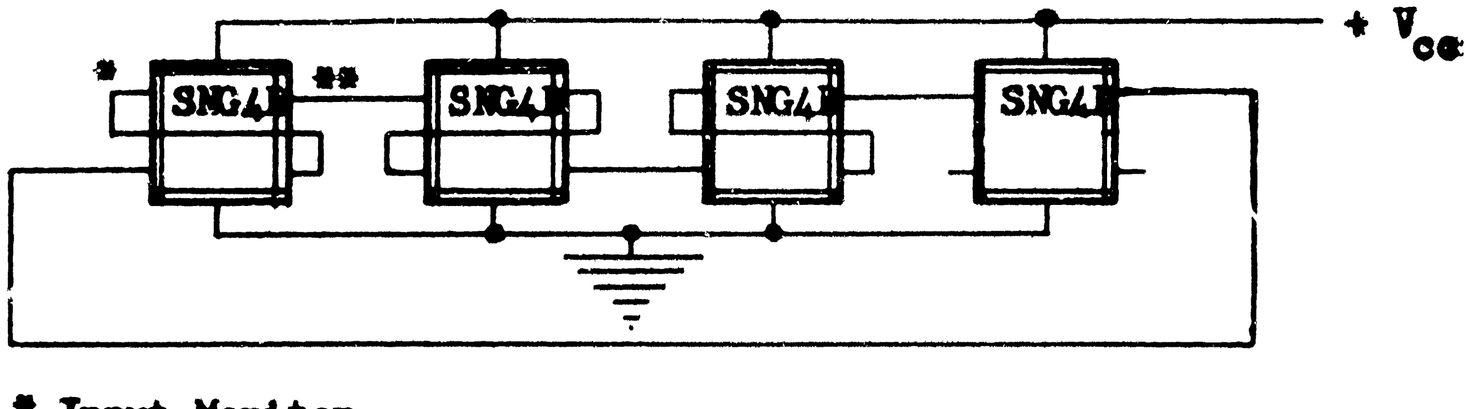
3.) Bottom trace = "1" in





* Input Monitor
** Output Monitor

Typical Test Set-up For Sylvania Gates



* Input Monitor
** Output Monitor

SNG 4B 7 Element Ring Counter

Circuit SNi 4B	Supply Voltage 4.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	2.7	2.6	2.9	2.3	2.8	2.7	3.0	2.4	2.9	2.9	3.4	2.6
Pulse Width (ns.)	200	185	200	179	200	190	200	185	200	195	200	196
T_r (ns.)	6.0	4.5	7.0	11	6.0	5.0	8.0	11	9.0	8.0	12	15
T_f (ns.)	8.5	10	9.0	31	8.0	10	8.0	27	6.0	6.0	5.4	14
T_d (ns.)		17		19		15		16		11		12
T_s (ns.)		8.0		8.0		8.0		8.0		7.0		7.0
T_{pd} (ns.)		13		19		12		16		9.5		12

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.1	3.7	2.8	3.2	3.3	3.7	2.8
Pulse Width (ns.)	200	201	200	205	200	206	200	211
T_r (ns.)	13	12	19	21	18	16	41	27
T_f (ns.)	5.0	5.0	5.0	13	5.5	5.5	6.0	12
T_d (ns.)		11		11		10		10
T_s (ns.)		7.5		8.5		8.0		9.0
T_{pd} (ns.)		8.5		12		8.5		11

Circuit SNJ 4B	Supply Voltage 5.0				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.1	3.5	2.8	3.3	3.1	3.6	2.8	3.4	3.3	3.9	3.0
Pulse Width (ns.)	200	192	200	192	200	193	200	194	200	198	200	200
T_r (ns.)	6.6	5.5	9.0	12	6.8	5.5	10	12	9.8	8.5	14	16
T_f (ns.)	6.8	8.5	7.0	26	6.0	7.5	6.0	19	5.0	5.5	5.0	13
T_d (ns.)		12.7		14		11.8		13		9.8		11
T_s (ns.)		7.4		8.0		7.0		7.0		7.0		7.0
T_{pd} (ns.)		10		15		9.0		13		8.0		11

Temperature:	+85°C				+125°C			
Lead	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.7	3.7	4.2	3.3	3.7	3.8	4.3	3.5
Pulse Width (ns.)	200	205	200	207	200	209	200	215
T_r (ns.)	15	13	38	23	20	17	39	27
T_f (ns.)	5.0	5.0	5.0	11	5.0	5.0	5.0	8.5
T_d (ns.)		9.4		9.5		9.0		9.0
T_s (ns.)		7.5		8.5		8.0		10
T_{pd} (ns.)		8.0		11		8.0		11

Circuit SMG 4B	Supply Voltage 5.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.7	3.5	4.1	3.2	3.7	3.6	4.2	3.3	3.9	3.8	4.5	3.5
Pulse Width (ns.)	200	196	200	196	200	196	200	197	200	199	200	204
T_r (ns.)	7.0	6.0	10	15	8.0	6.0	11	15	10	9.0	16	20
T_f (ns.)	6.0	7.0	5.0	18	5.0	6.0	5.0	15	4.5	5.0	5.0	12
T_d (ns.)		10		12		10		11		8.8		9.0
T_s (ns.)		7.0		7.0		7.0		7.0		6.5		7.0
T_{pd} (ns.)		9.5		13		8.5		13		7.0		10

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	4.1	4.1	4.9	3.8	4.2	4.2	4.8	3.9
Pulse Width (ns.)	200	206	200	211	200	212	200	218
T_r (ns.)	16	14	37	24	21	18	38	26
T_f (ns.)	4.5	4.5	5.0	11	4.8	4.6	5.0	8.0
T_d (ns.)		8.5		9.0		8.0		8.0
T_s (ns.)		7.0		8.0		8.0		10
T_{pd} (ns.)		7.5		11		11		11

Circuit SNC 4B	Supply Voltage 5.0				Frequency = 6 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.1	3.7	2.9	3.2	3.2	3.8	3.0	3.4	3.4	4.1	3.2
Pulse Width (ns.)	50	46	50	46	50	47	50	48	50	49	50	51
T_r (ns.)	6.5	6.0	10	14	7.0	6.0	11	15	10	9.0	35	18
T_f (ns.)	5.0	7.0	5.0	26	5.0	6.0	5.0	17	4.0	5.0	5.0	13
T_d (ns.)		10		11		9.0		10		8.0		9.0
T_s (ns.)		7.0		6.5		6.0		7.0		6.0		8.0
T_{pd} (ns.)		8.5		12		8.0		11		7.5		10

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.6	3.6	4.3	3.4	3.8	3.8	4.3	3.5
Pulse Width (ns.)	50	55	50	59	50	60	50	66
T_r (ns.)	15	13	38	23	20	17	39	27
T_f (ns.)	4.0	5.0	5.0	13	4.5	5.0	5.0	12
T_d (ns.)		8.0		9.0		8.0		8.0
T_s (ns.)		7.0		8.0		8.0		9.0
T_{pd} (ns.)		7.5		10		7.0		11

SNG 4B V_{cc}=5.0 v. Frequency = 1 mc. Input Pulse Width = 200 nsec.

Load Ckts.	20	18	16	14	12	10	8	6	4	2
T_{pd}	11.0	10.6	10.6	10.6	10.5	10.1	10.0	9.5	9.5	9.2
T_r Output	16.8	15.2	14.7	14.2	13.5	12.7	12.0	11.0	10.5	10.2
T_f Output	12.5	12.0	11.5	11.0	10.4	9.8	9.0	8.5	7.4	6.5
Pulse Amp. (Input)	4.0	3.8	3.8	3.7	3.7	3.6	3.6	3.5	3.4	3.3
Pulse Amp. (Output)	2.98	3.02	3.06	3.06	3.08	3.12	3.20	3.22	3.24	3.26

Temperature = 25°C.

SNG 4 B Ring Counter (7 elements)

Temperature °C	-55		-40		+25		+85		+125	
Frequency mc.	7.4 ---		8.0 ---		9.0 ---		8.5 ---		8.1 ---	
V_{cc} volts	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	2.9	2.9	3.0	2.8	3.1	2.9	3.3	3.2	3.5	3.2
Pulse Width nsec.	71	66	65	61	57	56	57	61	58	67
T_r nsec.	6.0	4.4	6.6	4.3	9.4	6.3	14	10	18	13
T_f nsec.	8.5	6.3	7.6	5.5	5.7	4.3	5.4	4.0	5.4	4.0
T_d nsec.	—	11	—	10	—	8.3	—	7.7	—	7.6
T_s nsec.	—	8.6	—	8.3	—	7.7	—	8.4	—	9.0
T_{pd} nsec.	—	9.1	—	8.6	—	7.4	—	7.2	—	7.4

SNG 4B Ring Counter (7 elements)

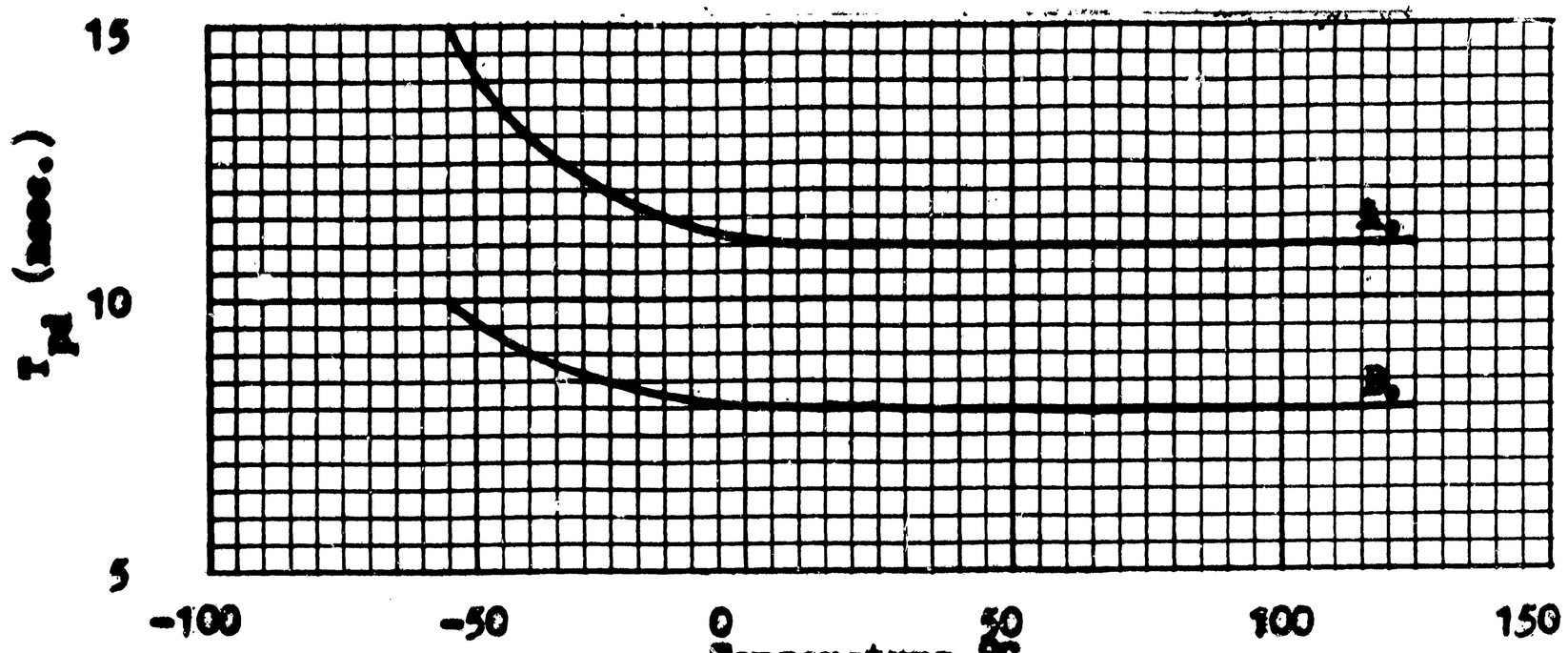
Temperature °C	-55		-40		+25		+85		+125	
Frequency mc.	8.4 ---		8.8 ---		9.6 ---		8.9 ---		8.3 ---	
V_{cc} volts	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.4	3.3	3.4	3.9	3.6	3.5	3.8	3.6	3.9	3.7
Pulse Width nsec.	62	60	58	56	52	54	53	60	55	67
T_r nsec.	7.2	4.7	7.5	4.9	10	7.6	15	12	20	15
T_f nsec.	7.4	5.5	6.6	5.0	5.0	4.0	4.9	4.0	5.0	4.2
T_d nsec.	—	9.6	—	8.8	—	7.3	—	7.0	—	7.0
T_s nsec.	—	8.5	—	8.1	—	7.7	—	8.0	—	9.0
T_{pd} nsec.	—	8.5	—	7.9	—	7.0	—	6.9	—	7.0

SNG 4 B Ring Counter (7 element)

Temperature °C	-55		-40		+25		+85		+125	
Frequency mc.	8.8 —		9.4 —		10 —		9.2 —		8.3 —	
V_{cc} volts	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.9	3.7	4.0	3.8	4.1	3.9	4.4	4.2	4.5	4.3
Pulse Width nsec.	56	56	53	53	49	52	50	60	53	68
T_r nsec.	8.3	5.2	9.0	5.6	12	8.7	17	13	21	16
T_f nsec.	6.5	5.0	5.8	4.5	4.6	3.9	4.5	4.0	4.8	4.1
T_d nsec.	—	8.4	—	7.7	—	6.6	—	6.4	—	6.6
T_s nsec.	—	8.4	—	8.0	—	7.7	—	8.3	—	9.0
T_{pd} nsec.	—	7.9	—	7.4	—	6.6	—	6.5	—	7.5

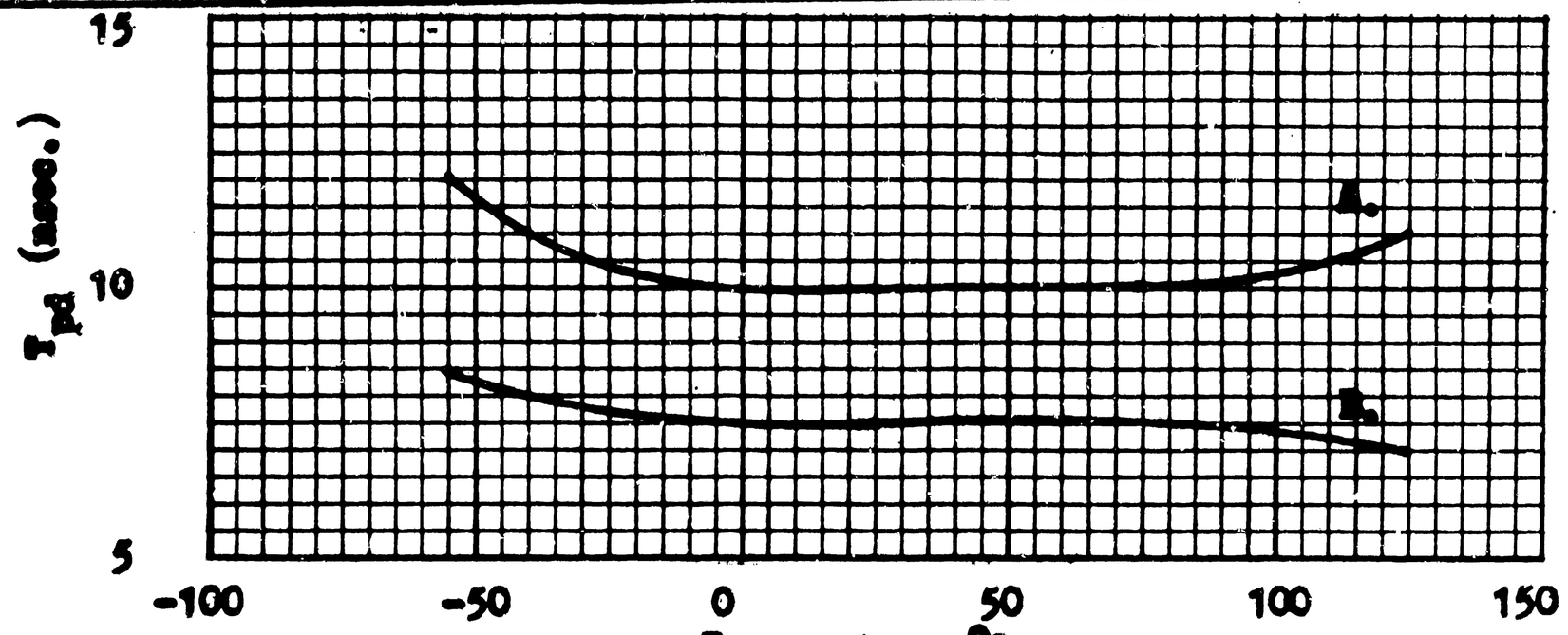
SNG 4 B Ring Counter (3 element)

Temperature °C	-55 —		-40 —		+25 —		+85 —		+125 —	
Frequency mc.	20.1 —		21.8 —		25.0 —		24.8 —		22.8 —	
V_{cc} volts	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0
Test Circuit	in	out	in	out	in	out	in	out	in	out
Pulse Amp. volts pp.	3.6	3.4	3.6	3.5	3.8	3.3	3.8	3.7	3.5	3.5
Pulse Width nsec.	27	25	25	23	19	22	18	23	17	27
T_r nsec.	5.0	5.0	5.0	5.0	11	9.0	11	10	13	13
T_f nsec.	6.7	6.0	6.0	5.0	4.0	4.0	5.0	4.0	5.0	4.0
T_d nsec.	—	9.0	—	8.0	—	7.0	—	7.0	—	7.0
T_s nsec.	—	8.0	—	8.0	—	8.0	—	8.0	—	8.0
T_{pd} nsec.	—	8.2	—	7.7	—	6.5	—	6.0	—	6.0



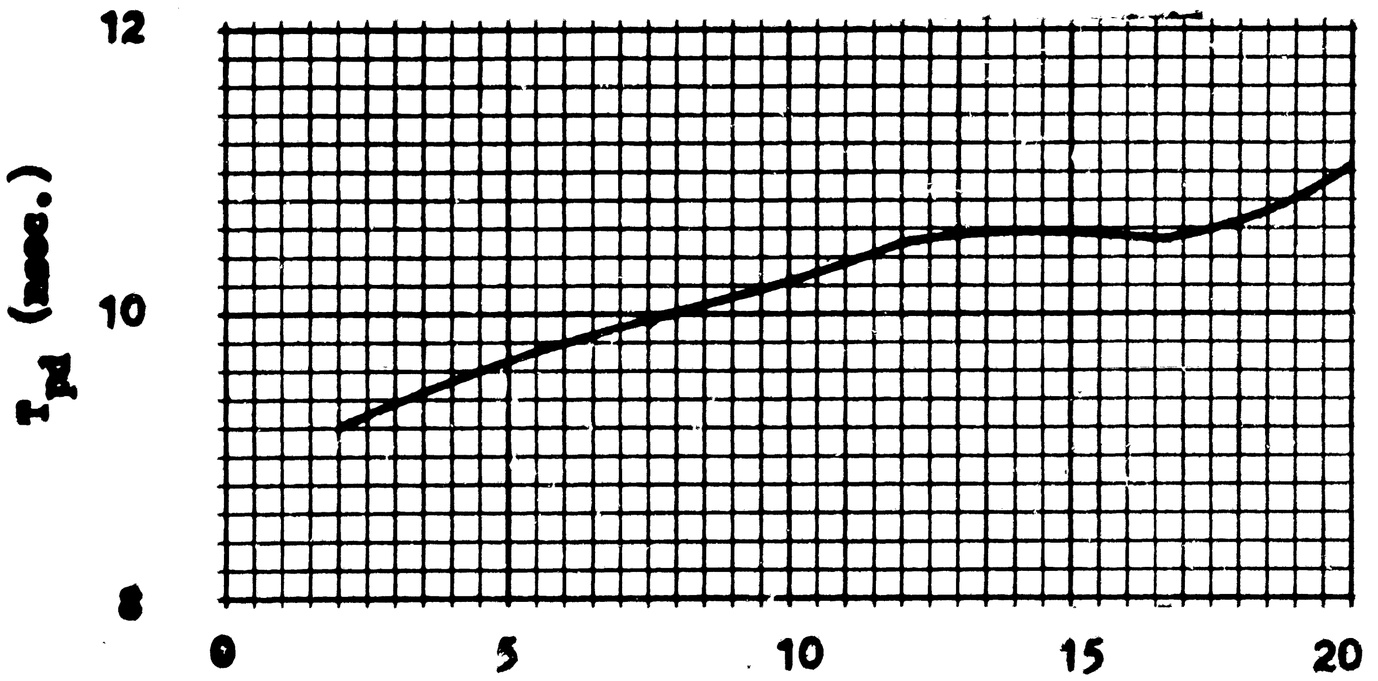
A. Load = 20
B. Load = 1

SNC-4B
Frequency = 1 mc.
V_{cc} = 5.0 volts

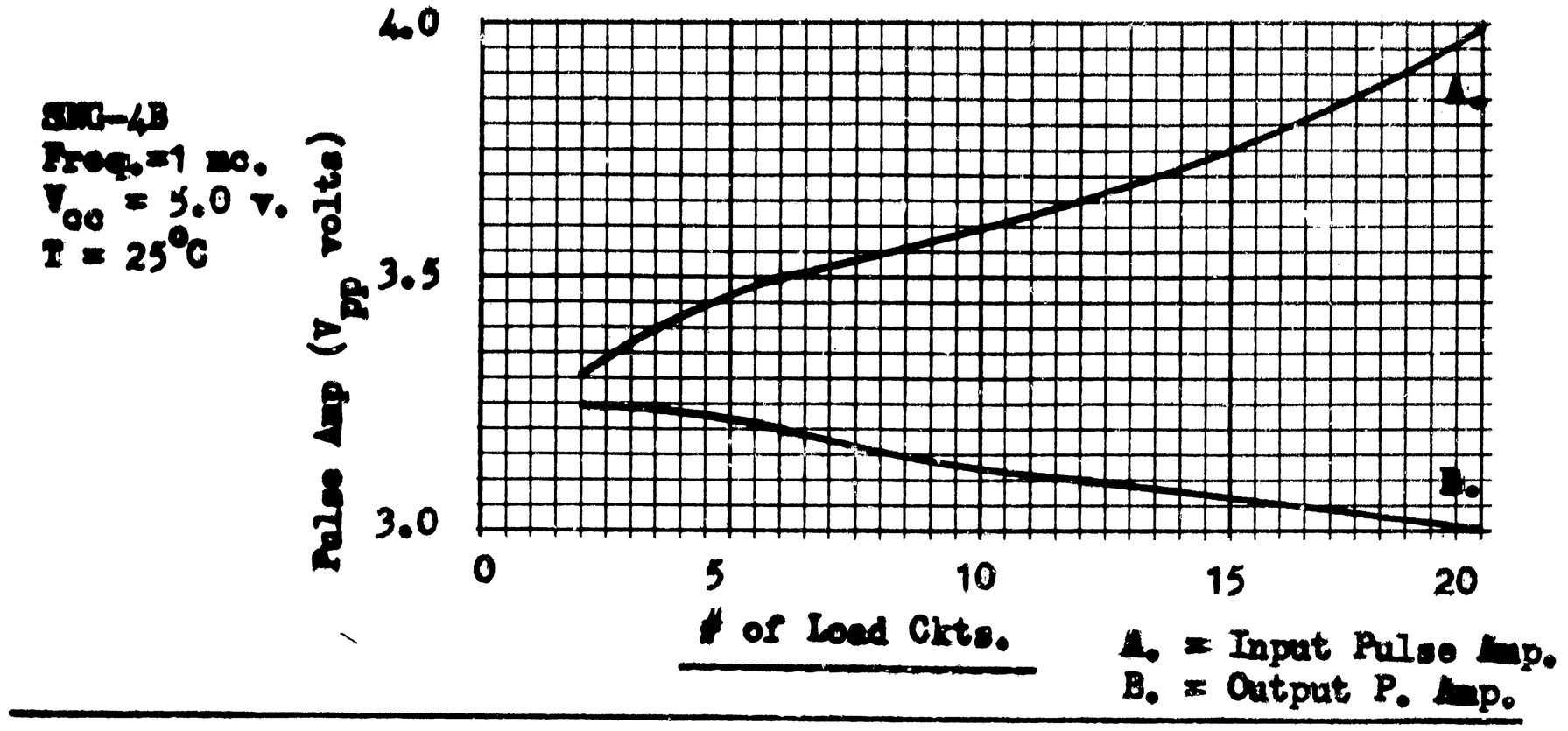


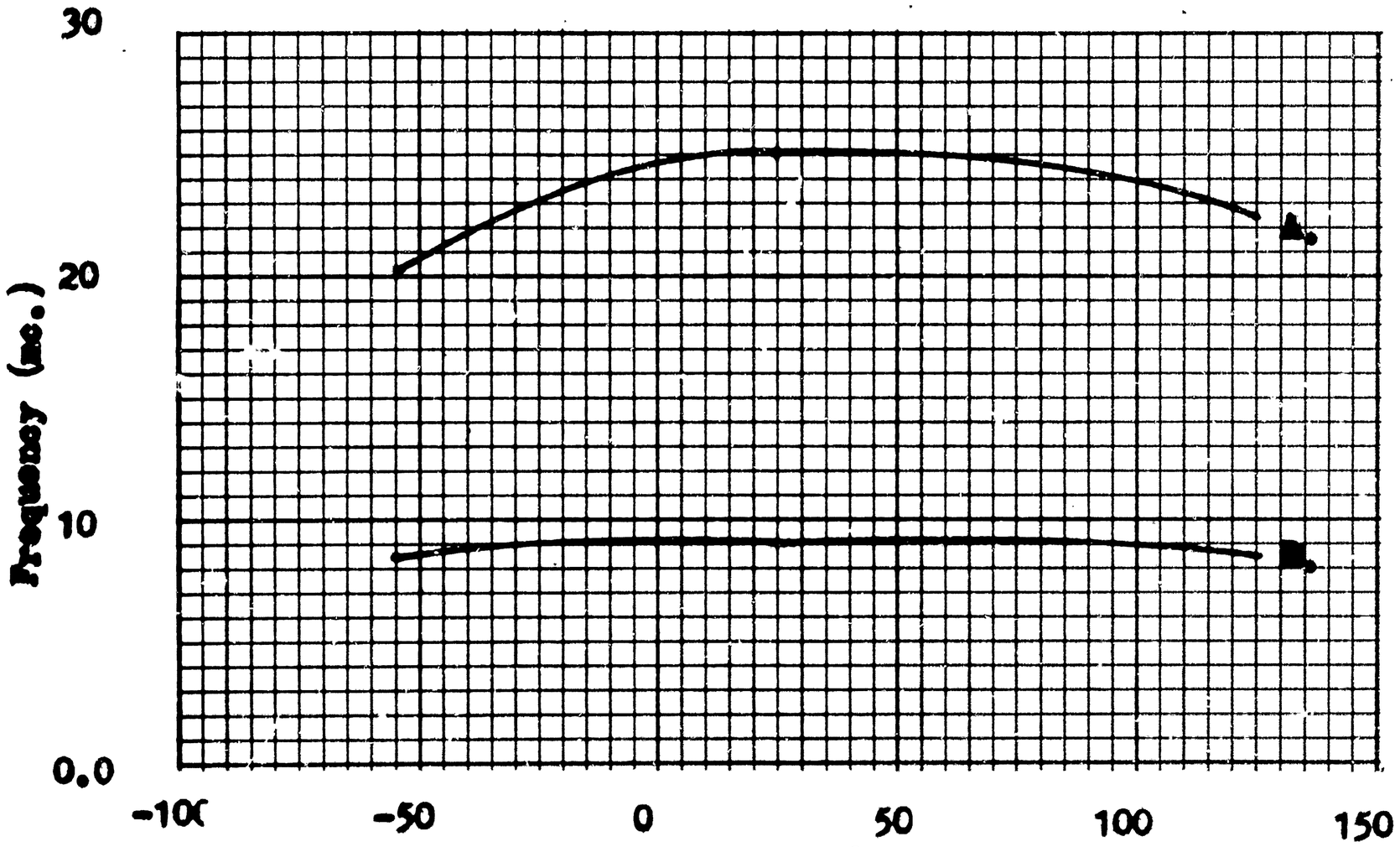
A. Load = 20
B. Load = 1

SNC-4B
Frequency = 6 mc.
V_{cc} = 5.0 volts



SNC-4B T = 25°C
Frequency = 1 mc.
V_{cc} = 5.0 volts

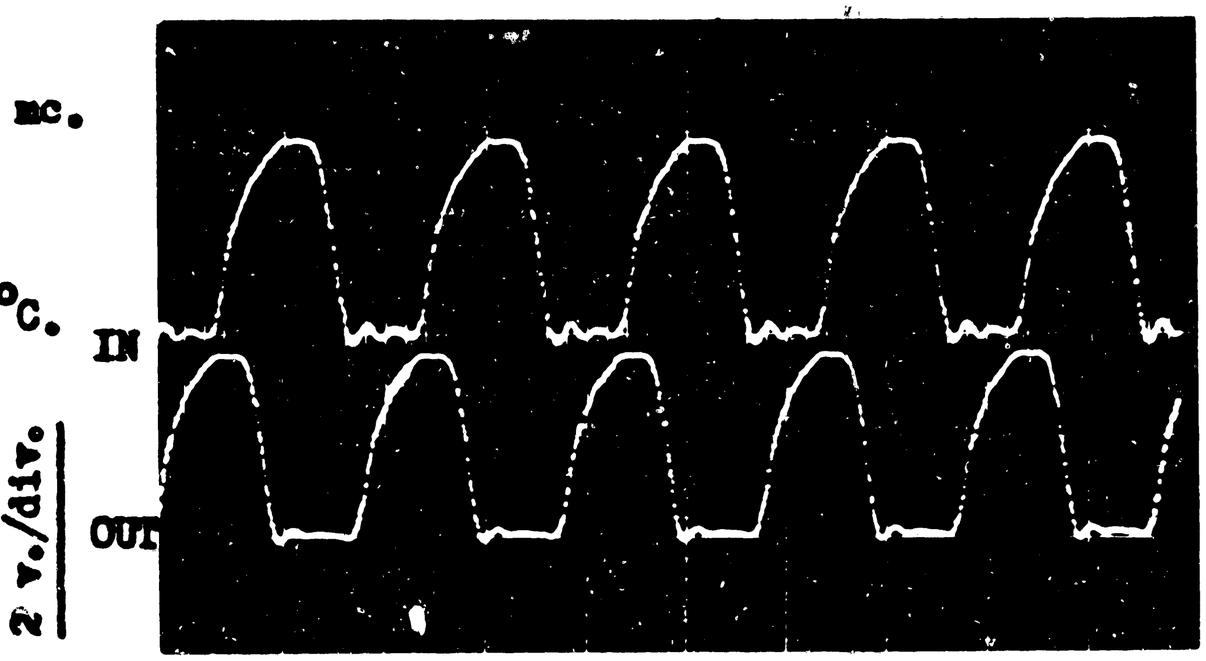




SMG-4B Ring Counter

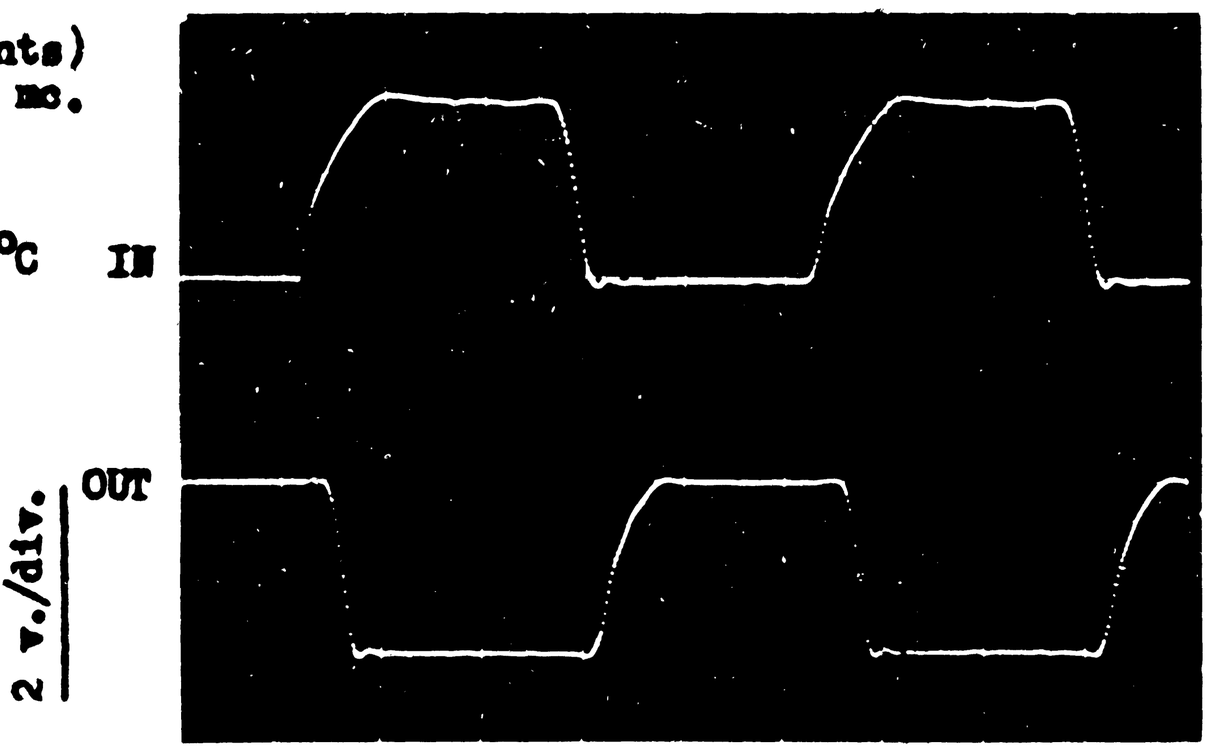
V_{cc} = 5.0 volts

Ring Counter
SNG-4B
Frequency = 24.2 mc.
(3 elements)
Load = 1 ckt.
V_{cc} = 5.0 v.
Temperature = 25°C.



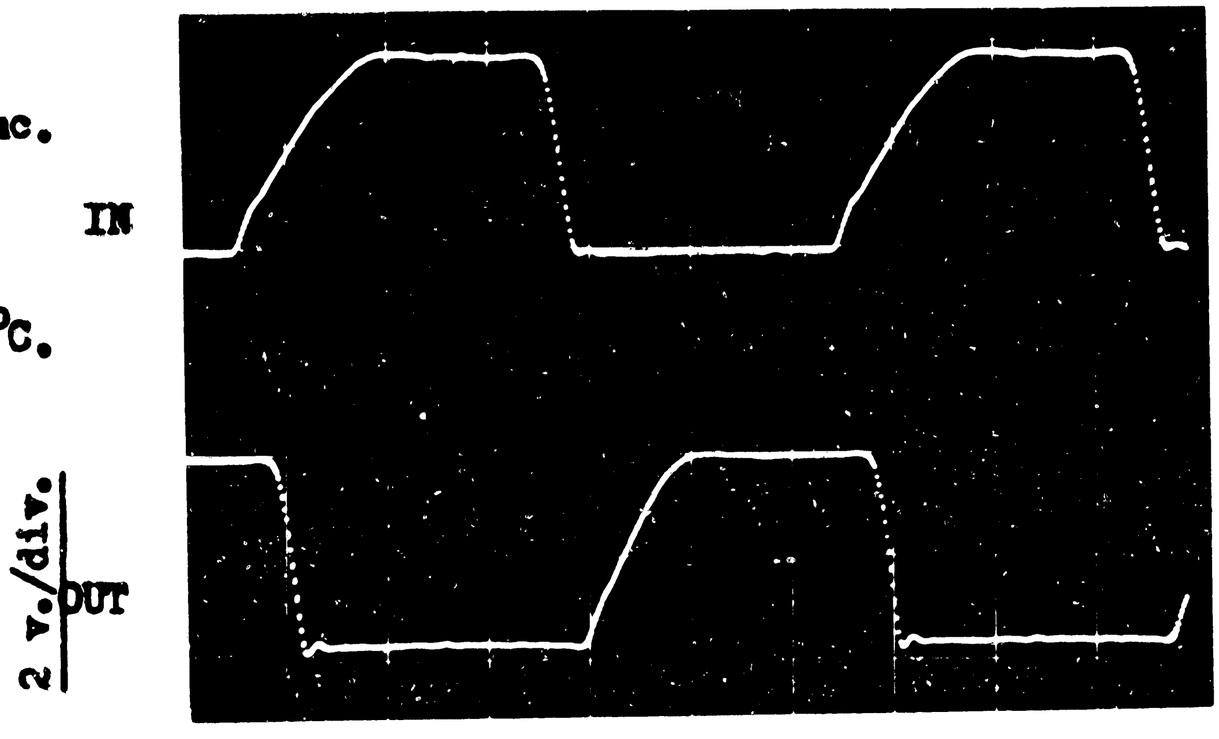
20 nsec./div.

Ring Counter
SNG-4B (7 elements)
Frequency = 9.58 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C



20 nsec./div.

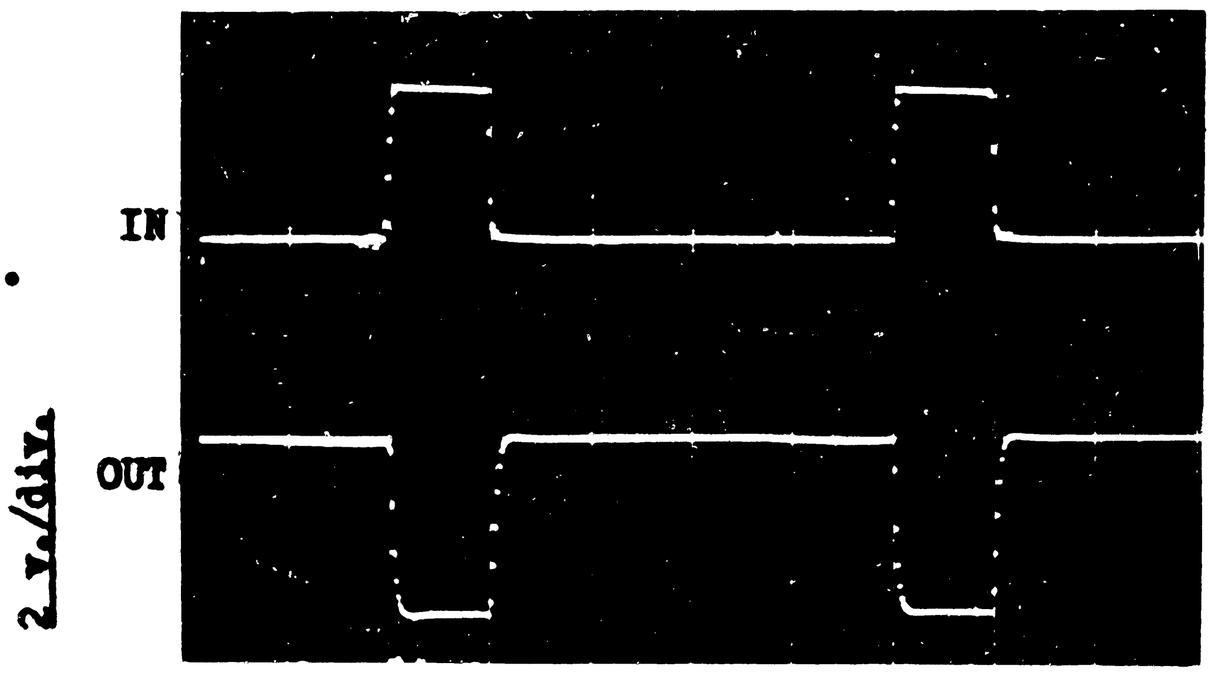
Ring Counter
SNG-4B
Frequency = 8.26 mc.
(7 elements)
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 125°C.



20 nsec./div.

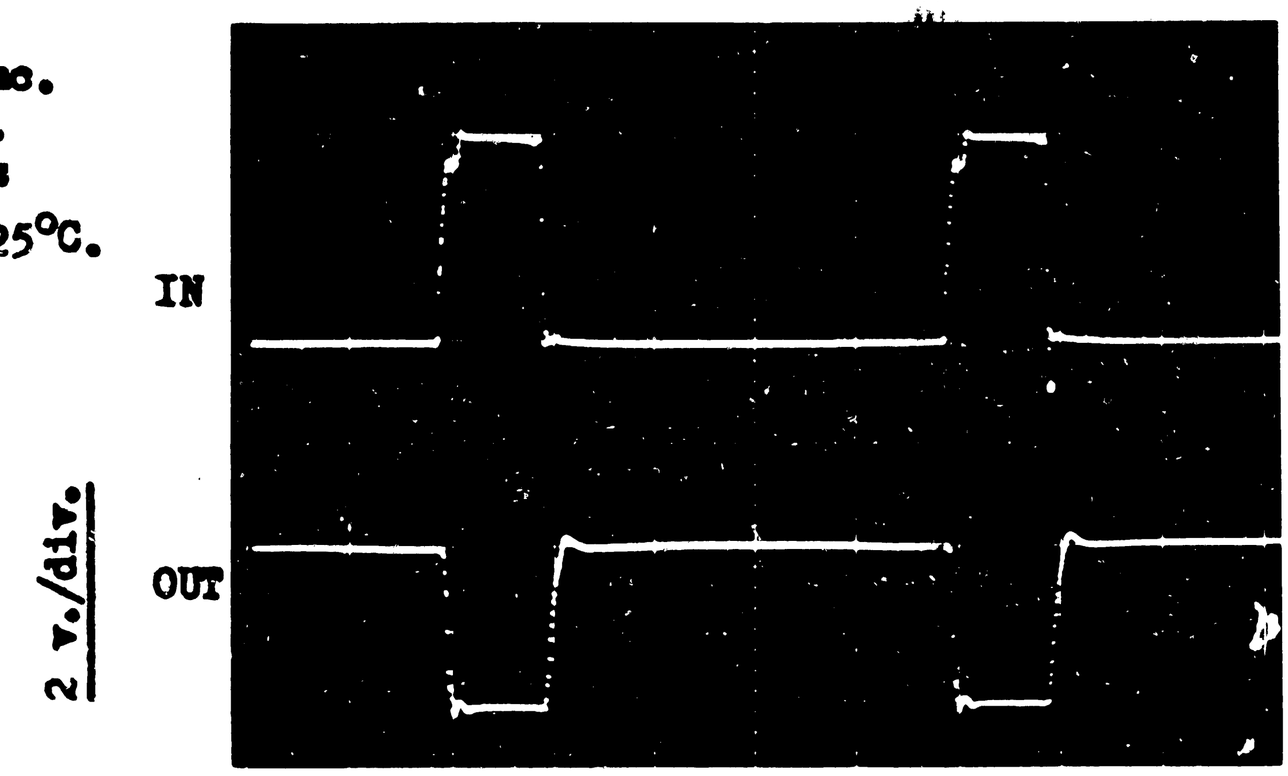
End of ring counter traces.

SNG-4B
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.



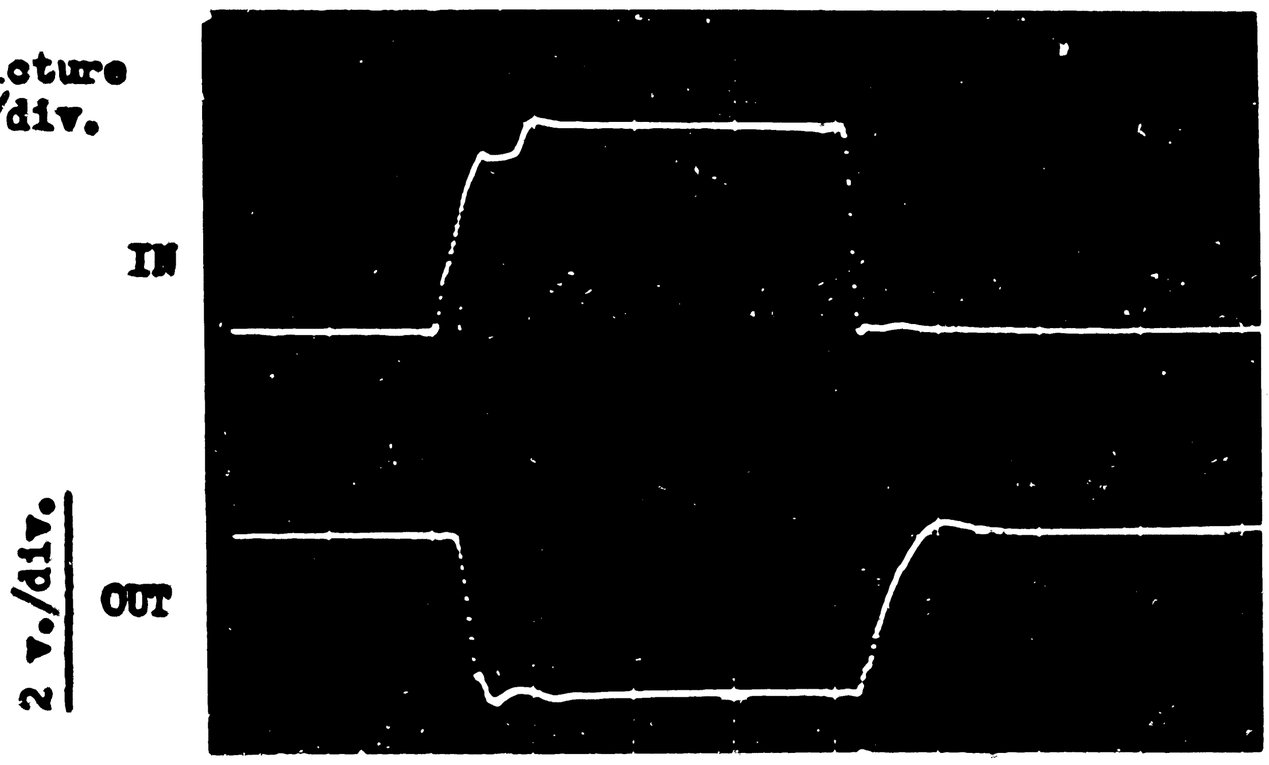
.2 msec./div.

SNG-4B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 25°C.



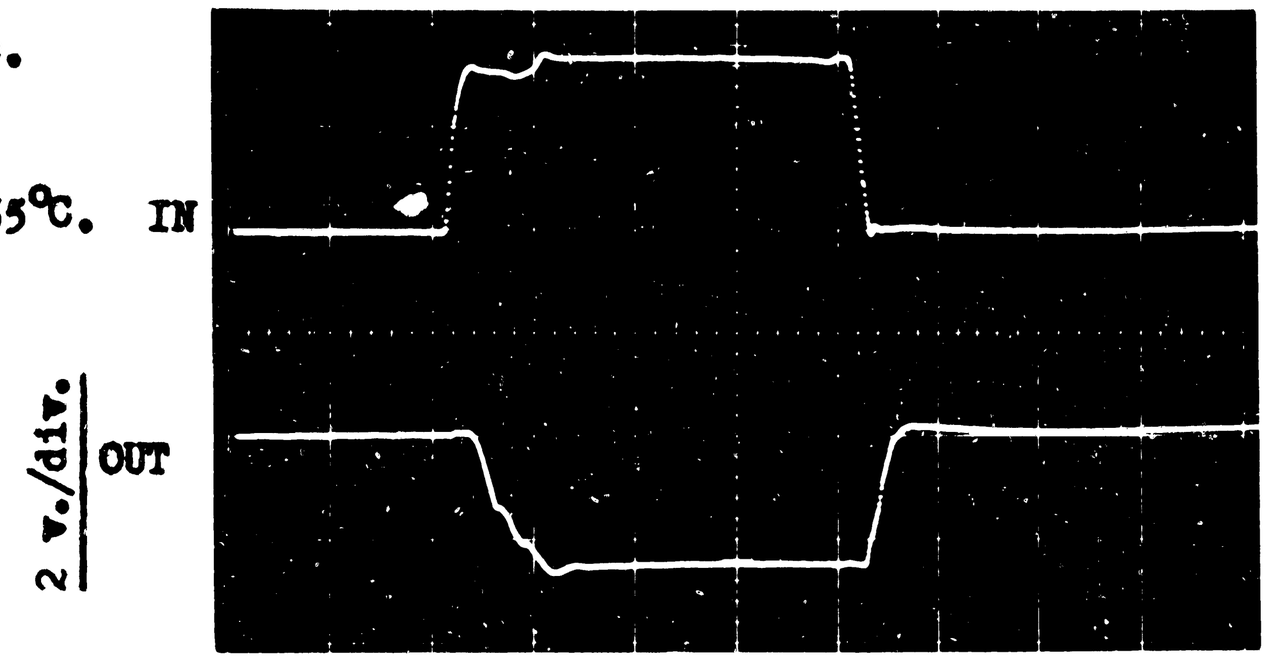
.2 μsec./div.

SNG-4B
Same as above picture except 50 nsec./div.



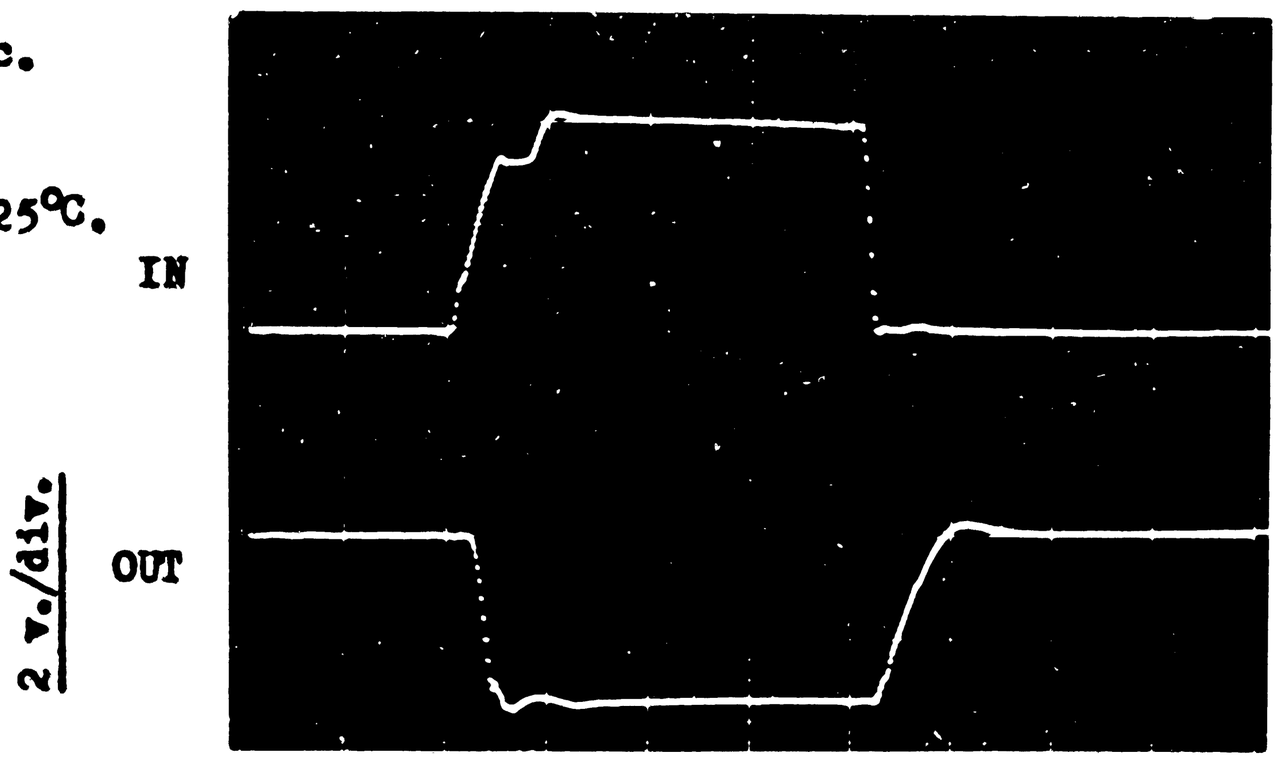
50 nsec./div.

SNG-4B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = -55°C.



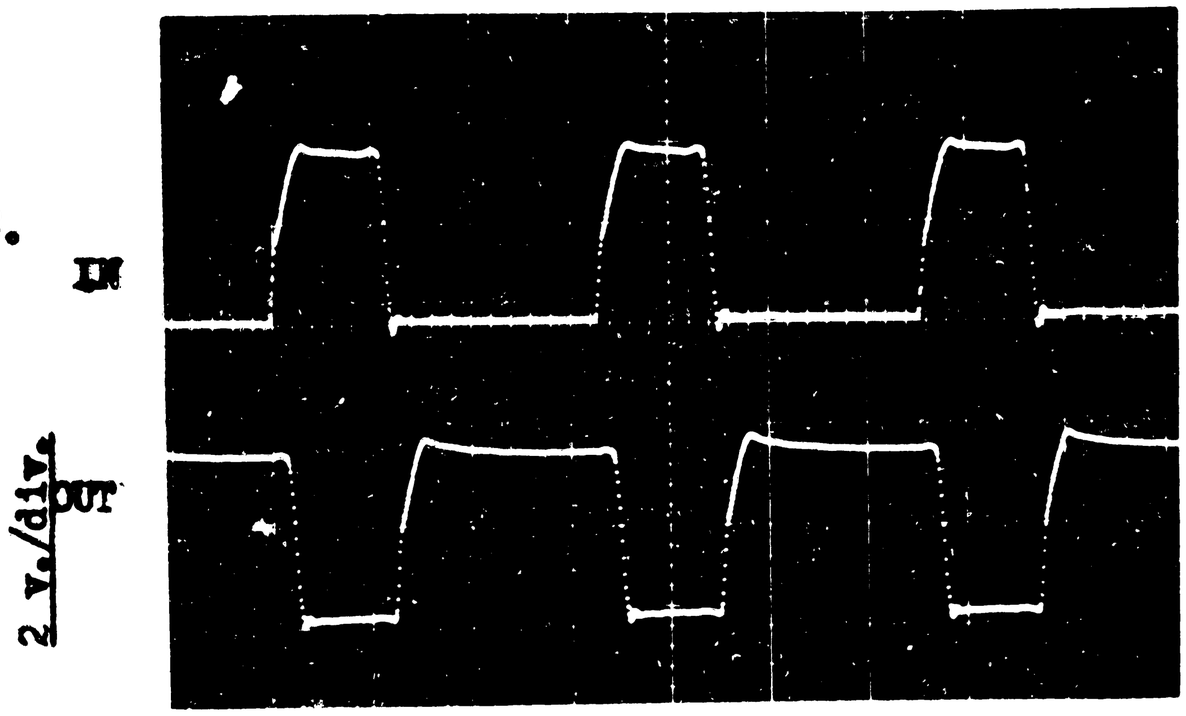
50 nsec./div.

SNG-4B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 125°C.



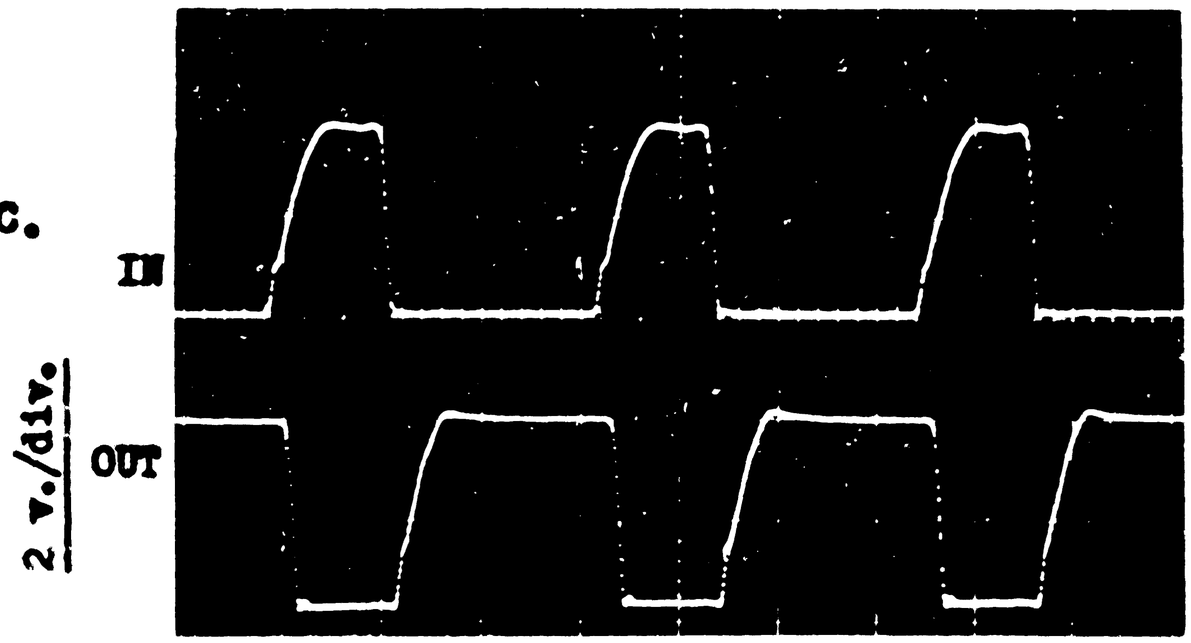
50 nsec./div.

SNG-4B
Frequency = 6 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.



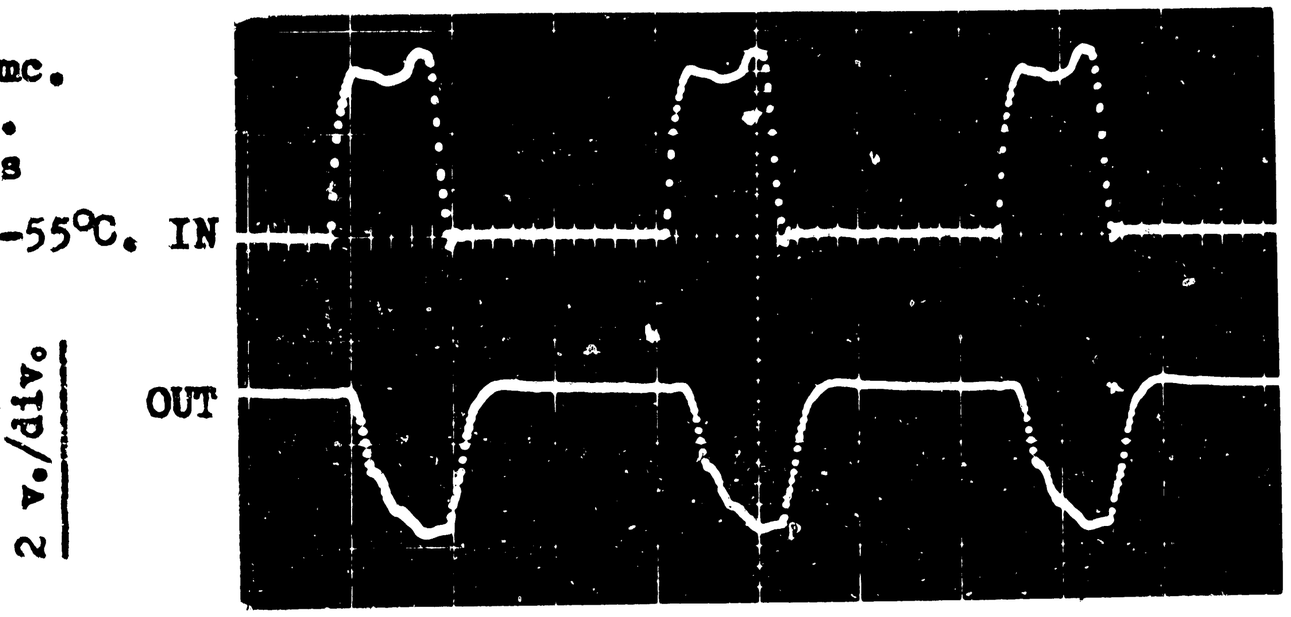
50 nsec./div.

SNG-4B
Frequency = 6 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 125°C.



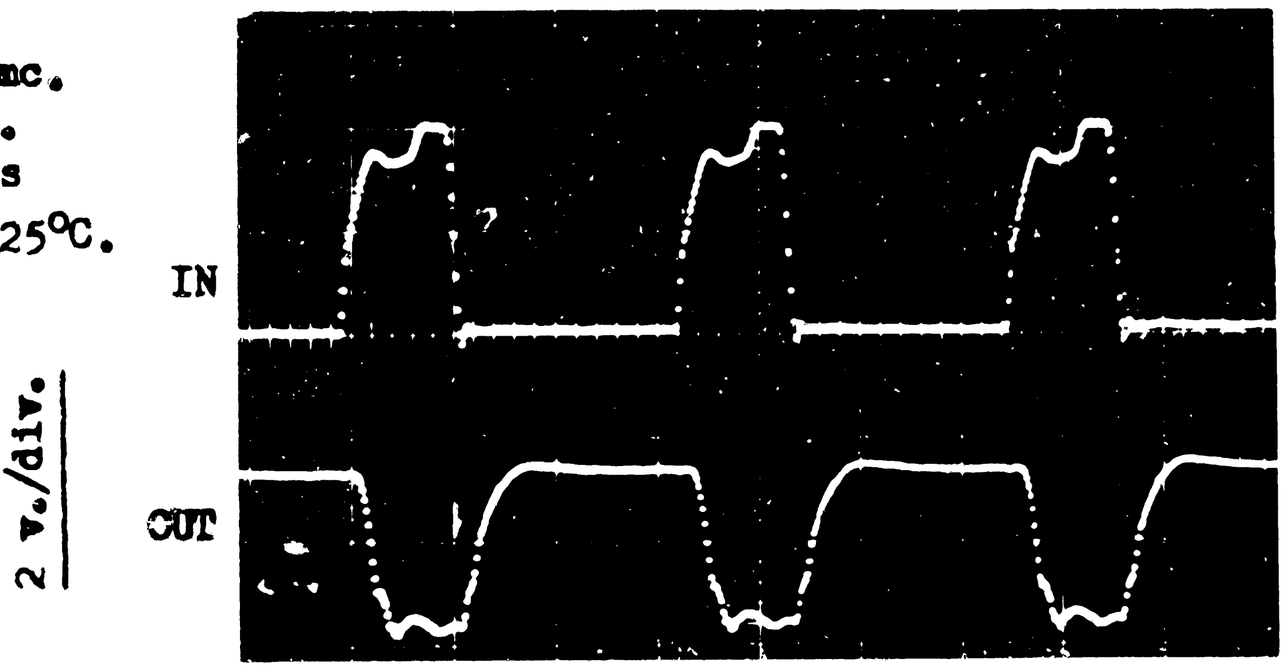
50 nsec./div.

SNG-4B
Frequency = 6 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = -55°C.



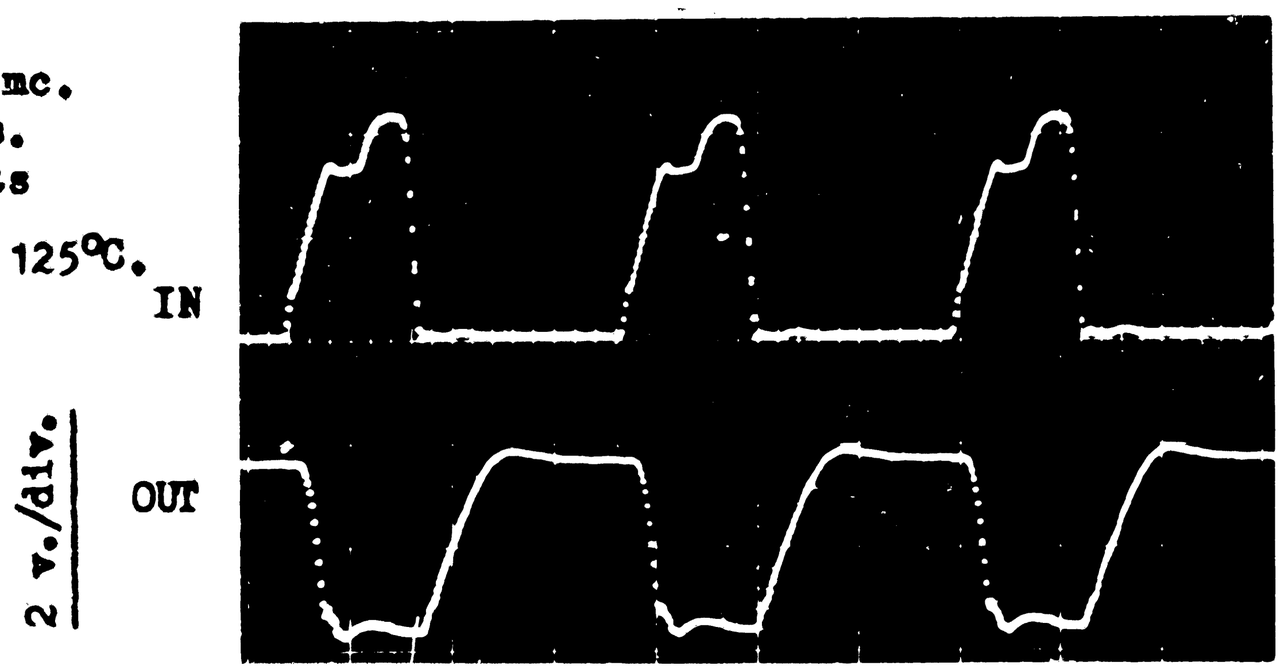
50 nsec./div.

SNG-4B
Frequency = 6 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 25°C.



50 nsec./div.

SNG-4B
Frequency = 6 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 125°C.



50 nsec./div.

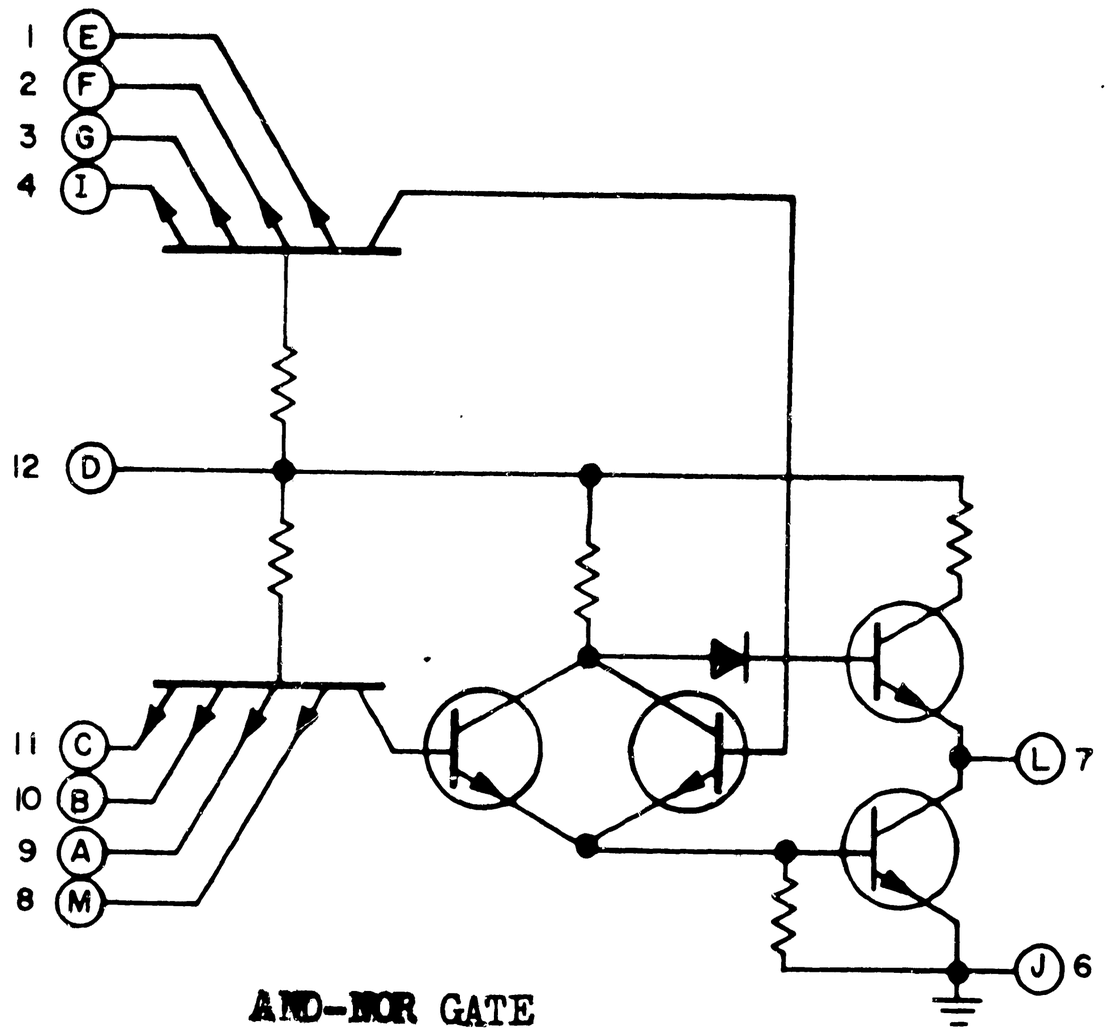
SNG 5A & B

(+) LOGIC

$$L = \overline{A \cdot B \cdot C \cdot M + E \cdot F \cdot G \cdot I}$$

(−) LOGIC

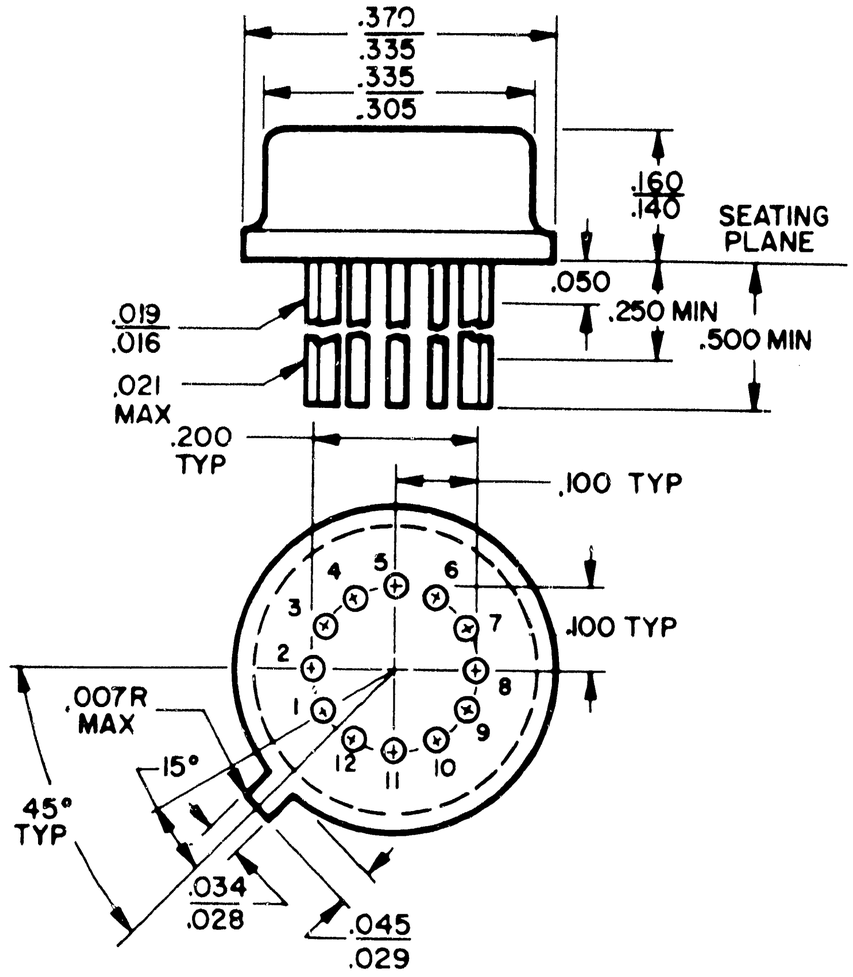
$$L = \overline{(A+B+C+M) \cdot (E+F+G+I)}$$



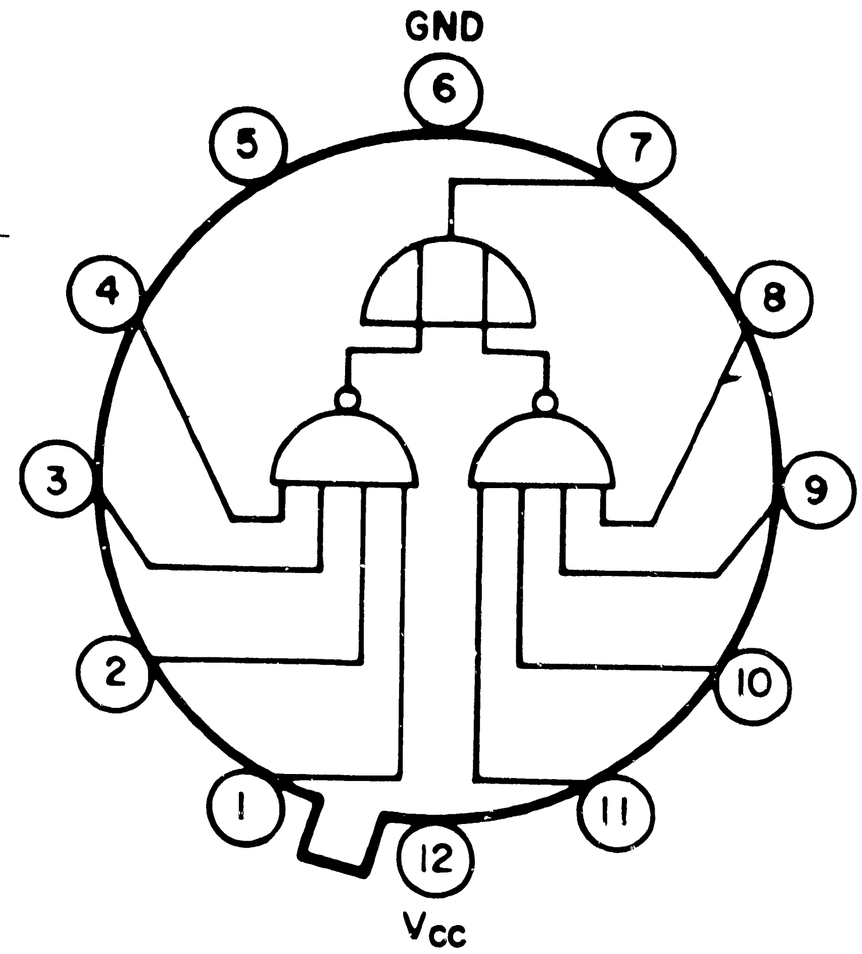
AND-NOR GATE

The SNG-5 AND-NOR gate functions as a AND-NOR element or as an EXCLUSIVE-OR element or one-half of a set-reset-trigger flip-flop. It is a monolithic, epitaxial, planar type and requires a single power supply.

The "A" version has three input points per input transistor, while the "B" version has four input points per input transistor. Both circuits have dual input transistors.



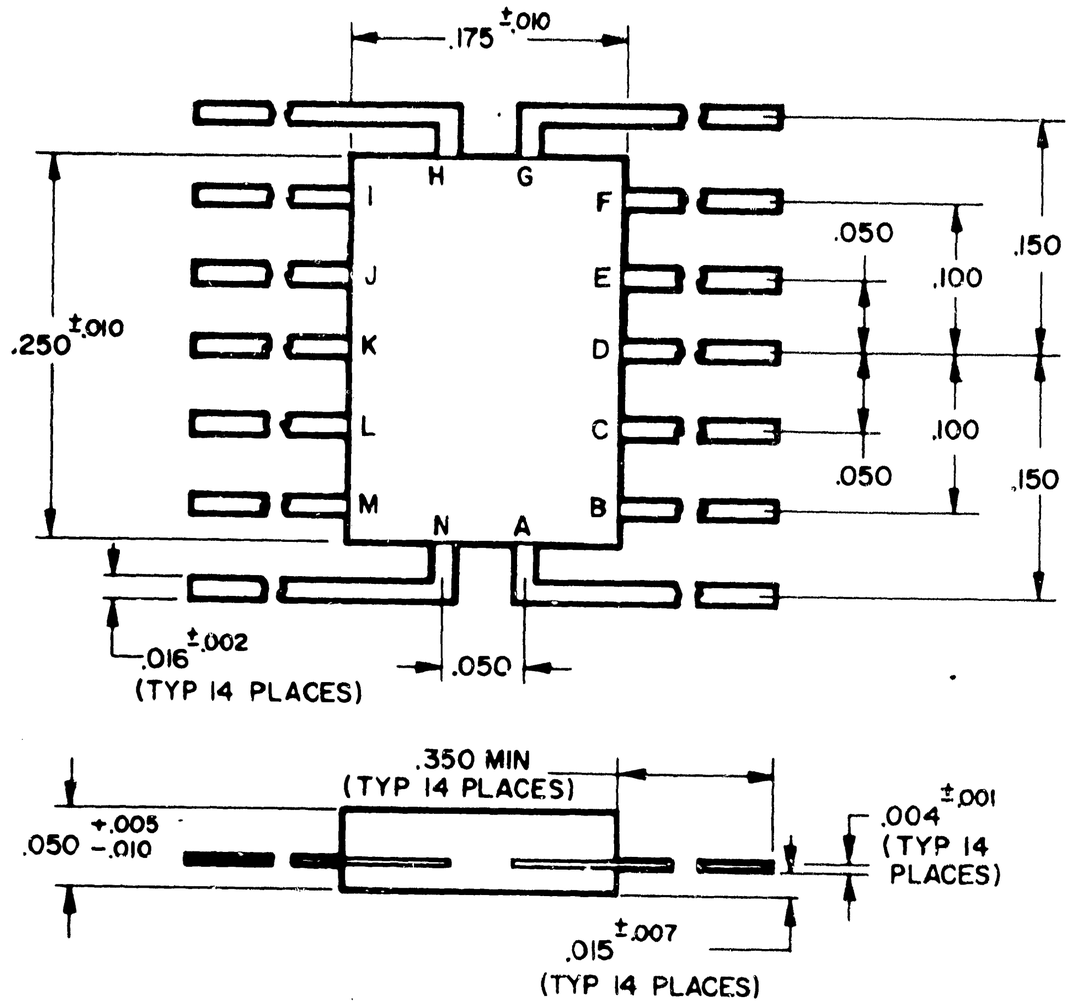
12 LEAD TO-5



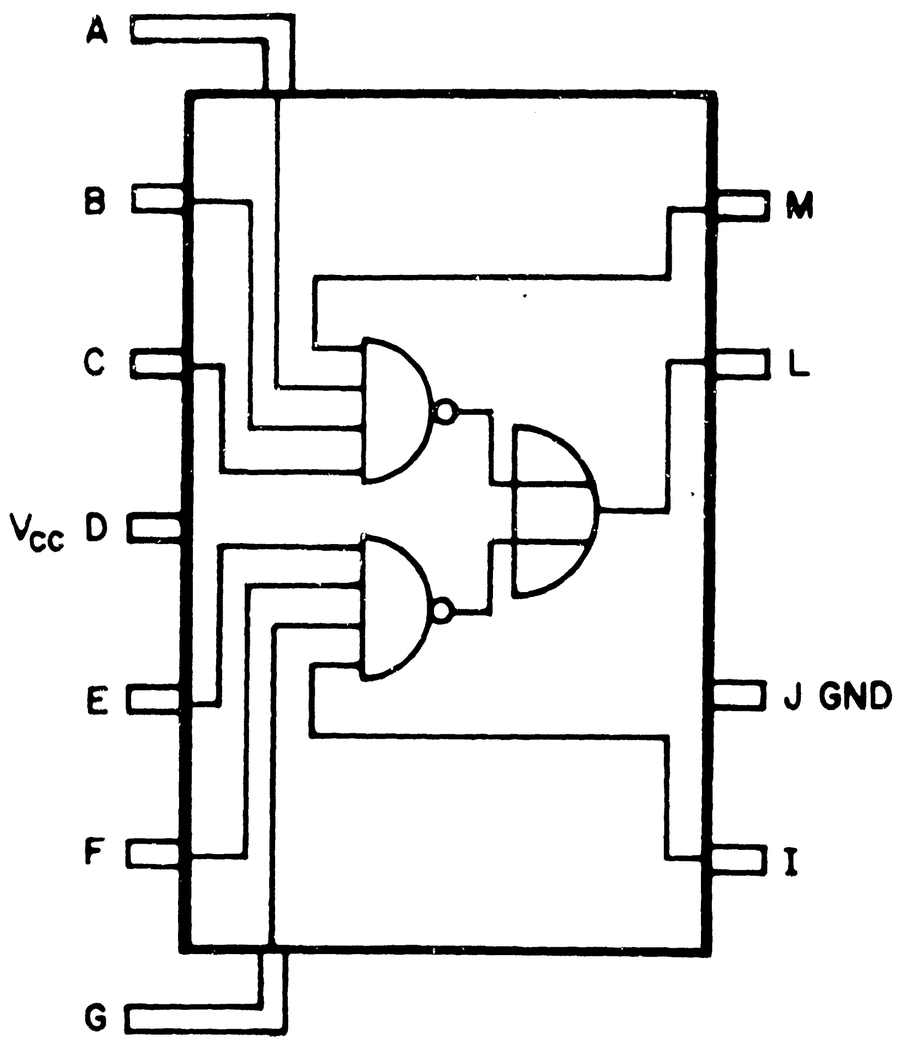
BOTTOM VIEW

SNG-5B

FOR SNG-5A INPUTS 9-A AND 3-G ARE NOT PRESENT



14 LEAD FLAT PACK

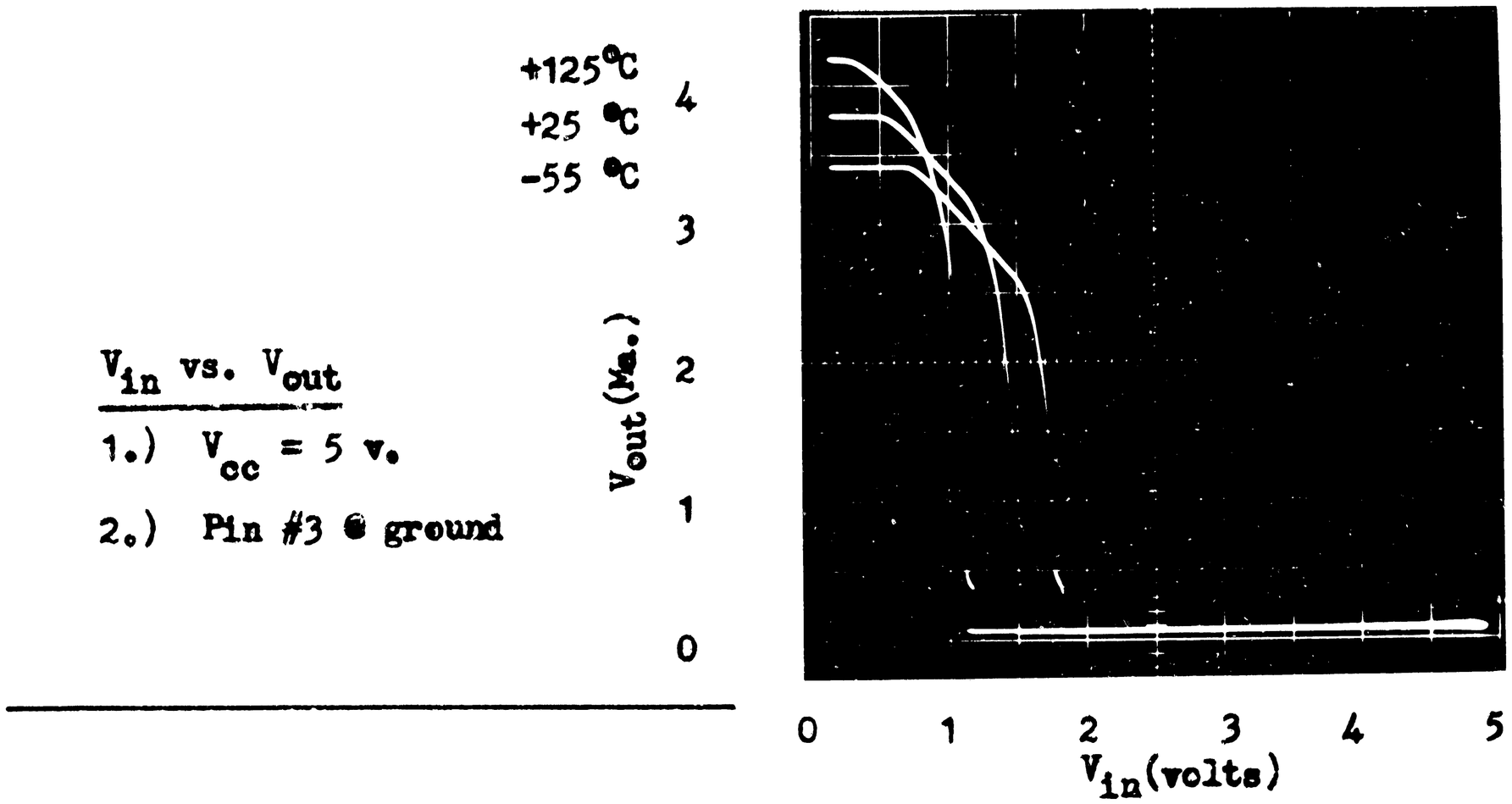


TOP VIEW

V_{in} vs. V_{out}

1.) V_{cc} = 5 v.

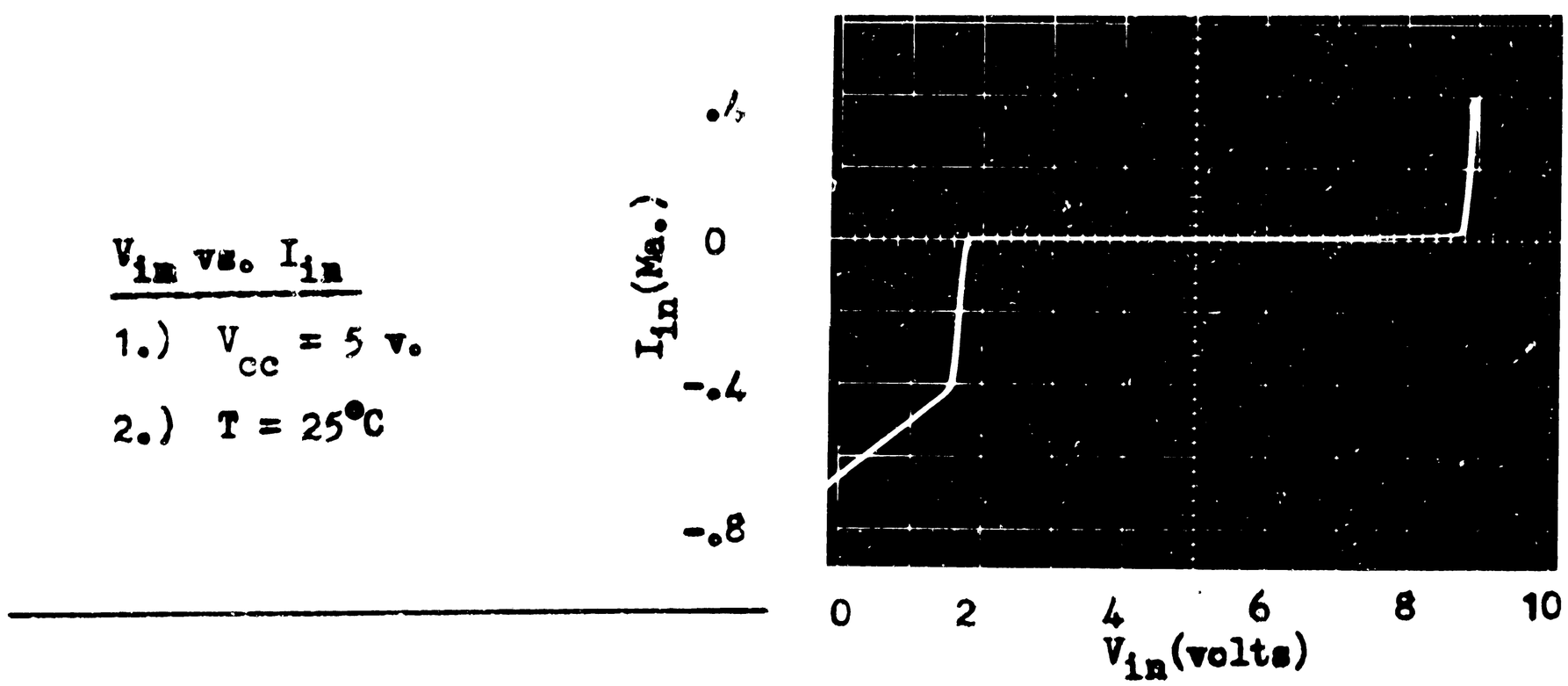
2.) Pin #3 @ ground



V_{in} vs. I_{in}

1.) V_{cc} = 5 v.

2.) T = 25°C

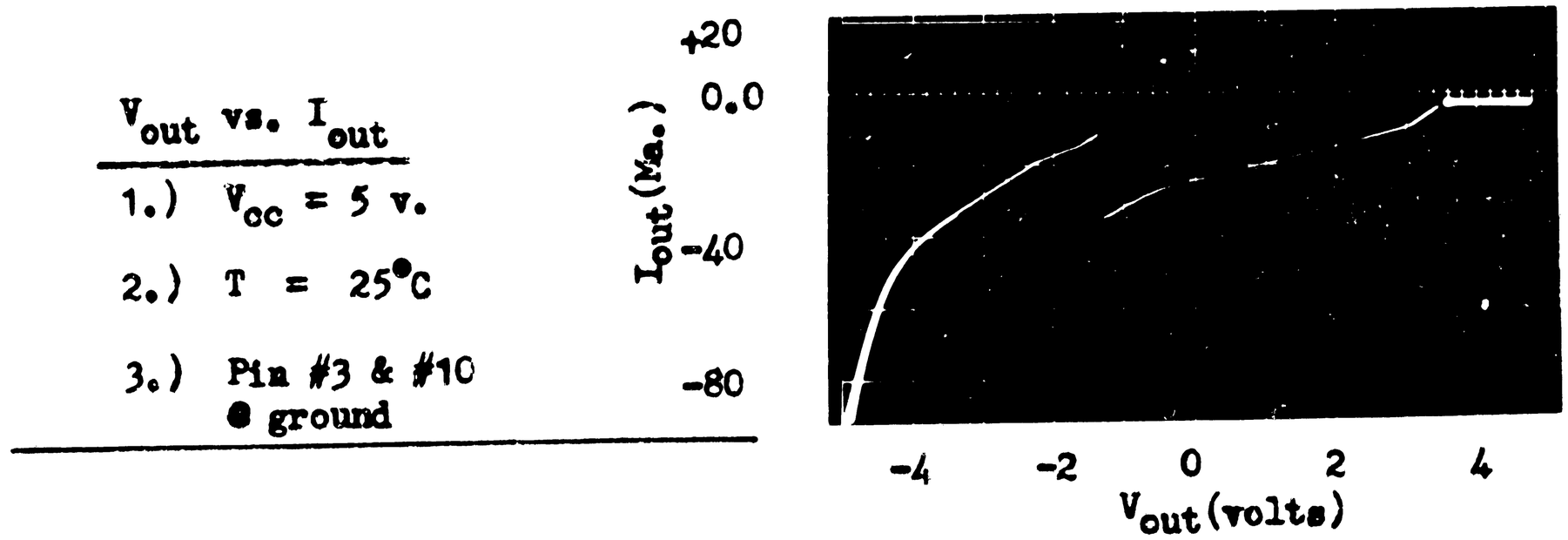


V_{out} vs. I_{out}

1.) V_{cc} = 5 v.

2.) T = 25°C

3.) Pin #3 & #10 @ ground

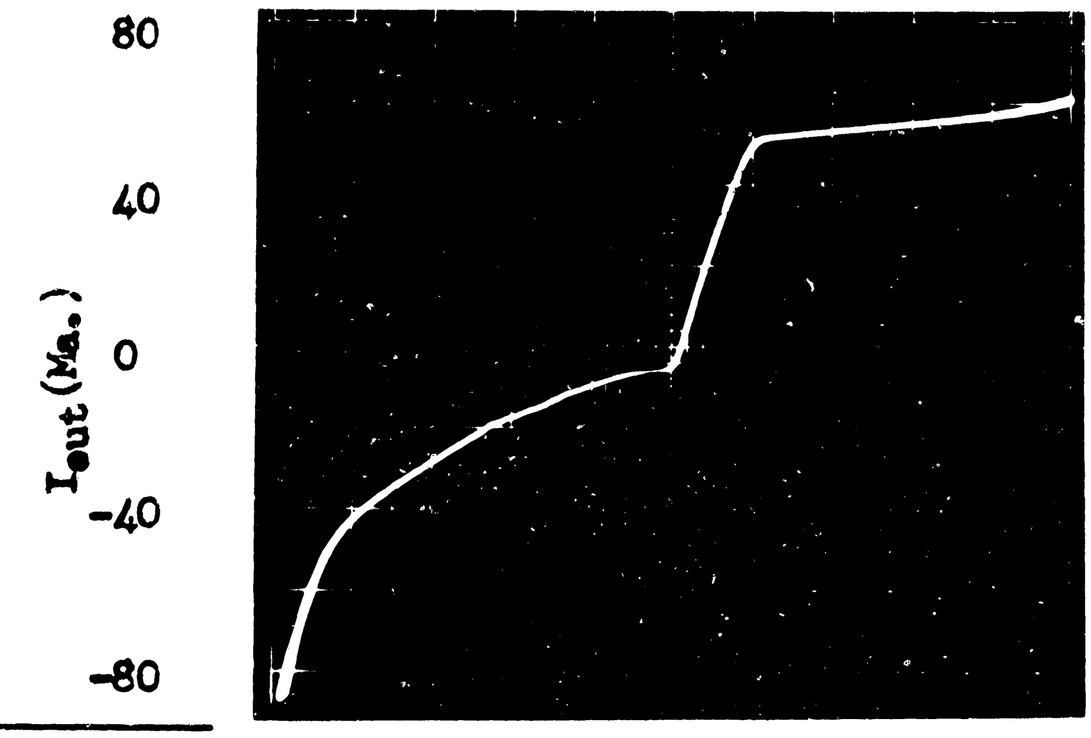


V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Pin #3 @ ground

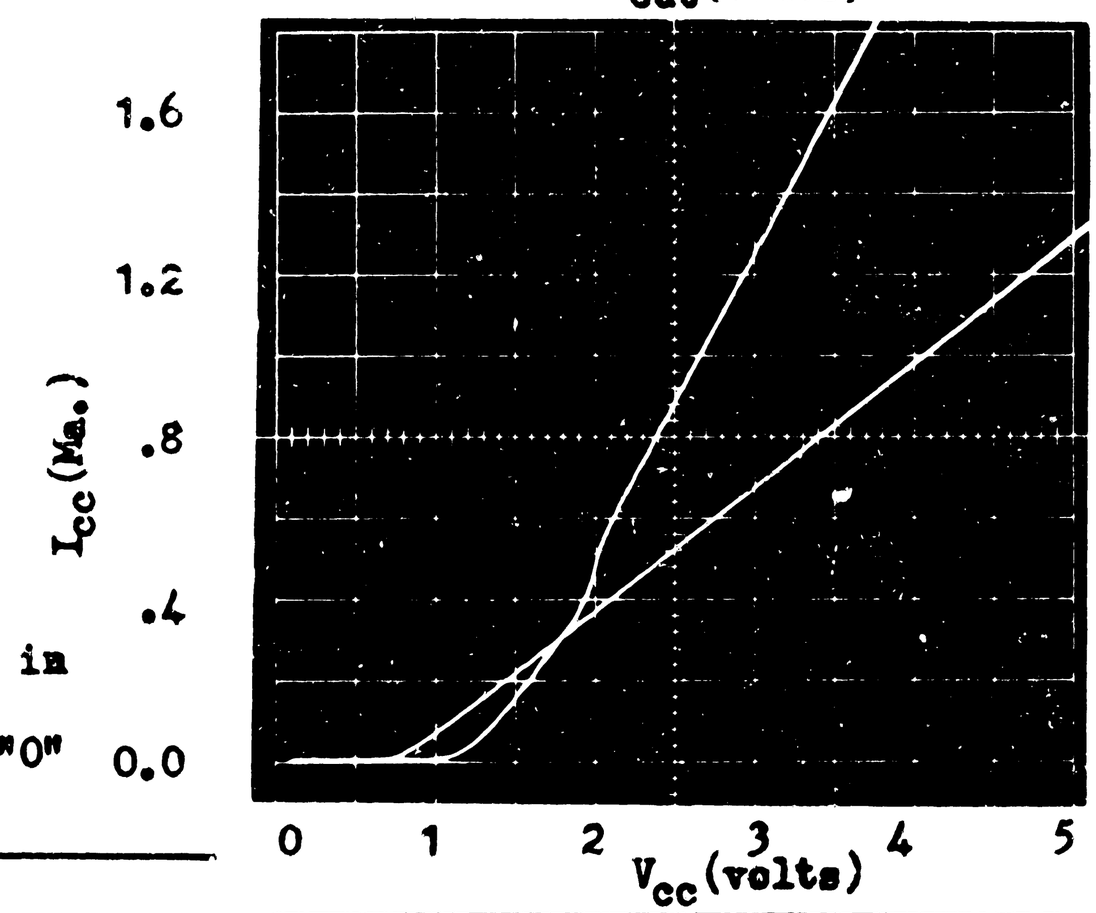


V_{cc} vs. I_{cc}

1.) T = 25°C

2.) Top trace with "1" in

3.) Bottom trace with "0" in.

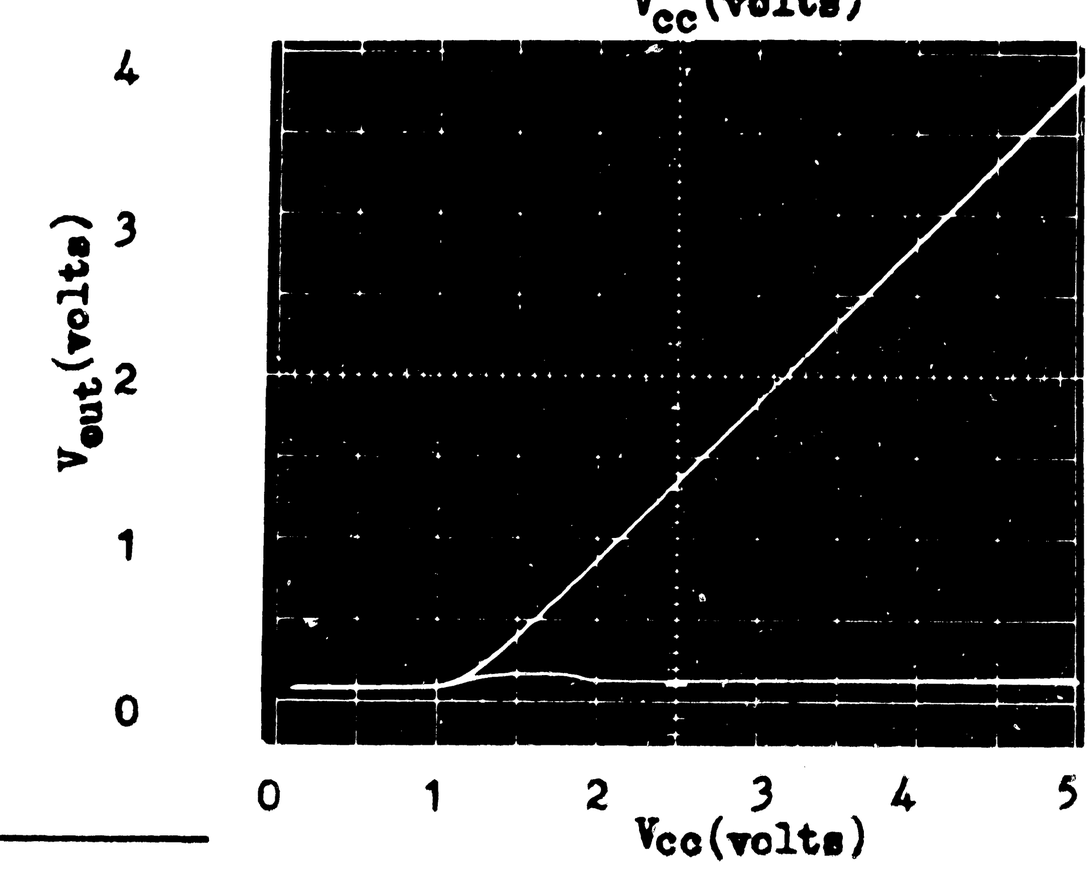


V_{cc} vs. V_{out}

1.) T = 25°C

2.) Top trace with "0" in

3.) Bottom trace with "1" in



Circuit SEC 5B	Supply Voltage 4.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	2.8	2.8	2.9	2.5	2.8	2.8	2.9	2.6	2.9	3.0	3.4	2.9
Pulse Width (ns.)	200	192	200	186	200	195	200	191	200	200	200	200
T_r (ns.)	5.0	15	6.0	28	5.0	14	6.0	25	6.0	14	9.0	21
T_f (ns.)	8.0	11	8.0	34	7.0	10	7.0	31	5.0	9.0	5.0	16
T_d (ns.)		18		19		16		17		12		13
T_s (ns.)		10		9.0		10		9.0		10		9.0
T_{pd} (ns.)		16		21		15		19		13		16

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.1	3.5	3.6	3.1	3.2	3.8	3.6	3.2
Pulse Width (ns.)	200	206	200	207	200	212	200	212
T_r (ns.)	10	17	13	21	13	20	17	25
T_f (ns.)	4.5	8.0	5.0	13	5.0	8.0	6.0	13
T_d (ns.)		11		11		10		11
T_s (ns.)		11		11		12		14
T_{pd} (ns.)		13		15		14		16

Circuit SNC 5B Supply Voltage 5.0 Frequency = 1 mc. Fan-in 1

Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.2	3.4	3.0	3.2	3.3	3.6	3.0	3.4	3.6	3.9	3.3
Pulse Width (ns.)	200	197	200	195	200	199	200	198	200	203	200	204
T_r (ns.)	5.0	14	7.0	28	5.0	13	7.0	26	7.5	13.5	11	21
T_f (ns.)	7.0	10	7.0	33	6.0	9.0	6.0	29	4.5	7.0	4.0	14
T_d (ns.)		13		15		12		14		10		11
T_s (ns.)		10		10		10		9.0		9.5		9.0
T_{pd} (ns.)		14		18		13		17		12		14.5

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.6	4.1	4.2	3.6	3.7	4.3	4.2	3.7
Pulse Width (ns.)	200	210	200	210	200	214	200	216
T_r (ns.)	11	17	16	22	15	20	19	26
T_f (ns.)	4.0	7.0	5.0	12	4.0	7.0	6.0	12
T_d (ns.)		10		10		9.0		10
T_s (ns.)		11		12		13		15
T_{pd} (ns.)		12.5		14		12.5		15

Circuit SNC 5B	Supply Voltage 5.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.6	3.7	4.0	3.4	3.7	3.8	4.2	3.5	3.8	4.1	4.4	3.7
Pulse Width (ns.)	200	201	200	199	200	204	200	201	200	205	200	206
T_r (ns.)	6.0	14	7.0	27	6.0	13	9.0	25	8.0	14	12	21
T_f (ns.)	6.0	9.0	6.0	32	5.0	8.0	5.0	27	4.0	7.0	5.0	13
T_d (ns.)		12		13		10		12		9.0		10
T_s (ns.)		10		9.0		10		8.0		10		9.0
T_{pd} (ns.)		13		17		12		16		11		14
Temperature:	+85°C				+125°C							
Load	1	1	20	20	1	1	20	20				
Test Circuit	input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})	4.1	4.6	4.7	4.0	4.2	4.8	4.6	4.1				
Pulse Width (ns.)	200	211	200	212	200	217	200	219				
T_r (ns.)	13	17	17	23	16	21	19	27				
T_f (ns.)	5.0	7.0	5.0	12	4.0	7.0	6.0	12				
T_d (ns.)		9.0		9.0		9.0		9.0				
T_s (ns.)		11		13		13		15				
T_{pd} (ns.)		12		14		13		15				

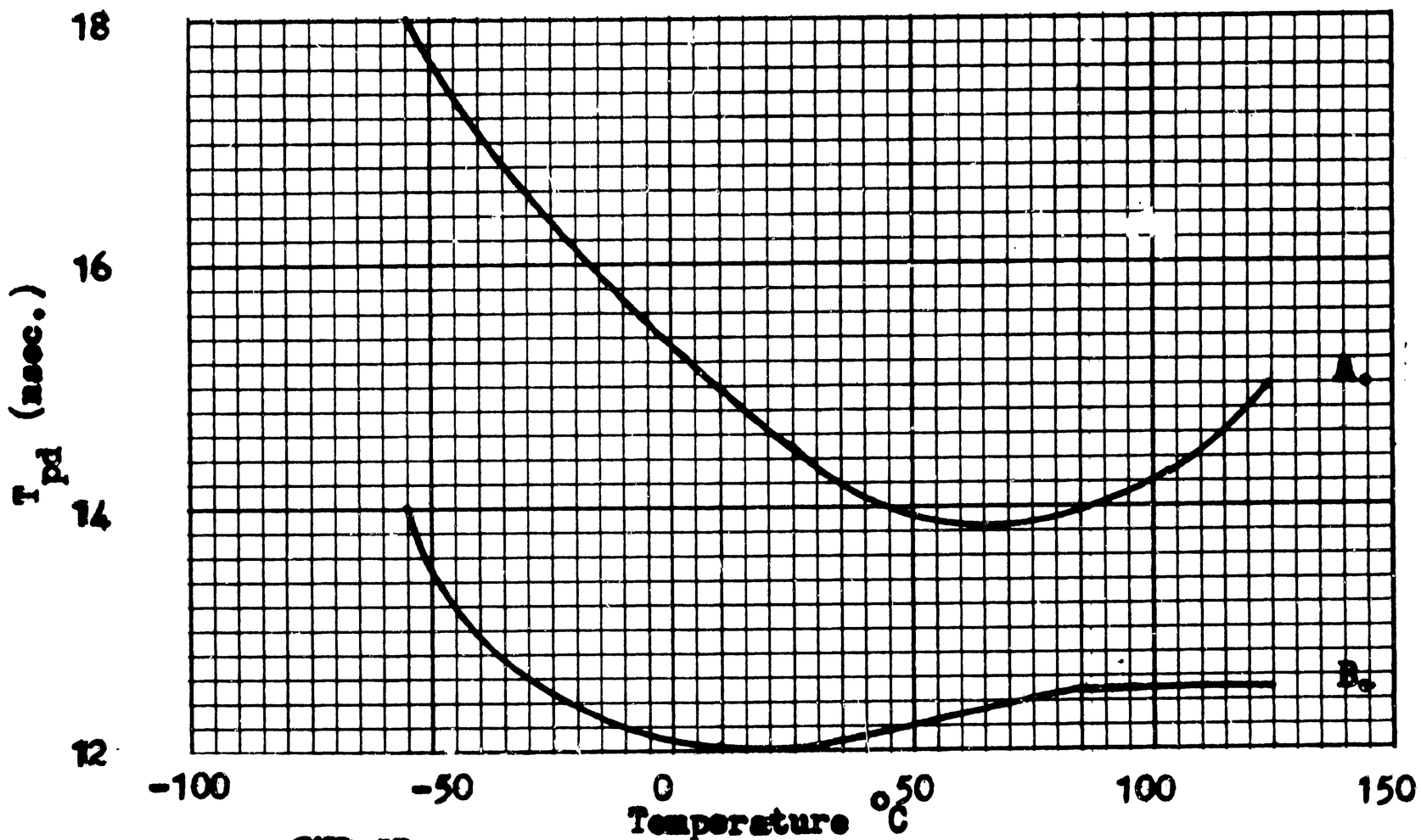
Circuit SNG 5	Supply Voltage 5.0					Frequency = 6 mc.	Fan-in 1					
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.3	3.3	3.6	3.1	3.3	3.4	3.8	3.1	3.5	3.8	4.2	3.4
Pulse Width (ns.)	50	49	50	47	50	50	50	49	50	54	50	55
T_r (ns.)	5.0	14	7.0	29	5.0	13	8.0	27	8.0	15	37	23
T_f (ns.)	5.0	9.0	6.0	34	5.0	8.0	5.0	30	4.0	7.0	5.0	13
T_d (ns.)		12		13		11		12		10		10
T_s (ns.)		9.0		8.0		9.0		47		9.0		10
T_{pd} (ns.)		13		16		12		16		11		14

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.7	4.4	4.5	4.0	3.7	4.6	4.5	4.1
Pulse Width (ns.)	50	60	50	61	50	65	50	68
T_r (ns.)	11	19	39	27	15	23	40	31
T_f (ns.)	4.0	7.0	4.0	14	4.0	7.0	4.0	13
T_d (ns.)		9.0		10		9.0		9.0
T_s (ns.)		11		11		13		13
T_{pd} (ns.)		12		15		13		16

SMG 5B V_{cc} = 5.0 v. Frequency = 1 mc. Input P.Width = 200 nsec.

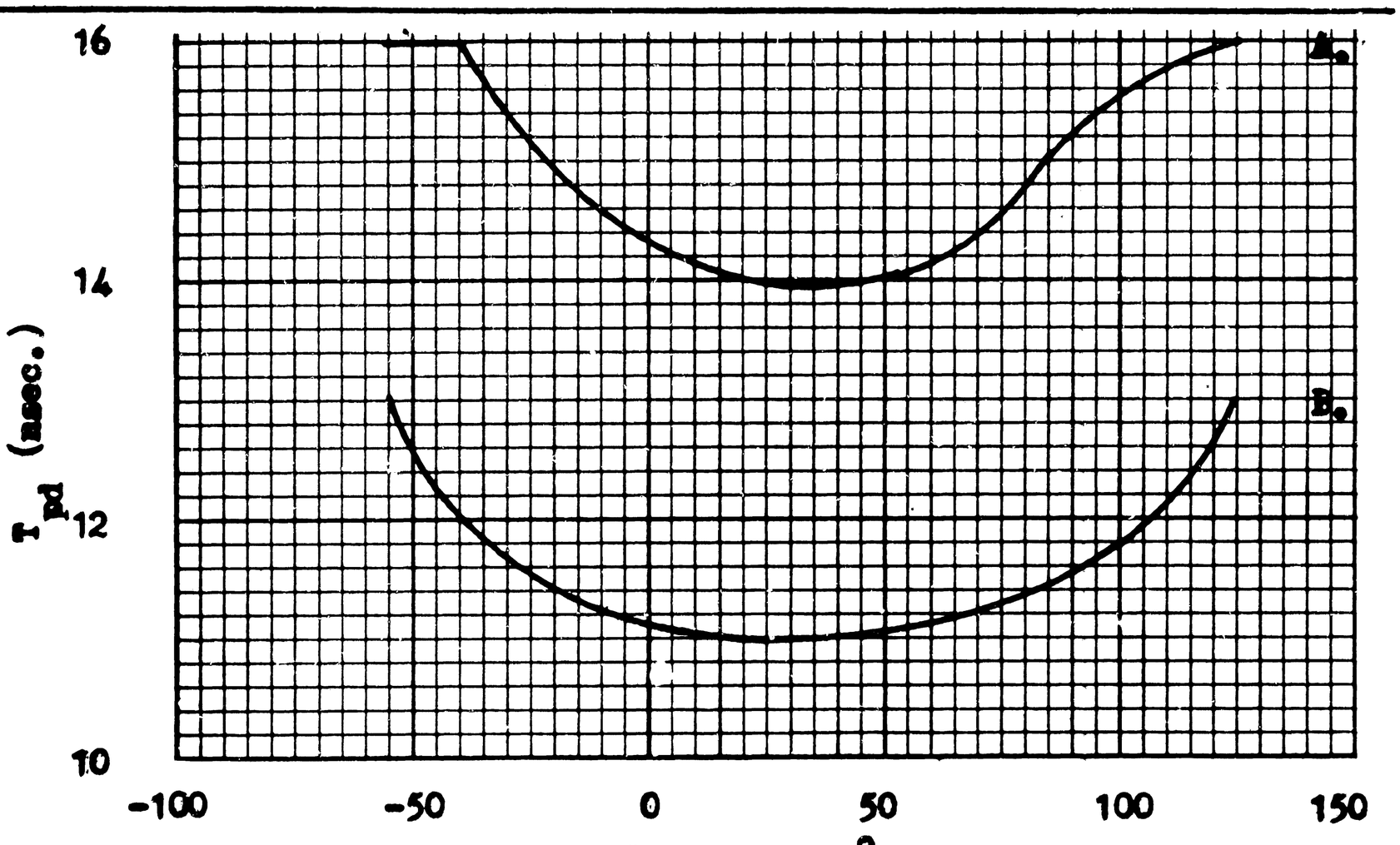
Load ckts.	20	18	16	14	12	10	8	6	4	2
T_{pd}	14.5	14.5	14.0	14.0	14.0	14.0	13.5	13.5	13.1	13.0
T_r Output	21.0	20.5	19.8	18.5	17.6	17.3	16.4	15.9	15.2	15.0
T_f Output	14.0	13.4	12.5	11.8	11.4	10.5	10.0	9.6	8.8	8.5
Pulse Amp. (Input)	3.82	3.76	3.72	3.60	3.56	3.52	3.44	3.36	3.31	3.24
Pulse Amp. (Output)	3.28	3.32	3.32	3.34	3.36	3.40	3.41	3.44	3.50	3.54

Temperature = 25°C.



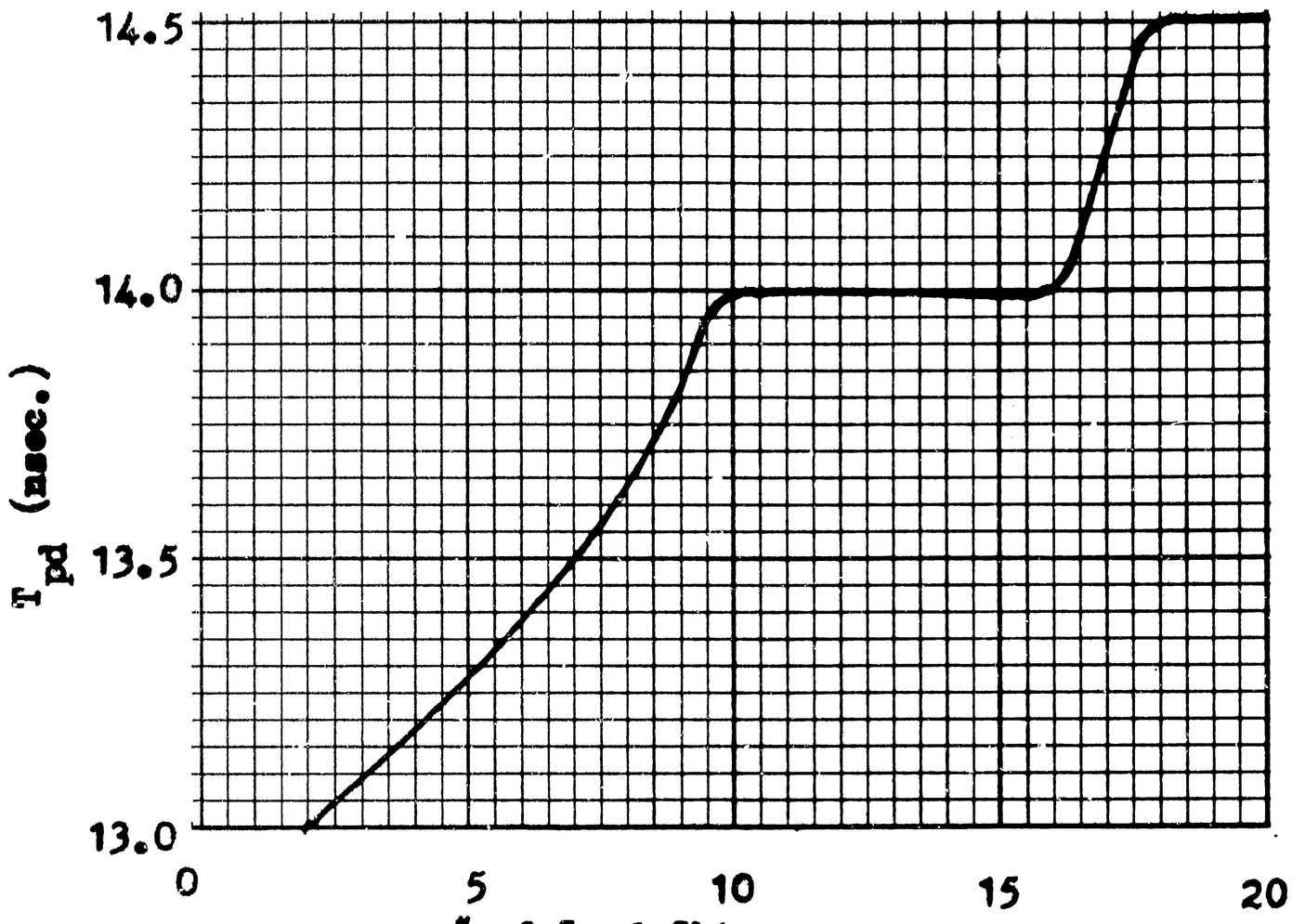
SNG-5B
Frequency = 1 mc.
V_{cc} = 5.0 volts

A. Load = 20
B. Load = 1



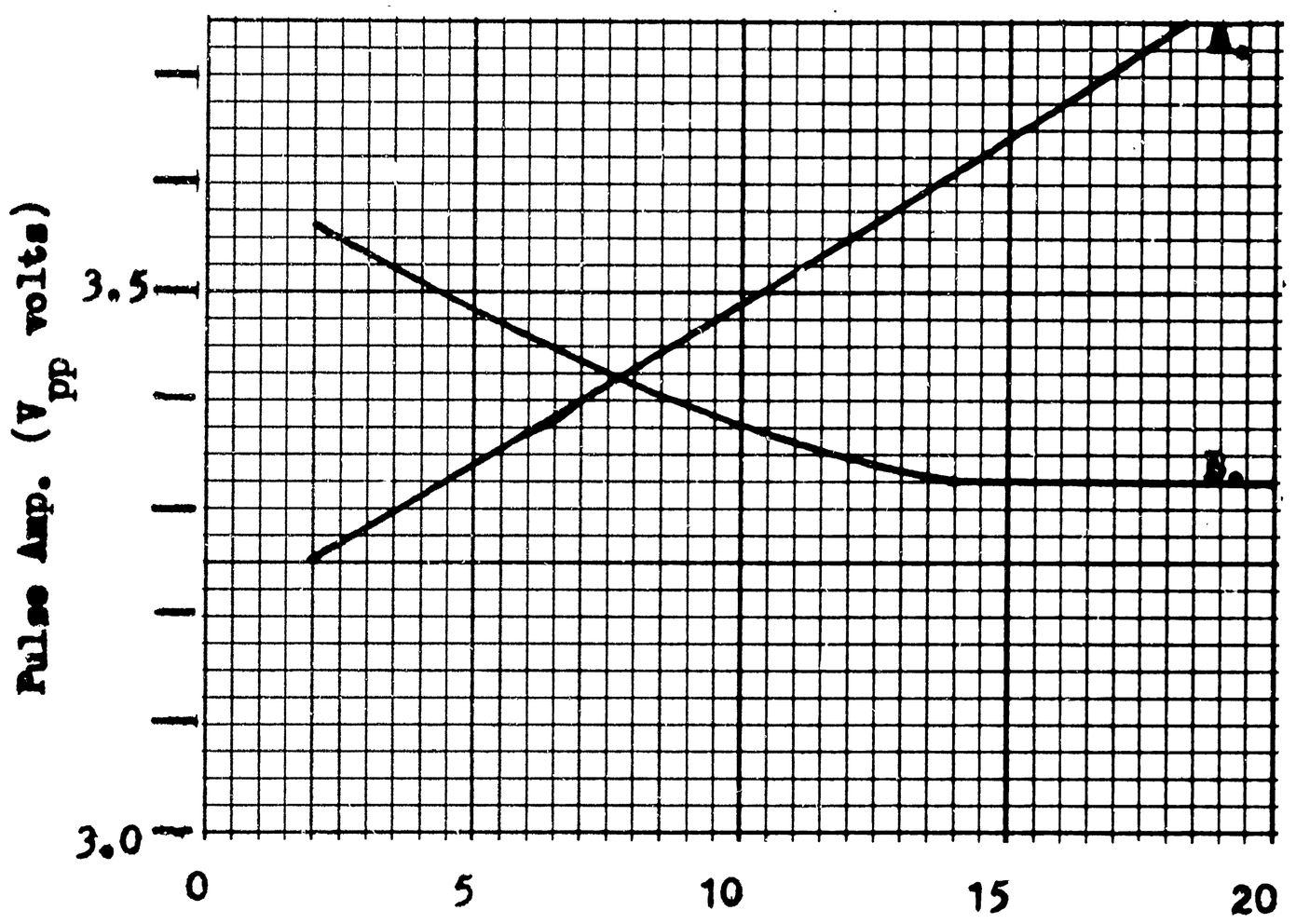
SNG-5B
Frequency = 6 mc.
V_{cc} = 5.0 volts

A. Load = 20
B. Load = 1



SNG-5B
Frequency = 1 mc.

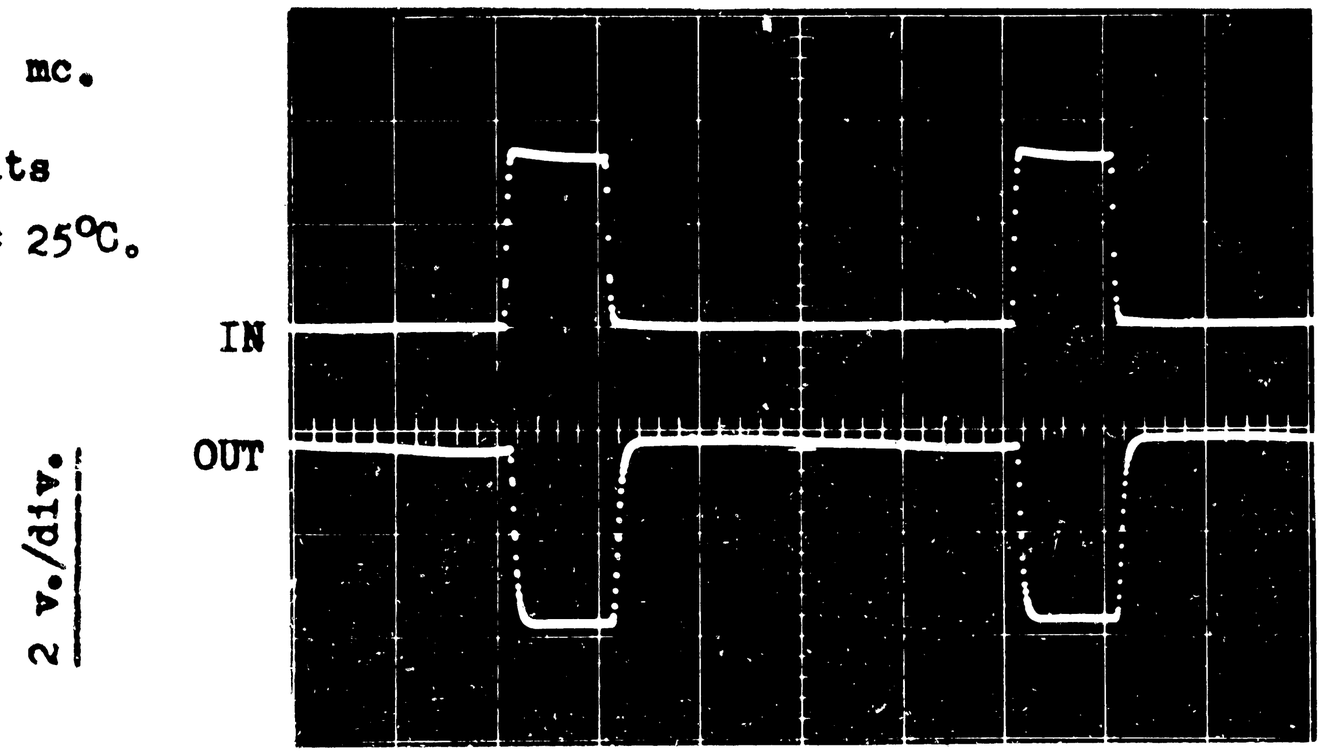
V_{cc} = 5.0 volts
T = 25 °C.



SNG-5B
Frequency = 1 mc.
V_{cc} = 5.0 volts

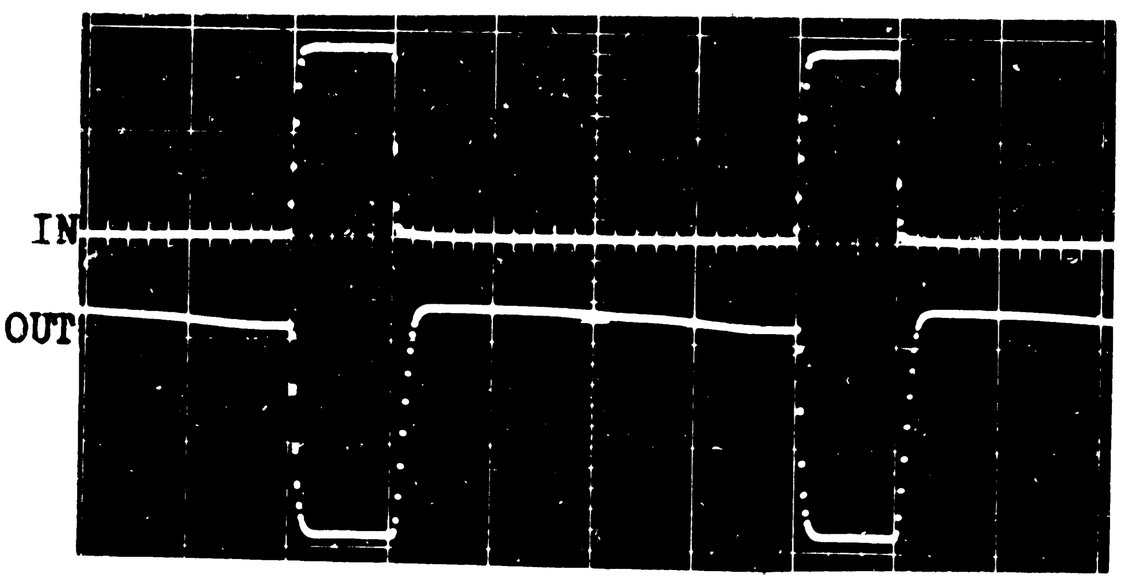
A. Input Pulse Amp.
B. Output Pulse Amp.

SNG-5B
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.



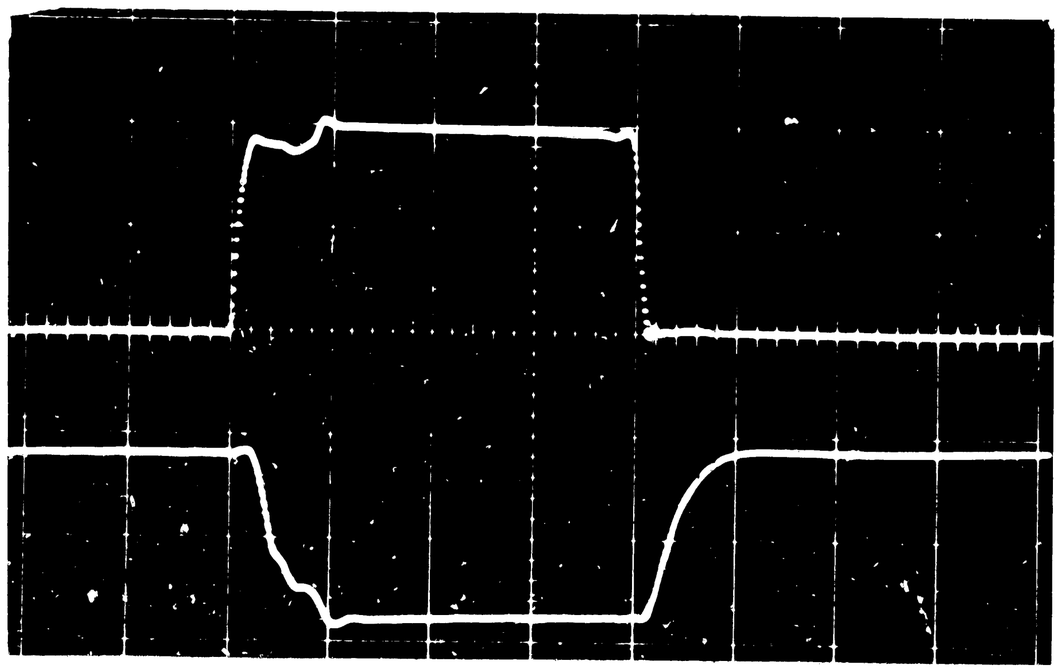
.2 μsec./div.

SNG-5B
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 125°C.



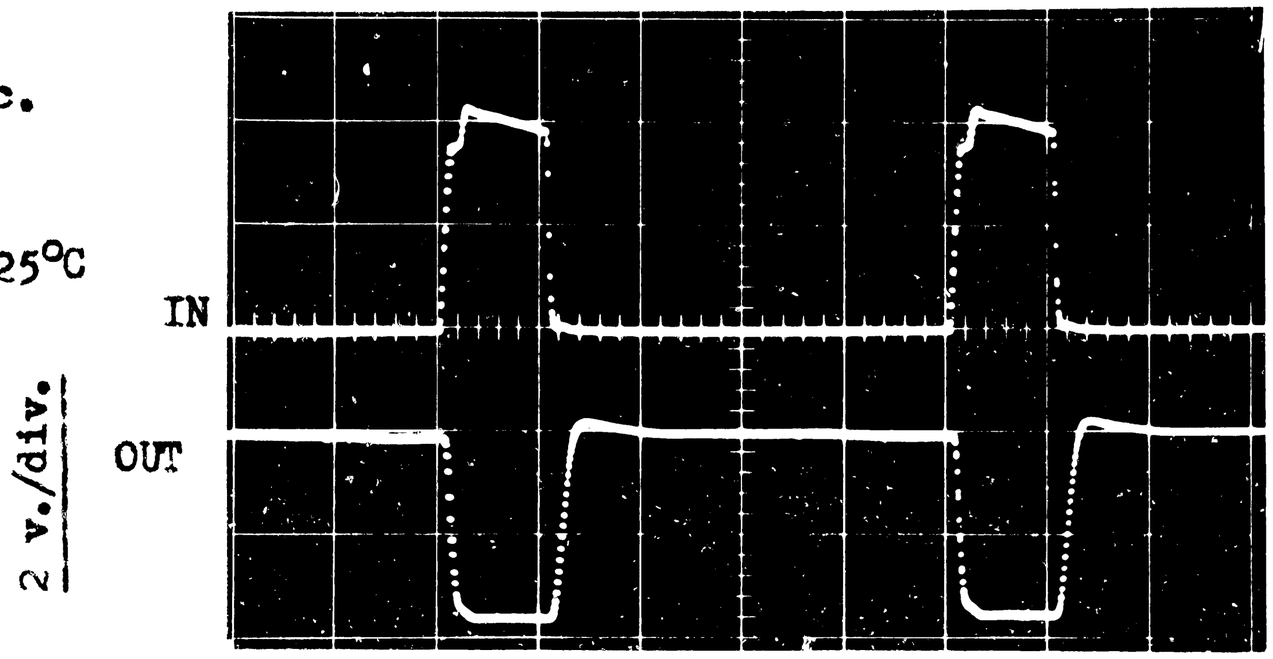
.2 μsec./div.

SNG-5B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = -55°C.



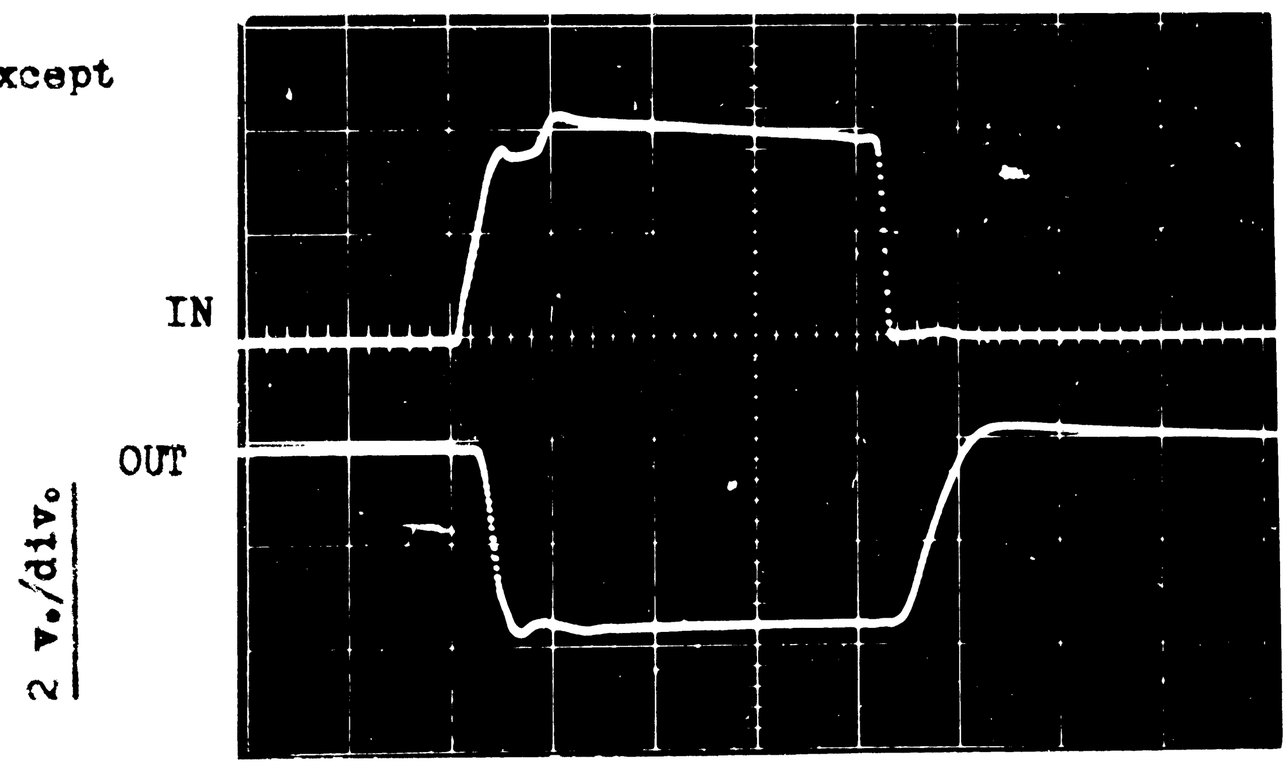
50 nsec./div.

SNG-5B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 125°C



.2 μsec./div.

SNG-5B
Same as above except
50 nsec./div.



50 nsec./div.

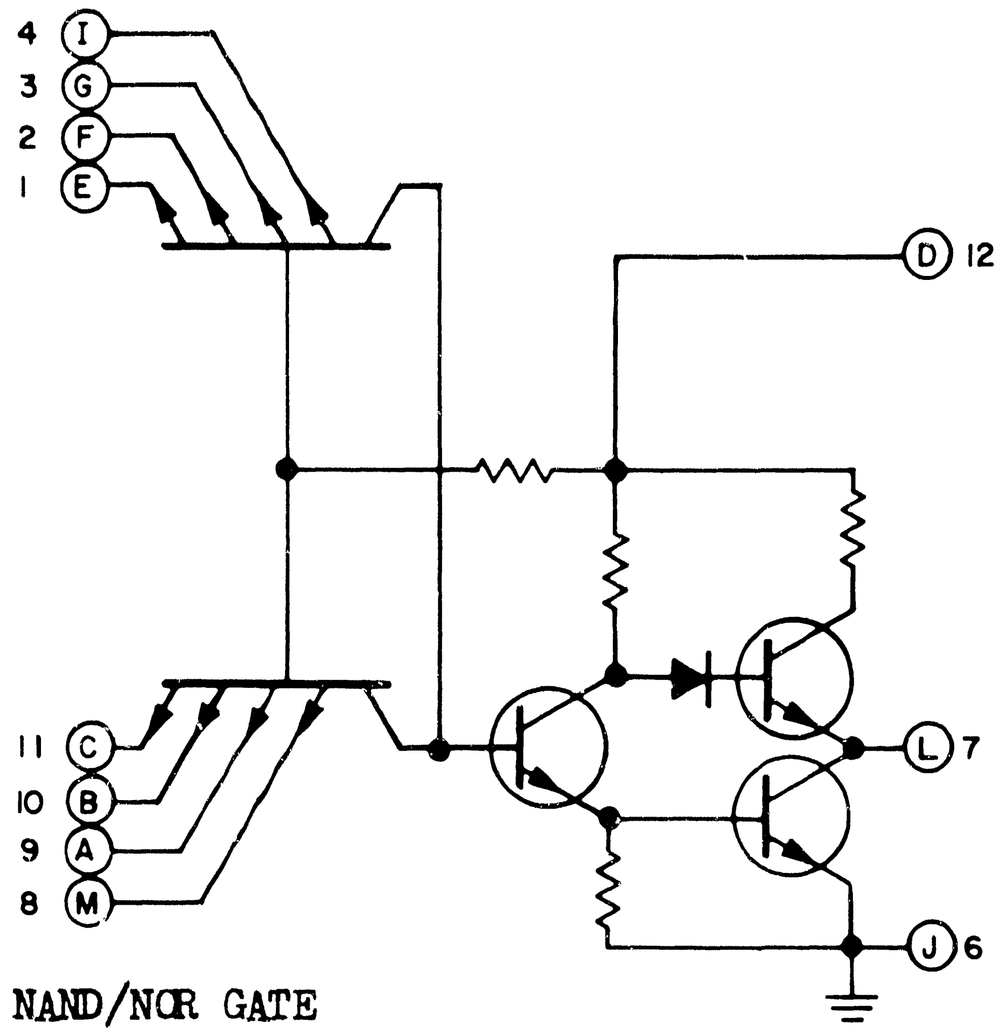
SNG 6A & B

(+) LOGIC

$L = \overline{A \cdot B \cdot C \cdot M \cdot E \cdot F \cdot G \cdot I}$

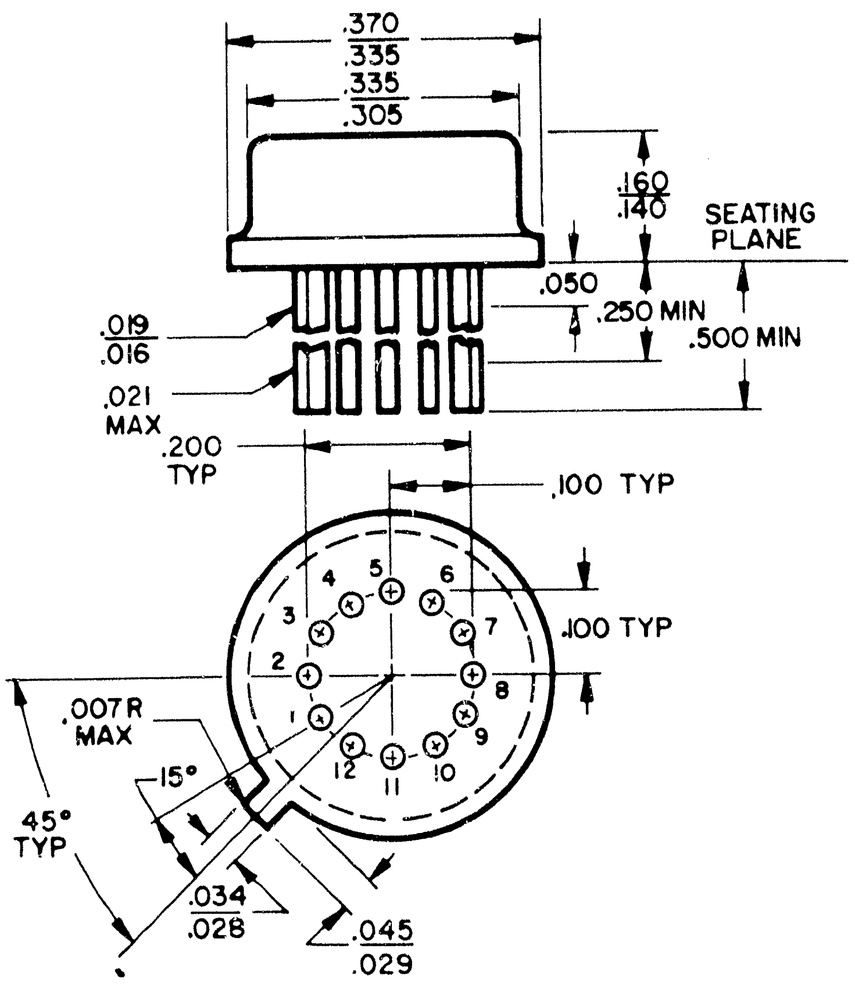
(−) LOGIC

$L = \overline{A+B+C+M+E+F+G+I}$

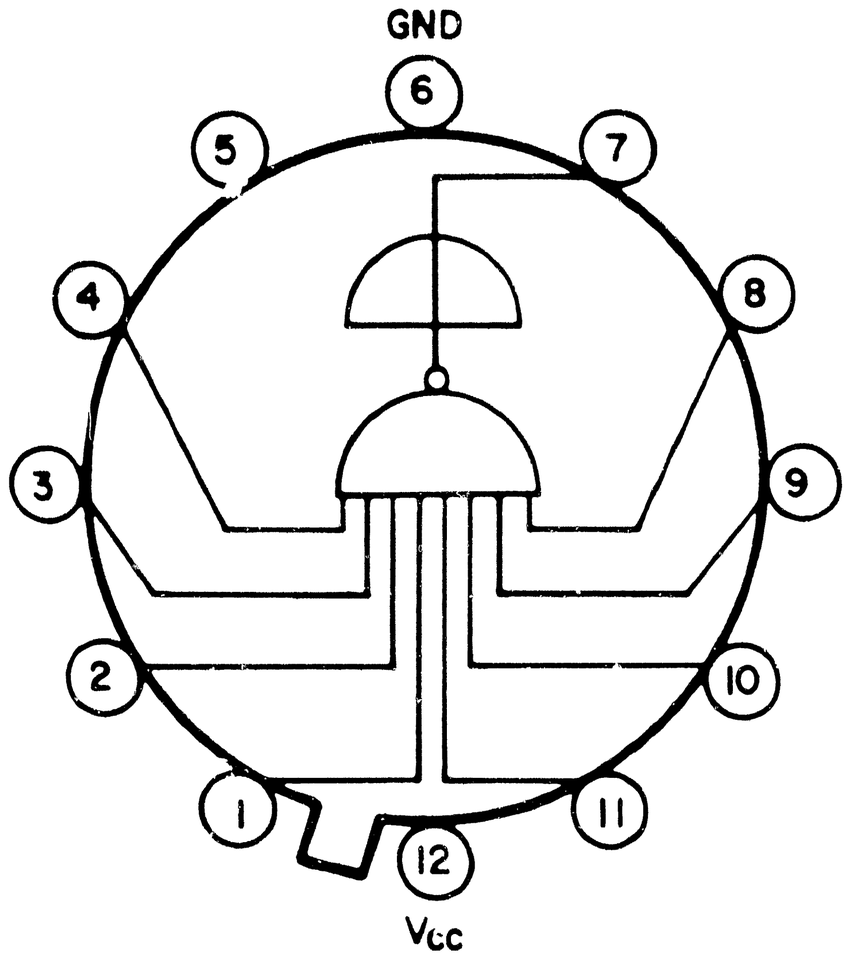


HIGH FAN-IN NAND/NOR GATE

The SNG-6 circuit is of the planar, epitaxial, and monolithic type and requires only one power supply. The "A" version consists of a single six input AND gate and the "B" version consists of a single eight input AND gate. Both of these circuits are followed by a cascaded amplifier inverting stage.



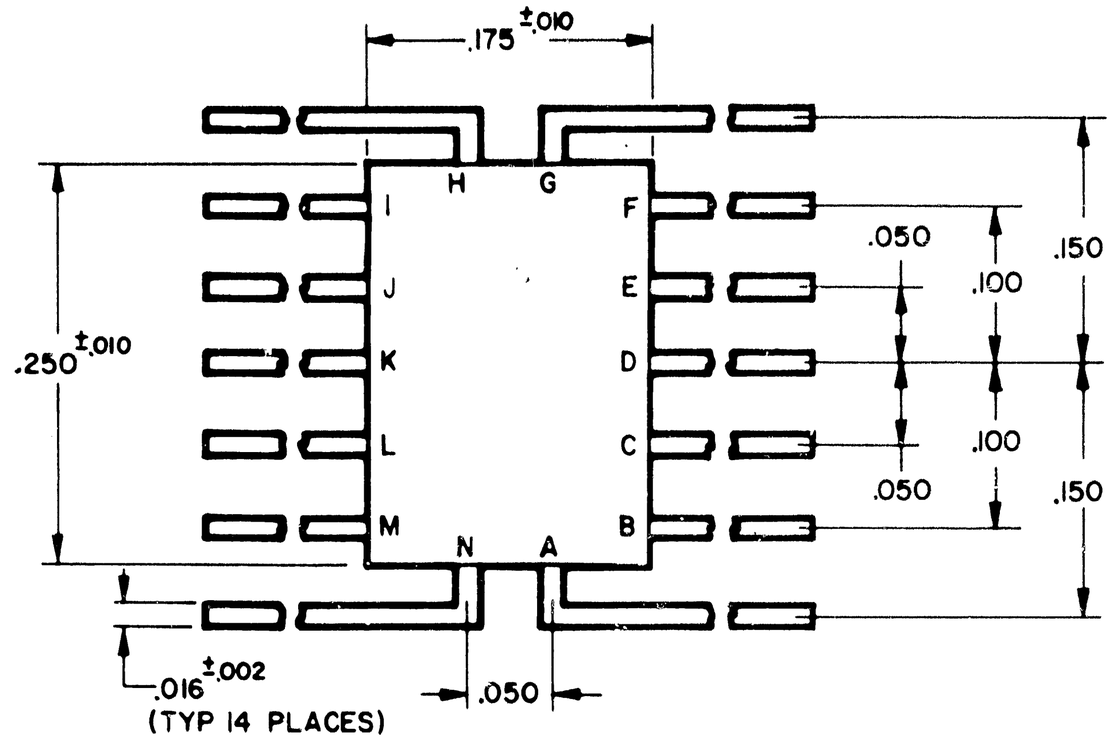
12 LEAD TO-5

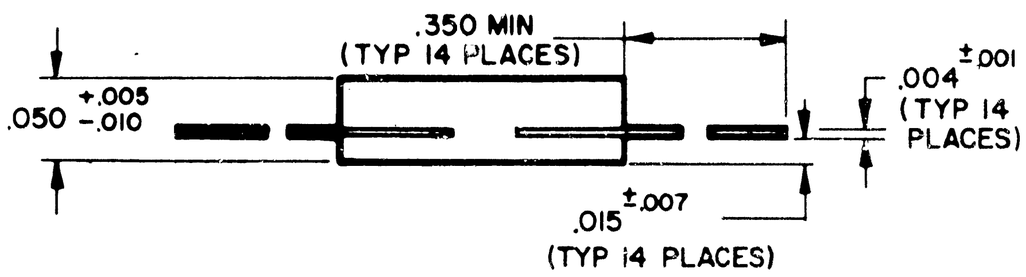


BOTTOM VIEW

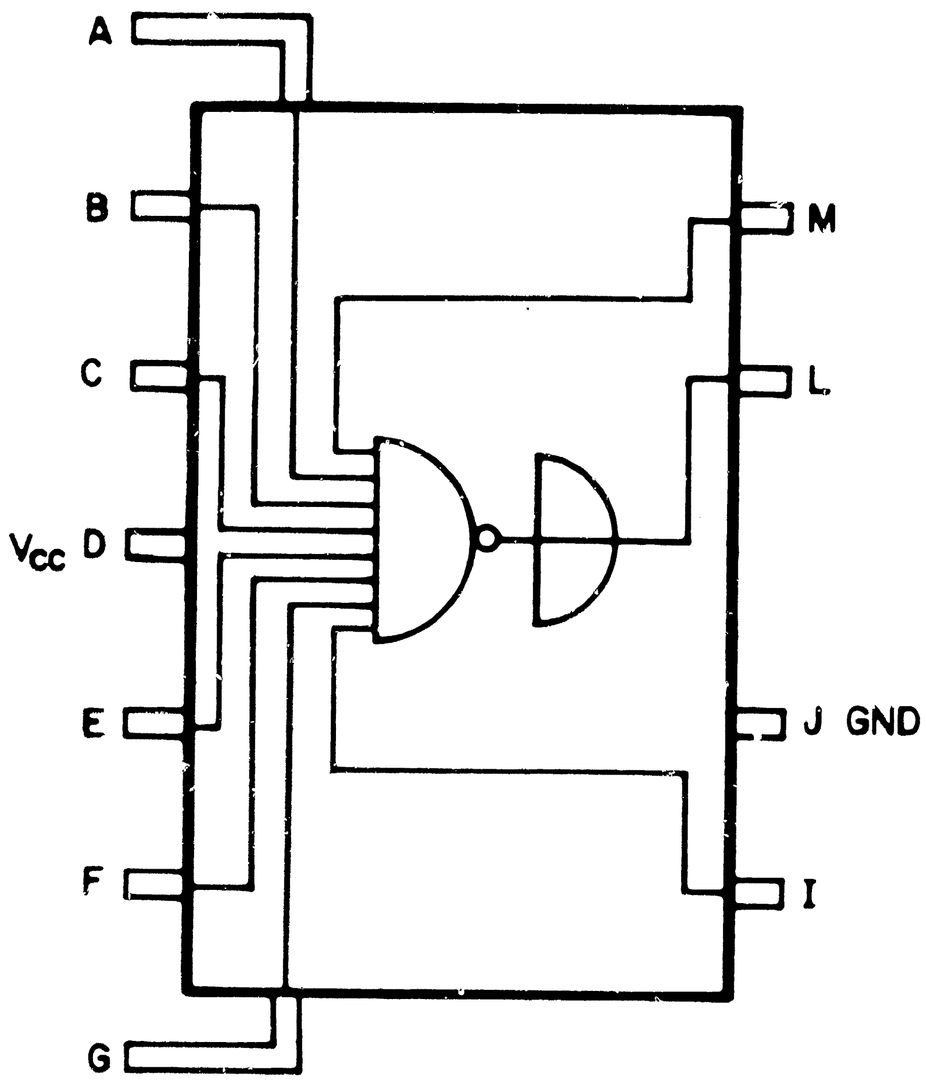
SNG-6B

FOR SNG-6A INPUTS 9-A AND 3-G ARE NOT PRESENT





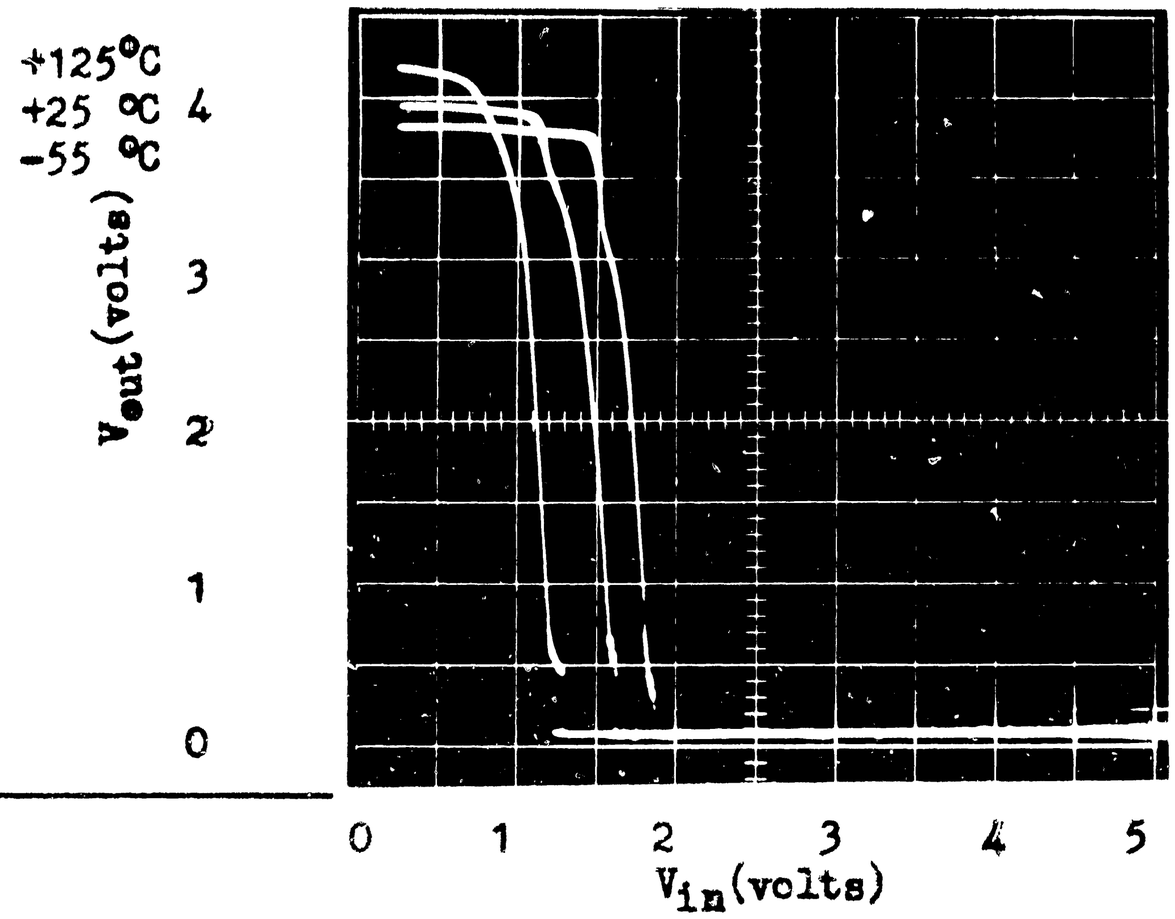
14 LEAD FLAT PACK



TOP VIEW

V_{in} vs. V_{out}

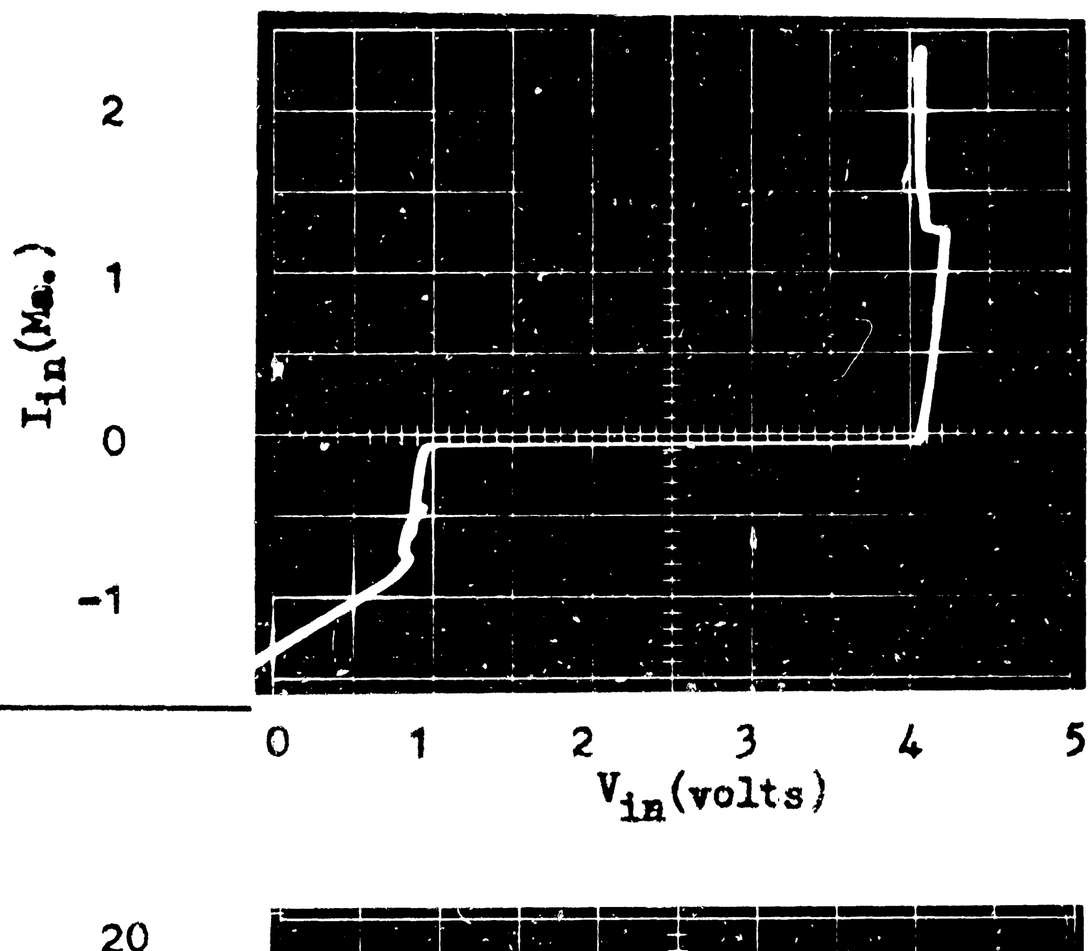
1.) V_{cc} = 5 v.



V_{in} vs. I_{in}

1.) T = 25°C

2.) V_{cc} = 5 v.

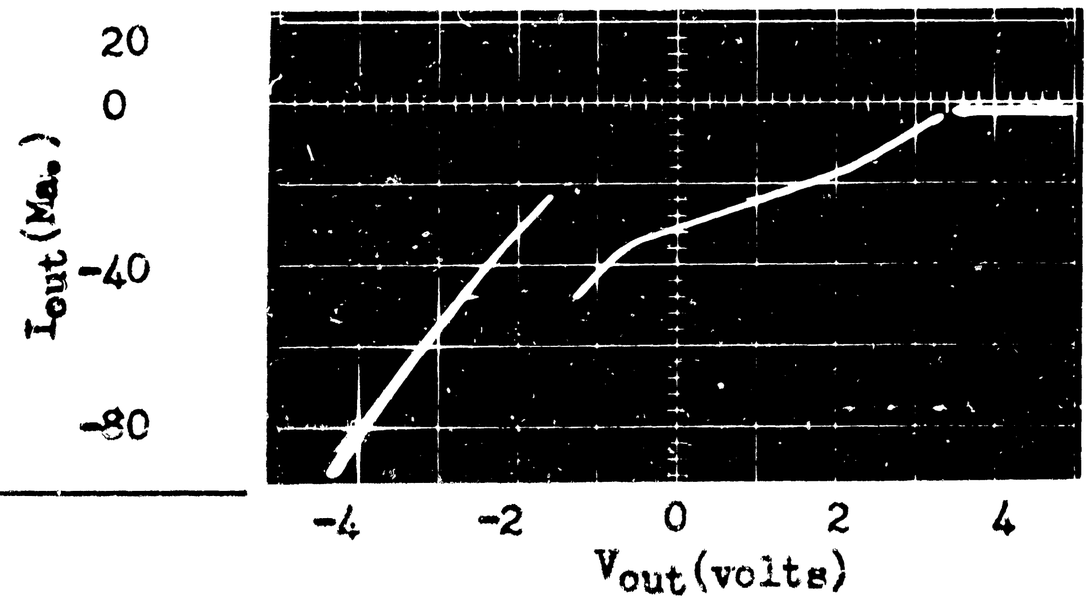


V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Pin #10 @ ground.



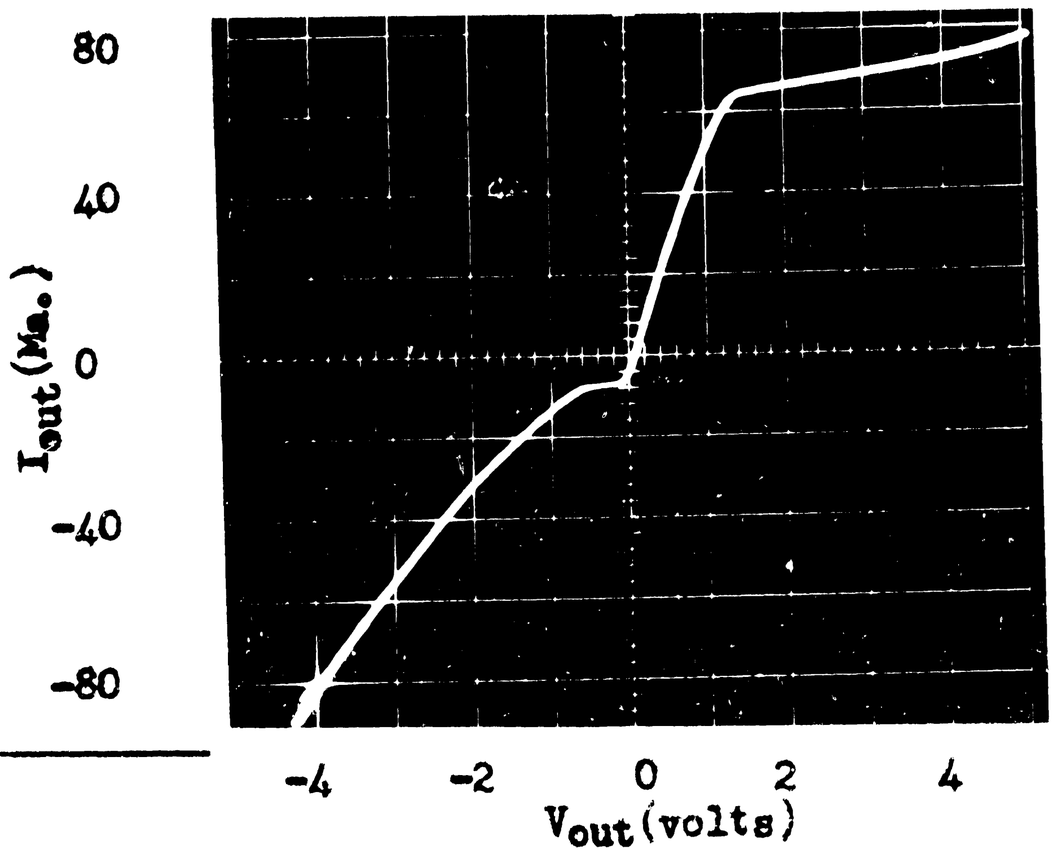
Normal operation

V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Pin #10 open.

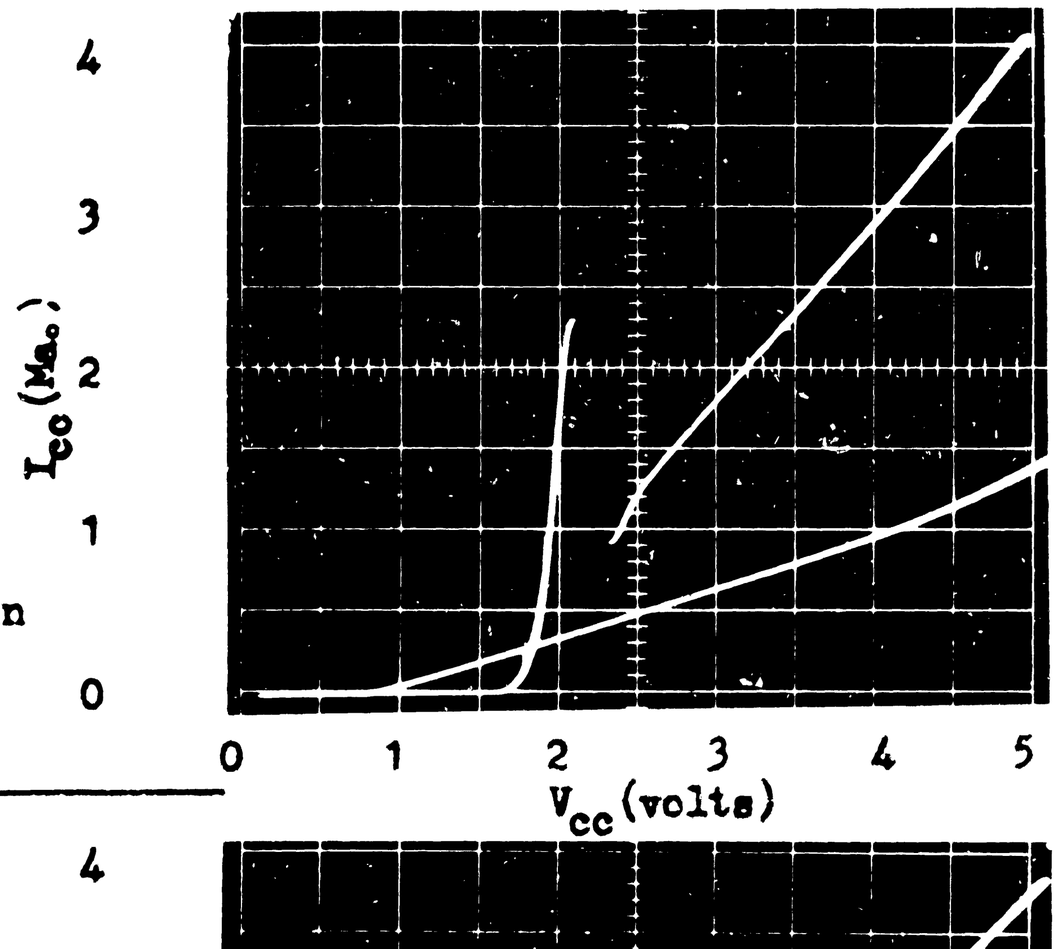


V_{cc} vs. I_{cc}

1.) T = 25°C

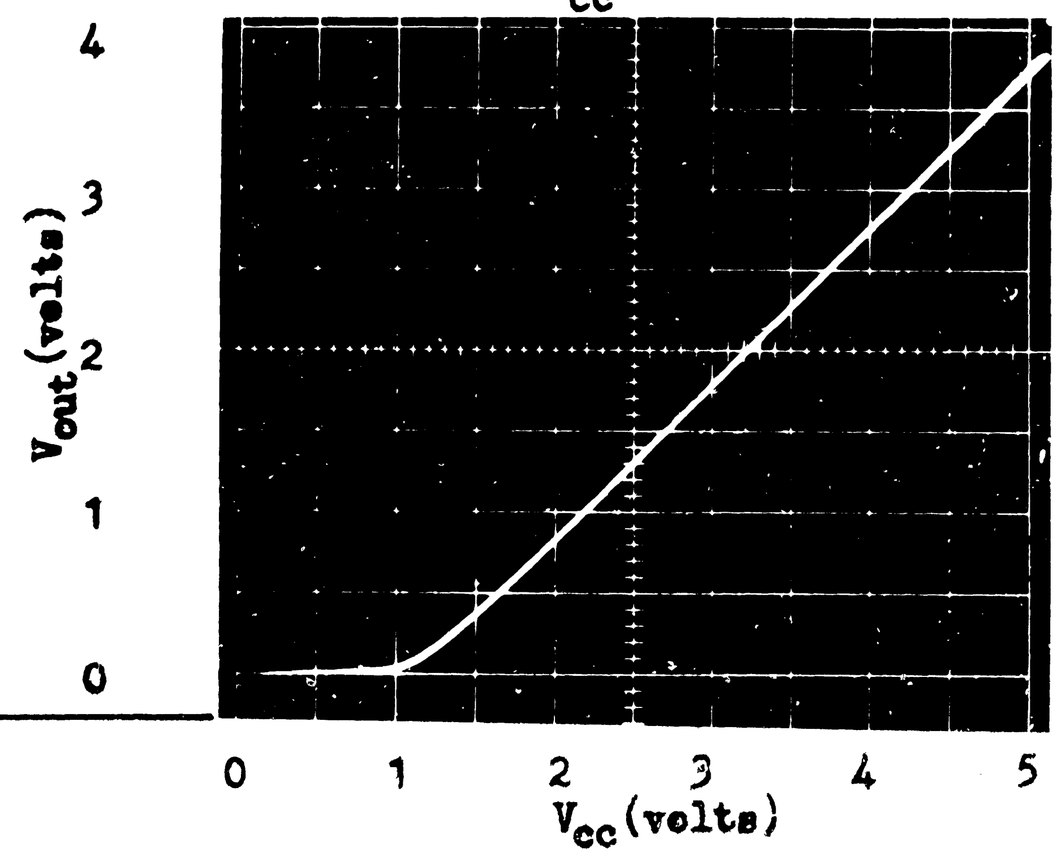
2.) Top trace with "1" in

3.) Bottom trace with "0" in.



V_{cc} vs. V_{out}

1.) T = 25°C



Circuit SNG 6B	Supply Voltage 4.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	2.8	2.7	2.9	2.4	2.8	2.8	3.0	2.4	3.0	3.1	3.4	2.7
Pulse Width (ns.)	200	197	200	194	200	198	200	197	200	202	200	205
T_r (ns.)	5.0	45	5.0	51	5.0	45	6.0	48	7.0	64	10	43
T_f (ns.)	8.0	13	8.0	33	7.0	12	7.0	29	5.0	10	4.5	17
T_d (ns.)		13		14		12		14		11		12
T_s (ns.)		9.0		9.0		9.0		9.0		8.0		8.0
T_{pd} (ns.)		14.5		20		14		19		13.5		17
Temperature:	+85°C				+125°C							
Lead	1	1	20	20	1	1	20	20				
Test Circuit	input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})	3.2	3.4	3.7	3.0	3.3	3.6	3.8	3.1				
Pulse Width (ns.)	200	206	200	213	200	211	200	220				
T_r (ns.)	11	66	15	41	14	52	17	50				
T_f (ns.)	5.0	9.0	5.0	15	5.0	10	5.0	15				
T_d (ns.)		11		12		10		11				
T_s (ns.)		9.0		11		9.0		12				
T_{pd} (ns.)		14		18		15		20				

Circuit SNG 6B	Supply Voltage 5.0				Frequency = 1 mc. Fan-in 1							
Temperature:	-55°C				-40°C				+25°C			
Load	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.3	3.2	3.5	2.8	3.3	3.3	3.6	2.9	3.5	3.6	4.0	3.2
Pulse Width (ns.)	200	200	200	201	200	201	200	203	200	204	200	208
T_r (ns.)	5.0	36	7.0	46	6.0	36	8.0	44	7.5	45	12	38
T_f (ns.)	7.0	11	7.0	30	6.0	10	6.0	28	4.5	8.5	4.5	14
T_d (ns.)		11		12		10		11		9.0		11
T_s (ns.)		9.0		9.0		8.0		8.0		8.0		8.0
T_{pd} (ns.)		13		18		12.5		17		12		16

Temperature:	+85°C				+125°C			
Load	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.7	3.9	4.2	3.4	3.8	4.0	4.3	3.5
Pulse Width (ns.)	200	208	200	216	200	214	200	224
T_r (ns.)	12	41	17	40	15	48	20	50
T_f (ns.)	5.0	9.0	5.0	14	4.5	9.0	5.0	14
T_d (ns.)		10		11		10		11
T_s (ns.)		9.0		11		9.0		12
T_{pd} (ns.)		13		18		14		20

Circuit SNG 6B	Supply Voltage 5.5				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.8	3.7	4.1	3.3	3.8	3.8	4.3	3.4	4.0	4.1	4.6	3.6
Pulse Width (ns.)	200	202	200	204	200	202	200	206	200	205	200	211
T_r (ns.)	6.0	31	8.0	44	6.0	31	9.0	42	8.5	36	14	37
T_f (ns.)	6.0	9.4	5.0	30	5.5	9.0	5.0	19	4.2	8.0	5.0	13
T_d (ns.)		10		11		9.0		11		9.0		10
T_s (ns.)		9.0		9.0		8.0		8.0		8.0		10
T_{pd} (ns.)		12		17		12		16		11		16

Temperature:	+85°C				+125°C			
Lead	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	4.2	4.1	4.9	3.9	4.3	4.6	4.9	4.0
Pulse Width (ns.)	200	211	200	219	200	216	200	227
T_r (ns.)	13	38	39	40	17	46	41	51
T_f (ns.)	4.0	8.0	5.0	13	4.0	9.0	4.5	13
T_d (ns.)		9.0		10		9.0		10
T_s (ns.)		9.0		11		10		12
T_{pd} (ns.)		12.5		17.5		13		20

Circuit SNG 6B	Supply Voltage 5.0				Frequency = 6 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.0	3.8	2.9	3.2	3.1	3.9	2.9	3.4	3.3	4.1	3.2
Pulse Width (ns.)	50	51	50	52	50	52	50	53	50	54	50	58
T_r (ns.)	5.0	25	7.0	43	5.0	24	9.0	39	8.0	25	34	35
T_f (ns.)	6.0	8.0	6.0	30	5.0	7.0	5.0	17	4.0	6.0	4.0	13
T_d (ns.)		9.0		11		8.0		10		7.0		8.0
T_s (ns.)		8.0		6.0		8.0		9.0		7.0		8.0
T_{pd} (ns.)		11.5		15.5		11		14.5		10		14

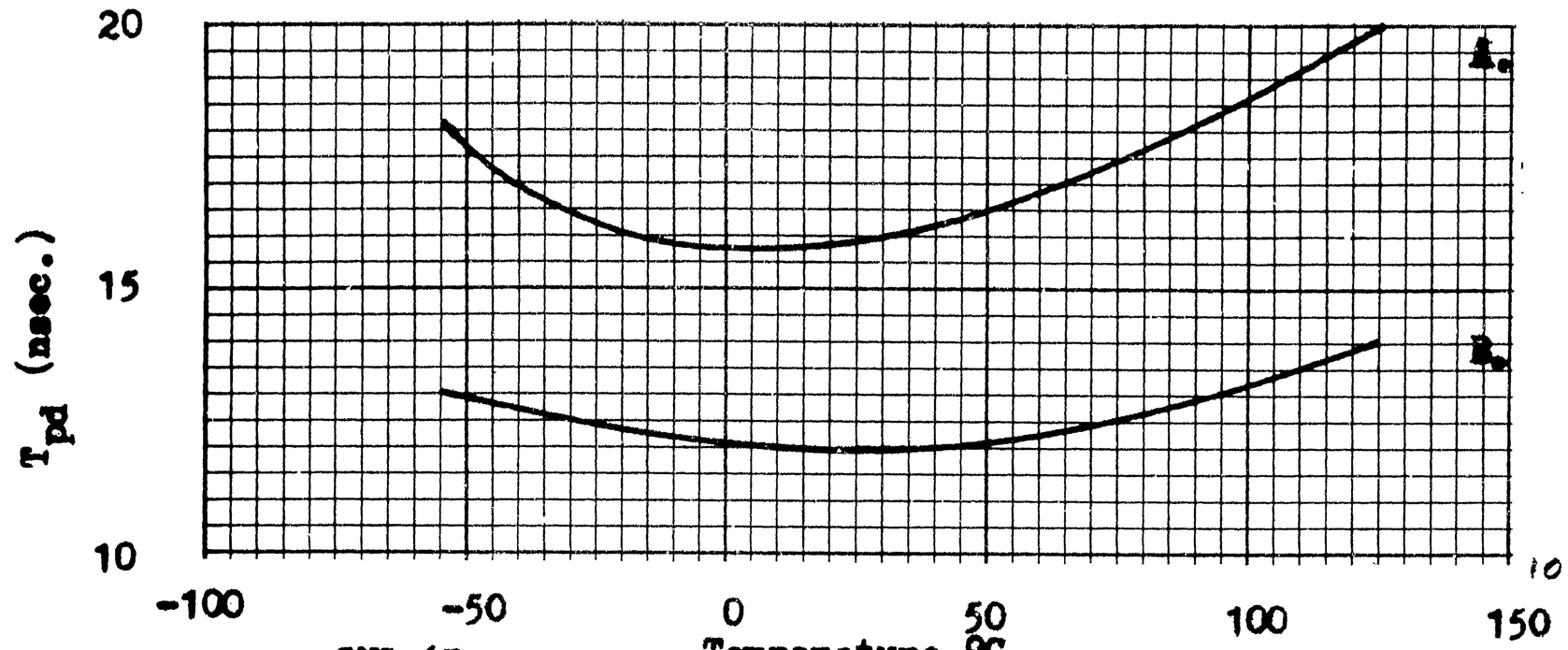
Temperature:	+85°C				+125°C			
Lead	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.6	3.6	4.4	3.3	3.7	3.7	4.4	3.4
Pulse Width (ns.)	50	59	50	68	50	66	50	78
T_r (ns.)	11	29	37	39	14	36	39	48
T_f (ns.)	4.0	6.0	4.0	13	4.0	6.0	4.0	13
T_d (ns.)		7.0		8.0		7.0		7.0
T_s (ns.)		7.0		10		8.0		11
T_{pd} (ns.)		10		15		11		17

3.3.16

SNG 6B V_{cc} = 5.0 v. Frequency = 1 mc. Input P. Width = 200 nsec.

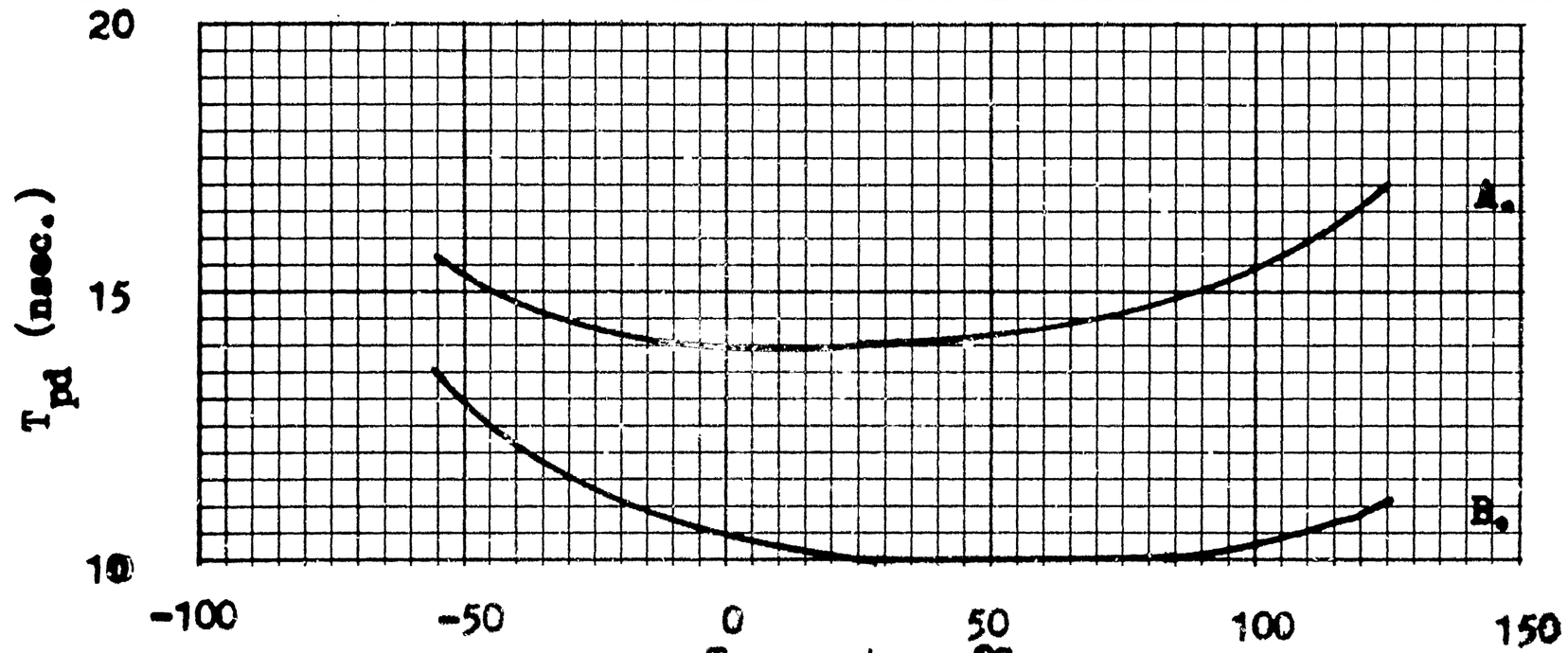
Load Ckts.	20	18	16	14	12	10	8	6	4	2
T_{pd}	16.0	15.5	15.0	14.5	14.5	14.0	13.5	13.5	13.0	12.5
T_r Output	37.5	37.0	36.0	34.0	33.0	33.0	33.0	33.0	33.0	33.0
T_f Output	13.5	13.0	12.5	12.0	11.5	11.0	11.0	10.0	10.0	9.0
Pulse Amp. (Input)	3.8	3.8	3.7	3.7	3.7	3.6	3.5	3.5	3.3	3.2
Pulse Amp. (Output)	3.0	3.1	3.1	3.2	3.2	3.3	3.3	3.3	3.3	3.4

Temperature = 25°C.



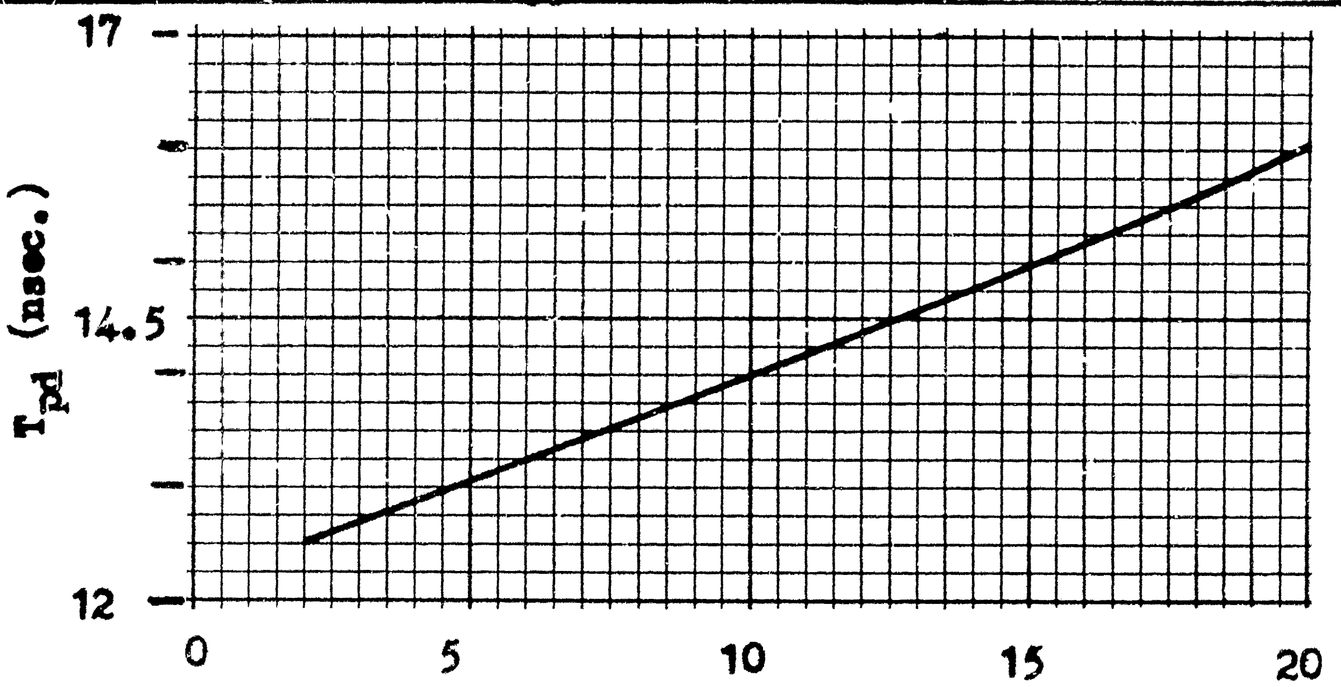
SNG-6B
Frequency = 1 mc.
V_{cc} = 5.0 volts

A. Load = 20
B. Load = 1



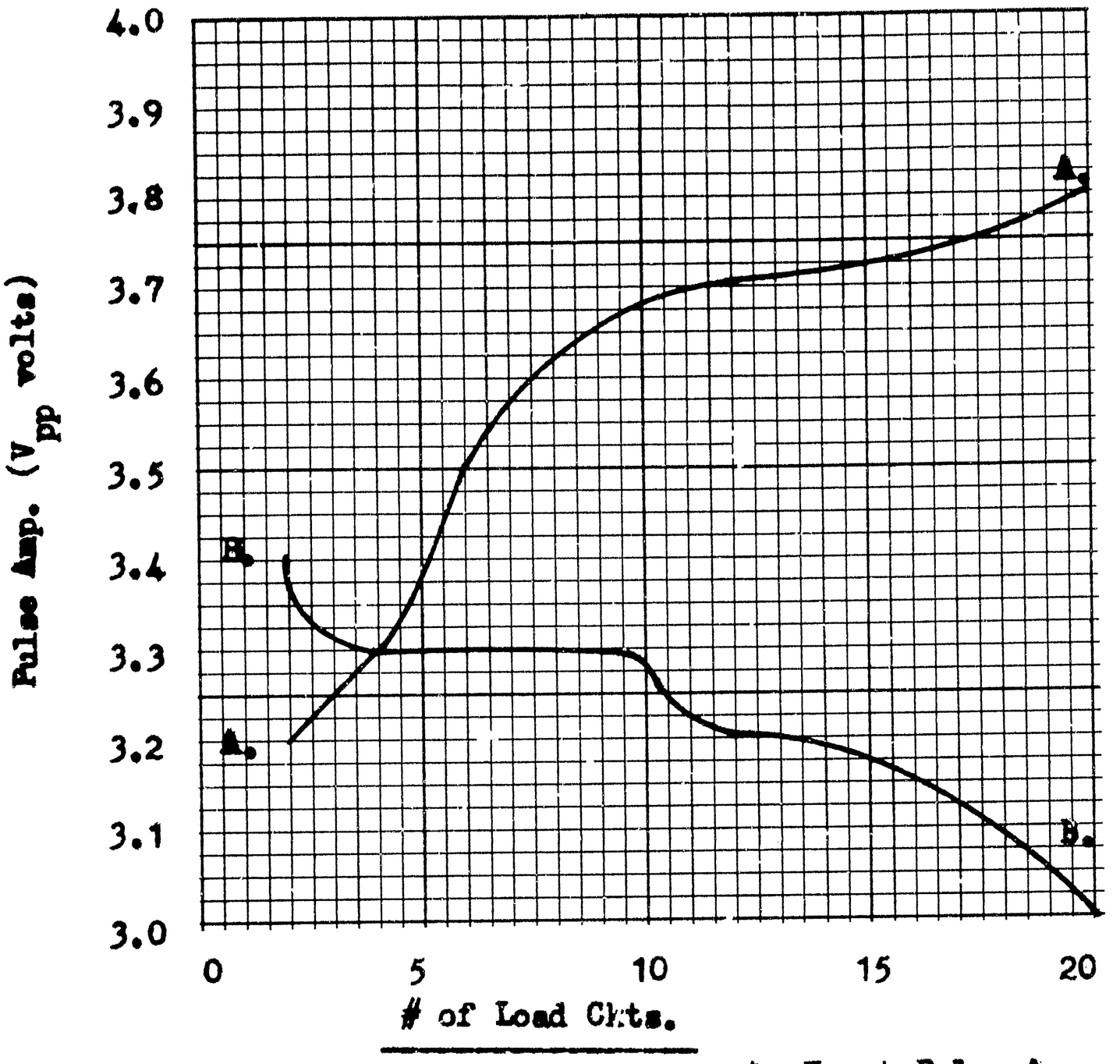
SNG-6B
Frequency = 6 mc. V_{cc} = 5.0 v.

A. Load = 20
B. Load = 1



SNG-6B
Frequency = 1 mc.

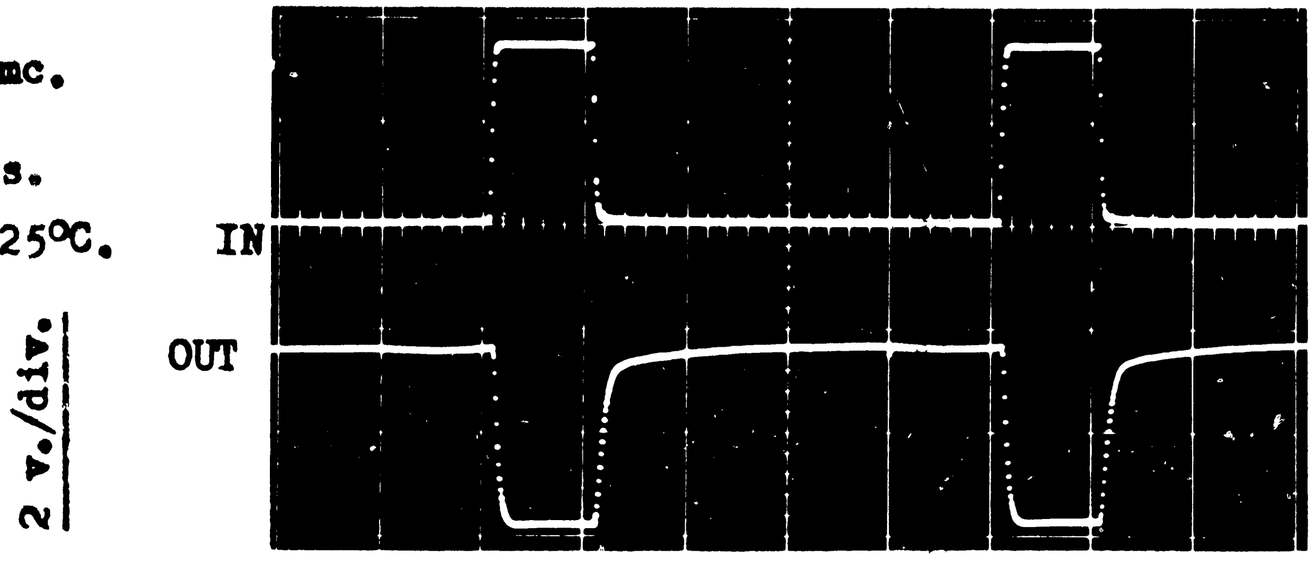
V_{cc} = 5.0 volts
T = 25 °C.



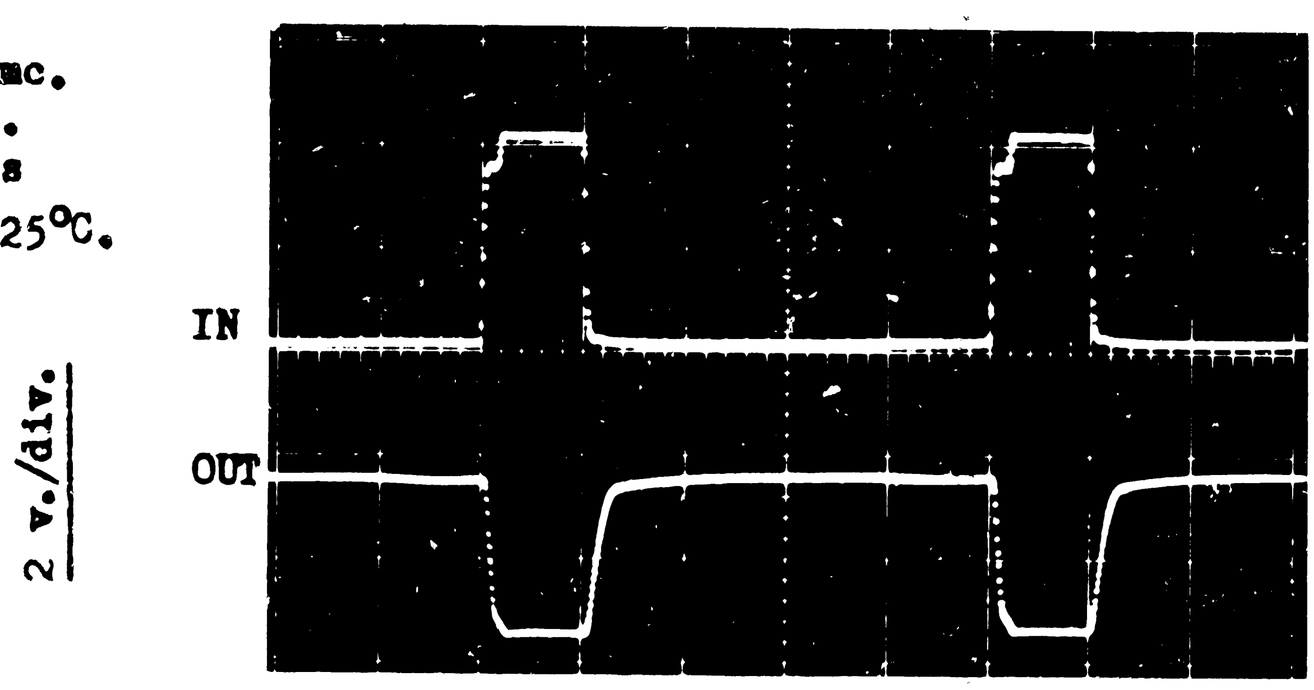
A. Input Pulse Amp.
B. Output Pulse Amp.

SNG-6B
Frequency = 1 mc.
V_{cc} = 5.0 volts
T = 25 °C.

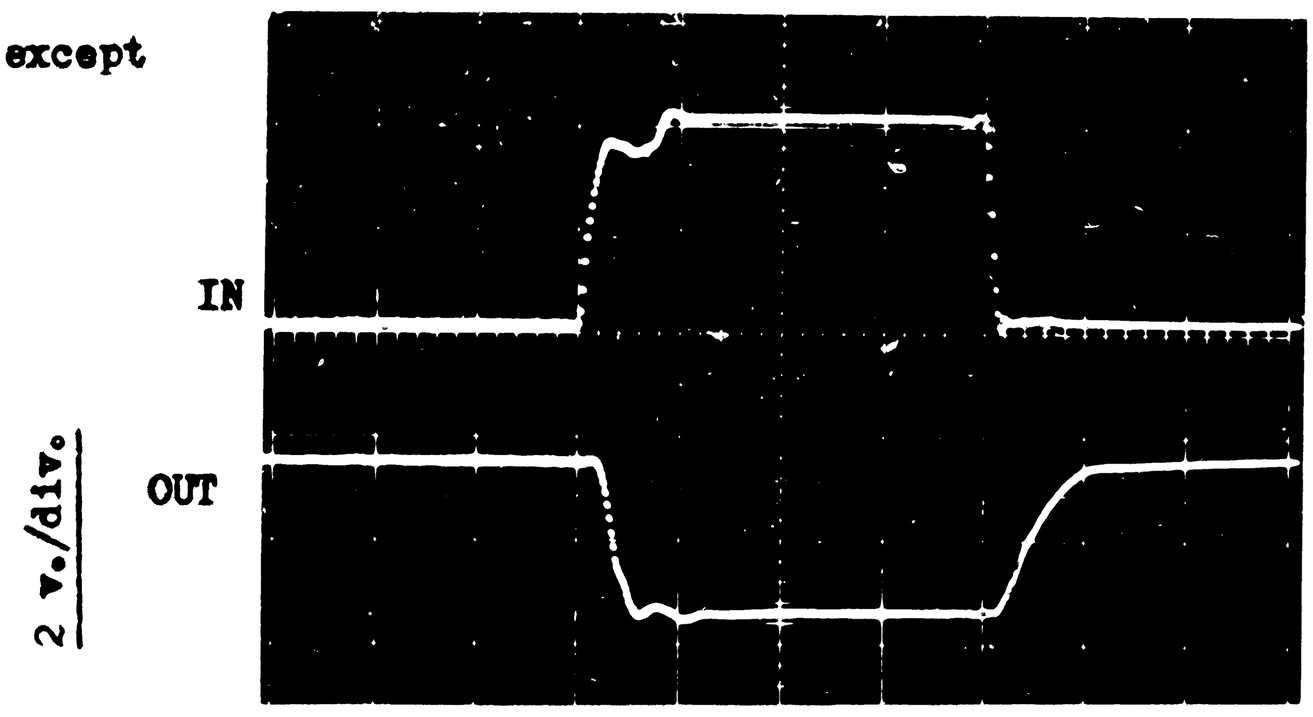
SNG-6B
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts.
Temperature = 25°C.



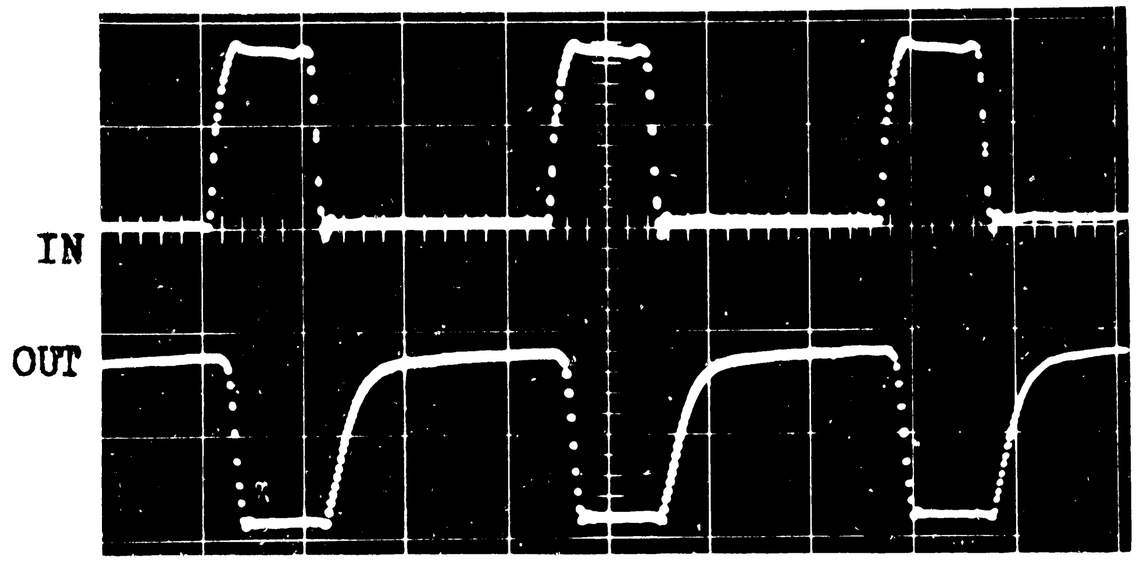
SNG-6B
Frequency = 1 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 25°C.



SNG-6B
Same as above except
50 nsec./div.

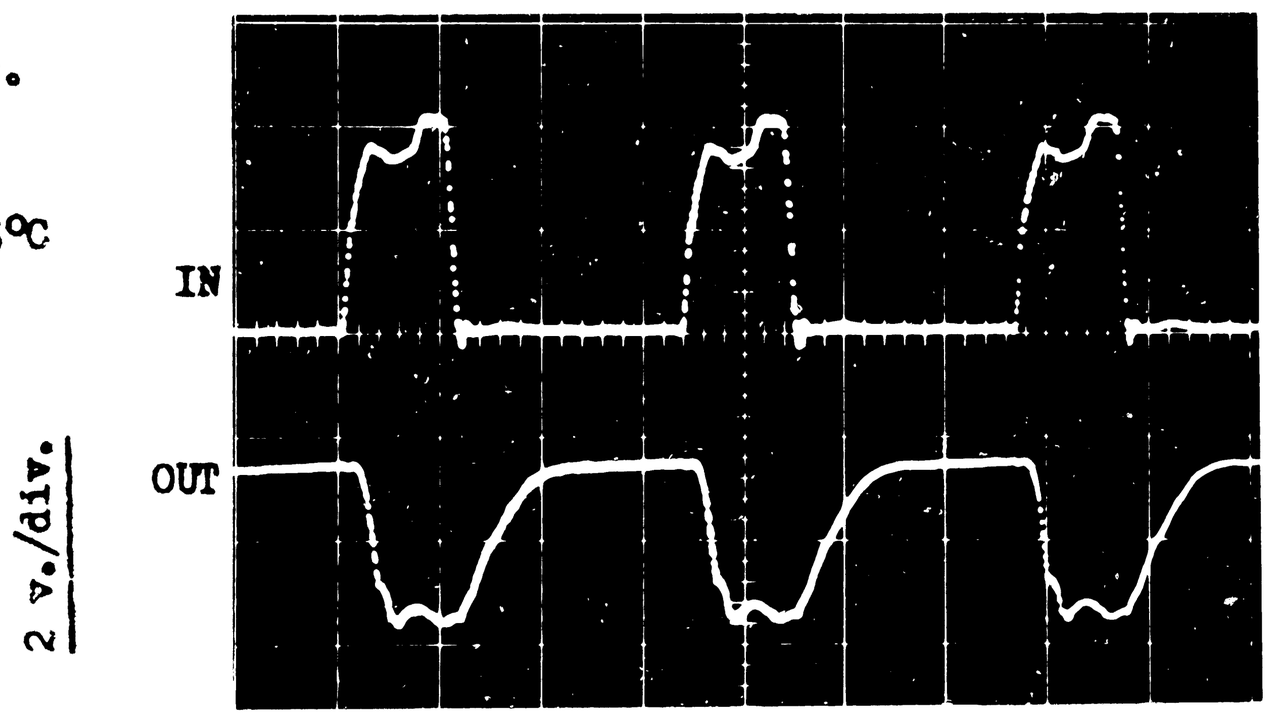


SNG-6B
Frequency = 6 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.

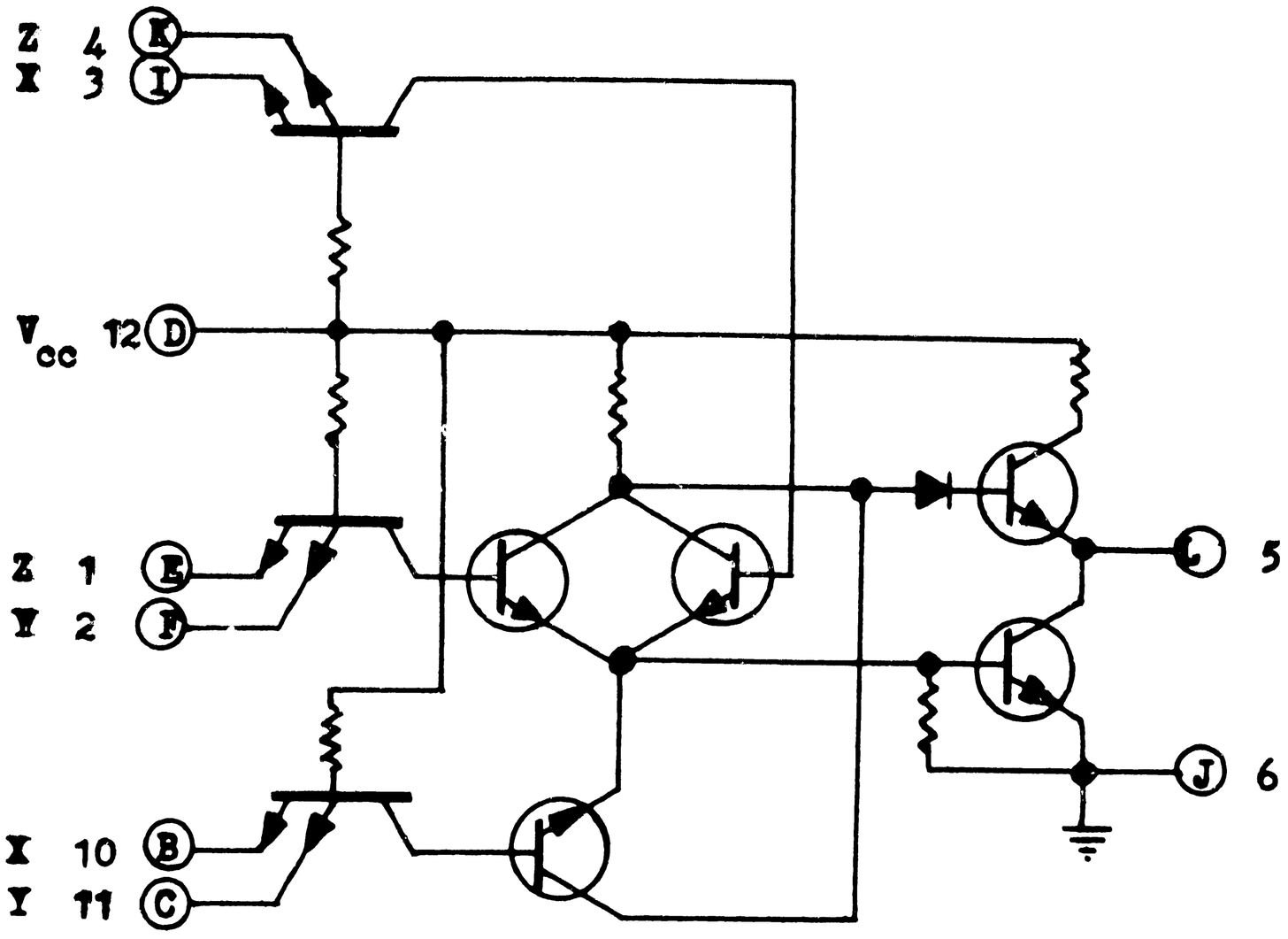


50 nsec./div.

SNG-6B
Frequency = 6 mc.
Load = 20 ckts.
V_{cc} = 5.0 volts
Temperature = 25°C



50 nsec./div.

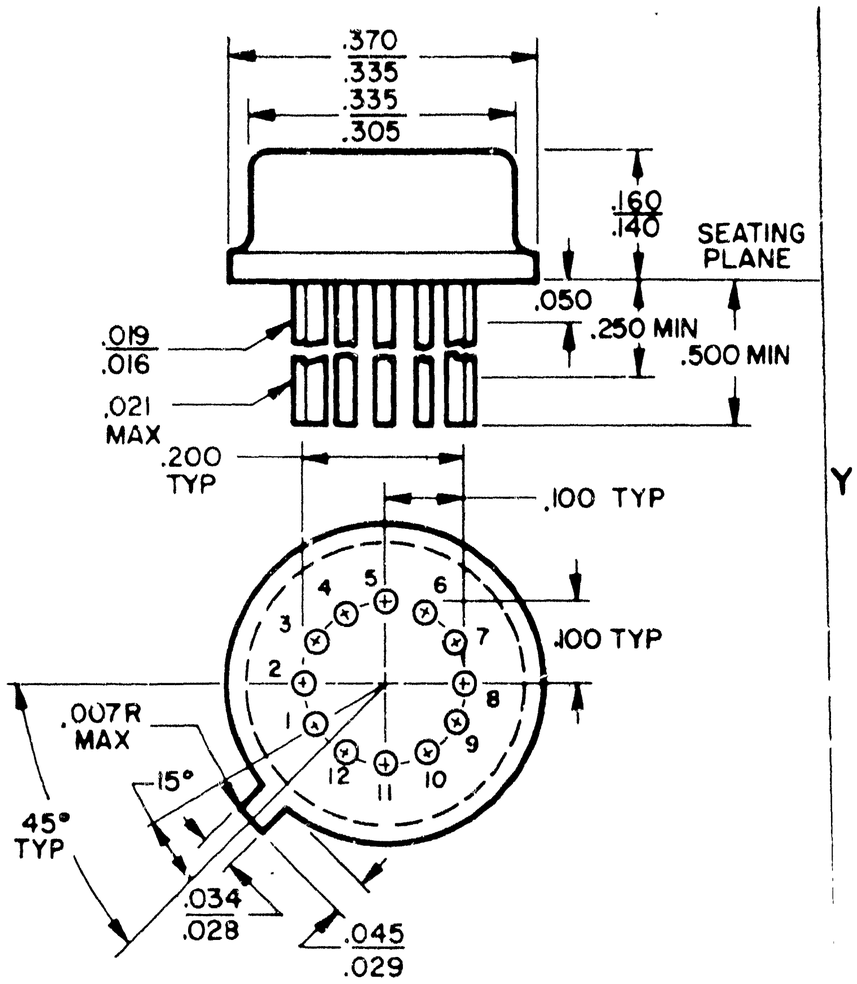


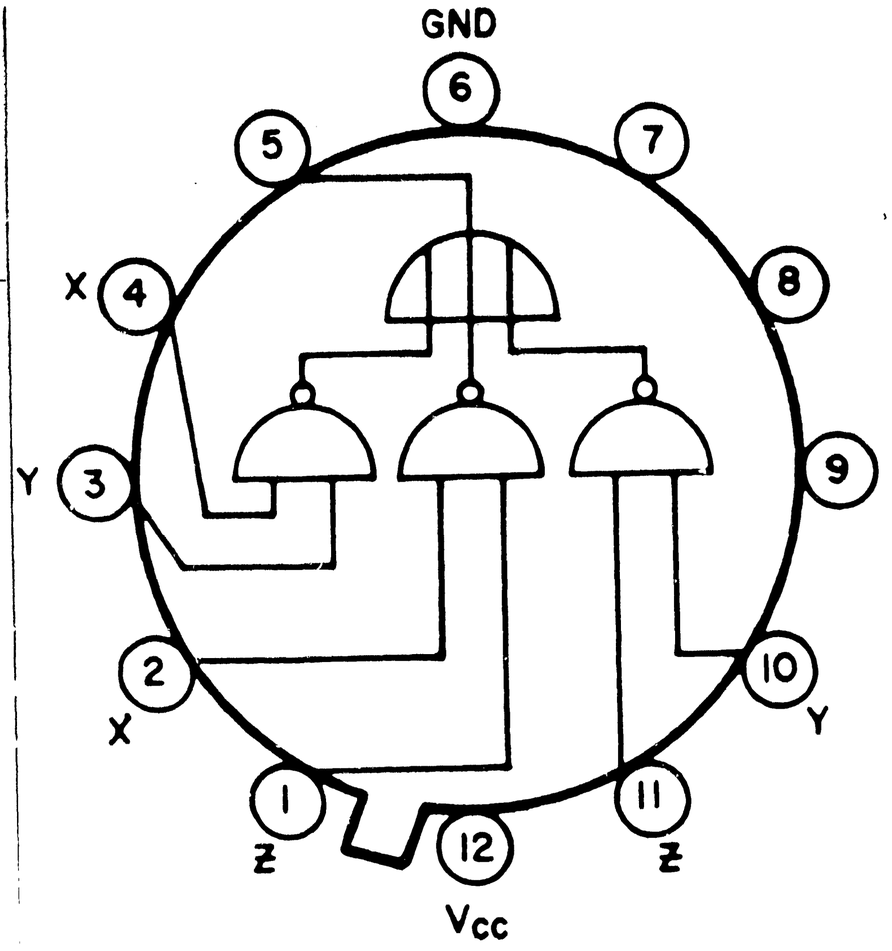
Majority Decision Gate SNG-20

(+) Logic $L = \overline{X \cdot Y + X \cdot Z + Y \cdot Z}$

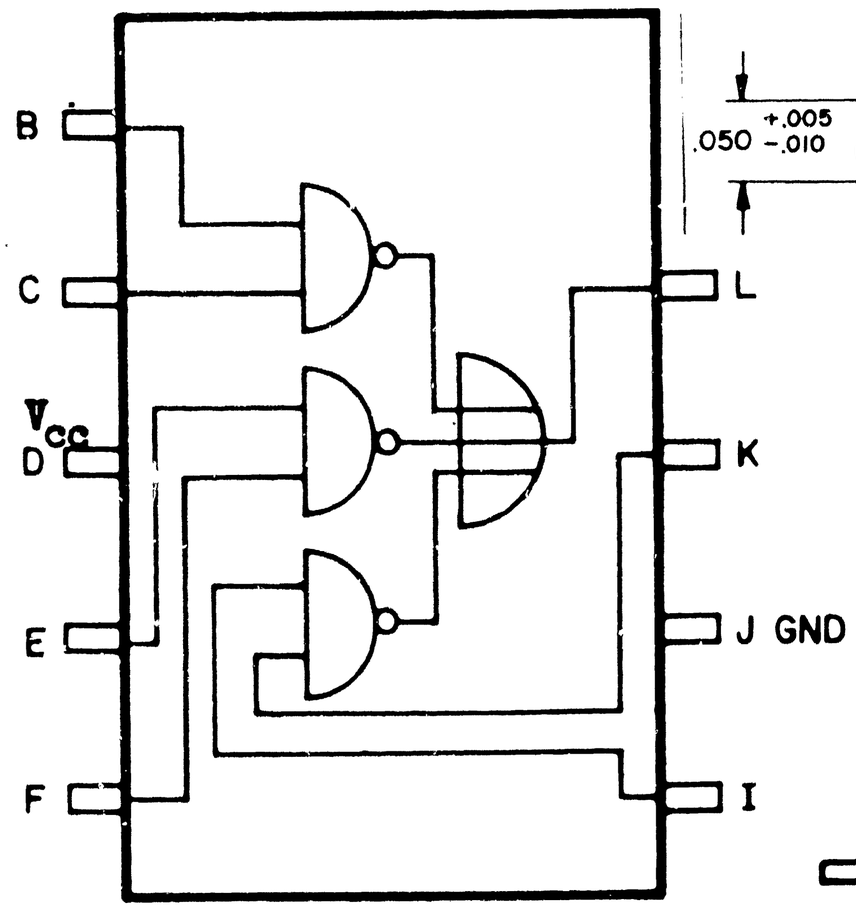
(-) Logic $L = \overline{(X+Y)(X+Z)(Y+Z)}$

The SNG-20 AND-NOR Gate (Voter) consists of three, two input AND gates followed by an OR element. It was intended primarily as a majority decision (voter) gate in systems using triple redundancy. The circuit, requiring a single power supply, is of the monolithic, epitaxial, and planar type.

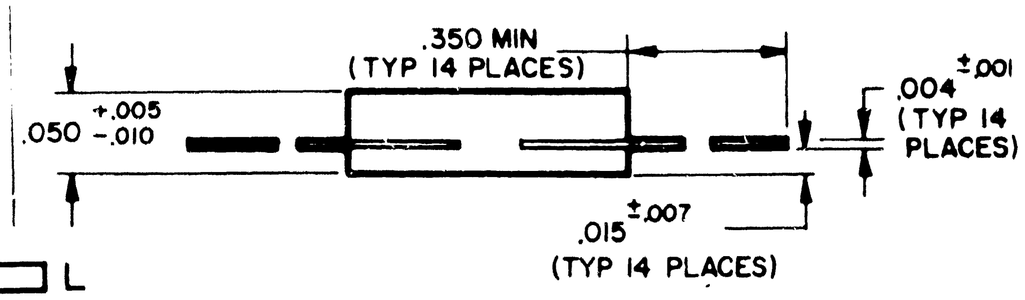




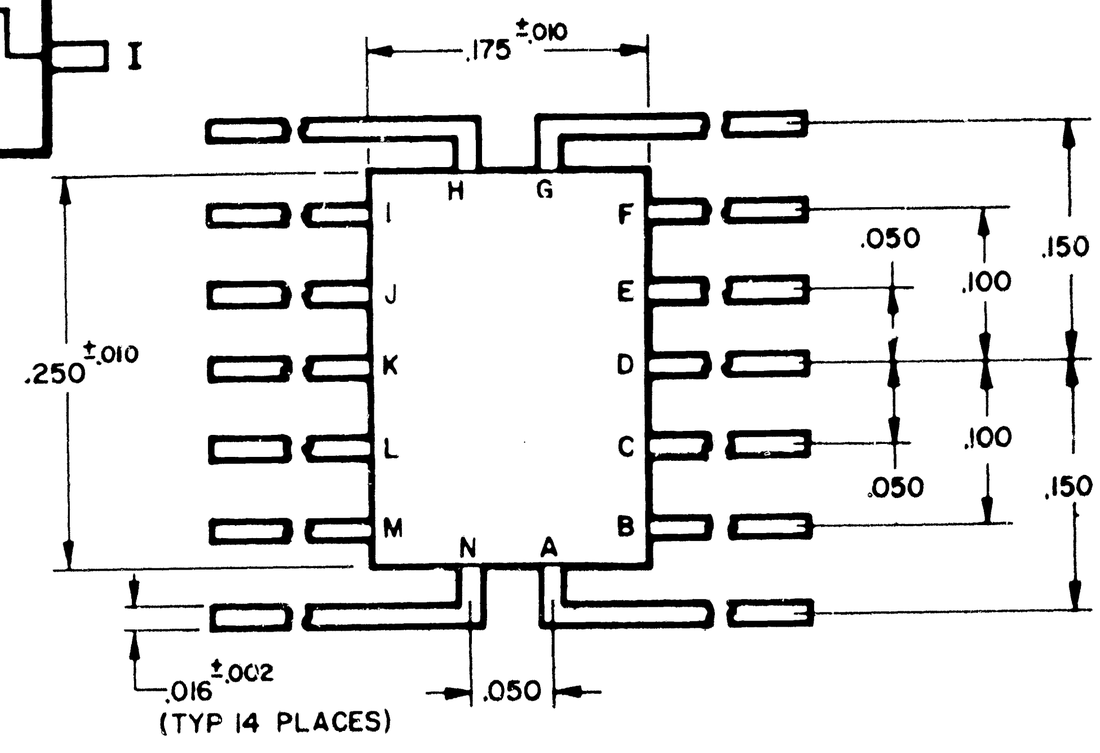
12 LEAD TO-5



BOTTOM VIEW



14 LEAD FLAT PACK



TOP VIEW

Circuit SNG 20 Supply Voltage 4.5 Frequency = 1mc. Fan-in 1

Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	2.9	3.2	2.9	2.6	2.9	3.3	2.9	2.6	3.0	3.4	3.0	2.7
Pulse Width (ns.)	200	197	200	193	200	200	200	195	200	207	200	205
T_r (ns.)	5.0	*82 273	5.0	35	5.0	*75 261	4.0	28	6.0	*27 200	7.0	23
T_f (ns.)	8.0	10	8.0	16	7.0	10	7.0	14	5.0	8.0	5.0	11
T_d (ns.)		19		20		17		17		13		13
T_s (ns.)		14		13		14		13		14		14
T_{pd} (ns.)		20		22		19		20		18		18.5

Temperature:	+85°C				+125°C			
Lead	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.2	3.5	3.2	2.9	3.3	3.6	3.4	3.0
Pulse Width (ns.)	200	215	200	212	200	222	200	220
T_r (ns.)	10	*25 78	10	26	13	38	13	30
T_f (ns.)	4.0	6.0	4.0	9.0	4.0	6.0	4.0	9.0
T_d (ns.)		12		12		11		11
T_s (ns.)		16		16		18		17
T_{pd} (ns.)		18		18		19		19

*Measured from 90% to 20% instead of 90% to 10% (The larger measurement is from 90% to 10%.)

Circuit SNG 20	Supply Voltage 5.0				Frequency = 1 mc.				Fan-in 1			
Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.3	3.7	3.4	3.0	3.3	3.7	3.3	2.9	3.4	3.8	3.5	3.2
Pulse Width (ns.)	200	202	200	199	200	204	200	201	200	210	200	208
T_r (ns.)	5.0	*33 / 232	5.0	26	5.0	*22 / 206	5.0	24	7.0	*21 / 150	8.0	22
T_f (ns.)	7.0	10	7.0	14	6.0	9.0	6.0	13	4.0	6.0	4.0	10
T_d (ns.)		14		15		13		14		11		11
T_s (ns.)		13		13		13		13		14		14
T_{pd} (ns.)		18		19		17		18		16		17

Temperature:	+85°C				+125°C			
Lead	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.6	4.0	3.7	3.3	3.8	4.0	3.9	3.5
Pulse Width (ns.)	200	218	200	215	200	224	200	224
T_r (ns.)	11	35	12	25	15	37	14	31
T_f (ns.)	4.0	5.0	4.0	8.0	4.0	6.0	4.0	7.0
T_d (ns.)		10		10		10		10
T_s (ns.)		16		16		19		18
T_{pd} (ns.)		17		17.5		18		19

*Measured from 90% to 20% instead of 90% to 10% (The larger measurement is from 90% to 10%.)

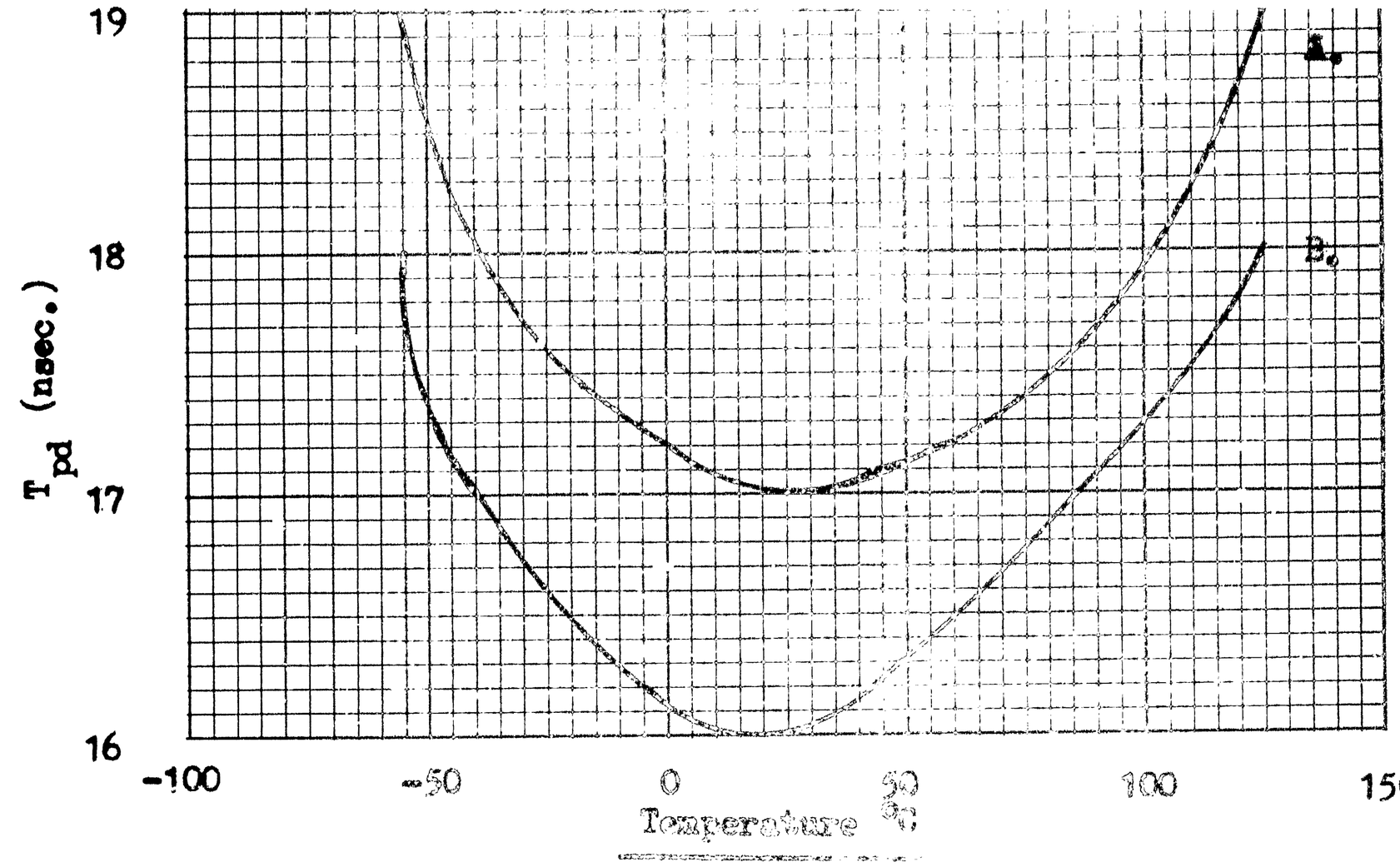
Circuit SNG 20 Supply Voltage 5.5 Frequency = 1 mc. Fan-in 1

Temperature:	-55°C				-40°C				+25°C			
Load	1	1	6	6	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.7	4.1	3.8	3.3	3.8	4.2	3.8	3.4	3.9	4.3	4.1	3.6
Pulse Width (ns.)	200	205	200	203	200	207	200	205	200	212	200	209
T_r (ns.)	5.0	~~*22~~ 190	6.0	24	6.0	~~*19~~ 160	6.0	22	8.0	~~*20~~ 95	9.0	22
T_f (ns.)	6.0	9.0	6.0	13	5.0	8.0	5.0	11	4.0	6.0	4.0	8.0
T_d (ns.)		12		12		11		11		10		11
T_s (ns.)		13		13		13		13		14		14
T_{pd} (ns.)		16		17.5		15		17		15		16

Temperature:	+85°C				+125°C			
Load	1	1	6	6	1	1	6	6
Test Circuit	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	4.2	4.5	4.3	3.8	4.4	4.5	4.4	3.9
Pulse Width (ns.)	200	219	200	218	200	227	200	225
T_r (ns.)	12	32	13	26	16	35	16	32
T_f (ns.)	4.0	5.0	4.0	7.0	4.0	6.0	4.0	7.0
T_d (ns.)		10		10		9.0		10
T_s (ns.)		17		16		19		18
T_{pd} (ns.)		16		17		17.5		19

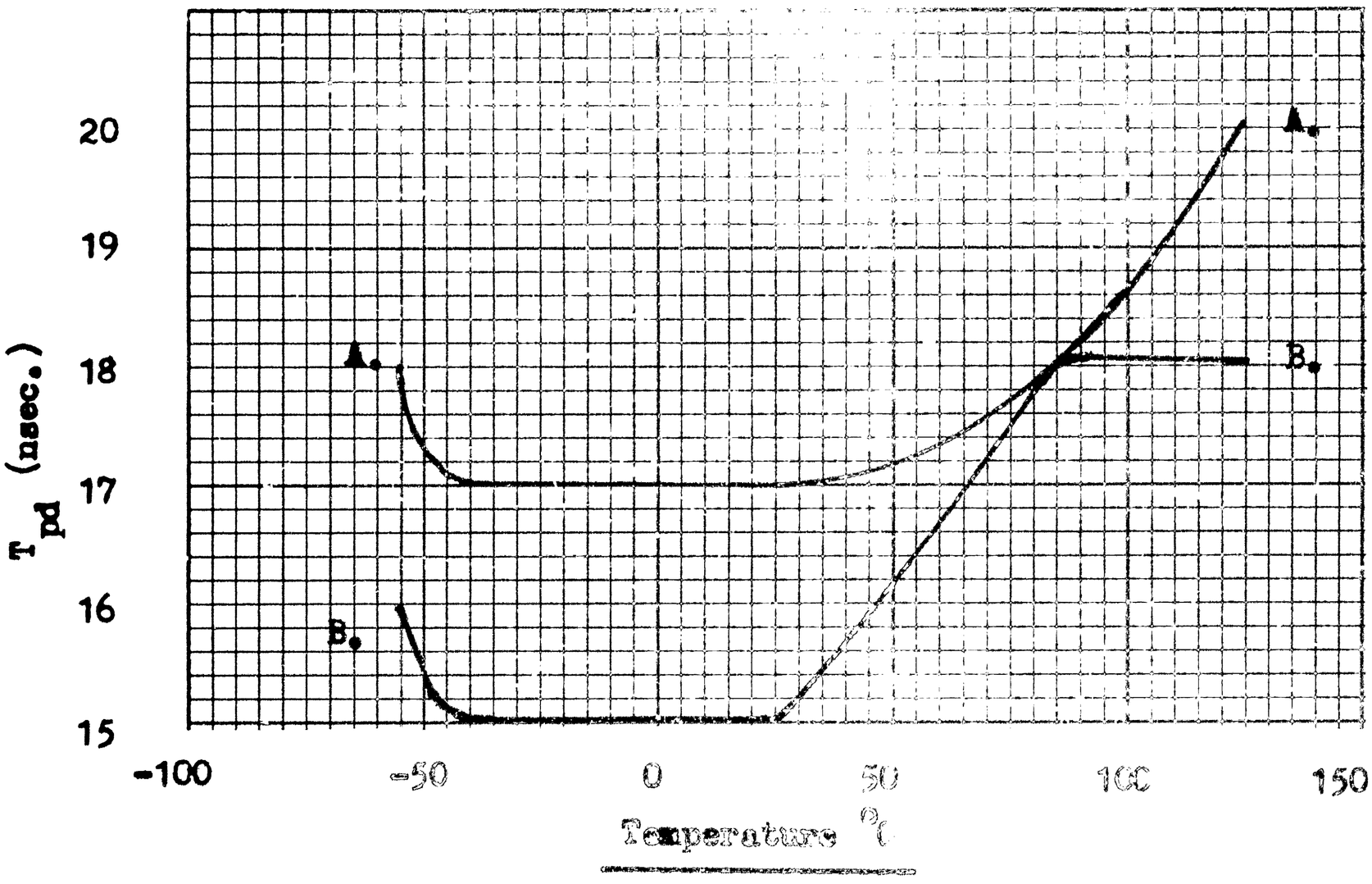
*Measured from 90% to 20% instead of 90% to 10%. (The larger measurement is from 90% to 10%.)

Circuit SNG 20	Supply Voltage 5.0				Frequency = 6 mc. Fan-in 1							
Temperature:	-55°C				-40°C				+25°C			
Lead	1	1	20	20	1	1	20	20	1	1	20	20
Test Circuit	input	output	input	output	input	output	input	output	input	output	input	output
Pulse Amplitude (V_{pp})	3.3	3.0	3.3	2.9	3.4	3.1	3.4	3.0	3.5	3.3	3.5	3.1
Pulse Width (ns.)	50	51	50	50	50	53	50	52	50	58	50	58
T_r (ns.)	5.0	18	5.0	25	5.0	18	5.0	24	7.0	21	8.0	23
T_f (ns.)	6.0	9.0	6.0	14	5.0	8.0	5.0	13	4.0	6.0	4.0	9.0
T_d (ns.)		13		13		12		12		11		11
T_s (ns.)		13		11		12		11		13		14
T_{pd} (ns.)		16		18		15		17		15		17
Temperature:	+85°C				+125°C							
Lead	1	1	20	20	1	1	20	20				
Test Circuit	input	output	input	output	input	output	input	output				
Pulse Amplitude (V_{pp})	3.6	3.7	3.8	3.6	3.8	3.9	3.9	3.7				
Pulse Width (ns.)	50	66	50	66	50	74	50	75				
T_r (ns.)	11	28	13	30	14	35	16	36				
T_f (ns.)	4.0	6.0	4.0	9.0	4.0	6.0	4.0	8.0				
T_d (ns.)		10		10		10		10				
T_s (ns.)		15		15		18		17				
T_{pd} (ns.)		18		18		18		20				



SNG-20
Frequency = 1 mc.
V_{cc} = 5.0 volts

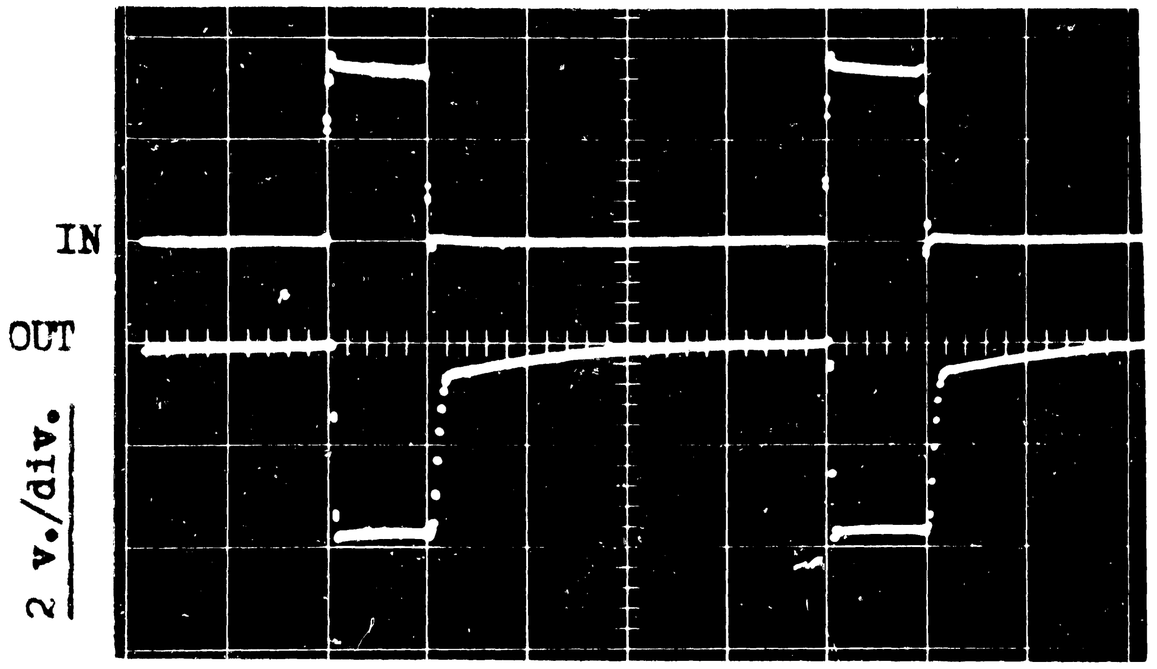
A. Load = 6
B. Load = 1



SNG-20
Frequency = 6 mc.
V_{cc} = 5.0 volts

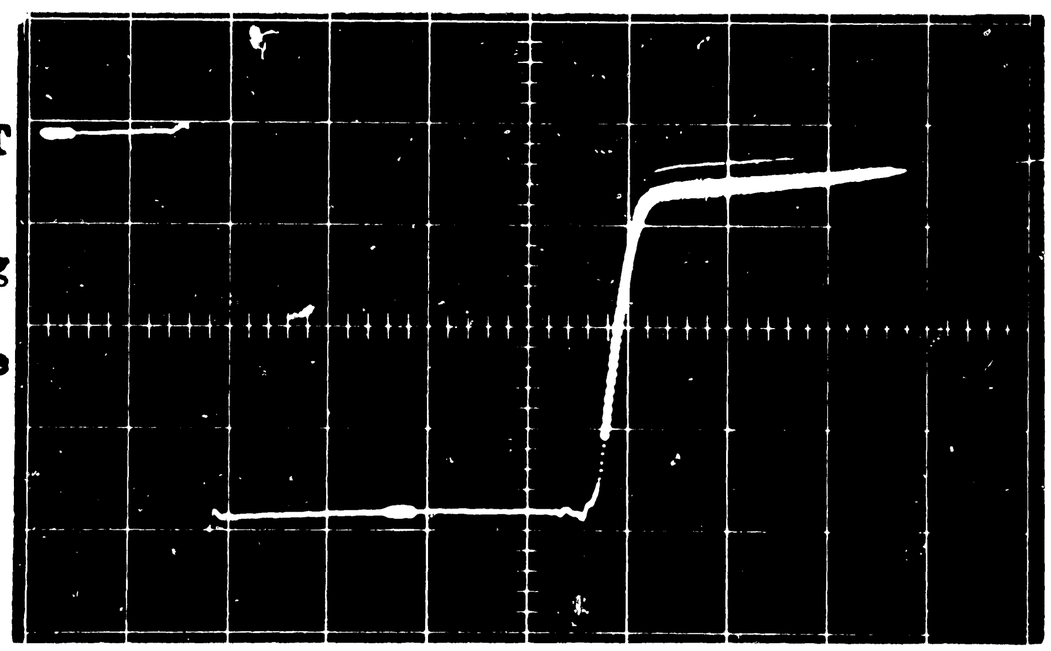
A. Load = 20
B. Load = 1

SNG-20
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.



.2 μsec./div.

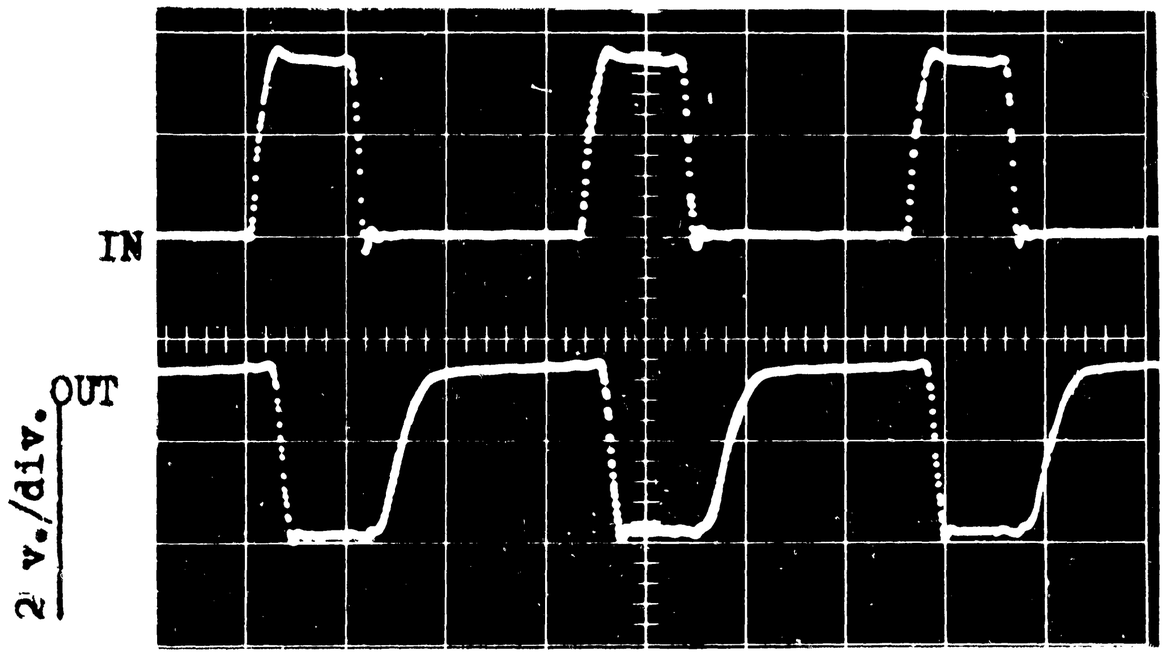
SNG-20
Frequency = 1 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.
Intensified zone showing 90% to 10% measurement of rise time on negative going output pulse.
The 90% to 20% measurement was also given since the intensified zone extended over the knee of the rise time.



50 nsec./div.

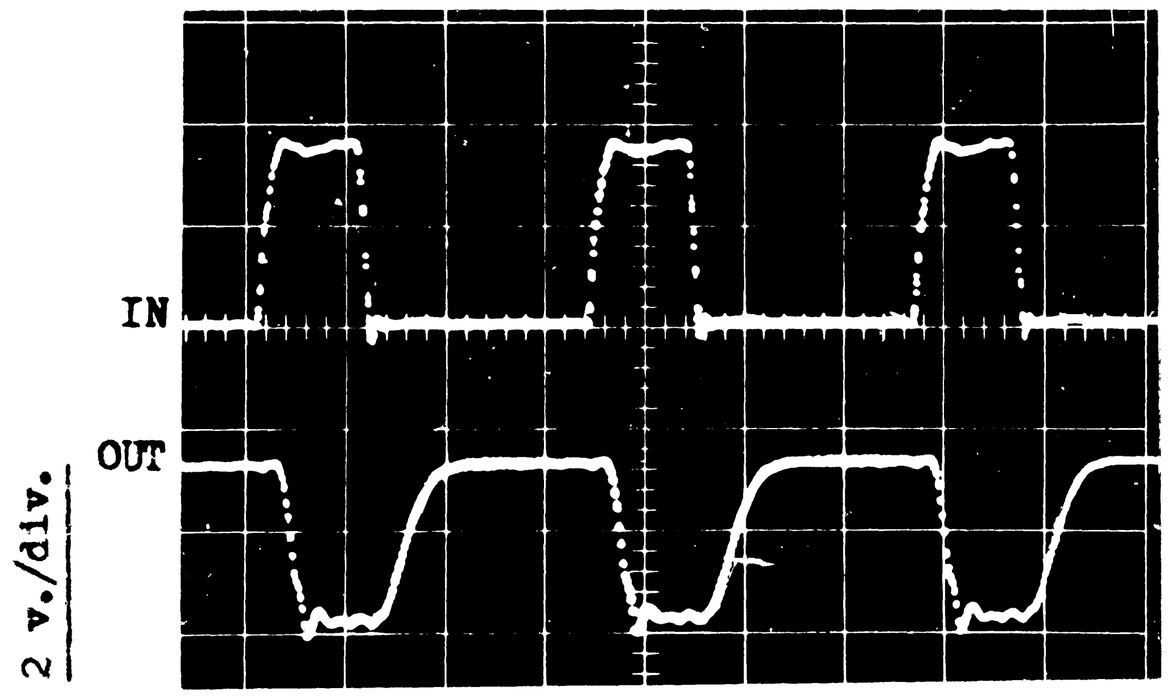
The 90% to 20% reading was much smaller than the 90% to 10% reading.

SNG-20
Frequency = 6 mc.
Load = 1 ckt.
V_{cc} = 5.0 volts
Temperature = 25°C.

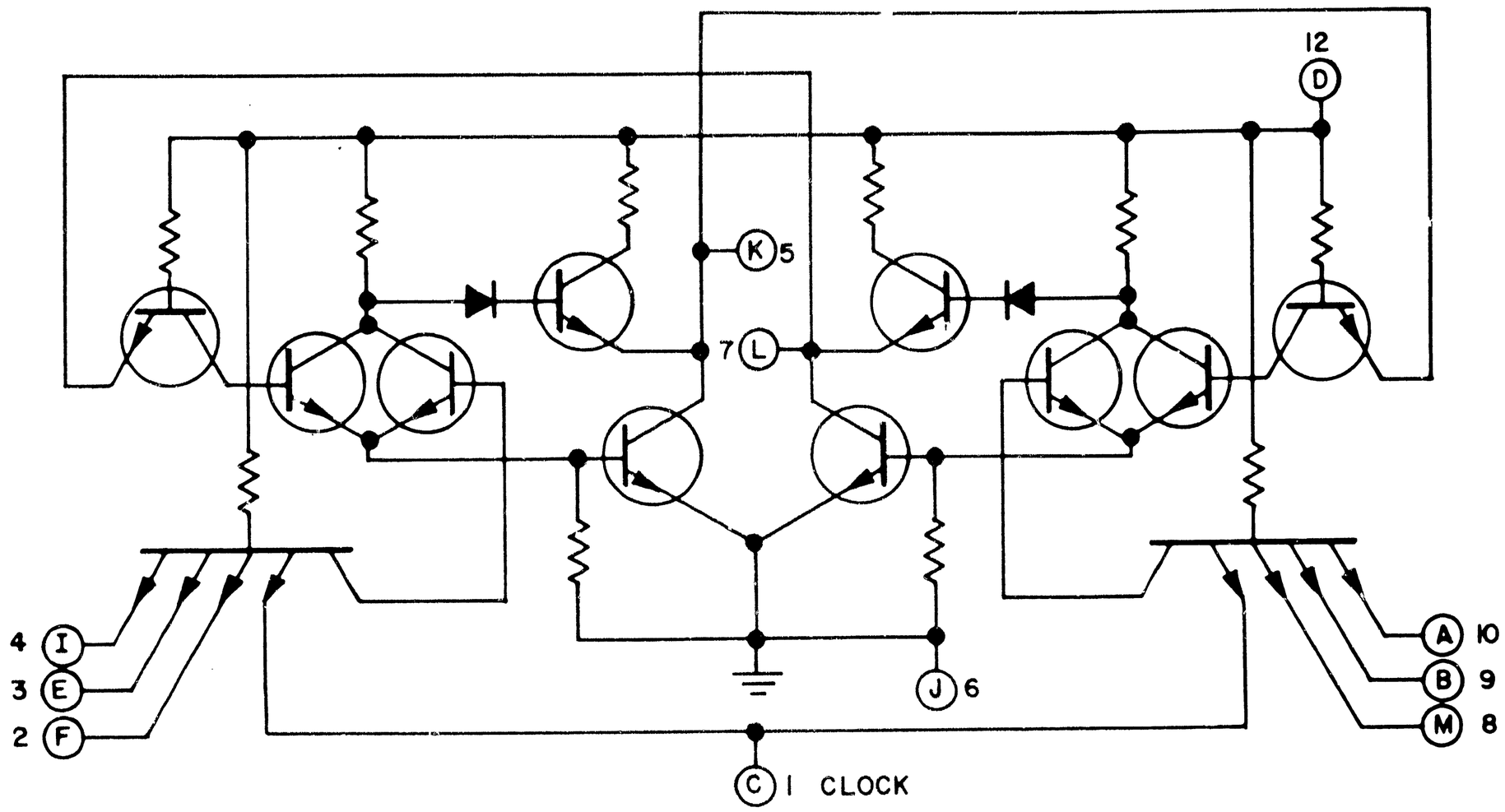


50 nsec./div.

SNG-20
Frequency = 6 mc.
Load = 6 ckts.
V_{cc} = 5.0 volts
Temperature = 25°C.



50 nsec./div.



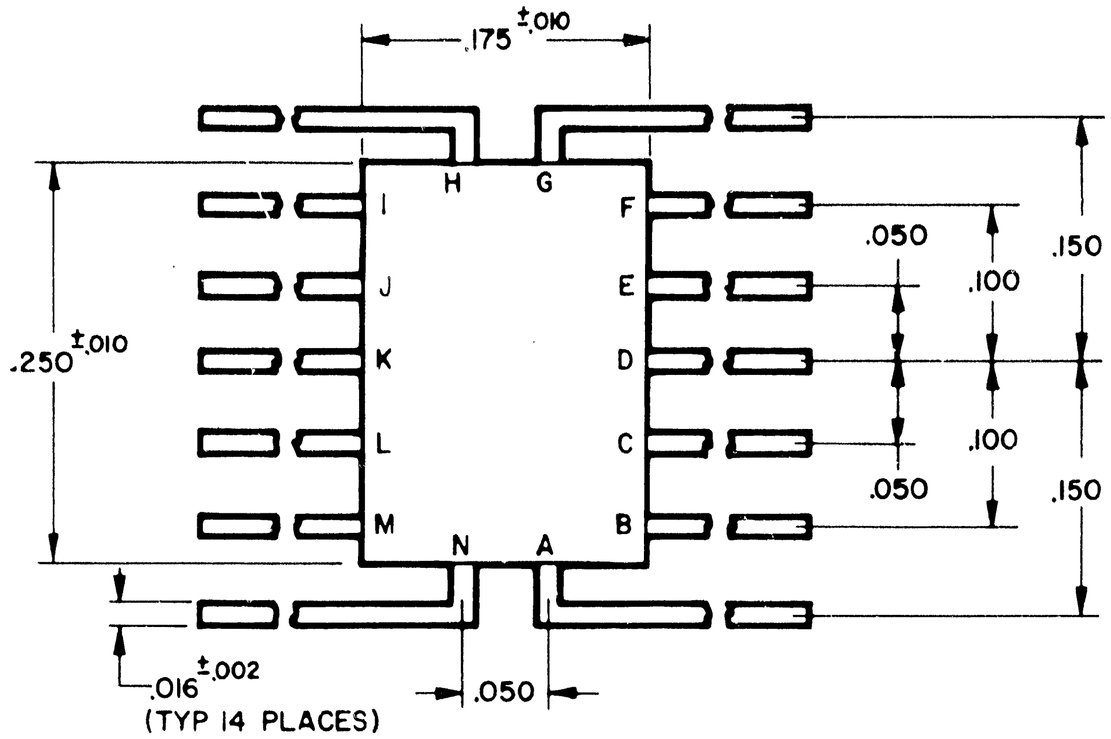
SFF 2A & B

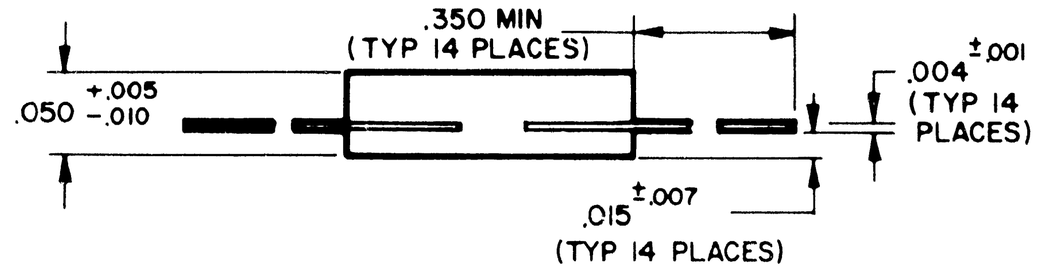
(+) LOGIC	(−) LOGIC
$\bar{K} = E \cdot F \cdot I \cdot C + L$	$K = \bar{E} \cdot \bar{F} \cdot \bar{I} \cdot \bar{C} = \bar{L}$
$\bar{L} = A \cdot B \cdot M \cdot C + K$	$L = \bar{A} \cdot \bar{B} \cdot \bar{M} \cdot \bar{C} + \bar{K}$

SET-RESET TRIGGER FLIP-FLOP

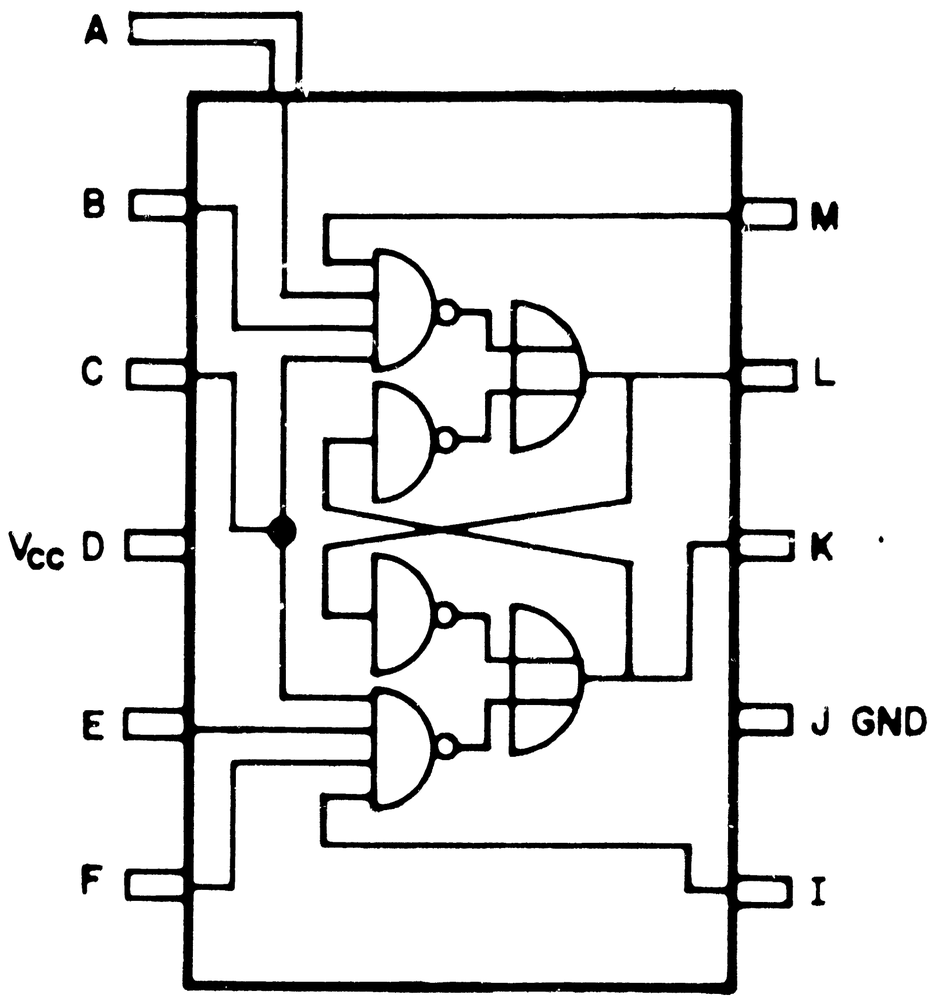
The SFF-2B set-reset two phase trigger flip-flop is made up of two AND-NOR gates interconnected to operate in the set-reset-trigger flip-flop mode. The circuit is manufactured with planar epitaxial techniques and is constructed on a monolithic silicon substrate.

There are two versions of the SFF-2 flip-flop; the "A" version has two inputs on each side, while the "B" version has three inputs on each side. Both of these circuits require only one power supply.

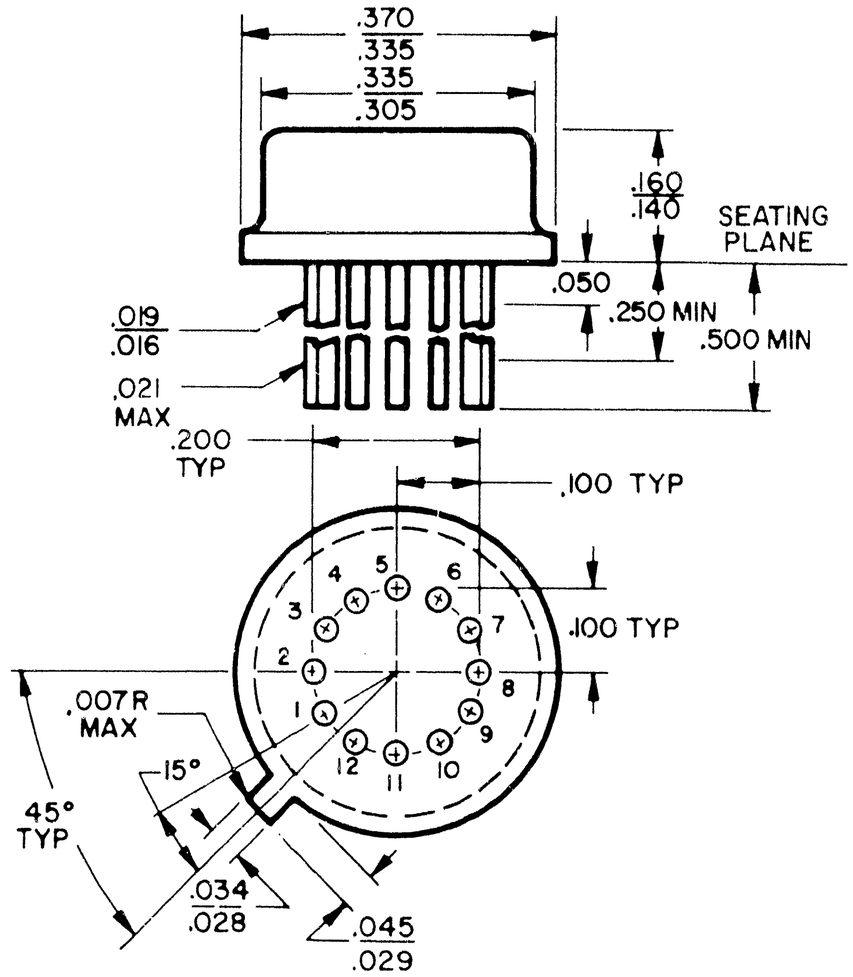




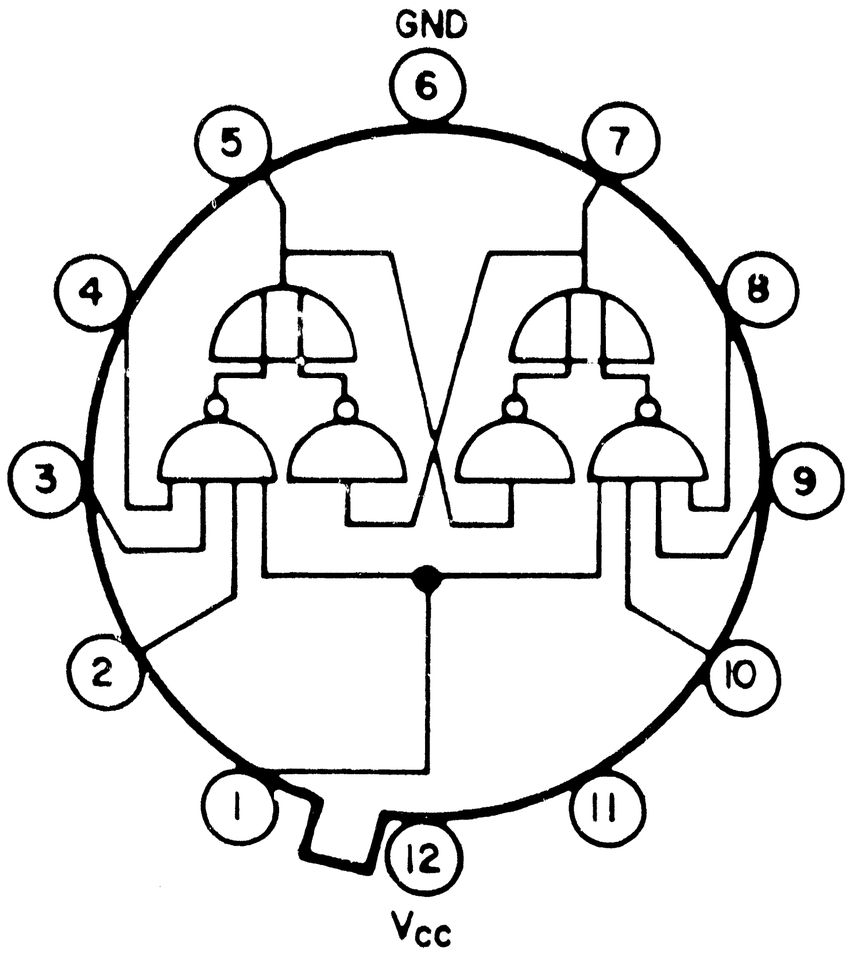
14 LEAD FLAT PACK



TOP VIEW



12 LEAD TO-5

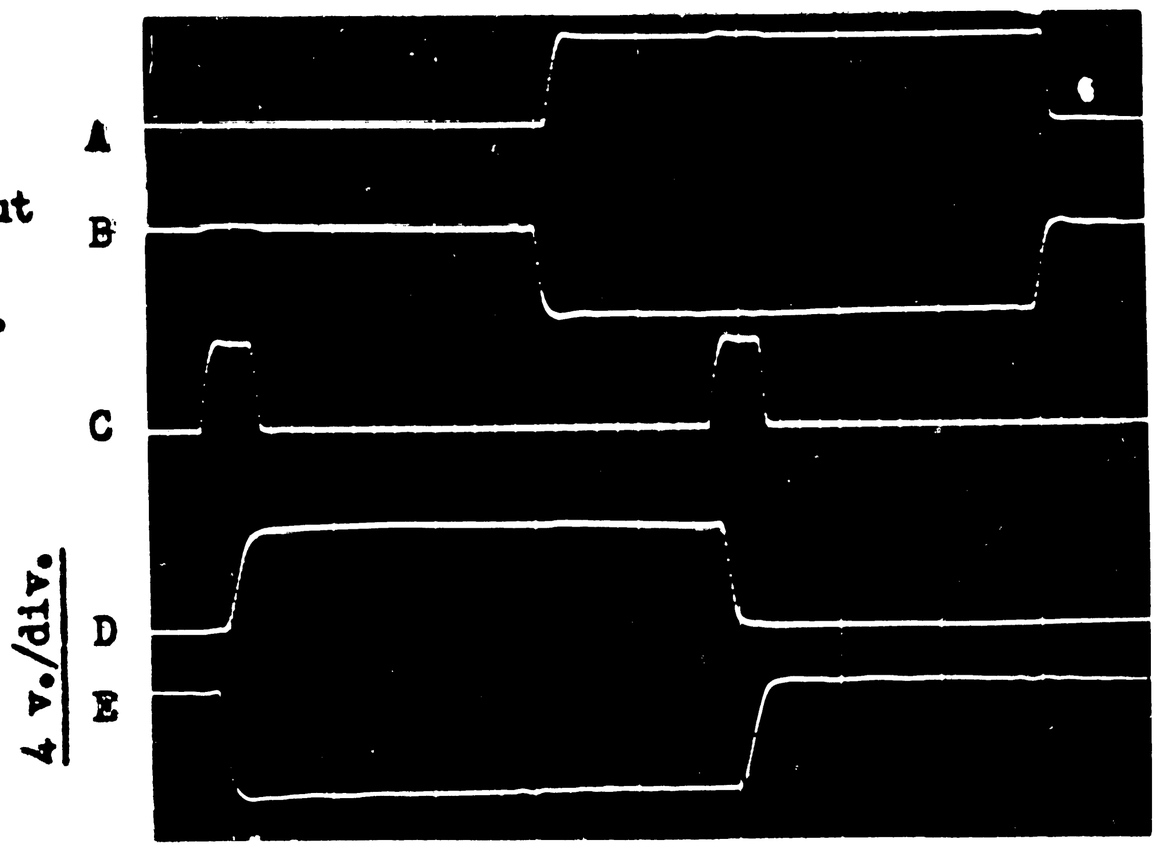


BOTTOM VIEW

SFF - 2B

FOR SFF-2A INPUTS 9-A AND 4-I ARE NOT PRESENT

SFF-2B
Input freq.= 1 mc.
Clock freq.= 2 mc.
Load = 1 ckt./output
V_{cc} = 5.0 volts
Temperature = 25°C.
A. = #3 input
B. = #9 input
C. = Clock Input
D. = #5 output
E. = #7 output



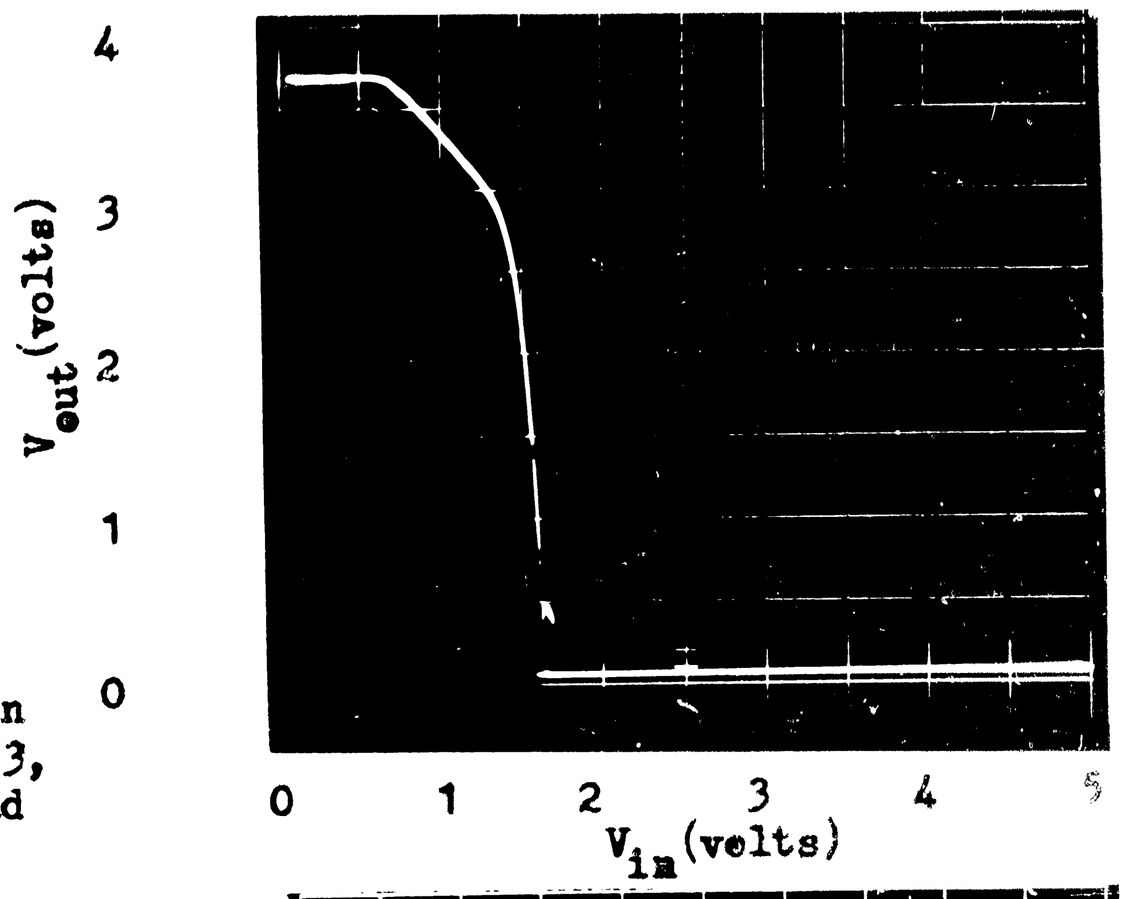
.1 μsec./div.

V_{in} vs. V_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Output taken on pin #5 with pins #1,2,3, and 4 connected and V_{in} applied to the same.

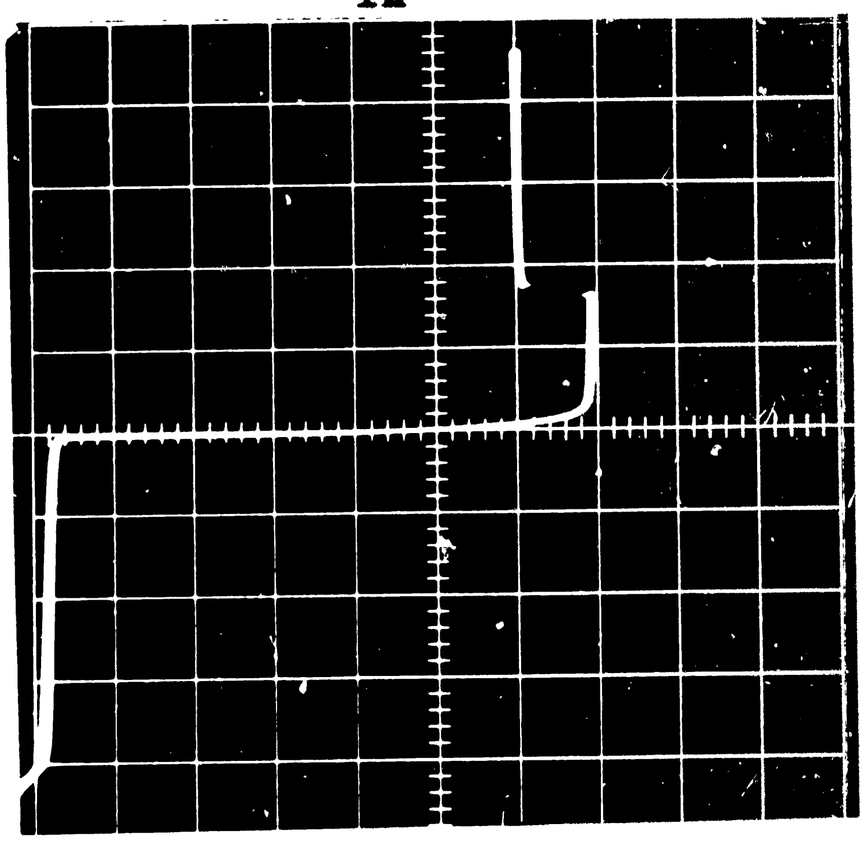


V_{in} vs. I_{in}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Pin #1 grounded.

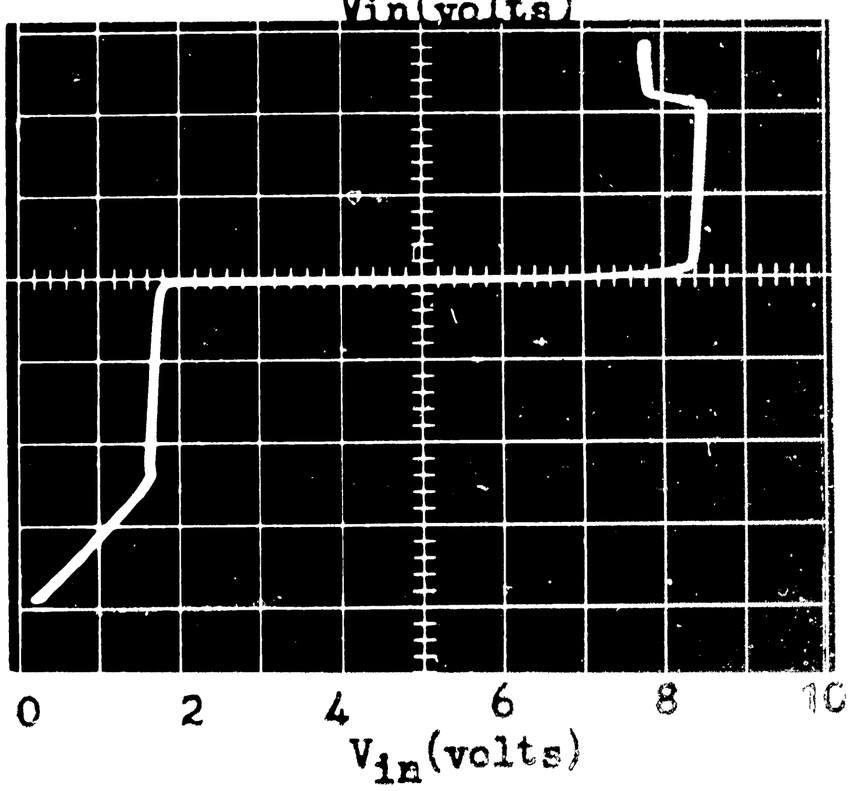


V_{in} vs. I_{in}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) Pin #1 high.

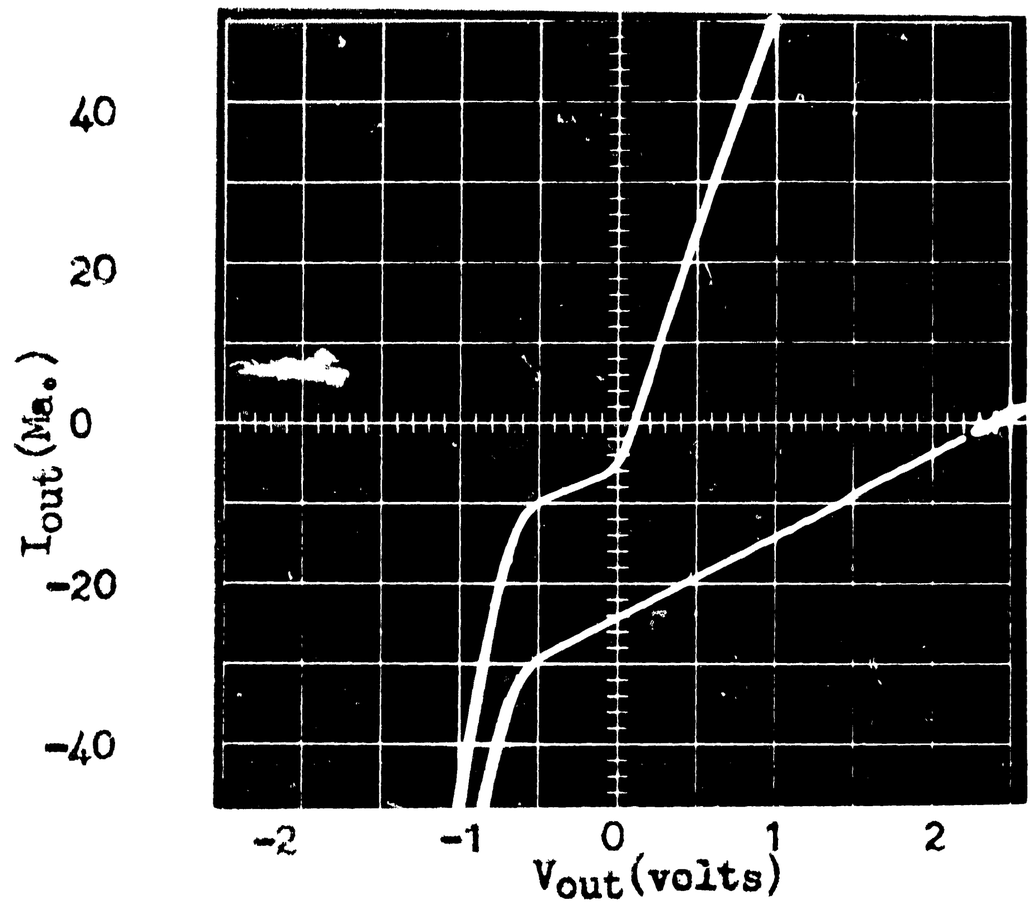


V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

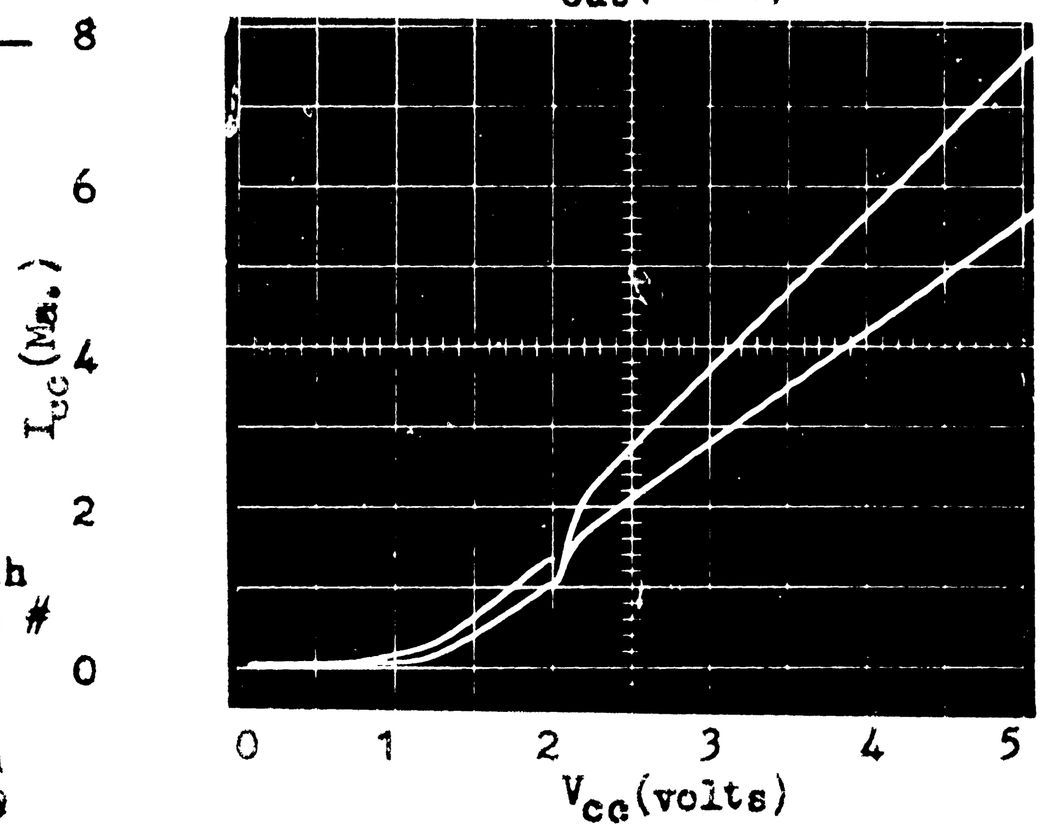
3.) Top trace is with pin #1 @ ground bottom trace is with Pin #1 high.



V_{cc} vs. I_{cc}

1.) T = 25°C

2.) Top trace ending with 7.6 ma. is with pins # 1,2,3,and 4 high. Bottom trace ending with 5.6 ma. is with pins #1,2,3, and 4 @ ground.

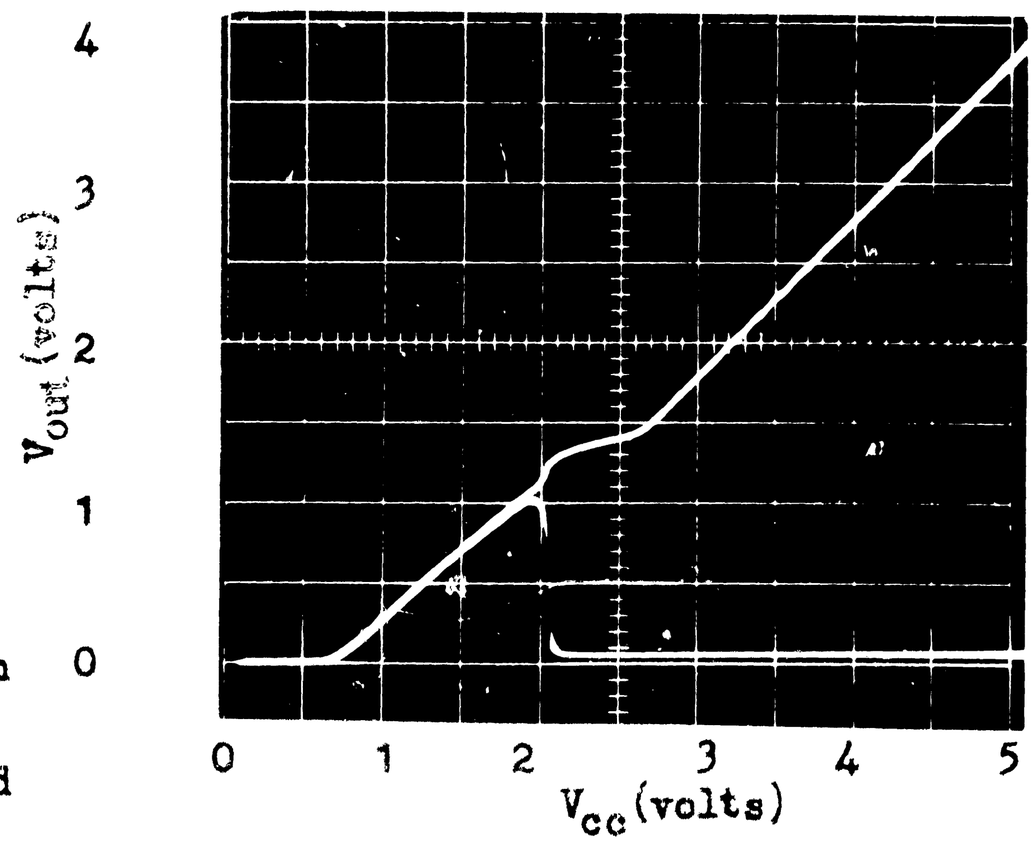


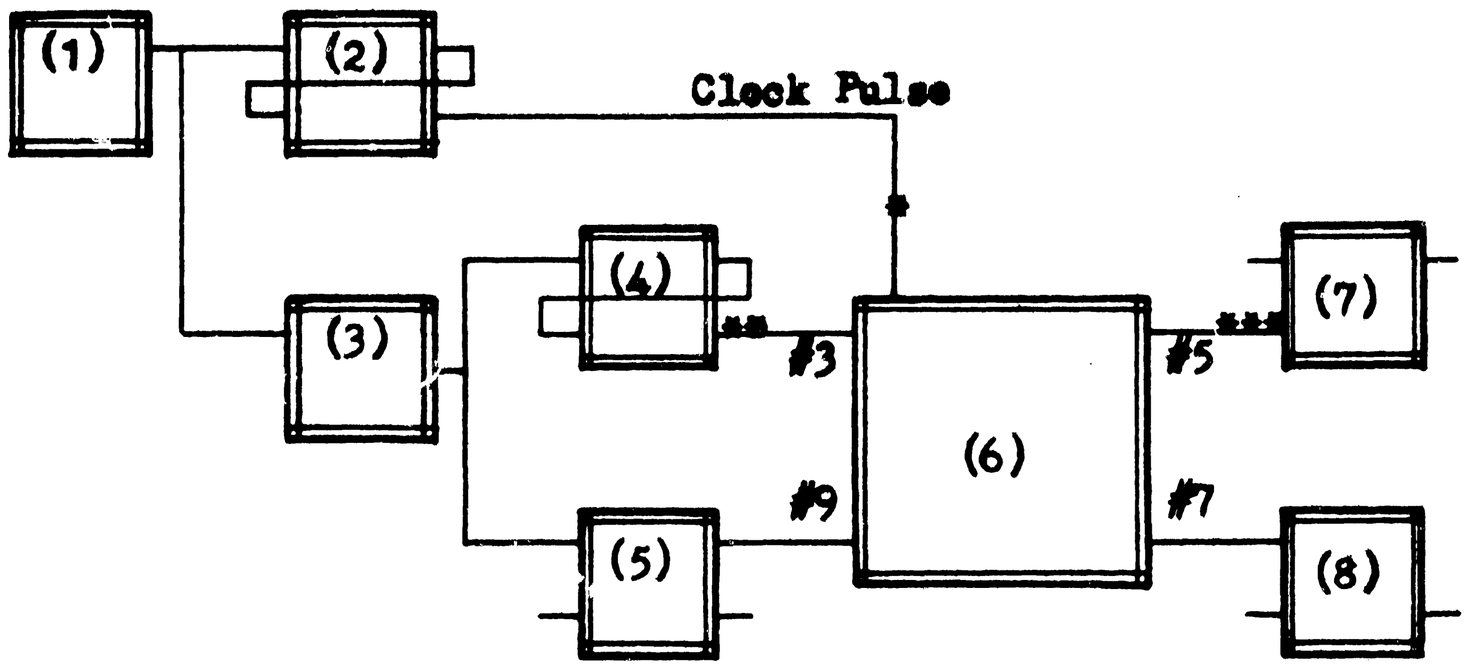
V_{cc} vs. V_{out}

1.) T = 25°C

2.) Top trace is with pin #1 high, and bottom trace is with pin #1 @ ground.

3.) Pin #3 @ ground, and output on pin #5.





Typical Test Set-up For SFF -2B Flip-Flop

1. Pulse Generator
2. Dual Driver (Clock) SNG-4B
3. Pulse Envelope Generator (Frequency divider)
4. Dual Driver (Input) SNG-4B
5. Driver (Alternate Input) SNG-4B
6. SFF-2B Test Circuit (Flip-Flop)
7. Load = 1 SNG-4B
8. Load = 1 SNG-4B

Clock Frequency = 2 mc.

Logic Inputs = 1 mc.

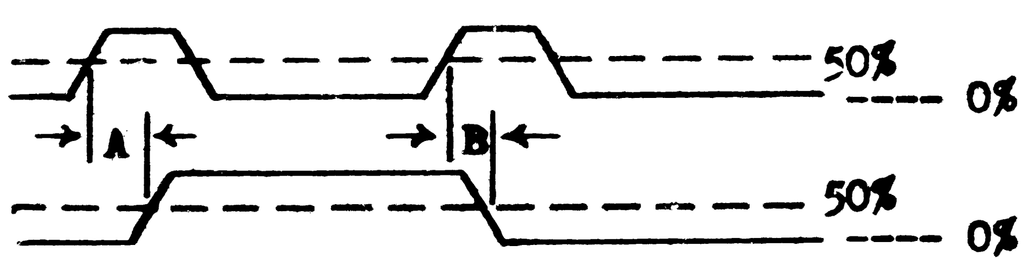
Set-up Drawn Without V_{cc} and Ground For Simplicity.

Clock gate, Input gates, Test circuit, and Load circuits were inside of the temperature chamber.

* Clock Input Monitor
** Logic Input Monitor
*** Logic Output Monitor

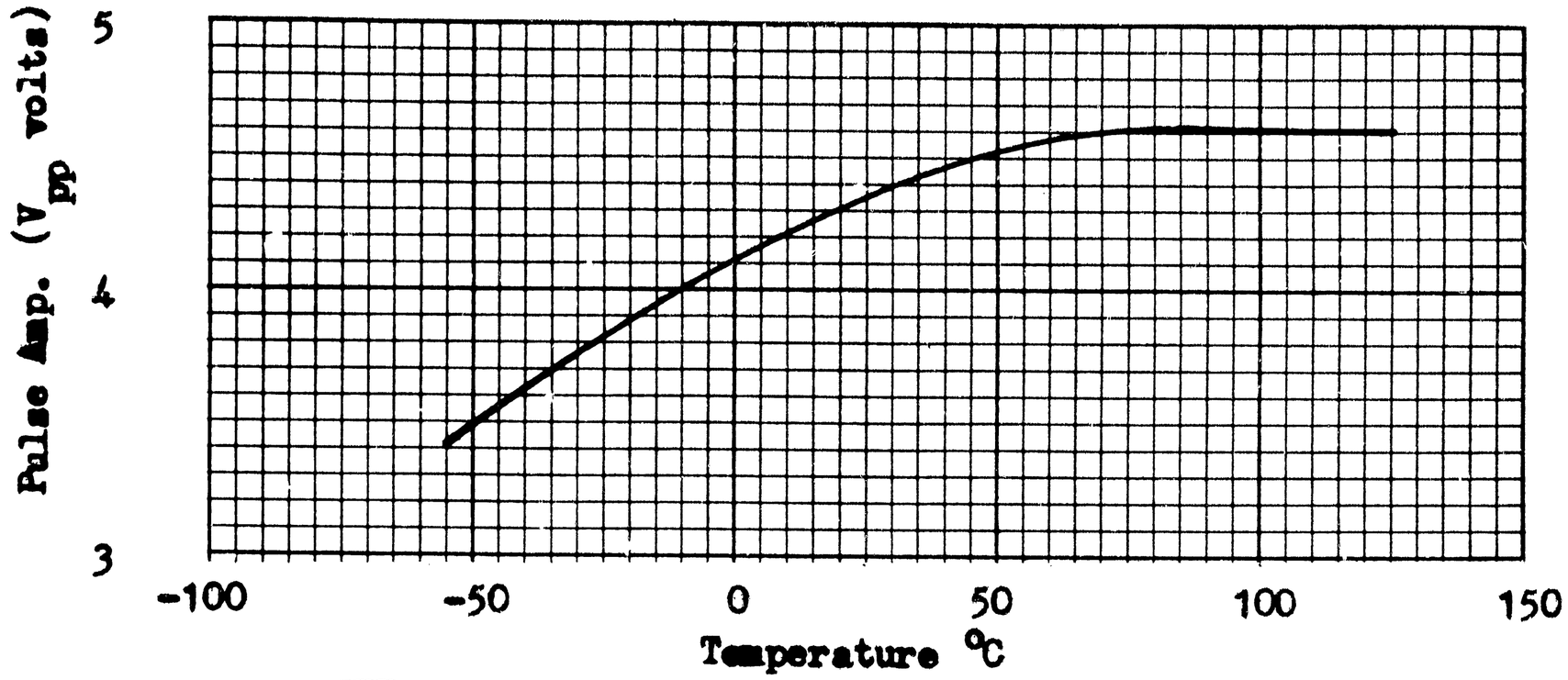
SFF 2B Input = 1 mc. Clock = 2 mc. Fan-in = 1 ckt. Load = 1 ckt./output

Temperature °C	-55			-40			+25			+85			+125		
Vcc	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5
Input #3															
Pulse Amp.	2.8	3.3	3.8	2.8	3.4	3.9	3.1	3.6	4.1	3.4	3.8	4.4	3.5	4.0	4.6
Pulse Width	497	497	499	497	498	499	500	500	502	500	502	503	504	504	507
T_r	6.0	8.0	8.0	7.0	8.0	9.0	10	11	12	15	17	18	20	22	24
T_f	10	9.0	7.0	9.0	8.0	6.0	7.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0
Clock Pulse															
Pulse Amp.	2.8	3.2	3.6	2.8	3.2	3.9	2.9	3.5	3.9	3.1	3.6	4.1	3.1	3.7	4.1
Pulse Width	55	53	51	54	52	50	51	50	49	50	50	49	50	49	48
T_r	7.0	8.0	8.0	6.5	7.0	7.0	9.0	10	11	11	12	13	15	16	16
T_f	12	10	9.0	10	9.0	7.0	7.0	7.0	7.0	6.0	6.0	5.0	7.0	6.0	5.0
Output #5															
Pulse Amp.	2.7	3.4	3.8	2.8	3.7	4.0	3.2	4.3	4.6	3.8	4.6	4.8	3.8	4.6	4.8
Pusle Width	492	490	489	492	487	486	487	486	484	480	480	480	480	477	477
T_r	13	13	14	13	13	14	20	21	21	21	22	23	25	26	27
T_f	12	12	11	12	11	9.0	12	12	11	11	9.0	8.0	10	8.0	8.0
T_1	31	30	26	30	30	26	33	31	31	33	33	31	35	35	33
T_2	24	20	15	22	19	14	20	15	14	15	14	10	12	11	9.0

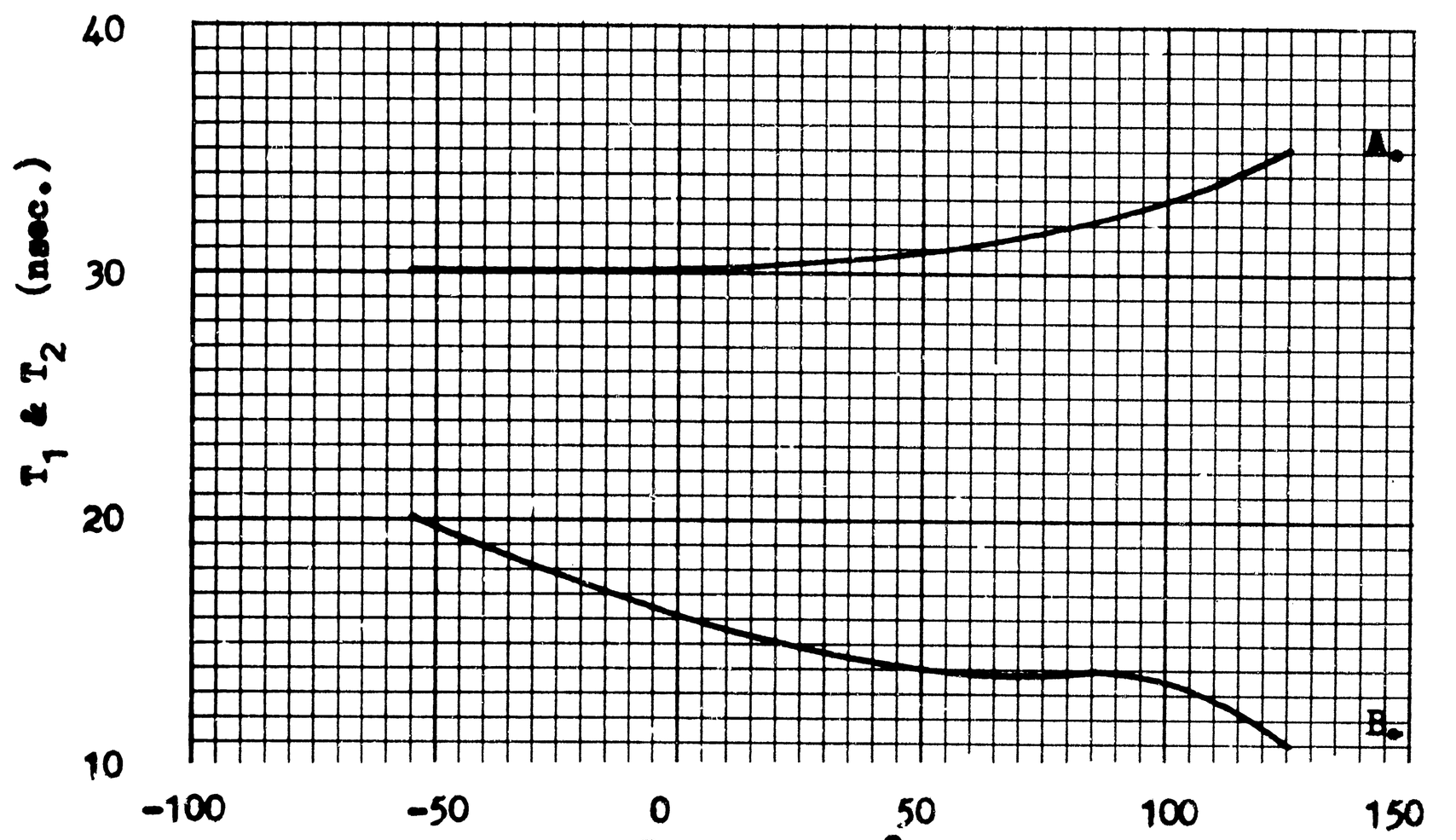


Clock Pulse $A = T_1$

Output Pulse $B = T_2$



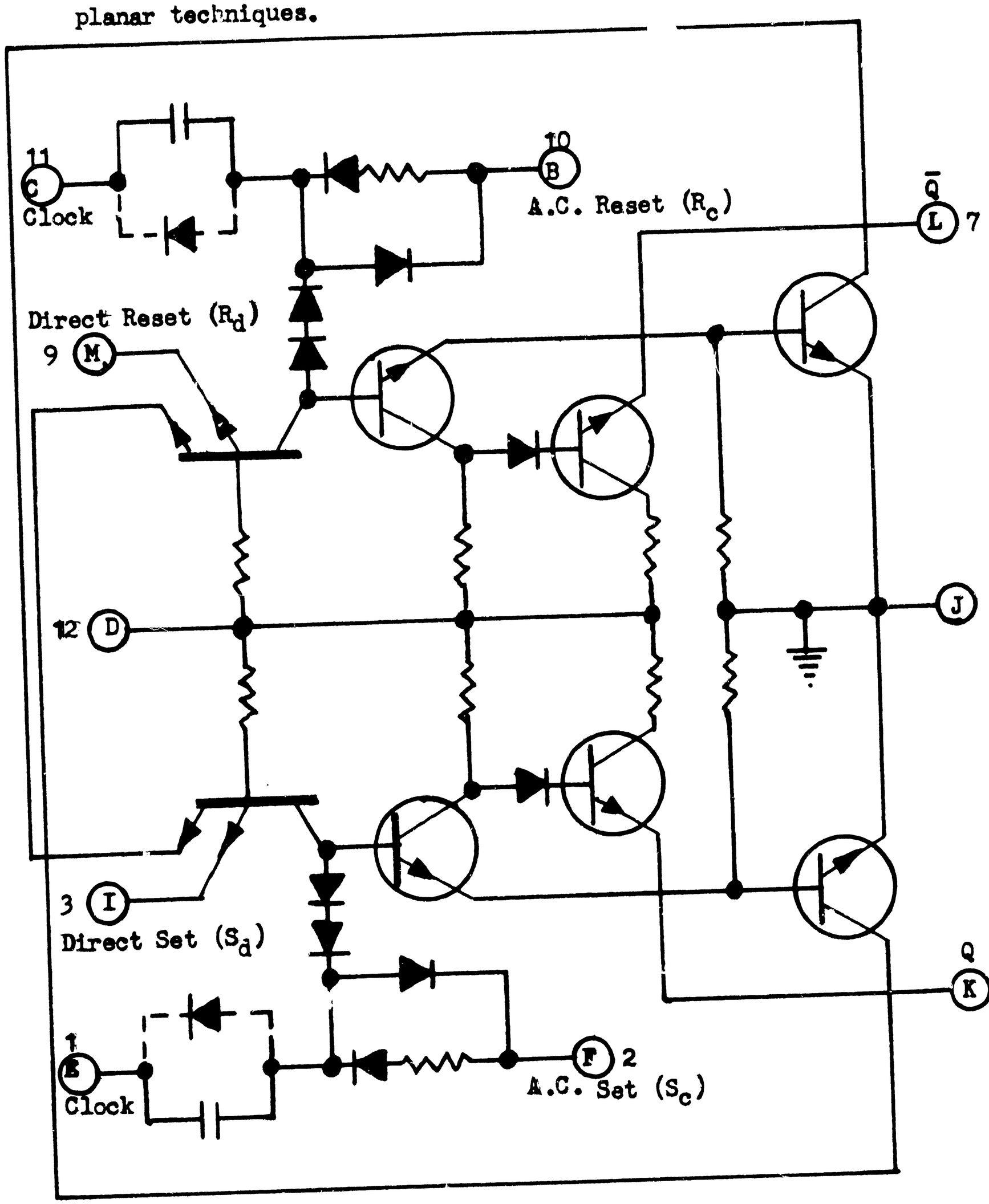
SFF-2B
Input Frequency = 1 mc.
Clock Frequency = 2 mc.
Load = 1 ckt./output
V_{cc} = 5.0 volts



SFF-2B
Input Frequency = 1 mc.
Clock Frequency = 2 mc.
Load = 1 ckt./output
V_{cc} = 5.0 volts

A. = T_1
B. = T_2

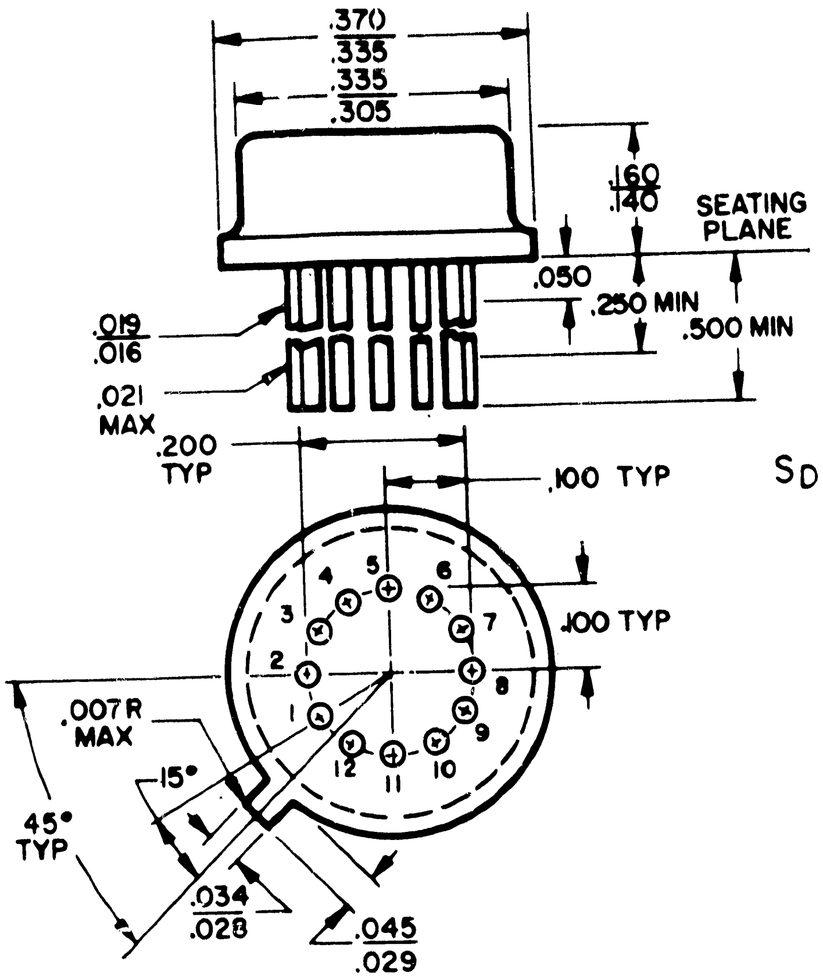
The SFF-3A is a single phase flip-flop constructed on a monolithic silicon substrate and manufactured by epitaxial planar techniques.



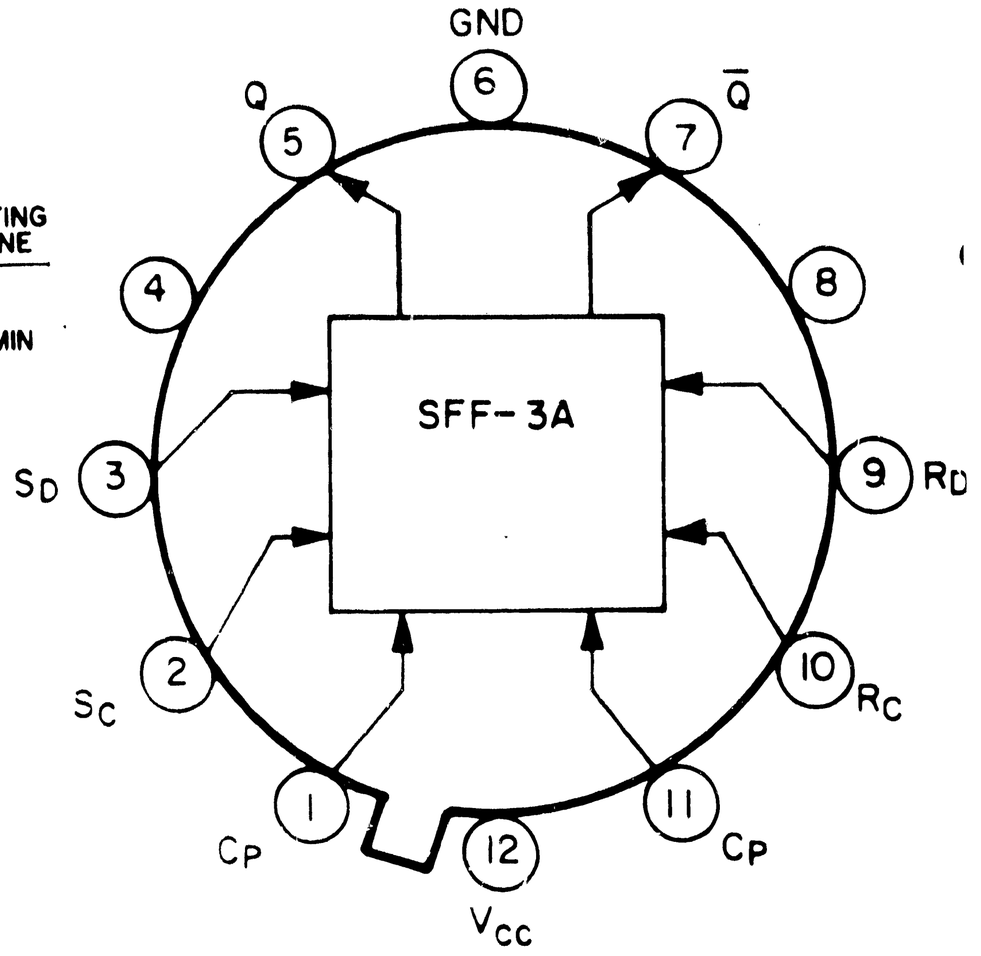
SFF-3A

SET-RESET TRIGGER FLIP-FLOP

Circuit operation requires a single power supply of 8.0 v. max.

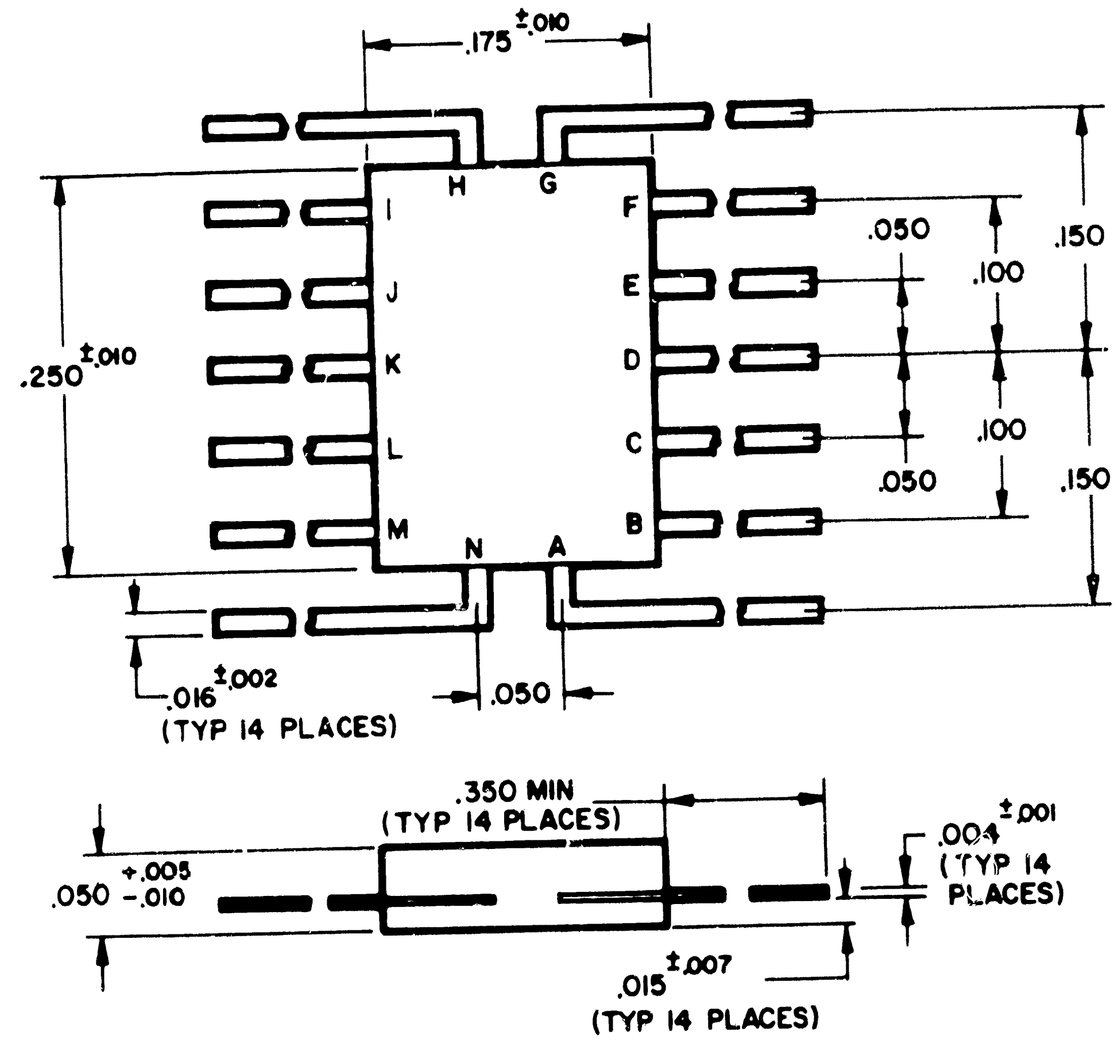


12 LEAD TO-5



TO-5 BOTTOM VIEW

The circuit consists of a dual Nand/Nor element with reactance coupled pulse level trigger inputs interconnected to operate in the set-reset-trigger flip-flop mode.



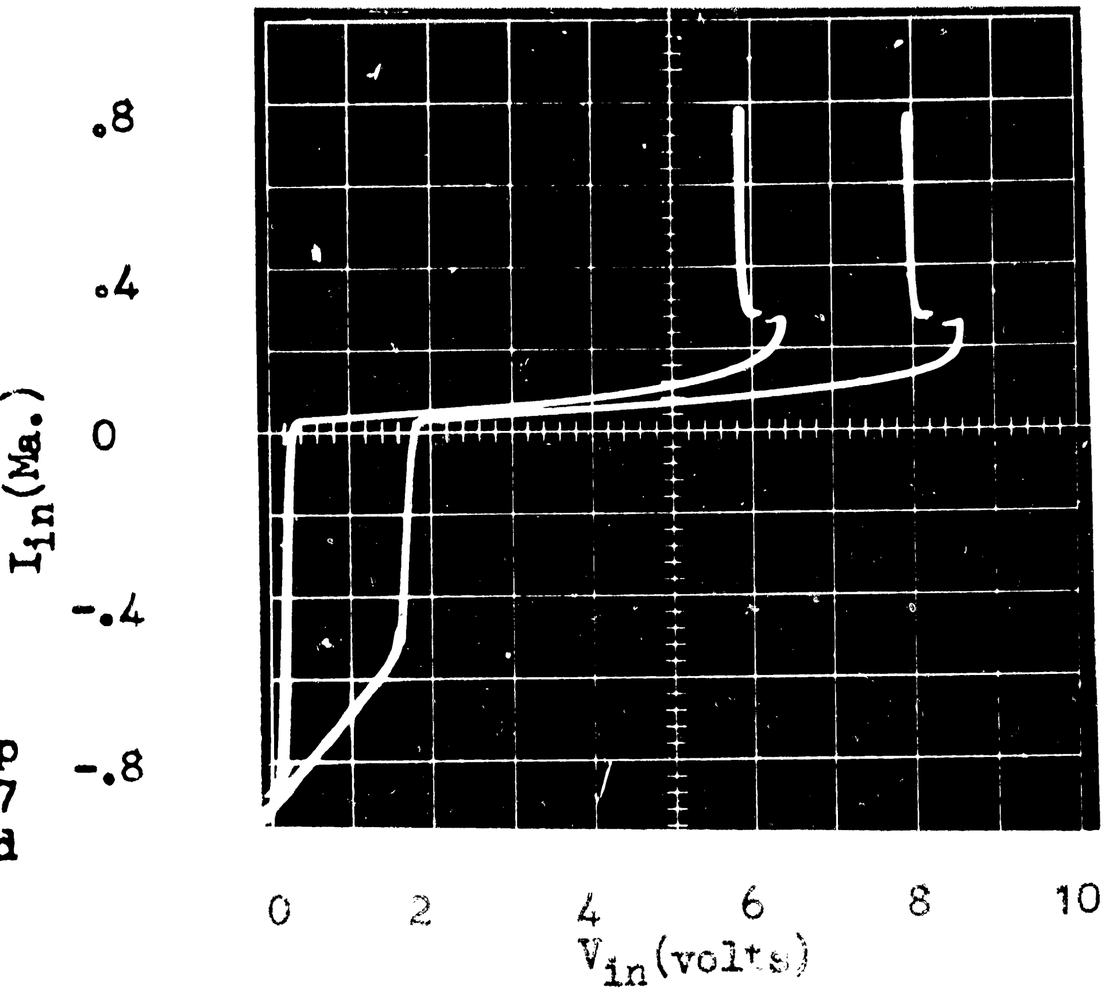
14 LEAD FLAT PACK

V_{in} vs. I_{in}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) The left-hand or top trace is with pin #7 high. The right-hand or bottom trace is with pin #7 low.

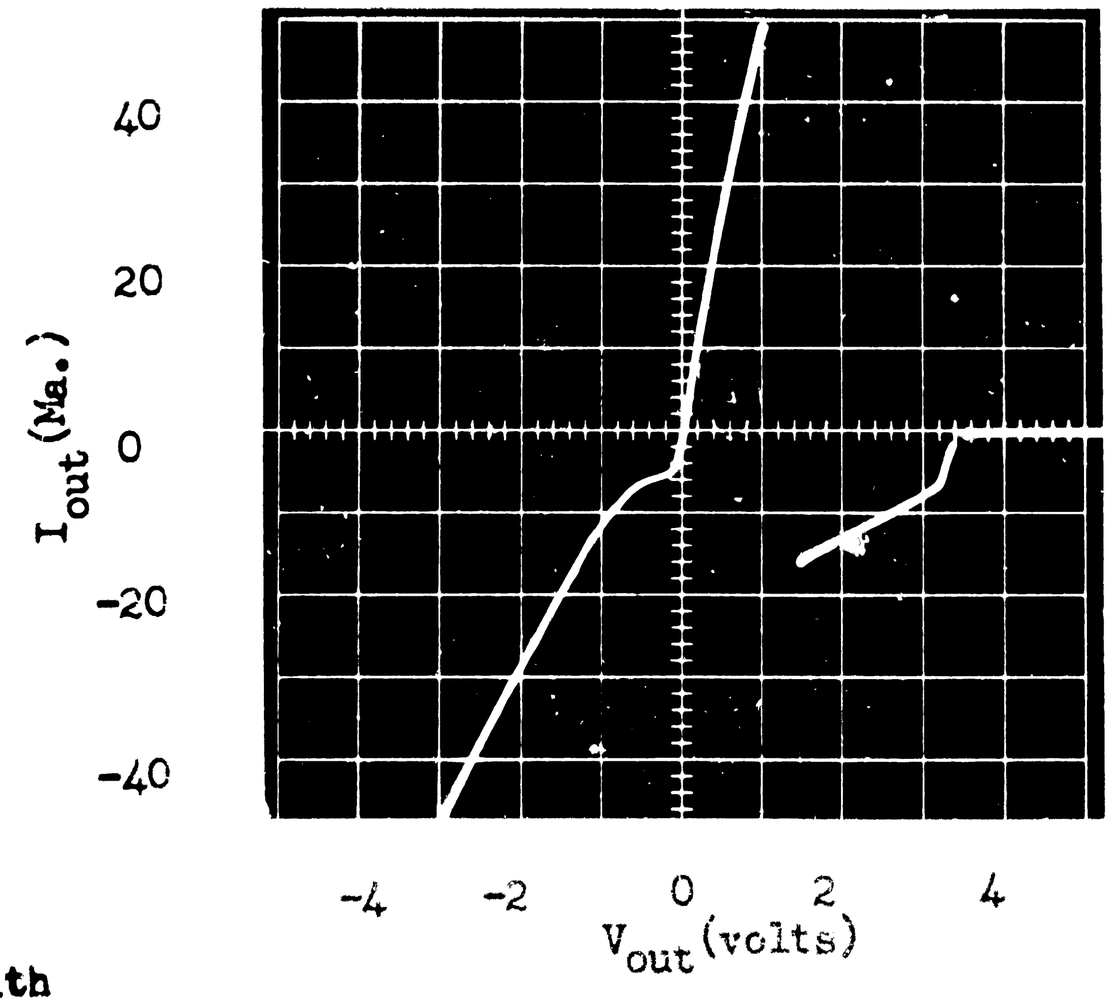


V_{out} vs. I_{out}

1.) T = 25°C

2.) V_{cc} = 5 v.

3.) The left-hand or top trace is with the output transistor "on", and the right-hand or bottom trace is with the output transistor "off".

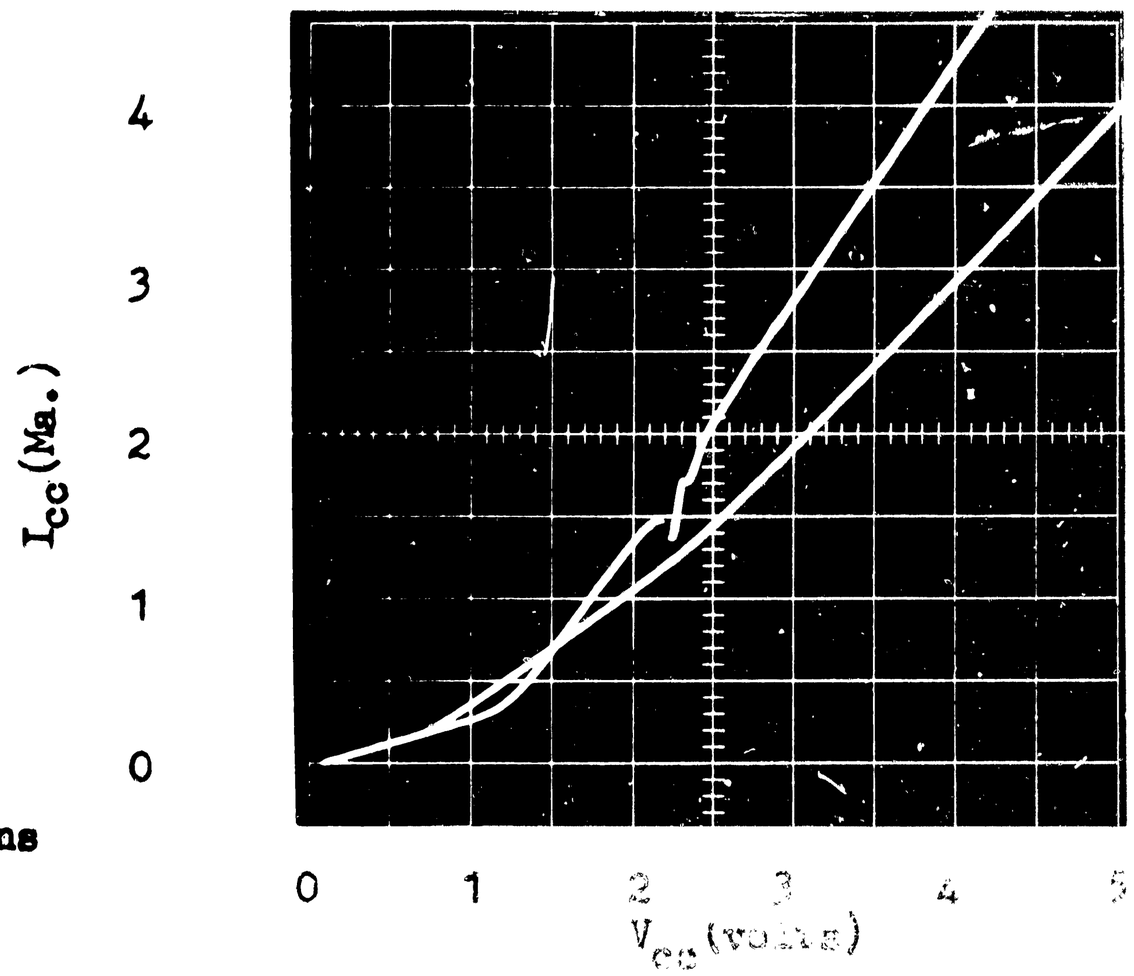


V_{cc} vs. I_{cc}

1.) T = 25°C

2.) Pins #1 &#11 @ ground for both traces.

3.) Top trace with pins #9 & #3 open, and bottom trace with pins #9 & #3 at ground level.

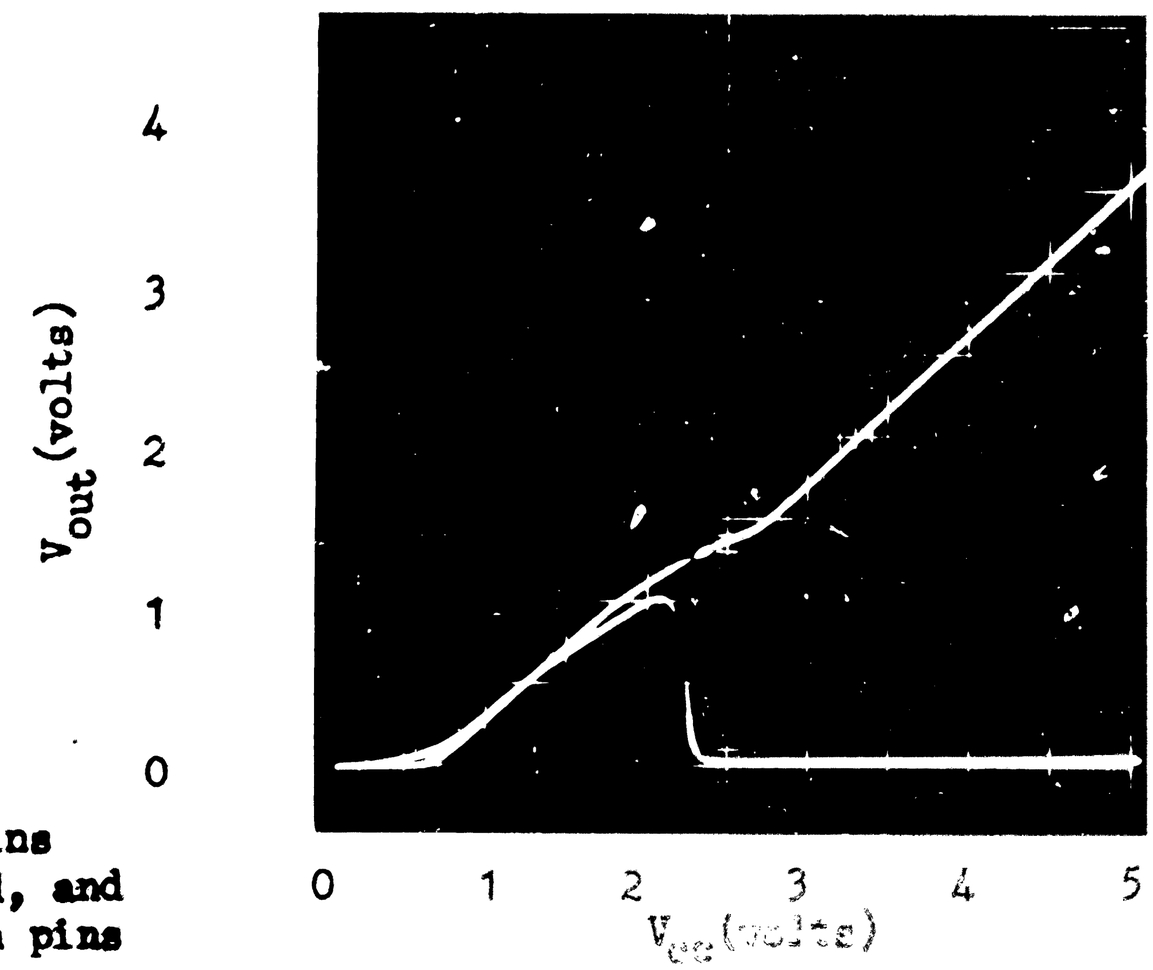


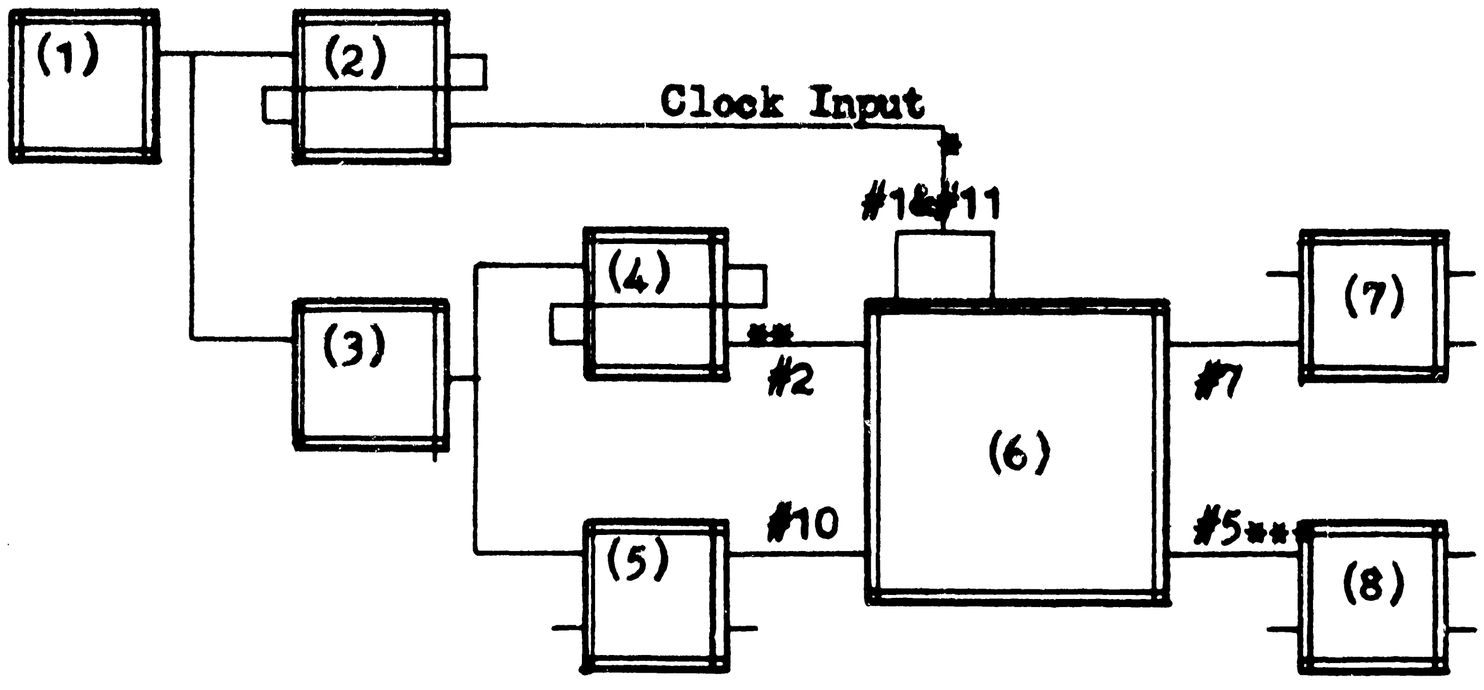
V_{cc} vs. V_{out}

1.) T = 25°C

2.) Pins #1 & #11 at ground for both traces.

3.) Top trace with pins #7 & #10 grounded, and bottom trace with pins #2 & #5 grounded.





Typical Test Set-up For SFF -3A Flip-Flop

1. Pulse Generator
2. Dual Driver (Clock) SNG-4B
3. Pulse Envelope Generator (Frequency divider)
4. Dual Driver (Input) SNG-4B
5. Driver (Alternate Input) SNG-4B
6. SFF-3A Test Circuit (Flip-Flop)
7. Load = 1 SNG-4B
8. Load = 1 SNG-4B

Clock Frequency = 2 mc.

Logic Inputs = 1 mc.

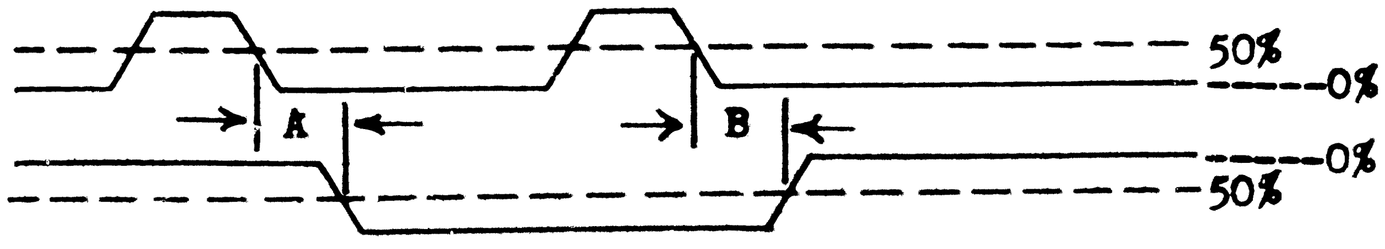
Set-up drawn without V_{cc} and ground for simplicity.

Clock gate, input gate, test circuit, and load circuits were inside of the temperature chamber.

* Clock Input Monitor
** Logic Input Monitor
*** Logic Output Monitor

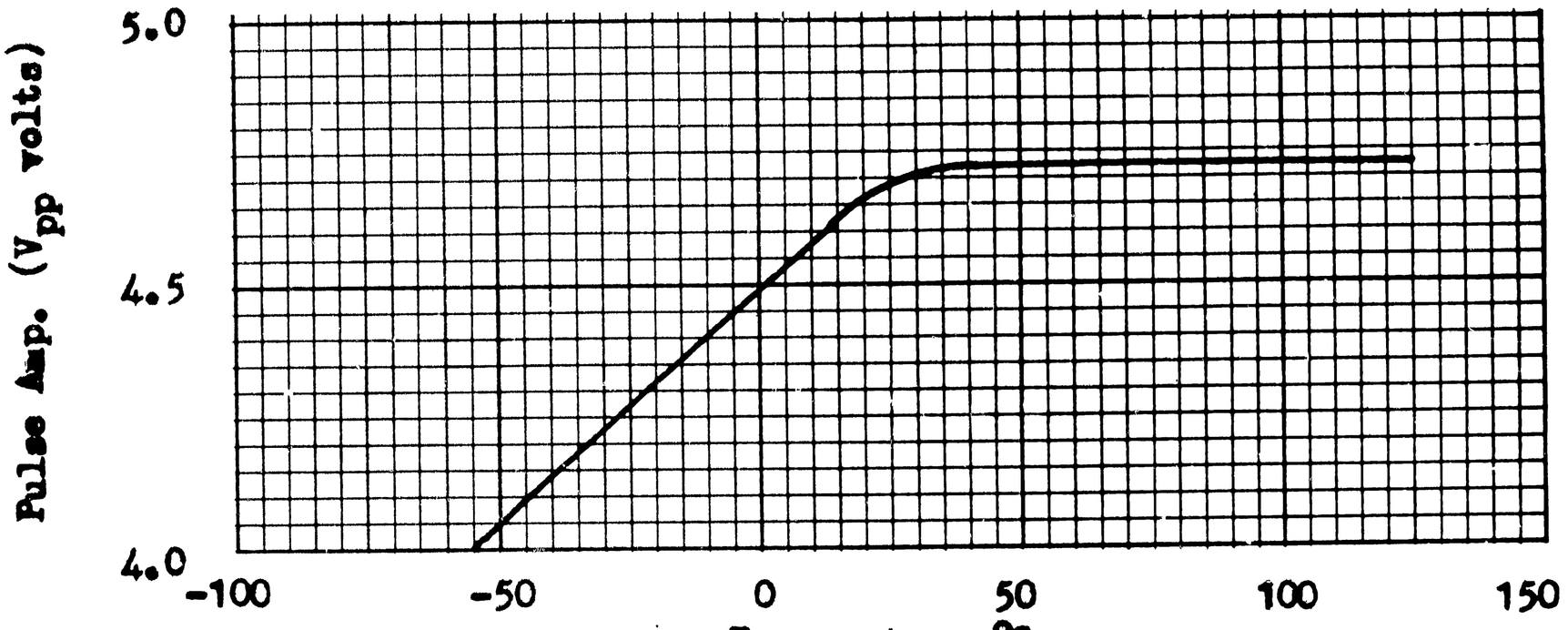
SFF 3A Input = 1 mc. Clock = 2 mc. Fan-in = 1 Load = 1 ckt./output

Temperature °C	-55			-40			+25			+85			+125		
V_{cc}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5
Input #2	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -
Pulse Amp.	2.7	3.2	3.7	2.8	3.2	3.8	3.0	3.6	4.1	3.2	3.7	4.3	3.4	3.9	4.5
Pulse Width	506	503	502	506	503	502	503	502	502	502	502	500	500	499	497
T_r	5.0	6.0	7.0	5.5	6.0	7.0	8.0	9.0	11	13	14	16	17	20	21
T_f	9.0	7.0	6.0	9.0	6.0	5.0	6.0	5.0	5.0	6.0	5.0	5.0	6.0	6.0	6.0
Clock	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -
Pulse Amp.	2.2	2.7	3.3	2.3	2.8	3.3	2.3	3.1	3.5	2.7	3.2	3.6	2.8	3.2	3.7
Pulse Width	51	49	48	51	49	49	50	50	49	50	50	49	51	49	48
T_r	12	14	17	12	15	17	17	19	22	23	24	28	27	30	32
T_f	8.0	7.0	7.0	8.0	6.0	6.0	6.0	6.0	6.0	7.0	6.0	6.0	6.0	6.0	6.0
Output #5	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -
Pulse Amp.	3.3	4.0	4.7	3.5	4.2	4.9	4.2	4.7	5.2	4.2	4.7	5.2	4.2	4.7	5.3
Pulse Width	484	489	492	488	492	494	495	498	501	502	504	507	506	509	511
T_r	14	14	17	15	17	19	23	23	24	28	29	30	34	36	37
T_f	9.0	8.0	8.0	9.0	8.0	7.0	9.0	8.0	7.0	9.0	8.0	8.0	10	9.0	8.0
T_1	29	25	21	26	22	20	22	20	18	22	20	20	23	22	22
T_2	15	15	14	14	15	15	17	18	19	22	23	25	28	29	31

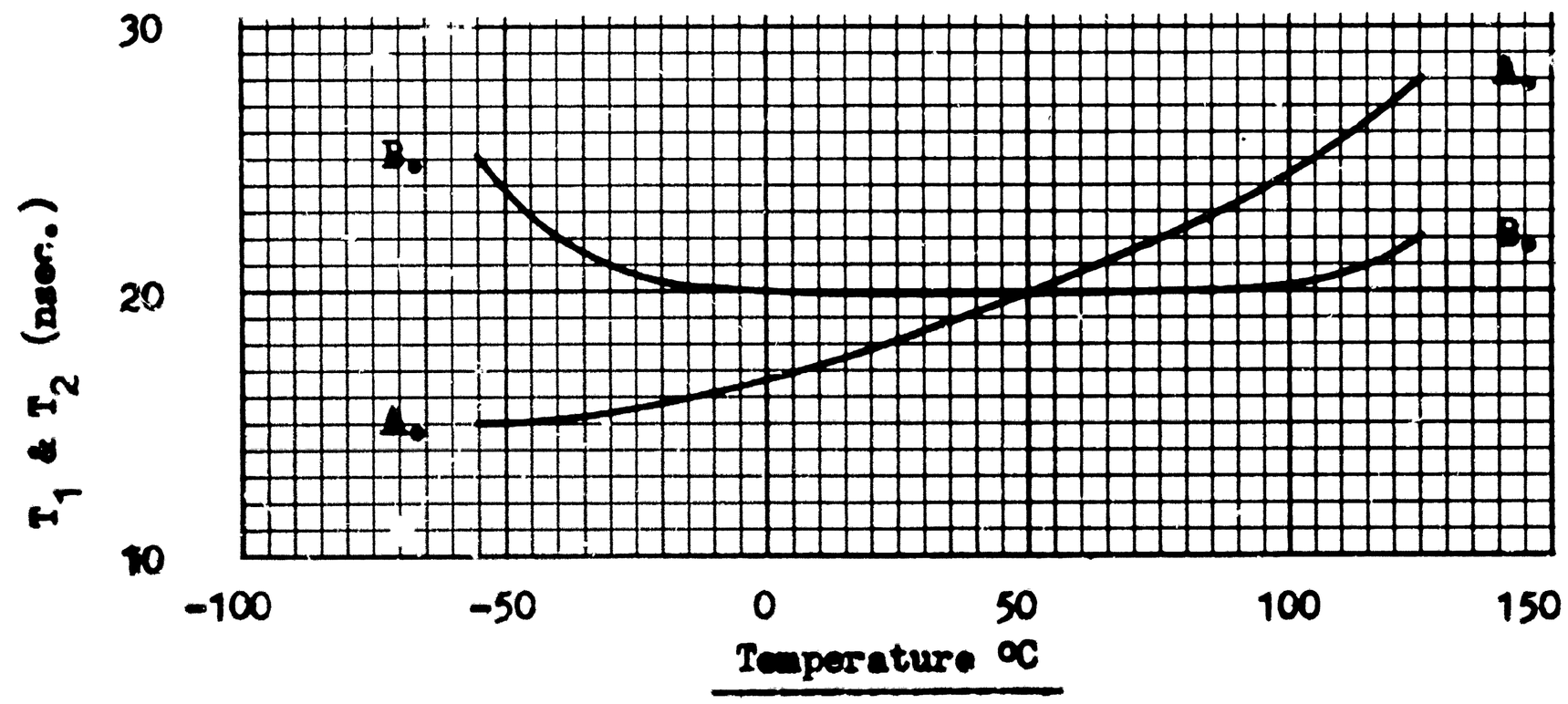


Clock Pulse A = T_1

Output Pulse B = T_2



SFF-3A
Input Frequency = 1 mc.
Clock Frequency = 2 mc.
V_{cc} = 5.0 volts
Load = 1 ckt./output

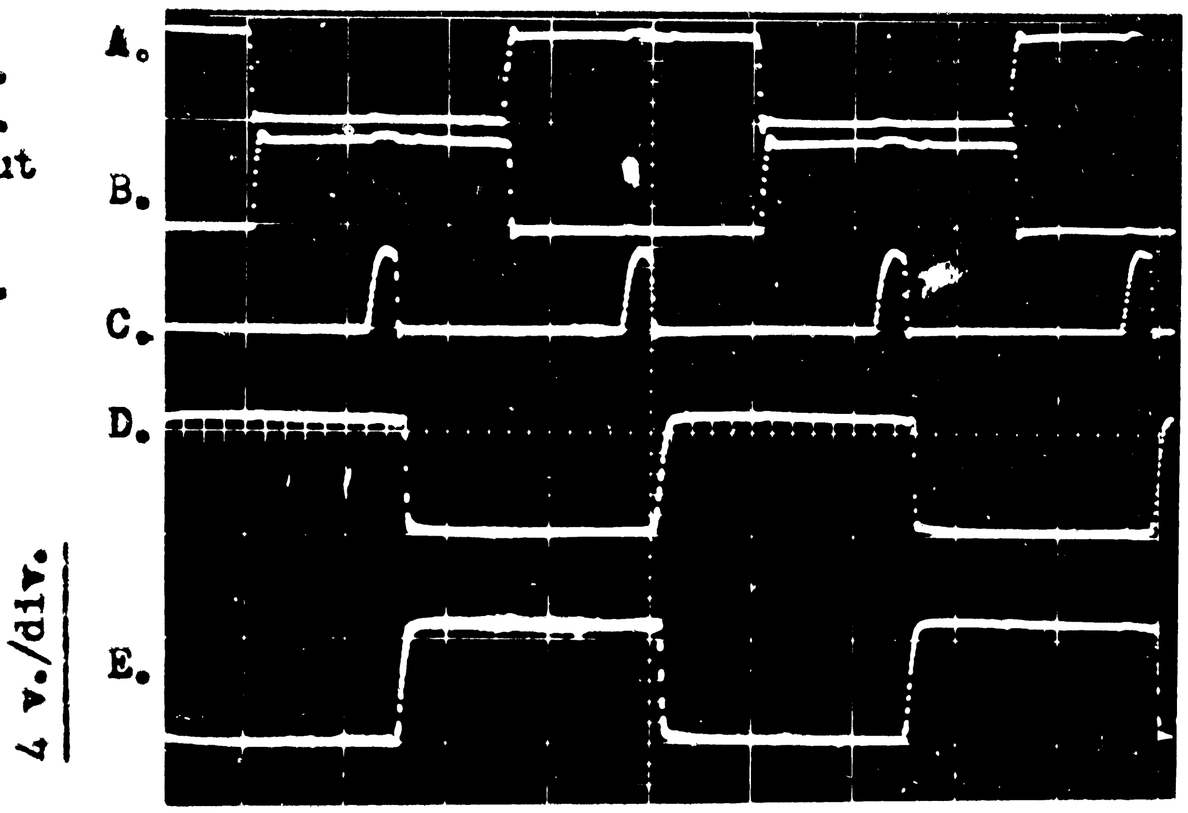


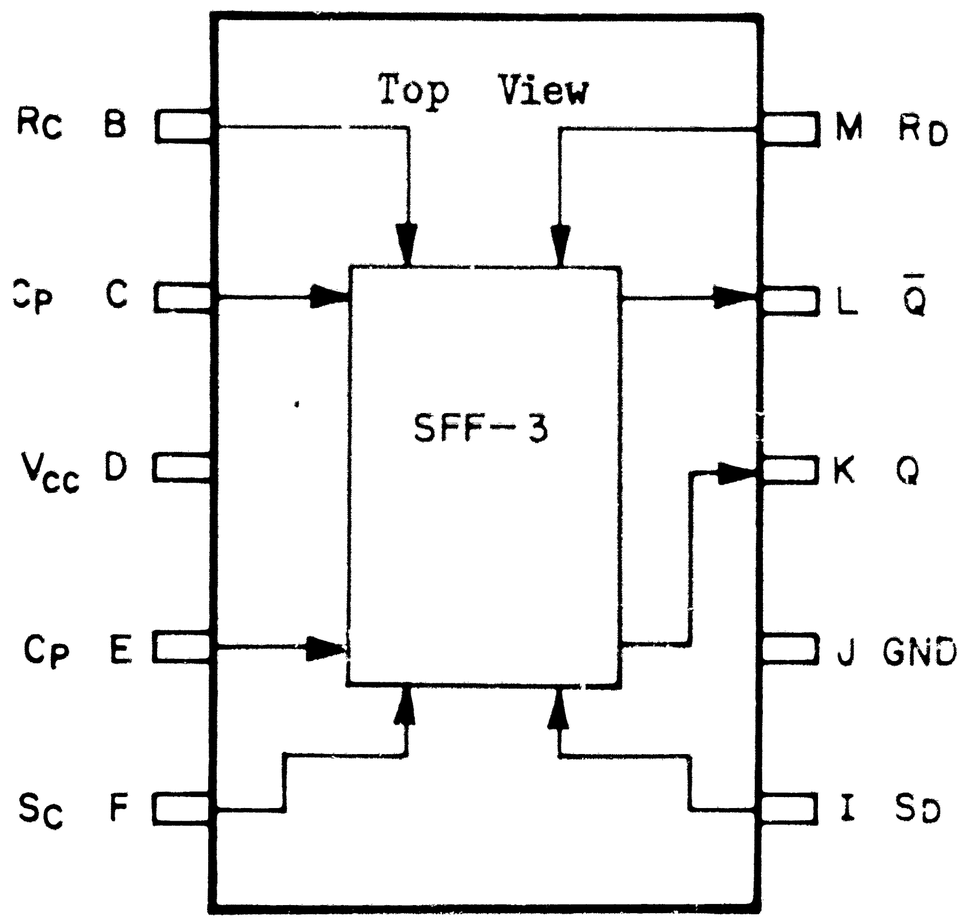
$A_o = T_2$
$B_o = T_1$

SFF-3A
Input Frequency = 1 mc.
Clock Frequency = 2 mc.
V_{cc} = 5.0 volts
Load = 1 ckt./output

SFF-3A

Input Freq. = 1 mc.
Clock Freq. = 2 mc.
Load = 1 ckt./output
V_{cc} = 5.0 volts
Temperature = 25°C.
A. = #10 input
B. = #2 input
C. = Clock Input
D. = #5 output
E. = #7 output





SECTION 4

APPLICATION

Section 4 - Application

μ-Note 941

Failure Analysis and Reliability Estimates of AN/ASW-25 (XN-) Microelectronic Digital One-Way Data Link

Failure rates and reliability estimates have been completed on a prototype Data Link (one-way) equipment, consisting of Receiver, Digital Logic, D/A Converters, Discrete Indicator and Power Supply. The Receiver and the D/A converters subsystems do not contain microelectronic circuitry. The type of microelectronic circuits contained in the other subsystems are described in μ-Note 613, μ-Note 811 and μ-Note 841.

The failure rate data was extracted from FARADA, Mil-Hdbk-217 and from commercial manufacturers literature and reports for those items not included in the military publications. The estimates were based on the simplifying assumption that any part failure will result in a functional failure. No wear out and drift failures were considered.

The estimated failure rates of the present (XN-1) equipment are shown below:

Functional Block	Rate (ppm)	% of Total
Receiver	211	10
Digital Logic	102	5
D.C. D/A Converter	275	13
A.C. D/A Converter	1003	47
Discrete Indicator	480	23
Power Supply and Misc.	35	2
Total	2106	100%

It can be seen in the above table that the A.C. D/A Converter and the Discrete Indicator contribute 70% of the estimated total failure rate. The A.C. D/A converter has been redesigned to replace 18 relays with solid-state circuitry (one differential amplifier and 18 transistors). The Discrete Indicator has been redesigned to eliminate complexity in the driver amplifiers by utilizing 7 micro-circuit darlington amplifiers.

Preliminary failure rate estimates of a tentative (XN-2A) equipment including the above two redesigned sub-assemblies are shown below:

Functional Block	Rate (ppm)	% of Total
Receiver	211	24
Digital Logic	115	13
D.C. D/A Converter	275	31
A.C. D/A Converter	200	22
Discrete Indicator	50	6
Power Supply and Misc.	35	4
Total	886	100%

It can be seen in the above table that the improvement in reliability or the decrease in the total failure rate of the tentative (XN-2A) equipment is approximately 2.5.

The total failure rate is the maximum that can be expected considering that an internal failure will cause a complete system failure. Such is not the case in this equipment. Various modes of operations are possible and reliability will be different for each operating mode. The resulting effective failure rates and the corresponding

MTBF's for specific operational requirements are tabulated below:

Minimum Acceptable Operating Condition	Present XN-1	Tentative XN-2A
Normal Operation (Visual & Automatic)	2106 ppm 470 hrs.	886 ppm 1130 hrs.
Manual Approach only (no Autopilot input)	1103 ppm 900 hrs.	686 ppm 1470 hrs.
Automatic Approach only (unusable Cross-Pointer)	1831 ppm 540 hrs.	611 ppm 1640 hrs.
Either Manual only or Automatic only	960 ppm 1040 hrs.	475 ppm 2100 hrs.

The above table indicates a reliability improvement of 2 to 1 between the various operating conditions.

SECTION 5

AVAILABILITY

μ-NOTE 951

MICROELECTRONIC DEVICES EVALUATED FOR μ-NOTES

The table on the following page lists the commercially available microelectronic functional devices which have been evaluated and reported upon in the μ-NOTES. The μ-NOTES issue number in which the evaluation results can be found is at the top of the table. The line below the μ-NOTES issue number identifies the source of the units by manufacturer. The basic description of each circuit type is referenced to each manufacturer by the particular manufacturers model number for the circuit evaluated.

μ-NOTES Issue No.	1	2	3	3	3	4	5	6	6	7	7	7	7	8	9	9	9	9	9	10
Circuit / Manufacturer*	TI	F	SIG.	PSI	RCA	W'HSE.	MOT.	M-H	M-H	TI	F	F	F	SIG.	SIL.	SYL	GME	SYL.
AND Gate								MHM3101		SN532				SE105K				2547C		SNG5B (2) SNG20
Dual AND										SN534								2547B		
NAND Gate			SE100T SE200T		DMC-100	WM2104		MHM3001		SN531	μL907			SE102K	A01A (1) A06A			2547A (1)	3658	SNG6B (1)
Dual NAND				PCC-101		WM2101				SN533			DTμL930		A02A (1) A07A			2642 (1)	3652	SNG4B (1)
NOR Gate	SN512	G									L907			SE102K (1)			C			
Dual NOR	SN514								MHM4101			MWμL910					D2 D3			
NOR w/Emitter Follower	SN513																			
OR/NOR Gate							MC306G		MHM4001										5436	
Exclusive OR	SN515		SE140T																	
Buffer		B	SE130T						MHM4401	SN535	μL900	MWμL909					B			
Flip-Flop	SN510	F	SE120T	PCF-101			MC302G	MHM3201		SN530	μL916		DTμL931	SE124K				2642B		SFF-2B SFF-3A
Flip-Flop w/Emitter Fol.	SN511																			
Half Adder		H		PCH-101			MC303G		MHM4301		μL904	MWμL912					H			
Adder									MHM4201			MWμL908					A			
Half Shift Register		S									μL905									
Shift Register				PCR-101					MHM4501						A03A		F			
Counter Adapter		C									μL901									
Bias Driver							MC304G													
Power Gate														SE110K			15303	2642 (1)		
Line Driver														SE150K	A05A (1)					
Monostable Multivib.														SE160K	A08A					

*
F--------Fairchild
GME------General Micro-Electronics
M-H------Minneapolis-Honeywell
MOT.-----Motorola
PSI------Pacific Semiconductor Inc.
RCA------Radio Corporation America
SIG.-----Signetics
SIL.-----Siliconix
SYL.-----Sylvania
TI-------Texas Instruments
W'HSE.---Westinghouse

(1) Same circuit performs NAND/NOR operation

(2) Same circuit performs AND/NOR operation