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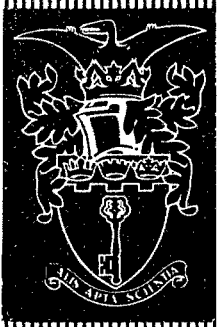
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**SOME APPLICATIONS OF
SYNTHESISED NEGATIVE
RESISTANCE CHARACTERISTICS
TO RING COUNTER DESIGN**

by

G. C. Lowe, Dip.Tech., Grad.I.E.E.

D. Thomas

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SOME APPLICATIONS OF SYNTHESISED NEGATIVE RESISTANCE
CHARACTERISTICS TO RING COUNTER DESIGN

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G. C. Lowe, Dip. Tech. Grad. I.E.E.
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SUMMARY

The large signal bistable properties of negative resistance devices are described and the simulation of negative resistance devices using positive feedback amplifiers is discussed. The form of an ideal characteristic for "unique bit" ring counter applications is suggested and a practical circuit that fulfils the requirements is proposed. Circuit details of a basic ring counter, a slave ring counter, and a shift register are given and important design criteria are presented. A method of generating interlaced sequential waveforms is described for a system using time division sub-multiplexing of input data.

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1 INTRODUCTION

To minimise circuit complexity it is normal to operate electronic digital data processing equipment at a constant predetermined bit rate, some arrangement being made to ensure that input information arrives at regular intervals. Various operations may be carried out, within the system, at different rates and timings and it is necessary to synchronise all events with respect to a fixed time base or "clock". To ensure synchronism all command signals are derived, by frequency division, from a master clock oscillator, and if ambiguity is to be avoided, the timing of each operation must be accurately related to some point on the lowest frequency waveform present.

The form taken by a particular frequency divider depends on the output waveform required and on certain practical points such as simplicity, economy, reliability, ease of synchronisation and power consumption. There are three basic forms of divider:-

- (a) Synchronised oscillators (e.g. multivibrators and staircase waveform generators).
- (b) Cascaded bistable elements in the form of binary ($\div 2$) dividers with feedback or gating of pulses to achieve the desired count down.
- (c) Cascaded bistable elements in the form of a "ring counter".

Synchronised oscillators provide the most economic means of dividing but they are of academic interest only in the present context because the critical nature of their operation makes them very unreliable. Methods (b) and (c) both employ bistable devices and the output waveform and power consumption requirements dictate which is preferable. Cascaded binaries yield square-wave outputs whose frequencies are submultiples of the frequency of the input waveform. Since one "side" of a binary is always conducting the power required by a binary chain is directly proportional to the number of bistable elements present. The action of a ring counter may be compared to a rotating single-pole multi-way switch, the pole of which is connected to a constant potential (V). The output from a given "way" will be V whilst the wiper is making contact and zero for the remainder of the revolution. In the case of a ring counter a "closed switch way" is represented by an "ON" stage (which will later be referred to as containing "one bit" of information). A ring counter can be designed so that only the "ON" stage consumes power, thus making it inherently more efficient than a binary chain. However, it employs more bistable elements for a given count down than does an equivalent binary chain, which in itself makes it less reliable.

Straightforward frequency division only requires a single output terminal and the use of cascaded binary dividers leads to the best compromise. However, command signals, having waveforms corresponding to those appearing at the outputs of a ring counter, are often required for applications where a number of operations have to be performed sequentially. The generation of this type of waveform from the information available at the outputs of a binary chain involves a large number of gates and power amplifiers, the latter being required to enable a reasonable amount of output power to be supplied. The ring counter described in this paper is capable of supplying considerable output power with no change in circuit configuration. The complexity of a binary chain plus gates and amplifiers is greater than that of an equivalent ring counter and thus in practice the minimal component advantage of the binary divider is lost, where a number of operations have to be performed sequentially. The ring counter is therefore now desirable from both reliability and power economy considerations.

Ring counter circuit techniques have not been developed to the same extent as have those for binary dividers, with the result that circuit designers tend to use binary dividers for applications where the use of a ring counter would lead to a more optimised design. A requirement for a reliable method of generating the sequential waveforms required for a time division submultiplexing data-handling system led to an investigation into the presently available ring counter techniques. Many methods utilise the negative resistance characteristic of certain devices (e.g. cold cathode discharge tubes, tunnel diodes and pnpn diodes), to provide the basic bistable element. This approach is theoretically sound but practical circuits using the above devices suffer in general from the following disadvantages:-

(i) The flexibility of circuit design is restricted because these devices have only two external connections (three in the case of trigger tubes and silicon controlled rectifiers). Usually there is also a considerable spread in parameters, and a compromise between power output capability and reliability of operation must be made.

(ii) The spread of the characteristics of most devices makes it impossible to design a ring counter which has the property of "unique bit" circulation (i.e. only one bit can be present in the ring at a time). Under these circumstances it is necessary to introduce a mechanism that will correct any faulty operation. This is normally achieved by a regularly (e.g. once per revolution) applied resetting process.

A satisfactory ring counter may be designed using the "negative resistance" approach if an idealised negative resistance characteristic, having a large and

predictable switching threshold, can be obtained. This paper describes the large signal properties of negative resistance devices and shows how a positive feedback amplifier may be used to provide a negative resistance characteristic. A particular circuit configuration is described which yields an almost ideal characteristic, all the parameters of which are under the control of the circuit designer. Some of these parameters may be made functions of an external control voltage enabling greater versatility to be realised. Three practical circuits are discussed, particular attention being paid to the methods available for providing a "commutative memory" and to the circuit tolerance requirements. The circuits dealt with are:-

- (1) A basic ring counter, having the following properties:-
 - (i) A supply power drain that is independent of the number of stages.
 - (ii) Large output power capability.
 - (iii) Facilities for accepting various types of synchronising signals.
 - (iv) Guaranteed unique bit circulation.
- (2) A "slave" ring counter, that operates at lower power levels and has relaxed circuit tolerances compared with (1), for use as a "floating" switch drive system in signal routing applications¹.
- (3) A shift register.

A method of obtaining an interlaced sub-multiplexing switch drive waveform using the basic ring counter is also discussed.

2 NEGATIVE RESISTANCE TECHNIQUES

2.1 Negative resistance characteristics and their large signal properties

Any device whose current-voltage (I-V) characteristic, between two terminals, has a region of negative slope, that is the dynamic resistance ($R = dV/dI$) is negative over a range of voltages, is known as a negative resistance device. The range of voltages over which R is negative must, in practice, be finite and the properties of a given device depend on the value of R at the turning points associated with the transition from the negative slope region to the regions of positive slope. There are two possible values R may take at a turning point, zero and infinity, and thus two distinct categories of device exist. If R increases to infinity at the transition, the characteristic of Fig.1(a) results and devices belonging to this group are said to be "short circuit stable" (s.c.s.) since a given voltage defines a unique point on the characteristic. Similarly if R decreases to zero at a transition the characteristic of Fig.1(b) results and

devices of this type are said to be "open circuit stable" (o.c.s.) since a given current defines a unique point.

We are interested here in the use of negative resistance devices as bistable elements. It may be shown that a simple circuit consisting of a linear (load) resistance in parallel with an o.c.s. negative resistance device (see Fig.2(a)) can yield the desired pair of bistable states. A condition that must be satisfied is that the "load line" must cut the device characteristic in three points. For o.c.s. devices a load resistance (R_L) less than the modulus of the negative slope resistance is a prime necessity. If this condition is fulfilled there is a range of supply current (I_B) for a given R_L , over which three point intersection occurs. This is shown in Fig.2(b), where the broken lines indicate the limiting positions of the load line for bistable operation. In the case of s.c.s. devices a similar situation exists for values of R_L greater than the modulus of the negative slope resistance. To study the stability at each of the "singular" points (1, 2 and 3) (Fig.2(b)) it is necessary to find and analyse the full equivalent circuit of the device and its associated components, including all inherent reactances. This analysis involves the solution of nonlinear differential equations. A graphical solution is shown in Fig.3 where the equivalent circuit used is representative of an o.c.s. device. The trajectories, shown in the "V-I" plane, are derived in a similar manner as are those obtained from a phase-plane analysis of a servo-system. The diagram may be used to determine how the voltage (V_T) and current (I_T) vary, from a known starting point, with respect to each other. The two singular points (1 and 3) at the intersections of the load line with the positive resistance sections of the characteristic are always stable and are either "nodal" (over-damped) or "focal" (under-damped) points. The remaining intersection (2) is a "saddle" point (unstable) for all values of L and C and for values of R_L less than the modulus of the negative slope resistance (i.e. for all values of R_L that yield a three point intersection). S.c.s. devices normally have an equivalent circuit which is the dual of that shown in Fig.3 and therefore the characteristic and trajectories hold for a s.c.s. device if the axes are interchanged. It will be shown later that o.c.s. devices are more suitable than s.c.s. devices for ring counter applications.

For a negative resistance device to be of use as a bistable element it is necessary to find a convenient means of switching from one stable state to the other. There are three methods by which the circuit may be switched:-

- (a) Modulation of the supply current.

(b) Introduction of energy, for example by capacitive coupling, to the junction of the load resistance and the device (point X in Fig.2).

(c) Modification of the device characteristic.

The principle of operation is basically the same in each case and depends on the temporary establishment of a unique stable singular point. Fig.4 illustrates the switching mechanism involved in the case of method (a). Assume that, prior to the negative going current pulse, the circuit is in its high current stable condition (i.e. point "1"). If the supply current (I_B) is now depressed, for a time T, by an amount (I_P) sufficient to ensure that the load line cuts the characteristic in a single point ("4"), the voltage (V_T) and current (I_T) must change from their initial values represented by point "1" to the values represented by point "4". The manner in which V_T and I_T vary with respect to each other is indicated by the trajectory "1.a.b.d.e.4". Since the velocity of travel along the trajectory is finite (not constant) the point reached at the end of the negative pulse depends on the pulse width T. If T is less than the time required for the operating point to reach a critical point lying between "b" and "d", the circuit will not switch but will revert back to its original condition along a trajectory such as "a1" or "b1". If the pulse is long enough to enable the operating point to move past this critical point the circuit will switch along a trajectory such as "d3" or "e3". While the pulse is present the operating point will approach point "4" in an exponential manner with time. A sufficiently long pulse allows the operating point to move close to point "4". The removal of the pulse then causes the operating point to move along the trajectory "43" to the final state "3". Fig.4 also shows how the circuit may be switched, in a similar manner to the above, from point "3" to the point "1" by the application of a positive current pulse. The temporarily stable point in this case is "5" and the critical switching point, on the trajectory 3fg5, lies between "f" and "g".

Method (b) is essentially an alternative means of modulating the supply voltage and thus results in a similar switching procedure. Method (c) involves the modification of the characteristic in such a manner as to ensure that the fixed load line only cuts the characteristic once. This type of mechanism is used in three terminal devices such as trigger tubes and silicon controlled rectifiers. These devices are often capable of being switched, by means of the trigger electrode, in only one direction, usually from the low to the high current states (this is the same as switching from the high to low voltage states). This modification is indicated in Fig.5 for the case of a trigger tube.

It can be seen that, whilst the characteristic is in the modified state, point "1" is a unique stable point and thus the circuit will tend to switch to this state.

2.2 The generation of negative resistance characteristics using positive feedback amplifiers

It is well known that the application of positive feedback to an amplifier can result in a negative output resistance. This principle is used in feedback oscillators. To generate a true d.c. negative resistance characteristic (one effective at zero frequency) it is necessary to employ direct coupling within the amplifier. A simple argument may be used to show that the two types of negative resistance characteristic, s.c.s. and o.c.s., can be generated, dependent on the form of the feedback. The schematic diagrams of Fig.6(a) and (b) indicate the form the output resistance takes in terms of the circuit parameters for both voltage and current feedback. The output resistance (R_o) for each case may be expressed in terms of the amplifier gain (A), the amplifier output resistance (R), the feedback attenuation (β), and the current feedback resistor (r):-

For positive voltage feedback

$$R_o = R / (1 - \beta A) \quad . \quad (1a)$$

For positive current feedback

$$R_o = R (1 - \beta Ar / R) \quad . \quad (1b)$$

These output resistances have been plotted, as functions of the amplifier gain in Fig. 7(a) and (b). Also the incremental resistance of the two characteristics of Fig.1 are plotted in Fig.7(c) and (d). It can be seen that, if the amplifier gain can be made to increase from zero to a maximum and then decrease to zero again with increasing source voltage V (Fig.6), the characteristic of Fig.7(c) may be obtained from Fig.7(a). The characteristic of Fig.7(d) may be obtained in a similar manner from Fig.7(b). These requirements are normally satisfied in a practical amplifier because the gain is zero at the limit conditions of cut-off and saturation. It may be concluded that:-

- (a) Direct coupled positive voltage feedback amplifiers give rise to a s.c.s. characteristic at their output terminals, and
- (b) direct coupled positive current feedback amplifiers give rise to an o.c.s. characteristic at their output terminals.

The circuits and waveforms of Figs.8 and 9 show an example of both types of amplifier. The circuit of Fig.8 operates as a current feedback amplifier because the load current (I) also flows in the collector circuit of T2 yielding an input to the amplifier which is proportional to the load current. The use of complementary transistors has the advantage that it allows simplified direct coupling arrangements. It can also be economic in power consumption because it is possible to adjust the characteristic so that the circuit takes a negligible amount of power when in one of the stable states.

2.3 An idealised characteristic for ring counter applications and its practical realisation

In the case of currently available negative resistance devices (e.g. silicon controlled rectifiers) the basic shape of the characteristic and the spread of parameters between devices make it exceedingly difficult to produce a ring counter configuration which has the property of "unique bit" circulation.

Fig.10 shows how both s.c.s. and o.c.s. devices can be cascaded to ensure that all but one of the devices are in the same stable condition (ideal characteristics are shown on this diagram, the desirable properties of which are described below). The parallel combination of o.c.s. devices has the practical advantage that all devices are connected between common supply lines, enabling information to be extracted from the ring with ease. The operation of both systems is similar, one being the dual of the other, and relies on the existence of a relatively large and stable threshold. The threshold in the case of the characteristic of Fig.10(b) is the current amplitude of the horizontal section of the characteristic (I_1). For a given device to be in the ON condition ("2") a current greater than I_1 must flow through it and hence if the total current (I) supplied to the parallel combination is less than twice I_1 it is impossible for more than one stage to come ON. The optimum magnitude of I is $3/2 I_1$ and for correct operation a maximum tolerance of $\pm 33\frac{1}{3}\%$ is permissible on this value. It will be shown later that the summation of the tolerance requirements in a practical circuit considerably reduces this latter figure. The circuit of a practical ring counter stage is shown in Fig.11(a) and it can be seen from the V-I characteristic of Fig.11(b) that this circuit provides an almost ideal characteristic. The approximate values of the parameters of the characteristic in terms of the circuit parameters are indicated in Fig.12. The horizontal position of the section AB of the characteristic is a function of the potential of the base of T2 and may therefore be varied by modulating this voltage, thus providing a possible means of introducing a commutative memory. When operated correctly transistor T1 (Fig.11) is either cut-off or fully bottomed, thus a convenient high power output

is available at its collector. The base drive current of T1 is the difference between the supply current (I) and the threshold current V_1/R_1 .

This basic stage has been used as the active element in the ring counter described in Section 3.

3 THE RING COUNTER

3.1 The basic ring. Description and operation

The full circuit of the basic ring is given in Fig.13, and the waveforms at the base of T2 are given in Fig.14.

Assume that stage 1 is in the ON condition, and that control current, I, is being supplied from the control circuit (collector of T5) to the emitter of 1T2. The action of the ring is such, that to put the next stage into a state from which it will switch ON, it is necessary to interrupt the control current (I). When this current is reduced below the threshold value (I_1) of the o.c.s. characteristic (Fig.10), stage 1 switches OFF. The bases of all P.N.P. transistors (1T2, 3T2 to nT2) are at +6 volts. The base of 2T2, however, is held negative with respect to the +6 volt line during the time that the control current is interrupted (i.e. for the period of the clocking pulse), by the charge on 1C1, which was accumulated during the ON period of stage 1. The peak voltage of the characteristic of stage 2, given by the value 0Δ (Fig.12) is therefore reduced in the manner described in Section 2.3. Thus when the current I is re-established, it is diverted into the emitter of 2T2, switching stage 2 ON. 1D2 is reverse biased allowing 1C1 to discharge. Simultaneously 2C1 is charged via 2R4, thus providing stage 3 with a commutative memory. The above operation can now be repeated to switch OFF stage 2 and switch ON stage 3, at the end of the next clock pulse.

There are thus four permissible voltage levels V_{B2} for the base of T2 (Fig.14). They are:-

- (a) +6 volts, when stage is OFF.
- (b) +5.7 volts, on the stage following, a stage with a memory voltage (residual memory).
- (c) +4.5 volts, on the stage with memory voltage applied.
- (d) +3.0 volts, when stage is ON.

The control circuit has been designed so that a number of cascaded ring counters may be synchronised accurately (i.e. without introducing unnecessary time delays). This condition is satisfied by using the OFF edge from the preceding ring,

ensuring that the control currents, I , in all rings, are switched OFF simultaneously. The input of the gating transistor T3 (Fig.13) is connected to the appropriate output of the preceding ring, via a resistor. The circuit is arranged so that when this output is in the ON state (i.e. 0 volts) the base drive current of T3 is diverted into the diode D3, thus cutting off T3. When the output stage of the preceding ring switches OFF (i.e. returns to the +6 volts line), T3 is switched ON rapidly via R6 providing a negative step at point A of 5 volts amplitude. This edge is transported to the base of T4 via C2 switching T4 ON and cutting off T5. Thus the control current (I) is interrupted in the required manner. The base of T4 recovers towards the +11 volts line on a time constant $C_2 R'$ [where $R' = R_8 \times R_9 / (R_8 + R_9)$]. When the base of T4 has recovered to the potential of the base of T5, the current (I) in T5 is switched ON and the ring steps forward by one position.

It was shown in Section 2.1 that the current I must be interrupted for sufficient time (T) to ensure that the stage switching OFF can make the transition to the OFF stable position. There is also an upper limit for T , as if the pulse is present too long the commutative memory will have decayed (see Section 3.2). In the practical circuit of Fig.13 the minimum value of T is found to be $< 1 \mu\text{sec}$ and the maximum value is $20 \mu\text{sec}$. A well defined clock pulse width of nominally $1 \mu\text{sec}$ is achieved here by comparing the exponential rising voltage on the base of T4 against the voltage at the base of T5, and ending the pulse when these voltages are equal, that is approximately at $t = 0.7 C_2 R'$ which is a fast rising part of the waveform.

Although it is impossible for more than one stage to conduct, it is, however, possible for no stages to come ON when supplies are initially connected, due to a possible sharing of the current in the emitters of several stages. To overcome this difficulty the characteristic of stage 1 is modified by the addition of a resistor (R5) between the base of 1T2 and the 0 volt line. This ensures that the emitter of 1T2 is always at a lower potential than the emitters (T2) of any other OFF stage. Thus the voltage levels for the base of 1T2 are modified by the self start resistor (R5), so that the voltages a, b, c and d become +5.5, +5.2, +4.0 and +2.5 volts respectively.

3.2 Design considerations

The major requirement which has been borne in mind in designing this counter is the guarantee of unique bit circulation. Among other requirements which will be considered are: flexible reset and sync. facilities, speed of operation, and output power capabilities. When taking into account parameter tolerances,

(e.g. line voltages, resistors, transistors), allowance must be made for the effect of temperature changes which in some applications, for example airborne systems, may be large.

3.2.1 Unique bit circulation

To ensure unique bit circulation when the o.c.s. elements of this counter are connected in parallel, it is necessary to define the allowable tolerances on the nominal value of the current (I), supplied from the control unit. This was shown to be $\pm 33\frac{1}{3}\%$ in the ideal case of Section 2.3. However, in practice a number of factors reduce this allowed tolerance. It is therefore necessary to derive new limits for I , and to analyse the control circuit to show that these closer tolerances can be achieved. For clarity the basic ring element and the relevant section of the control circuit have been re-drawn in Fig.15.

The basic relationships in Fig.15 are:-

$$\begin{aligned} \text{The threshold value of current } I(I_1) &= (V_3 + V_{bc1}) / (R_3 h_{FB2}) & (2) \\ & \text{(T1 not conducting)} \end{aligned}$$

$$\begin{aligned} \text{Collector current of T2} &= h_{FB2} I_1 + I_{b1} & (3) \\ & \text{(T1 conducting)} \end{aligned}$$

$$\text{Control current } (I) = (V - V_{be5}) h_{FB5} / R_{10} \quad (4)$$

$$\text{where} \quad V = R_{11}(V_2 - V_1) / (R_{11} + R_{12}) \quad (5)$$

in which V_{be1} , V_{be5} , h_{FB2} , h_{FB5} and I_{b1} are the base emitter voltage (when conducting) of T1 and T5, grounded base d.c. current gain of T2 and T5 and the base current of T1.

Denoting maximum and minimum values by upper and lower bars respectively, the minimum and maximum allowed values of the control current I are given by,

$$\text{Lt } \underline{I} = \bar{I}_1 + \bar{I}_{b1} / \underline{h_{FB2}} \quad (6)$$

$$\text{Lt } \bar{I} = 2 \underline{I}_1 \quad (7)$$

in which h_{FB2} is the grounded base current gain of T₂ assumed to have a maximum value of unity and:-

$$\bar{I}_1 = (\bar{V}_3 + \bar{V}_{be1}) / (\bar{R}_3 \cdot h_{FB2})$$

$$\underline{I}_1 = (\underline{V}_3 + \underline{V}_{be1}) / \bar{R}_3 .$$

Equations (6) and (7) represent the absolute limits for the control current I which will allow unique bit circulation in the basic ring. It remains to determine the possible maximum and minimum values of I in the control circuit of Fig.15. From (4) and (5) assuming $\overline{h_{FB5}}$ to be unity these are:-

$$\bar{I} = (\bar{V} - \underline{V}_{be5}) / \bar{R}_{10}$$

$$\underline{I} = (\underline{V} - \bar{V}_{be5}) h_{FB5} / \bar{R}_{10}$$

in which

$$\bar{V} = \bar{R}_{11}(\bar{V}_2 - \underline{V}_1) / (\bar{R}_{11} + \bar{R}_{12})$$

$$\underline{V} = \underline{R}_{11}(\underline{V}_2 - \bar{V}_1) / (\underline{R}_{11} + \bar{R}_{12}) .$$

To guarantee unique bit circulation the following relationships must hold:-

$$\text{Lt } \underline{I} \leq \underline{I} \leq I \leq \bar{I} \leq \text{Lt } \bar{I} . \quad (8)$$

The two "limit currents" ($\text{Lt } \underline{I}$, $\text{Lt } \bar{I}$) are 3.7 mA and 5.6 mA for the circuit of Fig.13 when the following parameter limits apply:

- (i) Resistor tolerance = $\pm 2\%$
- (ii) Supply line tolerance = $\pm 5\%$
- (iii) Minimum current gain (h_{FB}) = 0.966
- (iv) Base emitter voltage range (V_{eb}) = 0.5 to 0.8 volts
- (v) Maximum load current = 6 mA.

The values of \underline{I} and \bar{I} (control current) are 3.9 mA and 5.5 mA respectively using the same circuit parameter tolerances. Thus for the stated conditions, unique bit circulation is guaranteed, since conditions(8) have been satisfied.

3.2.2 Synchronisation and reset facilities

The synchronisation and reset functions both involve setting the counter to a predetermined state. Synchronisation is necessary when two or more counters are required to run in the correct phase with respect to each other, and is

normally related to the clock pulse rate. Reset is necessary if it is required to set a ring counter to any specified state in the absence of clock pulses.

The method which has been adopted here to achieve these functions is to modify the characteristic of the basic ring element by applying control voltages to the base of nT_2 (the required stage), from an external source. This is an extension of the mechanism used for providing commutative memory which has been described. The external control voltages override the existing memory voltage wherever it occurs. Fig.16 shows how the characteristic is modified and suggested limits are indicated for the levels of the various functions.

Any synchronising voltage level must lie between the maximum memory voltage and the minimum ON voltage (Fig.16). A synchronising pulse does not switch ON any stage but its presence ensures that the stage to which it is applied will switch ON at the end of the next clock pulse, instead of the stage which contained the memory. (The end of a clock pulse represents the re-establishment of control current and, therefore, the moment of switching.)

Re-set operation involves a different switching mechanism, since a clock pulse cannot be used to switch the ON stage OFF. Thus the voltage level for re-set must be lower than the lowest ON voltage, so that control current can be diverted from the existing ON stage to the stage which it is desired to switch ON. The minimum limit to this voltage is set by the emitter base breakdown voltage of nT_2 . Thus two voltage levels additional to those given in Section 3.2, are allocated to the base of nT_2 . In the practical circuit they are:-

- (a) +3.5 volts. Synchronisation voltage.
- (b) +1.5 volts. Re-set voltage.

3.2.3 Speed of operation

There is no lower limit to the rate of circulation of information (bit rate) in the counter, because the circuit is directly coupled. The maximum bit rate is limited by the finite times required to charge and discharge the memory capacitor. The voltage waveforms at the bases of T_2 , on each stage of a 4-way counter operating at a low bit rate are shown in Fig.17. (The letters a, b, c and d refer to stages 1, 2, 3 and 4 respectively.) Assume that stage 1 was conducting and is switched off by the clock pulse as shown. There is a delay of 0.3 μ sec before the base voltage of T_2 on stage 1 falls. The voltage falls rapidly for the duration of the clock pulse, at the end of which it decays slowly to 0 volts. The voltage on the base of T_2 (stage 2), which has had time to charge to the full memory voltage of 1.5 volts decays slightly during the period of the clock pulse, switching rapidly to the ON condition (3 volts) at the end of the clock pulse. In

stage 3, the voltage is constant during the clock pulse then charges to the full memory voltage, 1.5 volts, on a time constant of about 25 μ sec. The voltage at the base of T2 in stage 4 remains at about 0 volt.

At high bit rates, the counter will still operate even when the time to charge the memory capacitor is less than 25 μ sec. The limiting bit rate, however occurs when the decaying voltage on the base of the ON stage (a) and the charging memory voltage of the stage next to conduct, now represented by curve c, are equal. On Fig.17 this is called the crossover point and would occur 2.6 μ sec after the end of the clock pulse. An experimental 4 way ring, built in the laboratory, operated up to 250 kc/s. To ensure reliable operation under limit tolerance conditions, an upper frequency limit of 40 kc/s is recommended.

3.2.4 Output power capabilities

The output of the ring is obtained from the collector of the transistor T1 (Fig.15), which supplies a current I_L , into a load connected to a positive voltage line. This voltage must not exceed the collector-emitter breakdown voltage of the transistor T1. The breakdown voltage of T1 (ZT84) is 60 volts hence the maximum power output

$$P_{\max} = 60 \cdot I_L \quad (9)$$

The load current (I_L), is directly related to the base current (I_{b1}) by the grounded-emitter current gain of T1 (h_{FE1})

$$I_L = I_{b1} \cdot h_{FE1} \quad (10)$$

The base current (I_{b1}) is supplied from the control circuit. The relationship of I_{b1} to the control current is shown in Fig.18. It can be seen that if a tighter tolerance can be achieved on the control current, more current is available as base current for T1. Alternatively if the mean current I is increased then the base current is increased correspondingly. In the practical circuit of Fig.13 a load current of 6 mA is specified and from equation (9) the maximum power output of the ring counter, P_{\max} is 360 milliwatts.

3.3 Slave ring counter

A slave ring counter is run in synchronism with a master ring counter. Since the slave ring may be re-set once per revolution by information derived from the master ring, the slave ring may be of a simpler design and may consume

less power than the master ring. A specific requirement¹ for a low power ring of this type led to the development of the circuit shown in Fig.19. The control circuit of the basic ring has been replaced by a single resistor (R7), which is returned via a positive pulse generator to the -9 volt line. The negative resistance characteristic of the slave ring is shown in Fig.20.

The ring is stepped ON by apply a positive clock pulse greater than V_{CP} (Fig.20) to R7. This switches off the current in R7, switching the ON stage OFF. At the end of the clock pulse the stage with a modified characteristic switches ON. There are two possible ways of modifying the characteristic:-

(i) Commutative memory.

(ii) Re-set pulse.

(i) The commutative memory on C1 modifies the characteristic, as described previously, by increasing the peak voltage from $0A$ to $0A'$ (Fig.20).

(ii) The re-set pulse modifies the characteristic by increasing the peak voltage from $0A$ to $0A''$ (Fig.20). Only this stage will come ON, disregarding the memory on any other stage, at the end of the clock pulse. The re-set pulse is obtained from the appropriate output of the master ring. Normally the clock and re-set pulses are applied simultaneously, the re-set pulse being of longer duration.

Tests were made to ascertain the critical width-amplitude relationship of the pulses, both re-set and clock, for correct operation of the slave ring. The results are displayed in graph form in Fig.21. The rectangles show the limit values for the nominal pulses.

3.4 Shift register

3.4.1 Simplified account of operation

In complete contrast to the ring counter, in which uniqueness of bit is of prime importance, a shift register requires that any number of stages may be ON simultaneously. A practical circuit of a shift register stage is shown in Fig.22. Information either in the form of a 0 bit or 1 bit is fed into the first stage of the shift register, at point A. This bit is passed to the successive stage on receipt of clock information. A different clocking mechanism is employed in the shift register. The control circuit of the ring counter is replaced by a resistor R3 (Fig.22), in each stage in series with the emitter of T2. The other ends of the resistors are all connected through a common voltage generator to the +6 volt line. The voltage generator supplies pulses which modulate the o.c.s. characteristic of the shift register. Two 3 volt pulses of 1.5 microseconds

duration are required. The first pulse, being of negative polarity, switches all stages OFF. The second pulse follows immediately and is positive. Its amplitude is such that only stages with memory bias voltages present are switched ON. These memory voltages are developed across the capacitor C1, whilst the stage is ON.

The diode D1 of the basic ring counter (Fig.13) is replaced by diodes D4 and D5 (Fig.22). They fulfil the same function as D1, and in addition prevent feed forward of memory voltage. The output of the stage is taken from the collector of T1, and a large output can be obtained in a similar manner to that described in section 3.2.4.

3.4.2 Design considerations

A typical voltage-current plot of the desired negative resistance characteristic is presented in Fig.23. The form of this characteristic is a function of the circuit parameters as described in Section 2.3. The characteristic is modified by the memory voltage so that the peak voltage of the characteristic is reduced from OA to OA' . The series resistor is selected so that the load line cuts the characteristic in three unique points (1, 2, 3).

Intersection 2 must be between points C and B under limit tolerance conditions. It is convenient to make point A' and intersection 3 coincident to ease tolerancing requirements. Points 1 and 3 are stable and represent the ON and OFF states of the device respectively. Intersection 2 is unstable. From this diagram the approximate values of pulse amplitude may be obtained.

The negative pulse V_n must be > 1 volt. The positive pulse V_p must be between 0.75 and 3.75 volts. In practice this range is reduced. Limit voltage amplitude/pulse length plots for the negative and positive pulses were obtained in an experimental four way model and are shown in Fig.24. A certain minimum time is required for the transistors to switch OFF, for a given V_n , as described in Section 2.1. The predicted minimum value of V_n above only applies if the pulse length is infinite. As the pulse width reduces, the required minimum value of V_n increases rapidly. In a similar manner, a certain pulse height/width relationship is required for switch ON. From the instant of switch OFF, the memory is decaying and section $A'B'$ moves towards $A B$ (Fig.23). Hence the minimum value of V_p , for long T_p , depends on T_n , where T_p and T_n are the times of duration of positive and negative pulses. Switching occurs in approximately 0.2 microseconds for large V_p , hence the memory on the next stage commences to grow and thus the maximum value of V_p reduces as T_p is increased, because section $A B$ starts to move towards $A'B'$, on the next stage. From Fig.24, a pulse

amplitude of 3 ± 0.5 volts and a duration of 1.5 ± 0.5 microseconds were selected for both the positive and negative pulses. The permissible pulses are represented by the rectangles on Fig.24. The minimum bit time obtained with these pulses was 65 microseconds.

3.5 Generation of interlaced sub-multiplexing waveforms

In time-division multiplexing systems, where a large number of input signals have to be sampled, it is often desirable to use a sub-multiplexing technique to reduce the effect of certain sources of error, for example by trading shunt for series error components. The basic configuration of a sub-multiplexing system is shown in Fig.25(a). Rotating switches are shown for simplicity but in practice each switch "way" is usually a single pole ON/OFF switch. If the energisation of each of the input switches (a to p) is arranged to occur in a certain sequence it is possible to provide time intervals during which each switch may open or close without affecting the performance of the system. Under these conditions it is sometimes possible to use slow operating switches (e.g. reed relays) for the input switches. A method of achieving this type of operation is shown in Fig.25(b). The operating sequence of this system is as follows. Assume switches a and e are closed and that A has just closed. Switches i and m are now energised. A opens after one bit time and B closes for one bit. Thus when C closes switch i has been energised for two bits and may therefore have had time to reach equilibrium in the ON condition. As C closes a and e are de-energised and b and f are energised, again two bits elapse before A closes again. Fig.26 shows the complete timing sequence for this particular configuration. This diagram illustrates how the low speed switches (a to p) are divided into two groups (I and II), each group being driven by a separate synchronised ring counter.

The time available for a low speed switch to close will now be derived for a general system having the following parameters:-

- N = number of inputs
- T = sample or bit time
- a = number of low speed switches ganged together
- b = number of high speed switches
- p = interlacing ratio
- τ = time for a low speed switch to open or close.

The interlacing ratio p is defined by:

$$p = b/a \quad (+ve \text{ integer}) \quad (11)$$

p is also the number of ring counters required to drive the low speed sections of the system. Each of these ring counters must have N/b stages. The cycle time of the high speed switch is bT and the time for the high speed switch to traverse the positions connected to a group of closed low speed switches is aT . The difference between these times represents the time allowed for the low speed switches to come ON. In a practical system it is usually desirable to keep the number of high speed switches to a minimum and it is therefore convenient to express the operate time (τ) in terms of T , p and b , thus:

$$\tau = bT \left\{ \frac{p-1}{p} \right\} . \quad (12)$$

Since the factor $(p-1)/p$ rapidly approaches unity with increasing p (the number of low speed ring counters) it is normal to choose the lowest possible value of p above unity; this is also the lowest factor of b . Obviously it is preferable if b is made even enabling p to take the value 2.

Fig.27 shows how three of the ring counters described in Section 3.1 may be used to generate the required waveforms for a 2:1 interlaced system. Ring I steps on when output B of the high speed ring changes from a "1" to a "0". Similarly ring II steps on when D changes from a "1" to a "0". When ring II reaches stage (ℓ, p) , transistor T2 conducts and clamps the input of ring II and prevents further inputs from D having any effect. When ring I reaches stage (a, e) , T1 conducts cutting-off T2 thus enabling the next change in output D to step ring II on. In normal operation no input signals to ring II are lost because the output (a, e) of ring I is switched to the "1" state mid-way through the normal "ON" period of output (ℓ, p) of ring II. However if ring II is out of step with respect to ring I it waits at (ℓ, p) until ring I reaches (a, e) when it continues normally.

This circuit remains unchanged for any number of inputs providing a 2:1 interlace is possible (b even), additional high speed sections being evenly distributed between (A and B) and (C and D). Similarly extra low speed sections should be placed between $(i, m$ and $j, n)$, $(k, o$ and $\ell, p)$, $(a, e$ and $b, f)$ and $(c, g$ and $d, h)$.

This circuit has been used to provide the drive waveforms of a system having the following parameters:-

$$\begin{array}{ll} N = 144 & T = 0.7 \text{ mS} \\ a = 6 & b = 12 \\ p = 2 & \end{array}$$

Reed relays were used as the low speed switches in a double-pole system, 12 relays being operated by each drive coil. The time (τ) allowed for these relays to operate (from equation (12)) was 4.2 mS, which is sufficient for high speed reeds to reach equilibrium (i.e. for a contact to be made and any subsequent vibration to decay).

4 CONCLUSION

Consideration of the large signal parameters of negative resistance devices results in the formulation of a method by which both open and short circuit stable characteristics may be simulated using positive feedback amplifiers. An idealised open circuit stable characteristic is described which may be used as the basic element in ring counter and shift register applications. This form of ring counter is shown to have some advantages over binary ring counters. They are:

- (a) Reduced power requirements.
- (b) Economy of components and simplification of circuit.
- (c) High power output capability.

An example of the simplicity with which complex sequential waveforms may be generated using this kind of ring counter has been described in Section 3.5. It is felt that a micro-circuit version of the basic active element would provide a useful accessory to the existing range of logic elements.

REFERENCE

<u>No.</u>	<u>Author</u>	<u>Title, etc</u>
1	G.C. Lowe	Low-level high-speed multiplexing switches for data acquisition systems. R.A.E. Technical Report 64033, 1964

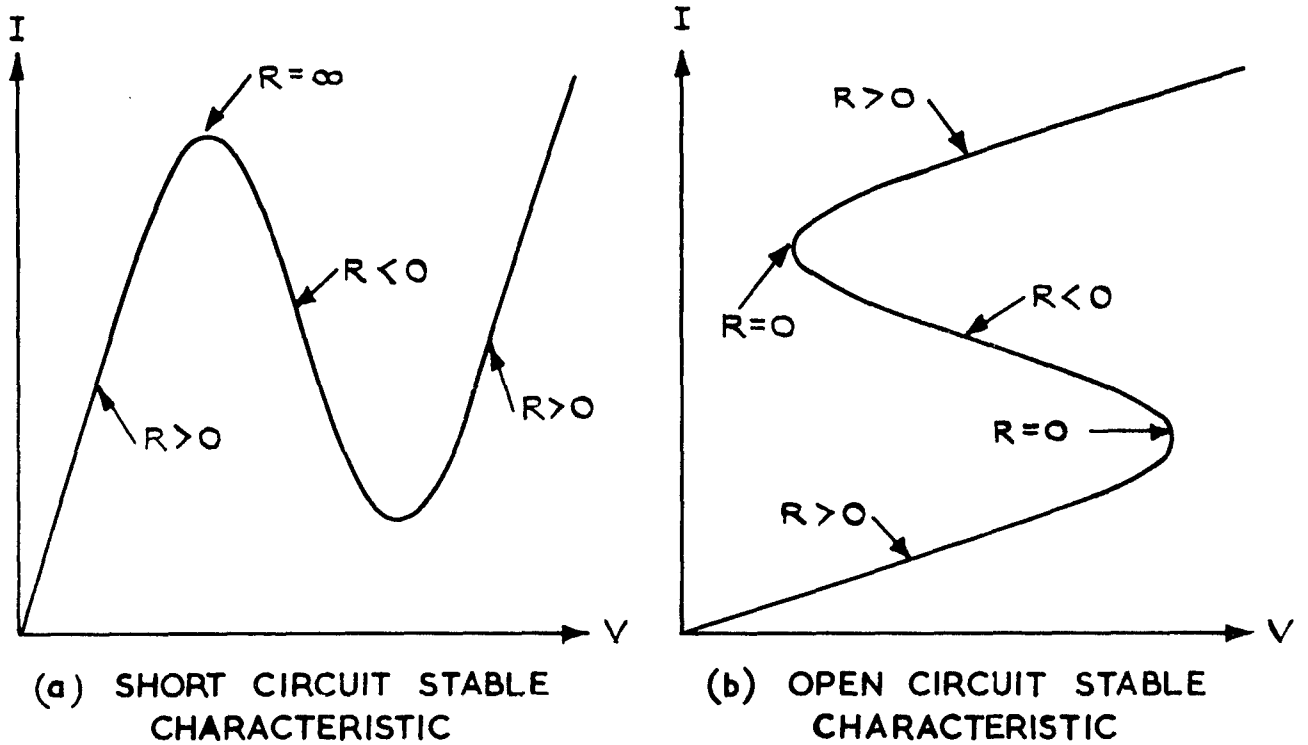


FIG 1 (a & b) CURRENT VOLTAGE CHARACTERISTICS OF THE TWO TYPES OF NEGATIVE RESISTANCE DEVICE

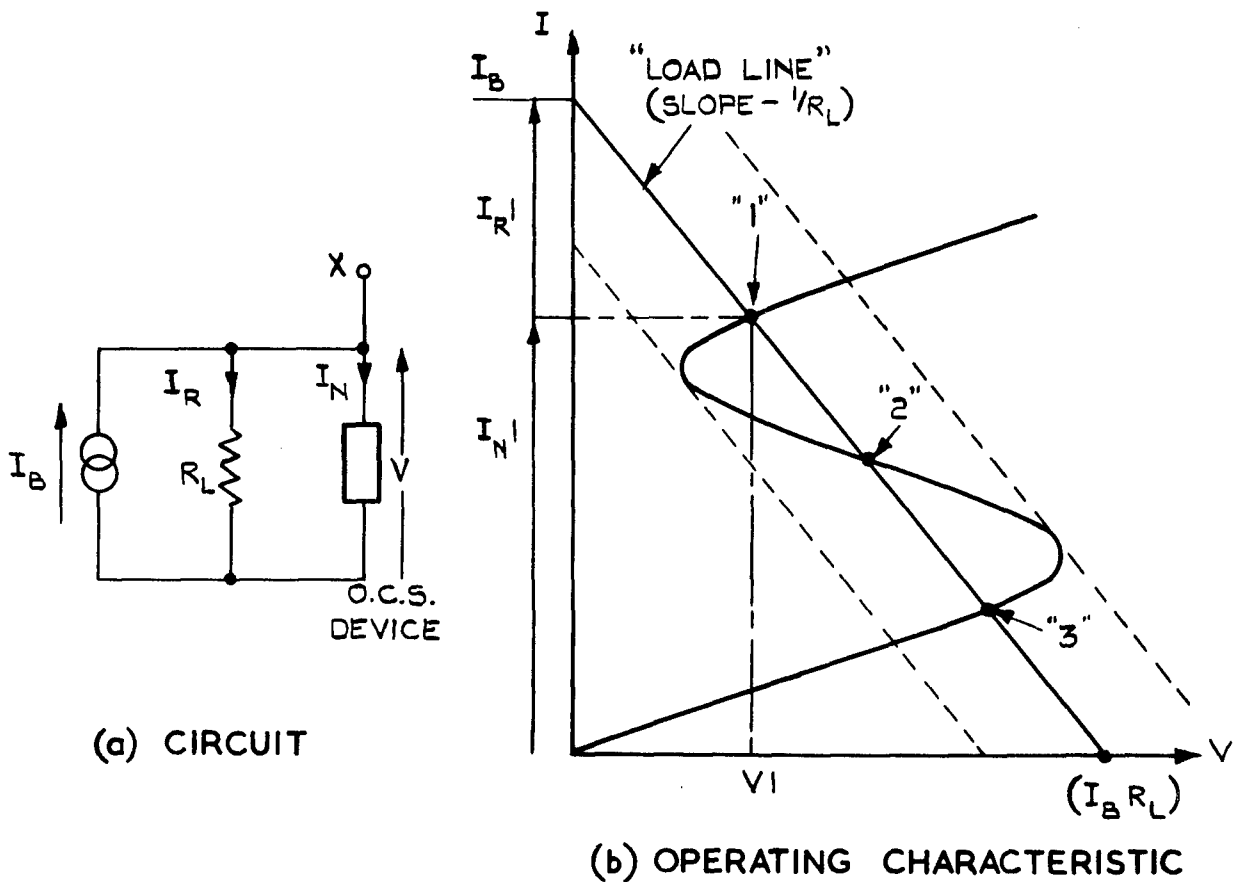


FIG 2 (a & b) THREE POINT INTERSECTION OF AN O. C. S. CHARACTERISTIC BY A LOAD LINE

Fig.3

IR/P 713

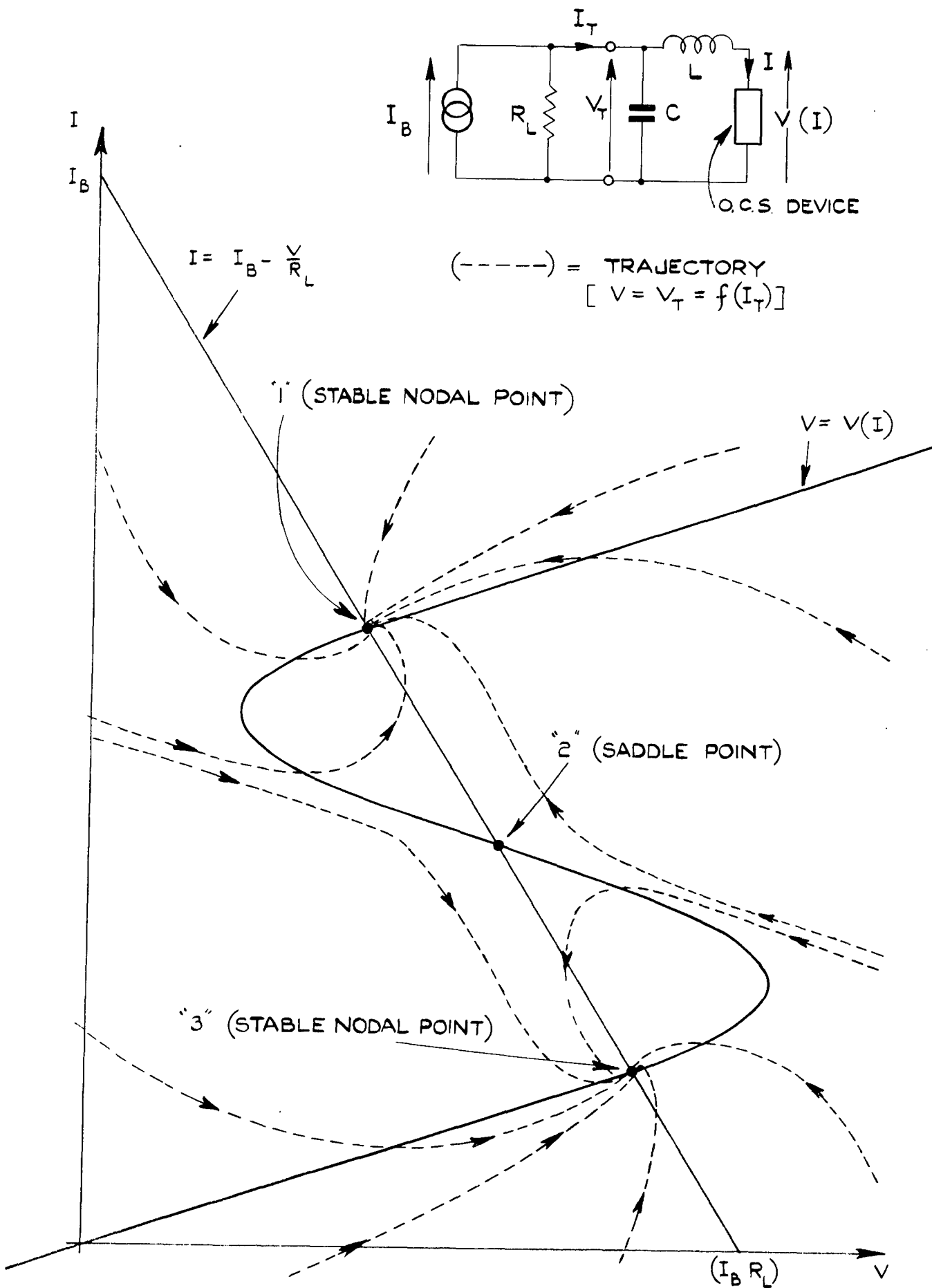
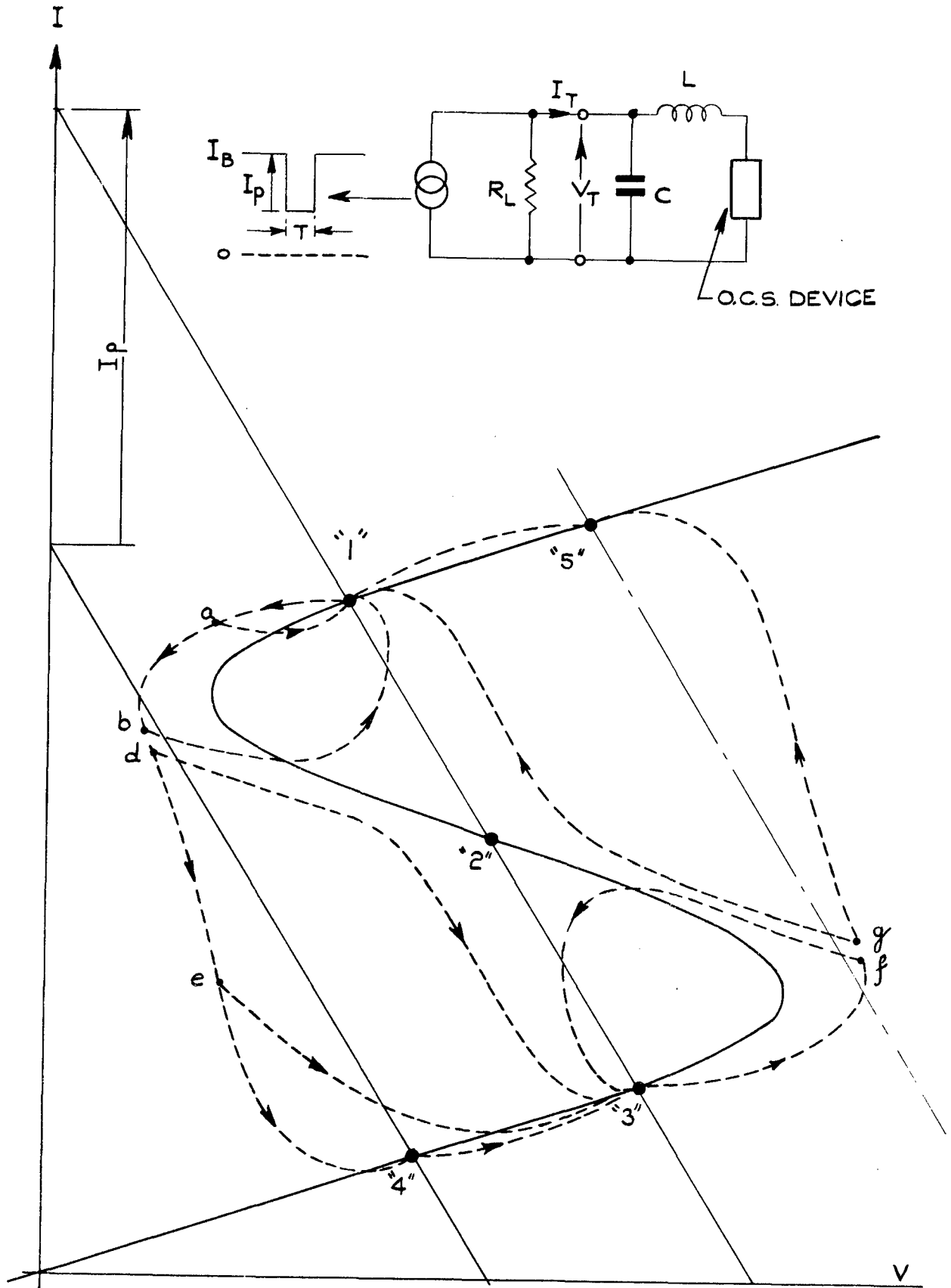


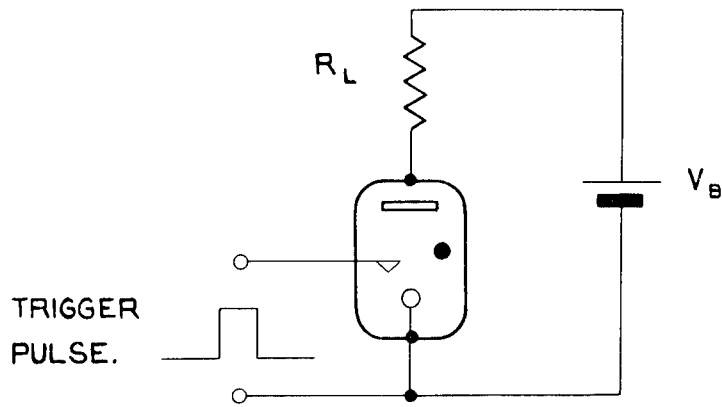
FIG.3 'V-I' PLANE DIAGRAM FOR A TYPICAL O.C.S. DEVICE



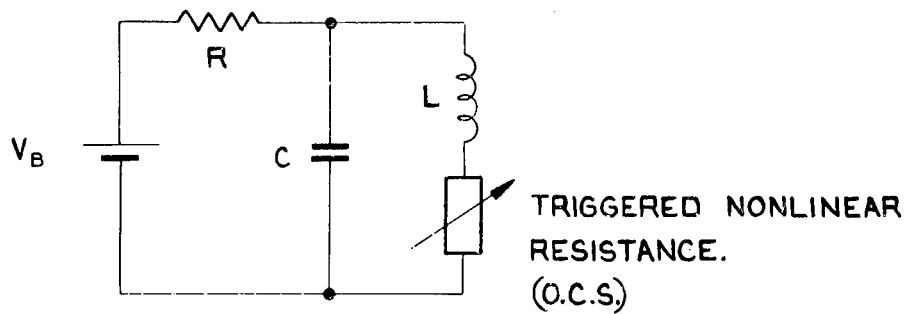
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FIG. 4 SWITCHING BY MEANS OF SUPPLY CURRENT MODULATION

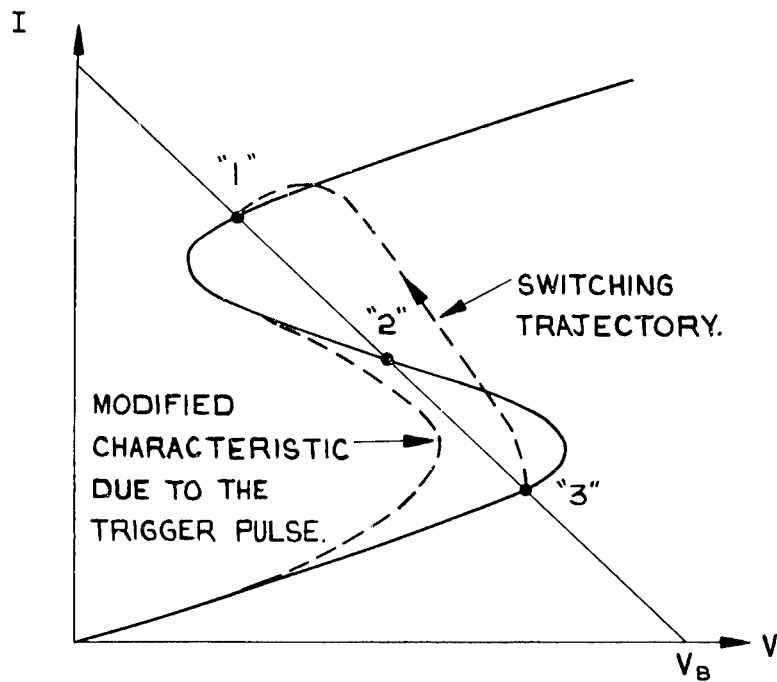
Fig.5



(a) TYPICAL CIRCUIT.

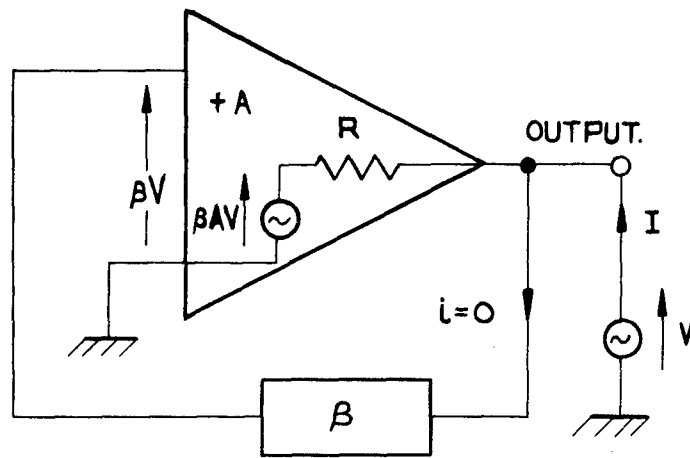


(b) EQUIVALENT CIRCUIT.



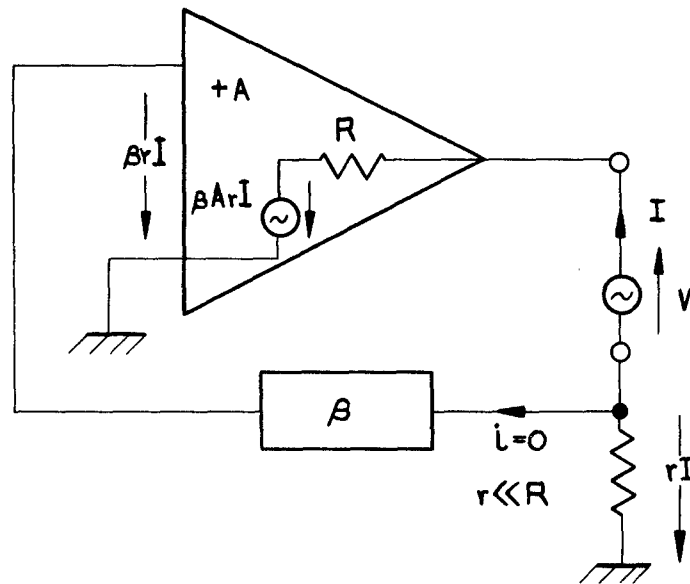
(c) GRAPHICAL SOLUTION.

FIG. 5 (a-c) SWITCHING BY MEANS OF MODIFICATION OF CHARACTERISTIC.



$$\text{OUTPUT RESISTANCE} = R_o = \frac{V}{I} = \frac{R}{1 - \beta A}$$

(a) POSITIVE VOLTAGE FEEDBACK.

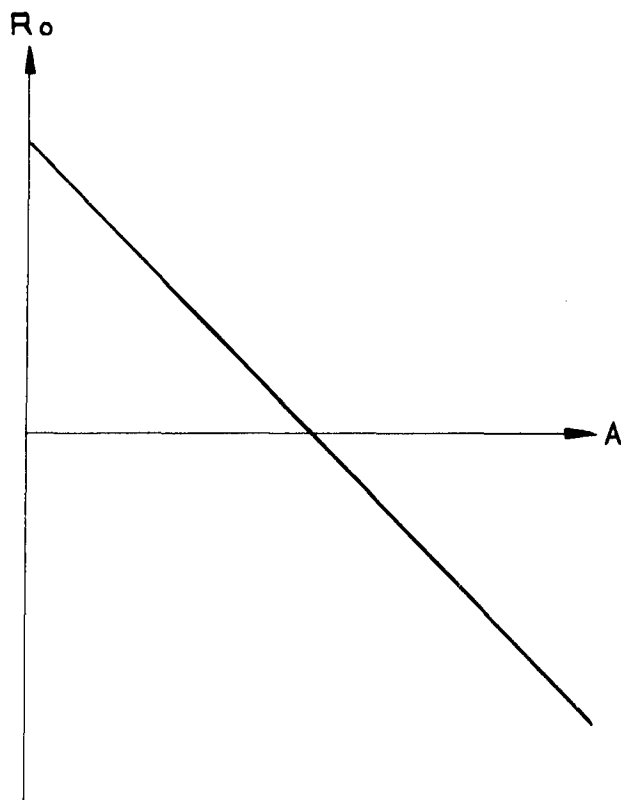
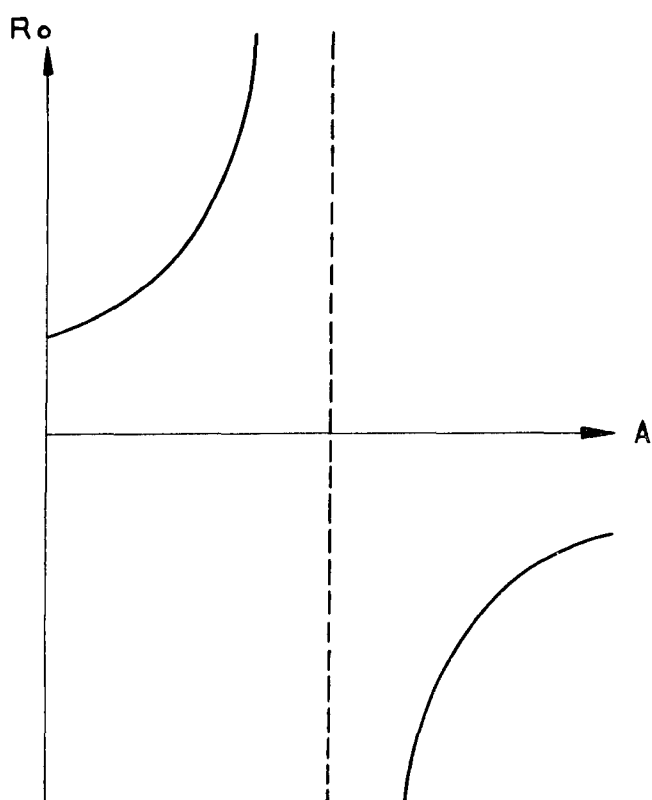


$$\text{OUTPUT RESISTANCE} = R_o = \frac{V}{I} \approx R \left(1 - \frac{\beta A r}{R} \right)$$

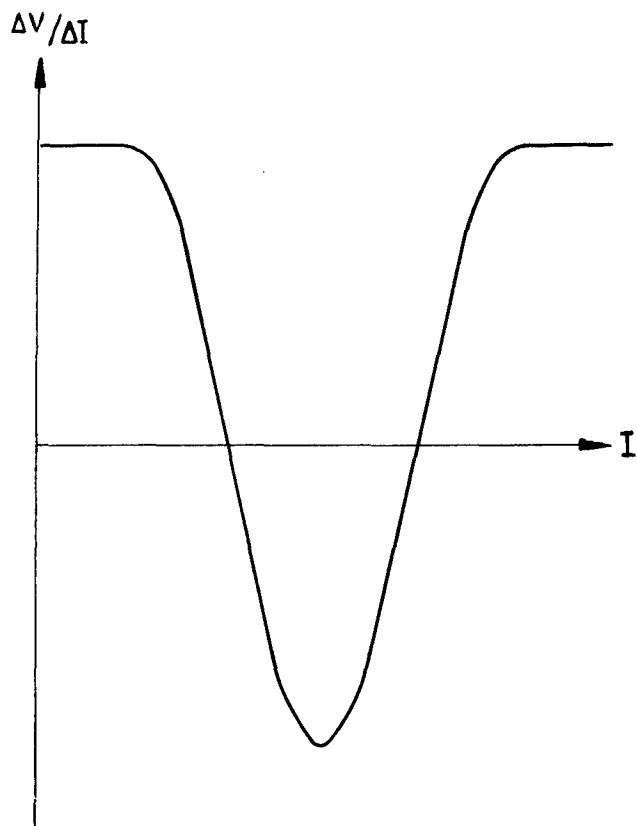
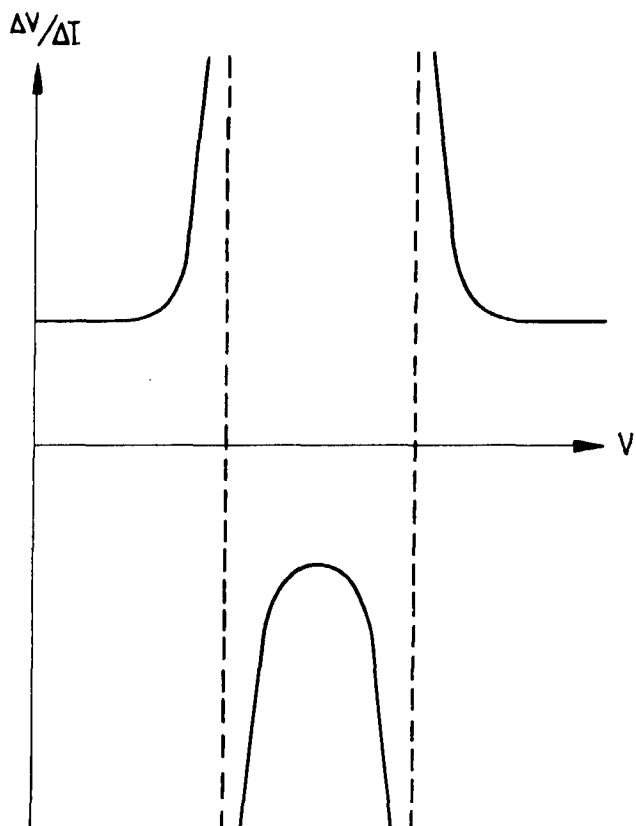
(b) POSITIVE CURRENT FEEDBACK.

FIG. 6 (a & b) SCHEMATIC DIAGRAMS OF POSITIVE FEEDBACK AMPLIFIERS.

Fig.7



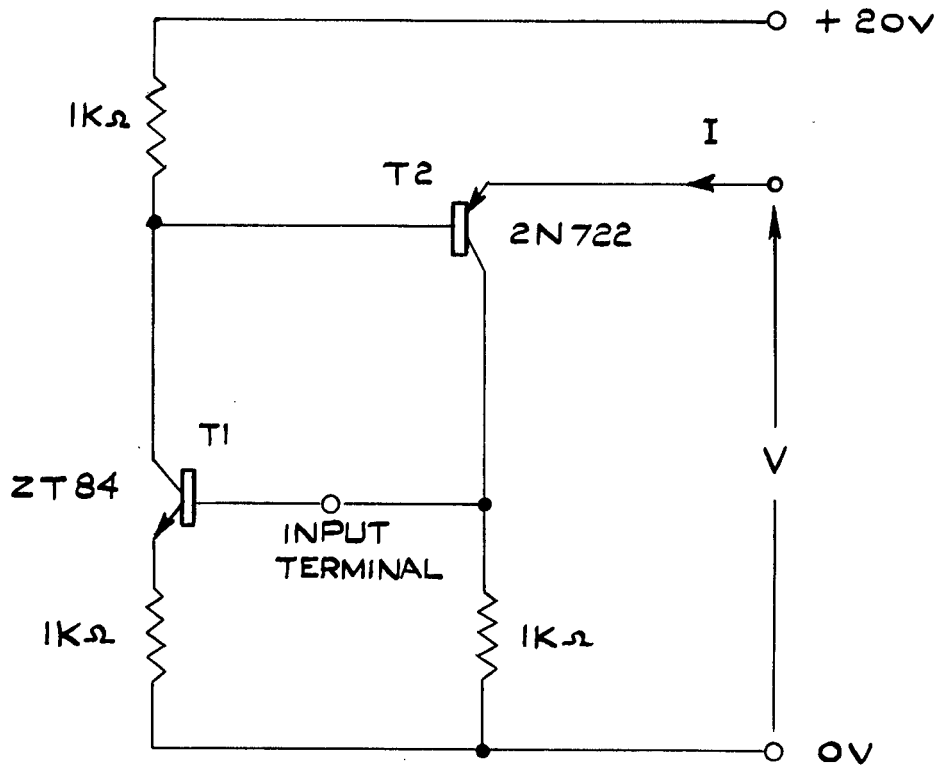
(a) VARIATION OF OUTPUT RESISTANCE WITH GAIN FOR A POSITIVE VOLTAGE FEEDBACK AMPLIFIER. (b) VARIATION OF OUTPUT RESISTANCE WITH GAIN FOR A POSITIVE CURRENT FEEDBACK AMPLIFIER.



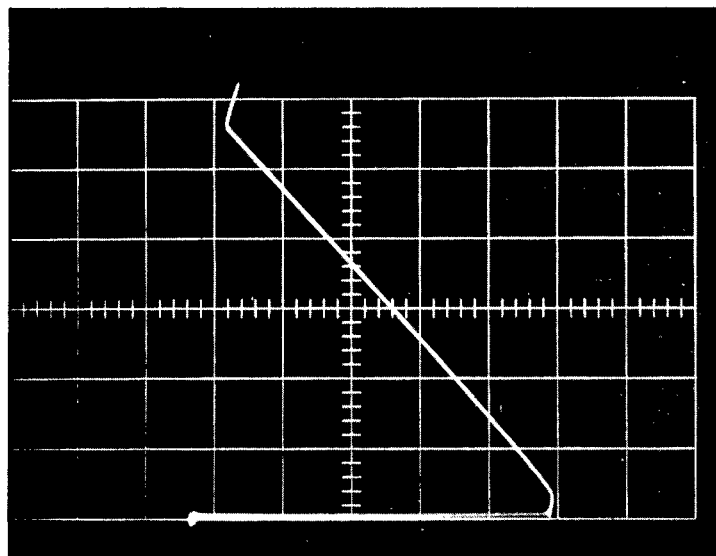
(c) VARIATION OF $\Delta V/\Delta I$ WITH V FOR A SHORT CIRCUIT STABLE DEVICE.

(d) VARIATION OF $\Delta V/\Delta I$ WITH I FOR AN OPEN CIRCUIT STABLE DEVICE.

FIG.7 (a—d) COMPARISON BETWEEN NEGATIVE RESISTANCE AND POSITIVE FEEDBACK AMPLIFIER OUTPUT RESISTANCE CHARACTERISTICS.



(a) SCHEMATIC CIRCUIT

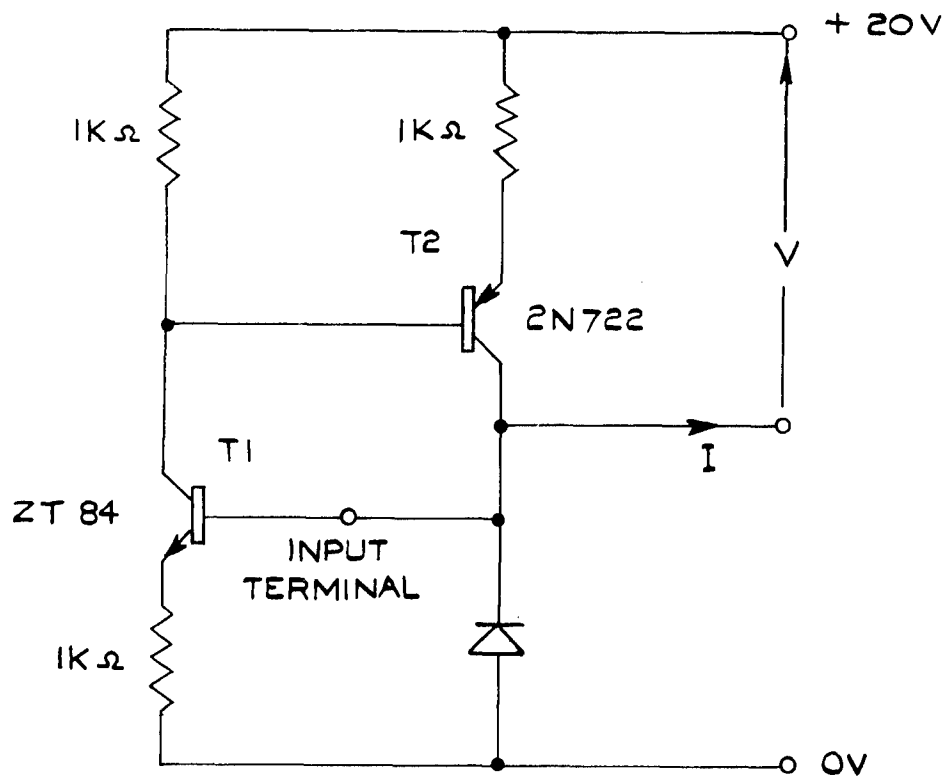


(b) OUTPUT V-I CHARACTERISTIC
(2V/div. hor. ; 2mA/div. vert.)

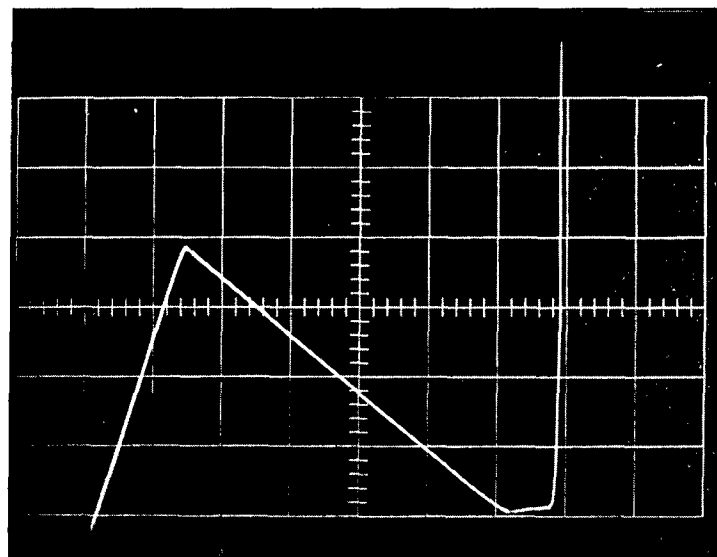
FIG.8 (a&b) SIMULATED O.C.S. CHARACTERISTIC

FIG.9

1R/P 719

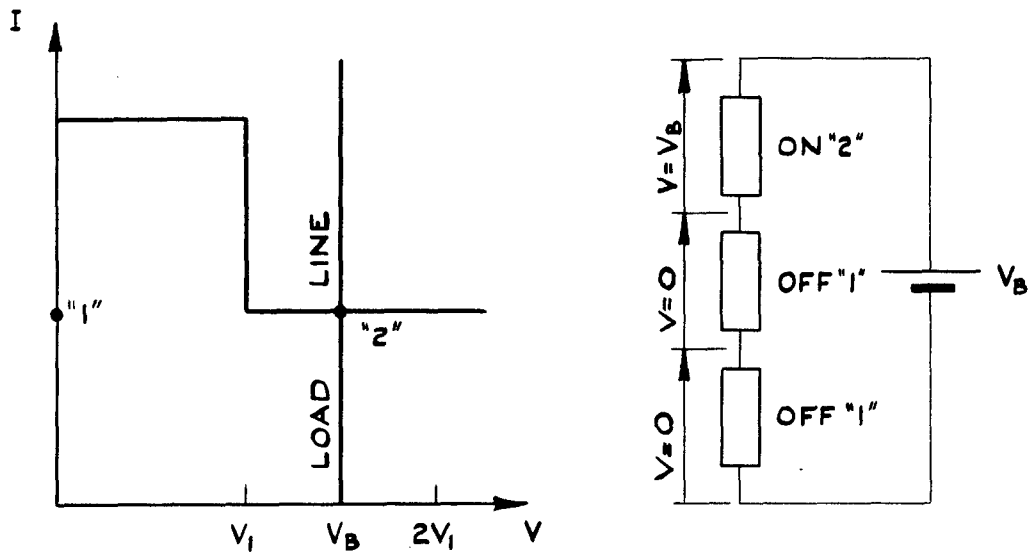


(a) SCHEMATIC CIRCUIT

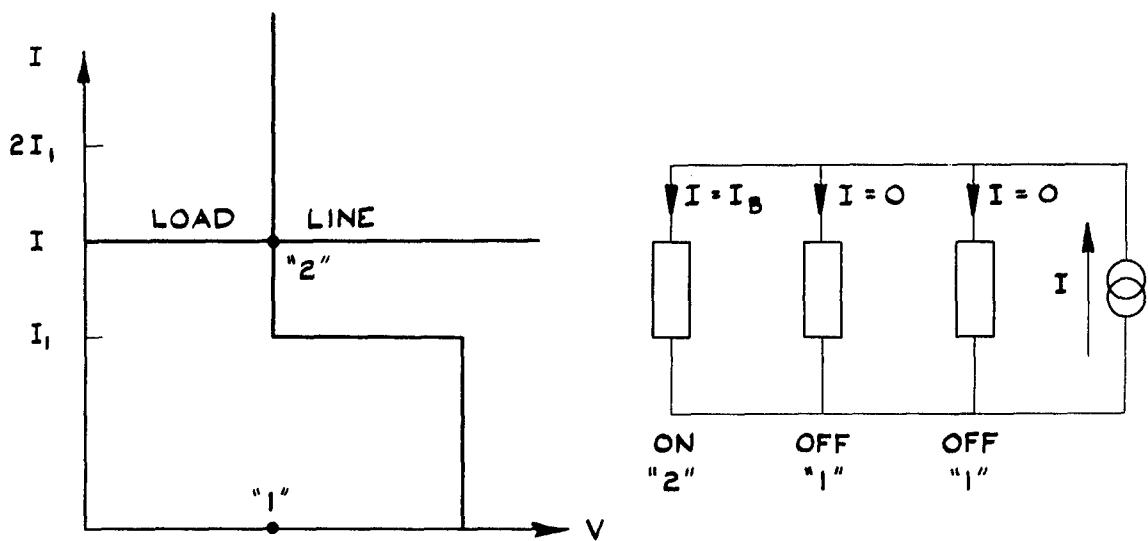


(b) OUTPUT V-I CHARACTERISTIC
(2V/div. hor. ; 2mA/div. vert.)

FIG.9 (a&b) SIMULATED S.C.S. CHARACTERISTIC

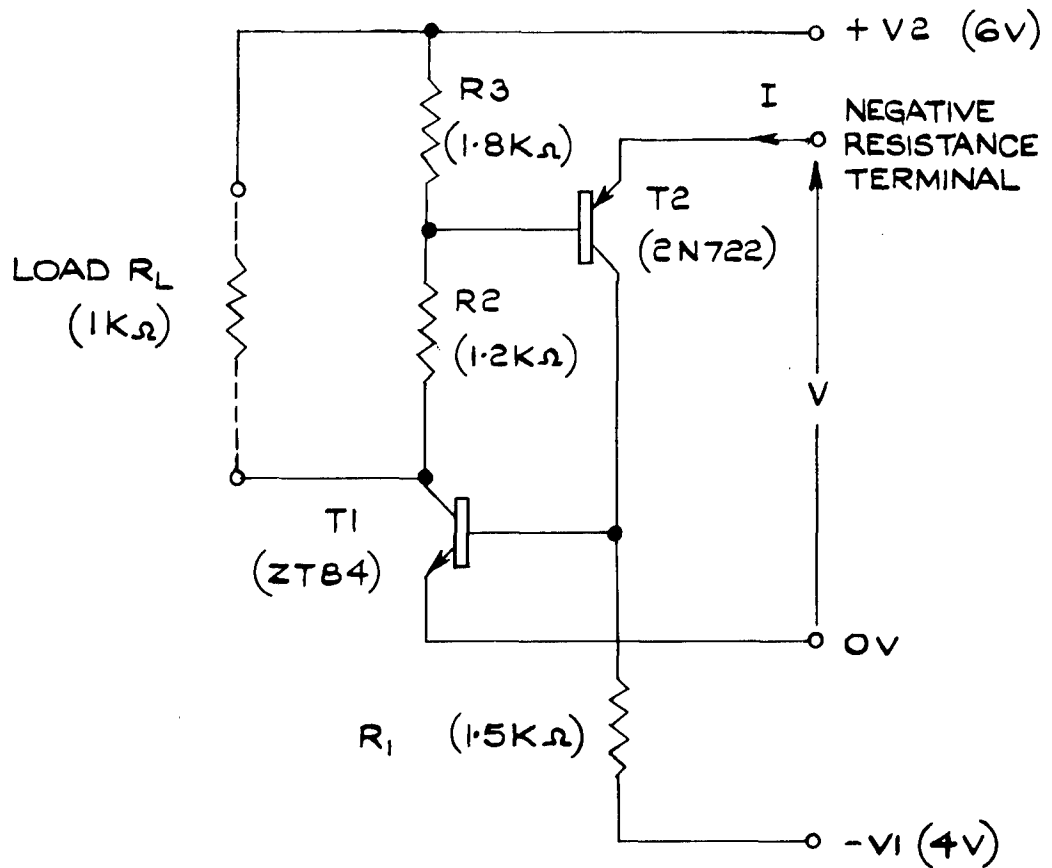


(a) S.C.S. CHARACTERISTIC AND CIRCUIT

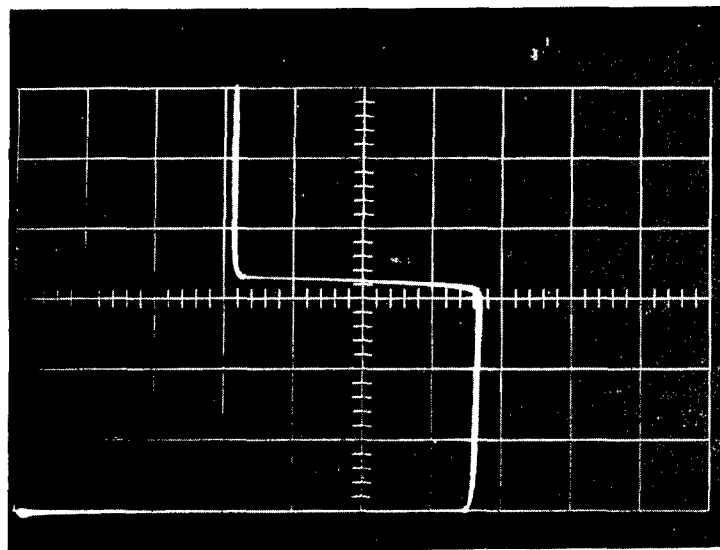


(b) O.C.S. CHARACTERISTIC AND CIRCUIT

FIG. 10 (a & b) IDEALISED NEGATIVE RESISTANCE CHARACTERISTICS SUITABLE FOR RING COUNTER APPLICATIONS



(a) CIRCUIT DIAGRAM
(EXPERIMENTAL VALUES IN BRACKETS)



(b) OUTPUT V-I CHARACTERISTIC
(1V/div.hor. ; 1mA/div. vert.)

FIG.II(a & b) BASIC RING COUNTER STAGE

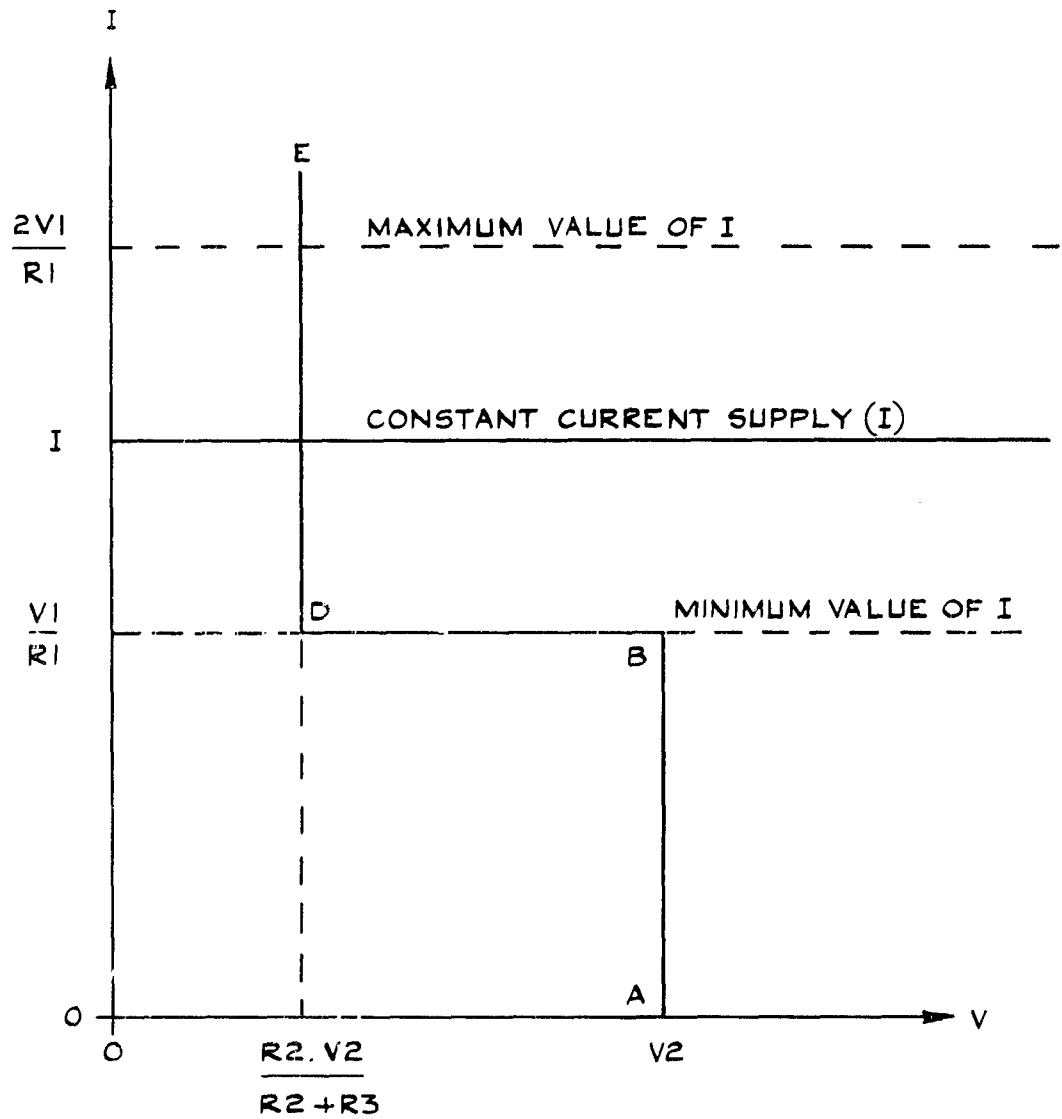


FIG. 12 DIAGRAM SHOWING THE APPROXIMATE VALUES OF THE PARAMETERS OF THE BASIC STAGE OF FIG. II

Fig.13

IR/P 723

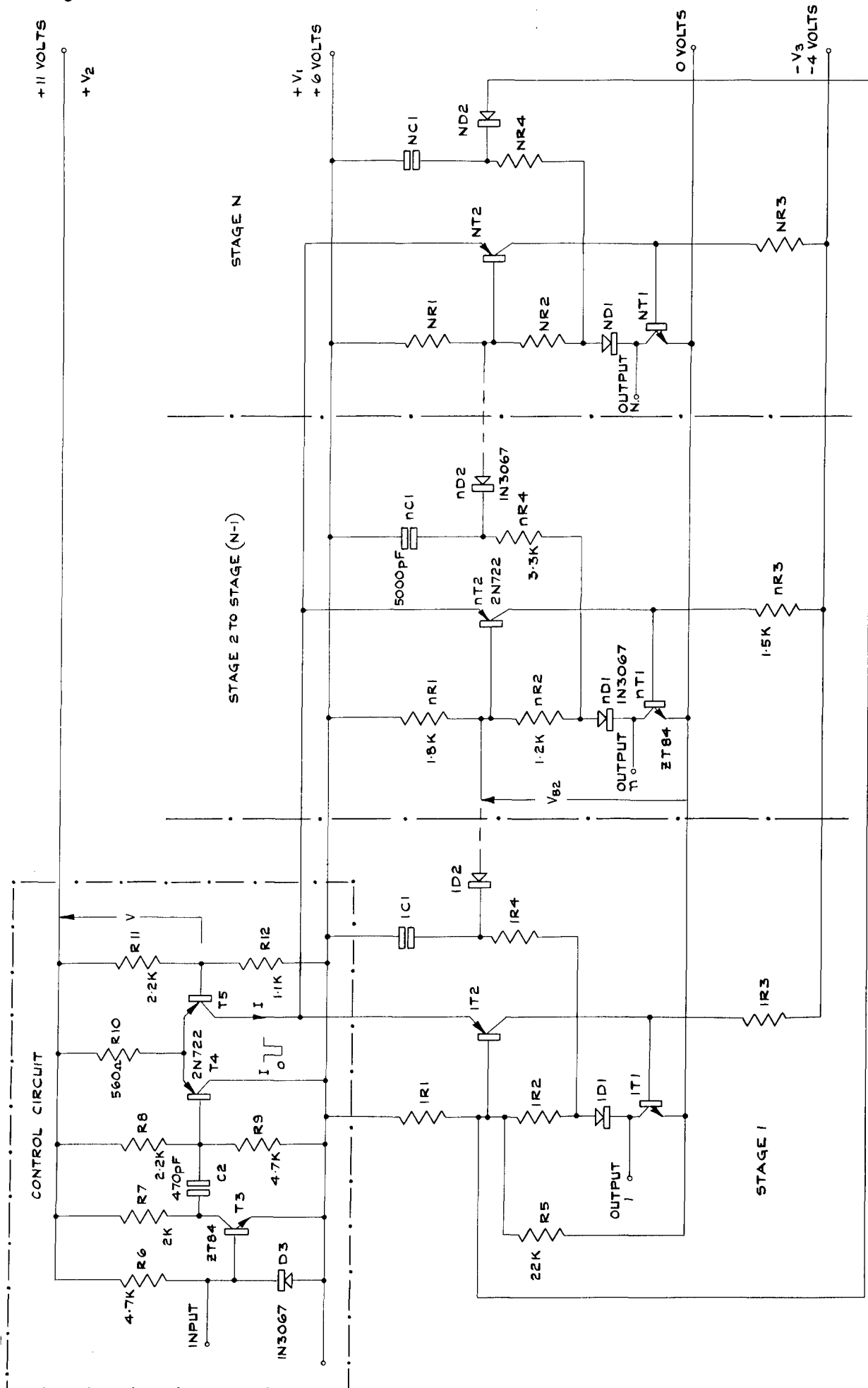
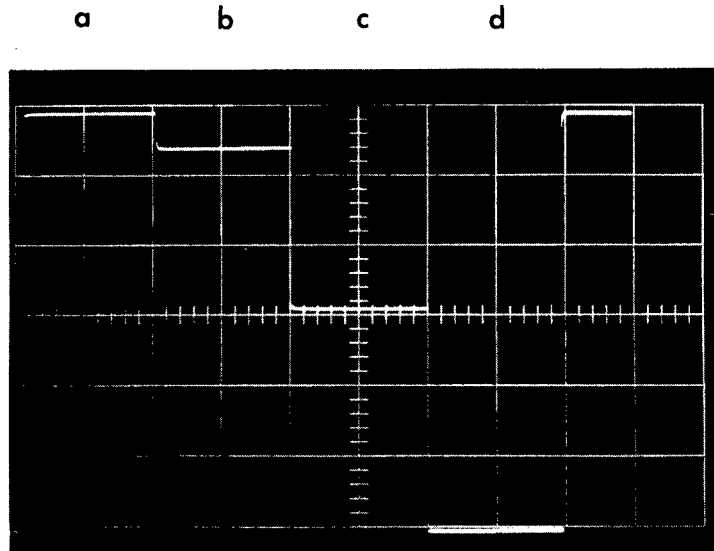


FIG. 13 CIRCUIT DIAGRAM OF N-WAY BASIC RING COUNTER



THE FOUR PERMISSIBLE VOLTAGE LEVELS FOR THE BASE OF nT_2 (V_{B2}).

- (a) +6 VOLTS WHEN STAGE IS OFF.
- (b) +5.7 VOLTS, ON STAGE FOLLOWING A STAGE WITH MEMORY (RESIDUAL MEMORY).
- (c) +4.5 VOLTS, ON THE STAGE WITH MEMORY VOLTAGE APPLIED.
- (d) +3.0 VOLTS, WHEN STAGE IS ON.

(1 VOLT/DIV. VERT. 0.5 MILLISEC/DIV. HOR.)
 BIT RATE 1 MILLISEC

Fig. 14 Photograph of Base Waveform

Fig.15

IR/P 724

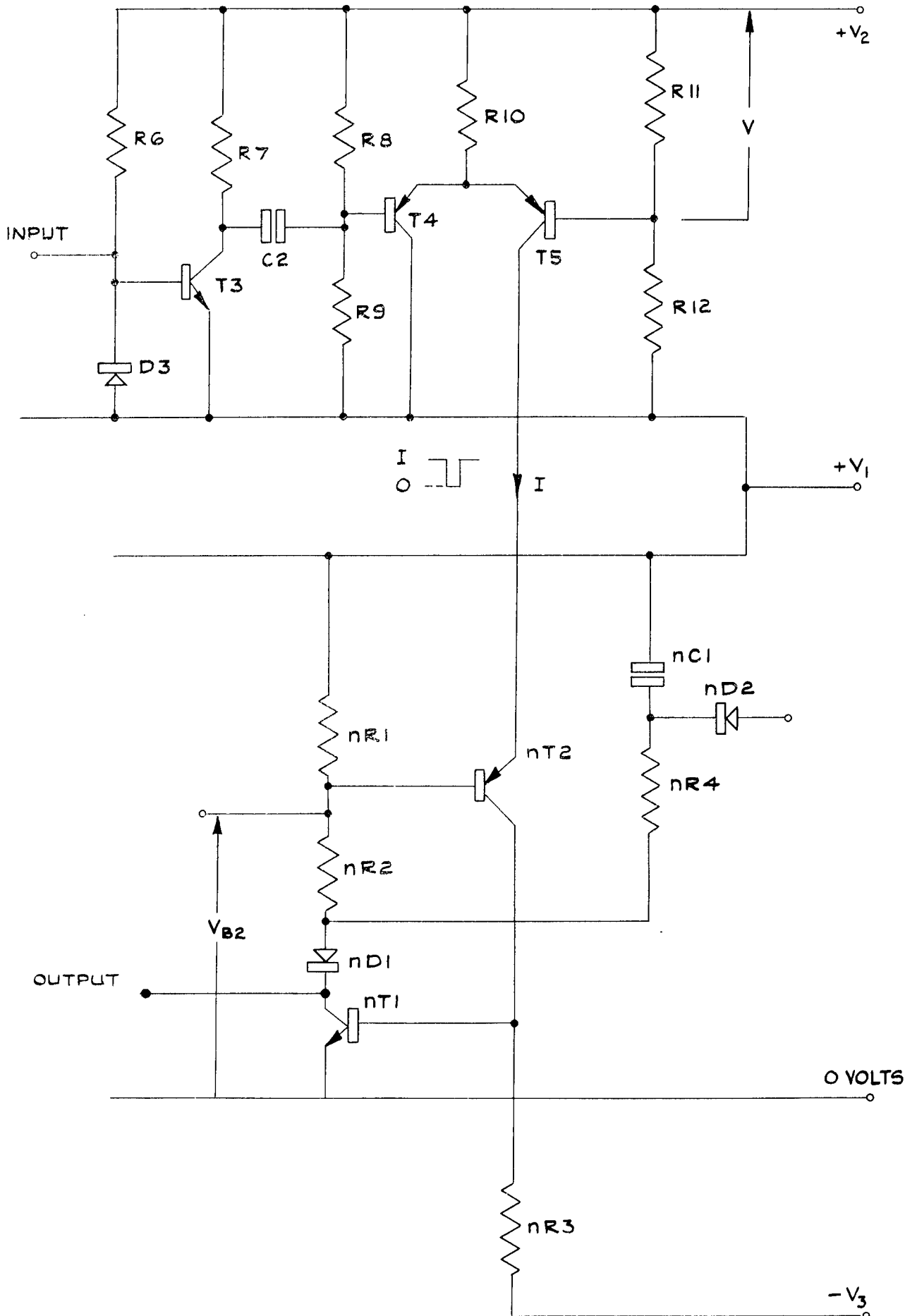


FIG. 15 CONTROL UNIT AND RING ELEMENT

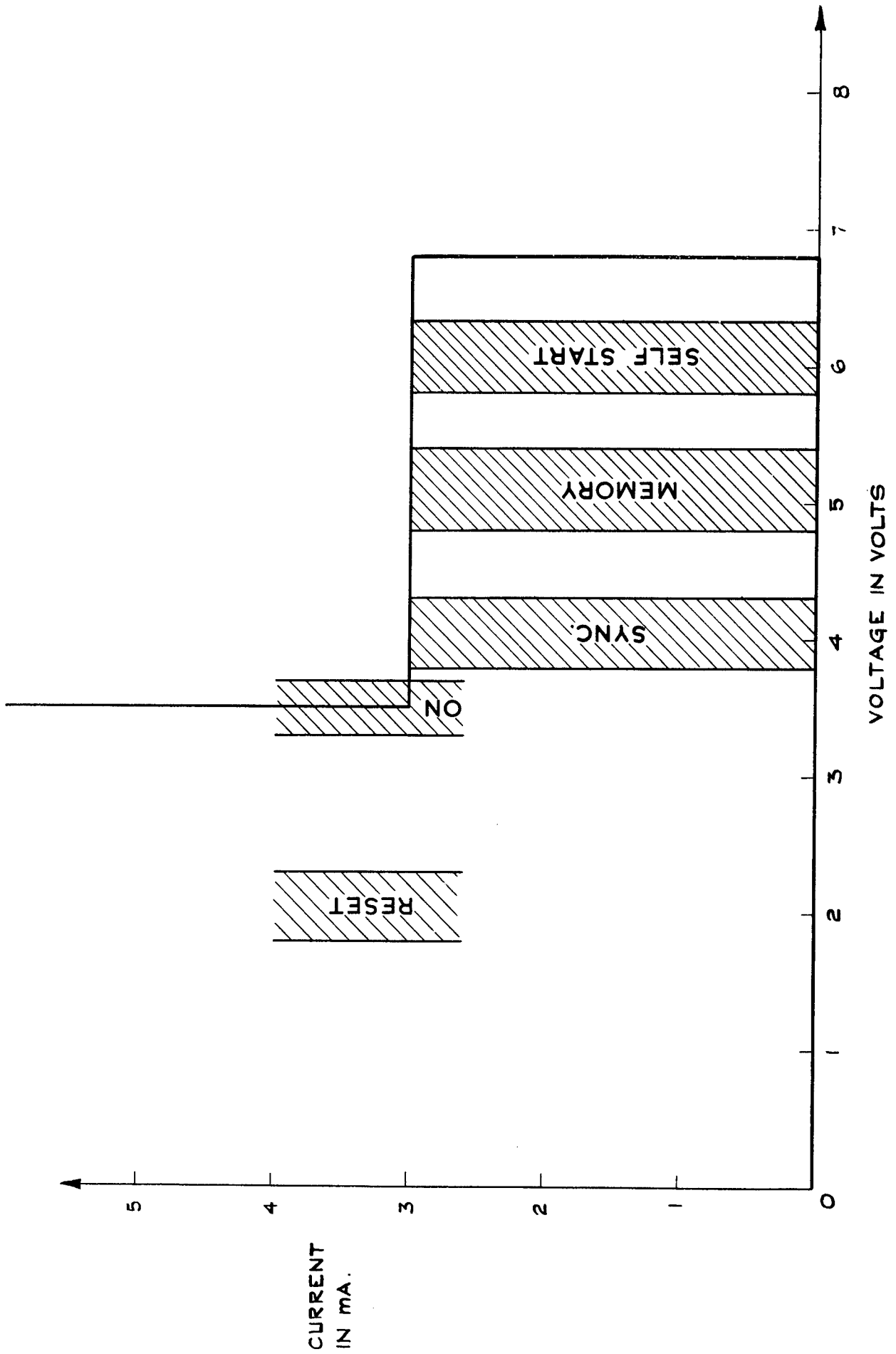


FIG. 16 MODIFICATION OF CHARACTERISTIC OF RING ELEMENT

Fig.17

1R/P 726

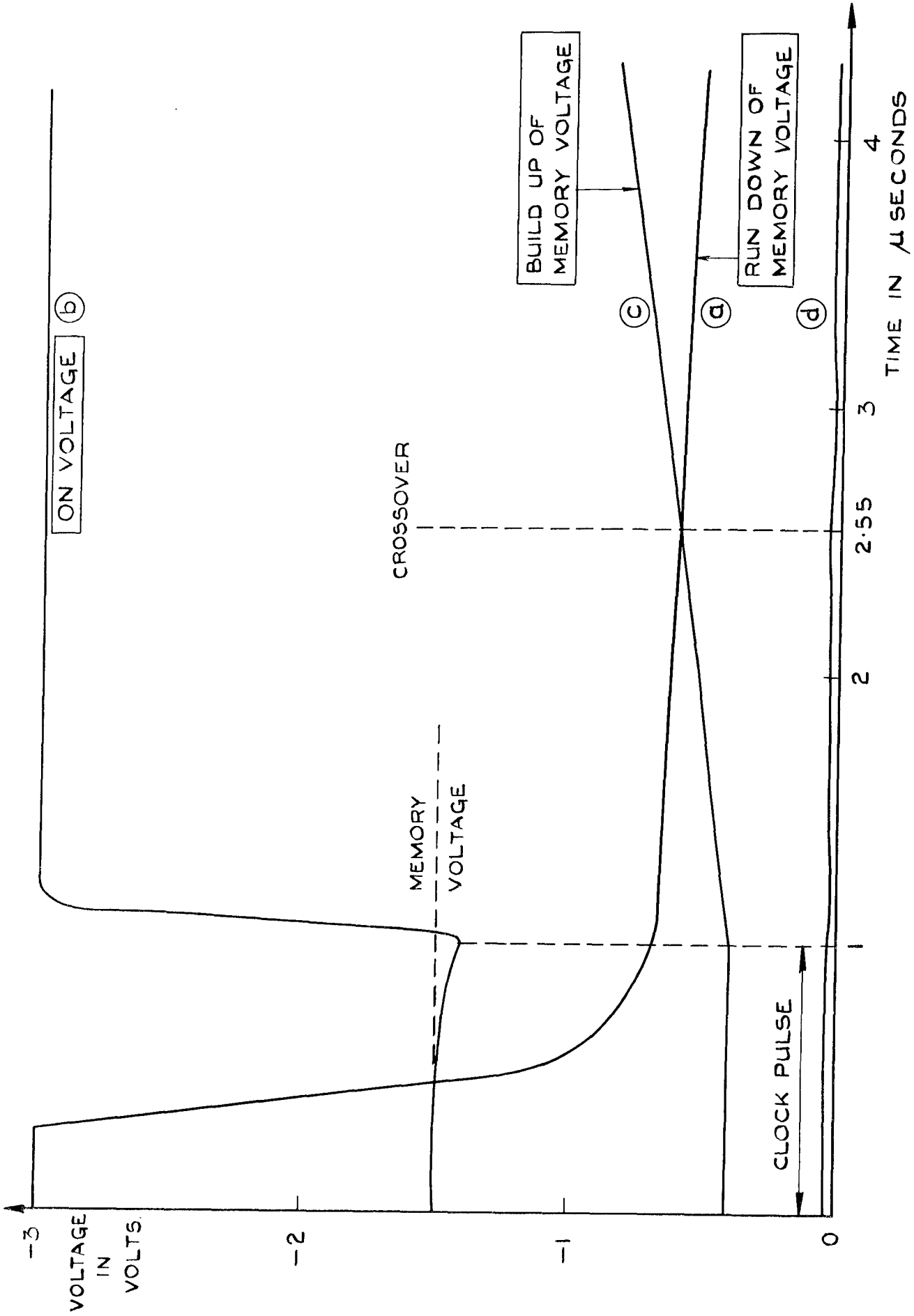


FIG.17 BASE WAVEFORM OF nT2 W.R.T. THE +6 VOLT LINE

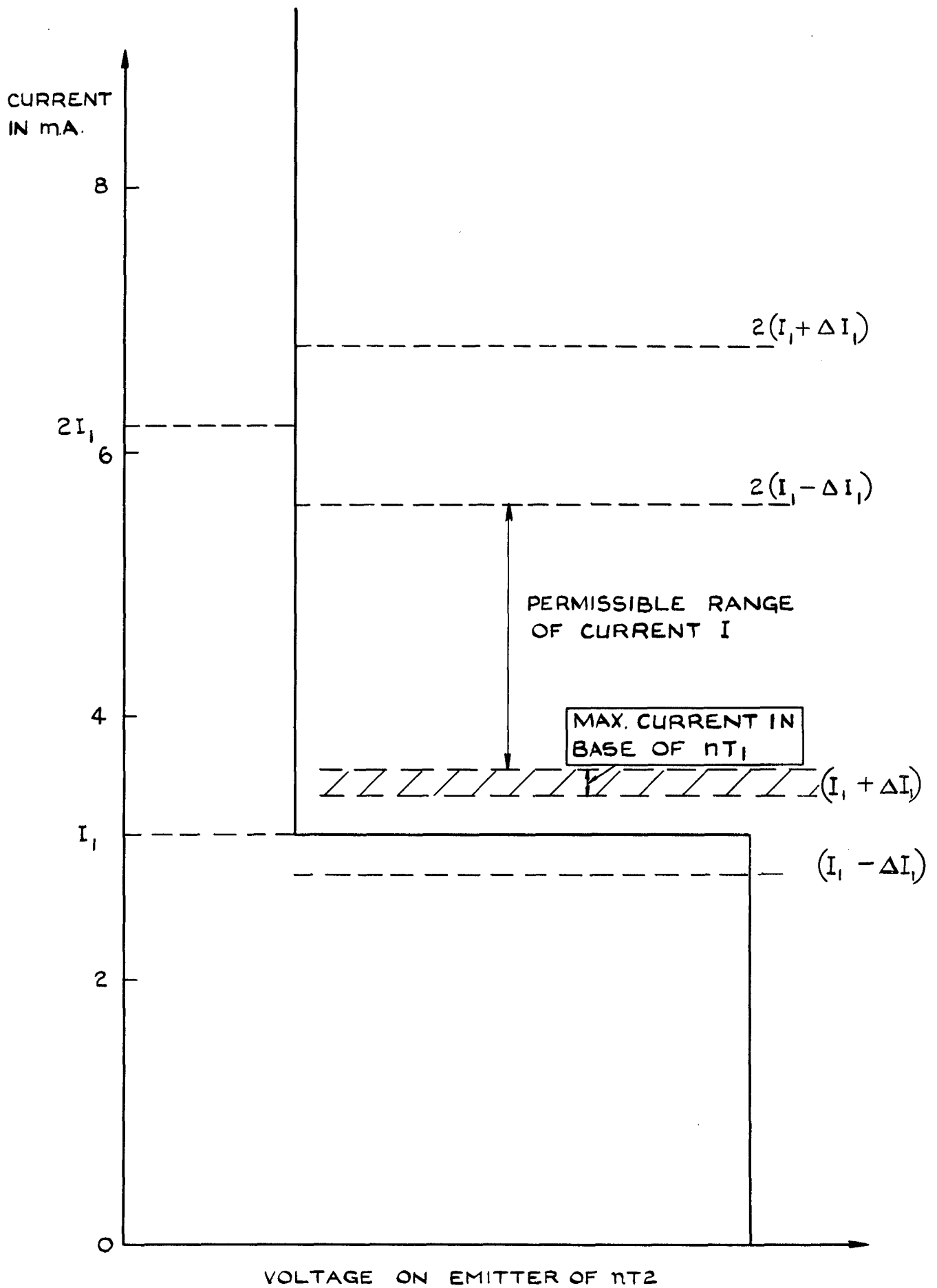


FIG.18 PRACTICAL DIVISION OF CURRENT I

Fig.19

IR/P 728

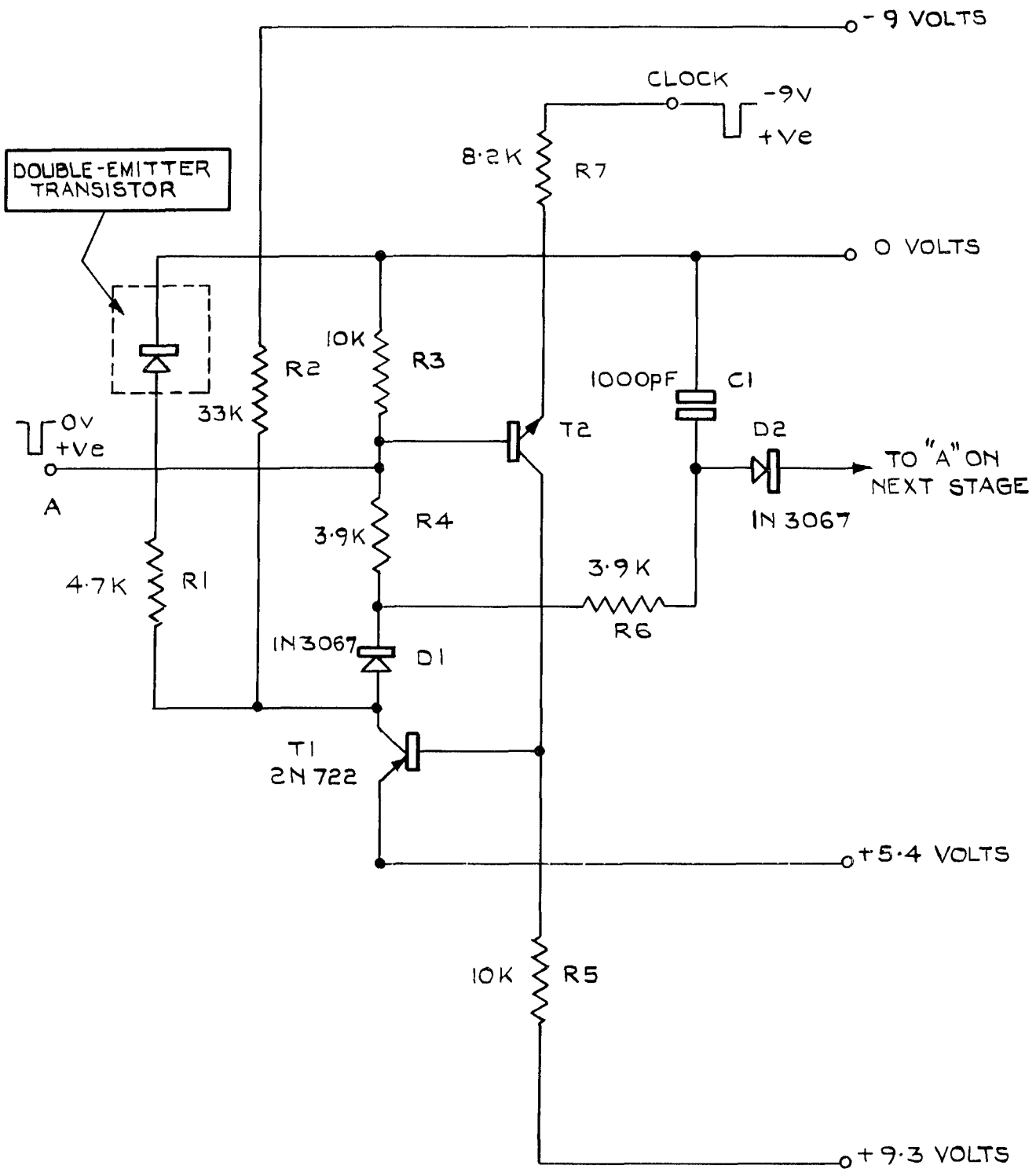


FIG. 19 FLOATING SLAVE RING

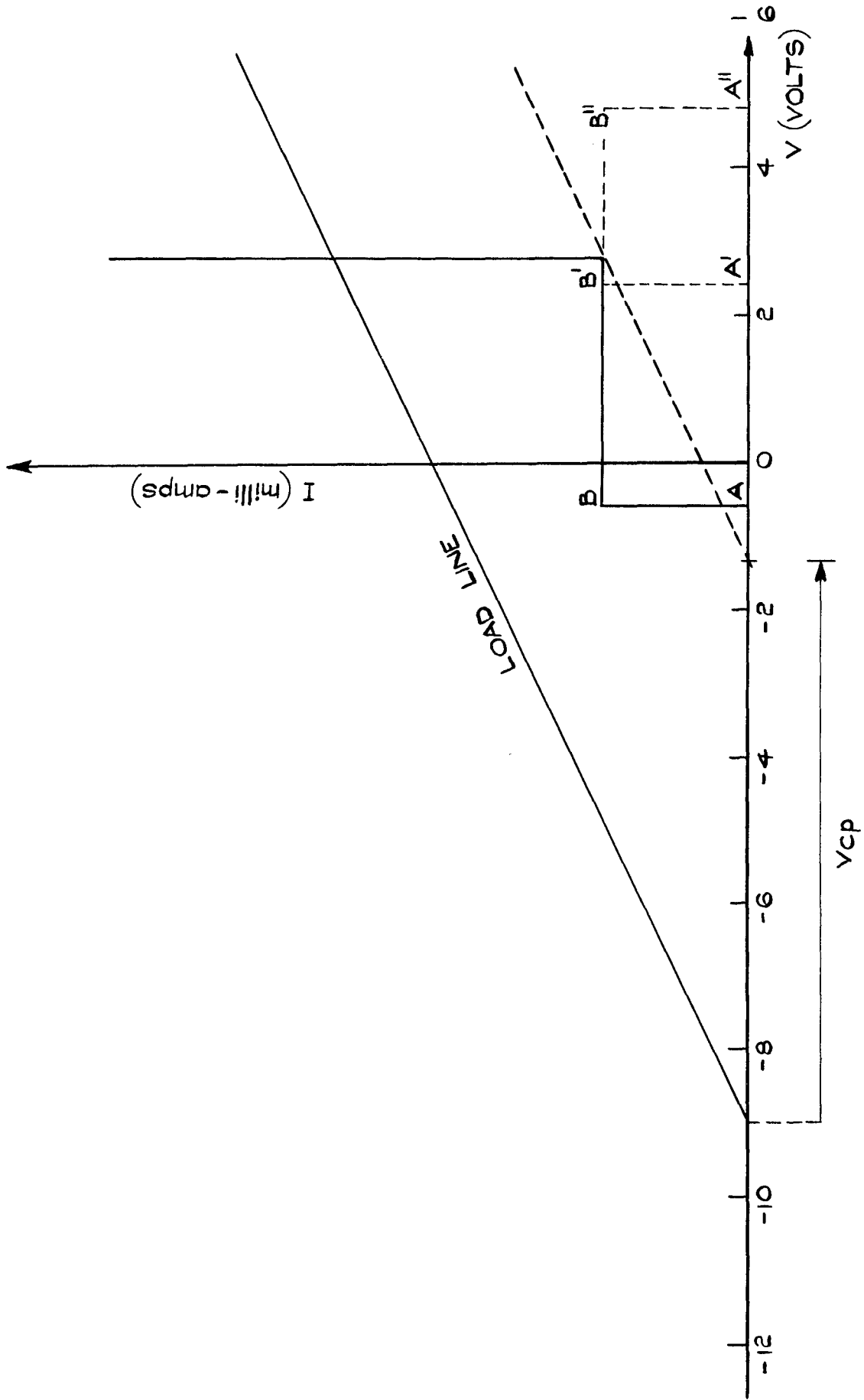
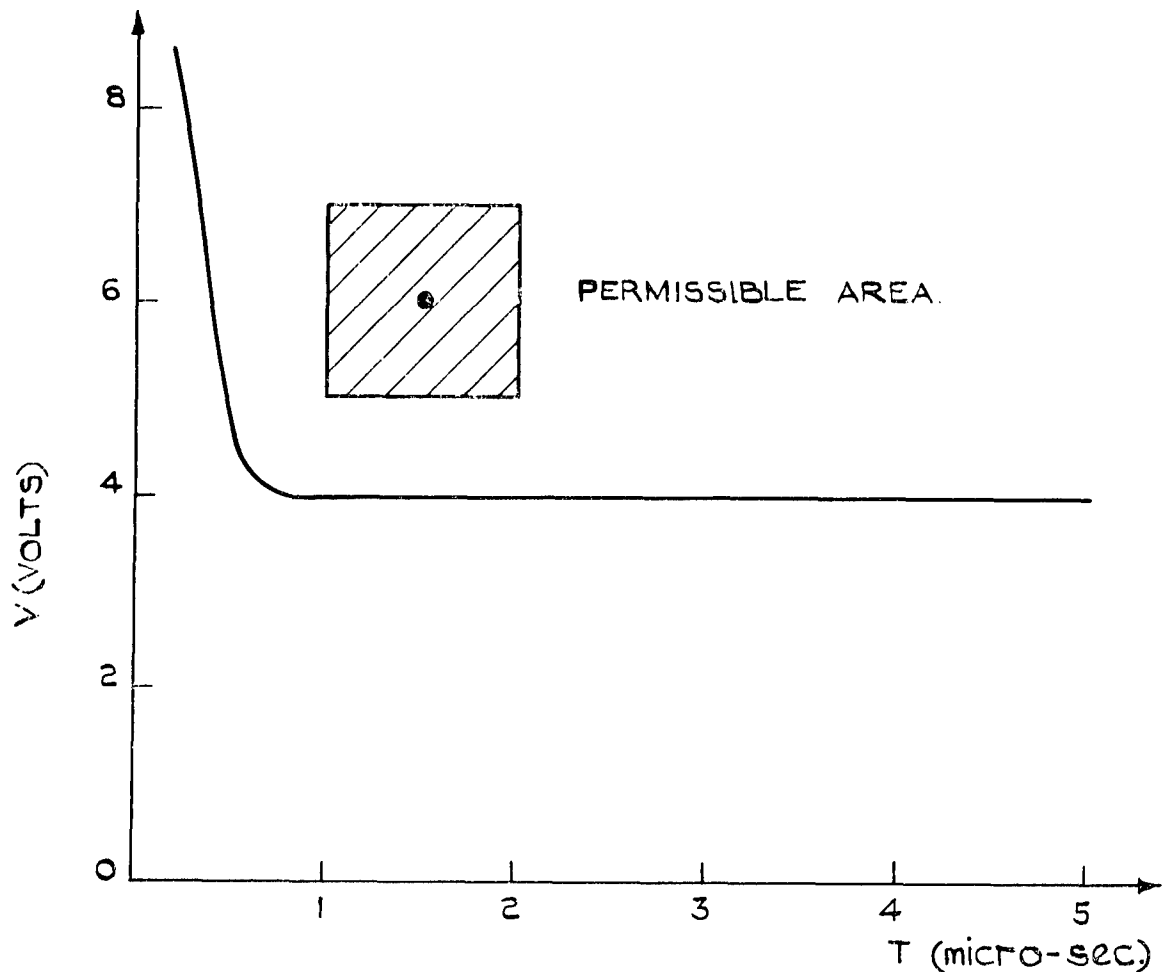


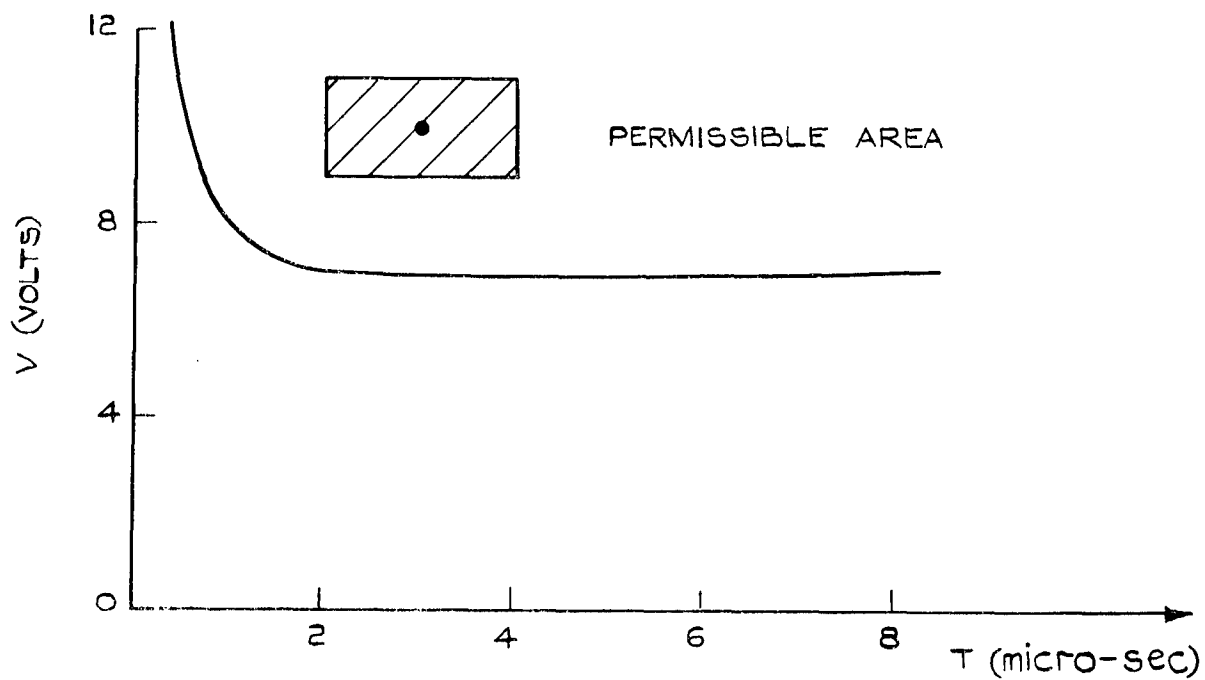
FIG. 20 NEGATIVE RESISTANCE CHARACTERISTICS OF SLAVE RING ELEMENT

Fig.21

IR/P 730

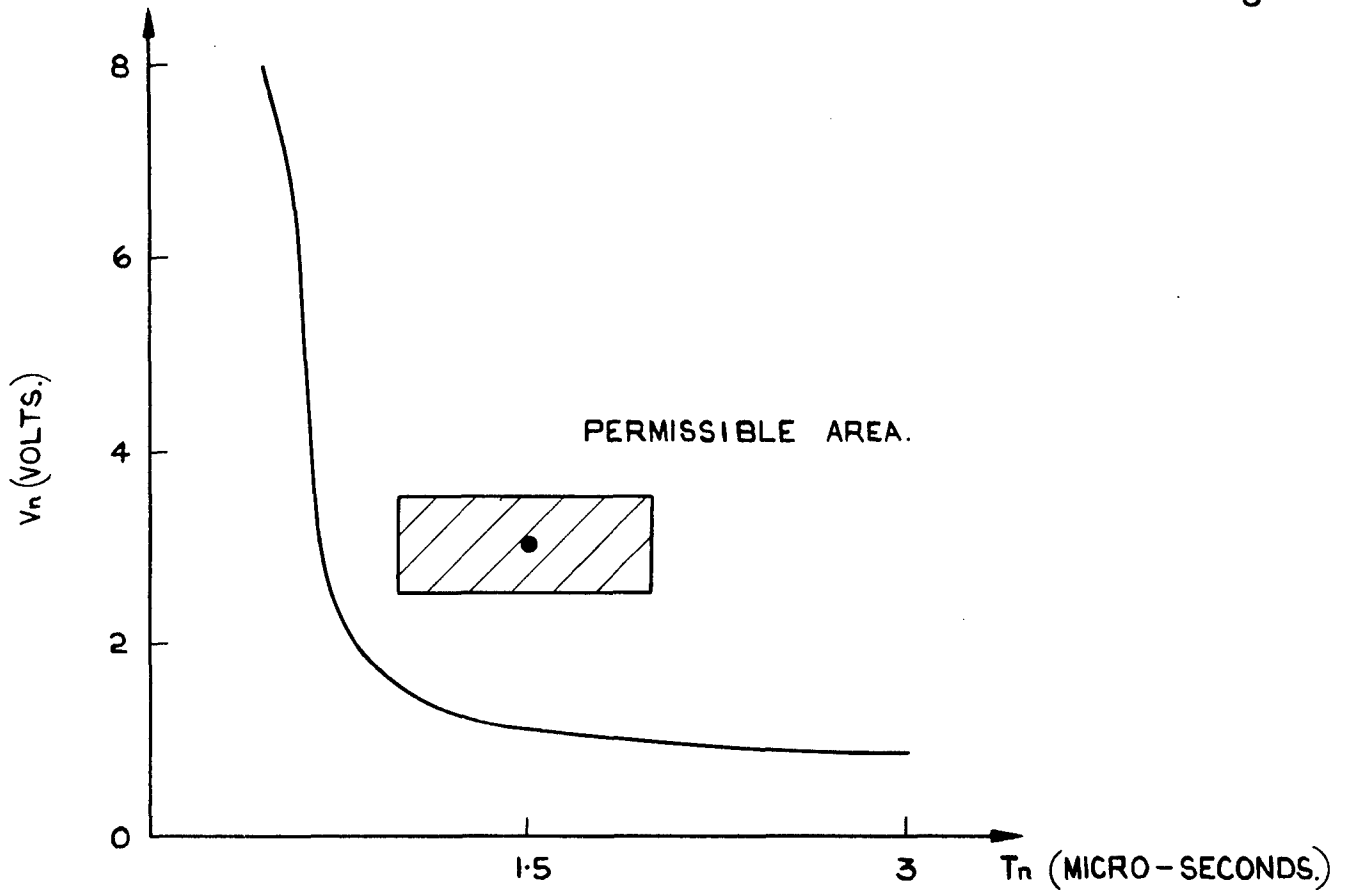


(a) RESET PULSE

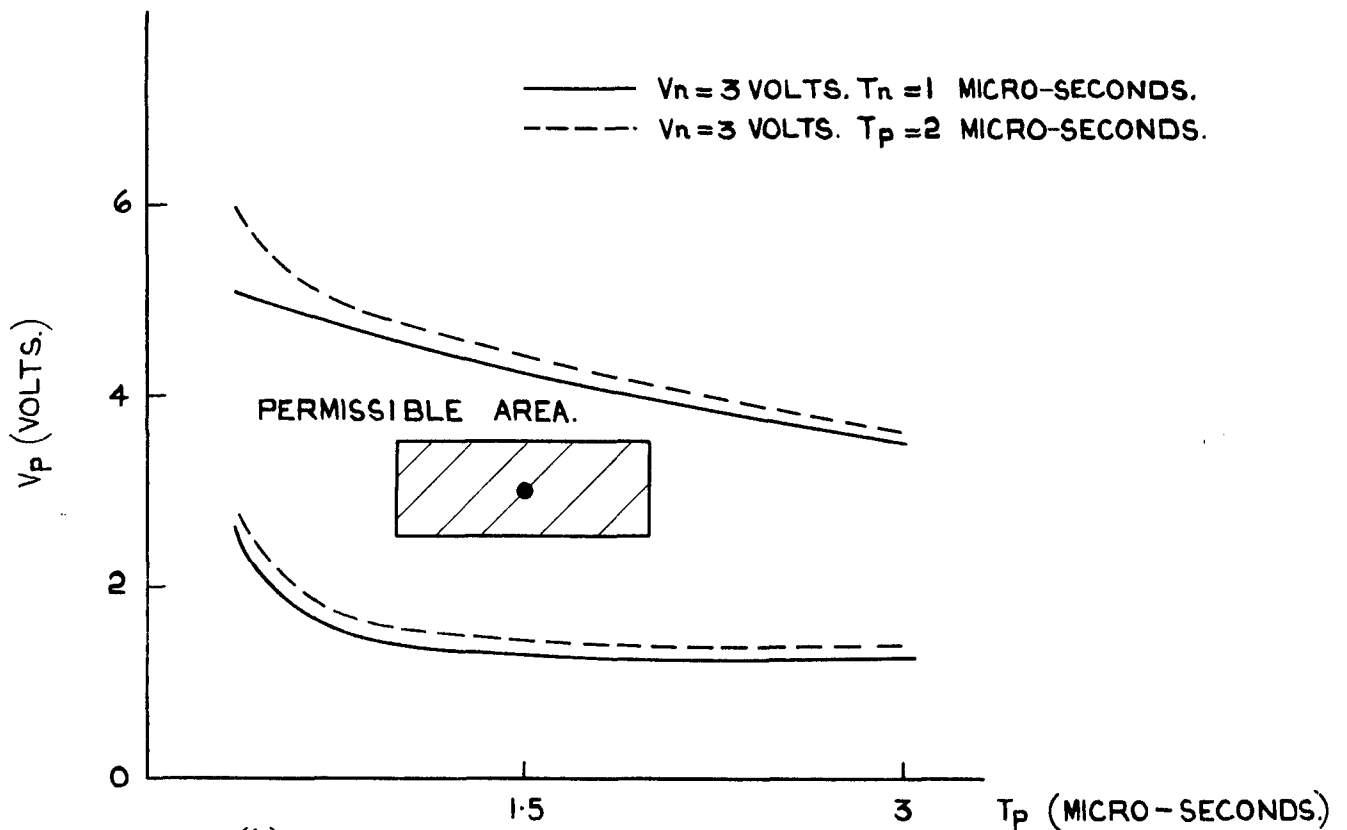


(b) CLOCK PULSE

FIG 21(a&b) AMPLITUDE AGAINST PULSE LENGTH FOR CLOCK AND RESET PULSES

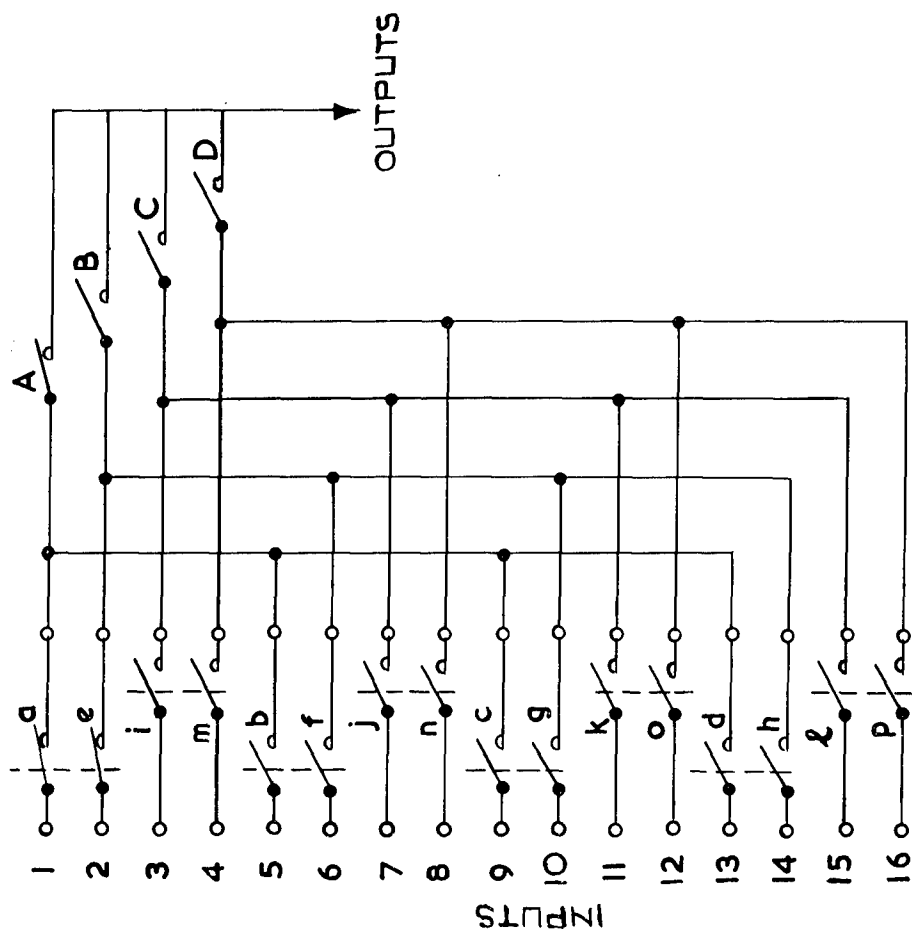


(a) MINIMUM NEGATIVE PULSE AMPLITUDE AGAINST PULSE LENGTH.

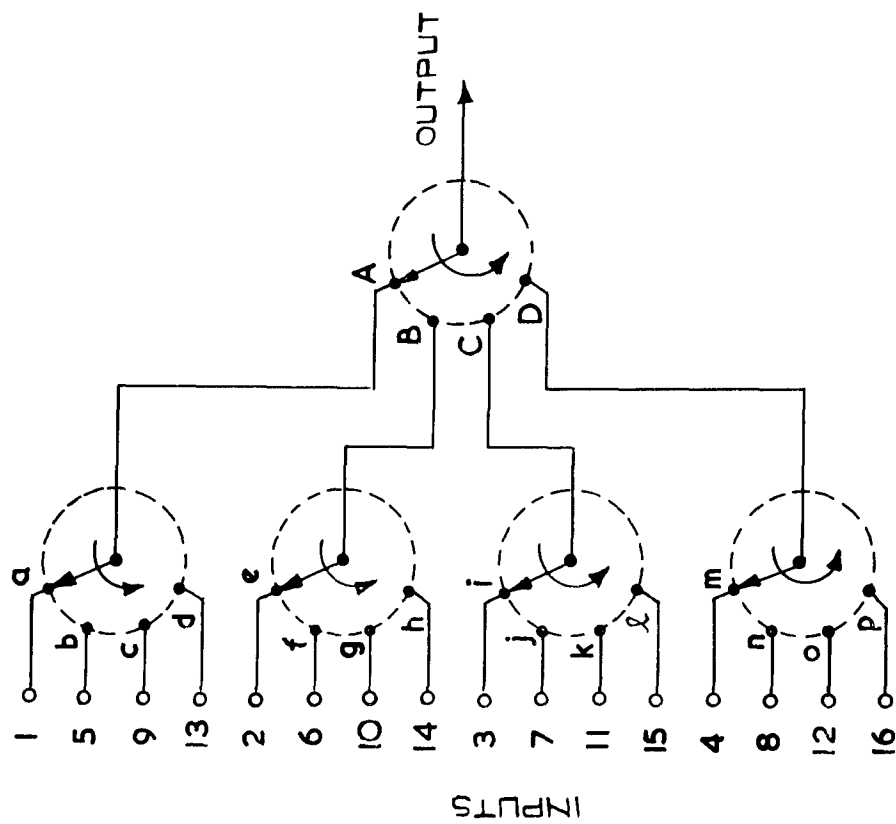


(b) MAXIMUM & MINIMUM POSITIVE PULSE AMPLITUDE AGAINST PULSE LENGTH.

FIG. 24 (a&b) AMPLITUDE AGAINST PULSE LENGTH GRAPH FOR POSITIVE AND NEGATIVE PULSES.



(b) CIRCUIT SHOWING GANGING OF PAIRS OF LOW SPEED SWITCHES



(a) SCHEMATIC DIAGRAM

FIG.25 (a & b) TWO TO ONE INTERLACED 4 X 4 SUBMULTIPLYING SYSTEM

KEY:-

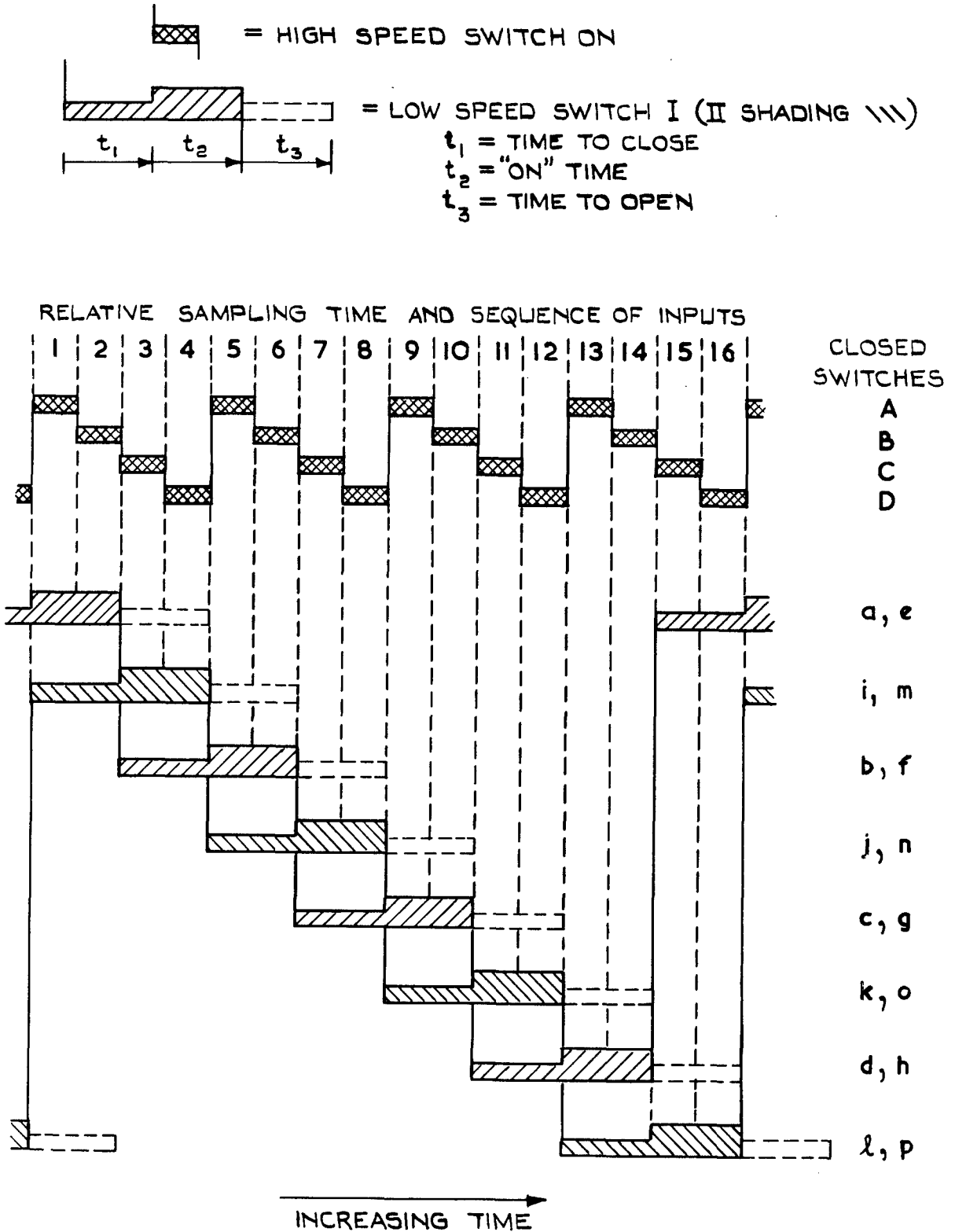


FIG.26 TIMING DIAGRAM FOR THE SUBMULTIPLEXING SYSTEM SHOWN IN FIG. 25

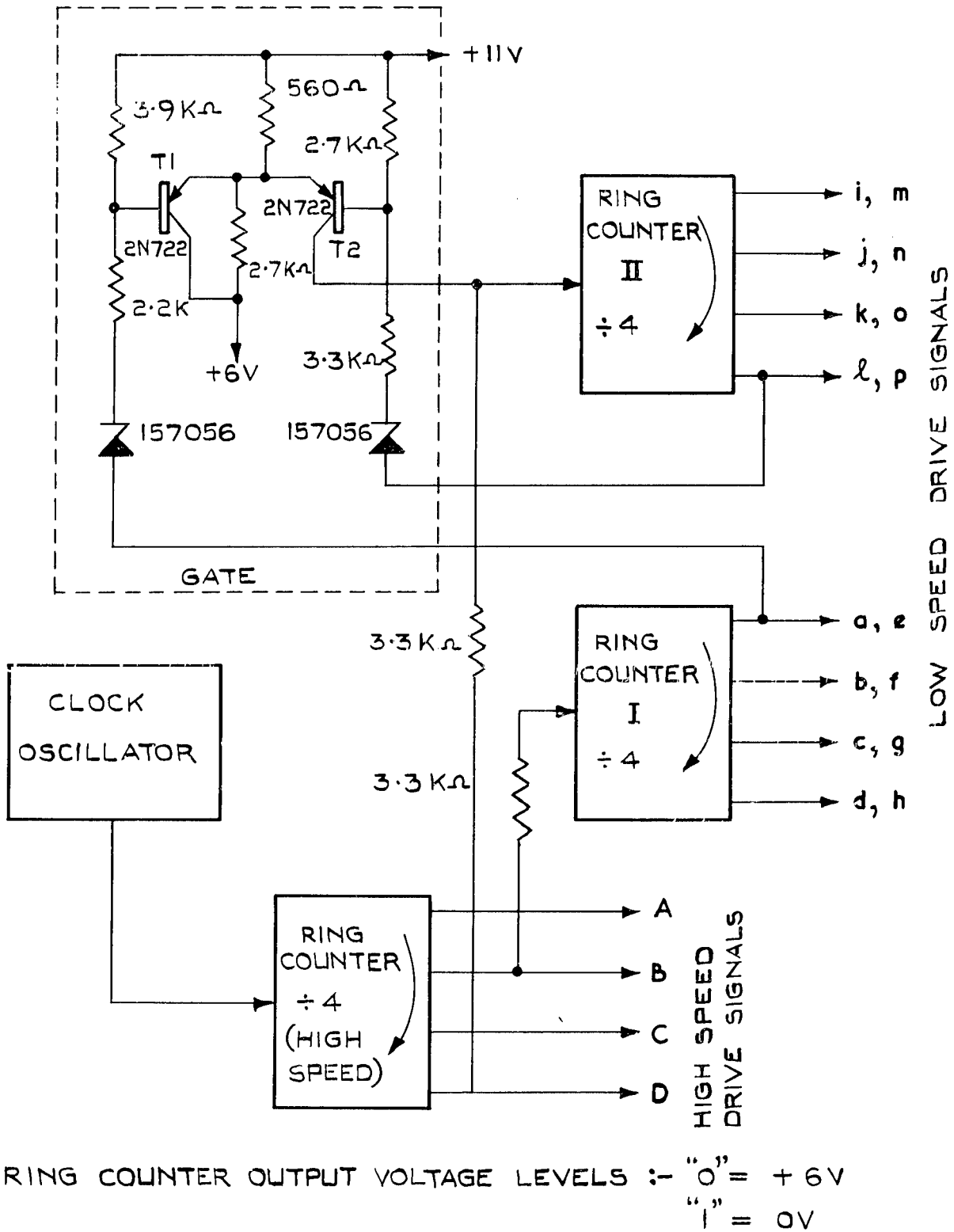


FIG. 27 SUBMULTIPLEXING SEQUENTIAL WAVEFORM GENERATOR

<p>Lowe, G. C. Thomas, D.</p> <p>621.374.32 : 621.373.422</p> <p>SOME APPLICATIONS OF SYNTHESISED NEGATIVE RESISTANCE CHARACTERISTICS TO RING COUNTER DESIGN</p> <p>Royal Aircraft Establishment Technical Report 65208 September 1965</p> <p>The large signal bistable properties of negative resistance devices are described and the simulation of negative resistance devices using positive feedback amplifiers is discussed. The form of an ideal characteristic for "unique bit" ring counter applications is suggested and a practical circuit that fulfills the requirements is proposed. Circuit details of a basic ring counter, a slave ring counter, and a shift register are given and important design criteria are presented. A method of generating interlaced sequential waveforms is described for a system using time division sub-multiplexing of input data.</p>	<p>Lowe, G. C. Thomas, D.</p> <p>621.374.32 : 621.373.422</p> <p>SOME APPLICATIONS OF SYNTHESISED NEGATIVE RESISTANCE CHARACTERISTICS TO RING COUNTER DESIGN</p> <p>Royal Aircraft Establishment Technical Report 65208 September 1965</p> <p>The large signal bistable properties of negative resistance devices are described and the simulation of negative resistance devices using positive feedback amplifiers is discussed. The form of an ideal characteristic for "unique bit" ring counter applications is suggested and a practical circuit that fulfills the requirements is proposed. Circuit details of a basic ring counter, a slave ring counter, and a shift register are given and important design criteria are presented. A method of generating interlaced sequential waveforms is described for a system using time division sub-multiplexing of input data.</p>
<p>Lowe, G. C. Thomas, D.</p> <p>621.374.32 : 621.373.422</p> <p>SOME APPLICATIONS OF SYNTHESISED NEGATIVE RESISTANCE CHARACTERISTICS TO RING COUNTER DESIGN</p> <p>Royal Aircraft Establishment Technical Report 65208 September 1965</p> <p>The large signal bistable properties of negative resistance devices are described and the simulation of negative resistance devices using positive feedback amplifiers is discussed. The form of an ideal characteristic for "unique bit" ring counter applications is suggested and a practical circuit that fulfills the requirements is proposed. Circuit details of a basic ring counter, a slave ring counter, and a shift register are given and important design criteria are presented. A method of generating interlaced sequential waveforms is described for a system using time division sub-multiplexing of input data.</p>	<p>Lowe, G. C. Thomas, D.</p> <p>621.374.32 : 621.373.422</p> <p>SOME APPLICATIONS OF SYNTHESISED NEGATIVE RESISTANCE CHARACTERISTICS TO RING COUNTER DESIGN</p> <p>Royal Aircraft Establishment Technical Report 65208 September 1965</p> <p>The large signal bistable properties of negative resistance devices are described and the simulation of negative resistance devices using positive feedback amplifiers is discussed. The form of an ideal characteristic for "unique bit" ring counter applications is suggested and a practical circuit that fulfills the requirements is proposed. Circuit details of a basic ring counter, a slave ring counter, and a shift register are given and important design criteria are presented. A method of generating interlaced sequential waveforms is described for a system using time division sub-multiplexing of input data.</p>