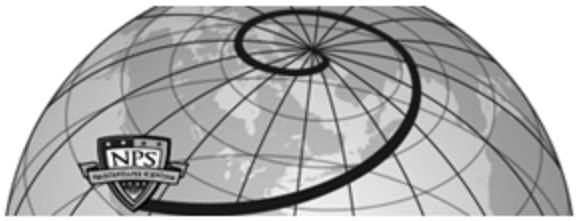
Calhoun
Institutional Archive of the Naval Postgraduate School



Author(s)	Cook, John H.
Title	Boolean minimization of large relay interlock and control systems.
Publisher	Monterey, California: U.S. Naval Postgraduate School
Issue Date	1963
URL	http://hdl.handle.net/10945/11734

This document was downloaded on June 19, 2015 at 11:03:26

DUDLEY KNOX LIBRARY

http://www.nps.edu/library

Calhoun is a project of the Dudley Knox Library at NPS, furthering the precepts and goals of open government and government transparency. All information contained herein has been approved for release by the NPS Public Affairs Officer.

Dudley Knox Library / Naval Postgraduate School
411 Dyer Road / 1 University Circle
Monterey, California USA 93943

NPS PRAESTANTIA PER SCIENTIAM

http://www.nps.edu/

NPS ARCHIVE
1963
COOK, J.

BOOLEAN MINIMIZATION OF LARGE RELAY INTERLOCK AND CONTROL SYSTEMS

JOHN H. COOK

LIBRARY
U.S. NAVAL POSTGRADUATE SCHOOL
MONTEREY CALIFORNIA

52

BOOLEAN MINIMIZATION

of

LARGE RELAY INTERLOCK AND CONTROL SYSTEMS

* * * * *

John H. Cook III

BOOLEAN MINIMIZATION

of

LARGE RELAY INTERLOCK AND CONTROL SYSTEMS

by

John H. Cook III

Lieutenant, United States Navy

Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING

United States Naval Postgraduate School
Monterey, California

1963

LIBRARY
U.S. NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

BOOLEAN MINIMIZATION

of

LARGE RELAY INTERLOCK AND CONTROL SYSTEMS

by

John H. Cook III

This work is accepted as fulfilling the

thesis requirements for the degree of

MASTER OF SCIENCE

IN

ELECTRICAL ENGINEERING

from the

United States Naval Postgraduate School

ABSTRACT

The perfection of the transistor and the subsequent birth of a vast digital technology has focused special attention on the methods and mathematics of Boolean algebra. The result of this attention has been the development of powerful methods of synthesis and minimization of logic circuits. This area continues to be the subject of extensive research.

The purpose of this paper is to explore the applicability of Boolean minimization methods to the design of large relay interlock and control systems. The investigation of an existing and representative system from the Boolean standpoint was judged the best way to accomplish this purpose. Accordingly, the system selected was the Livermore variable-energy 90-inch cyclotron located at the Lawrence Radiation Laboratory, Livermore, California.

The conclusion is that for this class of system a working knowledge of elementary Boolean algebra and an engineer's normal intuition would be sufficient to achieve minimal design. As a bonus result, the symbolic notation known as "gate notation" was found to be a valuable aid in the representation and understanding of the interlock and control logic of the cyclotron.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. Introduction

This paper is the result of work done in the Electronics Engineering Department of the Lawrence Radiation Laboratory, Livermore, California during the intersessional period, 1962. The departmental staff was interested in finding out if the new Boolean techniques would be a significant aid to the problem of designing large interlock and control systems. They were particularly interested in finding out if the use of Boolean methods would result in a better design.

The purpose of this paper is to investigate the applicability of Boolean minimization techniques to the class of large interlock and control system characterized by that of the 90-inch cyclotron. The 90-inch cyclotron is a large machine with numerous electronic, electrical and mechanical components. It is used to accelerate heavy particles to energies in the 2 to 20 MEV range for use in nuclear research. The function of the interlock and control system is to eliminate personnel hazards and prevent material casualties by monitoring the operation of all components of the cyclotron, stopping or preventing operation of the machine should hazard or casualty exist or appear.

The investigation was conducted in two parts. The first was the reduction of the existing interlock and control system to its logical essentials. The second was the examination of the logic flow chart (appendix I) with an eye to the applicability of minimization techniques.

The results of the investigation are:

a. The knowledge of elementary Boolean algebra and the use of a symbolic notation such as gate notation would be a substantial aid in the design of interlock and control systems.

b. Gate notation provides a compact and clear representation of the interaction of the various elements of the interlock and control system.

c. The more powerful Boolean minimization techniques are not needed to design a system of this class since the system is logically simple.

d. The use of Boolean algebra and techniques would not have resulted in a significantly better design.

2. Boolean Algebra and Gate Notation

The algebra of variables that can have only two states was developed primarily by George Boole and originally applied to the analysis of logic and the laws of thought.[1,2] Only recently has Boolean algebra been applied to relay circuits and other two state devices. Specifically, the first important contribution was made by Shannon in 1938[3] to the design of relay circuits used in telephone switching.

Boolean algebra is an algebra of sets. The familiar operations of union, intersection and complement are represented for switching analysis by the terms OR (+), AND (·), and NOT $\overline{(\ )}$. The variables in Boolean algebra may have only two states (1-0, on-off, true-false, etc.). No other state or indeterminate states are allowed. The operations are defined by means of a TRUTH TABLE.

variable		operations			
		A OR B	A AND B	NOT A	NOT B
A	B	A+B	A·B	$\overline{A}$	$\overline{B}$
0	0	0	0	1	1
1	0	1	0	0	1
0	1	1	0	1	0
1	1	1	1	0	0

****

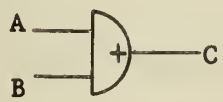
[1] George Boole, The Mathematical Analysis of Logic, Cambridge, England, 1847.

[2] George Boole, An Investigation of the Laws of Thought, London, England, 1854.

[3] C. E. Shannon, A Symbolic Analysis of Relay and Switching Circuits, Trans AIEE, Vol. 57, 1938, pp 713-723.

It is appropriate at this point to introduce the gate. The operations of ORing, ANDing and NOTing suggest a symbolic operator for use on circuit schematics. This operator is the gate. The three gates and their associated truth tables are shown below.

OR gate



A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

AND gate

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

NOT gate

A	$\overline{A}$
0	1
1	0

Gates are unidirectional devices, the inputs are the cause, the outputs the effect.

The following fundamental theorems of Boolean algebra will be illustrated where appropriate with gate notation.

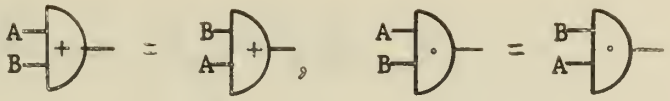
a. Properties of 1 and 0

$A + 1 = 1$
$A + 0 = A$
$A \cdot 1 = A$
$A \cdot 0 = 0$
$A + \overline{A} = 1$
$A \cdot \overline{A} = 0$

b. Commutative Laws

$A + B = B + A$

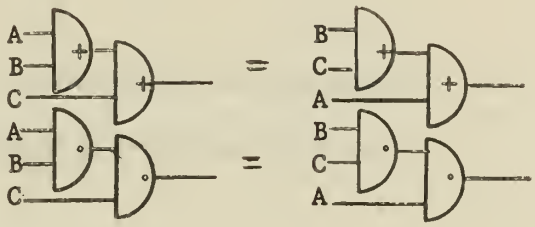
$A \cdot B = B \cdot A$



c. Associative Laws

$(A + B) + C = A + (B + C)$

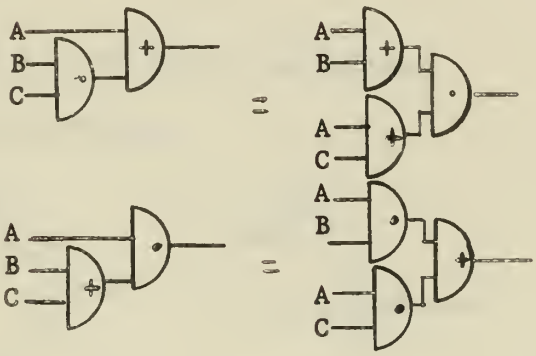
$(A \cdot B) \cdot C = A \cdot (B \cdot C)$



d. Distribution Laws

$A + (B \cdot C) = (A + B) \cdot (A + C)$

$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$



e. Idempotent Laws

$A + A = A$

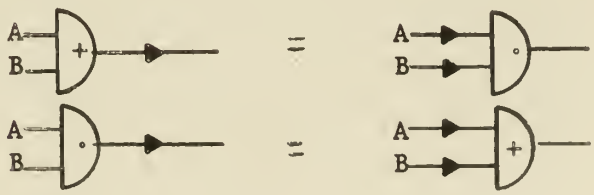
$A \cdot A = A$

These first five laws can easily be proved by inspection of the TRUTH TABLE. The truth of the following important theorem will be demonstrated. [1]

f. DeMorgan's Theorem

$\overline{(A + B)} = \overline{A} \cdot \overline{B}$

$\overline{(A \cdot B)} = \overline{A} + \overline{B}$



TRUTH TABLE

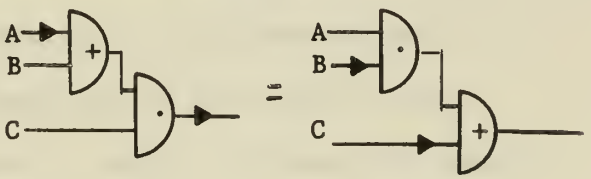
A	B	$\overline{A}$	$\overline{B}$	A + B	A · B	$\overline{(A + B)}$	$\overline{A} \cdot \overline{B}$	$\overline{(A \cdot B)}$	$\overline{A} + \overline{B}$
0	0	1	1	0	0	1	1	1	1
1	0	0	1	1	0	0	0	1	1
0	1	1	0	1	0	0	0	1	1
1	1	0	0	1	1	0	0	0	0

This theorem is not restricted to two variables or one operation under the NOT. Shannon suggested the following generalized form of DeMorgan's Theorem.

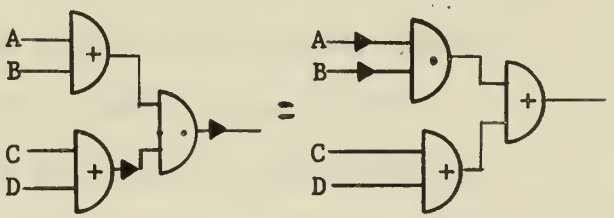
$$\overline{f(A,B,C,D,\cdots\cdots\cdots,\cdot,+)} = f(\overline{A},\overline{B},\overline{C},\overline{D},\cdots\cdots\cdots,+,\cdot)$$

That is, interchange the operations (+) and (·) and NOT all variables, care must be used to maintain groupings. For example:

$$\overline{((\overline{A} + B) \cdot C)} = (A \cdot \overline{B}) + \overline{C}$$



$$\overline{((A + B) \cdot \overline{(C + D)})} = \overline{A} \cdot \overline{B} + (C+D)$$



3. Gate Notation and Relay Circuits

Gate notation is a way of expressing the information to be found on wiring blue prints compactly in a flow chart form. It allows the designer to indicate clearly the relationship of the various control variables to the whole system. In reality, a relay is a gate. The form of the circuit that energizes the coil of the relay determines the type of gate. The relay contacts are the gate outputs.

The advantage of gate notation in design is that it can easily be converted to a wiring print. It allows the design to proceed to completion without the bother of having relay coils and contacts separated from each other. After completion of the design using gate notation, each gate will represent a relay, the number of inputs will represent the number of contacts in the input circuit, and the number of outputs the number of contacts needed on that relay. Figures 1, 2 and 3 illustrate typical gates and the equivalent circuit as it would be represented on a wiring print. Figure 4 illustrates the gate representation of the most common circuit in the 90-inch cyclotron interlock and control logic, the ON-OFF pushbutton circuit.

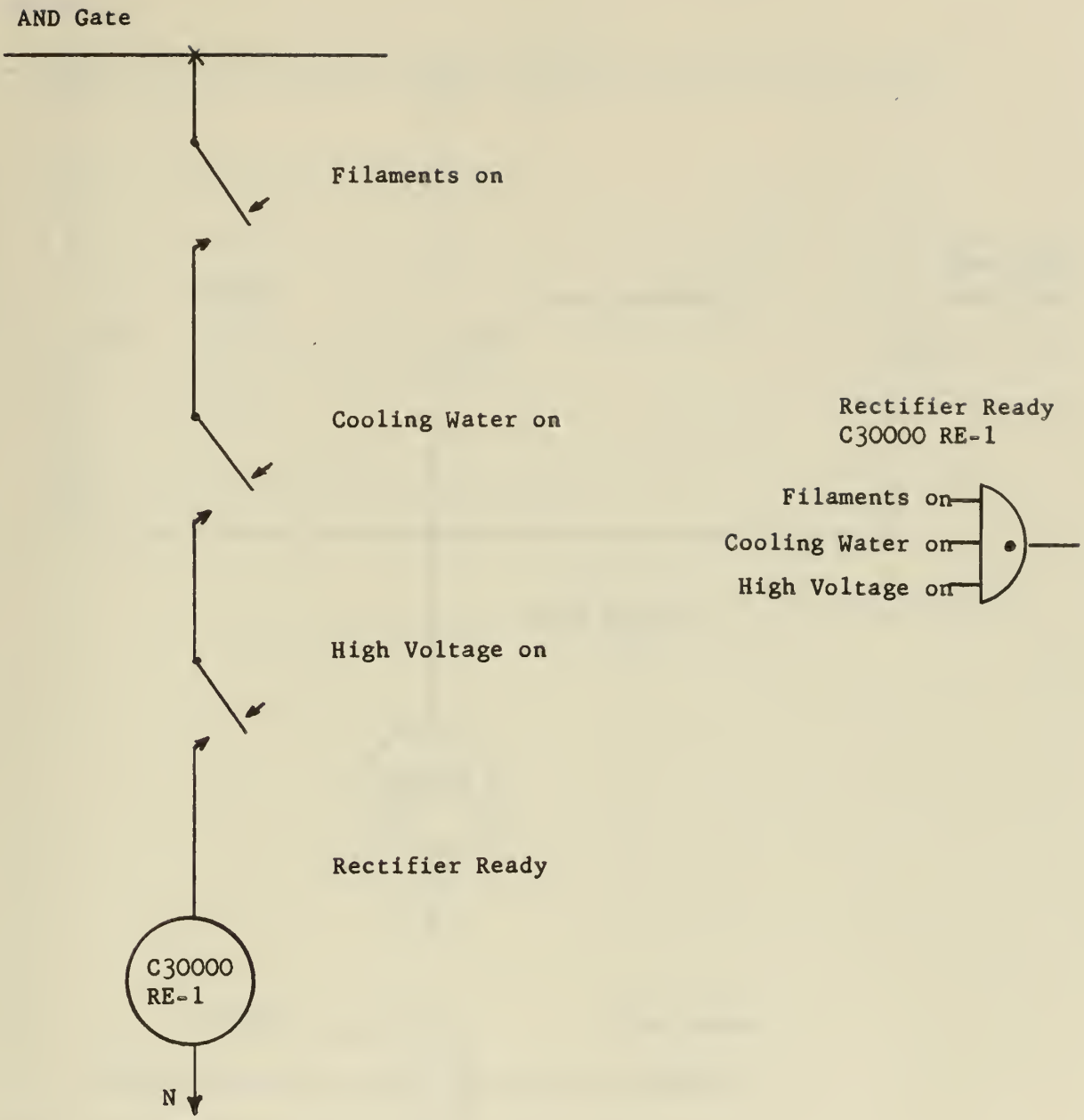


Figure 1. Relay AND Gate

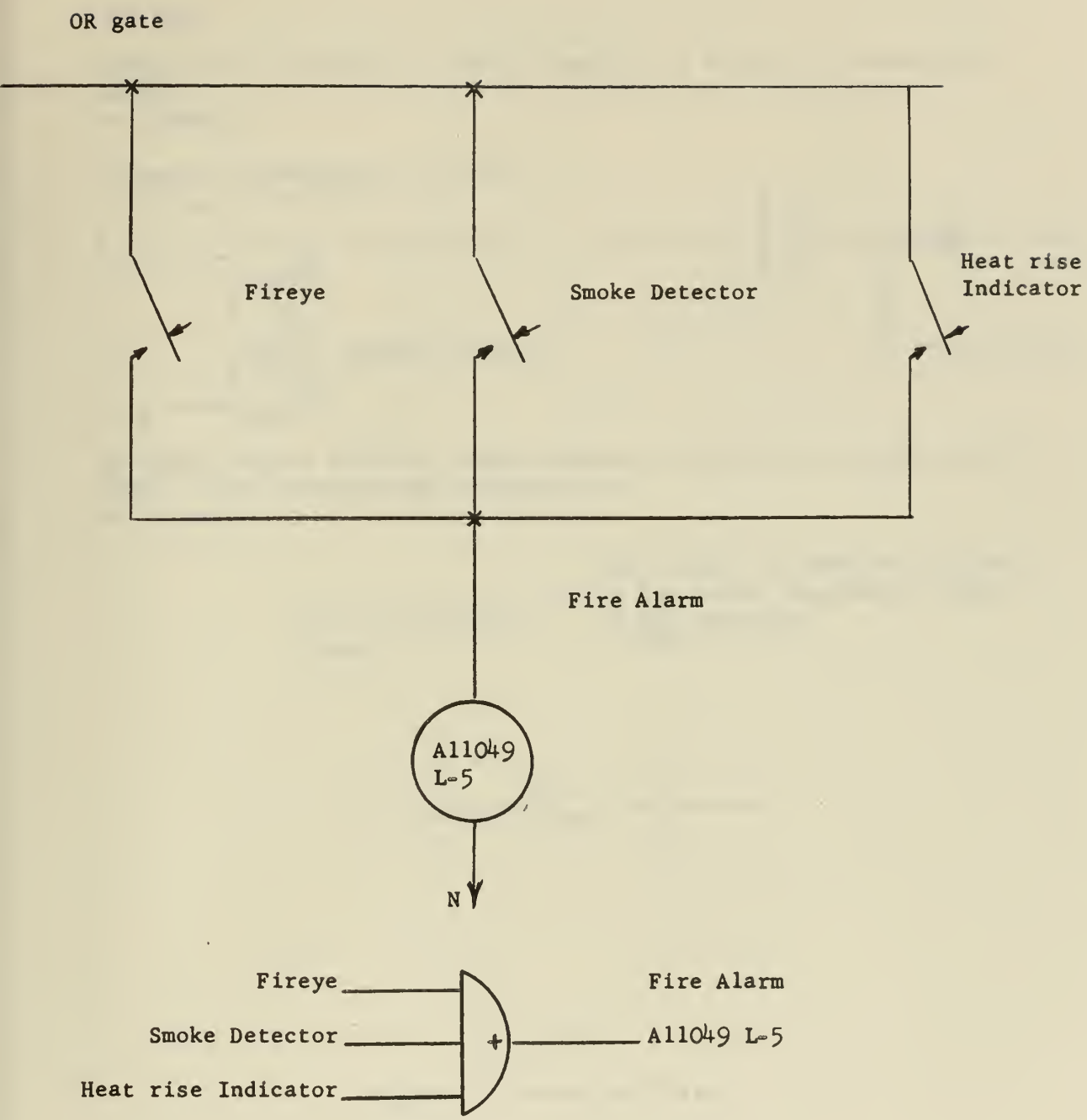
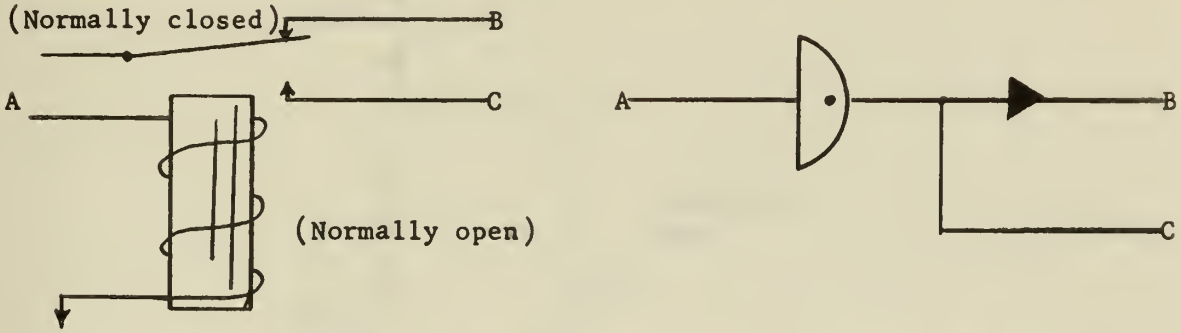


Figure 2. Relay OR Gate

NOT Gate

A NOT gate is actually an output function of a relay or mechanical switch.
For example:



In other words a normally closed contact or switch on a print is the "NOT" of the function that energizes it.
For example:

water temperature limit

The circuit is complete as long as the water temperature limit is not exceeded.

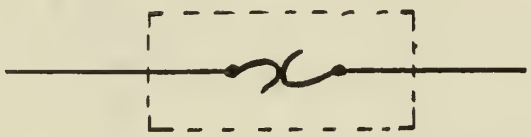


Figure 3. Relay NOT Gate

A commonly encountered circuit in a control system is the pushbutton ON - OFF circuit that has a relay "seal".

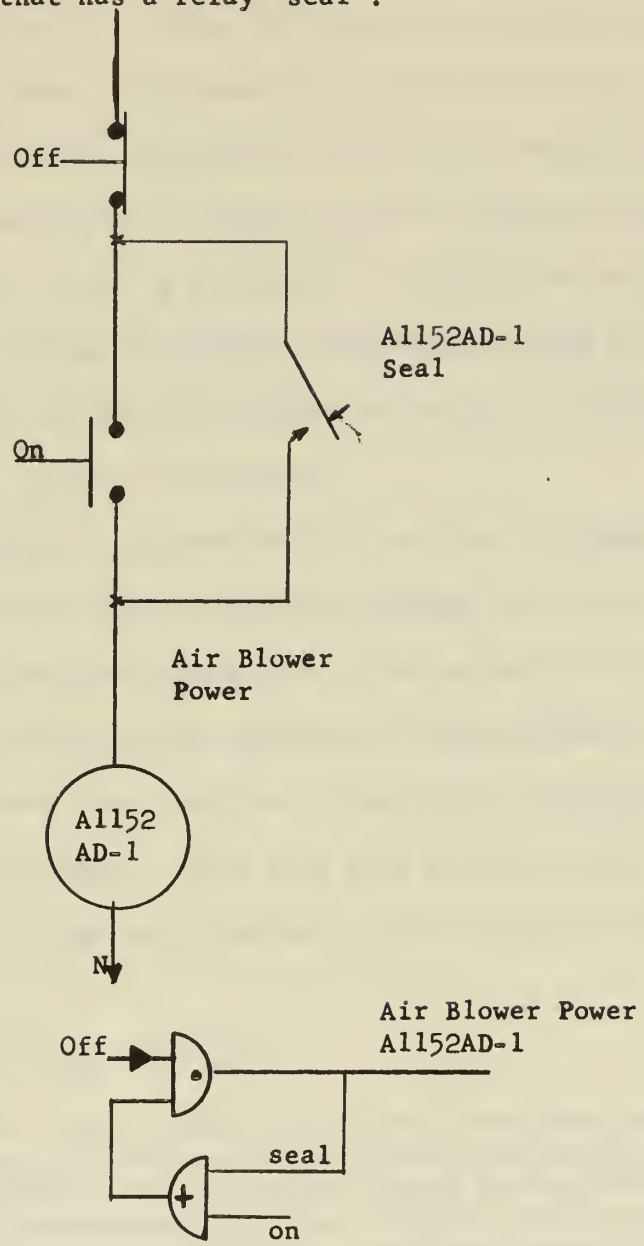


Figure 4. Relay ON - OFF - SEAL Circuit

4. Minimization of Relay Circuits

The minimization of a relay circuit can be defined as the elimination of superfluous operations from a switching circuit. A minimal switching circuit can be defined as that circuit which achieves the desired output from the given inputs with the smallest number of Boolean operations. This is equivalent to saying the smallest number of relays. A minimal switching circuit may or may not be unique, generally it isn't, giving the designer an option of choice in the final form of the circuit realization.

It is reasonable to assume that by the time the design of an interlock and control system becomes a problem, the major electronic, electrical and mechanical components of the system will have been decided upon. In addition, the operational requirements of the system as a whole will have been detailed, since this is inherent in the specification of a system. With this as a starting point, the design and minimization of the interlock and control system follows a definite procedure.

a. List the input variables.

b. List the output conditions desired from given combinations of input variables. It will be at this point that natural groupings of the input variables into subsystems should be exploited. It is easier to design several small systems with few input variables than one large system with many variables, since the number of operations needed to achieve minimal design with most Boolean techniques varies exponentially with the number of input variables.

c. Apply the minimization technique appropriate to the problem. Hopefully this will be by inspection. If the input-output conditions are too complicated, one of the synthesis techniques must be used. For non-sequential circuits the Quine-McClusky method is recommended.[2,3] Moore[4,5,6] are appropriate.

d. Translate the algebraic equations of the minimal circuit into gate notation.

e. Draw the wiring prints.

An example of the Quine-McClusky technique is given in Appendix II. The methods of sequential synthesis are complicated at best and cannot be treated compactly in this paper without suffering in the condensation . Mealy's article [5] is the most readable on this subject. Caldwell[1] has interpreted Huffman's work[4], but is difficult to follow.

5. Analysis of the Interlock and Control Logic

The logic flow chart of the 90-inch cyclotron interlock and control system should be folded out for inspection and reference while reading this section. The flow chart was prepared from the cyclotron wiring blue prints. Many of the notations on the chart are not vital to the analysis of the logic. They were made as a cross-referencing aid for the cyclotron engineers and technicians and are an example of the type of information that can be displayed on a logic flow chart.

Background. Prior to the analysis of the cyclotron logic, a brief description of the inner workings of the cyclotron is necessary. The 90-inch cyclotron was built as a facility for neutron research.[7] It produces a steady, mono-energetic beam of heavy particles (protons, deuterons, alpha particles) which strike targets of deuterium or tritium and produce mono-energetic neutrons. The cyclotrons accelerates these heavy particles with a high intensity electric field alternating at high frequency ($\sim$5MC). The particles are constrained to move in a circular path of increasing radius by a magnetic field perpendicular to their velocity vector. At an orbital radius of about 35 inches the particles are electrostatically deflected out of the cyclotron magnetic field into a beam tube and focused magnetically on the target. The cyclotron can be broken down into eleven functional subsystems.

a. An ION SOURCE to produce the heavy particles by ionization of a neutral gas.

b. A R. F. FINAL AMPLIFIER to provide the high power, radio frequency, accelerating field.

c. A R. F. TANK to act as the resonant load of the Final Amplifier, shape the electromagnetic accelerating field and act as the cyclotron vacuum chamber.

d. A HIGH VOLTAGE RECTIFIER to provide the controlled DC voltage to the Final Amplifier plate at a power level of 500KW.

e. A HIGH LEVEL DC SERIES REGULATOR to provide fine control of the Final Amplifier plate voltage.

f. An IGNITION CONTACTOR to act as a high speed switch between the High Voltage Rectifier and the 2500v, 3 phase supply.

g. A DRIVER AMPLIFIER to drive the Final Amplifier grid.

h. An EXCITER AMPLIFIER to drive the Driver Amplifier at a precise frequency.

i. A MAGNET to form the strong magnetic field. The 90-inch is the title of the cyclotron refers to the magnet pole face diameter. The Magnet weighs 300 tons.

j. A DEFLECTOR to electrostatically deflect the accelerated particles out of the cyclotron.

k. A VACUUM SYSTEM to maintain the high vacuum required in the RF Tank and beam pipe.

System Analysis. The interlock and control system of the 90-inch cyclotron has the following characteristics:

a. The system has a large number of independent inputs (176). The majority of these inputs are door interlocks, cooling flow switches and ON-OFF pushbuttons.

b. The system has eleven time delay elements and operates sequentially.

c. The system has a single output, a signal which turns on the Ignitron Contactor. (Ignitron Contactor Permissive and Phase Control Signal, location A-2 on the flow chart).

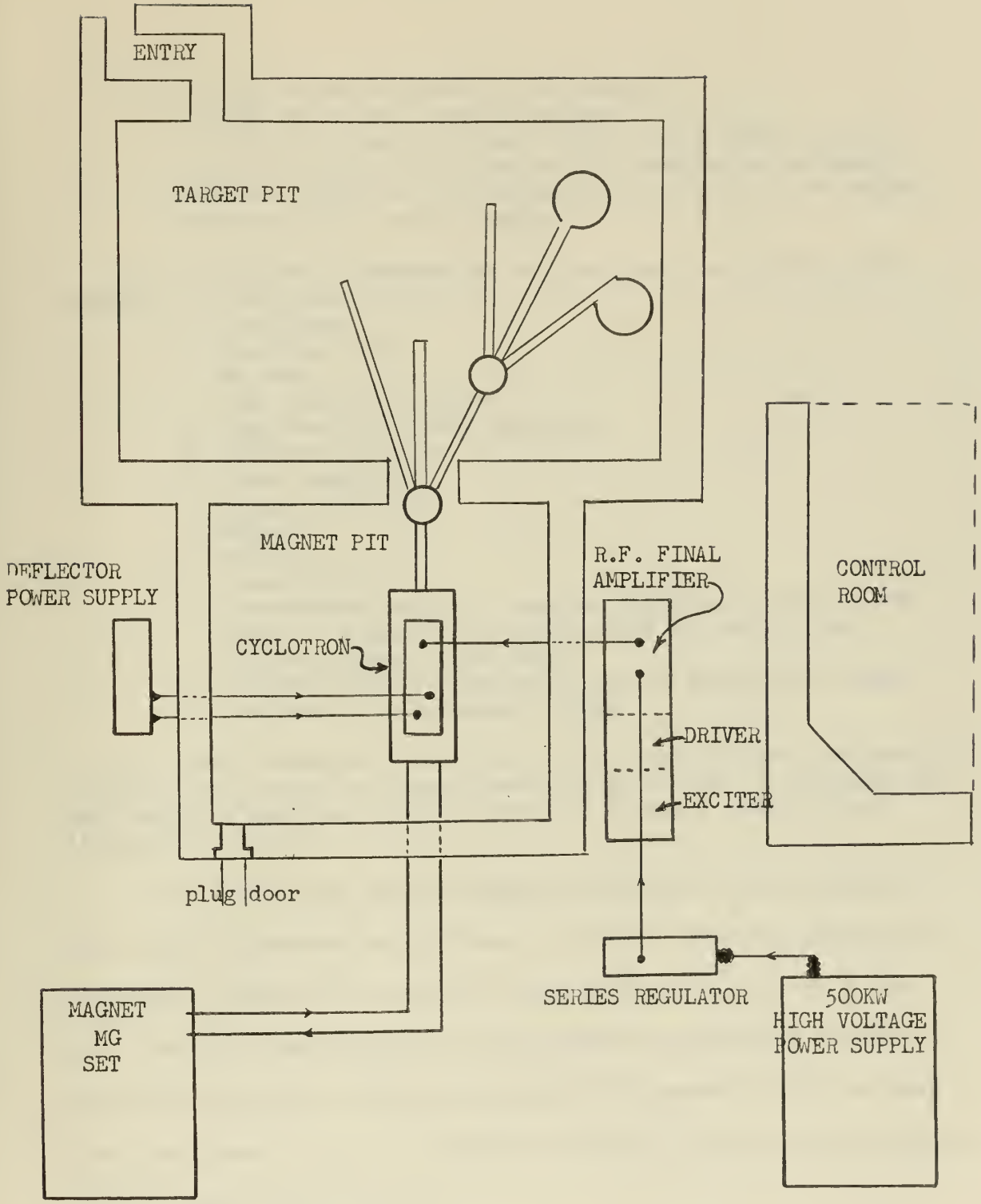


Figure 5. 90-inch CYCLOTRON, PLAN VIEW

d. The system has two modes of operation:
   1. RUN, the normal operational mode.
   2. TEST, to allow full power tuning of the Final Amplifier and RF Tank without the danger of a beam being accidently produced. This is to allow personnel to work in the magnet and target pits during tuning.

e. The system is composed of thirteen logic subsystems which parallel the functional subsystems.
   1. Ion Source
   2. Final Amplifier
   3. RF Tank
   4. High Voltage Rectifier
   5. High Level DC Series Regulator
   6. Ignitron Contactor
   7. Driver Amplifier
   8. Exciter Amplifier
   9. Magnet
   10. Deflector
   11. Vacuum Monitor
   12. A Radiation Monitor to monitor radiation levels in the target and magnet pits during TEST and warn of any Tritium leakage at any time.
   13. A Safety Chain to prevent cyclotron operation if radiation hazard to personnel exists.

f. Each subsystem is relatively independent of the other subsystems. The system as a whole functions as a chain of AND gates on two levels, a readiness level (Figures 6, 7) and a control level (Figures 8,9,10,11).

It is easy to see why the logical simplicity of the interlock and control system was not previously evident. The large number of independent inputs, the numerous wiring prints, the lack of a compact form of representing the system action and the large physical size of the cyclotron and its components all tended to hide the fact that the system is just a cascade of AND gates (relay chains) fanning in to a single ON-OFF control.

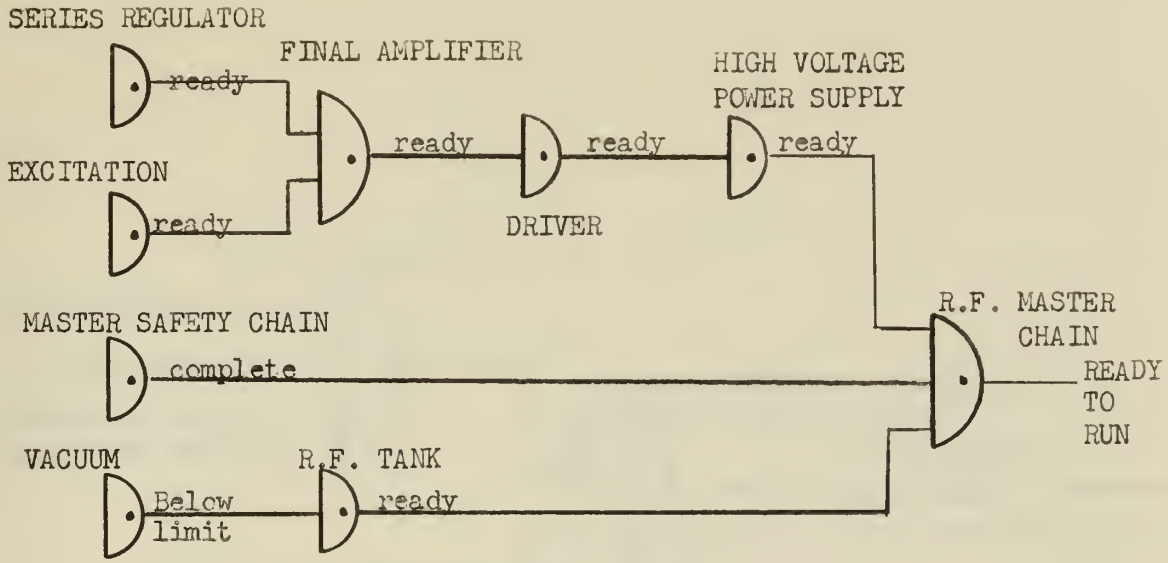


Figure 6. RF MASTER CHAIN, RUN MODE

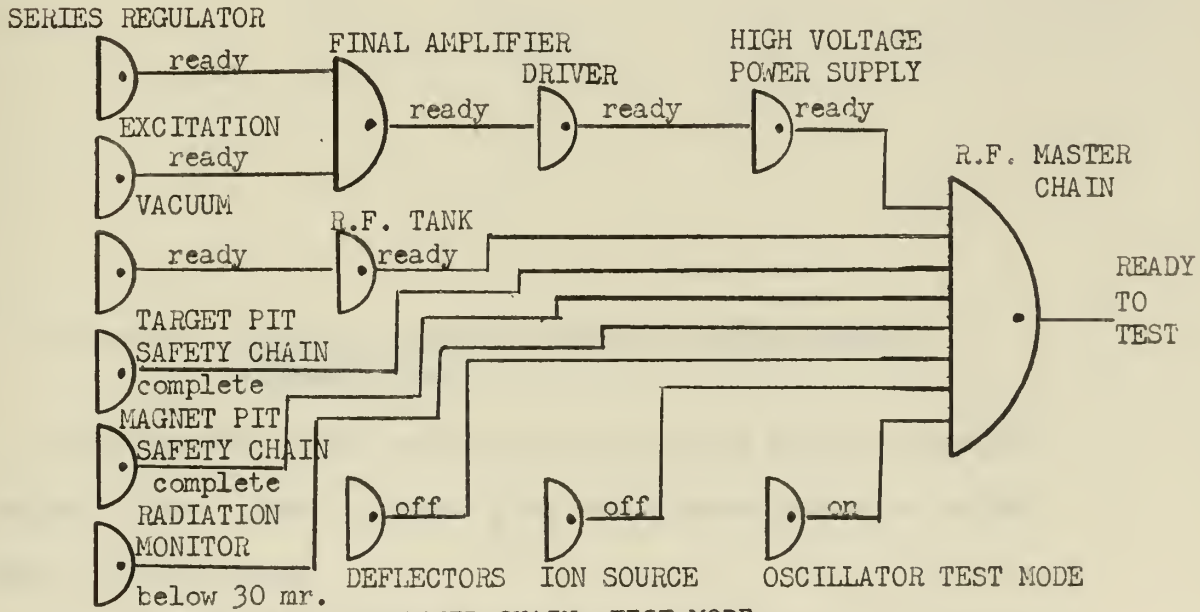


Figure 7. RF MASTER CHAIN, TEST MODE

Only the interaction of the major subsystems are shown on these simplified flow charts. The many inputs that determine if a given subsystem is ready or not are shown explicity in Appendix I.

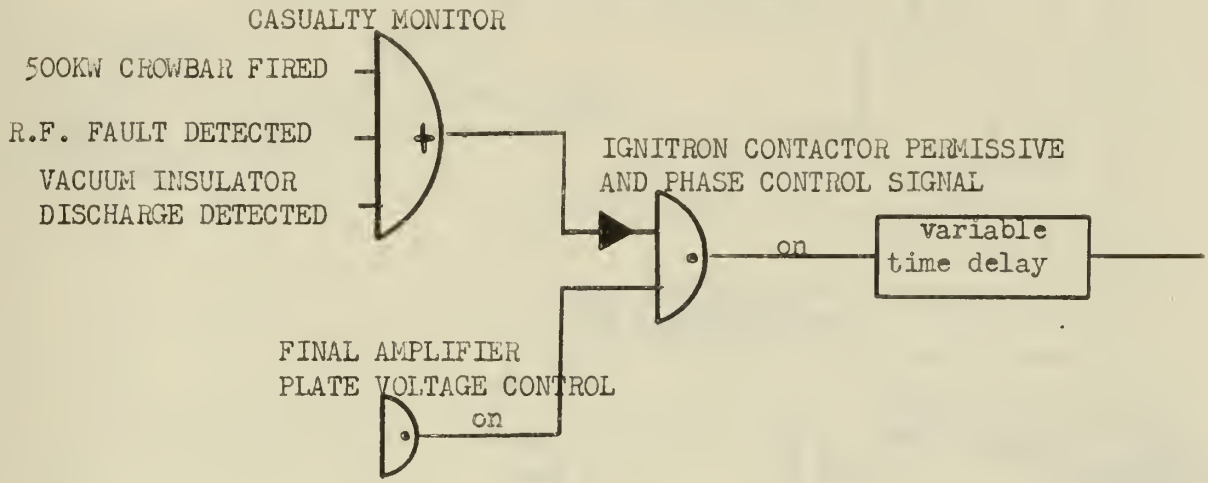


Figure 8. IGNITION CONTACTOR CONTROL OF HIGH VOLTAGE, AUTOMATIC MODE

The time delay shown and all the system time delays are of the "snapback" type. That is, they delay an ON signal but pass an OFF signal instantaneously.

In the Automatic Mode a casualty will shut the High Voltage Power Supply off by opening the Ignitron Contactor. When the casualty disappears the Ignitron Contactor will close automatically after a time delay.

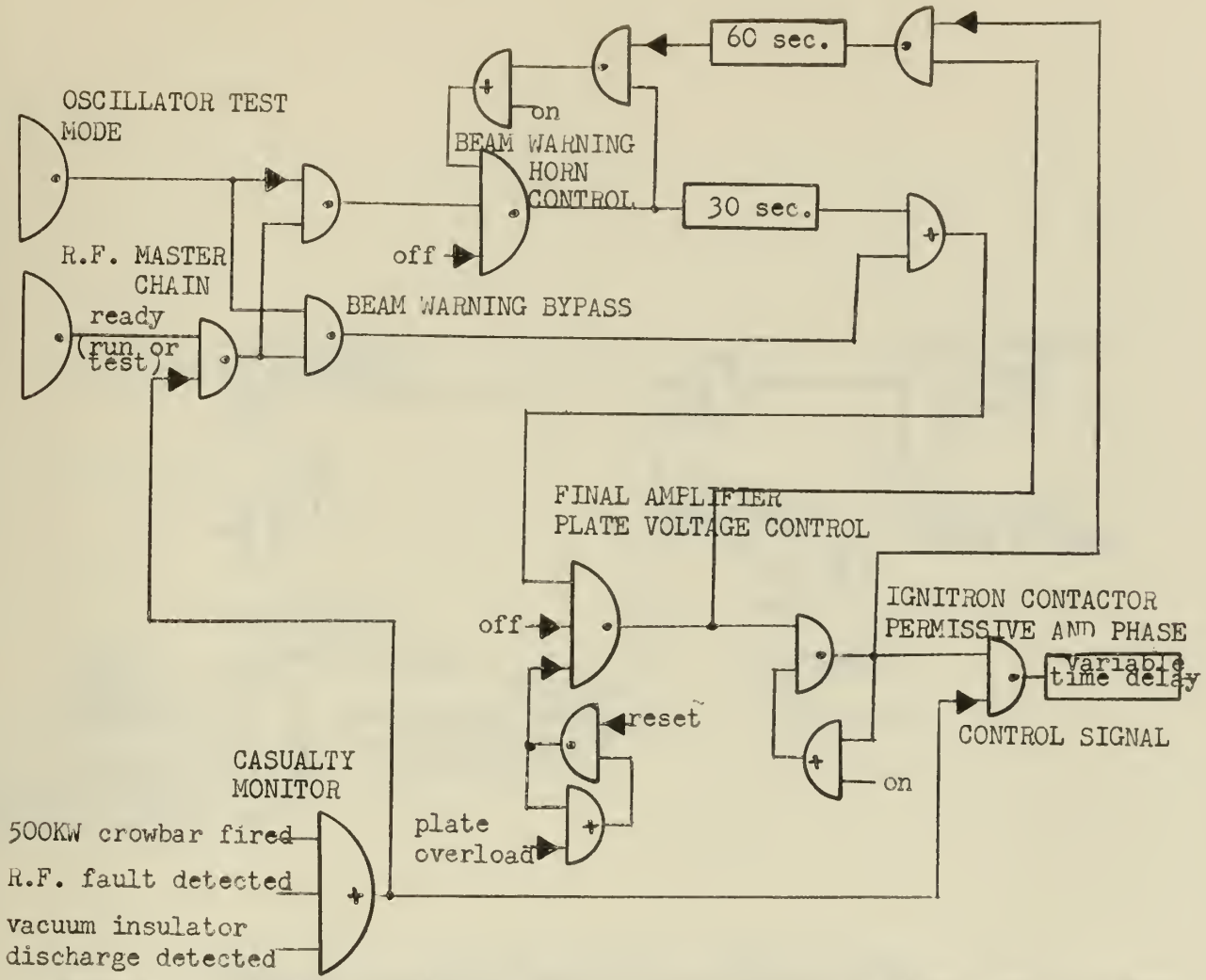


Figure 9. IGNITRON CONTACTOR CONTROL OF HIGH VOLTAGE, MANUAL RECYCLE MODE

In the Manual Recycle Mode a casualty will shut off the High Voltage Power Supply directly by opening the Ignitron Contactor. In addition, it will open the chain to the Final Amplifier plate voltage control. As this circuit is the most complicated in the interlock and control system it is worth examining in detail. The inputs are the casualty conditions, the RF Master Chain complete signal, the Oscillator Test Mode Signal and the ON-OFF relations indicated. In the RUN mode the operator presses the Beam Warning Horn Control ON button. The beam warning horn blows and after a time delay of thirty seconds the system is ready up to the Final Amplifier Plate Voltage Control. If the plate voltage is not turned on within sixty seconds the beam warning control will unseal and the whole routine must be repeated. Pressing the Final Amplifier Plate Voltage Control ON pushbutton completes the chain and closes the Ignitron Contactor through the Ignitron Contactor Permissive and Phase Control signal. In the TEST mode of operation the beam warning control is bypassed and the system is restored to operation after a casualty by pressing the Final Amplifier Plate Voltage Control ON pushbutton.

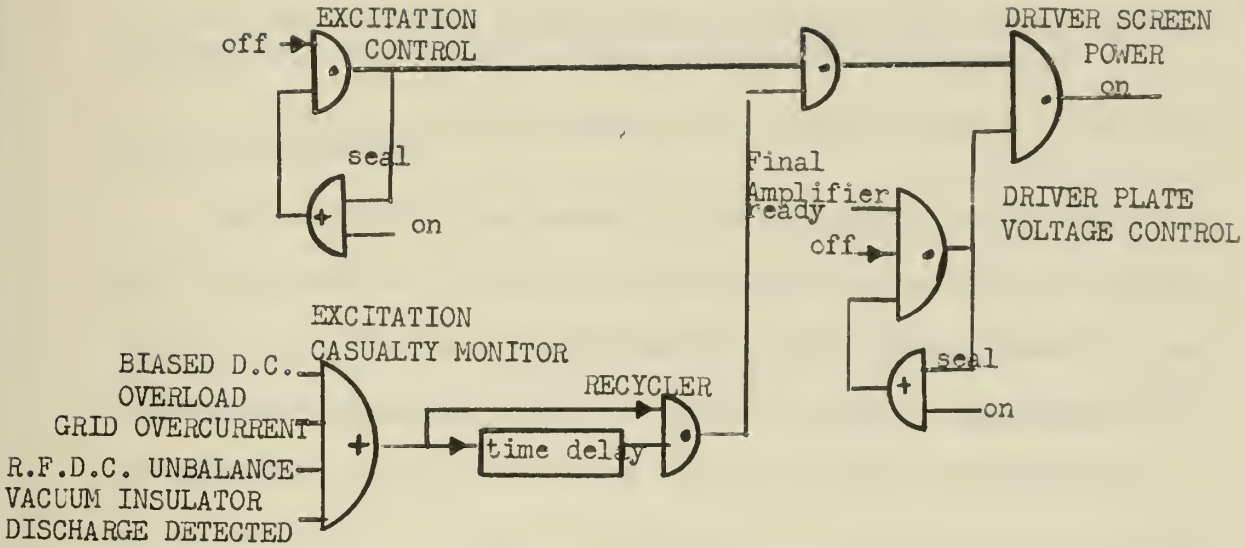


Figure 10. EXCITATION CONTROL, AUTOMATIC MODE

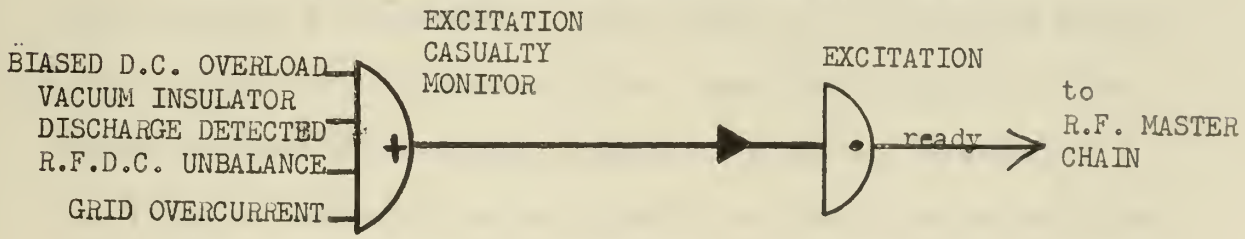


Figure 11. EXCITATION CONTROL, MANUAL MODE

In the AUTOMATIC mode the excitation recycles automatically after a casualty disappears. In the MANUAL mode a casualty interrupts the RF MASTER CHAIN (Figures 6 and 7) at the Exciter Ready interlock and the whole system shuts down and must be restarted.

6. Conclusions

The interlock and control system of the 90-inch cyclotron is logically simple. This simplicity is the result of three major factors:

a. The system is composed of semi-independent subsystems.

b. The operating characteristics dictate that the system be brought into operation in a rigid sequential order.

c. There is only one output, the signal to open or close the Ignitron Contactor.

The minimization techniques of Boolean algebra would not be useful in the design of interlock and control systems similar to that of the 90-inch cyclotron. The system breaks down into a number of semi independent subsystems which are logically simple. Application of minimization techniques to these subsystems would be superfluous since they can be designed and minimized by inspection from the operating requirements.

The use of Boolean techniques, elementary or advanced, would not have achieved a significantly better design of the interlock and control system of the 90-inch cyclotron. Analysis of the logic flow chart revealed few needlessly redundant operations. However, a knowledge of elementary Boolean algebra and gate notation would provide the engineer with a valuable design and analysis tool. The use of this tool would result in a logic flow chart of the system from which wiring prints could be easily prepared. In addition, the logic flow chart would be an aid for the training of operation and maintenance personnel after completion of the system.

BIBLIOGRAPHY

1. S. H. Caldwell, "Switching Circuits and Logical Design", John Wiley & Sons, Inc. 1958.

2. M. Phister, Jr., "Logical Design of Digital Computers", John Wiley & Sons, Inc. 1957.

3. R. S. Ledley, "Digital Computer and Control Engineering", McGraw Hill Book Co., 1960.

4. D. A. Huffman, "The Synthesis of Sequential Switching Circuits", J. Franklin Institute, pp 161-190, 275-303, March-April, 1954.

5. G. H. Mealy, "A Method for Synthesizing Sequential Circuits", B. S. T. S., pp 1045-1080, September, 1955.

6. E. F. Moore, "Gendanken Experiments on Sequential Machines", Automata Studies, Princeton University Press, 1956.

7. UCRL - 5971, "The Livermore Variable Energy 90-inch Cyclotron", 1960.

APPENDIX I

LOGICAL FLOW CHART OF THE 90-INCH CYCLOTRON

INDEX OF LOCATION

R. F. FINAL AMPLIFIER	- B-2
DEFLECTORS	- C-2
EXCITER	- B-2, 3
IGNITRON CONTACTOR	- A-2
ION SOURCE	- C-2
MAGNET	- D-2
500 KW POWER SUPPLY	- A-2, 3
RADIATION MONITOR	- B-3
SAFETY CHAIN	- C, D-1
SERIES REGULATOR	- B-2
VACUUM MONITOR	- D-3

LE9467-1

60 CYCLOTRON - LOGICAL FLOW CHART

1/2 2/3 3/4 4/5 5/6

BST B RECTIFIER FILAMENTS A11432 T 3-1, A11534 AD-2 & A10615 A1-1 LE1514-1 [E-3]

OFF SEAL ON RECTIFIER COOLING AIR FLOW SW6030

HIGH VOLTAGE READY A11022 L-2 & A11046 L-7 LE1519-1 [E-4]

A11019 L-1 LE1519-1 [D-2]

2400V POWER TO IGNITRON CONTACTOR C30090 RE-1 LE1514-1 [A-2]

IGNITRON COOLING WATER FLOW
COOLING WATER TEMP. LIMIT
IGNITRON CONTACTOR DOORS INTERLOCK
IGNITRON CONTACTOR KEYS INTERLOCK
500 KW RECTIFIER DOORS INTERLOCK
500 KW RECTIFIER KEYS INTERLOCK
500 KW CROWBAR DOORS INTERLOCK
500 KW CROWBAR KEYS INTERLOCK
2400V TRANSFORMER DOOR INTERLOCK
2400V DISCONNECT SWITCH ON
TUNE UP SWITCH OPEN
SERIES REGULATOR HIGH VOLTAGE
LINE SWITCH BOX COVER ON

SCREEN CURRENT TO V-1
PLATE CURRENT TO ½ V-2
PLATE CURRENT TO ½ V-2
PLATE CURRENT TO ½ V-3
FILAMENT ON V-4
PLATE VOLTAGE ON V-4

FAULT DETECTOR & CROWBAR FIRING CHASSIS C30085 RE-2 & RE-7 LE2581-1

A2332 PLATE VOLTAGE CONTROL

HIGH VOLTAGE ON A11015 L-2, A11015 L-4, A11019 L-5, LE2514-1 [E-3]

IGNITRON CONTACTOR FAILURE A11028 L-2 LE1519-1 [B-3]

TO BST B RECTIFIERS C30090 RE-2 LE1514-1 [B-1]

BEAM WARNING HORN CONTROL A11121 L-4 & A10434 TD-1 LE1514-1 [J-2]

A10434 TD-2 LE1514-1 [J-4]

60SEC.T.D. 365SEC.T.D.

BEAM WARNING BYPASS

OSCILLATOR TEST SIGNAL FROM 2MA CHAIN

D.E. CHAIN COMPLETE

BST B FILAMENTS WARMED UP

BST B FILAMENTS ON

C30824, +300V POWER ON

MANUAL

C30334 RE-1 LE1830-1

500 KW CROWBAR FIRED
R.F. FAULT DETECTED

IGNITRON CONT. PERMISSIVE & PHASE CONTROL SIGNAL

VAR. T.D.

C30334 RE-2 & ELECTRONICS CIRCUITS LE 1830-1

A2332 PLATE D.C. OVERLOAD A11037 L-6 LE1514-1 [H-3]

BIASED RELAY C30090 RE-2 LE1514-1 [F-1]

RESET

HIGH VOLTAGE ON
DISCHARGE DETECTED

VACUUM INSULATOR DISCHARGE DETECTOR C5421 RE-1 LE4260

NOTE 1

A2332 AIR & WATER INTERLOCKS

ANODE WATER ON
WATER TEMP. LIMIT
BEAM CYLINDER COOLING WATER
GRID RING WATER
SEAL AIR FLOW

A11025 L-6 LE1909-1 [F-2]

A2332 BIAS POWER INTERLOCK

R.F. TRANSMISSION LINE AIR FLOW
TRANSMISSION LINE COVER ON
AIR TUBE IN PLACE
R.F. EXCITER DOORS CLOSED
A2332 AMPL. DOORS CLOSED
CHOKE BOX DOORS CLOSED
R.F. TROMBONE IN PLACE

A11149 L-1 LE1909-1 [H-2]

INDUCTION REGULATOR AT MINIMUM

UNDER-200V BIAS INTERLOCK

BIAS LIMIT C2641 RE-1 LE8114-1 [C-3]

A2332 FILAMENT CONTROL

A10611 A1-2 A11025 L-3 A11027 L-3

A2332 FINAL AMP. TUBE READY

A11036 L-5 LE1909-1 [F-4]

2V SHUNT T.D. C30060 RE-2 LE1909-1 [C-2]

A2332 PLATE VOLTAGE ON

A2332 PLATE H.V. CONTROL

UPPER LIMIT INCREASE H.V. C60001 RE-2

LOWER LIMIT DECREASE H.V. C60001 RE-1

A2332 FILAMENT AUTOMATIC RUN-UP RUN-DOWN CIRCUIT C30061 RE-1

RAISE INDUCTION REGULATOR

LOWER INDUCTION REGULATOR C30061 RE-2

UPPER LIMIT

LE1909-1 [C-4]

SERIES REGULATOR BYPASSED
A5822 ANODE WATER FLOW
A5821 GRID RING WATER FLOW
A5821 BEAM CYLINDER WATER FLOW
SERIES REGULATOR DOOR INTERLOCK

A5822 BIAS H.V. INTERLOCK A11731 AD-2 LE6932-1

INDUCTION REGULATOR AT LOWER LIMIT

OFF UPPER LIMIT LOWER LIMIT TO RUN AUTO RUN DOWN

1 M.T.D.

A11031 SERIES REGULATOR READY

A11119 L-2 LE6932-1

FUSE F-1

A5821 FIL. 0A 0A

FUSE F-2

A11119 L-5 LE6932-1

LOCAL ON SW. LOW LEVEL CHASSIS READY

FUSE F-1 OK

A11119 L-1 LE6932-1

NOTE 2

R.F. EXCITATION READY A11025 L-5 LE1914-1 [C-2]

EXCITATION CONTROL A11016 L-1 A11016 L-5 LE1914-1 [C-1]

A2332 PLATE BIASED D.C. OVERLOAD; C30080 RE-2 LE1514-1 [L-2]

VACUUM INSULATOR DISCHARGE

EXCITATION RECYCLE MODE - AUTO

A11016 L-3 LE1914-1 [M-2]

A2332 GRID OVERCURRENT; C2611 PJC LE1509-1 [E-3]

A6615 RE-4

R.F. D.C. UNBALANCE

1SEC.T.D.

A6615 RE-1 LE6955-1

R.E.D.C. INTERLOCK A6615 RE-3 LE6955-1

EXCITATION TIME DELAY RECYCLER

VAR. T.D.

2400V POWER ON C30090 RE-2 LE1514-1 [G-2]

A11019 L-7 LE1519-1 [B-3]

D.C. SERVO DISCONNECT A11146 L-5 LE1914-1 [F-3]

NOTE 3

500 KW D.C. ON

R.E.D.C. INTERLOCK D.C. DISABLING RELAY A6615 RE-1 LE6955-1

A2332 FINAL AMPLIFIER READY

6166 FILAMENT CONTROL A11426 T 2-3, A10731 AT-1 LE1920-1 [B-1]

6166 AIR INT'K. COOLING AIR DOOR INT'K.

6166 BIAS POWER A11010 RE-1 LE7532-1

480V POWER TO DRIVER A11130 L-1 LE1920-1 [D-1]

6166 H.V. POWER SUPPLY FILAMENT CONTROL C30075 RE-2; A10715 AT-1 LE1920-1 [F-2]

A11026 L-6 [G-3]

6166 D.C. OVERLOAD LE1920-1

6166 SCREEN CURRENT O.L.; A10411 H-1 [C-3]
6166 PLATE CURRENT O.L.; C30075 RE-3 [D-4]
6166 A.C. A ϕ OVERLOAD; C30075 RE-3 [C-3]
6166 A.C. B ϕ OVERLOAD; C30075 RE-4 [C-3]

2ϕ EXCITER PLATE POWER CONTROL A11534 AD-3 LE1914-1 [E-2]

R.F. EXCITER PLATE POWER ON A11121 RE-1 LE1514-1 [C-2] & SW6052

6166 SCREEN POWER ON

6166 DRIVER AMPLIFIER PLATE VOLTAGE CONTROL C30075 RE-1 A11426 T 2-1 LE1920-1 [E-3]

R.F. EXCITER D.C. OVERLOAD A11016 L-6 LE1914-1 [D-3]

4-250A PLATE & SCREEN OVERLOAD A10411 H-1; LE1914-1 [C-2]

R.F. EXCITER FILAMENT CONTROL A11432 T 2-3 LE1914-1 [B-1]

2400V A.C. OVERLOAD A11037 L-5 LE1514-1 [J-1]

A11125 L-1 A ϕ A BANK RESET SEAL TRIP A10720 AT 3-1

A11125 L-2 C ϕ A BANK RESET SEAL TRIP A10720 AT 3-2

A11125 L-3 A ϕ B BANK RESET SEAL TRIP A10720 AT 3-1

A11125 L-4 C ϕ B BANK RESET SEAL TRIP A10720 AT 3-2

2400V A.C. OVERLOAD CIRCUITS LE1514-1 [J-1] & [D-2]

MASTER SAFETY CHAIN

TARGET PIT SAFETY CHAIN

MAGNET PIT SAFETY CHAIN

MASTER SAFETY CHAIN (REDUNDANT CIRCUIT) A11022 L-7 & A11022 L-6 LE1916-1 [F-4]

NORTH TRENCH GATE CLOSED
SOUTH TRENCH GATE CLOSED
MAGNET PIT DOOR CLOSED
TARGET PIT DOOR CLOSED
SCINTILLATION CAVE DOOR
MAGNET PIT DOOR KEY
TARGET PIT DOOR KEY
YELLOW WARNING LIGHT: DEFLECTOR, N. TRENCH, WATER WINDOW, S. TRENCH

MAGNET PIT SAFETY CHAIN A11040 L-1 & A11040 L-2 LE1916-1 [E-1]

LOWER DECK S.W.
LOWER DECK S.E.
LOWER DECK N.W.
LOWER DECK N.E.
CENTER DECK
MAIN DECK S.
MAIN DECK N.
PIT DOOR LIGHT
YELLOW WARNING LIGHT

TARGET PIT SAFETY CHAIN A11040 L-2 & A11040 L-3 LE1916-1 [E-2]

LOWER DECK S.
LOWER DECK N.
MAIN DECK W.
MAIN DECK S.
MAIN DECK E.
MAIN DECK N.
PIT STAIR TOP
PIT DOOR LIGHT

TARGET PIT WATER FLOW SWITCHES DEPENDENT ON EXPERIMENTS IN PROGRESS

MAGNET PIT WATER FLOW TO: 2 JAW COLLIMATOR, BEAM SWEEPER, RANGER, 9 JAW COLLIMATOR, BENDING MAG. #1, STEERING MAG., STRONG FOCUS MAG.

RE-1 / RE-8 LE1917-10

DEFLECTOR WATER & SEPTUM WATER FLOW

DEFLECTOR P.S. FILAMENTS A10611 A1-1 LE1196-1 [D-2]

FILAMENT POWERSTAT AUTO RUN-UP - RUN DOWN CIRCUIT

RUNNING UP

POWERSTAT AT LOWER LIMIT

OFF ON LOWER RAISE UPPER LIMIT

DOWN T.D.

A.C. OVERLOAD A11010 L-3 LE1196-1 [E-2]

RESET

INSTANTANEOUS O.L.
ENTRANCE DEFLECTOR TIME O.L.
INSTANTANEOUS O.L.
EXIT DEFLECTOR TIME O.L.
SEAL

C4123 RE-1 [D-3] C4122 A1-1 [E-3] LE1196-1

DEFLECTOR H.V. A11028 A1-2 A11028 L-5 A11028 L-7 LE1196-1 [H-2]

EAST H.V. POWER SUPPLY DOOR INTL'K.
WEST H.V. POWER SUPPLY DOOR INTL'K.
DEFLECTOR HOUSE DOOR INTL'K.

ARC SUPPLY PLATE VOLTAGE A11013 L-7 LE1910-1 [G-3]

DEFLECTOR H.V. KEY

FILAMENT P.S. AIR FLOW
ION SOURCE WATER FLOW
FIL. P.S. DOOR INTL'K.
ARC P.S. DOOR INTL'K.
ION SOURCE KEY

ION SOURCE KEY A11013 L-2 LE1910-1 [H-1]

ENTRANCE DEFLECTOR H.V. CONTROL C4123 RE-1, A11046 L-3 LE1196-1 [E-2]

ENTRANCE DEFLECTOR D.C. OVERLOAD C4123 RE-2 LE1199-1

EXIT DEFLECTOR D.C. OVERLOAD C4122 RE-2 LE1199-1

EXIT DEFLECTOR H.V. CONTROL C4122 RE-1; A11046 L-3 LE1196-1 [E-2]

ZEUS I A11046 L-2 LE1913-1 [C-2]

ZEUS II A11043 L-6 LE1917-1 [C-2]

ION SOURCE FILAMENT C30093 RE-1 LE1910-1 [E-1]

INDUCTION REG LOWER LIMIT

LOWER P.B.

FILAMENT AUTO RUN-DOWN

RAISE CALVE P.B.

ARC VOLTAGE CONTROL CIRCUIT

UPPER LIMIT RAISE P.B. INCREASE ARC VOLTAGE A11013 L-6 LE1910-1

LOWER P.B. LOWER LIMIT A11013 L-5 DECREASE ARC VOLTAGE

ARC SUPPLY FILAMENT A10711 A1-2 LE1910-2 [G-3]

30 MR RANGE

RADIATION INTERLOCK POWER A11043 L-7 LE1912-1 [D-1]

OSCILLATOR TEST A11121 L-6-1 A11124 T-1 & A11124 T-2 LE1912-1 [D-2]

TANK CHAIN WATER FLOW INTERLOCK LE1917-1 [D-10]

NORTH DEE LINE, T8-T1
TARGET PROBE
SOUTH DEE LINE, T15-T10
POLE FACE WINDING, Q-R
SOUTH DEE LINE, T9-T16
POLE FACE WINDING, D9-D20
SOUTH DEE LINE, T11-T14
SO. LOWER HEAD/NO. UPPER LINER, M-T
SOUTH DEE LINE, T13-T12
NO. LOWER HEAD/SO. UPPER LINER, N-M
SOUTH LOWER STEM, T22-T23
SOUTH LOWER LINER, L-A
SO. UPPER STEM/SO. SHORTING PLANE, T21-T24
NORTH LOWER LINER, J-B
NO. UPPER STEM/NO. SHORTING PLANE, T11-T20
TRIMMER CAPACITOR, G-G
NORTH LOWER STEM, T18-T19
R.S. LOOP, E-E
SHORTING MECHANISM, T27-T28
NORTH DEE LINE, T2-T7
TOP PROBE, T25-T26
NORTH DEE LINE, T4-T5
UPPER HEAD, T25-T26
NORTH DEE LINE, T6-T7

WATER FLOW SWITCHES

TANK CHAIN READY A11022 L-1 LE1917-1 [C-3]

LE1917-1 [F-3]

POWER ON FUSEBLOW VACUUM LIMIT

UNTRAPPED TANK VACUUM INTERLOCK A11010 L-3 LE1918-1 [E-2]

1 IN TRAPPED TANK VACUUM GAGE-BEAM PIPE VAC. INT'K. A11146 L-1 LE1915-1 [E-2]

POWER ON VACUUM LIMIT

TANK VACUUM HASTINGS DUAL VAC. T.C. INT'K. A6824 A11010 L-4; A11043 L-2 LE1950-1 [ ]

CLOSE OPEN LIMIT SEAL OPEN

GATE VALVE CONTROL A11149 L-7 LE1950-1 [B-3]

V12R BEAM PIPE GATE VALVE OPEN A11149 L-4 LE1950-1 [B-3]

MAGNET GROUND G121 RE-4 LE1279-1 [B-3]

RESET

GND DET. SHUNT VOLTAGE LIMIT

GENERATOR O.L. G121 RE-2 LE1279-1 [B-3]

2V SHUNT VOLTAGE LIMIT

BEARING TEMP. LIMIT

OVER/UNDER VOLTAGE G236 RE-2 LE1279-1 [C-1]

THERMAL LIMIT

MOTOR GENERATOR CONTROL G121 A1-1 LE1279-1 [D-3]

G11 RE-1 [D-1] G11 RE-2 [D-2]

COOLING OR TEMP. LIMIT
COOLING OIL FLOW
OIL-COOLING WATER FLOW
2V SHUNT COOLING WATER FLOW
H.D. ACTUATOR DOOR INTL'K.

240V 3 ϕ POWER ON G216 B 1

SHUNT FLD. REG. FIL. G11 A1-2 LE1279-1 [F-1]

FLD. ACTUATOR COOLING AIR FLOW

MAGNET CONTROL G115 A1-2 LE1279-1 [G-2]

SHUNT T.D.

OSCILLATOR TEST

- NOTES -

NOTE 1 THE IGNITRON CONTACTOR IS NOT DIRECTLY CONTROLLED BY THE RELAY CONTROL SYSTEM BUT BY THE SELECTRONIC CIRCUITRY OF THE RECYCLER AND IGNITRON CONTROL. IN THE AUTOMATIC MODE IT IS A FAULT IF OPERATED THE IGNITRON CONTACTOR IS PERMITTED ONLY AND AFTER A TIME DELAY AUTOMATICALLY TURNED ON. IN THE MANUAL MODE A FAULT SHUTS DOWN THE 480CV HIGH VOLTAGE CHARGE AND A RESTART AT THE BEAM WARNING HORN CONTROL MUST BE MADE.

NOTE 2 IN THE AUTOMATIC MODE THE EXCITATION RECYCLE AUTOMATICALLY RESETS AN EXCITATION OVER CURRENT FAULT. IN THE MANUAL MODE THE EXCITATION MUST BE RESTARTED AT THE EXCITATION CONTROLS OR BUTTON AFTER AN OVER CURRENT FAULT.

NOTE 3 THE D.C. SERVO DISCONNECT RELAY AND THE R.E.D.C. DISABLING RELAY ACTUALLY CONNECT THE SERVO SYSTEM AND ENABLE THE R.E.D.C. INTERLOCK WHEN ENERGIZED.

- LEGEND -

AND GATE

OR GATE

NOT GATE [INVERTER]

A2332 BIAS POWER INTERLOCK A11149 L-1 LE 1909-1 [H-2] — FUNCTION — RELAY COIL — PRINT LOCATION

OUTPUT

INPUTS

ALL THE RELAYS ARE OF THE "SNAP BALL" TYPE, THAT IS, THEY DELAY AN "ON" SIGNAL THE GIVEN LENGTH OF TIME BUT PASS AN "OFF" SIGNAL INSTANTANEOUSLY.

APPENDIX II

THE QUINE-McCLUSKEY MINIMIZATION TECHNIQUE

The design engineer has completed the first two steps in the design process. He has defined the system input variables and listed the desired input-output conditions. If the system is non-sequential (no time-delays) and too complicated to solve by inspection, the Quine-McCluskey minimization technique may be applied.[II-1,II-2]

Use of this technique results in the realization of the desired circuit in the "simplest sum of products" (Fig. II-1) or the dual, "simplest product of sums" (Fig. II-2) form as desired.

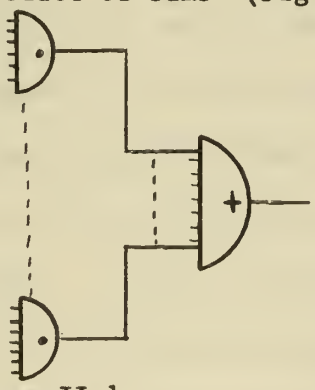


Figure II-1

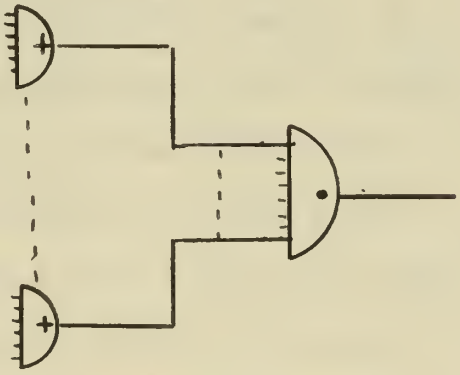


Figure II-2

The purpose of this appendix is not to present a detailed account of the technique, but to present a simple example with limited explanation. If the reader is still interested after this exposure, Chapter 11 of Ledley[II-3] presents a detailed description of the method.

II-1 Quine, W. V., A Way to Simplify Truth Functions, Am. Math. Monthly, Vol. 62, pp 627-631, November, 1955.

II-2 McCluskey, E. J. Jr., Minimization of Boolean Functions, B.S.T.J., Vol. 35, pp 1-26, November, 1956.

II-3 Ledley, R. S., Digital Computer and Control Engineering, McGraw Hill Book Co., 1960.

The Quine-McCluskey technique involves binary numbers called "designation numbers". Every input variable, combination of inputs, and output variable has a unique designation number associated with it. The designation numbers of the input variables are assigned by means of the "basis". The basis of a n-variable system will be a n x2^n matrix of ones and zeros (Fig. II-3, n = 3).

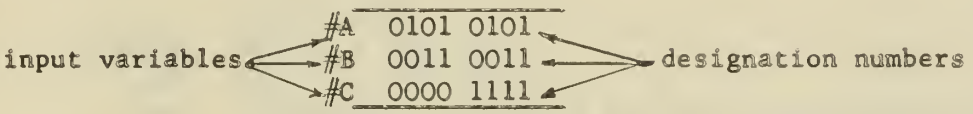


Figure II-3, n = 3

The rows of the basis are the input variable designation numbers, the columns represent all permutations of n ones and zeros, hence 2^n columns.

The output designation number is derived from the basis in the same way that we derived the operational relations in Section 2 from the truth table. In fact, the basis is just a truth table on its side. The basis or truth table is a natural result of the first two steps in the design procedure. For use in this example we assign an arbitrary output variable Y the designation number 0111 0101 and associate it with the basis.

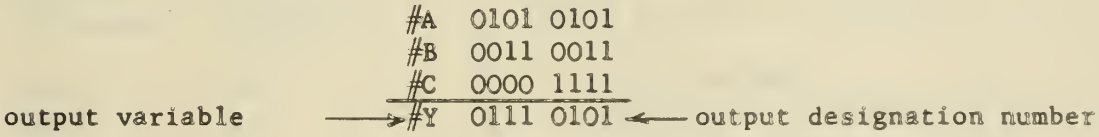


Figure II-4

We see by inspection that one possible Boolean equation for desired output is: $A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + A \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot C = Y$. This is the most complicated expression for the output. The Quine-McCluskey technique derives the simplest.

The technique is based on the implication property of Boolean functions. The goal is to find the "prime implicant", the simplest sum of Boolean products that imply the desired output. By implication we mean that a given designation number implies another designation number ($\#X \rightarrow \#Y$) if $\#X$ does not have ones where $\#Y$ has zeros. For example:

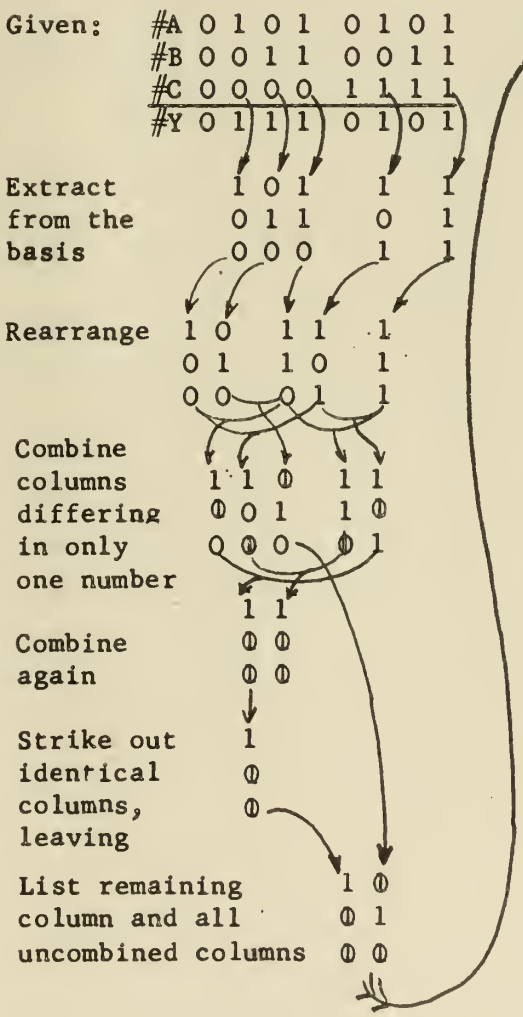
$\#(A \cdot B) \rightarrow \#A$

since $\#(A \cdot B) = 0001\ 0001$

and $\#A = 0101\ 0101$

but $\#A \not\rightarrow \#(A \cdot B)$ since $\#A$ has ones where $\#(A \cdot B)$ does not.

The procedure of the Quine-McCluskey technique is as follows:



The two remaining columns show that the desired output may be formed from the sum of two products.

1
0 corresponds to the single variable A
0
0
1 corresponds to the product $B \cdot \overline{C}$
0

Therefore $Y = A + (B \cdot \overline{C})$

To check:

$\#Y = 0\ 1\ 1\ 1\ \ 0\ 1\ 0\ 1$

$\#A = 0\ 1\ 0\ 1\ \ 0\ 1\ 0\ 1$

$\#B \cdot \overline{C} = 0\ 0\ 1\ 1\ \ 0\ 0\ 0\ 0$

so we see that

$\#A \rightarrow \#Y$, and $\#(B \cdot \overline{C}) \rightarrow \#Y$

and that $\#A + \#(B \cdot \overline{C}) = \#Y$

The Quine-McCluskey technique is of limited usefulness for minimization of circuits with more than seven input variables. The basis gets too big to handle with ease, since the number of columns increases as 2^n. There are digital computer programs in existence that will simplify circuits with up to 24 input variables.

thesC7472
Boolean minimization of large relay inte
3 2768 001 02269 2
DUDLEY KNOX LIBRARY