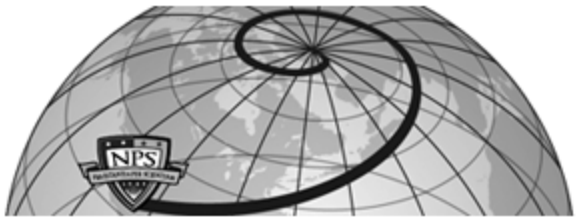

THEORETICAL ANALYSIS OF TWO CORE SELF-SATURATING MAGNETIC AMPLIFIERS

RAYMOND B. YARBROUGH

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the requirements for the degree of

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ABSTRACT

The analysis is based on piecewise linearization of the saturable reactor and semiconductor diode, and the principle of zero average magnetic flux change in a saturable reactor for a cycle which begins and ends with saturation. This allows a purely mathematic analysis in terms of half cycle average values.

The consideration of circuit topology leads to a set of eight realizable output configurations and six basic control configurations for two core amplifiers. The nontrivial combinations of control and output circuits are considered, leading to three classes of two core self-saturating magnetic amplifiers.

The analysis of each class of amplifiers provides terminal relations in the form of finite difference equations. These relations show the inherent limitations of the amplifiers and the optimum control configurations. General design considerations are developed. The theoretical results are compared with the characteristics of actual circuits, showing the limitations of the analysis.

The author wishes to thank Dr. Charles H. Rothauge for his guidance and Dr. George J. Thaler for his encouragement in this investigation.

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TABLE OF SYMBOLS AND ABBREVIATIONS

Symbol	Description
A_c	Cross-section area of magnetic core
A_{cu}	Cross-section area of wire
A_w	Window area of magnetic core
B	Magnetic flux density
$E_j(n)$	Average value of e_j during the n^{th} half cycle
F	Magnetomotive force
f	Frequency
G	Dynamic core conductance referred to gate winding
H	Magnetic field strength
J	Current density
K_I	Current gain
K_p	Power gain
K_v	Voltage gain
k	Dynamic core conductance per turn
l_c	Mean length of magnetic path of a magnetic core
N_j	Turns ratio between the j^{th} winding and the gate winding: n_g/n_j
n_j	Number of turns of the j^{th} winding
T	Period of a half cycle
t	Time
Δ	Incremental change
Φ	Magnetic flux

INTRODUCTION.

From an engineering point of view, a method of analysis should be capable of two accomplishments. First, it should provide design criteria related to the physical properties of the devices under analysis. Secondly, it should determine the utility of new applications of the devices.

The development of magnetic amplifiers was retarded during the first half of the twentieth century by the rapid development and application of vacuum tube amplifiers. The development of semiconductor diodes has permitted realization of high gain magnetic amplifiers which are competitive with vacuum tube and transistor amplifiers.

Magnetic amplifier art produced practical amplifiers prior to the development of adequate methods of analysis. Emerging theories of analysis were tested on the existing circuits with varying degrees of success. The most successful analysis is based on a piecewise linear method, leading to input-output difference equations. This method of analysis has been applied to existing circuits, providing design criteria with reasonable results.

In the work presented here, this method was applied to analyze two-core self-saturating magnetic amplifiers. The objective of the investigation was to determine the best circuit topology for the possible amplifiers as developed in the analysis. The criterion for "best" was that which provides the highest gain.

This work was logically divided into two parts. The

first three chapters established the method of analysis, treating a single core amplifier. Chapters four through eight constituted a systematic investigation of all possible two core self-saturating circuits.

In the first chapter the general philosophy of the method of analysis was presented. The second chapter developed the piecewise linear models for the saturable cores and semiconductor diodes. The third chapter established the logical sequences of modes of operation for a single core circuit.

In chapter four the topology of output and control circuits was considered for two core configurations. Eight fundamental output circuits, three half-wave and five full-wave, were obtained. The four fundamental control circuits without diodes were developed, and two commutated control circuits completed the basic control arrangements.

Half-wave output circuits were investigated in chapter five. The analysis limited the control circuits to series-differential and parallel-differential, and bias circuits to series and parallel connections. This analysis indicated that the parallel-differential control and series bias provide the optimum control, whereas the series-differential control is in general use. Design considerations were developed for each type of circuit.

In chapter six the voltage reset amplifiers were investigated, leading to circuit limitations and design considerations.

Doublet amplifiers were investigated from a general point of view in chapter seven. All possible control circuits without diodes were included to determine the best control and bias connections for each type of amplifier. Design considerations included limits of mode sequences of operation.

The analysis of chapters five and seven indicated that improved performance for three types of amplifiers is possible. In chapter eight these results were verified by laboratory measurements.

CHAPTER I. MAGNETIC AMPLIFIER ANALYSIS

The quantitative analysis of magnetic amplifiers by the use of finite difference equations have been shown [1,2,3] to yield reasonable prediction of their performance for certain waveforms and with resistive loads. The nonlinear elements are linearized in a piecewise manner. For each linear mode of the nonlinear elements linear circuit equations are obtained, and mode sequences are determined from the waveforms and amplitudes of all forcing functions. The finite difference equations are expressed in terms of the half-cycle average values of terminal quantities. The use of half-cycle averages arises naturally from the cyclic operation of the saturating magnetic core.

The principle of operation of the self-saturating magnetic amplifier is qualitatively explained in terms of the fundamental circuit shown in Figure 1.1. The alternating power source e_g is adjusted to drive the core flux from negative to positive saturation in exactly one half-cycle of the source frequency if it were applied directly to the gate winding n_g. Then if the initial flux at the beginning of the positive or gating half-cycle is between positive and negative saturation the core will reach what is chosen as positive saturation at some time before the end of the half-cycle.

[1] P.R. Johannessen, Analysis of Magnetic Amplifiers by the use of Difference Equations, AIEE Transactions, Pt. 1 (Communications and Electronics), Vol 73, 1954 (Jan. 1955 section) pp 700-11.

[2] H. C. Bourne, and Nitzan, D., Institute of Engineering Research University of California, Berkeley. Ferromagnetic Core Functions in the Analysis and Design of Self-Saturating Magnetic Amplifiers. Series No. 60, Issue No. 261. Dec. 1, 1959

[3] P.R. Johannessen, Analysis of Magnetic Amplifiers with Diodes. Communications and Electronics, No. 45. Nov. 1959, pp 485-504.

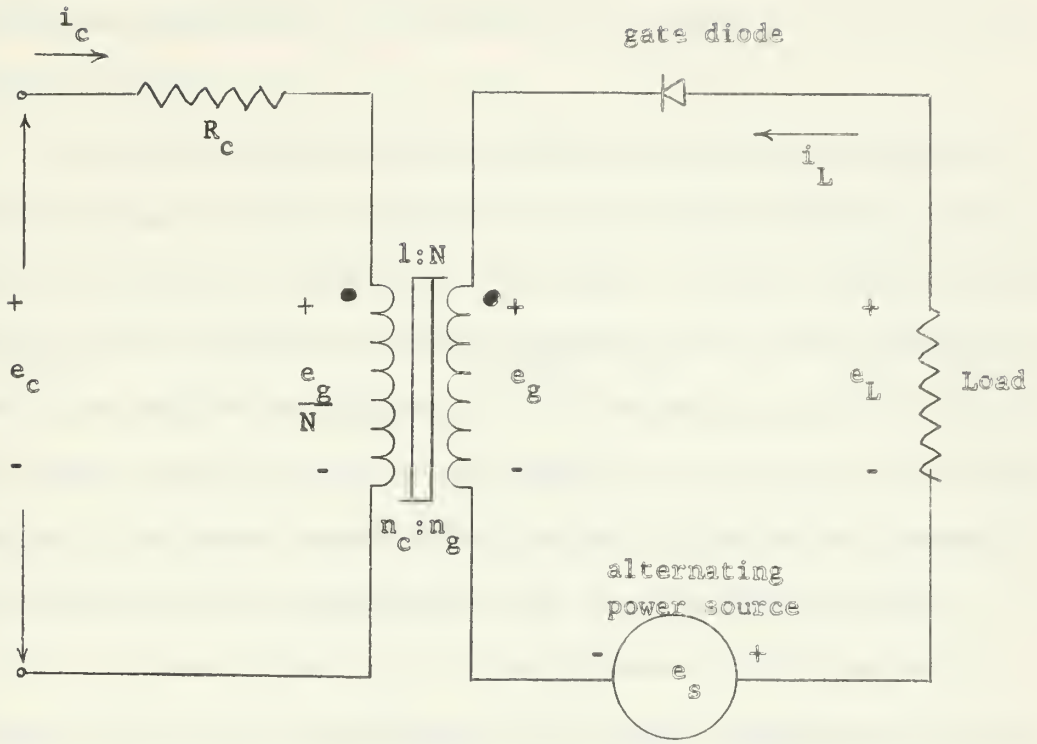


Figure 1.1. Fundamental Self-saturating Magnetic Amplifier.

Prior to saturation the voltage e_g appears across the gate windings n_g, caused by the time rate of change of flux: $e_g = n_g \frac{d\Phi}{dt}$. The dot convention is chosen so that a positive voltage at the dot corresponds to a positive time rate of change of flux. During the time when the flux is increasing, the gating interval of the positive or gate half-cycle, the core absorbs a large fraction of the supply voltage thereby limiting the output current. After the core has reached saturation flux the time rate of change of flux is small and the current is limited only by the

loop resistance. In this manner the core acts as a switch which limits the current prior to saturation and allows it to flow freely after saturation.

In the power-source negative half-cycle the diode absorbs the source voltage. If the core is to be reset from saturation it must be done by the control voltage e_c. In order to provide reset the control voltage must be negative. At the beginning of the reset interval the flux is at positive saturation. In the following gate half-cycle the flux again reaches saturation and remains at saturation until the beginning of rhe reset interval that follows. Thus the net change of flux during the cycle beginning at the onset of reset is zero.

As the core voltage e_g is proportional to the time rate of change of flux, the time integral of the core voltage over the cycle beginning at the onset of reset is zero. Thereby the average of the core voltage during the cycle is also zero. From this it follows that the average of the core voltage E_g in the gate interval is the negative of that in the reset interval.

The average value of the output current in the gate half-cycle is the difference between the average values of the source voltage and the core voltage divided by the loop resistance. As the average of the core voltage in the gate half-cycle is the negative of its average in the previous reset half-cycle provided the core started the reset half-cycle at saturation and again reaches saturation in the gate half-cycle, the average of the load current in the gate half-cycle is proportional to the average core voltage in the previous reset half cycle. If the core is not allowed to reach negative satura-

tion during the reset half-cycle the change of flux, and thereby the average core voltage is proportional to the average of the control voltage during the reset half-cycle. It follows that the average load current in the gate half-cycle is then proportional to the average control voltage in the previous reset half-cycle, under the above restrictions.

The above proportionality can be expressed in the form of a degenerate difference relation:

$$I_L\,(k+1) \propto E_c\,(k) \tag{1.1}$$

where the capital letters indicate half-cycle average values, and k indicates the reset half cycle and $k+1$ the following gate half-cycle.

Similar relations for the control current in terms of differences may be obtained. The average value of this current in any half-cycle is proportional to the difference between the averages of the control voltage and the core voltage divided by the turns ratio:

$$R_c I_c(k) = E_c(k) - E_g(k)/N \tag{1.2}$$

and

$$R_c I_c(k+1) = E_c(k+1) - E_g(k+1)/N \tag{1.3}$$

As $E_g(k)$ is proportional to the control voltage equation 1.2 yields the proportionality:

$$I_c(k) \propto E_c(k) \tag{1.4}$$

The average of the core voltage in the gate half-cycle is the negative of its average in the previous reset half-cycle. Then equation 1.3 yields the proportionality:

$$I_c(k+1) \propto E_c(k+1) + AE_c(k) \tag{1.5}$$

where A is a positive constant.

The above relations have been obtained under a set of assumptions which have been indicated: the control voltage is negative, at least during the reset half-cycle; at the beginning of the reset half-cycle the initial value of flux is positive saturation; the core does not saturate negatively; the core again reaches positive saturation in the following gate half-cycle; and though not previously stated explicitly, the diode is back biased (blocked) during the reset half-cycle, and conducting the gate half-cycle.

This qualitative discussion has indicated the normal operation of the fundamental circuit, and has shown the method of finite differences applied to half-cycle average values of terminal quantities leads to linear relations. It is necessary to investigate the nonlinear elements and establish instantaneous relations before quantitative results may be obtained.

CHAPTER II. PIECEWISE LINEAR ANALYSIS

The quantitative analyses of circuits containing nonlinear elements require a mathematic approximation or model for each nonlinearity. The piecewise linear technique has been found to provide results which are useful in the design of complex magnetic amplifier circuits. In this method of analysis the nonlinear element is approximated as linear over limited ranges of its operation. In each of these modes of operation the device is described by a set of linear differential equations with constant coefficients. In the transition from one mode of operation to another, the final values of the one are the initial conditions of the other.

For simplicity of analysis, the minimum number of modes which still retain the essential nature of the nonlinear element are generally desirable. In this way the analysis yields results which are of the proper form, though not as accurate as could be obtained by considering more modes. Some accuracy is sacrificed to prevent the analysis from becoming unduly complicated.

The operation of the self-saturating magnetic amplifier is dependent on the nonlinearity of the saturable core and that of the diode. The alternating power source in series with the core and diode causes the operation of the circuit to be periodic. The saturable core undergoes a sequence of modes during each cycle of the source, and the diode may alternate between the forward and back biased condition several times during the cycle. Prior to discussion of mode sequences it is necessary to establish models for the nonlinear elements.

2.1 Diode Characteristics

The static volt-ampere characteristic for a typical semiconductor diode is shown in figure 2.1 and a piecewise linear model in figure 2.2 Reverse breakdown of the diode is not considered as it is avoided by design. Though the reverse current for a semiconductor diode is small, it may be neglected only if it is much smaller than the magnetizing current associated with the winding through which it flows. If this requirement is satisfied the mathematical model for the diode may be expressed by the following two equations:

Mode 1: $v = V_f + iR_f \qquad v \geq V_f \qquad (2.1)$

Mode 2: $i = 0 \qquad v < V_f \qquad (2.2)$

2.2 Saturable Reactor Characteristics

The saturable core is more complex in its behavior than the diode, and requires more modes to describe its behavior adequately. A threshold value of magnetomotive force must be exceeded before the flux can change, as shown in the static flux-mmf characteristic in figure 2.3. Once the threshold mmf has been reached, if the flux is to change at a finite rate, additional mmf must be supplied to compensate for eddy current losses. The dynamic relation of the time rate of change of flux and mmf for a typical saturable reactor is shown in figure 2.4 with sinusoidal excitation. The corresponding dynamic flux-mmf characteristic is shown superimposed with dashes.

A piecewise linear model for the unsaturated region of figure 2.4 is shown in figure 2.5. When saturated the time rate of change of flux is small, and for mathematical convenience is considered negligible. The saturable reactor may then be approximated by five modes of operation, as follows:

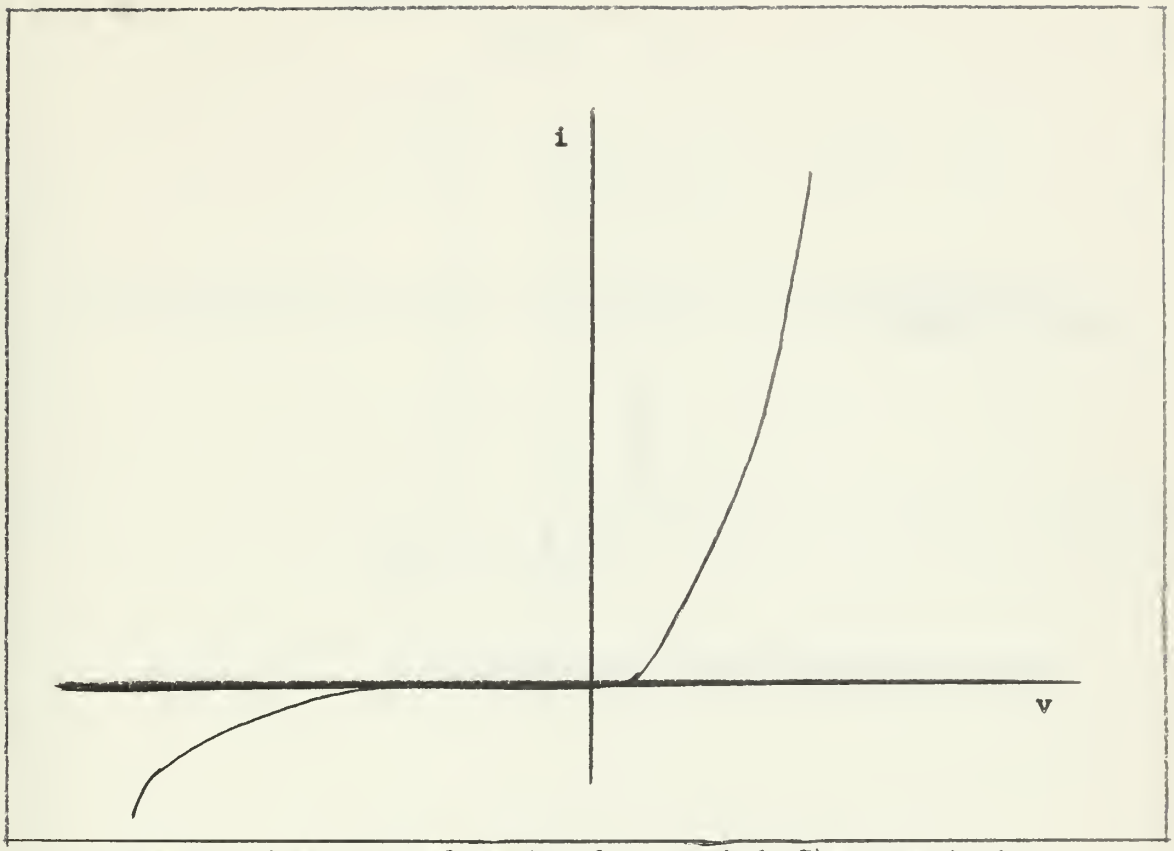


Figure 2.1 : Typical Semiconductor Diode Characteristic.

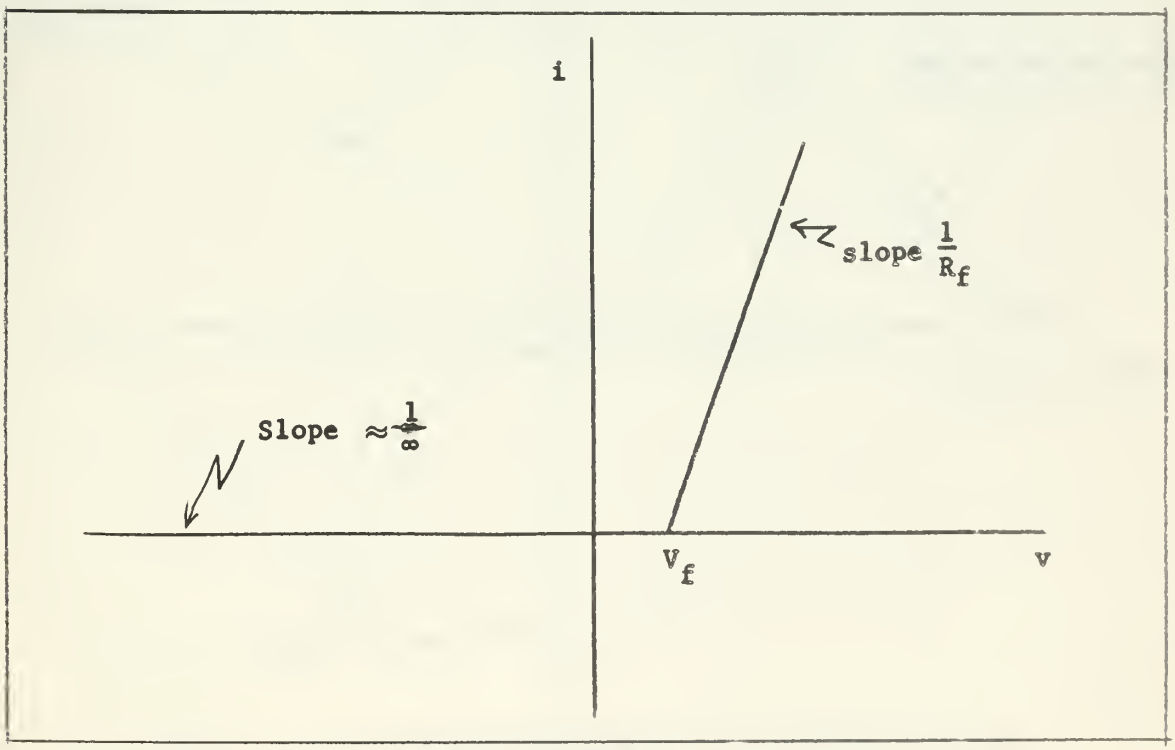


Figure 2.2 : Piecewise Linear Model for Semiconductor Diode.

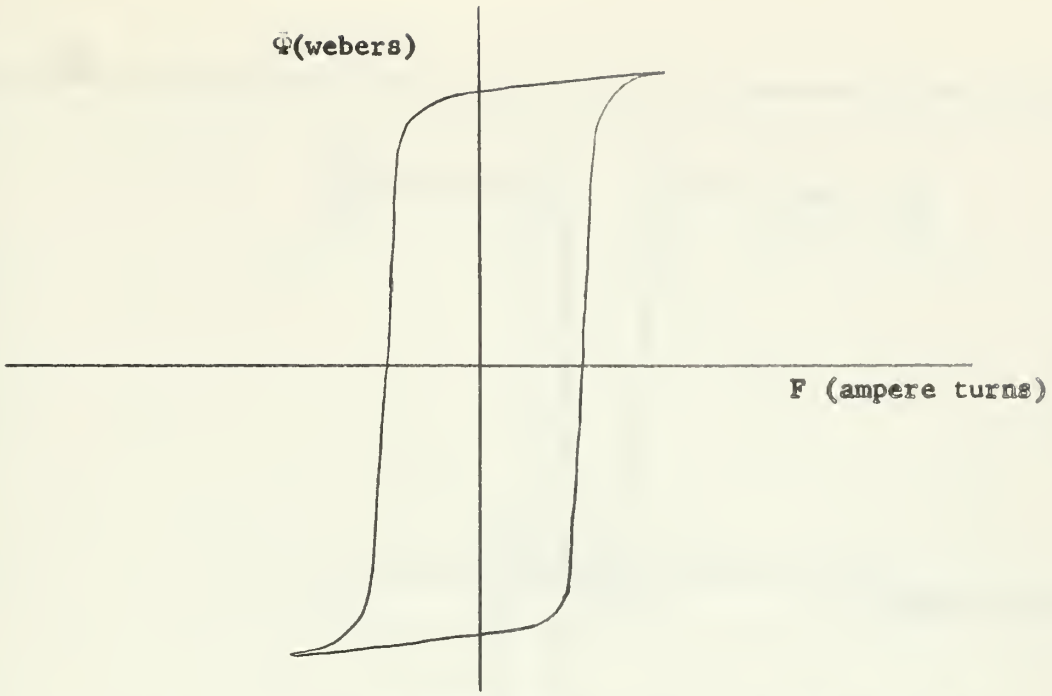


Figure 2.3 Saturable Reactor Static Hysteresis Loop.

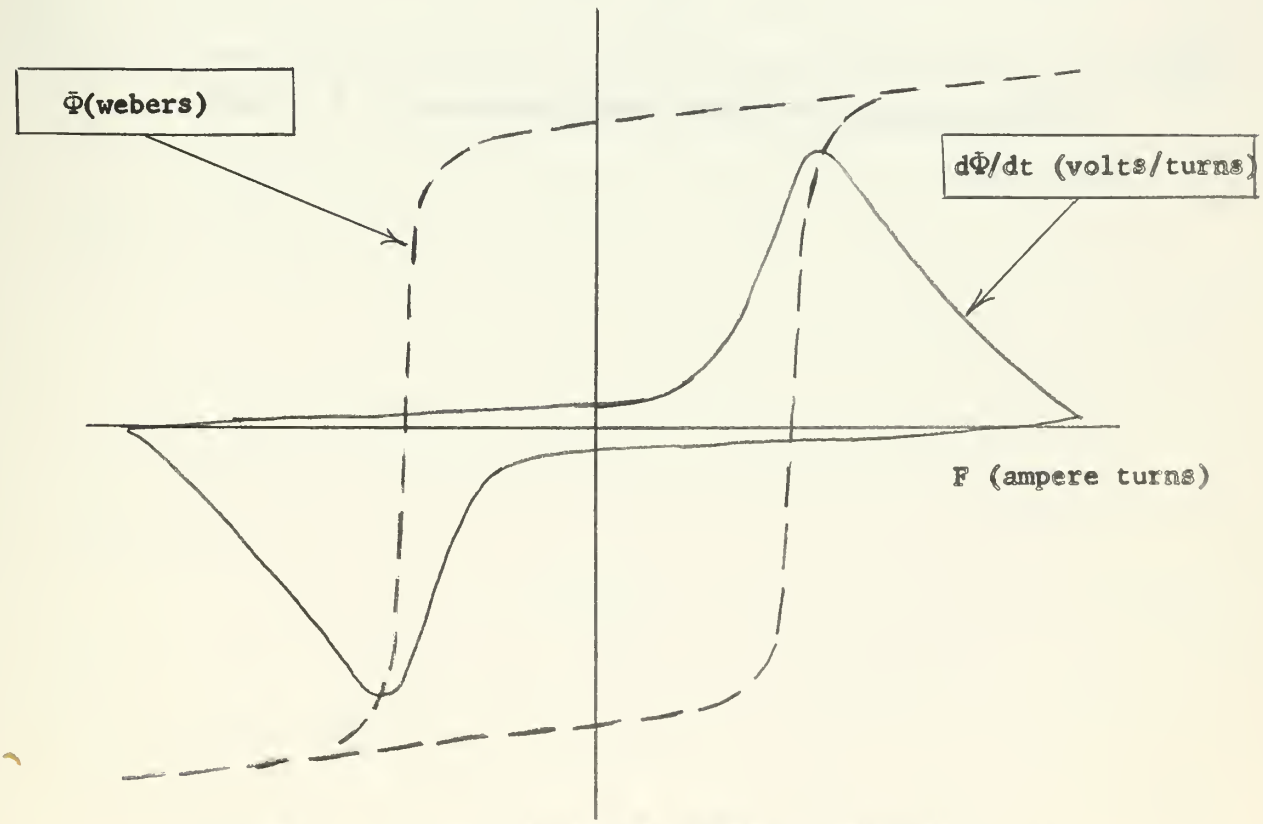
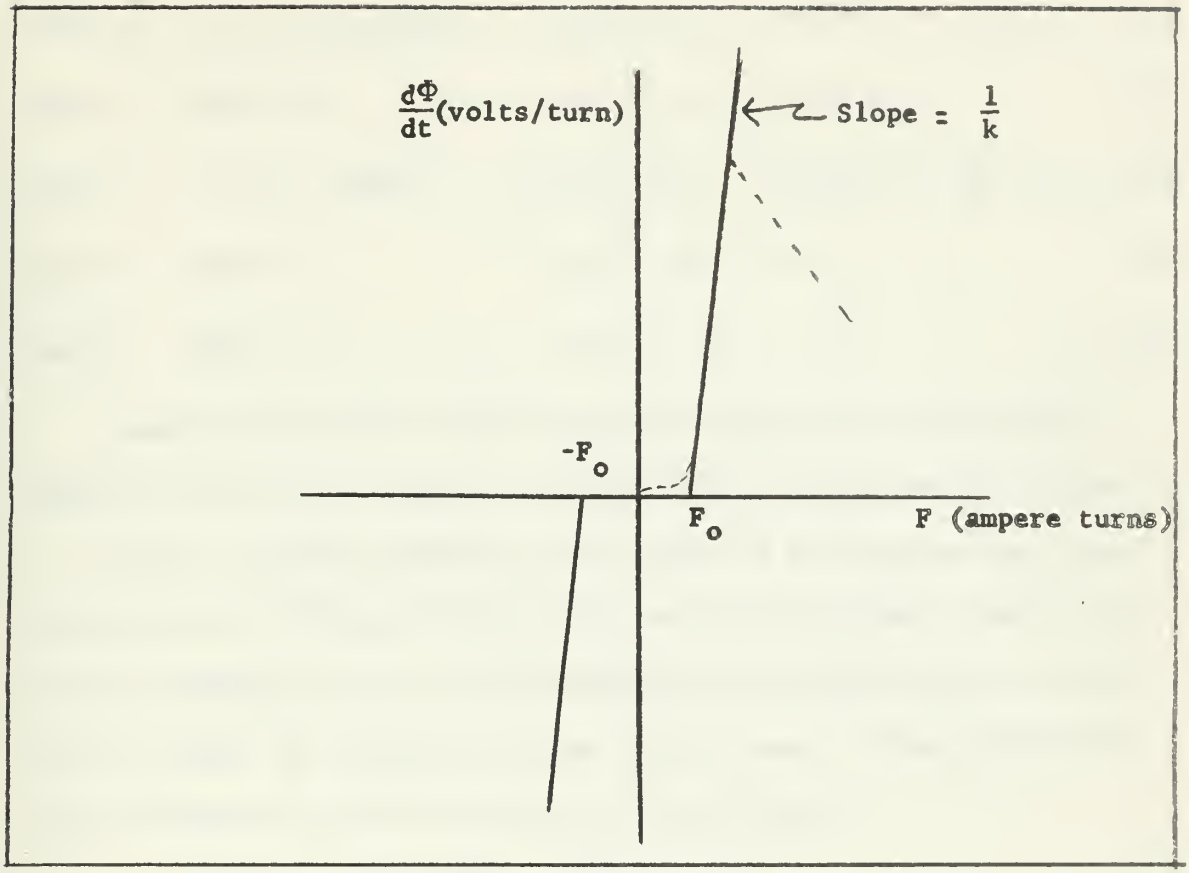


Figure 2.4 Saturable Reactor Dynamic Characteristics.



Figur 2.5 : Piecewise Linear Model for Unsaturated Core.

Mode A: $F = -F_o + k d\Phi/dt$ for $F \leq -F_o$, $d\Phi/dt < 0$, $|\Phi| < \Phi_s$ (2.3)

Mode B: $d\Phi/dt = 0$ for $|F| < F_o$, $|\Phi| < \Phi_s$ (2.4)

Mode C: $F = F_o + k d\Phi/dt$ for $F \geq F_o$, $d\Phi/dt > 0$, $|\Phi| < \Phi_s$ (2.5)

Mode D: $d\Phi/dt = 0$ for $\Phi = \Phi_s$, $F > -F_o$ (2.6)

Mode E: $d\Phi/dt = 0$ for $\Phi = -\Phi_s$, $F < F_o$ (2.7)

These relations are used in design considerations and are more useful if referred to the basic properties and dimensions of the core.

With a constant frequency power source of rectangular wave form the time rate of change of flux must meet the requirement that, with the core completely reset at the beginning of a half-cycle, the time rate of change of flux must be less than or equal to that which will cause saturation at the very end of the half-cycle:

$$\left.\frac{d\Phi}{dt}\right|_{max} \leq \frac{2\Phi_s}{T} = 4f\Phi_s \tag{2.8}$$

The magnetizing force required for this value of time rate of change of flux is found from figure 2.5 to be:

$$F_m = F_o + k \left.\frac{d\Phi}{dt}\right|_m = F_o + k\ 4f\Phi_s \tag{2.9}$$

From this a value of k may be determined if the magnetomotive force - time rate of change of flux characteristic of the core is available:

$$k = \frac{F_m - F_o}{4f\Phi_s} \tag{2.10}$$

This is more conveniently referred to the core parameters when the only source of information is manufacturers data. In this case an estimation of the core function may be made from the dynamic and static

B - H loops which are generally available.[4]

Then from the relations of Ampere's Law and Faraday's Law:

$$k = \frac{(H_f - H_o)\ell_c}{4\, f\, A_c B_s} \tag{2.11}$$

$$F_o = H_o \ell_c \tag{2.12}$$

where: H_f is the average magnetizing field strength at the operating frequency; H_o is the average static magnetizing field strength for the case where manufacturers data is used, or, where $H - \frac{dB}{dt}$ curves are available, the intercept of the straight line approximation on the H axis; ℓ_c is the mean length of magnetic path; A_c is the effective core cross-sectional area; and B_s is the saturation flux density. All quantities in the M K S rationalized system.

2.3 The Basic Circuit

The circuit for the basic self-saturating magnetic amplifier is shown in figure 2.6. The n-1 control windings on the left and the output or gate winding on the right of the core make up the n windings of the core. All of the control loops have a similar form, with an unspecified control voltage and control current. The gate loop differs in that it has an alternating power source and a diode in series with the winding.

The circuit contains two nonlinear elements, the saturable core, and the diode. The piecewise linear models have been assumed to have the modes defined in the previous sections, two modes for the diode, and five for the core.

[4]For instance Magnetics Incorporated Catalogue #TWC-300
Magnetics Incorporated - Butler, Pa. 1962

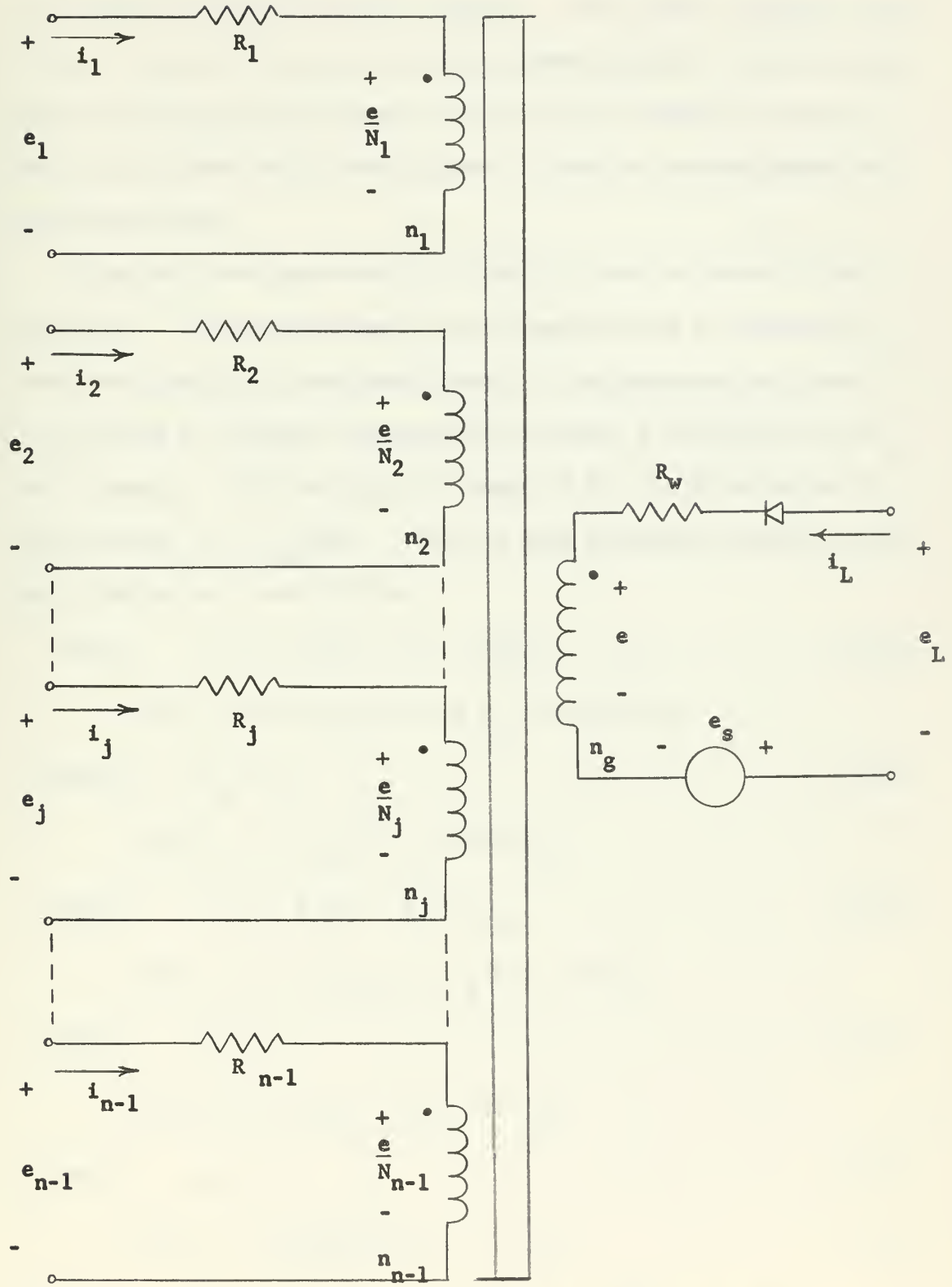


Figure 2.6: Basic Self-saturating Magnetic Amplifier Circuit.

All possible combinations of each diode mode with each core mode yield ten possible modes of circuit operation. The general analysis of the circuit requires that the relations between terminal quantities and the core voltage be determined for each mode. Then the limits for each circuit mode may be established in terms of instantaneous terminal conditions.

The core mode equations 2.3 through 2.7 are in terms of core quantities. These equations are more readily used if referred to the gate winding by transformer theory. The magnetomotive force F is referred by dividing the equations for Mode A and Mode C by the gate turns n_g. The time rate of change of flux is referred to the gate voltage $e_g = n_g d\Phi/dt$. The core mode equations referred to the gate winding are then written:

Mode A: $$i_L + \Sigma\, i_j/N_j = -I_o + Ge_g \quad \ldots\ldots\ldots\ldots \quad (2.13)$$

with $i_L + \Sigma\, i_j/N_j \leqq -I_o$, $e_g < 0$, $|\Phi| < \Phi_s$

Mode B: $$e_g = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2.14)$$

with $|i_L + \Sigma\, i_j/N_j| < I_o$, $|\Phi| < \Phi_s$

Mode C: $$i_L + \Sigma\, i_j/N_j = I_o + Ge_g \quad \ldots\ldots\ldots\ldots \quad (2.15)$$

with $i_L + \Sigma\, i_j/N_j \geqq I_o$, $e_g > 0$, $|\Phi| < \Phi_s$

Mode D: $$e_g = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2.16)$$

with $i_L + \Sigma\, i_j/N_j > -I_o$, $\Phi = \Phi_s$

Mode E: $$e_g = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2.17)$$

with $i_L + \Sigma\, i_j/N_j < I_o$, $\Phi = -\Phi_s$

where: $N_j = n_g/n_j$, $I_o = F_o/n_g$ and $G = k/n_g^2$

The control loops may be represented by the single expression indicating the generic loop:

$$i_j/N_j = e_j/N_jR_j - (1/N_j^2R_j)e_g \qquad (2.18)$$

where j may take on any integer value from one to n-1.

The diode mode equations may be incorporated into the gate loop equation:

Mode 1: $$e_s + e_L - V_f = i_LR_w + e_g,\ i_L \geq 0 \qquad (2.19)$$

Mode 2: $$e_s + e_L = v_r + e_g,\ v_r < V_f \qquad (2.20)$$

The circuit solutions for each circuit mode are obtained by solving the n-1 control loop equations first with equation 2.19 then with equation 2.20 for each of the core mode equations. The expressions for core voltage and the limits for each mode are tabulated in table 2.1.

From the limits of the modes given in table 2.1 it is seen that when the sum of the source voltage and load terminal voltage exceeds the forward voltage drop of the diode, the possible modes are A1, B1, C1, C2, D1 and E1. When the sum of the source and load voltages is less than the forward diode drop the possible modes are A1, A2, B2, C2, D2 and E2. The ranges of the possible modes for these two situations are indicated in figure 2.7. The case where the sum of the source and load voltages exceeds the forward drop of the diode are shown in figure 2.7 and the case for the sum less in figure 2.7b.

It is convenient for design purposes to refer the core parameters to the gate circuit. These are related to G and I_o as follows:

$$G = \frac{(H_f - H_o)\ell_c}{4fn_g^2 A_c B_s} \qquad (2.21)$$

$$I_o = \frac{H_o\ell_c}{n_g} \qquad (2.22)$$

Table 2.1

MODE	Core voltage e_g	Mode limits
A 1	$\dfrac{(e_s+e_L-V_f)/R_w+I_o+\Sigma e_j/N_jR_j}{G+1/R_w+\Sigma 1/N_j^2R_j}$	$\Sigma e_j/N_jR_j \lessgtr \begin{cases}(G+\Sigma 1/N_j^2R_j)(e_s+e_L-V_f)-I_o \\ -(e_s+e_L-V_f)/R_w-I_o\end{cases}$ Which-ever is alge-braically least
A 2	$\dfrac{\Sigma e_j/N_jR_j+I_o}{G+\Sigma 1/N_j^2R_j}$	$(G+\Sigma 1/N_j^2R_j)(e_s+e_L-V_f)-I_o<\Sigma e_j/N_jR_j<-I_o$
B 1	0	$-I_o-(e_s+e_L-V_f)/R_w<\Sigma e_j/N_jR_j<I_o-(e_s+e_L-V_f)/R_w$ and $e_s+e_L>V_f$
B 2	0	$-I_o<\Sigma e_j/N_jR_j<I_o$ and $e_s+e_L<V_f$
C 1	$\dfrac{(e_s+e_L-V_f)/R_w-I_o+\Sigma e_j/N_jR_j}{G+1/R_w+\Sigma 1/N_j^2R_j}$	$\Sigma e_j/N_jR_j > I_o-(e_s+e_L-V_f)/R_w$ $\Sigma e_j/N_jR_j <I_o+(e_s+e_L-V_f)(G+\Sigma 1/N_j^2R_j)$
C 2	$\dfrac{\Sigma e_j/N_jR_j-I_o}{G+\Sigma 1/N_j^2R_j}$	$\Sigma e_j/N_jR_j > \begin{cases}I_o \\ I_o+(e_s+e_L-V_f)(G+\Sigma 1/N_j^2R_j)\end{cases}$ Which-ever is algebraically greater
D 1	0	$\Sigma e_j/N_jR_j> -I_o-(e_s+e_L-V_f)(G+\Sigma 1/N_j^2R_j)$ and $e_s+e_L > V_f$
D 2	0	$\Sigma e_j/N_jR_j >-I_o-(e_s+e_L-V_f)/R_w$ and $e_s+e_L<V_f$
E 1	0	$\Sigma e_j/N_jR_j< I_o-(e_s+e_L-V_f)/R_w$ and $e_s+e_L > V_f$
E 2	0	$\Sigma e_j/N_jR_j <I_o-(e_s+e_L-V_f)/R_w$ and $e_s+e_L < V_f$

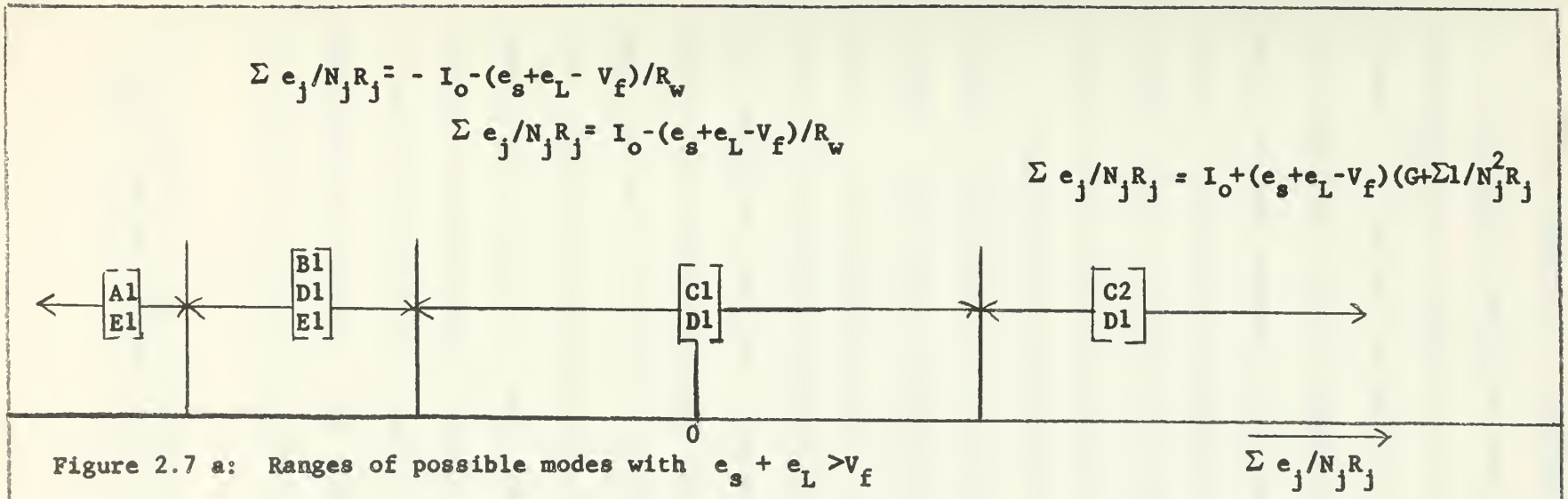


Figure 2.7 a: Ranges of possible modes with $e_s + e_L > V_f$

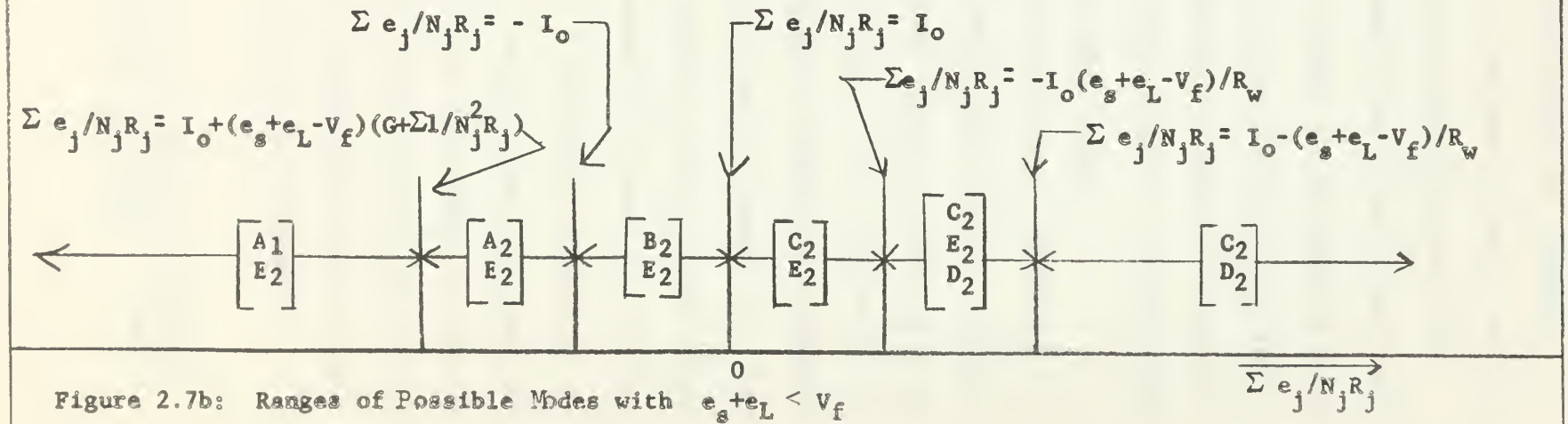


Figure 2.7b: Ranges of Possible Modes with $e_s+e_L < V_f$

CHAPTER III. SEQUENTIAL ANALYSIS WITH DC CONTROL.

The magnetic amplifier operates in a sequence of modes which are constrained to be periodic by the periodicity of the power source. Dynamic or transient analysis of the magnetic amplifier is made under the assumption of small signals about a steady state operating point where the mode sequence is assumed that of the corresponding steady state. To carry out a sequential analysis it is necessary that the possible modes of operation be known. This requires a detailed knowledge of the terminal and source voltage wave forms.

DC amplification constitutes perhaps the widest application of magnetic amplifiers, and is the least complicated type of a control to analyze. The source waveform which is most like a dc input is rectangular. The advantage of the rectangular wave over a sinusoid lies in the instantaneous reversal of its amplitude, whereas the sinusoid is a continuous function. The rectangular wave is capable of instantaneously switching the diode from the forward to the reversed biased condition and of supplying sufficient magnetizing current to initiate flux change at the instant of reversal. The sinusoid requires a more complicated analysis as there are time intervals when the magnetizing current is insufficient to cause flux change, and causes the reversal of the diode condition to occur at times other than when the source wave reverses polarity. The choice of a rectangular source is not impractical, as the static inverter[5] provides such a waveform

[5] G. H. Royer, "A Switching Transistor DC to AC Converter Having an Output Frequency Proportional to the DC Input Voltage." Communications and Electronics, No. 19, pp 322-26, July 1955.

economically when the required operating frequencies are other than available power frequencies.

3.1 Steady State Modes with DC Terminal Voltages

The ranges of the modes are given in figure 2.7. With the terminal voltages assumed constant it is possible to determine the possible modes of operation as a function of the level of the terminal voltages. For a non-trivial mode sequence to exist, that is one in which there is a change of flux during the cycle, both Mode A and Mode C must be contained in the region. From figure 2.7a it is found that for mode C to exist it is necessary that:

$$\Sigma\, e_j/N_jR_j > I_o - (|e_s + e_L - V_f|)(1/R_w) \qquad (3.1)$$

And from figure 2.7b for mode A to exist it is necessary that:

$$\Sigma e_j/N_jR_j < -\, I_o \qquad (3.2)$$

Then the limits for the non-trivial sequences of operation with DC control are:

$$I_o - (|e_s + e_L - V_f|)(1/R_w) < \Sigma\, e_j/N_jR_j < -\, I_o \qquad (3.3)$$

and necessarily:

$$e_s + e_L - V_f > 2\, I_oR_w \qquad (3.4)$$

Within these limits it is possible for two sets of modes to exist: A2, C1, D1, E2, and A1, C1, D1, E2.

If a further restriction is placed on the circuit operation, that the core be allowed to saturate only once per cycle, then four non-trivial steady state mode sequences may be postulated:

Sequence I : A2-C1-D1

Sequence II : C1-A2-E2

Sequence III: C1-A1-E2

Sequence IV : A1-C1-D1

Each of the sequences is defined to start at the instant in time that the core flux reversal from saturation is initiated. The flux transitions for each of the sequences are indicated in figure 3.1. In each of these sequences it is noted that it is necessary for a zero time transition through core mode B.

As the core begins and ends the sequence at saturation the net change of flux for the cycle is zero. The average value of the core voltage being proportional to the average flux is also then zero for the sequence cycle. For each of the sequences postulated the core is reset during one half-cycle of the source voltage, and gated to saturation in the following half-cycle.

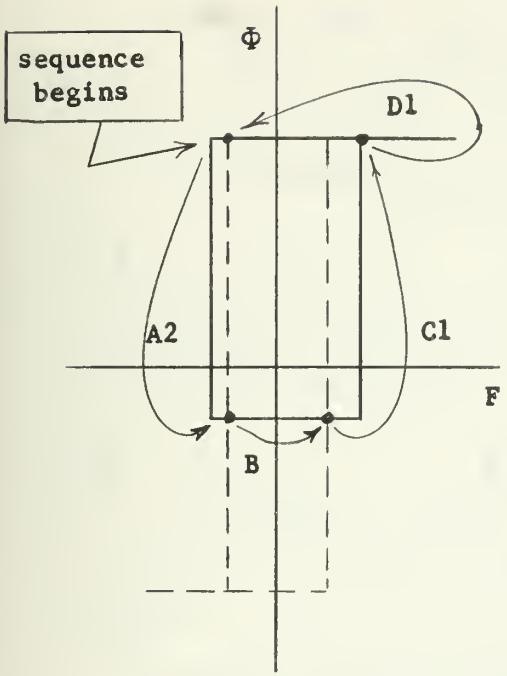
3.2 Mode Sequence I

Under the assumed terminal conditions the waveforms of the circuit for sequence I are shown in figure 3.2. In this sequence the diode is forward biased during the positive half-cycle and reversed biased in the negative half-cycle of the source. The load current in the negative half-cycle is constrained to be zero and the load voltage is irrelevant except in determining the limits of the sequence. In the positive half-cycle, as the diode is forward biased, the average value of the load current is found from equation 2.14:

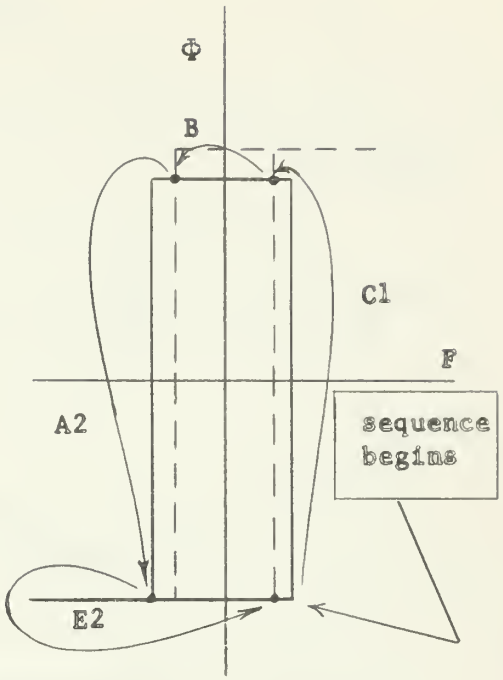
$$I_L(k+1) = \frac{1}{R_w T}\int_{kT}^{(k+1)T} (e_s + e_L - V_f - e_g)\, dt \qquad (3.5)$$

where $k + 1$ indicates the positive half-cycle of the source, which for this sequence is the gating half-cycle.

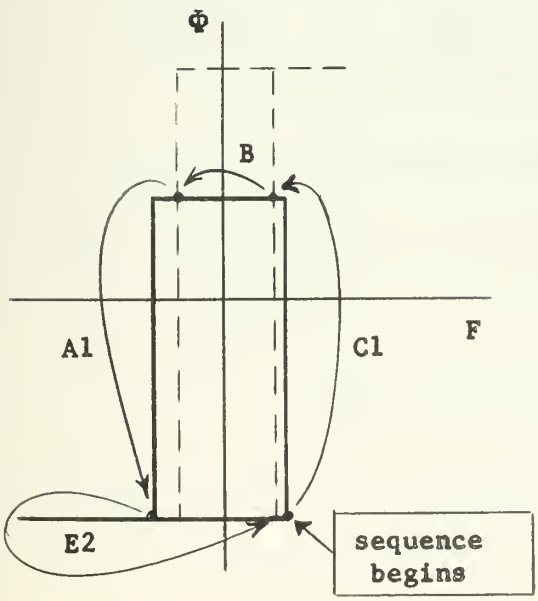
The integral can be broken into four separate integrals, each of these upon integration yields the average of each of the quantities



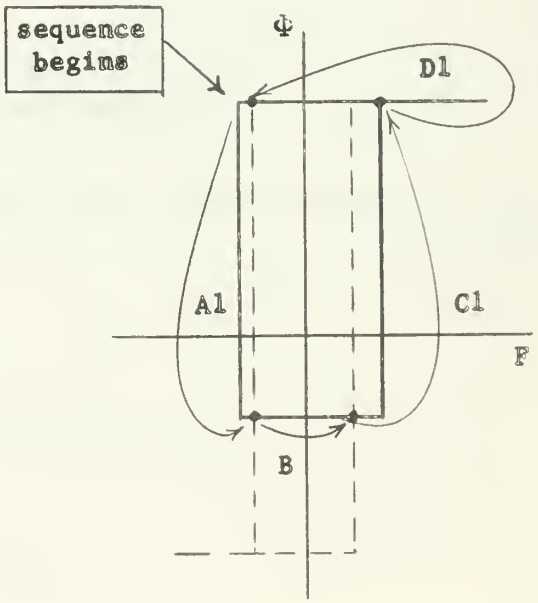
(a) Mode sequence I



(b) Mode sequence II



(c) Mode sequence III



(d) Mode sequence IV

Figure 3.1 Flux Magnetomotive Force Relations for Mode Sequences.

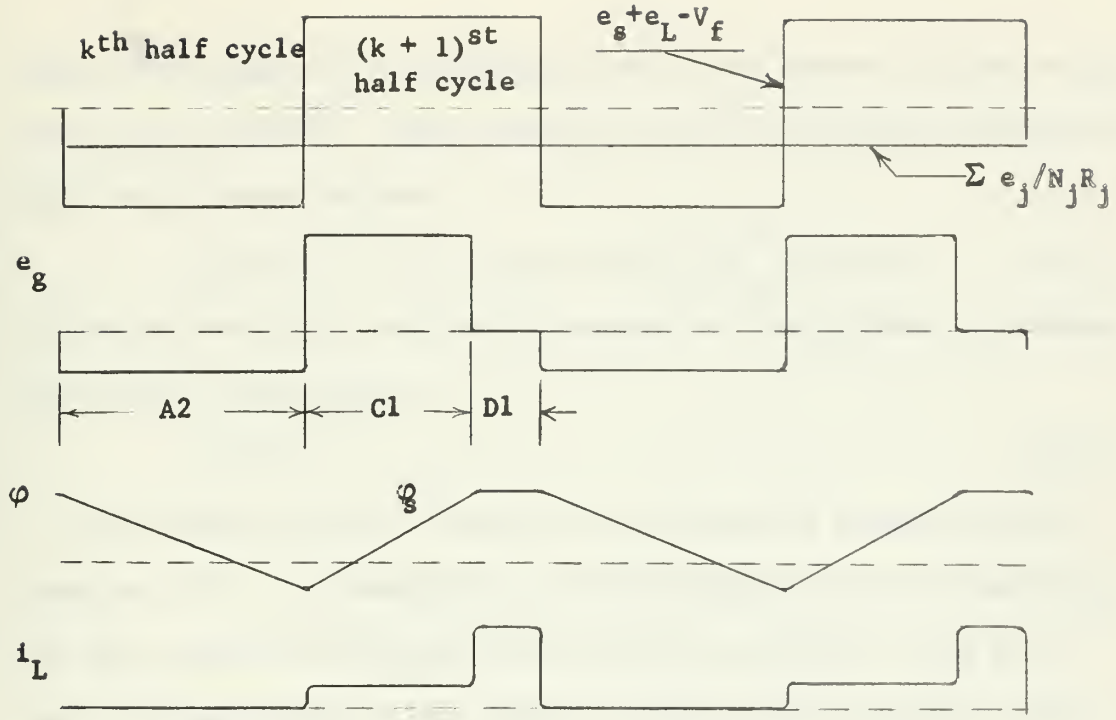


Figure 3.2 Waveforms for Mode Sequence I.

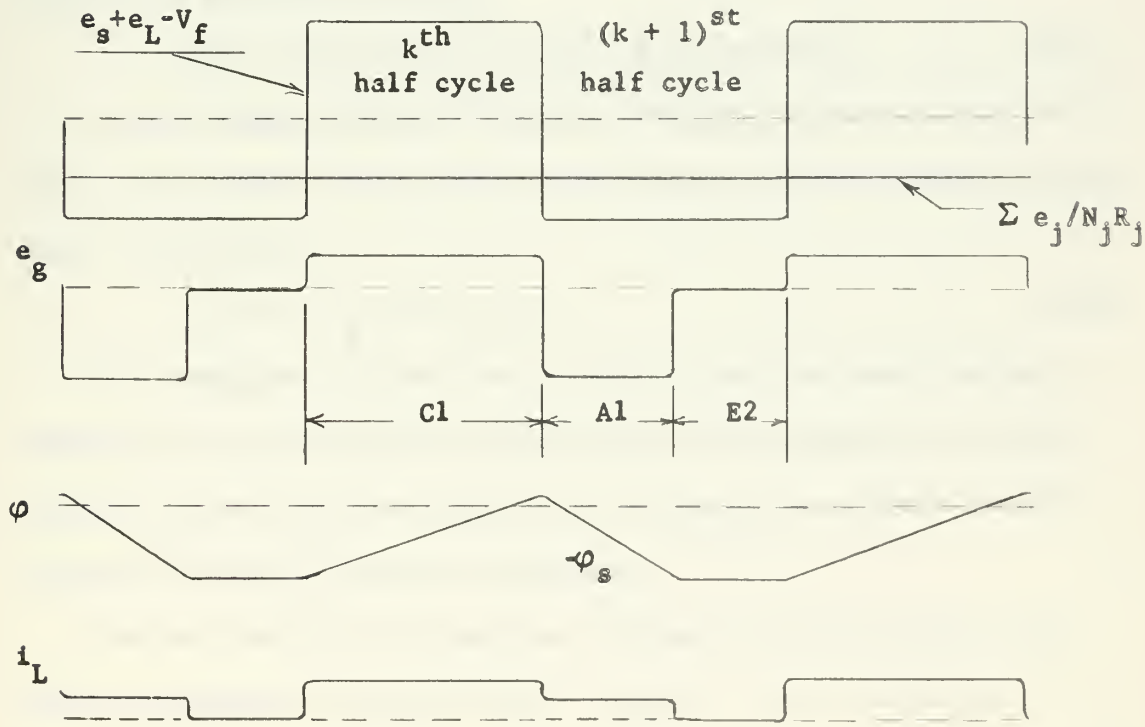


Figure 3.3 Waveforms for Mode Sequence III.

under the integrand. The average value of the source voltage is E_s, and V_f is a constant. Then equation 3.5 may be written in terms of the half cycle average values:

$$R_w I_L(k + 1) = E_s + E_L(k + 1) - V_f - E_g (k + 1) \qquad (3.6)$$

In the negative half cycle of the source the load current is blocked by the back biased diode:

$$I_L (k) = 0 \qquad (3.7)$$

The control circuit currents may be obtained at any time from equation 2.13. By integration of this expression over the appropriate half cycle and division by the half cycle period T, the half cycle average values of the control currents may be obtained. The typical control current in the reset half cycle then is:

$$R_j I_j (k) = E_j (k) - E_g(k)/N_j \qquad (3.8)$$

And in the gating half cycle:

$$R_j I_j (k + 1) = E_j (k + 1) - E_g (k + 1)/N_j \qquad (3.9)$$

As the average value of the core voltage is zero for the entire cycle, the average value of the core voltage for the two half cycles has the relation:

$$E_g (k) + E_g (k + 1) = 0 \qquad (3.10)$$

The addition of equations 3.8 and 3.9 and the substitution of equation 3.10 into the result shows that the average value of any control current over the full cycle is simply the average terminal voltage divided by the loop resistance.

The average value of the core voltage in the gate half cycle may be eliminated from equations 3.6 and 3.9 with equation 3.10. This eliminates any necessity of knowledge of the saturation interval during the gate half cycle. The average value of the core voltage may

be obtained by averaging the expression given in table 2.1 for mode A2, as the reset half-cycle and the mode are concurrent. The terminal difference equations are then obtained by substitution:

$$R_w I_L(k+1) = E_s - V_f + E_L(k+1) + \frac{\Sigma E_j(k)/N_j R_j + I_o}{(G + \Sigma \frac{1}{N_j^2 R_j})} \tag{3.11}$$

$$R_j I_j(k+1) = E_j(k+1) + \frac{\Sigma E_j(k)/N_j R_j + I_o}{N_j(G + \Sigma \frac{1}{N_j^2 R_j})} \tag{3.12}$$

$$R_j I_j(k) = E_j(k) - \frac{\Sigma E_j(k)/N_j R_j + I_o}{N_j(G + \Sigma \frac{1}{N_j^2 R_j})} \tag{3.13}$$

In spite of the fact the above difference equations were obtained under restricted waveforms, the results are quite general as long as the mode sequence is sequence I.

3.3 Mode Sequence II.

In this sequence the positive half-cycle of the source is the reset half-cycle, because the core begins at negative saturation. The gate half cycle is the negative half-cycle, because the core saturates negatively during this interval. The diode is forward biased in the positive half cycle and back biased in the negative half-cycle as in sequence I: however the roles of the half-cycles are interchanged. The output current occurs in the reset half-cycle, and the terminal equations in terms of the half-cycle averages are:

$$R_w I_L(k) = E_s - V_f + E_L(k) - E_g(k) \tag{3.14}$$

$$I_L(k+1) = 0 \tag{3.15}$$

$$R_j I_j(k) = E_j(k) - E_g(k)/N_j \tag{3.16}$$

$$R_j I_j(k+1) = E_j(k+1) - E_g(k+1)/N_j \tag{3.17}$$

The average value of the core voltage over the cycle beginning at the start of the positive half-cycle is zero:

$$E_g(k) + E_g(k+1) = 0 \tag{3.10}$$

The core voltage in the reset half-cycle in the sequence is that of mode C1. Mode C1 and the positive half-cycle are concurrent for this sequence. Then the average value of the core voltage in the reset half-cycle is obtained by averaging the expression for mode C1 in table 2.1:

$$E_g(k) = \frac{(E_s - V_f + E_L(k))/R_w - I_o + \Sigma E_j(k)/N_j R_j}{G + 1/R_w + \Sigma\, 1/N_j^2 R_j} \tag{3.18}$$

Then this expression may be substituted directly into equations 3.14 and 3.16. Equation 3.10 substituted into equation 3.16 yields:

$$R_j I_j(k+1) = E_j(k+1) + E_g(k)/N_j \tag{3.19}$$

into which equation 3.18 may be substituted to yield the last of the set of difference equations for mode sequence II.

3.4 Mode Sequence III.

In this sequence the positive half-cycle of the source is the reset interval, and load current occurs during this interval, as the diode is forward biased (mode C1). During the portion of the negative half-cycle when the flux is changing, the core voltage is sufficient to overcome the source, and load current may flow until the core is saturated negatively and the core voltage collapses, allowing the diode again to be reverse biased. This is the only difference in operation in this sequence from sequence II. However this difference causes the operation in this sequence to be nonlinear, in terms of the terminal difference equations, whereas the difference equations for sequences I

and II are linear.

The nonlinearity arises in the load current flow during the negative half cycle of the source. The average value of the load current in the negative half cycle is dependent on the time when the core saturates, and the nonlinear operation is demonstrated in the expression for the average value of the load current in this half-cycle:

$$R_w I_L(k+1) = \frac{1}{T} \int_{KT}^{kT + \Delta T(k+1)} e_s + e_L - V_f - e_g)dt \qquad (3.20)$$

Where T is the period of one half-cycle of the source frequency, and $\Delta T\ (k+1)$ is the unsaturated time in the gate half-cycle. The wave forms associated with this sequence are shown in figure 3.3.

As the core voltage e_g is zero when the core is saturated, the portion of the integral in equation 3.20 involving e_g yields the half-cycle average of $E_g(k+1)$. However the rest of the integrand does not yield a half-cycle average. Under the assumption that the voltages are constant during a half cycle, the integration may be performed, yielding the result:

$$R_w I_L(k+1) = \lfloor E_s(k+1) + E_L(k+1) - V_f \rfloor \lfloor \Delta T(k+1)/T \rfloor E_g(k+1) \qquad (3.21)$$

The net change of flux for the sequency is zero, and therefore the average core voltage is also zero. This relation may be written:

$$E_g(k) + \frac{1}{T} \int_{kT}^{kT + \Delta T(k+1)} e_{gA1} dt = 0 \qquad (3.22)$$

Where e_{gA1} is the core voltage in mode A1. If the core voltage is constant during the interval, as assumed, then:

$$\frac{1}{T} \int_{kT}^{kT + \Delta T(k+1)} e_{gA1} dt = \frac{\Delta T(k+1)}{T} E_{gA1}(k+1) = -E_g(k) \qquad (3.23)$$

Substituting from equation 3.23 into equation 3.21 the terminal difference equation for the load current in the negative half-cycle is obtained:

$$R_w I_L(k+1) = \left\{ \left[\frac{-E_s + E_L(k+1) - V_f}{E_{gA1}(k+1)} \right] - 1 \right\} \left[E_g(k) \right] \qquad (3.24)$$

The other terminal relations are similar to those found in sequence II:

$$R_w I_L(k) = E_s + E_L(k) - E_g(k) - V_f \qquad (3.25)$$

$$R_j I_j(k) = E_j(k) - E_g(k)/N_j \qquad (3.26)$$

$$R_j I_j(k+1) = E_j(k+1) + E_g(k)/N_j \qquad (3.27)$$

where:

$$E_{gA1}(k+1) = \frac{(-E_s + E_L(k+1) - V_f)/R_w + \Sigma E_j(k+1)/N_j R_j + I_o}{G + 1/R_w + \Sigma\, 1/N_j^2 R_j} \qquad (3.28)$$

and

$$E_g(k) = \frac{(E_s + E_L(k) - V_f)/R_w + \Sigma E_j(k)/N_j R_j - I_o}{G + 1/R_w + \Sigma 1/N_j^2 R_j} \qquad (3.29)$$

3. 5 Mode Sequence IV.

The circuit operation in this sequence is similar to that in sequence I, except that in the negative half-cycle the diode is forward rather than reverse biased. The terminal difference equations for sequence IV are linear, as the load current flows throughout the negative half-cycle. In a similar manner to that in the previous sequences the terminal differnece equations may be obtained:

$$R_w I_L(k) = -E_s + E_L(k) - V_f - E_g(k) \tag{3.30}$$

$$R_w I_L(k+1) = E_s + E_L(k+1) - V_f + E_g(k) \tag{3.31}$$

$$R_j I_j(k) = E_j(k) - E_g(k)/N_j \tag{3.32}$$

$$R_j I_j(k+1) = E_j(k+1) + E_g(k)/N_j \tag{3.33}$$

3.6 Summary:

The terminal difference equations for the sequences considered are linear with the exception of sequence III. The nonlinearity arises from the mode change of the diode during a half-cycle. It may be generally stated that such nonlinear difference equations will arise whenever the diode changes its mode of operation during a half-cycle.

Sequence I is the normal mode of operation of the magnetic amplifier under this type of excitation. In cases where the amplifier is to be operated at cut-off, the most desirable sequence is sequence II. Both sequence II and sequence III exhibit a negative gain, however the difference between the two sequences lies in the forward biasing of the diode during the negative half-cycle in sequence III. The gain is greater in magnitude in sequence III for this reason, causing this mode to be less desirable as a cutoff condition. In general it is undesirable for the diode to be forward biased in the negative half-cycle of the source. Then the sequences of principle interest are I and II. Sequences III and IV are undesirable and are of interest only in avoiding them.

The single core magnetic amplifier is of limited value in practical application, being used in applications where gain is of minor importance. However this circuit is of importance as a building block for multi-core applications.

CHAPTER IV. TWO CORE MAGNETIC AMPLIFIERS

The various connections of two basic self-saturating magnetic amplifiers can be divided into three general classes: (1) half-wave output, polarity-reversible circuits, (2) full-wave output, half-cycle response circuits and (3) full-wave output, high-gain circuits. The first is commonly called "half-wave circuits", the second "voltage reset circuits" and the third "doublet circuits".

The source phasing and diode polarities determine whether a circuit may have outputs in one or both half cycles of the source. Half-cycle response occurs naturally in half-wave circuits, and may be obtained in full-wave circuits by the use of synchronous switching of the control windings. Full-wave circuits without synchronous control switching have longer response times because of feedback. The half wave circuits provide output power during only one half of the source period. This output may be either positive or negative and may be used as a polarity-reversible direct, or a phase-reversible alternating output depending on the application. As the output is controlled only by the average value of the control signal in the reset half-cycle, half-wave circuits may be controlled either by a polarity-reversible direct control, or a phase-reversible alternating control which is synchronized with the gating source.

Full-wave circuits may have either rectified or alternating outputs. As the rectified outputs are unidirectional and the alternating outputs are not phase-reversible these circuits are generally thought of as single ended. However, it is possible by use of differential input windings to obtain both polarity-reversible direct output and

phase-reversible alternating output. Single ended direct controlled circuits have control windings connected such that the direct control signal affects both cores in the same sense, whereas the alternating control has control windings connected such that the source affects the cores oppositely in a given half-cycle. The normal direct control circuit acts as a differential alternating control, and the normal alternating control as a differential direct control.

4.1. Topology of Output Circuits.

A pair of windings may be connected in four basic ways: series (aiding or differential), and parallel (aiding or differential). As the diode forward direction has been used to define the dot on the gate winding, the diode and gate winding are to be considered invariant in their relation. That is, if the diode were reversed it would automatically redefine the position of the dot for the core. This is shown in figure 4.1. Then two cores have only four possible orientations, and these may be symbolized using only the associated gate diodes as shown in figure 4.2.

By definition the self-saturating magnetic amplifier must have the topological property that when the core is in its gating half cycle the source must be in series with the core and the load, and when it is in its reset half cycle the source must tend to block the gate diode. It is first assumed that each diode of figure 4.2 represents a source and a core in series with a diode.

The series aiding connection of figure 4.2a can be seen to be relatively useless unless the two sources are in phase. However the output is then unidirectional and occurs only during the positive half cycle of the sources. This circuit has no advantage over a single core

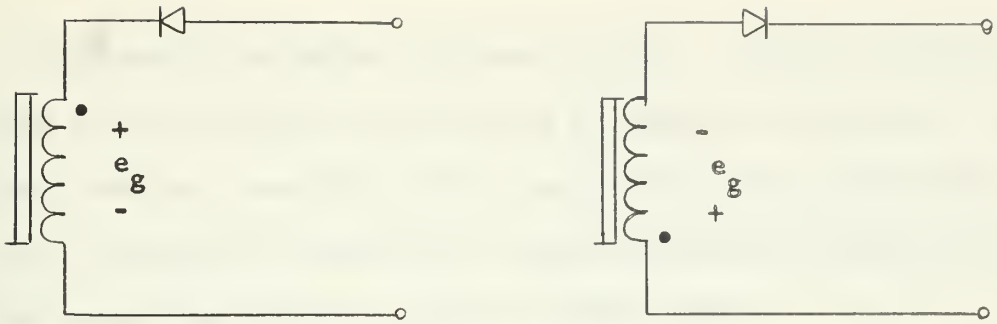
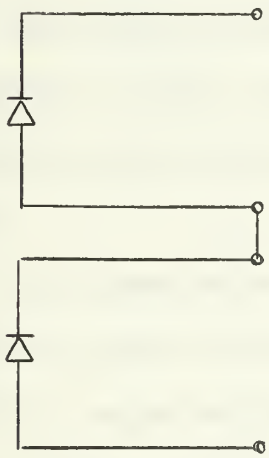
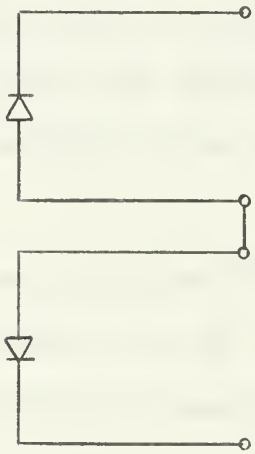


Figure 4.1. Gate Diode - Winding Polarity Convention.



(a)



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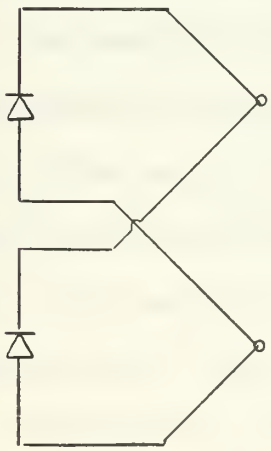

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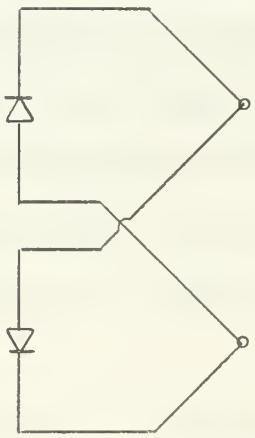


(d)

Figure 4.2 Basic Single Output Winding Connections:
(a) series (b) series-differential (c) parallel (d) parallel - differential

circuit and is therefore considered trivial. If some provision is made so that the cores can be gated in opposite half-cycles, a current path provided, then this circuit can provide a full-wave output. This can be realized by inserting a terminal between the diodes, and providing commutating diodes as shown in figure 4.3a.

It is to be noted that the commutating diodes must oppose the gate diodes in each gate loop circuit. A reordering of elements in the lower circuit allows the use of a single source to gate both cores as shown in figure 4.3b. The diodes which have been shaded indicate the load current path for the half cycle indicated by the source polarity.

The insertion of commutating diodes for the series differential circuit fails to allow a current path. However if in the place of diodes a mixingresistor is placed in each circuit a useable, but somewhat inefficient circuit is obtained which may be operated either as a half wave or full wave amplifier as shown in figure 4.4. Figure 4.4a shows the half wave and 4.4b the full wave connections.

The parallel additive connections of figure 4.2c provide useful connections for out of phase voltages. With voltages in phase no differentiation can be made at the output terminals as to which core has saturated and there is no advantage over a single core circuit. The case with voltages in phase results in a full wave circuit with rectified output as shown in figure 4.5.

The parallel differential output connection of figure 4.2d may be used with sources in phase or out of phase. With sources out of phase a full wave alternating output is obtained (figure 4.6a) and for in phase sources a half wave circuit is obtained as in figure 4.6b.

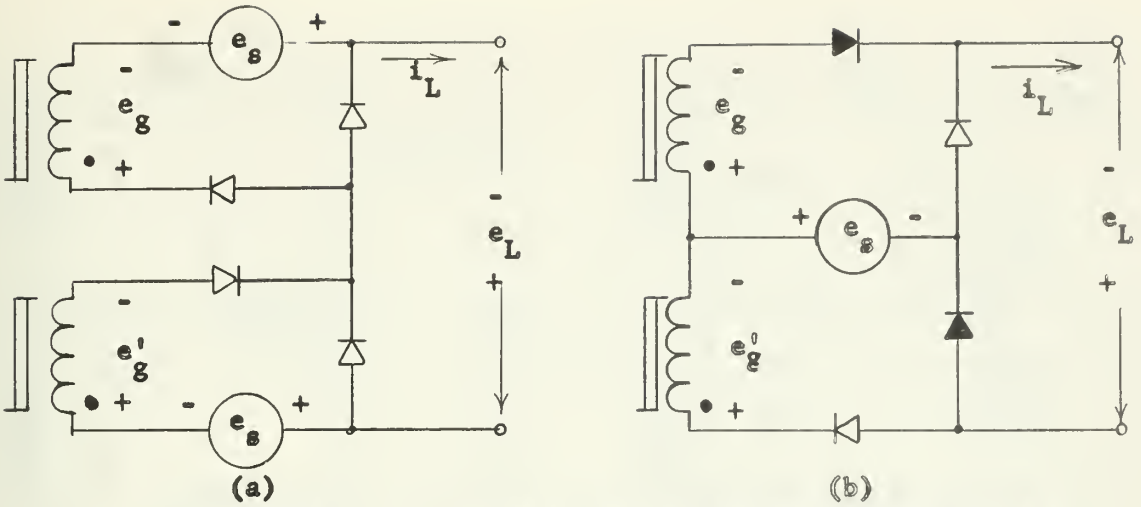


Figure 4.3. Series Output with Commutating Diodes.

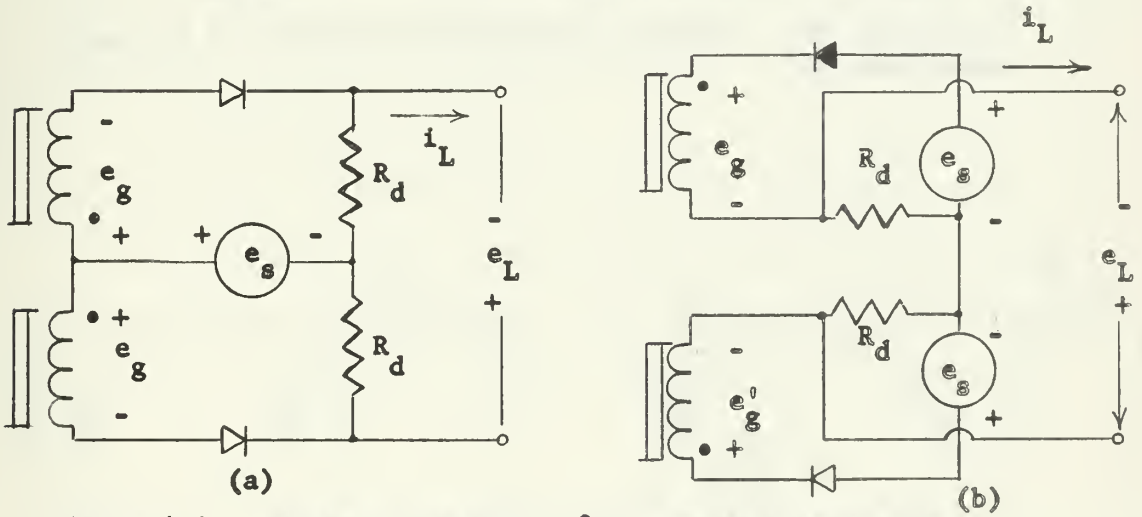


Figure 4.4. Series-differential Outputs: (a) half-wave
(b) full-wave.

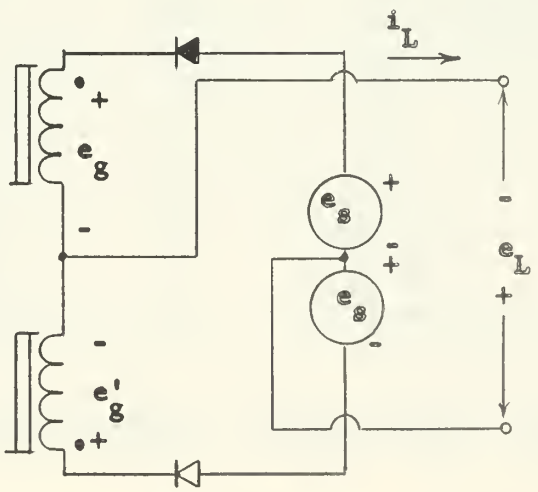


Figure 4.5. Parallel Output

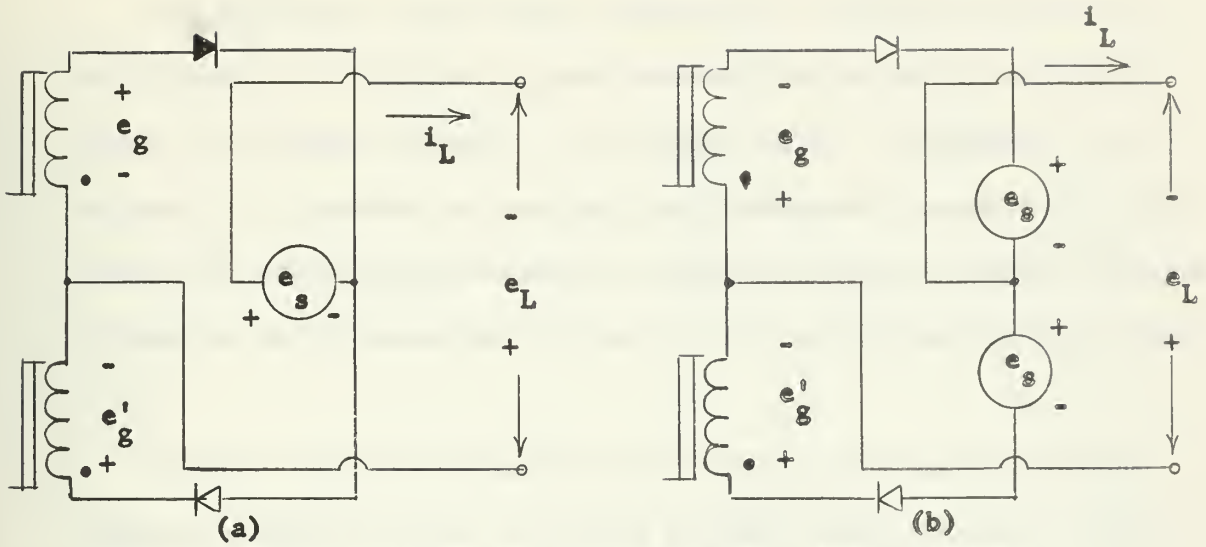


Figure 4.6. Parallel-differential Outputs: (a) full-wave, (b) half-wave.

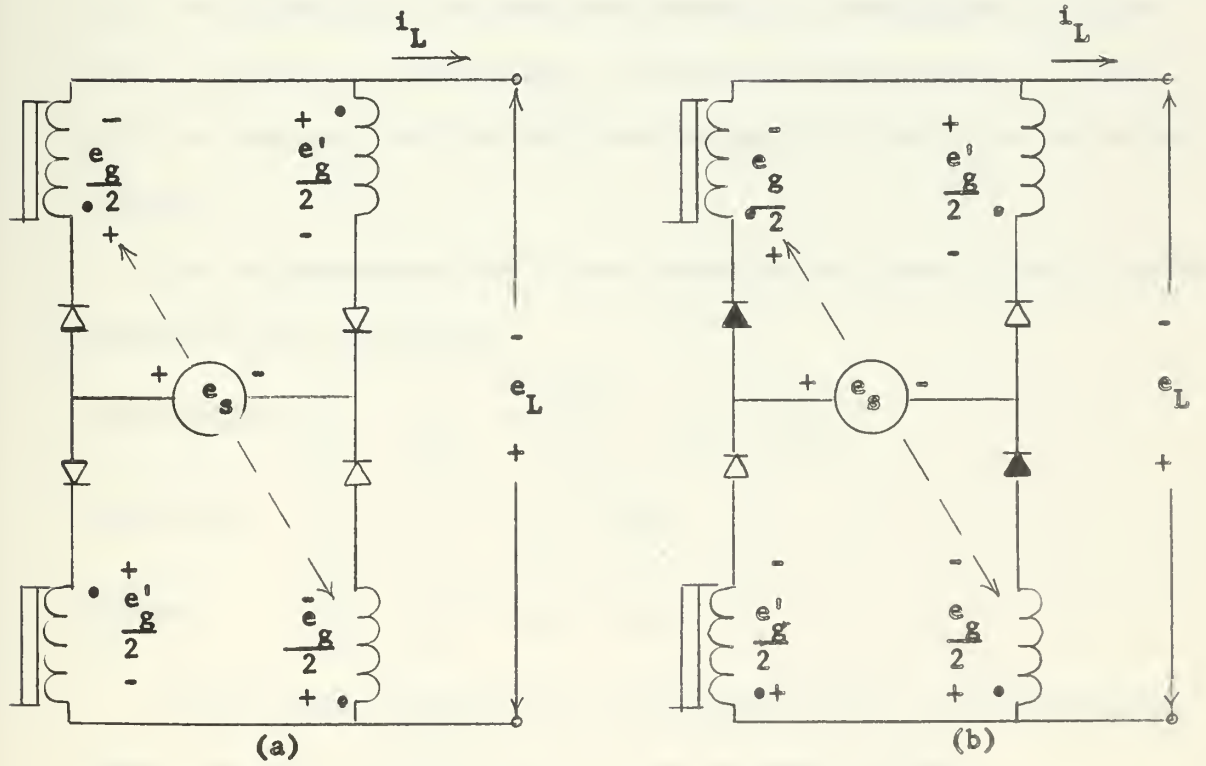


Figure 4.7 Two-core Bridges: (a) half wave (b) full wave

In addition to these basic connections a bridge connection can be obtained by splitting the gate windings, and adding an additional diode to each gate circuit. As a single source is necessary in the bridge it is possible to have only two fundamental connections, with either the cores gating together as shown in figure 4.7a (the half-wave bridge), or in alternate half-cycles as in the full-wave bridge (figure 4.7b).

Then it has been determined that for two core self-saturating magnetic amplifiers there are eight possible output circuits, three half wave and five full wave circuits.

4.2. Half-Wave Output Circuits.

The three half wave output circuits are shown together in figure 4.8. For convenience the series-differential arrangement of figure 4.4a is called the semi-bridge, the parallel-differential of figure 4.6b the centertap and the half-wave bridge of figure 4.7a the bridge circuit.

The instantaneous output loop relations for these circuits during the output half-cycle are:

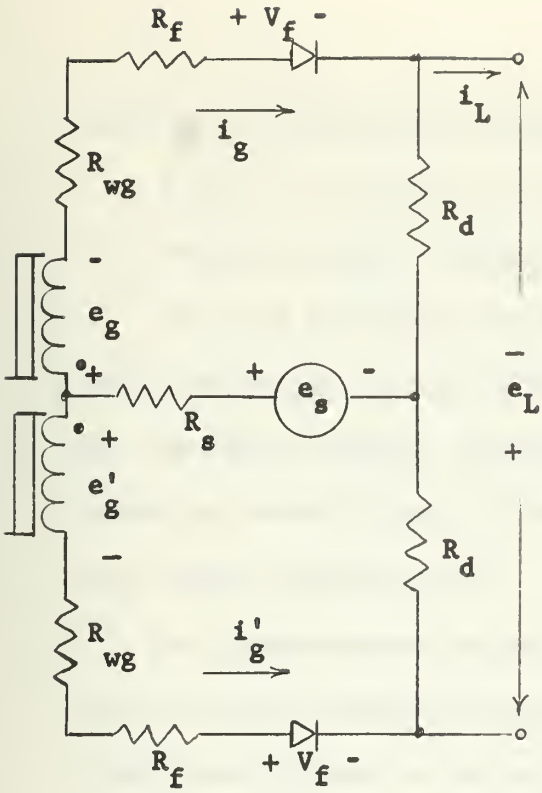
semi-bridge: $e_g - e'_g = \frac{R_D + R_w}{R_D} e_L - 2 R_w i_L$

centertap: $e_g - e'_g = 2 e_L - R_w i_L$

Bridge: $e_g - e'_g = 2 e_L - R_w i_L$

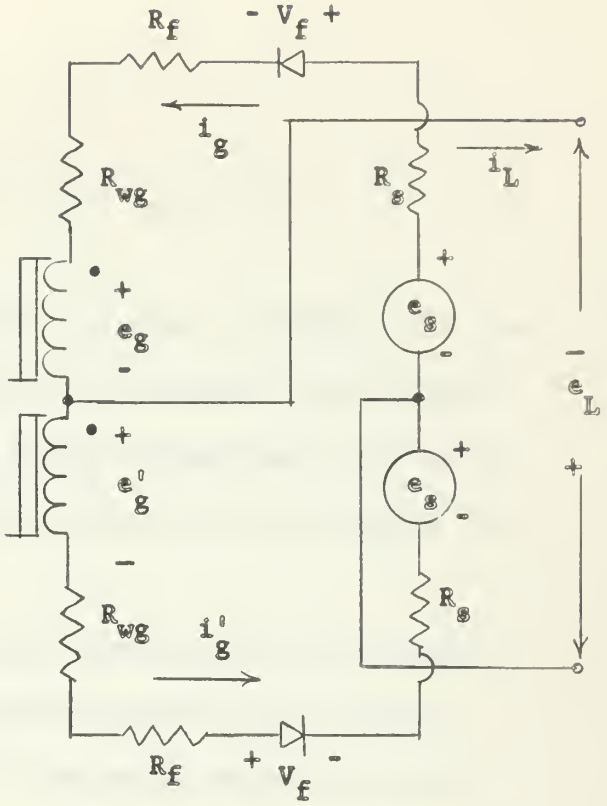
If the output half-cycle is called the $(n+1)^{st}$, then averaging these over the output half-cycle, for the semi bridge:

$$E_g(n+1) - E'_g(n+1) = \frac{R_d + R_w}{R_d} E_L(n+1) - 2R_w I_L(n+1) \qquad 4.1$$



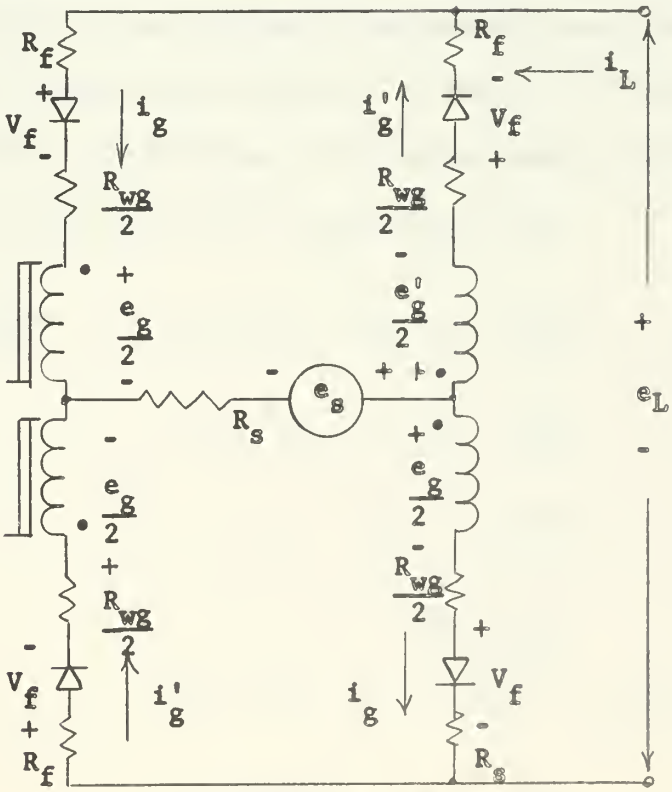
(a) Semi-bridge

$R_w = R_{wg} + R_f$



(b) Center tap

$R_w = R_s + R_{wg} + R_f$



(c) Bridge: $R_w = R_{wg} + 2R_f$

Figure 4.8. Half-wave Output Circuits.

and for the centertap or bridge:

$$E_g(n+1) - E_g'(n+1) = 2E_L(n+1) - R_w I_L(n+1) \qquad 4.2$$

4.3 Full-wave Output Circuits.

The five full-wave output circuits are shown in figure 4.9. The rectified output circuits from figures 4.3, 4.5 and 4.7b are called the incomplete bridge, centertap and bridge respectively, and the alternating output circuits from figures 4.6a and 4.4b the doubler and semi-bridge respectively.

The instantaneous outputs of these circuits, under the assumption that the resetting core's gate diode remains in the reverse biased state, depend on the polarity of the power source or sources. If it is assumed that the n^{th} half-cycle corresponds to the instantaneous directions of the sources as shown in figure 4.9, then core-one is gated in the n^{th} half-cycle, providing the output power in that half-cycle, while the gate diodes of the primed core (core-2) prevent current flow in their gate windings. In the $n+1^{st}$ half-cycle the roles of the cores are reversed. The instantaneous output circuit relations are found for the n^{th} half-cycle to be:

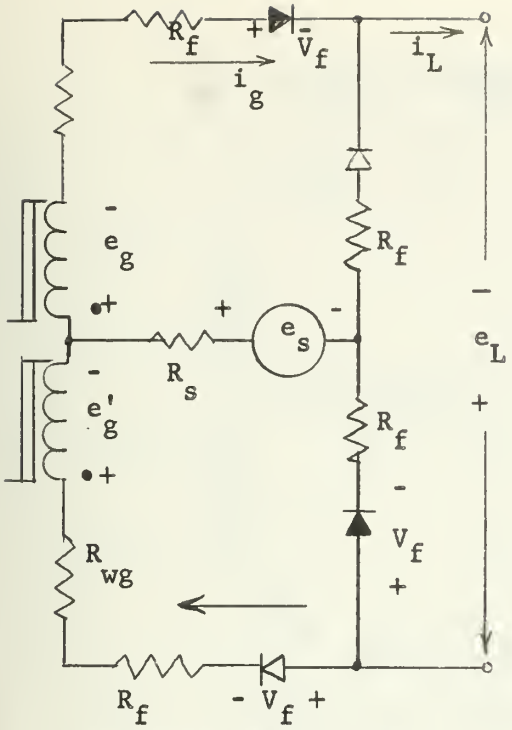
incomplete bridge: $e_g = e_s - 2V_f + e_L - R_w i_L$

centertap: $e_g = e_s - V_f + e_L - R_w i_L$

bridge: $e_g = e_s - 2V_f + e_L - R_w i_L$

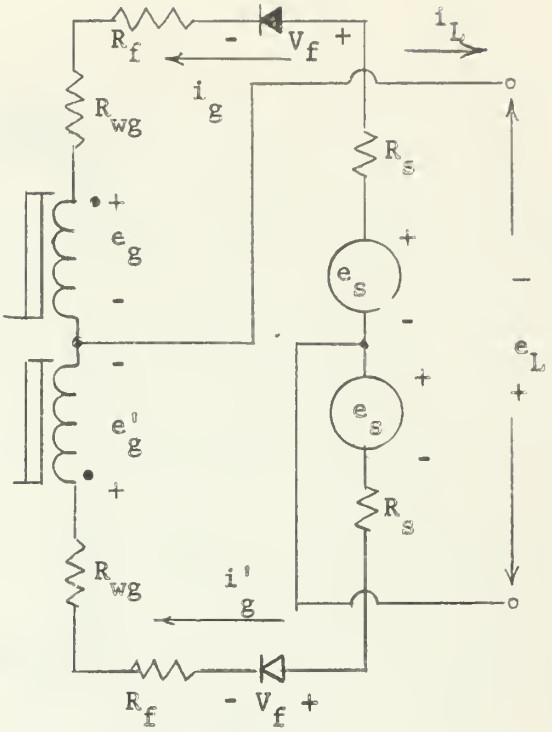
doubler: $e_g = e_s - V_f + e_L - R_w i_L$

semi-bridge: $e_g = e_s - V_f + \frac{R_w + R_d}{R_d} e_L - (2R_w + R_d) i_L$



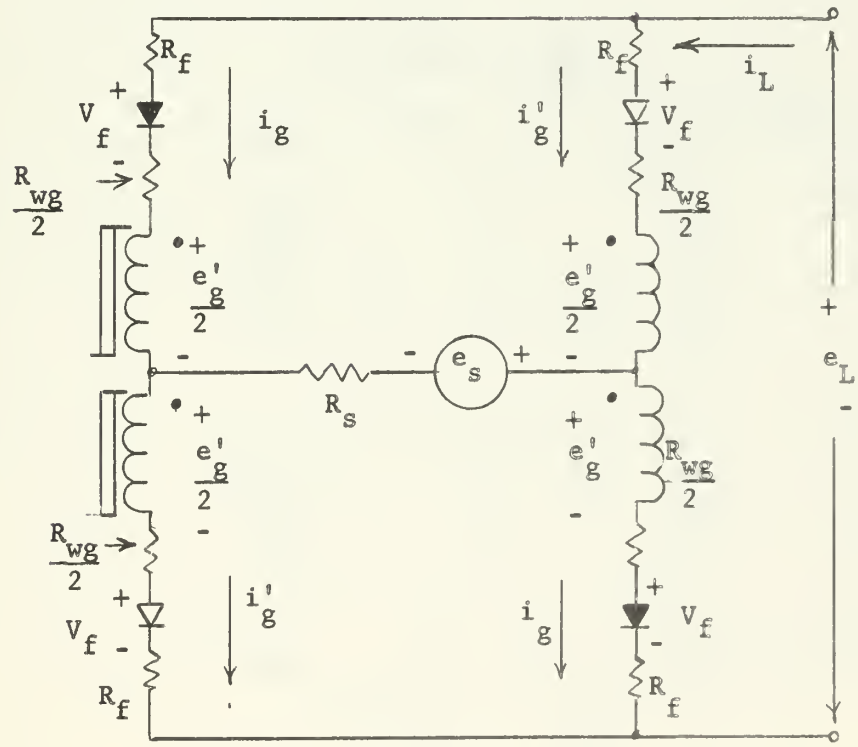
(a) Incomplete Bridge

$R_w = R_{wg} + R_s + 2R_f$



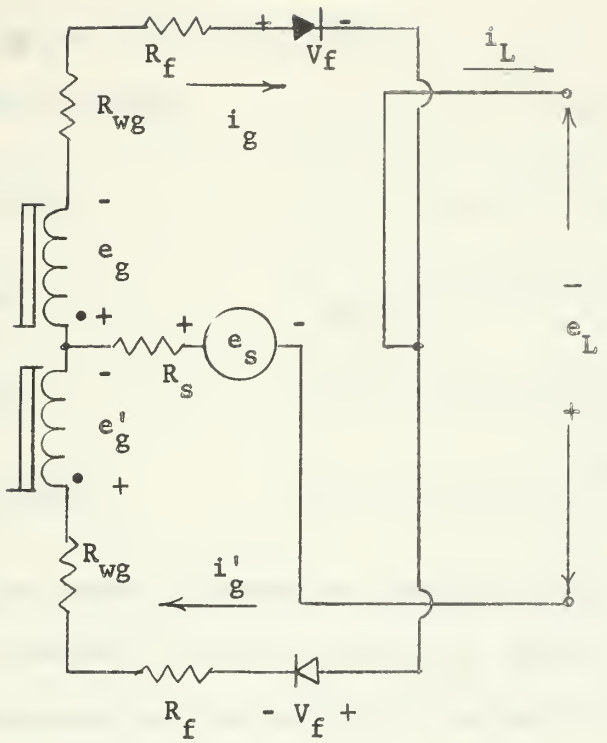
(b) Center tap

$R_w = R_{wg} + R_s + R_f$

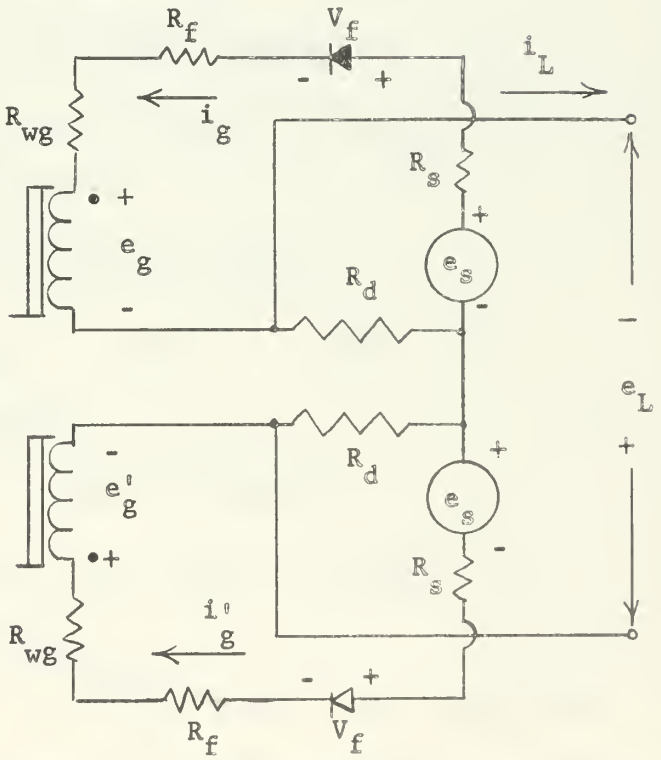


(c) Bridge $R_w = R_{wg} + R_s + 2R_f$

Figure 4.9. Full-wave Output Circuits. (a) (b) & (c) unidirectional (c) & (d) alternating



(d) Doubler: $R_w = R_{wg} + R_f + R_s$



(e) Semi-bridge (a.c. centertap) $R_w = R_{wg} + R_s + R_f$

Figure 4.9 Continued.

In the $n + 1^{st}$ half-cycle:

incomplete bridge: $e_g' = - e_s - 2V_f + e_L - R_w' i_L$

centertap: $e_g' = - e_s - V_f + e_L - R_w' i_L$

bridge: $e_g' = - e_s - V_f + e_L - R_w' i_L$

doubler: $e_g' = - e_s - V_f - e_L + R_w' i_L$

semi-bridge: $e_g' = - e_s - V_f - \frac{R_w' + R_d}{R_d} e_L + (2R_w' + R_d) i_L$

The source voltages are negative in the $n + 1^{st}$ half-cycle and V_f' is assumed to be the same as V_f, and R_f' the same as R_f. Then the relations for the half-cycle averages for the output circuits are found to be:

incomplete bridge and bridge:

$$E_g(n) = E_s - 2 V_f + E_L(n) - R_w I_L(n) \qquad 4.3$$

$$E_g'(n + 1) = E_s - 2 V_f + E_L(n + 1) - R_w I_L(n + 1) \qquad 4.4$$

for the centertap circuit:

$$E_g(n) = E_s - V_f + E_L(n) - R_w I_L(n) \qquad 4.5$$

$$E_g'(n + 1) = E_s - V_f + E_L(n + 1) - R_w I_L(n + 1) \qquad 4.6$$

for the doubler circuit:

$$E_g(n) = E_s - V_f + E_L(n) - R_w I_L(n) \qquad 4.7$$

$$E_g'(n + 1) = E_s - V_f - E_L(n + 1) + R_w I_L(n + 1) \qquad 4.8$$

and for the semi-bridge:

$$E_g(n) = E_s - V_f + \frac{R_w + R_d}{R_d} E_L(n) - (2R_w + R_d) I_L(n) \qquad 4.9$$

$$E_g'(n + 1) = E_s - V_f - \frac{R_w + R_d}{R_d} E_L(n + 1) + (2R_w + R_d) I_L(n + 1) \qquad 4.10$$

These may all be placed in the same form, by defining new parameters which differ from circuit to circuit:

$$E_{sd} = \begin{cases} E_s - 2V_f & \text{incomplete bridge and bridge} \\ E_s - V_f & \text{centertap, doubler and semi-bridge} \end{cases}$$

$$R'_s = \begin{cases} R_w & \text{all but semi-bridge} \\ 2R_w + R_d & \text{for semi-bridge} \end{cases}$$

$$K_d = \begin{cases} 1 & \text{all but semi-bridge} \\ (R_w + R_d)/R_d & \text{for semi-bridge} \end{cases}$$

and if the half-cycle average values of the output quantities e_L and i_L are taken to mean their magnitudes, then all the relations may be described by the relations:

$$E_g(n) = E_{sd} + K_d E_L(n) - R'_s I_L(n) \qquad 4.11$$

$$E'_g(n+1) = E_{sd} + K_d E_L(n+1) - R'_s I_L(n+1) \qquad 4.12$$

Then the full wave output circuits are described by these two equations under the restriction that the gate diodes remain reverse biased in the reset half-cycle, and forward biased in the gate half-cycle.

4.4 Control Circuits.

Besides the four basic connections of two coils shown in figure 4.10 a,b,c and d, there are two circuits which allow an isolation of the control windings by commutating. The commutating arrangements are used in full-wave output amplifiers to decouple the input and output circuits completely and thereby retain the half-cycle

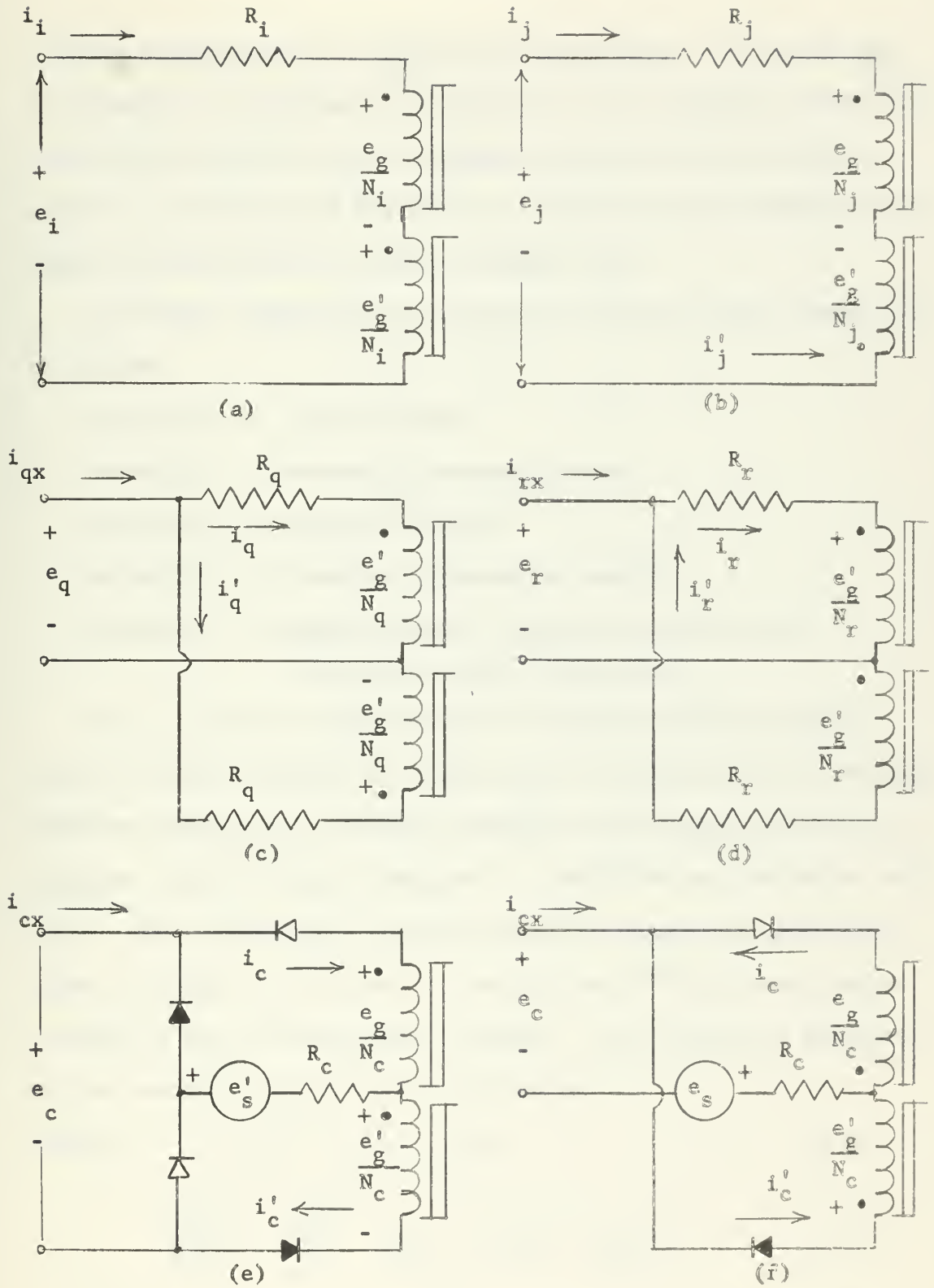


Figure 4.10: Two core Control Circuits: (a) Series, (b) Series-differential, (c) Parallel, (d) Parallel-differential, (e) Commutated, (f) Commutated-differential

response characteristic of single core amplifiers. The commutating arrangements are topologically identical to the incomplete bridge and doubler output circuits, and therefore are not the only possible methods of obtaining the commutation. The six control configurations which were considered are shown in figure 4.10.

Subscripts differentiate between the various control connections as follows:

subscript i: series control

subscript j: series-differential control

subscript q: parallel control

subscript r: parallel-differential control

subscript c: general control subscript used for both commutated control connections

The six control configurations of figure 4.10 were analyzed and the results averaged for a half-cycle yielding half-cycle average relations between the terminal quantities and the core voltages and currents. The half-cycle indicator k indicates any particular half-cycle. The instantaneous polarities for the commutated connections shown in figures 4.10 e and f are for the n^{th} half cycle similar to those of the full-wave output circuits. The half-cycle relations for the control circuits are the following:

Series:
$$I_{ix}(k) = I_i(k) = I_i'(k) \qquad 4.13$$

$$\frac{E_{ix}(k)}{N_i R_i} = \frac{I_{ix}(k)}{N_i} + \frac{1}{N_i^2 R_i}\left[\bar{E}_g(k) + E_g'(k)\right] \qquad 4.14$$

series-differential: $$I_{jx}(k) = I_j(k) = -I'_j(k) \qquad 4.15$$

$$\frac{E_{jx}(k)}{N_j R_j} = \frac{I_{xj}(k)}{N_j R_j} + \frac{1}{N_j^2 R_j}\left[E_g(k) - E'_g(k)\right] \qquad 4.16$$

Parallel: $$I_{qx}(k) = I_q(k) + I'_q(k) \qquad 4.17$$

$$\frac{E_{qx}(k)}{N_q R_q} = \frac{I_q(k)}{N_q} + \frac{1}{N_q^2 R_q} E_g(k) \qquad 4.18$$

$$\frac{E_{qx}(k)}{N_q R_q} = \frac{I'_q(k)}{N_q} + \frac{1}{N_q^2 R_q} E'_g(k) \qquad 4.19$$

Parallel-differential: $$I_{rx}(k) = I_r(k) - I'_r(k) \qquad 4.20$$

$$\frac{E_{rx}(k)}{N_r R_r} = \frac{I_r(k)}{N_r} + \frac{1}{N_r^2 R_r} E_g(k) \qquad 4.21$$

$$\frac{-E_{rx}(k)}{N_r R_r} = \frac{I'_r(k)}{N_r} + \frac{1}{N_r^2 R_r} E'_g(k) \qquad 4.22$$

Commutated: $$\frac{E_c(n) - E'_s(n) + 2V_{fc}}{N_c R_c} = \frac{I'_c(n)}{N_c} + \frac{1}{N_c^2 R_c} E'_g(n) \qquad 4.23$$

$$\frac{E_c(n+1) + E'_s(n+1) + 2V_{fc}}{N_c R_c} = \frac{I_c(n+1)}{N_c} + \frac{1}{N_c^2 R_c} E_g(n+1) \qquad 4.24$$

Commutated-differential:

$$\frac{E_c(n) - E'_s(n) + V_{fc}}{N_c R_c} = \frac{I'_c(n)}{N_c} + \frac{1}{N_i^2 R_i} E'_g(n) \qquad 4.25$$

$$\frac{-E_c(n+1) + E'_s(n+1) + V_{fc}}{N_c R_c} = \frac{I_c(n+1)}{N_c} + \frac{1}{N_c^2 R_c} E_g(n+1) \qquad 4.26$$

4.5 Summary.

Of the eight possible single gate winding output connections of two basic magnetic amplifiers six are found to be useful. Two of these require mixing circuits. The half-wave differential output requires resistive mixing but the full-wave semi-bridge may use transformer mixing. These six useful single gate winding output circuits together with the two bridge connections give three half wave and five full wave output connections.

The four basic control connections provide the possible connections for a pair of control windings for the half-wave and full-wave high gain amplifiers. The two commutating connections provide a method of retaining half-cycle response with a full-wave output, and may be used with any of the full-wave output circuits.

The half-wave circuits, being perhaps the simplest to visualize in their operation, are considered first in chapter five. The full-wave circuits are considered in the following two chapters.

CHAPTER V. TWO CORE HALF-WAVE CIRCUITS

The three half-wave circuits of figure 4.8 have similar operations as is indicated by the output-core relations 4.1 and 4.2. These relations may be put into a common form so that the analysis may be carried out on all three simultaneously. Both of these expressions may be written:

$$K_d E_L(n+1) - R_s^{\circ} I_L(n+1) = E_g(n+1) - E_g^{\circ}(n+1) \qquad 5.1$$

$$K_d = \begin{cases} 1 + R_W/R_d & \text{for the semi-bridge} \\ 2 & \text{for the centertap and bridge} \end{cases}$$

$$R_s^{\circ} = \begin{cases} 2R_W & \text{for the semi-bridge} \\ R_W & \text{for centertap and bridge} \end{cases}$$

In general it is necessary to use a bias with these circuits to allow the most linear operation and the greatest efficiency. The bias must be applied in such a way as to affect both cores in the same sense. This bias must then be applied by either the series or the parallel control connection and must be in the proper sense to reset the cores during the negative half-cycle of the power source, the n^{th} half-cycle.

The half-wave circuits constitute a class of differential amplifiers as their outputs are dependent on the difference of the core voltages. In order to obtain any control it is necessary that the inputs affect the cores in opposite senses. For this reason the only control configurations which are of value are the differential-controls. As both cores are gated in the same half cycle it is necessary that

the control accomplish any reset on both cores in the same half-cycle, which rules out the commutated-control configurations. Then the only useful control connections are the series-differential and parallel-differential connections.

The inputs may be either polarity-reversible direct control or phase-reversible alternating control. The major effect of the control occurs in the reset or n^{th} half cycle, so that the polarity of the output is dependent on the polarity of the input in this half cycle.

The output of these amplifiers is half-wave, limited to the gate half-cycle. This output may be considered to be either a polarity-reversible direct output or a phase-reversible alternating output.

There are three combinations of linear mode sequences which are of interest: where both cores are operated in mode sequence I; one core saturated and the other operated in mode sequence II; and one core in sequence I while the other is in sequence II.

The normal bias condition for the core where both cores are operated in sequence I is such that the cores both saturate at about the middle of the gate half-cycle in the absence of control. Then the differential action of the control, when applied, tends to cause one core to saturate earlier and the second later. This gives rise to an output wave form that is more or less symmetrical about the bias point. This operation is appropriate for alternating outputs where the phase relation is required to be constant.

With both cores in sequence I the operation is similar to an electronic push-pull amplifier in class A operation with the resulting higher gain (than class B) but also with the lower efficiency associated with class A operation.

Operation with one core in sequence I and the other in sequence II occurs normally with the bias adjusted so that both cores reach saturation at the end of the gate half-cycle when the control inputs are zero. The resulting output waveform is not symmetrical and the phase shift of the fundamental component of the output is dependent on the amplitude. For this reason the output is not well suited to alternating outputs. The operation in this case is similar to class B operation of electronic amplifiers. The efficiency is higher, but the gain is lower than that of the case where both cores are operated in sequence I.

Operation with one core saturated and the other in sequence II corresponds to saturation for either of the other two types of operation.

The general case of this type of amplifier may be represented by equation 5.1 for the output circuits, and has an arbitrary number of control windings of the series-differential and parallel-differential types as well as a bias winding. The bias may be either alternating or direct and may be applied by either a series or a parallel connection. The general expressions must therefore include the possibility of either type of bias and an arbitrary number of control windings.

5.1 Operation with Both Cores in Sequency I.

With both cores operating in this sequence both are gated to saturation in the $(n+1)^{st}$ half-cycle, and are reset in the n^{th}. The reset is assumed to occur over the whole n^{th} half-cycle, so that the instantaneous equations for the core correspond to those of mode A2 as given by equation 2.13 when the gate loop current is zero.

$$\sum \frac{I(n)}{N} = - I_o + GE_g(n) \qquad 5.2$$

$$\sum \frac{I'(r)}{N} = -I_o + GE'_g(n) \qquad 5.3$$

Neither core saturates in the n^{th} half-cycle, both saturate in the $n+1^{st}$ half-cycle. Then the average values of both core voltages are zero for the cycle:

$$E_g(n) + E_g(n+1) = 0 \qquad 5.4$$

$$E'_g(n) + E'_g(n+1) = 0 \qquad 5.5$$

To account for a possible series bias the current in such a loop is found from equations 4.13 and 4.14 to be represented by:

$$\frac{I_{bi}(n)}{N_i} = \frac{I'_{bi}(n)}{N_i} = \frac{E_{bi}(n)}{N_i R_i} - \frac{1}{N_i^2 R_i} \left[E_g(n) + E'_g(n) \right] \qquad 5.6$$

For the possibility of a parallel bias from equations 4.20, 4.21 and 4.22 the currents for this type of loop are:

$$\frac{I_q(n)}{N_q} = \frac{I_{bq}(n)}{2N_q} - \frac{1}{2N_q^2 R_q} \left[E_g(n) - E'_g(n) \right] \qquad 5.7$$

$$\frac{I'_q(n)}{N_q} = \frac{I_{bq}(n)}{2N_q} + \frac{1}{2N_q^2 R_q}\left[E_g(n) - E'_g(n)\right] \qquad 5.8$$

For an arbitrary number of series-differential control circuits, the sum of such currents is found from equation 4.15 and 4.16 to be:

$$\sum \frac{I_j(n)}{N_j R_j} = -\sum \frac{I'_j(n)}{N_j R_j} = \sum \frac{E_j(n)}{N_j R_j} - \sum \frac{1}{N_j^2 R_j}\left[E_g(n) - E'_g(n)\right] \qquad 5.9$$

And for an arbitrary number of parallel-differential control circuits, from equations 4.20, 4.21 and 4.22 the control currents are given by:

$$\sum \frac{I_r(n)}{N_r} = \sum \frac{I_{rx}(n)}{2N_r} - \sum \frac{1}{2N_r^2 R_r}\left[E_g(n) + E'_g(n)\right] \qquad 5.10$$

$$\sum \frac{I'_r(n)}{N_r} = -\sum \frac{I_{rx}(n)}{2N_r} - \sum \frac{1}{2N_r^2 R_r}\left[E_g(n) + E'_g(n)\right] \qquad 5.11$$

Eliminating the control currents from the above current relations and the two core-function equations 5.2 and 5.3 the core voltages are found for the n^{th} half-cycle to be:

$$E_g(n) = \frac{\dfrac{E_{bi}(n)}{N_i R_i} + \dfrac{I_{bq}(n)}{2N_q} + I_o}{G + \dfrac{2}{N_i^2 R_i} + \sum \dfrac{1}{N_r^2 R_r}} + \frac{\sum \dfrac{E_j(n)}{N_j R_j} + \sum \dfrac{I_{rx}(n)}{2N_r}}{G + \dfrac{1}{N_q^2 R_q} + \sum \dfrac{2}{N_j^2 R_j}} \qquad 5.12$$

$$E'_g(n) = \frac{\dfrac{E_{bi}(n)}{N_i R_i} + \dfrac{I_{bq}(n)}{2N_q} + I_o}{G + \dfrac{2}{N_i^2 R_i} + \sum \dfrac{1}{N_r^2 R_r}} - \frac{\sum \dfrac{E_j(n)}{N_j R_j} + \sum \dfrac{I_{rx}(n)}{2N_r}}{G + \dfrac{1}{N_q^2 R_q} + \sum \dfrac{2}{N_j^2 R_j}} \qquad 5.13$$

The output in the $(n+1)^{st}$ half-cycle is obtained by substracting the above two equations, finding the difference of the two voltages for the n^{th} half-cycle and using the relations 5.2 and 5.3.

$$R_s' I_L(n+1) - K_d E_L(n+1) = \frac{\sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r}}{G/2 + \frac{1}{2N_q^2 R_q} + \sum \frac{1}{N_j^2 R_j}} \qquad 5.14$$

The relations between the control currents are found from the input terminal relations and the core relations. from equation 5.9.

$$N_j \left[E_j(n) - R_j I_j(n) \right] = E_g(n) - E_g'(n) \qquad 5.15$$

and for the following half-cycle:

$$N_j \left[E_j(n+1) - R_j I_j(n+1) \right] = E_g(n+1) - E_g'(n+1) \qquad 5.16$$

From equations 5.12 and 5.13:

$$N_j \left[E_j(n) - R_j I_j(n) \right] = \frac{\sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r}}{G/2 + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q}} \qquad 5.17$$

and for the $(n+1)^{st}$ half-cycle:

$$E_j(n+1) - R_j I_j(n+1) = - \left[E_j(n) - R_j I_j(n) \right] \qquad 5.18$$

The parallel differential control relations are found from equations 4.20, 4.21 and 4.22.

$$N_r \left[2E_r(k) - R_r I_{rx}(k) \right] = E_g(k) - E_g(k) \qquad 5.19$$

Then similarly to the above:

$$N_r\left[2E_r(n) - R_rI_{rx}(n)\right] = \frac{\sum\frac{E_j(n)}{N_jR_j} + \sum\frac{I_{rx}(n)}{2N_r}}{G/2 + \sum\frac{1}{N_j^2R_j} + \sum\frac{1}{2N_q^2R_q}} \qquad 5.20$$

and

$$2E_r(n+1) - R_rI_{rx}(n+1) = -\left[2E_r(n) - R_rI_{rx}(n)\right] \qquad 5.21$$

The relations 5.14, 5.17, 5.18, 5.20 and 5.21 are sufficiently general to determine relative gains, as well as the input impedances for each variation of the half-wave output circuits. Equation 5.14 indicates the gain is dependent on the resistances of the series-differential control and the parallel bias. If the bias is restricted to the series circuit then the higher gain may be realized. This is accounted for in the previous expressions by letting N_q become infinite.

The commonly used connection for control is the series-differential connection. For a single control with series bias the output relation becomes:

$$R_s'I_L(n+1) - K_dE_L(n+1) = \frac{N_jE_j(n)}{1 + \frac{GN_j^2R_j}{2}} \qquad 5.22$$

The control current in the n^{th} half-cycle is:

$$R_jI_j(n) = \frac{GN_j^2R_j}{2+GN_j^2R_j}E_j(n) \qquad 5.23$$

The control current in the gate half-cycle is

$$R_jI_j(n+1) = E_j(n+1) + \frac{2}{2+GN_j^2R_j}E_j(n) \qquad 5.24$$

The average control currents for the two half cycles for direct control then is

$$R_j I_j = \frac{1}{2}\left[E_j(n+1) + \frac{2+GN_j^2R_j}{2+GN_j^2R_j} E_j(n)\right] = E_j \qquad 5.25$$

The average resistance of the control circuit is then seen to be simply the control resistance for direct control. Assuming that the input power for any half-cycle may be represented by the product of the average input current and voltage, the input power in the n^{th} half-cycle is:

$$P_j(n) = \frac{E_j^2(n)}{R_j}\left[\frac{GN_j^2R_j}{2+GN_j^2R_j}\right] \qquad 5.26$$

For the $(n+1)^{st}$ half cycle:

$$P_j(n+1) = \frac{E_j^2(n+1)}{R_j} + \frac{2}{2+GN_j^2R_j} E_j(n)E_j(n+1) \qquad 5.27$$

For direct control in steady state $E_g(n+1) = E_j(n)$ and the average power for the cycle is:

$$P_{jdc} = \frac{1}{2}\left[P_j(n)+P_j(n+1)\right] = \frac{E_j^2}{R_j} \qquad 5.28$$

Which indicates that the input impedance in steady state may be truly assumed to be merely the control resistance for direct control.

With alternating control $E_j(n+1) = -E_j(n)$ and the average power input is thereby:

$$P_{jac} = \frac{1}{2}\left[P_j(n) + P_j(n+1)\right] = \frac{E_j^2}{R_j}\quad\frac{2GN_j^2R_j}{2+GN_j^2R_j} \qquad 5.29$$

Then the effective input impedance for alternating control is

$$Z_{jac} = R_j \left[\frac{1}{2} + \frac{1}{GN_j^2 R_j} \right] \qquad 5.30$$

which may be less or greater than the direct controlled case depending on the magnitude of N_j and G. In general $GN_j^2R_j$ is less than one at power frequencies so that the input power requirements are generally less for the alternating control than for direct control.

For a purely resistive load the output current may be written:

$$R_o I_L(n+1) = \frac{N_j E_j(n)}{1+\frac{1}{2}GN_j^2R_j} \qquad 5.31$$

where $R_o = R_s' + K_d R_L$

The output power is then:

$$P_L = \frac{1}{2} P_L(n+1) = \frac{1}{2} \frac{R_L}{R_o^2} \left[\frac{N_j E_j(n)}{1+\frac{1}{2}GN_j^2R_j} \right]^2 \qquad 5.32$$

The power gairs which may be expected for the series-differential control with series bias are then:

$$K_{pjdc} = \frac{P_L}{P_{jdc}} = \frac{2N_j^2R_j}{(2+GN_j^2R_j)^2} \frac{R_L}{R_o^2} \qquad 5.33$$

$$K_{pjac} = \frac{P_L}{P_{jac}} = \frac{1}{G(2+GN_j^2R_j)} \frac{R_L}{R_o^2} \qquad 5.34$$

Expression 5.33 is maximum with respect to control resistance when $GN_j^2R_j$ is 2. In this condition the two expressions

for the power gain are equal and are given by:

$$K_{pjdc}\Big|_{max.} = \frac{1}{4G}\frac{R_L}{R_o^2}$$

The maximization of power gain for the alternating control case occurs where $GN_j^2R_j$ is negligibly small with respect to 2, and is twice the value given by equation 5.35.

It is noted that the expression for output in equation 5.14 may be made some sort of maximum for parallel-differential control when there are no series-differential or parallel control windings:

$$R_s'I_L(n+1) - K_dE_L(n+1) = \sum \frac{I_{rx}(n)}{G\,N_r} \qquad 5.36$$

under this condition, with a single control winding of the parallel-differential type and series bias, the input voltages from equations 5.20 and 5.21 are:

$$E_r(n) = \frac{R_r}{2}\left[1 + \frac{1}{GN_r^2R_r}\right] I_{rx}(n) \qquad 5.37$$

$$E_r(n+1) = \frac{R_r}{2} I_{rx}(n+1) - \frac{1}{2N_r^2G} I_{rx}(n) \qquad 5.38$$

The associated powers are:

$$P_r(n) = \frac{R_r}{2}\left[1 + \frac{1}{GN_r^2R_r}\right] I_{rx}^2(n) \qquad 5.39$$

$$P_r(n+1) = \frac{R_r}{2} I_{rx}^2(n+1) - \frac{1}{2N_r^2G} I_{rx}(n)\, I_{rx}(n+1) \qquad 5.40$$

With direct control current: $I_{rx}(n) = I_{rx}(n+1)$

and:

$$P_{rdc} = \frac{1}{2}\left[P_r(n) + P_r(n+1)\right] = \frac{R_r}{2} I_{rx}^2 \qquad 5.41$$

For alternating current control $I_{rx}(n+1) = -I_r(n)$ and:

$$P_{rac} = \frac{R_r}{2}\left[1 + \frac{1}{GN_r^2R_r}\right] I_{rx}^2 \qquad 5.42$$

The power output for parallel differential control for a purely resistive load from equation 5.36:

$$P_{Lr} = \frac{1}{2} P_L(n+1) = \frac{1}{2} \frac{R_L}{R_o^2} \left[\frac{I_{rx}}{GN_r}\right]^2 \qquad 5.43$$

The power gains for this connection are then given by:

$$K_{prdc} = \frac{P_{Lr}}{P_{rdc}} = \frac{R_L}{R_o^2} \frac{1}{G^2N_r^2R_r} \qquad 5.44$$

$$K_{prac} = \frac{P_{Lr}}{P_{rdc}} = \frac{R_L}{R_o^2} \frac{1}{G(1+GN_r^2R_r)} \qquad 5.45$$

In order to make comparisons between the series-differential control and the parallel-differential control it is assumed that the direct control resistance in both cases is the same. From equations 5.25 and 5.41 then R_r must be $2R_j$. On this basis it is seen that where the maximum power gain for the direct controlled, series-differential circuit is obtained the power gain from equation 5.44 is the same as is given by equation 5.35. However there is no mathematical limitation on the power gain for the parallel-differential control and it is, according to this analysis, a high gain connection for half wave amplification which was previously unreported.

The series differential control winding has been widely used, and the voltage and current gains for the purely resistive load with direct control are:

$$K_{vjdc} = \frac{R_L}{R_o} \frac{1}{N_jR_j\left[G+2\sum\frac{1}{N_j^2R_j}\right]} \qquad 5.46$$

$$K_{Ijdc} = \frac{1}{R_o} \frac{1}{N_j(G + 2\frac{1}{N_j^2 R_j})} \qquad 5.47$$

The parallel-differentially controlled amplifiers, for direct inputs, have gains of:

$$K_{vrdc} = \frac{R_L}{R_o} \frac{1}{GN_r R_r} \qquad 5.48$$

$$K_{Irdc} = \frac{1}{R_o} \frac{1}{2GN_r} \qquad 5.49$$

For a single control winding the maximum gains for the series-differential control occur when $GN_j^2 R_j$ is negligably small compared with 2. The limiting gains are then

$$K_{vjdc\ max} = \frac{N_j R_L}{R_o} \qquad 5.50$$

$$K_{Ijdc\ max} = \frac{N_j}{R_j R_o} \qquad 5.51$$

Then the voltage and current gains are restricted to some value less than the turns ratio. On the other hand the gains of the direct controlled parallel differential amplifier do not have this inherent restriction. The primary reason is seen from the general difference equation 5.14 to be the fact that series differential control circuits reflect their loop impedances into all control circuits whereas parallel differential controls circuit do not. The polarity of the windings in the parallel differential control is such that on the average over a half cycle the impedances are cancelled.

5.2 Mode Sequence I Limits.

In order to maintain the mode sequence it is necessary that at no time during the reset half-cycle the gate diodes become forward biased. The forward biasing can occur only when the core voltage is sufficiently negative to overcome the power source which is also negative in the reset half-

cycle. The conditions for either core voltage to unblock the gate diode are found for the output loop to be:

$$E_g(n) \leqq \begin{cases} -(E_s - V_f) & \text{for semi-bridge or center tap} \\ -(E_s - 2V_f) & \text{for bridge} \end{cases} \qquad 5.52$$

The values of $E_g(n)$ and $E'_g(n)$ were found for expression 5.12 and 5.13. If the inputs are positive then the core 2 voltage is most negative and the inequality of expression 5.52 will occur first for that core. The diode forward biasing will not occur for either core if, from expressions 5.12 and 5.13:

$$\frac{\frac{E_{bi}(n)}{N_i R_i} + I_o \pm \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r}}{G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}} \geqq -\left[E_s - V_f\right] \qquad 5.53$$

$$G + 2\sum \frac{1}{N_j^2 R_j}$$

where $V_f \longrightarrow 2V_f$ for the bridge circuit:

The above should be read in the most general case in terms of instantaneous rather than average values.

The mode sequence may also be violated in the gate half-cycle if either core voltage can become sufficiently positive to prevent current flow. In order to determine whether this can occur in this sequence it is necessary to write the instantaneous expressions for the core voltages and the gate currents in the gating period. If this is done, it is found that such a condition can arise only where alternating control and alternating bias are used. Blocking

is an undesirable condition and can be avoided by using only direct bias when alternating inputs are to be used. However as the core voltages for the gate half cycle are essential for design considerations, they are derived. From the mode C1 core equation (2.15), with neither core saturated, the core voltages for a resistive load are found to be:

$$E_g(C_1) = \frac{\frac{E_{sd}}{R_1} - I_o + \frac{E_{bi}}{N_i R_i}}{G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r} + \frac{1}{R_2}} \pm \frac{\sum \frac{e_j}{N_j R_j} + \sum \frac{i_{rx}}{2N_r}}{G + \sum \frac{2}{N_j^2 R_j} + \frac{1}{R_3}} \qquad 5.54$$

where the upper sign is for the core 1 and the lower for core 2. and where:

$$E_{sd} = \begin{cases} E_s - 2\,V_f & \text{for bridge} \\ E_s - V_f & \text{for centertap} \\ E_s - V_f & \text{for semi-bridge} \end{cases}$$

$$R_1 = \begin{cases} 2R_s + R_w & \text{for bridge} \\ R_w & \text{for centertap} \\ R_w + 2R_s + \frac{2R_d(R_L + R_d)}{R_L + 2\,R_d} & \text{for semi-bridge} \end{cases}$$

$$R_2 = \begin{cases} 2R_s + R_w & \text{for bridge} \\ R_w + 2R_L & \text{for centertap} \\ R_w + 2R_s + \frac{2R_d(R_L + R_d)}{R_L + 2\,R_d} & \text{for semi-bridge} \end{cases}$$

$$R_3 = \begin{cases} 2R_s + R_w & \text{for bridge} \\ R_w & \text{for centertap} \\ R_w & \text{for semi-bridge} \end{cases}$$

After one core has saturated the core voltage is given (for core 2) by:

$$E_g'(C_1) = \frac{\frac{E_{sd}}{R_1} - I_o + \frac{E_{bi}}{N_i R_i} - \sum \frac{e_j}{N_j R_j} - \sum \frac{i_{rx}}{2N_r}}{G + \frac{1}{N_j^2 R_j} + \sum \frac{1}{N_j^2 R_j} + \sum \frac{1}{2N_r^2 R_r} + \frac{1}{R_4}} \qquad 5.55$$

where

$$R_4 = \begin{cases} (2R_s+R_w)(2R_L+R_w)/(R_L+R_s+R_w) & \text{for bridge} \\ R_w(R_w+2R_L)/(R_w+R_L) & \text{for centertap} \\ R_w \left[1 + \frac{1}{1+\frac{R_w}{R_s+R_L}} \right] & \text{for semi-bridge} \end{cases}$$

5.3 Design Considerations for Mode Sequence I Operation.

The cores may be biased so that they saturate half way through the gate half-cycle when the control signals are zero. In this case the relation between source and bias may be obtained from the consideration that the average value of the reset voltage must be the negative of the average gate voltage for both cores. The reset occurs throughout the reset half-cycle, while the gate voltage appears for only half the gate half-cycle. The gate voltage must then be twice the reset voltage in order to maintain the equal magnitude of averages. This may be expressed mathematically:

$$E_g(A2) + 2E_g(C1) = 0 \qquad 5.56$$

From equations 5.12 and 5.54 the relation of bias to source voltage is then:

$$\frac{E_{bi}}{N_i R_i} + I_o = \frac{-\frac{E_{sd}}{R_1} + 2\,I_o}{2 + \frac{1}{R_2}\left[G + {}^{2}/N_i^2 R_i + \sum \frac{1}{N_r^2 R_r}\right]} \qquad 5.57$$

for direct series bias and a purely resistive load.

The linear operation of this type of amplifier has the greatest possible range when one core receives no reset, and thereby has full output the following half-cycle, while the other core is completely reset so that in the following half-cycle, it will not saturate until the instant the gate half-cycle terminates. In this condition, during the reset half-cycle with both cores in mode A2, one core, say core I, has exactly zero reset voltage ($E_g(n) = 0$). The average value of the reset voltage of core 2 must be exactly the same magnitude as its gating voltage in the next half-cycle with core 1 saturated throughout the half-cycle. Then from equation 5.12

$$\frac{\sum \frac{E_i(n)}{N_i R_i} + \sum \frac{I_{rx}(n)}{2N_r}}{G + 2\sum \frac{1}{N_j^2 R_j}} = -\frac{\frac{E_{bi}}{N_i R_i} + I_o}{G + \frac{2}{N_j^2 R_j} + \sum \frac{1}{N_r^2 R_r}} \qquad 5.58$$

in order that $E_g(n)$ be zero.

Wth the above condition occuring, in equation 5.13

$$E_g'(n) = 2\,\frac{\frac{E_{bi}}{N_i R_i} + I_o}{G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}} \qquad 5.59$$

In the next half-cycle with core 2 saturated and with equation 5.58 still holding, then from equation 5.55

$$E_g'(n+1) = \frac{\frac{E_{sd}}{R_1} - 2\,I_o + \left[\frac{E_{bi}}{N_i R_i} + I_o\right]\left[1 + \frac{G + \sum \frac{2}{N_j^2 R_j}}{G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}}\right]}{G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{N_j^2 R_j} + \sum \frac{1}{2N_r^2 R_r} + \frac{1}{R_4}} \qquad 5.60$$

Then as expression 5.59 must be the negative of expression 5.60 in order that the core just reach positive saturation at the end of the gate half-cycle, the relation between bias and source must be:

$$\frac{E_{bi}}{N_i R_i} + I_o = \frac{\left[-\frac{E_{sd}}{R_1} + 2\,I_o\right]\left(G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}\right) R_4}{2 + 4\,R_4\left[G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r} + \sum \frac{2}{N_j^2 R_j}\right]} \qquad 5.61$$

Comparision between equations 5.57 and 5.61 shows that the two criteria for choosing bias do not necessarily give the same value of bias. If the two equations are set equal, then a design criterion may be obtained which will insure symmetry of the output about the midpoint of the gate half cycle. This is desirable for the situation where the output is alternating and the phase shift is to be held at zero on the fundamental component.

If the two equaions are set equal for the bridge circuit, the resulting design criterion is that:

$$R_s = R_L \qquad 5.62$$

$$\sum \frac{1}{N_j^2 R_j} = \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} \qquad 5.63$$

For the centertap circuit the criterion for symmetrical operation over the entire linear range of mode sequence I is that:

$$\sum \frac{1}{N_j^2 R_j} = \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} \qquad 5.64$$

And for the semibridge circuit it is impossible to realize symmetrical operation. From the results given by equations 5.63 and 5.64 it is seen that symmetrical operation is only possible for series-differential control windings, and the higher gain parallel-differential control cannot achieve perfect symmetry of the output wave form.

In order to make the most efficient use of the magnetic core characteristics, the maximum core voltage which is obtained when one core is saturated should be just sufficient to drive the core from negative to positive saturation in exactly one half-cycle of the supply frequency. The maximum voltage can occur when there is direct bias and when the control is sufficient to completely reset one core in the reset half cycle and prevent the other from receiving any reset, as in equations 5.58. Then in the following positive half cycle, if this control is alternating, the net mmf from the bias and control circuits is zero, and the gate circuit

must provide all the magnetizing current as well as the flux change. Then if the change in flux is to be limited to the full flux change of $2\Phi_s$ the following inequality must hold:

$$\frac{2E_s}{n_g} \leq 2\Phi_s T \qquad 5.65$$

for the bridge and centertap circuits, where T is the period of the half-cycle. In terms of core dimensions and properties:

$$E_s \leq 2fn_g A_c B_s \qquad 5.66$$

The smallest core is obtained for the equality.

The gate windings, on the other hand, must be capable of carrying the maximum average load current when one core is saturated, and the maximum average gate current when both cores are saturated. For midpoint bias both cores are saturated for half the cycle when there are no control inputs. The maximum gate currents for the source in this case are, on an average basis:

$$I_{g\ max.} = \begin{cases} e_s/(2R_s + R_w + R_d) & \text{semi bridge} \\ e_s/(2R_s + R_w) & \text{bridge} \\ e_s/R_w & \text{center tap} \end{cases} \qquad 5.67$$

When one core is saturated and the other unsaturated the maximum gate winding current is approximately the load current, neglecting the magnetizing current in the unsaturated core. Then for a resistive load:

$$I_{Lmax} = \begin{cases} e_s / \left[R_s + R_w + \dfrac{R_d(R_L + R_d)}{R_L + 2R_d} \right] & \text{semi-bridge} \\ e_s / (R_s + R_w + R_L) & \text{bridge} \\ e_s / (R_w + R_L) & \text{center tap} \end{cases} \qquad 5.68$$

In order to obtain maximum power transfer to the load for the semi-bridge the mixing resistor has the value

$$2 R_d^2 = R_L^2 \qquad 5.69$$

The maximum gate current is limited to twice the maximum load current for design purposes. Then the resistance restrictions are:

semi-bridge: none

bridge: $2R_s \geq R_L$

center tap: $R_s \geq R_L$

Then the heating current for the case where both cores saturate half way through the gate half cycle is restricted on the average to:

$$I_g \Big|_{I_L = 0} \leq \frac{1}{2} I_{Lmax} \qquad 5.70$$

And when full output is obtained

$$I_g \Big|_{I_L} = I_{Lmax} = \frac{I_{Lmax}}{2\sqrt{2}} \qquad 5.71$$

Then the gate windings must be capable of carrying half the maximum load current, on the average.

Heating current density for amplifiers operating without external cooling is limited to one milliampere per cir-

cular mil.[6] The wire size for the gate windings is then determined by the load current requirements:

$$A_{cu} = \frac{I_{Lmax\ avg.}}{2\ J_{max}} \quad \left[\text{circular mils}\right] \qquad 5.72$$

where J_{max} is the maximum current density in amperes per circular mil.

The core area available for gate windings [7] is a fraction of the total window area K_{wg}. In this area all n_g gate turns must be placed:

$$n_g\ A_{cu} = K_{wg}\ A_w \qquad 5.73$$

Then a measure of the smallest core, to meet the power requirements of the amplifier, is given by the product of the window area and core cross-section area. From equations 5.66 5.72 and 5.73:

$$A_c A_w \geq \frac{E_s\ I_{Lmax\ avg}}{f\ J_{max}\ K_{wg}\ B_s} \quad \left[\text{circular mil-M}^2\right] \qquad 5.74$$

Equation 5.74 indicates the smallest core size in general which will be capable of controlling the required load power.

5.4 Operation with One Core in Sequence I and the Other in Sequence II.

With this combination of sequences the analysis is complicated by the fact that the core operating in sequence I saturates positively in the gate half cycle while the core

6. See chapter seven page 118
7. See chapter seven page 119

in sequency II saturates negatively in the normal reset half-cycle. The core voltage relations for core one in sequence I and core two in sequence II are:

$$E_g'(n) + E_g'(n-1) = 0 \qquad 5.75$$

$$E_g(n) + E_g(n+1) = 0 \qquad 5.76$$

The average values for both cores are not available in the same half cycle. The core-one voltage must be related to the n^{th} half-cycle when it remains unsaturated. The core-two voltage must be related to the gate half-cycle when it remains unsaturated. These relations are found through the core functions. In the reset half-cycle:

$$\sum \frac{I(n)}{N} = - I_o + GE_g(n) \qquad 5.77$$

As core-one is in mode A2 throughout the half-cycle. In the gate half-cycle:

$$I_g'(n\pm1) + \sum \frac{I'(n\pm1)}{N} = I_o + GE_g'(n\pm1) \qquad 5.78$$

As core-two remains in mode C1 throughout the gate half-cycle.

The gate winding current in the gate half-cycle may be written:

$$I_g'(n\pm1) = \frac{E_{sd}}{R_5} - \frac{1}{R_6} E_g(n\pm1) - \frac{1}{R_7} E_g'(n\pm1) \qquad 5.79$$

where

$$E_{sd} = \begin{cases} E_s - 2V_f & \text{bridge} \\ E_s - V_f & \text{center tap} \\ E_s - V_f & \text{semi-bridge} \end{cases}$$

$$R_5 = \begin{cases} 2R_s + R_w & \text{bridge} \\ R_w & \text{center tap} \\ 2R_s + R_w + R_d & \text{semi-bridge} \end{cases}$$

$$\frac{1}{R_6} = \begin{cases} \frac{1}{2}\left(\frac{1}{2R_s+R_w} + \frac{1}{R_o}\right) & \text{bridge} \\ \frac{1}{2}\left(\frac{1}{R_w} + \frac{1}{R_o}\right) & \text{center tap} \\ \frac{1}{2}\ \frac{1}{R_o}\left[\frac{R_d + R_s(2 + R_L/R_d)}{2R_s + R_w + R_d}\right] & \text{semi-bridge} \end{cases}$$

$$\frac{1}{R_7} = \begin{cases} \frac{1}{2}\left(\frac{1}{2R_s+R_w} - \frac{1}{R_o}\right) & \text{bridge} \\ \frac{1}{2}\left(\frac{1}{R_w} - \frac{1}{R_o}\right) & \text{center tap} \\ \frac{1}{2}\left(\frac{1}{2R_s+R_w+R_d}\right)\left[1 - \frac{R_d+R_s(2+R_L/R_d)}{R_o}\right] & \text{semi-bridge} \end{cases}$$

The control currents are given in equations 5.6 through 5.11 and are valid for any time by inserting the particular half cycle where n appears in these equations.

Then it can be shown that: 5.80

$$\frac{E_{sd}}{R_5} - I_o + \frac{E_{bi}(n\pm1)}{N_i R_i} + \frac{I_{bq}(n\pm1)}{2N_q} - \sum \frac{E_j(n\pm1)}{N_j R_j} - \sum \frac{I_{rx}(n\pm1)}{2N_r}$$

$$= \left[\frac{1}{R_6} + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} - \sum \frac{1}{N_j^2 R_j} - \frac{1}{2N_q^2 R_q} \right] E_g(n\pm1)$$

$$+ \left[G + \frac{1}{R_7} + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} \right] E_g'(n\pm1) \qquad 5.80$$

and that

$$\frac{E_{bi}(n)}{N_i R_i} + \frac{I_{bq}(n)}{2N_q} + \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r} + I_o$$

$$= \left[G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} \right] E_g(n)$$

$$+ \left[\frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} \right] E_g'(n) \qquad 5.81$$

Then it may be shown by use of equations 5.75, 5.76, 5.80, 5.81, 5.1 and 5.15 through 5.21 that:

$$AX(n+1) + B\left[\frac{E_{sd}}{R_5} - I_o + \frac{E_{bi}(n+1)}{N_i R_i} + \frac{I_{bq}(n+1)}{2 N_q} - \sum \frac{E_j(n+1)}{N_j R_j} - \sum \frac{I_{rx}(n+1)}{2 N_r} \right]$$

$$+ C\left[\frac{E_{bi}(n)}{N_i R_i} + \frac{I_{bq}(n)}{2N_q} + \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r} + I_o \right]$$

$$+ D\left[\frac{E_{sd}}{R_5} - I_o + \frac{E_{bi}(n-1)}{N_i R_i} + \frac{I_{bq}(n-1)}{2N_q} - \sum \frac{E_j(n-1)}{N_j R_j} - \sum \frac{I_{rx}(n-1)}{2 N_r} \right]$$

$$= E\, X\, (n-1) \qquad 5.82$$

where X (n±1) may be any one of the following:

$$K_d E_1(n\pm1) - R's I_1(n\pm1)$$

$$N_j[E_j(n\pm1) - R_j I_j(n\pm1)]$$

$$N_r[2E_r(n\pm1) - R_r I_{rx}(n\pm1)]$$

and where

$$A = \left[G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N^2{}_j R_j} + \frac{1}{2N_q^2 R_q} \right]$$

$$\left[G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} + \frac{1}{R_7} \right]$$

$$B = G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q}$$

$$C = G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r} + \frac{1}{R_6} + \frac{1}{R_7}$$

$$D = \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} - \sum \frac{1}{N_j^2 R_j} - \frac{1}{2N_q^2 R_q}$$

$$E = \left[\frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} - \sum \frac{1}{N_j^2 R_j} - \frac{1}{2N_q^2 R_q} \right]$$

$$\left[\frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_i^2 R_r} - \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} + \frac{1}{R_6} \right]$$

In steady state all quantities in the $(n+1)^{st}$ half-cycle are equal to those in the $(n-1)^{st}$ half-cycle. For direct control signals the control functions are identical for all three half-cycles. With alternating control signals the control functions in the $(n+1)^{st}$ and $(n-1)^{st}$ half-cycles

are the negative of those in the n^{th} half-cycle. Then the equation 5.82 for steady state becomes:

$$K_a\, X(n+1) = K_b + K_c \left[\sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{rx}(n)}{2N_r} \right] \qquad 5.83$$

where, with direct control and bias:

$$K_a = (G + \frac{1}{R_7})(G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q})$$

$$- \frac{1}{R_6}(\frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} - \sum \frac{1}{N_j^2 R_j} - \frac{1}{2N_q^2 R_q})$$

$$+ 4\,(\frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r})(\sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q})$$

$$K_b = \left[\frac{E_{sd}}{R_5} - 2I_o \right] \left[G + \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} + \sum \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} \right]$$

$$+ \left[\frac{E_{bi}}{N_i R_i} + \frac{I \Phi q}{2N_q} + I_o \right] \left[2(G + \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}) + \frac{1}{R_6} + \frac{1}{R_7} \right]$$

$$K_c = \frac{1}{R_6} + \frac{1}{R_7}$$

This expression may be directly applied to obtain the bias level, as the output must be zero in steady state when the control signals are zero. Then the bias necessary is obtained by setting K_b to equal zero.

The gain for this type of operation may be obtained by taking $X(n+1)$ as the output. For example, with a resistive load and for series control and bias:

$$R_o I_L(n+1) = \frac{(1 + R_7/R_6)\, N_j E_j(n)}{(1+GR_7)[1+(G+ \frac{1}{N_i^2 R_i})N_j^2 R_j]} \qquad 5.84$$

This connection is then very similar to that of the single-core amplifier in its gain but has the advantage of a reversible output. In instances where the output circuit resistance is small in comparison to the control resistance the results of the analysis differ only slightly from the single core amplifier, and the analysis is unnecessary except in establishing the bias.

The above is true when the negative gain for the cutoff core is sufficiently low that the core saturates negatively at very nearly the end of the reset half cycle.

The power requirement for this type of operation is roughly half that for operation with both cores in sequence I, thereby allowing half the core cross-section area - window area product for the core. However the gain is somewhat less than half that obtainable for the larger core.

CHAPTER VI VOLTAGE RESET CIRCUITS

Any of the full wave output circuits of figure 4.9 may be used with either the commutated or commutated-differential control circuits of figure 4.10 to realize the class of two core circuits known as voltage reset circuits. These circuits are two core adaptions of a circuit devised by R. A. Ramey [8] in 1951.

The commutating control allows for the isolation of the gating core from the resetting core, removing all core interaction. The primary advantages of these circuits is the half-cycle response, and the low input power requirements. For normal operation the input power is actually negative as the commutating, or reset, source causes current to flow into the positive terminal of the control source.

The analysis of the voltage reset circuits is quite simple because of the core isolation. The analysis may be performed on a single core for all mode sequences of interest, and then the effects of two cores taken into account on a superposition basis. This is possible as only one core can be affected by either the input or output currents for a particular half cycle.

The above is true under the assumption that the gating core's reset diode remains reverse biased, and that the resetting core's gate diode remains reversed biased during

[8] Ramey, R. A., On the Mechanics of Magnetic Amplifier Operation, Trans AIEE, vol 70,, part II pp 1214-1222,1951

the entire half-cycle.

6.1 Analysis with a Core Operating in Mode Sequence I.

With mode-sequence I operation core two is reset in the n^{th} half-cycle, with the core-diode mode A2. Then from equation 2.13 the core function is:

$$\frac{I_c(n)}{N} = - I_o + GE'_g(n) \qquad 6.1$$

Then from equation 4.23 or 4.25:

$$\left[G + \frac{1}{N_c^2 R_c}\right] E'_g(n) = \frac{E_c(n)}{N_c R_c} - \frac{E'_s(n) - V_{fc}}{N_c R_c} + I_o \qquad 6.2$$

The average value of core two voltage for the cycle is zero, as the core began the n^{th} half-cycle in saturation and ended the $(n + 1)^{st}$ half-cycle in saturation.

$$E'_g(n) + E'_g(n + 1) = 0 \qquad 6.3$$

The output relation for the $(n + 1)^{st}$ half-cycle is then found to be:

$$\left[G + \frac{1}{N_c^2 R_c}\right] \left[R'_s I_L(n + 1) - K_d E_L(n + 1)\right]$$

$$= \frac{E_c(n)}{N_c R_c} + \left(G + \frac{1}{N_c^2 R_c}\right) E_{sd} - \frac{E'_s(n) - V_{fc}}{N_c R_c} + I_o \qquad 6.4$$

The maximum output is obtained when the reset voltage in the n^{th} half-cycle is zero. This occurs when

$$E_c(n) = E_s(n) - V_{fc} - N_c R_c I_o \qquad 6.5$$

The minimum output occurs when the reset voltage is just sufficient to balance the gate voltage in the $(n+1)^{st}$ half-cycle, so that the core does not saturate in the output half-cycle. In this situation the core must be in mode C1 throughout the gate half-cycle. The core function for mode C1 is:

$$i_g' = I_o + G e_g' \qquad 6.6$$

For all circuits except the semi-bridge the gate current and the load current are identical. In the semi-bridge:

$$(R_s + R_w + R_d/2)\, i_g' = e_{sd} - e_g' + \frac{1}{2} e_L \qquad 6.7$$

or with a purely resistive load

$$\left[R_s + R_w + \frac{R_d(R_L + R_d)}{R_L + 2R_d} \right] i_g' = e_{sd} - e_g' \qquad 6.8$$

Then for a resistive load, for all the output circuits

$$R_o\, i_g' = e_{sd} - e_g' \qquad 6.9$$

where

$$R_o = \begin{cases} R_s' + K_d R_L & \text{for all but semi bridge} \\ R_s + R_w + \dfrac{R_d(R_L + R_d)}{R_L + 2R_d} & \text{for the semi bridge} \end{cases}$$

For a resistance load the gate voltage in mode C1 is:

$$\left(G + \frac{1}{R_o}\right) e_g'(C1) = \frac{E_{sd}}{R_o} - I_o \qquad 6.10$$

In order to maintain the core in the unsaturated condition throughout the gate half-cycle it is necessary that the core voltage in the reset half-cycle be the negative of that given by equation 6.10. The minimum output occurs when:

$$\frac{\frac{E_c(n)}{N_c R_c} - \frac{E_s'(n)-V_{fc}}{N_c R_c} + I_o}{G + \frac{1}{N_c^2 R_c}} + \frac{\frac{E_{sd}}{R_o} - I_o}{G + \frac{1}{R_o}} = 0 \qquad 6.11$$

In general it is desirable to have the minimum output when the control is zero. The bias then, is normally set by equation 6.11 when $E_c(n)$ is zero:

$$\frac{E_s'(n) - V_{fc}}{N_c R_c} - I_o = \frac{G + \frac{1}{N_c^2 R_c}}{G + \frac{1}{R_o}} \left[\frac{E_{sd}}{R_o} - I_o \right] \qquad 6.12$$

Substituting the relation of equation 6.12 into the output relation 6.4, the minimum output is found to be:

$$I_{Lmin.} = \frac{GE_{sd} + I_o}{1 + GR_o} \qquad 6.13$$

The maximum output when $E_g'(n)$ is zero is:

$$I_{Lmax} = \frac{E_{sd}}{R_o} \qquad 6.14$$

The value of control for maximum output is:

$$N_c E_c(n) = \frac{1 + GN_c^2 R_c}{1 + G R_o} \left[E_{sd} - R_o I_o \right] \qquad 6.15$$

And the gain from equation 6.4 is

$$\frac{\Delta I_L(n+1)}{\Delta E_c(n)} = \frac{1}{R_o} \frac{N_c}{1+GN_c^2R_c} \qquad 6.16$$

All of the above results are applicable to the input-output relations for the $(n+1)^{st}$ and $(n+2)^{nd}$ half-cycles when the control voltage is direct for the commutated or alternating for the commutated differential connection.

6.2 Consideration of Other Mode Sequences.

Mode sequence I is the normal linear mode of operation. Other mode sequences are of interest if the amplifier is to be operated to saturation or cutoff.

For saturated operation the control in the n^{th} half-cycle must exceed the value given by equation 6.15. When this occurs, the increase first blocks or reverse biases the control diodes. A further increase will not affect the commutated control circuit, but will tend to unblock the control diode of core-one in the commutated differential circuit. However, as core one is also saturated, the increase in control will not affect the output.

For cutoff operation mode sequence II occurs. This mode sequence does not affect the output, which remains at the minimum , because the cores are decoupled. The operation in this case only affects the control current.

6.3 Mode Sequence Limits.

The only remaining consideration then is that the resetting core's gate diode remains reverse biased for the

resetting half cycle. The output current is given by equation 6.13 before core one saturates and by 6.14 after. The conditions necessary to maintain reverse bias on the diode of the resetting core are tabulated in table 6.1, which was determined from the output loop equations and equation 6.2

	$\frac{NE_c(n)}{1+GN_c^2R_c} \geq$
Incomplete bridge	$\left[\frac{R_s+R_f}{R_o} - \frac{GR_o}{1+GR_o}\right]E_s - \left[\frac{R_s+R_f+R_o}{1+GR_o}\right] 2V_f - \frac{R_oI_o}{1+GR_o}$
Centertap	$-\frac{G(R_L+R_o)}{1+GR_o}E_s - \frac{2+G(R_o-R_L)}{1+GR_o} V_f - \frac{R_o+R_L}{1+GR_o} I_o$
Bridge	$\frac{R_o-R_L-R_s}{1+GR_o}\left[G(E_s - 2V_f) + I_o\right]$
Doubler	$\left[\frac{R_L}{R_o} - \frac{GR_o}{1+GR_o}\right] E_s - \left[\frac{R_L}{R_o} + \frac{2+GR_o}{1+GR_o}\right] V_f - \frac{R_oI_o}{1+GR_o}$
Semi-bridge	$\frac{G(R_o+R_d)}{1+GR_o} E_s - \frac{2+G(R_o-R_d)}{1+GR_o} V_f - \frac{R_o+R_d}{1+GR_o} I_o$

Table 6.1. Conditions to maintain reverse bias on gate diode of reset core during the reset half-cycle.

It is noted that the doubler circuit tends to have its gate diode unblocked for most of the linear range of operation. The fact that this does not significantly alter the operation from the predicted indicates that the unblocking in this circuit, which takes place after the gating core has saturated, is not of very great importance. For this reason it is more reasonable to expect that the unblocking

which takes place before the gating core has saturated (which occurs for a smaller value of control then indicated in table 6.1 for the semibridge, bridge and doubler) is of much more critical importance. The values of control which will cause unblocking before the gating core has saturated are given in table 6.2.

	$\frac{N_c E_c(n)}{1+GN_c^2R_c} \geq$
Incomplete bridge	$-\frac{R_o-R_s-R_f}{1+GR_o}\left[GE_s+I_o\right]-\frac{1+G(R_s+R_f)}{1+GR_o}V_f$
Centertap	Same as table 6.1
Bridge	$-\frac{R_o-R_1-R_s}{1+GR_o}\left[G(E_s-2V_f)+I_o\right]$
Doubler	$-\frac{R_o-R_L}{1+GR_o}\left[GE_s+I_o\right]-\frac{2+G(R_o-R_L)}{1+GR_o}V_f$
Semi bridge	same as table 6.1

Table 6.2 Conditions to maintain resetting gate diode reverse biased prior to saturation of the gating core.

Then the linear operation is maintained essentially for all values of positive control up to saturation. However the negative region of control may show a slight negative slope depending on the output circuit.

6.4 Amplifier Characteristics.

The static characteristics of the voltage reset circuits are shown in figure 6.1. The limits of mode sequence I are determined from equations 6.13 and 6.14 with the bias set by equation 6.12.

6.5 Design Considerations.

The minimum size of core may be determined from considerations similar to those of chapter five. The expression for the minimum core size for the voltage reset circuits may be shown to be:

$$A_c A_w \geq \frac{\eta P_{Lmax}}{4fK_{wg} j_{max} B_s} \qquad 6.17$$

where η is 1/2 for 50% duty cycle.

The input current is found from equations 6.1, 6.2 and 6.12 for normal bias to be:

$$\frac{I_c(n)}{N_c} = \frac{GNE_c(n)}{1+GN^2R_c} - \frac{GE_{sd}+I_o}{1+GR_o} \qquad 6.18$$

The input source power in linear operation is then

$$P_{in} = \frac{N^2GE_L^2}{1+GN^2R_o} - \frac{GE_{sd}+I_o}{1+GR_o} NE_c \qquad 6.19$$

The voltage reset circuits are fast response circuits with the voltage gain limited to the turns ratio. The input power in the linear region of operation is negative, and the control source must be capable of absorbing this power. The input and outputs are completely decoupled,

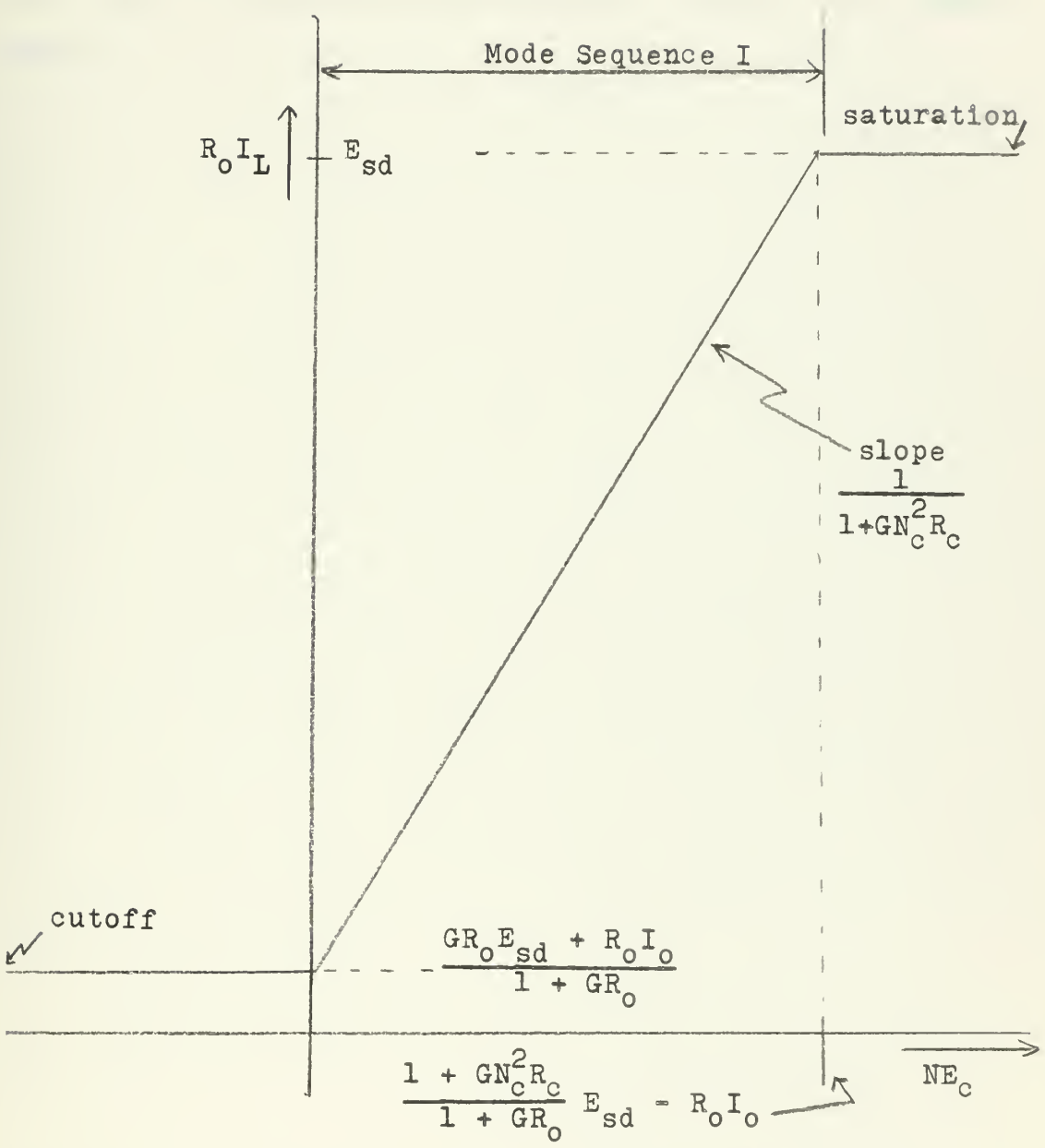


Figure 6.1. Characteristics of Voltage Reset Amplifiers.

and any additional windings will destroy this property. This class of circuits is practically limited to a single input.

CHAPTER 7 DOUBLET AMPLIFIERS

The full wave output circuits, used with control circuits without diodes, provide the possibility of obtaining high gain, greater than would be expected by the turns ratio. This must necessarily be accomplished by some form of positive feedback. For these circuits the positive feedback is provided by the topology of the input circuits. The feedback mechanism in these circuits occurs because the gating core voltage is proportional to the negative of the output, as is seen in equations 4.3 through 4.12. If the control circuit is connected in such a way that the gating voltage of the gating core is reflected into the control circuit in such a sense as to oppose the reset of the resetting core, the feedback is negative. This is seen to occur in the series-differential connection of figure 4.10, as well as the parallel control connection. For the series control and the parallel-differential control the feedback is positive, as the gate voltage of the gating core is in the sense to aid the reset of the resetting core.

Feedback in two-core magnetic amplifiers is possible only when there is an output during the time that a core is resetting. For this reason feedback is impossible in half-wave output circuits, where both cores are gated to saturation in the same half cycle. The use of feedback though possible, is undesirable in half cycle response circuits as it destroys the half cycle response. Feedback in the circuits which alternate gate half-cycles, and have

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no diodes in the basic control circuits, have a natural feedback. As previously mentioned this feedback is positive for two of the four basic configurations. Then it is reasonable to expect that the gain of these two circuits will be higher than that of the basic amplifier. The other two control connections have negative feedback and would not seem to be high gain amplifiers. However they may provide high gain if they are used as differential amplifiers, where the difference in the outputs between two adjacent half cycles is the effective output.

Besides the natural feedback which occurs in these circuits, the fact that one core resets while the opposite core is in the output half-cycle allows for the use of external feedback. The magnetic amplifier may use either magnetic or electric feedback, or a combination of the two. The fact that external feedback can be realized makes this class of magnetic amplifiers the most versatile of all those discussed in this work.

In the operation of these circuits it is important to maintain the gate diodes in their proper bias condition. That is, when a core is in its output half-cycle it is necessary that the associated diode or diodes be maintained in the forward biased condition. In the half cycle that the core is being reset, it is necessary to maintain its associated gate diode in the reverse bias condition. If these conditions are not maintained then the amplifying characteristics degenerate. If the gate diode of the resetting core

forward biased, then the efficiency of the reset source is impaired by the incremental output impedance which appears to shunt the core. This leads to what is generally a drastic reduction in gain, as the output loop impedance is usually much less than the core's dynamic resistance. If the gating diode becomes reverse biased during the gating period, then control is lost for the interval and the gain may be either reduced drastically, or may even become negative.

To assure that the diode bias conditions are maintained in the circuits, it is necessary to determine the critical values of core voltage at which they are violated. For circuits with purely resistive loads the critical core voltages, as determined for the various output loops, are given in table 7.1. These relations were derived only for the n^{th} half cycle where core 1 is gated and core 2 reset. That the results are general may be determined by the symmetry of the output circuits.

Table 7.1

	To prevent the gate diode from being reverse biased	To prevent the reset diode from being forward biased
Incomplete bridge	$e_g \leq e_s - 2V_f$	$e'_g \geq -e_s + i_L(R_s + R_f)$
Center tap	$e_g \leq e_s - V_f$	$e'_g \geq -e_s + V_f + i_L R_L$
Bridge	$e_g \leq e_s - 2V_f$	$e'_g \geq -e_s + 2V_f + i_L(R_L + R_s)$
Doubler	$e_g \leq e_s - V_f$	$e'_g \geq -(e_s + V_f) + i_L R_L$
Semi-bridge	$e_g \leq e_s - V_f$	$e'_g \geq -e_s + V_f + i_L R_d$

It is noted that, in cases where the unblocking of the resetting cores gate diode is of critical importance, the center tap circuit is superior to the incomplete bridge, which in turn is superior to the bridge for direct outputs. For alternating outputs, the semibridge circuit is superior to the doubler in terms of unblocking of the resetting cores gate diode, but has the disadvantage of the resistive mixing circuit.

In order that the high gain feature of these circuits be realized, it is necessary that the cores be operating in mode sequence I. That is, both cores must be in their high gain regions, though operating in time translation from each other. Mode sequence II is of some interest for some applications, as it corresponds to the cutoff condition for electronic amplifiers. The sequence combination in which one core is operated in mode sequence I while the other is in sequence II is of interest in the case of differential amplifiers, but is not a high gain situation. The results in the latter case are not very different from the half-wave circuits.

7.1.Analysis With Both Cores In Mode Sequence I.

In mode sequence I a core is gated to saturation in the positive half-cycle, corresponding to core-diode modes C1 and D1. In the negative half-cycle of its source it is reset, not reaching negative saturation, and is in core-diode modes A2 for the entire half-cycle. With this se-

quence occurring in both cores, core 1 gates and saturates in the n^{th} half-cycle while core 2 resets. In the $(n+1)^{st}$ half cycle the roles of the cores are reversed and core 2 gates to saturation while core 1 resets. It is therefore possible to relate the gate voltage of core 1 to the output in the n^{th} half-cycle through equation 4.11 and the gate voltage of core 2 to the output in the $(n+1)^{st}$ half-cycle through equation 4.12. As the net change of flux in core 2 is zero for the cycle beginning with the onset of the n^{th} half-cycle these core voltages are related by the equation:

$$E_{g2}(n) + E_{g2}(n+1) = 0$$

For an arbitrary number of series control circuits the sum of the resetting currents are found from the average values of the loops in equations 4.13 and 4.14:

$$\sum \frac{I_i'(n)}{N_i} = \sum \frac{E_i(n)}{N_i R_i} - \sum \frac{1}{N_i^2 R_i} \left[E_g(n) + E_g'(n) \right] \qquad 7.2$$

For the series-differential control with an arbitrary number of windings, equations 4.15 and 4.16 yield:

$$\sum \frac{I_j'(n)}{N_j} = - \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{1}{N_j^2 R_j} \left[E_g(n) - E_g'(n) \right] \qquad 7.3$$

For the parallel control circuits from equations 4.17, 4.18 and 4.19:

$$\sum \frac{I_q'(n)}{N_q} = \sum \frac{I_{qx}(n)}{2N_q} + \sum \frac{1}{2N_q^2 R_q} \left[E_g(n) - E_g'(n) \right] \qquad 7.4$$

And for the parallel-differential case, from equations 4.20, 4.21 and 4.22:

$$\sum \frac{I_r'(n)}{N_r} = -\sum \frac{I_{rx}(n)}{2N_r} - \sum \frac{1}{2N_r^2 R_r}\left[E_g(n) + E_g'(n)\right] \qquad 7.5$$

These relations may be combined to eliminate the reset currents by the use of the core function which corresponds to mode A2 as given in equation 2.13.

$$\sum \frac{I}{N} = -I_o + GE_g \qquad 2.13$$

The resulting expression:

$$E_g'(n) = K_1\left[\sum \frac{E_i(n)}{N_i R_i} - \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{qx}(n)}{2N_q} - \sum \frac{I_{rx}(n)}{2N_r} + I_o\right] - K_2 E_g(n) \qquad 7.6$$

where $K_1 = 1/\left[G + \sum 1/N_i^2 R_i + \sum 1/N_j^2 R_j + \sum 1/N_q^2 R_q + \sum 1/N_r^2 R_r\right]$

$$K_2 = K_1\left[\sum 1/N_i^2 R_i - \sum 1/N_j^2 R_j - \sum 1/N_q^2 R_q + \sum 1/N_r^2 R_r\right]$$

Then the output difference equation is obtained by eliminating the core voltages from equations 4.11, 4.12, 7.1 and 7.6. The result given in equation 7.7:

$$R_s I_L(n+1) - K_d E_L(n+1) = K_1\left[\sum \frac{E_i(n)}{N_i R_i} - \sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{qx}(n)}{2N_q} - \sum \frac{I_{rx}(n)}{2N_r}\right]$$
$$K_2\left[R_s I_L(n) - K_d E_L(n)\right] + K_1 I_o + (1-K_2) E_{sd} \qquad 7.7$$

A similar development between the $(n+1)^{st}$ and $(n+2)^{d}$ half-cycles yields an expression which differs from this only in

the signs of voltages associated with the differential windings indicated by the subscripts j and r. The expressions for K_1 and K_2 are unchanged.

An examination of K_2, regarding its effect on the difference equation, shows that the series control circuits and the parallel differential control circuits exhibit positive feedback, while the series differential and parallel controls have negative feedback, as previously suggested.

Another interesting point in the development is in the expressions for the control with the parallel circuits. If these had been written in terms of the terminal voltages rather than the currents, no interaction between the cores would have appeared in the output difference equation for the parallel circuits. Similarly if for the series control circuits, the control currents had been taken as the variables, no core interaction would have appeared in the equations. From these considerations it is preferable to consider the series windings as voltage controlled and the parallel windings as current controlled.

The series and parallel control circuits retain their positive sign in the difference equation, indicating they are direct control configurations for ordinary amplifiers, or alternating control circuits for differential amplifiers. For straight amplification the positive feedback of the series control make it more desirable than the parallel control. However for differential amplifiers the negative feedback is more desirable, as it acts as if it were actually positive in that application. Then the series control is seen to be a natural configuration for direct control of ordinary amplifiers, while the parallel is the natural configuration for differential amplifiers with alternating control.

By similar reasoning the parallel differential control is the natural configuration for ordinary amplifier with alternating control while the series differential circuit is natural for a differential amplifier with direct control.

Direct series control and alternating parallel-differential control are grouped as ordinary amplifier control configurations, and the direct series-differential and alternating parallel controls as differential amplifier ordinary control configurations.

7.2 Output Circuit Analysis for Amplifiers Operating in Sequence I.

For the ordinary amplifier the difference equation is modified by letting the resistances with subscripts p and q become infinite while the generated control voltages and currents become zero. Then K_2 retains only the positive feedback terms, and the difference equation between the $(n+1)^{st}$ half cycle and the $(n-2)^{d}$ is of the same form when the terms I_r reverse their signs each half cycle, as is expected in alternating control signals.

In steady state the output is constant from one half cycle to the next, recalling that equations 4.11 and 4.12 were defined in terms of the amplitude of the output. In this case the steady state solution yields a gain which is proportional to $K_1/(1-K_2)$, which, with only positive feedback terms in K_2, is the inverse of the dynamic core conductance G. Then in steady state, for straight amplification using series control for direct signals and parallel-differential control for alternating signals, the input-output relation is:

$$R_s I_L - K_d E_L = \frac{1}{G}\left(\frac{E_1}{N_1 R_1} + \frac{I_{rx}}{2N_r} + I_o + I_{sd}\right) \qquad 7.8$$

A measure of the dynamic characteristic of the self-saturating magnetic amplifier is obtained by considering the step response, the time response to a step change of direct control, or a step change of magnitude for the alternating control. The rise time of the amplifier is defined as the number of half-cycles necessary for the amplifier to come within 1/e of the difference between the initial and final values.

With the step input applied at the beginning of a half-cycle the output in that half cycle remains the same as the previous steady state.

$$R_s I_L(0) - K_d E_L(0) = K_1 \left[\sum \frac{E_i(0)}{N_i R_i} + \sum \frac{I_{xx}(0)}{2N_x} + I_o \right]$$

$$+ (1-K_2)E_{sd} + K_2 \left[R_s I_L(0) - R_d I_L(0) \right]$$

$$R_s I_L(1) - K_d E_L(1) = K_1 \left[\sum \frac{E_i(0)}{N_i R_i} + \sum \frac{I_{xx}(0)}{2N_x} + I_o \right]$$

$$+ (1-K_2)E_{sd} + K_2 \left[R_s I_L(0) - R_d I_L(0) \right]$$

In the half-cycle following the step input the output changes:

$$R_s I_L(2) - K_d E_L(2) = K_1 \left[\sum \frac{E_i(1)}{N_i R_i} + \sum \frac{I_{xx}(1)}{2N_x} + I_o \right]$$

$$+ (1-K_2)E_{sd} + K_2 \left[R_s I_L(1) - R_d I_L(1) \right]$$

The output in the second half-cycle may be manipulated to obtain the result

$$R_s I_L(2) - K_d E_L(2) = K_1 \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{xx}(1) - I_{xx}(0)}{2N_x} \right]$$

$$+ K_1 \left[\sum \frac{E_i(0)}{N_i R_i} + \sum \frac{I_{xx}(0)}{2N_x} + I_o \right] + (1-K_2)E_{sd} + K_2 \left[R_s I_L(1) - R_d I_L(1) \right]$$

$$= K_1 \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{xx}(1) - I_{xx}(0)}{2N_x} \right] + R_s I_L(0) - K_d E_L(0)$$

Then for the third half-cycle the output becomes

$$R_s I_L(3) - K_d E_L(3) = K_1 \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1) - I_{rx}(0)}{2N_r} \right]$$

$$+ K_1 \left[\sum \frac{E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(0)}{2N_r} + I_{sd} - (1 - K_2) E_{sd} - K_2 \left[R_s I_L(2) - K_d E_L(2) \right] \right] \qquad 7.13$$

which becomes:

$$R_s I_L(3) - K_d E_L(3) = K_1 (1 + K_2) \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1) - I_{rx}(0)}{2N_r} \right]$$

$$+ R_s I_L(0) - K_d E_L(0) \qquad 7.14$$

And for the fourth half-cycle

$$R_s I_L(4) - K_d E_L(4) = K_1 (1 + K_2 + K_2^2) \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1) - I_{rx}(0)}{2N_r} \right]$$

$$+ R_s I_L(0) - K_d E_L(0) \qquad 7.15$$

For the n^{th} half-cycle after the step change has occurred the difference between the current in the n^{th} half-cycle and the initial value is given by

$$R_s I_L(n) - K_d E_L(n) - \left[R_s I_L(0) - K_d E_L(0) \right]$$

$$K_1 \sum_{j=0}^{n-2} (K_2^j) \left[\sum \frac{E_i(1) - E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1) - I_{rx}(0)}{2N_r} \right] \qquad 7.16$$

As K_2 is always less in magnitude than 1 the [illegible] mation may be put into [illegible]

$$\sum_{j=0}^{\infty} K_2^j = \frac{1}{1-K_2} = \sum_{j=0}^{n-2} K_2^j + \sum_{j=n-1}^{\infty} K_2^j \qquad 7.17$$

Factoring out K_2^{n-1} from the last term the partial summation may then be written:

$$\sum_{j=0}^{n-2} K_2^j = \frac{1}{1-K_2} - \frac{K_2^{n-1}}{1-K_2} = \frac{1-K_2^{n-1}}{1-K_2} \qquad 7.18$$

The steady state condition occurs in general when the number of half-cycles becomes infinite. In this case K_2^{∞} becomes zero as K_2 is less in magnitude than one. The difference between the initial and final values is then:

$$\frac{K_1}{1-K_2}\left[\sum \frac{E_i(1)-E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1)-I_{rx}(0)}{2N_r}\right] \qquad 7.19$$

While the difference in outputs between the n^{th} half-cycle and the initial value is given by:

$$\frac{K_1}{1-K_2}(1-K_2^{n-1})\left[\sum \frac{E_i(1)-E_i(0)}{N_i R_i} + \sum \frac{I_{rx}(1)-I_{rx}(0)}{2N_r}\right] \qquad 7.20$$

Then in order for the above difference to be 1-1/e of the final difference it is necessary that:

$$K_2^{n_t-1} = e^{-1} \quad \text{or} \quad n_t = 1 + \frac{1}{\ln 1/K_2} \qquad 7.21$$

In this development it was assumed that n_t was a continuous variable. The discreteness of the number of half-cycles causes an indeterminancy in the exact rise time, and the rise time is taken as the next integer value

above that given by equation 7.21.

7.3 Limits of Sequence I Operation for Ordinary Amplifiers.

The limits for mode sequence I may be defined from the physical action in the cores. The maximum output is obtained when the core average voltage in the gate half-cycle is zero and the minimum when the core does not saturate in either the reset or gate half-cycle. The latter case occurs at the boundary between mode sequences I and II. For the ordinary amplifier the maximum output is easily defined, as both cores operate in the same manner, so that when one core is at maximum output the other must receive no reset flux. This occurs then in the n^{th} half-cycle when the core 2 voltage is zero with core 2 in core-diode mode A2 and with core 1 in core-diode mode C1. In this situation $e_g = 0$ and e_g' is given by equation 7.6 and must be zero. Then the maximum output for a straight amplifier occurs at the limit of mode sequence I where:

$$\sum \frac{e_i}{N_i R_i} - \sum \frac{i_{rx}}{2N_r} + I_o = 0 \qquad 7.22$$

The value of 7.22 inserted into the steady state equation shows that

$$(R_s' I_L - K_d E_L)\Big|_{maximum} = E_{sd} \qquad 7.23$$

In order to find the condition for minimum output it is necessary to find the expressions for e_g and e_g' when core 1 is in core-diode mode C1 and Core 2 is in core-diode mode A2. In a more general case it would also be

necessary to find the voltages with these modes reversed. The amplifier is symmetrical and in steady state the expressions for the reversed case are the same as the case considered.

Equation 7.6 taken as an instantaneous relation is the relation between the core voltages derived from the core function of core 2 in mode A2. Equation 2.16 is the appropriate core function for core-diode mode C1. This shows that an expression for the gate circuit current is required for the solution.

If a resistive load R_L is assumed, then the solutions for the core voltages with core 1 in mode C1 and core 2 in mode A2 are given by:

$$\Delta e_g = G\left[\sum \frac{e_i}{N_i R_i} + I_o\right] + \left\{G + \sum \frac{2}{N_r^2 R_r} + \sum \frac{1}{N_r^2 R_r}\right\} \sum \frac{i_{rx}}{2N_r}$$

$$+ \left\{G + \sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r}\right\}\left[\frac{e_{so}}{R_o} - 2\, I_o\right] \qquad 7.24$$

$$\Delta e_g' = \left\{G + \frac{1}{R_o}\right\}\left[\sum \frac{e_i}{N_i R_i} + I_o\right] - \left\{G + \frac{1}{R_o} + \sum \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}\right\}$$

$$\times \sum \frac{i_{rx}}{2N_r} - \left\{\frac{1}{N_i^2 R_i} + \frac{1}{2N_r^2 R_r}\right\}\left[\frac{e_{so}}{R_o} - 2I_o\right] \qquad 7.25$$

where

$$= G\left[G + \sum \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}\right] + \frac{1}{R_o}\left[G + \sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r}\right]$$

and for:

incomplete bridge	$e_{so}=e_s-2V_f$	$R_o= R_w+R_L$
center tap	$e_{so}=e_s-V_f$	$R_o= R_w+R_L$
bridge	$e_{so}=e_s-2V_f$	$R_o= R_w+R_L$
doubler	$e_{so}=e_s-V_f$	$R_o= R_w+R_L$
semi-bridge	$e_{so}=e_s-V_f$	$R_o= R_w+\frac{R_d(R_L+R_d)}{R_L+2R_d}$

In order to obtain minimum output the core must not saturate in either half cycle, gating or resetting, so that it must operate in a degenerate sequence I of C_1 and A_2, and the averge of the core voltage for both modes must be zero. Then in steady state with minimum output, e_g in mode C1 plus e_g' in mode A2 must be zero. From this criterion the minimum output for mode sequence I occurs when:

$$(2G + \frac{1}{R_o})\left[\sum\frac{e_i}{N_iR_i} + I_o\right] - \frac{1}{R_o}\sum\frac{i_{rx}}{2N_r} = - G\left[\frac{e_{so}}{R_o} - 2I_o\right] \qquad 7.26$$

In order that the amplifier be able to operate between the limits given by equations 7.22 and 7.26 it is necessary that the diode biasing conditions remain valid. The mode combinations of interest are one where core 1 is in mode C1 and core 2 in mode A2, and the other where core 1 is in mode D1 and core 2 in mode A2. The latter case, being simpler, is investigated first.

When core 1 is saturated it is impossible for the gate diode to be back biased while the source is positive. Then in this situation it is only necessary to determine the condition of the gate diode for the resetting core. The re-

verse bias limits for each of the output circuits are given in the second column of table 2.1, while the core voltage is given by equation 7.6 when it is taken as an instantaneous equation with $e_g = 0$. For the straight amplifier

$$e_g' = K_1 \frac{e_i}{N_i R_i} - \frac{i_{rx}}{2N_r} + I_o \qquad 7.27$$

and this must remain greater than the right hand member of the inequalities of table 7.1. With core 1 saturated the requirements for the resetting diode to remain reverse biased are given in table 7.2

When core 1 is in mode C1 and core 2 is in mode A2 the criteria to maintain the gating diode unblocked is found from equation 7.24 and the first column of table 7.1. The resulting inequality is expressed in terms of e_{so} and R_o as given after equation 7.25:

$$G\left[\sum \frac{e_i}{N_i R_i} + I_o\right] + \left[G + \sum \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}\right] \sum \frac{i_{rx}}{2N_r}$$

$$\leq -\left(G + \sum \frac{2}{N_i^2 R_i} + \sum \frac{1}{N_r^2 R_r}\right) G E_{so} + \left[G + \sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r}\right] 2I_o$$

As the direct-control currents are negative in mode sequence I, it is impossible that they block the gate diode. However it is possible for the gate diode to be blocked with alternating control.

In order to prevent the resetting core's diode from becoming forward biased, the right hand column of table 7.1 must be satisfied. Solving for the load current for each of the output loops, using equation 7.25 for the gate voltage and equation 7.26 for the resetting core voltage:

incomplete bridge	$\left[G+\frac{1}{N_i^2R_i}+\frac{1}{2N_r^2R_r}\right]^{-1}\left[\frac{e_i}{N_LR_L}-\left[\frac{I_{rx}}{2N_r}+I_o\right]\right] \geq$
incomplete bridge	$-e_s\left[1-\frac{R_s+R_f}{R_o}\right]-2V_f\ \frac{R_s+R_f}{R_o}$
center tap	$-\ e_s\left[1+\frac{R_L}{R_o}\right]+V_f\left[1-\frac{R_L}{R_o}\right]$
bridge	$-\ e_s\ (1-\frac{R_s+R_L}{R_o})+2V_f\ (1-\frac{R_s+R_L}{R_o})$ $-(e_s-2V_f)(1-\frac{R_s+R_L}{R_o})$
doubler	$-\ e_s\ (1-\frac{R_L}{R_o})\ -\ V_f(1+\frac{R_L}{R_o})$
semi bridge	$-\ e_s\left[1+\frac{R_d^2}{R_o(R_L+R_d)}\right]+V_f(1-\frac{R_d^2}{R_o(R_L+R_d}$

Table 7.2. Necessary conditions to prevent reset diode unblocking when the gate core is saturated. Values for R_o given after equation 7.25. R_s = source resistance, R_f = diode forward resistance; R_w includes R_s, R_f and winding resistance R_w.

For the incomplete bridge circuit:

$$\left[G\left(1+\frac{R_s+R_f}{R_o}\right)+\frac{1}{R_o}\right]\left[\sum\frac{e_i}{N_iR_i}+I_o\right]$$

$$-\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_s+R_f}{R_o}\right)+\frac{1}{R_o}\right]\sum\frac{i_{rx}}{2N_r}$$

$$\geq -Ge_s\left[\left(G+\frac{2}{N_i^2R_i}+\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_s+R_f}{R_o}\right)+\frac{1}{R_o}\right]$$

$$-\left[G\left(G+\frac{2}{N_i^2R_i}+\frac{1}{N_r^2R_r}\right)\frac{R_s+R_f}{R_o}+\frac{1}{R_o}\left(\frac{1}{N_i^2R_i}+\frac{1}{2N_r^2R_r}\right)\right]2V_f$$

$$-\left[\left(\frac{1}{N_i^2R_i}+\frac{1}{2N_r^2R_r}\right)\left(1-\frac{R_s+R_f}{R_o}\right)-G\frac{R_s+R_f}{R_o}\right]2I_o \qquad 7.29$$

For the centertap circuit:

$$\left[G\left(1-\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]\left[\sum\frac{e_i}{N_iR_i}+I_o\right]$$

$$-\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1+\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]\sum\frac{i_{rx}}{2N_x}$$

$$\geq -Ge_s\left[\left(G+\frac{2}{N_i^2R_i}+\frac{1}{N_r^2R_r}\right)\left(1+\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]$$

$$-V_f\left[G\left(1-\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]\left[G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right]$$

$$-2I_o\left[\left(\sum\frac{1}{N_i^2R_i}+\sum\frac{1}{2N_r^2R_r}\right)\left(1+\frac{R_L}{R_o}\right)+G\frac{R_L}{R_o}\right] \qquad 7.30$$

For the bridge circuit:

$$\left[G\left(1+\frac{R_L+R_s}{R_o}\right)+\frac{1}{R_o}\right]\left[\sum\frac{e_i}{N_i R_i}+I_o\right]-\left[\left(G+\sum\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_L+R_s}{R_o}\right)+\frac{1}{R_o}\right]\sum\frac{i_{rx}}{2N_r}$$

$$\geq -G(e_s-V_f)\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_L+R_s}{R_o}\right)+\frac{1}{R_o}\right]$$

$$-2I_o\left[\left(\sum\frac{1}{N_L^2R_L}+\sum\frac{1}{2N_r^2R_r}\right)\left(1-\frac{R_L+R_s}{R_o}\right)-G\frac{R_L+R_s}{R_o}\right] \qquad 7.31$$

For the doubler circuit:

$$\left[G\left(1+\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]\left[\sum\frac{e_i}{N_i R_i}+I_o\right]-\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]$$

$$\times\sum\frac{i_{rx}}{2N_r}$$

$$\geq -Ge_s\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1-\frac{R_L}{R_o}\right)+\frac{1}{R_o}\right]$$

$$-2I_o\left[\left(\sum\frac{1}{N_i^2R_i}+\sum\frac{1}{2N_r^2R_r}\right)\left(1-\frac{R_L}{R_o}\right)-G\frac{R_L}{R_o}\right] \qquad 7.32$$

For the semi-bridge circuit:

$$\left[G\left(1-\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right)+\frac{1}{R_o}\right]\left[\sum\frac{e_i}{N_i R_i}+I_o\right]$$

$$-\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1+\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right)+\frac{1}{R_o}\right]\sum\frac{i_{rx}}{2N_r}$$

$$=-Ge_s\left[\left(G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right)\left(1+\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right)+\frac{1}{R_o}\right]$$

$$-V_f\left[G\left(1-\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right)+\frac{1}{R_o}\right]\left[G+\sum\frac{2}{N_i^2R_i}+\sum\frac{1}{N_r^2R_r}\right]$$

$$-2I_o\left[\left(\sum\frac{1}{N_i^2R_i}+\sum\frac{1}{2N_r^2R_r}\right)\left(1+\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right)+G\frac{R_d}{R_L+2R_d}\frac{R_d}{R_o}\right] \qquad 7.33$$

In order that the amplifier operate over the whole range of mode sequence I, it is necessary that none of the inequalities expressed in table 7.2, equation 7.28 and equations 7.29 through 7.33 be violated. For the general amplifier with both direct and alternating control it is difficult, if not impossible, to give the exact limits of the sequence, or to say whether the diode bias conditions are violated, as the dependency of the various conditions do not have any direct correlation. In order to show the effects of the restrictions placed by the inequalities it is necessary to consider more limited cases.

For a direct controlled amplifier the problem of reverse biasing of the gated core's diode cannot occur, and it is only necessary to determine whether forward biasing of the resetting core's diode may occur. From equation 7.26 the value of control for minimum output with only direct control is shown in figure 7.1. If the amplifier does not experience unblocking of the reset diode then a more negative value of control will cause the amplifier to operate in mode sequence II as indicated by the dotted line to the left of the minimum point. If unblocking occurs at a less negative value than for the minimum point, the gain will be decreased as shown on the dashed line until some new minimum is achieved and the slope will then become negative. The mode sequences for the dashed line are sequences III and IV and are generally undesirable. It is seen in table 7.2 and equations 7.29 through 7.33 that the points of reset

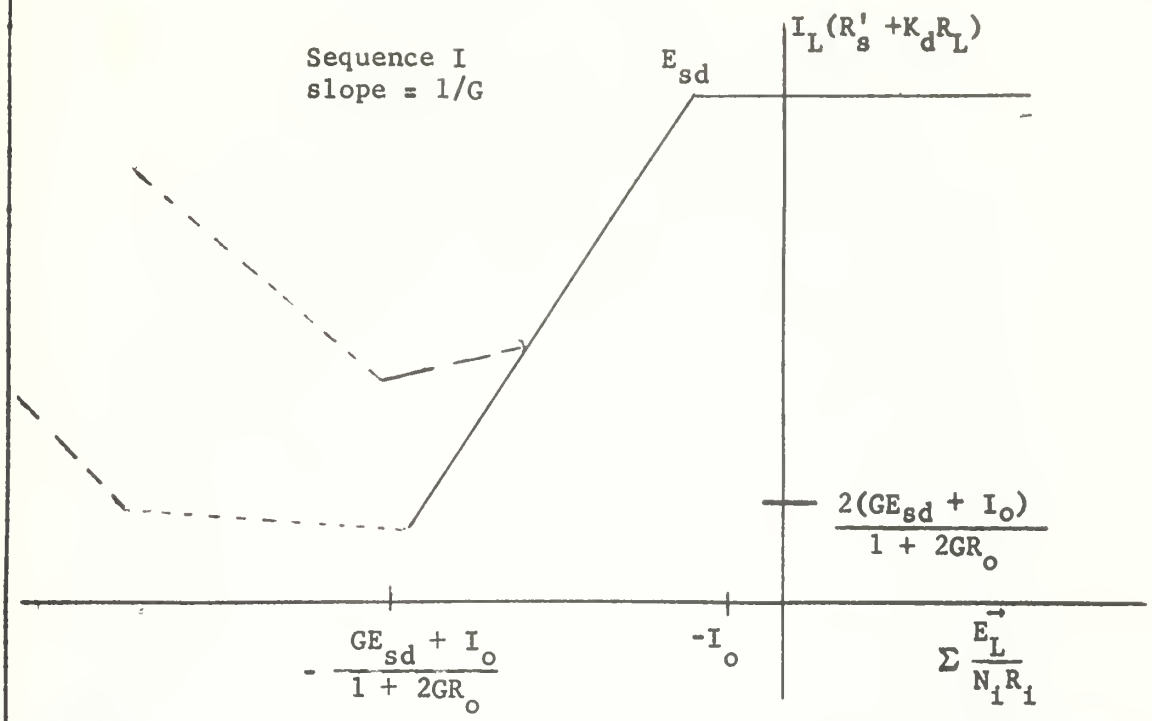


Figure 7.1: Amplifier Characteristic with only Direct Control Windings.

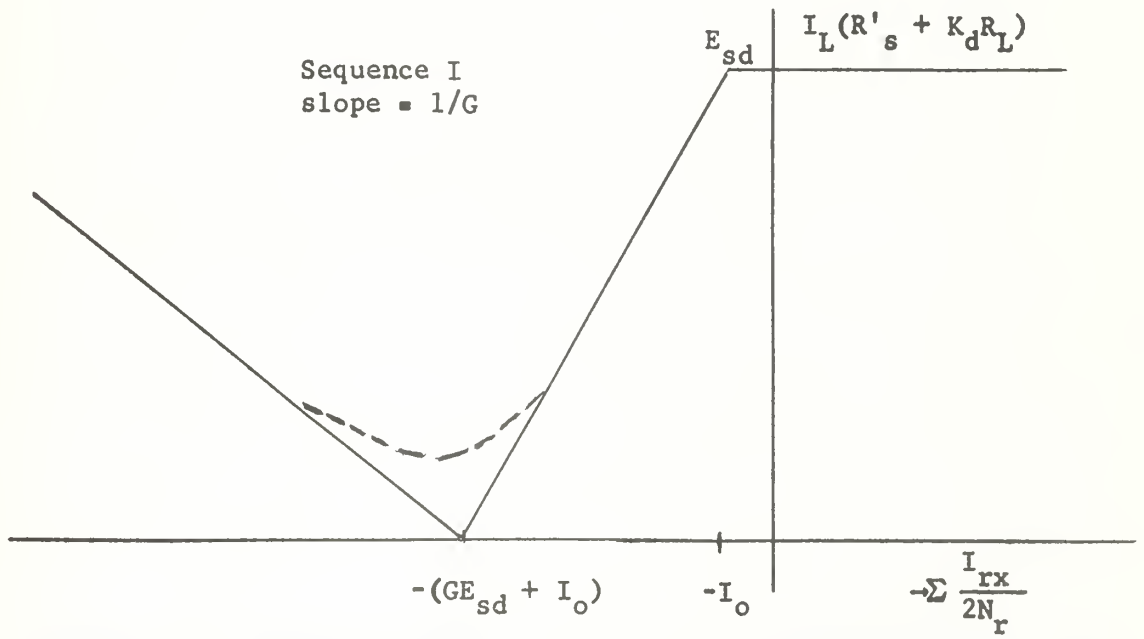


Figure 7.2: Amplifier Characteristic with only Alternating Control Windings.

diode unblocking are not fixed with respect to the characteristic, but are functions of the circuit parameters. In the design of direct controlled amplifiers these inequalities constitute design considerations which may be critical.

For alternating control the minimum theoretical output is zero. However a comparison of the value of control which causes minimum output, with critical values for the diode bias conditions, shows that the diode bias inequalities are violated at very nearly the same value of control as is necessary for minimum output, in the part of the half cycle before the gating core has saturated. Then it is unreasonable to expect that the minimum output of zero is attainable, as the piecewise linearization of the diodes is a poor approximation at small values of currents, and the greatest deviation from theory is to be expected where small diode currents occur.

The theoretical characteristic for a straight alternating controlled amplifier is shown by the solid line in figure 7.2. In laboratory measurements using the center tap output circuit the results were of the form shown by the dashed curve.

The zero output which is theoretically possible for alternating inputs is often desirable in amplifiers. The fact that it is not attainable in practice, or only attainable with difficulty, does not invalidate the foregoing analysis. It indicates that the alternating control circuits are capable of a lower minimum output than are the

direct control circuits. However the alternating control circuits have the unfortunate property of reverse biasing the gate diode, which prevents the zero output point from being reached. The practical conclusion reached was that the use of a small direct bias for alternating circuits will allow a lower minimum, approaching but not reaching zero, and that an alternating bias in direct controlled amplifiers can be used to decrease the minimum output for those circuits.[9]

7.4 Input Circuit Analysis in Mode Sequence I.

In order to determine the input characteristic of the amplifiers an input difference equation is derived in a similar manner to the output difference equation. However as both cores are affected by the input terminal conditions in every half-cycle, it is necessary to use the relation for the reset voltage of the resetting core in each half-cycle. In addition to equation 7.6 in the nth half-cycle, a similar expression for e_g in the $(n + 1)^{st}$ half cycle is required. From equation 4.14 through 4.22 expressions for the core 1 control currents are developed similarly to equations 7.2 through 7.5 with sign changes occuring throughout expressions 7.3 and 7.5, and in the core voltage terms of expression 7.5.

Then solving these new equations with equation 2.13, the counterpart of equation 7.6 is found for the $(n + 1)^{st}$ half-cycle to be:

[9] "Magnetic Amplifiers with A.C. Bias" LtCDR B.W.Compton, Master's thesis in progress at U.S.N.P.G.S.

$$E_g(n+1)=K_1\left[\sum\frac{E_i(n+1)}{N_iR_i}+\sum\frac{E_j(n+1)}{N_jR_j}+\sum\frac{I_{qx}(n+1)}{2N_q}+\sum\frac{I_{rx}(n+1)}{2N_r}+I_o\right]$$

$$-K_2E'_g(n+1) \qquad 7.34$$

For any single direct control loop:

$$N_i\left[E_i(n)-R_iI_i(n)\right]=E_g(n)+E'_g(n) \qquad 7.35$$

and

$$N_i\left[E_i(n+1)-R_iI_i(n+1)\right]=E_g(n+1)+E'_g(n+1) \qquad 7.36$$

And for any single alternating control:

$$N_r\left[2E_r(n)-R_rI_{rx}(n)\right]=E_g(n)-E'_g(n) \qquad 7.37$$

and

$$N_r\left[2E_r(n+1)-R_rI_{rx}(n+1)\right]=E_g(n+1)-E'_g(n+1) \qquad 7.38$$

As the differential amplifier expressions are quite similar they are included at this point. For any single series-differential control loop:

$$N_j\left[E_j(n)-R_jI_j(n)\right]=E_g(n)-E'_g(n) \qquad 7.39$$

and

$$N_j\left[E_j(n+1)-R_jI_j(n+1)\right]=E_g(n+1)-E'_g(n+1) \qquad 7.40$$

And for any single parallel control input:

$$N_q\left[2E_q(n)-R_qI_{qx}(n)\right]=E_g(n)+E'_g(n) \qquad 7.41$$

and

$$N_q\left[2E_q(n+1)-R_qI_{qx}(n+1)\right]=E_g(n+1)+E'_g(n+1) \qquad 7.42$$

It is noted that solutions for the control difference equations for the series and parallel controls are of the same form, and that solutions for the differential arrangements are of the same form. That is, all of the additive

connections will have one form of a difference equation, and all of the differential connections another form. Then it is only necessary to determine the form of the input difference equation for the ordinary amplifier input circuits and the results are applicable, under proper substitutions, to the differential amplifier input circuits.

7.5 Control Circuits for Ordinary Amplifiers.

Eliminating the core voltages from equations 7.1, 7.6, 7.34, 7.35 and 7.36 the input difference equation for a direct control input is found to be:

$$N_i\left[E_i(n+1)-R_iI_i(n+1)\right]-K_2N_i\left[E_i(n)-R_iI_i(n)\right]=K_1\left[\sqrt{\frac{E_i(n+1)-E_i(n)}{N_iR_i}}+\sqrt{\frac{E_j(n+1)+E_j(n)}{N_jR_j}}+\sqrt{\frac{I'_{qx}(n+1)-I_{qx}(n)}{2N_q}}+\sqrt{\frac{I'_{rx}(n+1)-I_{rx}(n)}{2N_r}}\right] \quad 7.43$$

For the alternating control circuit the core voltages are eliminated from equations 7.1, 7.6, 7.34, 7.37 and 7.38 to yield the input difference equation:

$$N_r\left[2E_r(n+1)-R_rI_{rx}(n+1)\right]+K_2N_r\left[2E_r(n)-R_rI_{rx}(n)\right]$$

$$K_1\left[\sqrt{\frac{E_i(n+1)+E_i(n)}{N_iR_i}}+\sqrt{\frac{E_j(n+1)-E_j(n)}{N_jR_j}}+\sqrt{\frac{I'_{qx}(n+1)+I_{qx}(n)}{2N_q}}+\sqrt{\frac{I'_{rx}(n+1)-I_{rx}(n)}{2N_r}}+I_o\right] \quad 7.44$$

Some rather important conclusions may be drawn from the above two equations. For ordinary amplification with the terms with subscripts j and q deleted, the steady state input impedance for direct control is simply the input loop resistance. This is seen by letting all terms $E_i(n+1) = E_i(n)$ and all terms $I_{rx}(n) = - I_{rx}(n+1)$.

However the input voltage at the alternating control terminals does not have a simple relation to the associated current, even in steady state. Hence a phenomenon occurs in these amplifiers, with mixed control circuits, where there is a coupling from the d.c. windings to the a.c. windings but none from the a.c. windings to the d.c. in steady state.

For an amplifier with only a single alternating control winding the steady state control voltage is:

$$E_r = I_{rx} \frac{R_r}{2} \left[1 + \frac{1}{3N_r^2 R_r} \right] + \frac{I_o}{GN_r} \qquad 7.45$$

The effective value of input resistance in steady state may then be much greater than the two resistances R_r in parallel for the alternating controlled amplifier. A comparison of the differential gains in an amplifier for alternating or direct control shows that for a pure resistive load:

$$K_{Ir} = \frac{\Delta I_L}{\Delta I_{rx}} = \frac{1}{2N_r G(R_s' + K_d R_L)} \qquad 7.46$$

$$K_{Vr} = \frac{\Delta E_L}{\Delta E_r} = \frac{R_L}{R_s' + K_d R_L} \quad \frac{N_r}{1+GN_r^2 R_r} \tag{7.47}$$

$$K_{Pr} = K_{Ir}\ K_{Pr} = \frac{R_L}{(R_s'+K_d R_L)^2} \quad \frac{1}{2G(1+GN_r^2 R_r)} \tag{7.48}$$

For the direct controlled amplifier

$$K_{Ii} = \frac{\Delta I_L}{\Delta I_i} = \frac{1}{GN_i(R_s'+K_d R_L)} \tag{7.49}$$

$$K_{Vi} = \frac{\Delta E_L}{\Delta E_i} = \frac{R_L}{(R_s'+K_d R_L)} \quad \frac{1}{GN_i R_i} \tag{7.50}$$

$$K_{Pi} = K_{Vi}\ K_{Ii} = \frac{R_L}{(R_s'+K_d R_L)^2} \quad \frac{1}{G^2 N_i^2 R_i} \tag{7.51}$$

In order to obtain high gains it is necessary to have $GN^2R_c \ll 1$. If this condition is met, then an inspection of the above gain expressions shows that high gains of voltage, current and power are possible for direct control. However the voltage gain for the alternating control is limited to the turns ratio, as was found for the half cycle response circuits. Then the alternating control, while being capable of yielding high current and power gain is limited in voltage gain. This further emphasizes the previous statement that parallel controlled amplifiers are best considered to be current amplifiers.

In considering the use of feedback connections in a doublet amplifier, the above results, (both the input difference equations and the input impedances in steady state), indicate that direct feedback windings are preferable.

First from the input difference equation the alternating input voltage is seen to cause additional interaction with other windings. Secondly the feedback is seen to be less efficient for alternating feedback because of the higher input impedance, coupled with the fact that the parallel control is a current control.

One of the principle advantages of direct controlled amplifiers is the fact that a magnetic feedback may be used to increase the gain without affecting the input resistance in steady state. This is a direct result of the consideration of the direct-control input difference equation. The magnetic feedback is accomplished by supplying an additional winding with a voltage which is proportional to either the load voltage or the load current as desired. If this voltage is fed back in a positive sense, the gain of the amplifier may be increased by an arbitrary amount, even to the extent that the gain becomes negative. The amplifier then exhibits instability with a characteristic similar to a relay with hysteresis.

If positive feedback is adjusted to give infinite gain then the amplifier may be used as an operational amplifier, as described by Geyger[10] in his self-balanced circuits. This is accoumplished by the use of electric feedback in addition to the magnetic feedback.

[10]Geyger, W. A. - Magnetic Amplifier Circuits, Ch. 15 McGraw-Hill, New York, 1957

7.6 Amplifiers with Both Cores Operating in Mode Sequence II.

Mode sequence II is the operation most closely analogous to cut-off operation in electronic amplifiers. If an amplifier is to be operated in this sequence, then its analysis is essential for design considerations. The gain in this region is small in magnitude relative to that of mode sequence I.

Perhaps the most important consideration for the sequence is its limits due to violation of the diode bias conditions. The limits established in the previous section for the cases where the gating core is unsaturated and the resetting core unsaturated are valid also for this sequence. However in this sequence the gating core does not saturate, whereas the resetting core does. When this occurs it is no longer possible to forward bias the resetting core's gate diode, but it is quite possible to reverse bias the gating core's diode when alternating control is used.

The criterion to prevent the gate diode from blocking when the resetting core has saturated is:

$$\sum \frac{e_i}{N_i R_i} + \sum \frac{i_{rx}}{2N_r} - I_o = \left[G + \sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r} \right] e_{sd} \qquad 7.52$$

The above expression, expression 7.28 and the appropriate one from expressions 7.29 through 7.33 must all be satisfied in order that the sequence occur.

The output difference equation for this mode sequence is obtained from the input loop equations as used for the input difference equations of the previous expression, because the core which does not saturate in the n^{th} half-cycle is core 1, and core 2 does not saturate in the $(n+1)^{st}$ half-cycle. The appropriate voltage relation for this sequence is therefore:

$$E_g(n) + E_g(n+1) = 0 \qquad 7.53$$

The core function equations are, for the gating core, in mode C1:

$$i_g + \sum \frac{i}{N} = I_o + Ge_g \qquad 2.15$$

Then substituting all of the control currents and the gate winding current expressions into equation 2.15 for the n^{th} half-cycle

$$E_g(n) = \frac{K_1}{1+\frac{K_1}{R_o}} \left[\sum \frac{E_i(n)}{N_i R_i} + \sum \frac{I_{rx}(n)}{2N_r} + \frac{E_{so}}{R_o} - I_o \right] - \frac{K_2}{1+\frac{K_1}{R_o}} E'_g(n) \qquad 7.54$$

assuming a purely resistive load.

Substituting the control currents and gate currents for the second core into the core function equation for the $(n+1)^{st}$ half-cycle:

$$E'_g(n+1) = \frac{K_1}{1+\frac{K_1}{R_o}} \left[\sum \frac{E_i(n+1)}{N_i R_i} - \sum \frac{I_{rx}(n+1)}{2N_r} + \frac{E_{so}}{R_o} - I_o \right] - \frac{K_2}{1+\frac{K_1}{R_o}} E_g(n+1) \qquad 7.55$$

The output equations with resistive load:

$$E_{sd} - \left[R'_s + K_d R_L\right] I_L(n+1) = E'_g(n+1) \qquad 7.56$$

$$E_{sd} - \left[R'_s + K_d R_L\right] I_L(n) = E_g(n) \qquad 7.57$$

Then solving the above four expressions together with equation 7.53 to eliminate the core voltages the output difference equation is obtained:

$$(R'_s+K_dR_L)I_L(n+1) = \frac{K_1}{1+\frac{K_1}{R_o}}\left[\sum\frac{E_i(n+1)}{N_iR_i} - \sum\frac{I_{rx}(n+1)}{2N_r} + \frac{E_{so}}{R_o} - I_o\right] \qquad 7.58$$

$$+ \frac{K_2}{1+\frac{K_1}{R_o}}\left[R'_s+K_dR_L\right] I_L(n) + \left[1 - \frac{K_2}{1+\frac{K_1}{R_o}}\right] E_{sd}$$

The steady state expression is then:

$$(R'_s+K_dR_L)\ I_L = \frac{-1}{G+\frac{1}{R_o}}\left[\sum\frac{E_i}{N_iR_i} - \sum\frac{I_{rx}}{2N_r} + \frac{E_{so}}{R_o} - I_o\right] + E_{sd} \qquad 7.59$$

The steady state gain for direct control is negative. Expression 5.59 indicates the slope to be positive for alternating control, which is reasonable only if the output remains positive. If the amplifier has been adjusted for minimum output in mode sequence I, then the sequence II operation of alternating control should not be expected to occur except over a relatively small range of values of control.

Typically the dynamic core conductance for power frequencies is in the range of from 10^{-3} to 10^{-6}, so that it may be expected that $1/R_c$ is the dominant term in the co-

efficient of the control terms of equation 5.59. If this is true, then for all output circuits except the semi-bridge $R_s'+K_dR_1=R_o$, and the current gain to be expected is simply the turns ratio for direct control, and half the turns ratio for alternating control.

An examination of the output difference equation shows that there is not a half-cycle delay before an input change affects the output. By analogy with the development of the rise time for mode sequence I the rise time in half cycles is:

$$n_\uparrow = \frac{1}{\ln\left[\frac{1+K_1/R_o}{K_2}\right]} \qquad 7.60$$

In many circuits at power frequencies the rise time is comparable to a half-cycle.

7.7 Design Considerations for Two Core Amplifiers.

The selection of a magnetic core is based on the load requirements for the amplifier. For the amplifier to be able to operate to the minimum output, the core must be able to support the source voltage for an entire half-cycle without saturating. The source voltage is necessarily larger than the maximum required load voltage.

In order that the core be able to support the source voltage for a half cycle without saturating:

$$\frac{E_{sd}}{n_g} T \leq 2\phi_s = 2A_cB_s \qquad 7.61$$

where T is the time of a half cycle and is equal to 1/2f where f is the source frequency. Then

$$E_s \leq 4f\, n_g A_c B_s \qquad 7.62$$

but

$$I_{Lmax}\, R_L < E_s \qquad 7.63$$

therefore

$$4fn_g A_c B_s > I_{Lmax} R_L \qquad 7.64$$

From heating considerations the gate windings must have wire of sufficient cross sectional area that the temperature does not rise significantly above ambient. For amplifiers operated without cooling, the range of current densities is from 0.8 to 1.25 milliamperes per circular mil of wire cross section area. The heating value of the current is its root mean square value. If the current in the gate winding is considered to be purely a pulse-width-modulated current occurring on alternate half-cycles of the source, then for maximum output the wave form is shown in figure 7.3(a), and for half the maximum output as in figure 7.3(b).

For any arbitrary saturation time t between zero and T, the effective heating current is given by

$$I_{eff} = \sqrt{\frac{1}{2T}\int_t^T I_{Lmax}^2 dt} = I_{Lmax} \sqrt{\frac{1}{2}\left(1 - \frac{t}{T}\right)} \qquad 7.65$$

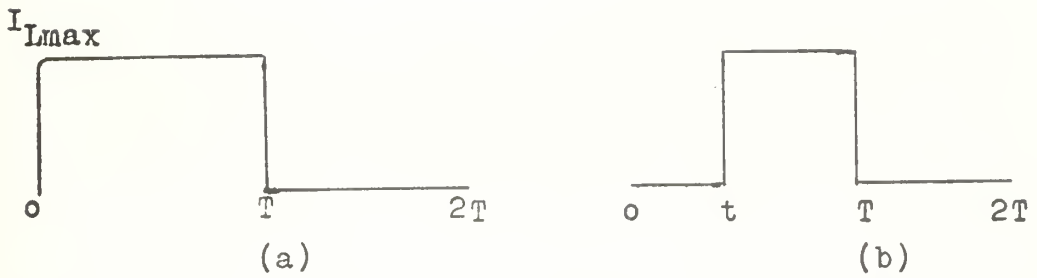


Figure 7.3 Approximate wave forms of gate current for one winding. (a) full output, (b) half output.

If the duty cycle of the amplifier is well known then the average current is known, and the wire size selected. For an amplifier operating in only the linear range (mode sequence I) the average effective current is taken from the case where t is T/2. Then the effective current is 1/2 of I_{Lmax}. The above is true only in those cases where the load and gate current are identical, which rules out the semi bridge. However a similar criterion based on the percentage of gate current going to the load may be developed.

The effective heating current may be written:

$$I_{Leff} = \eta\, I_{Lmax} \qquad 7.66$$

based on either a duty cycle or, for linear amplifiers, the above. A wire size may then be chosen from a table of varnished wire sizes. For a more general method it is assumed that wire sizes vary continuously so that the wire size is based on criterion of one milliampere per circular mil. Then the wire size bears the relation to the heating current:

$$A_{cu} = \frac{I_{Leff}}{.001} \left[\text{circular mils}\right] \qquad 7.67$$

or

$$A_{cu} = 10^3 \eta I_{Lmax} \qquad 7.68$$

The window area of a toroidal core may be filled only to a certain percentage by the windings.[11] The total available window area for machine wound cores may range from 0.3 to 0.6 of the total area. In a magnetic amplifier with bias and feedback windings a reasonable approach is to assign half of the available window area to the gate windings. Then the n_g turns are allowed k_{wg} of the total window area, or

$$n_g A_{cu} = k_{wg} A_w \qquad 7.69$$

and

$$n_g = \frac{k_{wg} A_w}{A_{cu}} = \frac{10^{-3} k_{wg} A_w}{\eta I_{Lmax}} \qquad 7.70$$

If, for a particular design, A_{cu} is determined from current requirements and the above expression does not require equation 7.68, expression 7.64 may then be written:

$$\frac{4f\, k_{wg} A_w A_c B_s}{A_{cu}} = \frac{4f \times 10^{-3} k_{wg} A_w A_c B_s}{I_{Lmax}} \rightarrow I_{Lmax} R_L \qquad 7.71$$

From which the following expression determines the minimum core size which may be used:

$$A_c A_w > \frac{A_{cu} E_{Lmax}}{4f\, k_{wg} B_s} = \frac{P_{Lmax}}{4 \times 10^{-3} f k_{wg} B_s} \qquad 7.72$$

[11] Magnetics Incorporated Catalog TWC 300, Magnetics Inc. Butler, Pa. 1962 pp 17, 60 & 61.

In a basic circuit, that is one with only a single control winding, the gain and rise time are opposing functions, in that an increase of gain corresponds to an increase in time constant. If a design of a more complicated circuit, with multiple controls including bias and feedbacks is used, then the ratio of gain to bandwidth is invariably less than for the basic circuit. Therefore the basic circuit of a single control gives the highest attainable ratio of gain to time constant. This basic circuit is then used to develop a criterion for selecting the largest permissible core which may be used to meet gain and rise time specifications. If the gain and rise time, or the associated bandwidth, are specified, then the development begins with the rise time, which is independent of whether voltage or current relations are required. The rise time is given by:

$$\tau = n_t T = \frac{n_t}{2f} = \frac{1}{2f}\left[1 + 1/\, n^1/K_2\right] \qquad 7.73$$

Then

$$\ell n^1/K_2 = \frac{1}{2f - 1} \qquad 7.74$$

or

$$K_2 = \mathrm{EXP}\left\{ - \, 1/(2f - 1)\right\}$$

From the definition of K_2

$$K_2 = \frac{\sum 1/N_i^2 R_i + \sum 2N_r^2 R_r}{G + \sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r}} \qquad 7.75$$

or

$$G = \frac{1-K_2}{K_2}\left[\sum \frac{1}{N_i^2 R_i} + \sum \frac{1}{2N_r^2 R_r}\right] \qquad 7.76$$

Considering a single direct control winding, the gain may be written from the characteristic in mode sequence I from figure 7.1:

$$\frac{\Delta I_L \left[R_s' + K_d R_L\right]}{\Delta F_i} = \frac{E_{sd}}{\Delta E_i} = \frac{1}{GN_i R_i} \qquad 7.77$$

From chapter two:

$$G = \frac{\Delta H\, l_c}{4fn_g^2 A_c B_s} \qquad 2.21$$

Similarly to the development of equation 7.62

$$E_{sd} \leqq 4fn_g A_c B_s \qquad 7.78$$

then

$$E_c \leqq \frac{H\, l_c}{4fn_g^2 A_c B_s}(4f\, n_g A_c B_s)\frac{n_g}{n_i} R_i \qquad 7.79$$

or

$$n_i \leqq \frac{\Delta H l_c R_i}{\Delta E_i} \qquad 7.80$$

And from equation 7.76 with a single direct control:

$$GN_i^2 R_i = \frac{n_g}{n_i}\frac{E_i}{E_{sd}} \geqq \frac{1-K_2}{K_2} \qquad 7.81$$

then

$$\frac{n_g \Delta E_i}{\frac{\Delta H l_c R_i}{\Delta E_i}\, 4fn_g A_c B_s} > \frac{1-K_2}{K_2} \qquad 7.82$$

The maximum core size is then determined in terms of the available input power and the rise time:

$$A_c l_c \leq \frac{(\Delta E_1)^2 R_1}{4f\Delta H B_s} \frac{K_2}{1-K_2} = \frac{\Delta P_i \left[e^{\frac{1}{2f\tau - 1}} - 1 \right]^{-1}}{4f\ H B_s} \qquad 7.83$$

Expression 7.83 determines the maximum volume of the core, and thereby limits the maximum core size. Expression 7.72 determines the smallest possible core size in terms of the product of the core cross-sectional area and window area. For a set of specifications involving maximum load power, maximum input power and rise time to be realizable, a core must be able to satisfy both of these inequalities. If the operating frequency is fixed, then the only variable for the designer is the type of core material.

Expression 7.83 determines the maximum core volume for a single direct control winding. If multiple windings are used, then the maximum volume must be less. If alternating control is used the volume will also necessarily be smaller as the input power requirements are greater to obtain full swing of the output as indicated by the power gain expressions 7.48 and 7.51.

7.8 Differential Amplifiers with both Cores Operating in Mode Sequence I.

In differential amplifiers the effective output is the difference between the outputs in two successive half cycles. For direct outputs the appropriate circuits are the doubler and the semi bridge, which then provide a polarity reversible output. The appropriate alternating output circuits

are the incomplete bridge, the bridge, and the centertap. Thus it is seen that the direct outputs have a component of alternating output which must be dissipated in the load, while the alternating output has a direct component which must also be dissipated in the load. With both cores operating in sequence I the unwanted components of output are essentially constant over the linear range of operation. These circuits differ from the half-wave circuits in that the dissipation of the unwanted output is accomplished in the core circuits rather than the load. Another point of difference, the one which makes these circuits valuable, is that the full-wave differential amplifiers may utilize external feedback, which is not the case with the half wave circuits.

The output difference equation (7.7) and the input difference equations (7.43 and 7.44) were derived from a sufficiently general point of view to be used for the differential applications. These were written for the n^{th} and $(n+1)^{st}$ half-cycles, and may be extended to the relation between the $(n+1)^{st}$ and $(n+2)^{nd}$ and half-cycles by observing the basic symmetry of the parallel control circuit and the asymmetry of the series differential control:

$$R_s' I_L(n+1) - K_d E_L(n+1) = K_1 \left[- \left\lceil \frac{E_j(n)}{N_j R_j} + \left\lceil \frac{I_{qx}(n)}{2N_q} + I_o \right] \right.$$

$$+ K_2 \left[R_s' I_L(n) - K_d E_L(n) \right] + (1-K_2) E_{sd} \qquad 7.85$$

$$R_s' I_L(n+2) - K_d E_L(n+2) = K_1 \left[\sum \frac{E_j(n+1)}{N_j R_j} + \sum \frac{I_{qx}(n+1)}{2N_q} + I_o \right]$$

$$+K_2 \left[R_s' I_L(n+1) - K_d E_L(n+1) \right] + (1-K_s) E_{sd} \qquad 7.86$$

The input difference equations for the series-differential connection is seen from equations 7.40, 7.41 and 7.37, 7.38 to be of the same form as for the parallel-differential control relations:

$$N_j \left[E_j(n+1) - R_j I_j(n+1) \right] + K_2 N_j \left[E_j(n) - R_j I_j(n) \right]$$

$$= K_1 \left[\sum \frac{E_j(n+1) - E_j(n)}{N_j R_j} + \sum \frac{I_{qx}(n+1) + I_{qx}(n)}{2N_q} + 2I_o \right] \qquad 7.87$$

and for the next half-cycles

$$N_j \left[E_j(n+2) - R_j I_j(n+2) \right] + K_2 N_j \left[E_j(n+1) - R_j I_j(n+1) \right]$$

$$= -K_1 \left[-\sum \frac{E_j(n+2) - E_j(n+1)}{N_j R_j} + \sum \frac{I_{qx}(n+2) + I_{qx}(n+1)}{2N_q} + 2I_o \right] \qquad 7.88$$

The relations for the parallel are similar to the series connection:

$$N_q \left[2E_q(n+1) - R_q I_{qx}(n+1) \right] - K_2 N_q \left[2E_q(n) - R_q I_{qx}(n) \right]$$

$$= K_1 \left[\sum \frac{E_j(n+1) + E_j(n)}{N_j R_j} + \sum \frac{I_{qx}(n+1) - I_{qx}(n)}{2N_q} \right] \qquad 7.89$$

And for the $(n+1)^{st}$ and $(n+2)^{nd}$ half-cycles:

$$N_q\left[2E_q(n+2) - R_qI_{qx}(n+2)\right] - NK_2\left[2E_q(n+1) - R_qI_{qx}(n+1)\right]$$

$$= K_1\left[-\sum\frac{E_j(n+2) + E_j(n)}{N_jR_j} + \sum\frac{I_{qx}(n+2) - I_{qx}(n+1)}{2N_q}\right] \qquad 7.90$$

K_1 and K_2 were defined after equation 7.6, and for the differential amplifier:

$$K_1 = \frac{1}{G + \sum\frac{1}{N_j^2R_j} + \sum\frac{1}{2N_q^2R_q}} \qquad 7.91$$

$$K_2 = -K_1\left[\sum\frac{1}{N_j^2R_j} + \sum\frac{1}{2N_q^2R_q}\right] \qquad 7.92$$

Solving for the relations between the n^{th} and $(n+2)^{nd}$ half-cycles from the above:

$$R_s'I_L(n+2) - K_dE_L(n+2) = K_1\left[\sum\frac{E_j(n+1)}{N_jR_j} - K_2\sum\frac{E_j(n)}{N_jR_j} + \sum\frac{I_{qx}(n+1)}{2N_q} + \sum\frac{I_{qx}(n)}{2N_q}\right] \qquad 7.93$$

$$+ K_2^2\left[R_s'I_L(n) - K_dE_L(n)\right] + K_1(1+K_2)I_o + (1-K_2^2)E_{sd}$$

For the direct control windings:

$$N_j\left[E_j(n+2) - R_jI_j(n+2)\right] - K_2^2N_j\left[E_j(n) - R_jI_j(n)\right]$$

$$= K_1\left[\sum\frac{E_j(n+2)}{N_jR_j} - (1+K_2)\sum\frac{E_j(n+1)}{N_jR_j} + K_2\sum\frac{E_j(n)}{N_jR_j}\right] \qquad 7.94$$

(Equation continued on next page.)

$$-K_1\left[\sum\frac{I_{qx}(n+2)}{2N_q} + (1-K_2)\sum\frac{I_{qx}(n+1)}{2N_q} + K_2\sum\frac{I_{qx}(n)}{2N_q}\right]$$

$$- 2K_1\left[1+K_2\right] I_o$$

And for the alternating control windings:

$$N_q\left[2E_q(n+2)-R_qI_q(n+2)\right] -K_2^2N_q\left[2E_q(n)-R_qI_q(n)\right]$$

$$= - K_1\left[\sum\frac{E_j(n+2)}{N_jR_j} + (1-K_2)\sum\frac{E_j(n+1)}{N_jR_j} - K_2\sum\frac{E_j(n)}{N_jR_j}\right] \qquad 7.95$$

$$+ K_1\left[\sum\frac{I_{qx}(n+2)}{2N_q} - (1-K_2)\sum\frac{I_{qx}(n+1)}{2N_q} - K_2\sum\frac{I_{qx}(n)}{2N_q}\right]$$

In steady state the outputs in the n^{th} and $(n+1)^{st}$ half cycle are the same. The alternating inputs are constant in magnitude from one half-cycle to the next, but alternate their sign.

Then in steady state the output in the $(n+2)^{nd}$ half-cycle is obtained from equation 7.93.

$$R_s'I_L(n+2) - K_dE_L(n+2)\Big|_{s.s.} = \frac{K_1}{1-K_2}\left[\sum\frac{E_j(n+1)}{N_jR_j} + \sum\frac{I_{qx}(n+1)}{2N_q}\right] \qquad 7.96$$

$$\frac{K_1}{1-K_2} I_o + E_{sd}$$

And in steady state the output in the $(n+1)^{st}$ half-cycle is obtained from equations 7.85 and 7.96.

$$R_s'I_L(n+1)-K_dE_L(n+1)\Big|_{s.s.} = \frac{-K_1}{1+K_2}\left[\sum\frac{E_j(n+1)}{N_jR_j}+\sum\frac{I_{qx}(n+1)}{2N_q}\right]$$

$$+\frac{K_1}{1-K_2}I_o + E_{sd} \qquad 7.97$$

The differential output is one half the difference between the output in the $(n+2)^{nd}$ half-cycle and the output in the $(n+1)^{st}$ half-cycle. Then in steady state the differential output is written:

$$R_s'I_L - K_dE_L\Big|_{eff.} = \frac{K_1}{1+K_2}\left[\sum\frac{E_j(n+1)}{N_jR_j}+\sum\frac{I_{qx}(n+1)}{2N_q}\right] \qquad 7.98$$

From equations 7.91 and 7.92

$$\frac{K_1}{1+K_2} = \frac{1}{G} \qquad 7.99$$

This it is seen that the negative feedback inherent in the series-differential control and straight control windings is an effective positive feedback in differential application. The gain of the differential amplifier is the same as the gain of the ordinary amplifier.

7.9 Control Circuits for Differential Amplifiers.

For the direct control windings in steady state the input relation for the $(n+2)^{nd}$ half-cycle is found from equation 7.94 to be:

$$N_j\left[E_j(n+2) - R_jI_j(n+2)\right]\Big|_{s.s.} = \frac{-2K_1I_o}{1-K_2} \qquad 7.100$$

And the steady state value of the input relations for the $(n+1)^{st}$ half-cycle from equations 7.87 and 7.100.

$$N_j \left[E_j(n+1) - R_j I_j(n+1) \right] \Big|_{s.s.} = \frac{2K_1 I_o}{1-K_2} \qquad 7.101$$

The average input impedance for the direct control is seen to be the control resistance R_j. Though an alternating component appears in the current of the series-differential input circuits, it is of constant amplitude and independent of the control voltage.

The alternating control input relations in steady state for the $(n+2)^{nd}$ half-cycle are found from equation 7.95.

$$N_q \left[2E_q(n+2) - R_q I_{qx}(n+2) \right] \Big|_{s.s.}$$
$$= \frac{-2K_1}{1+K_2} \left[\sum \frac{E_j(n+1)}{N_j R_j} + \sum \frac{I_{qx}(n+1)}{2N_q} \right] \qquad 7.102$$

The steady state input relations for the $(n+1)^{st}$ half-cycle from equations 7.89 and 7.102 are found to be:

$$N_q \left[2E_q(n+1) - R_q I_{qx}(n+1) \right] \Big|_{s.s.}$$
$$= \frac{2K_1}{1+K_2} \left[\sum \frac{E_j(n+1)}{N_j R_j} + \sum \frac{I_{qx}(n+1)}{2N_q} \right] \qquad 7.103$$

The average input voltage is the average magnitude of the above two expressions taking into account that the sign of the input current changes each half cycle:

$$\left|2N_qE_q\right|_{avg} = \left|N_qR_qI_{qx}(n+1) + \frac{2K_1}{1+K_2}\left[\sum \frac{E_j(n+1)}{N_jR_j} + \sum \frac{I_{qx}(n+1)}{2N_q}\right]\right| \qquad 7.104$$

The magnitude of $E_q(n+2)$ is seen to be the same as that of $E_q(n+1)$, if I_{qx} changes sign but maintains its magnitude between the $(n+1)^{st}$ and $(n+2)^{nd}$ half-cycles. The differential control impedance is then:

$$\left.\frac{E_q}{I_q}\right|_{s.s.} = \frac{R_q}{2}\left[1 + \frac{1}{GN_q^2R_q}\right] \qquad 7.105$$

which is of the same form as was found for alternating control of the straight amplifier as given in equation 7.46.

It can be shown, by the same method as was used to determine the rise time for the ordinary amplifier, that if a step change of input occurs in the n^{th} half cycle the change of output in an arbitrary half cycle n+2K is from equation 7.93:

$$R_s'I_L(n+2k)-K_dE_L(n+2k) = K_1\frac{1-K_2^{2k}}{1+K_2}\left[\sum \frac{E_j}{N_jR_j} + \sum \frac{I_{qx}}{2N_q}\right] \qquad 7.106$$

As K_2 is less than one, the final value is obtained by letting K_2^{2k} go to zero. The rise time in half-cycles may then be found by comparing $(1-e^{-1})$ times the final value to

the value 2k half-cycles after the input change. Then the relation is necessarily:

$$1 - K_2^{2k} = 1 - e^{-1} \qquad 7.107$$

or

$$K = \frac{1}{\ell n \frac{1}{K_2^2}} \quad \text{or} \quad 2K = \frac{1}{\ell n \left| \frac{1}{K_2} \right|} \qquad 7.108$$

where 2k is the number of half cycles necessary to obtain $(1-e^{-1})$ of the final change. 2k then corresponds to n_t. The rise time for the differential amplifier is then seen to be essentially the same as for the ordinary amplifier. The lack of the additional one half-cycle is due to the fact that the difference equation used gave outputs in only every second half-cycle.

7.10 Bias considerations for Differential Amplifiers.

For both cores to be operated in mode sequence I it is necessary to supply external bias which affects both cores in the same sense. As was seen in the ordinary amplifier analysis an alternating control tends to reverse bias the output gate rectifier, so that for alternating control the bias should be direct. On the other hand the alternating bias will allow a lower minimum output than the direct bias. Hence for direct controlled amplifiers an alternating bias is somewhate superior. The bias in general should reset both cores to zero flux in their reset half-cycles, so that in the absence of any control the output for each half-cycle is half the difference between the

maximum and minimum outputs.

It is desirable that the bias circuit be of the same type as the control circuits so that it will not cause any regeneration between half-cycles and thereby diminish the effective positive feedback between every second half-cycle. Thus alternating bias should be applied by the series-differential configuration and direct bias by the parallel circuit.

The bias is adjusted to give the maximum linear range of control. When the control is sufficient to prevent one core from having any reset in its reset half-cycle, the output will be maximum for that core in the following half-cycle. During the time that the maximum output is occurring the other core should be completely reset so that in its gating half cycle there will be the minimum output. When the maximum output core is in its reset half cycle it is in core-diode mode A2 and the minimum output core is in its gating period in mode C1. For the minimum output for this second core to occur and for the maximum output to occur in the following half cycle while still maintaining the mode sequence (this is the limit of the sequence), then voltage of the resetting core must remain zero throughout the half-cycle, and the gating core must reach saturation at the instant the half-cycle ends.

In the following half-cycle the output core is saturated, as it was not reset, and the resetting core is in mode A2 throughout the half-cycle. In order that the reset-

ting core be completely reset its average voltage must be the negative of its gating voltage. In steady state these conditions are expressed:

$$E'_g(n) = 0 \qquad 7.109$$

$$E_g(n) + E_g(n+1) = 0 \qquad 7.110$$

From the input and output loop equations and the core mode equations it is can be shown that for a purely resistive load:

$$E_g(n) = \frac{K_1}{1+\frac{K_1}{R_o}}\left[\sum\frac{E_j(n)}{N_jR_j} + \sum\frac{I_{qx}(n)}{2N_q} + \frac{E_{so}}{R_o} - I_o\right] - \frac{K_2}{1+\frac{K}{R_o}}E'_g(n) \qquad 7.111$$

$$E'_g(n) = K_1\left[-\sum\frac{E_j(n)}{N_jR_j} + \sum\frac{I_q(n)}{2N_q} + I_o\right] - K_2E_g(n) \qquad 7.112$$

And with core 2 saturated in the $(n+1)^{st}$ half-cycle

$$E_g(n+1) = K_1\left[\sum\frac{E_j(n+1)}{N_jR_j} + \sum\frac{I_q(n+1)}{2N_q} + I_o\right] \qquad 7.113$$

To account for the bias terms in these expressions the series-differential alternating bias is E_{bj} and it changes sign from the n^{th} to the $(n+1)^{st}$ half-cycle. The parallel direct bias term, (I_{bq}) does not change signs from one half-cycle to the next.

Two general expressions are obtained from the above five equations which relate the maximum output values of input and bias to meet the criterion of maximum linear operation.

$$\sum \frac{E_j(n)}{N_j R_j}\left[2+\frac{K_1}{R_o}\right] - \frac{K_1}{R_o}\frac{E_{bj}(n)}{N_{bj}R_{bj}} + \left(2+\frac{K_1}{R_o}\right)\frac{I_{bq}}{2N_{bq}} - \frac{K_1}{R_o}\sum\frac{I_{qx}(n)}{2N_q}$$

7.114

$$= -\frac{E_{so}}{R_o} - \frac{K_1}{R_o} I_o$$

and

$$\left[K_2+1+\frac{K_1}{R_o}\right]\left[\frac{E_{bj}(n)}{N_j R_j} + \sum\frac{E_j(n)}{N_j R_j}\right] + \left[K_2-1-\frac{K_1}{R_o}\right]\left[\frac{I_{bq}}{2N_{bq}} + \sum\frac{I_{qx}(n)}{2N_q}\right]$$

$$= -K_2\frac{E_{so}}{R_o} + \left[K_2+1+\frac{K_1}{R_o}\right] I_o \qquad 7.115$$

The above are obtained for steady state taking into account the sign changes between half-cycles.

As only two equations are available from the bias criterion it is not possible to solve for the general situation of two biases and two types of controls. The best that can be accomplished is to obtain the relations of bias and maximum input for a single bias and a single type of control.

For direct control with alternating bias the value of bias necessary to give maximum linear range of output is:

$$\frac{E_{bj}(n)}{N_{bj}R_{bj}} = -\left[\frac{K_2}{1+\frac{K_1}{R_o}} + 1 + K_2\right]\frac{E_{so}}{R_o} + \frac{I_o}{1+\frac{K_1}{R_o}} \qquad 7.116$$

And the value of control for the maximum output (negative in this case) is

$$\frac{E_j(n)}{N_j R_j} = -\left[\frac{K_2}{1+\frac{K_1}{R_o}} + 1 + K_2 + \frac{K_2}{1+K_2+\frac{K_1}{R_o}}\right]\frac{E_{so}}{R_o} + I_o \qquad 7.117$$

For alternating control with direct bias , the bias necessary to give the maximum range of linearity is:

$$\frac{I_{bq}}{2N_{bq}} = -\left[\frac{1-K_2}{2\left(\frac{K_1}{R_o} + 1 - K_2\right)}\right]\frac{E_{so}}{R_o} - \left[\frac{\frac{K_1}{R_o}}{\frac{K_1}{R_o} + 1-K_2}\right] I_o \qquad 7.118$$

The alternating control current to obtain the maximum output is:

$$\frac{I_{qx}(n)}{2N_q} = \left[\frac{1 + K_2}{\frac{K_1}{R_o} + 1-K_2}\right]\frac{E_{so}}{R_o} - \left[\frac{1 + K_2}{\frac{K_1}{R_o} + 1-K_2}\right] I_o \qquad 7.119$$

For both of these biases the steady state output for any half-cycle is half the difference between the minimum and maximum output when the control inputs are all zero. The maximum output for any half-cycle is E_{sd}, and to a first approximation the minimum output may be assumed to be zero. Then the approximate expression for bias for either case is found from the difference equation between the n^{th} and $(n+1)^{st}$ half-cycles to be:

$$\left|\frac{E_{bj}}{N_{bj}R_{bj}}\right| \approx \left|\frac{I_{bq}}{2N_{bq}}\right| \approx \left[G + 2\,\frac{1}{N_q^2 R_q}\right]\frac{E_{so}}{2} + I_o \qquad 7.120$$

The inclusion of the bias terms will alter the constants for difference equations for any two half cycles, but will not change the gain as the circuits chosen for the bias are of the same types as the control circuits.

7.11 Differential Amplifiers Operating in Saturation.

If the limits of the mode sequence I region of operation are exceeded without violating diode bias requirements one core remains in saturation while the other operates in mode sequence II. For analysis purposes it is assumed that core 1 is saturated and core 2 operating in mode sequence II. Then at all times $E_g = 0$. This corresponds to positive output.

In the $(n+1)^{st}$ half-cycle core 2 starts at negative saturation and does not saturate positively, remaining in moce C1 throughout:

$$E'_g\,(n+1) = \frac{K_1}{1+\frac{K_1}{R_o}}\left[-\sum\frac{E_j(n+1)}{N_jR_j}+\sum\frac{I_{qx}(n+1)}{2N_q}+\frac{E_{so}}{R_o}-I_o\right] \qquad 7.121$$

Then the output in this half-cycle is independent of the previous half-cycle:

$$R'_sI_L(n) - K_dE_L(n) = E_{sd} \qquad 7.122$$

Then the net output is one half the difference between the n^{th} and $n+1^{st}$ half-cycles:

$$R'_sI_L - K_dE_{L_{eff.}} = \frac{\frac{1}{2}K_1}{1+\frac{K_1}{R_o}} \times$$

$$\left[-\sum\frac{E_j(n+1)}{N_jR_j}+\sum\frac{I_{qx}(n+1)}{2N_q}+\frac{E_{so}}{R_o}-I_o-\frac{E_{bj}(n+1)}{N_{bj}R_j}+\frac{I_{bq}}{2N_q}\right] \qquad 7.123$$

The gain in this sequence is then similar to that of

the cutoff gain for straight amplifiers. This gain has very nearly zero slope, but must be determined for an application where saturated operation is required.

7.12 Mode Sequence Limits for Differential Amplifiers.

In order to maintain proper mode sequence it is necessary for the design to maintain the proper diode bias conditions. The cases of interest are for both mode sequence I and saturated operations. For the saturated operations the possibilities of the diode biasing being violated lie only with the active core operating in mode sequence II. In the gating half cycle it is possible to reverse bias the gate diode when:

$$E_g'(n+1) \geq E_{so} \qquad 7.124$$

In this case, the core voltage in mode C1 is given by equation 7.121. Then in order that the bias assumption be valid:

$$-\frac{E_j(n+1)}{N_j R_j} - \frac{E_{bj}(n+1)}{N_{bj} R_{ij}} + \frac{I_{qx}(n+1)}{2N_q} + \frac{I_{bq}}{2N_{bq}} \leqq$$

$$G + \frac{1}{N_j^2 R_j} + \frac{1}{2N_q^2 R_q} E_{so} + I_o \qquad 7.125$$

where the summations multiplying E_{so} include the appropriate bias terms. Both the alternating bias and direct control tend to prevent the occurance of reverse bias. The only danger then lies in the alternating control, or the alternating bias.

In mode sequence I the possibility of reverse biasing of the output diode can occur in either half-cycle. The direct bias applied through the parallel connections always tend to decrease the possibility of reverse biasing of the gate diode, while the alternating bias tends to cause blocking. The alternating control tends to block the diode of the core having the smaller output, and to oppose blocking of the core having the larger output. On the other hand the direct control has the opposite effect in tending to block the gate diode in the n^{th} half cycle, when positive, and prevent blocking of the gate diode in the $(n+1)^{st}$ half cycle.

With core 1 in mode C1 and core 2 in mode A2 the core voltages are found from equation 7.111 and 7.112 to be:

$$E_g(C1) = \frac{K_1(1+K_2)}{1-K_2^2+\frac{K_1}{R_o}}\left[\sum\frac{E_j(n)}{N_jR_j} + \frac{E_{bj}(n)}{N_{bj}R_{bj}} - I_o\right] + \frac{K_1}{1-K_2^2+\frac{K_1}{R_o}}\ \frac{E_{so}}{R_o}$$

$$+ \frac{K_1(1-K_2)}{1-K_2^2+\frac{K_1}{R_o}}\left[\sum\frac{I_{qx}(n)}{2N_q} + \frac{I_{bq}}{2N_{bq}}\right] \qquad 7.126$$

$$E_g'(A2) = \frac{K_1}{1-K_2^2+\frac{K_1}{R_o}}\left[-(1-K_2+\frac{K_1}{R_o})\left\{\sum\frac{E_j(n)}{N_jR_j} + \frac{E_{bj}(n)}{N_{bj}R_{bj}} - I_o\right\}\right.$$

$$\left. + (1-K_2+\frac{K_1}{R_o})\left\{\sum\frac{I_{qx}(n)}{2N_q} + \frac{I_{bq}}{2N_{bq}}\right\} + K_2\ \frac{E_{so}}{R_o}\right] \qquad 7.127$$

In order that the core 1 diode not block in this time it is necessary that:

$$(1+K_2)\left[\sum \frac{E_j(n)}{N_j R_j} + \frac{E_{bj}(n)}{N_{bj} R_{bj}}\right] + (1-K_2)\left[\sum \frac{I_{qx}(n)}{2N_q} + \frac{I_{bq}}{2N_{bq}}\right] \quad 7.128$$

$$\leq (1-K_2)\, GE_{so} + (1+K_2)\, I_o$$

The relations for the $(n+1)^{st}$ half cycle are similar to the above, so that with proper modification these can be applied. However this is not necessary in general as the information can be obtained by letting the control quantities take on both positive and negative values.

Then equations 7.128 and 7.125 are sufficient to determine the limits of output diode forward biasing.

The problem of reset diode unblocking is considerably more complex. This can occur in one of two situations of which only the first can occur in saturation. Both are possible in the linear region. The first case considered is where the output core is saturated and the reset core is in core-diode mode A2. The appropriate core equation then is:

$$E'_g(n) = K_1 \left[-\sum \frac{E_j(n)}{N_j R_j} - \frac{E_{bj}(n)}{N_{bj} R_{bj}} + \sum \frac{I_{qx}(n)}{2N_q} + \frac{I_{bq}(n)}{2N_{bq}} + I_o \right] \quad 7.129$$

This equation must satisfy the inequalities of table 7.1 when core 1 is saturated.

The second case is where core 1 is unsaturated and E'_g is given by equation 7.127. In this case the inequalities of table 7.1 must hold with the gating core unsaturated.

With gating core unsaturated	$-K_1\left[G+\frac{1}{R_o}\right]\sum\frac{E_j(n)}{N_jR_j}+\left[1-K_2+\frac{K_1}{R_o}\right]\sum\frac{I_{qx}(n)}{2N_q}\geq$
Incomplete Bridge	$-\left\{(1-K_2)\left[G(1-GR_f)+K_2\frac{1}{R_o}\right]+\frac{1}{R_o}\left[1-GR_f+K_2\frac{K_1}{R_o}\right]\right\}(E_s-2V_f)-2\left[G(1-K_2)+\frac{1}{R_o}\right]V_f-\left[(G+\frac{1}{R_o})(K_1+R_f)-GK_2R_f\right]I_o$
Centertap	$-\left\{(1-K_2)[G(1+GR_L)+K_2\frac{1}{R_o}]+\frac{1}{R_o}[1+GR_L+K_2\frac{K_1}{R_o}]\right\}(E_s-V_f)-2[G(1-K_2)+\frac{1}{R_o}]V_f-[(G+\frac{1}{R_o})(K_1-R_w)+GK_2R_L]\ I_o$
Doubler	$-\left\{(1-K_2)[G\{1-G(R_L+R_s)\}+K_2\frac{1}{R_o}]+\frac{1}{R_o}[1-G(R_L+R_s)+K_2\frac{K_1}{R_o}]\right\}(E_s-V_f)$ $-2[G(1-K_2)+\frac{1}{R_o}]V_f-[(G+\frac{1}{R_o})(K_1+R_L+R_s)-GK_2(R_L+R_s)]\ I_o$

Table 7 3a. Conditions to maintain reverse bias on diode of resetting core. Determined for core 2 in the nth half cycle. Results for Bridge obtained by substituting $2V_f$ for V_f in Doubler relations. Results for semibridge obtained by substituting $R_d^2/(R_L+R_d)$ in Centertap relations.

Table 7.3 b.

With gating core saturated	$-\sum \frac{E_j(n)}{N_j R_j} + \sum \frac{I_{qx}(n)}{2N_q} \geqq$
Incomplete Bridge	$- I_o - \frac{1}{K_1} [E_s(1- \frac{R_f}{R_o}) + 2V_f \frac{R_f}{R_o}]$
Center tap	$- I_o - \frac{1}{K_1} [E_s(1+ \frac{R_L}{R_o}) + V_f(1 - \frac{R_L}{R_o})]$
Doubler	$- I_o - \frac{1}{K_1} [E_s(1- \frac{R_s+R_L}{R_o}) + V_f(1 + \frac{R_s+R_L}{R_o})]$

Note: Summations include bias terms.

The limits for the two cases for each type of output circuit, assuming a purely resistive load, are given in table 7.3. It has been assumed in the calculations that when the gating core is unsaturated the gating current is $GE_{so} + I_o$, which is only approximately true.

7.13. Design Considerations for Differential Amplifiers.

The maximum effective output for the differential amplifier is slightly less than half that for the ordinary amplifier, as the output occurs only for half a cycle. The maximum power output is thereby effectively half that of the ordinary amplifier. Thus the design requirements for the minimum core size from the ordinary amplifier development (relation 7.72) may be applied to the differential amplifier by multiplying the right hand side of relation 7.72 by a factor of two. This indicates that for the same power requirements, the core size of a differential amplifier is roughly twice that of an ordinary amplifier.

The gain and rise time for the differential amplifier are essentially the same as for the ordinary amplifier. Then the largest permissible core, considering input power and rise time specifications, may also be obtained from relation 7.83.

CHAPTER VIII. EXPERIMENTAL VERIFICATION

8.1 Dynamic Core Model.

The analysis has been based on the piecewise linearization of the saturable reactor core and that of the semiconductor diodes. To make any comparison of theoretical results with actual amplifiers, it was necessary to establish the models of the nonlinear elements.

The semiconductor diodes used in the experiments were measured and found to have the standard forward voltage drop for silicon of 0.6 volts, and a forward resistance of 0.8 ohms.

The dynamic characteristic of the core was measured by the use of an oscilloscope as shown in the circuit diagram on figure 8.1. The resulting magnetomotive force-time rate of change of flux characteristic, shown in the same figure, was measured while the 400 cycles per second source voltage was varied. The values recorded are the average time rate of change of flux and the average magnetomotive force.

8.2 Parallel Controlled Half-Wave Amplifiers.

The principal result of chapter five was the development of the parallel control circuit. The analysis predicts higher gains with parallel control than with the commonly used series control.

In order to make a comparison between the two types of control circuits the same output circuit, shown in figure 8.2 (a), was used for both control configurations. The half wave bridge output circuit was chosen as it is the most com-

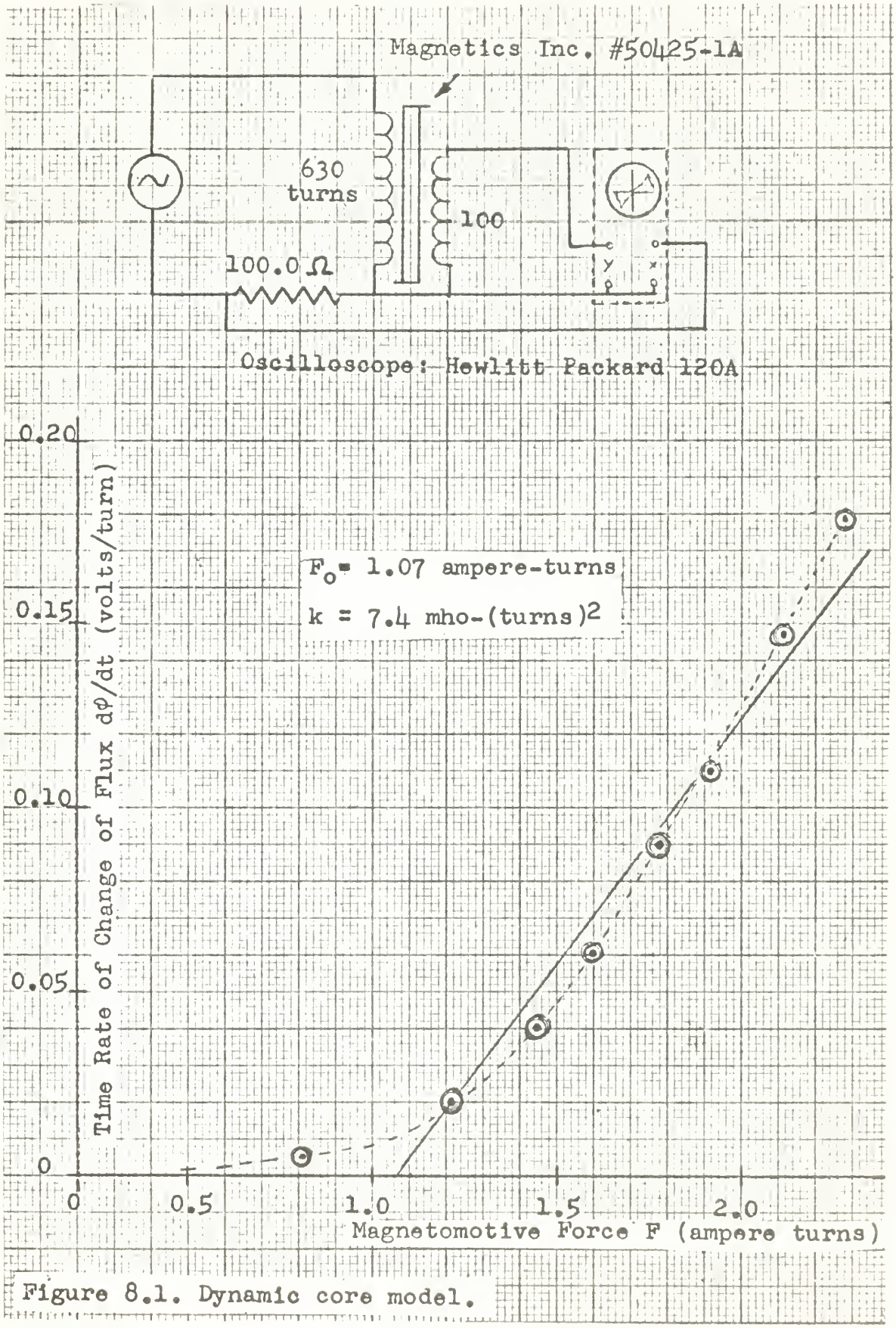


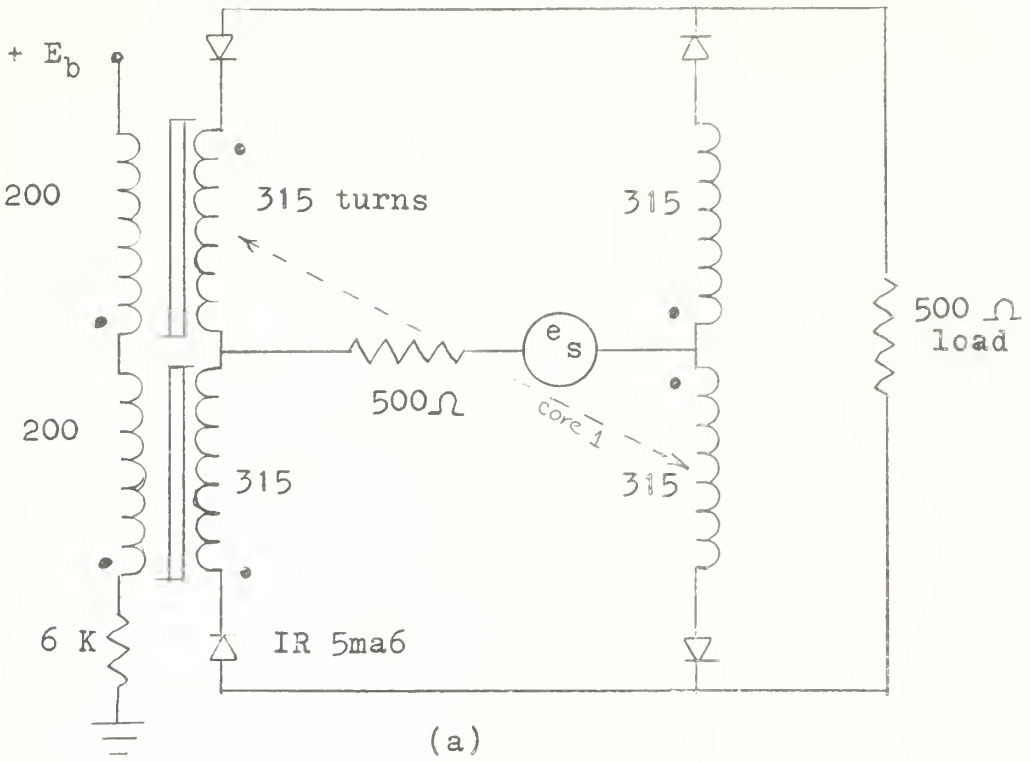
Figure 8.1. Dynamic core model.

monly encountered half-wave figuration. The bias circuit used the series connection as shown in figure 8.2 (a). It was found that a higher value of bias voltage was necessary for parallel control than for series control. The reason for this, while shown in the mathematics of chapter five, is that, in the series control the reflected core voltages in the control circuit oppose each other, while they aid in the parallel control circuit. The parallel control circuit is thereby subject to much larger circulating currents than the series control, and requires greater bias and source power.

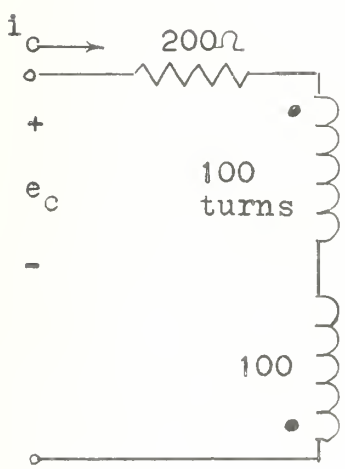
The series control circuit was connected as shown in figure 8.2 (b). The resulting current and voltage gains are shown in figures 8.3 and 8.4 respectively. These characteristics are symmetrical about the origin and only the positive halves are shown.

The parallel control circuit was connected first with a current source which was obtained by the use of a variable voltage source in series with 47,000 ohms (R_x). The parallel control resistances were twice the value of that in the series control in order to maintain the same value of control terminal resistance. The circuit arrangement for the current source control was that of figure 8.2 (c) with the inductor shunting switches closed. The resulting current and voltage gains are shown in figures 8.3 and 8.4 respectively in order to provide a comparison with the series control.

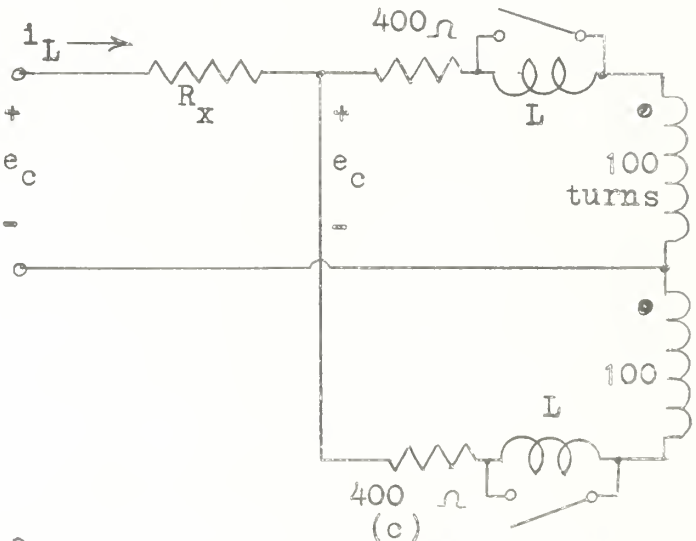
The comparison shows that the current gain of the par-



(a)



(b)



(c)

L = 1 Hy R_w = 1.16 Ω Control circuit resistances inxlude winding resistance.

V_f = 0.6 volts

E_s = 64 volts (half cycle avg.), 400 cps.

5 % Matched cores: Magnetic, Inc. #50425 - 1A

Figure 8.2: Experimental Circuits for Half wave Amplifiers. (a) Bridge output circuit with bias. (b) Series Control arrangement. (c) Parallel control arrangement.

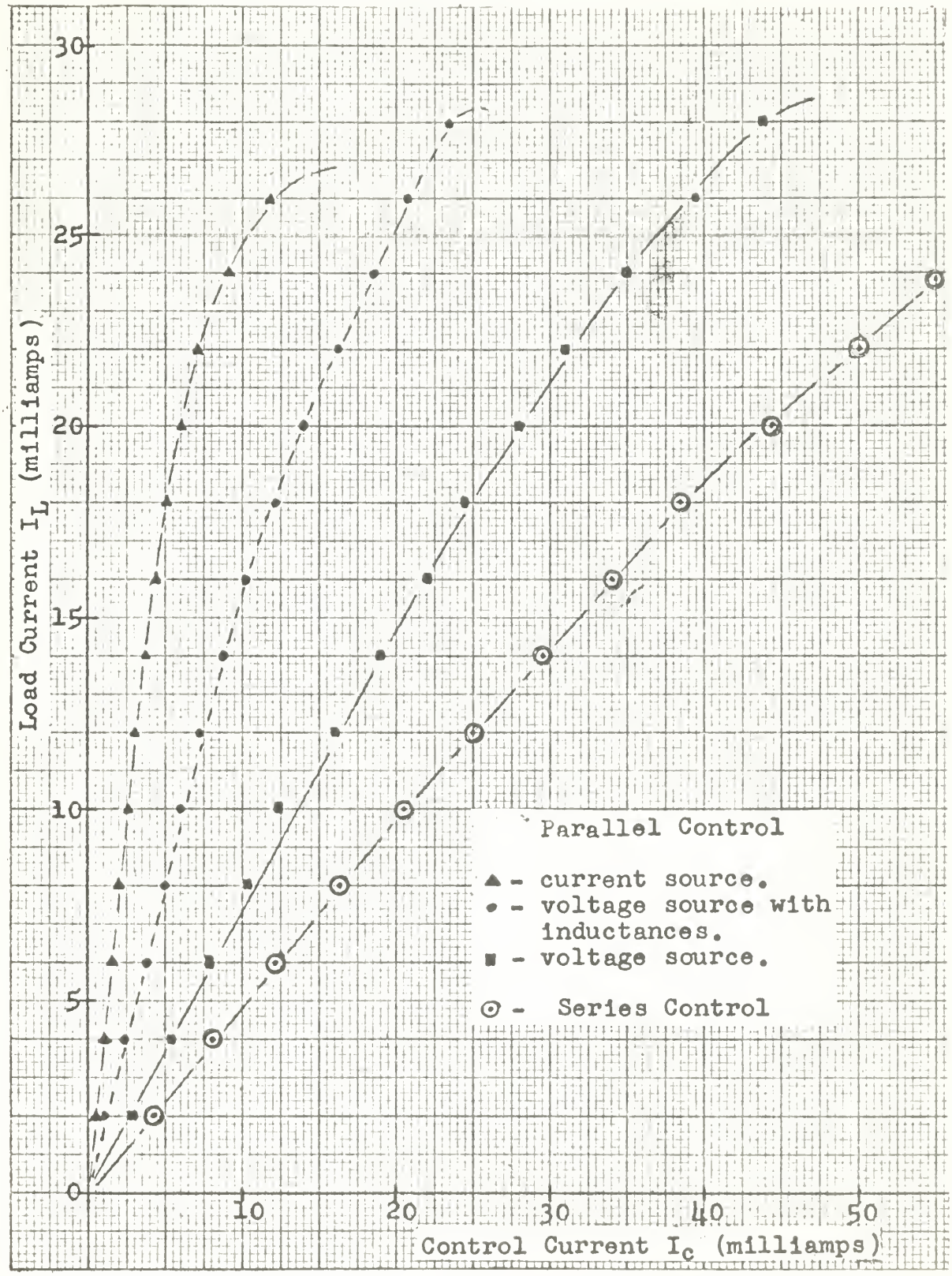


Figure 8.3: Current Gain Characteristics for Half-Wave Bridge Amplifiers.

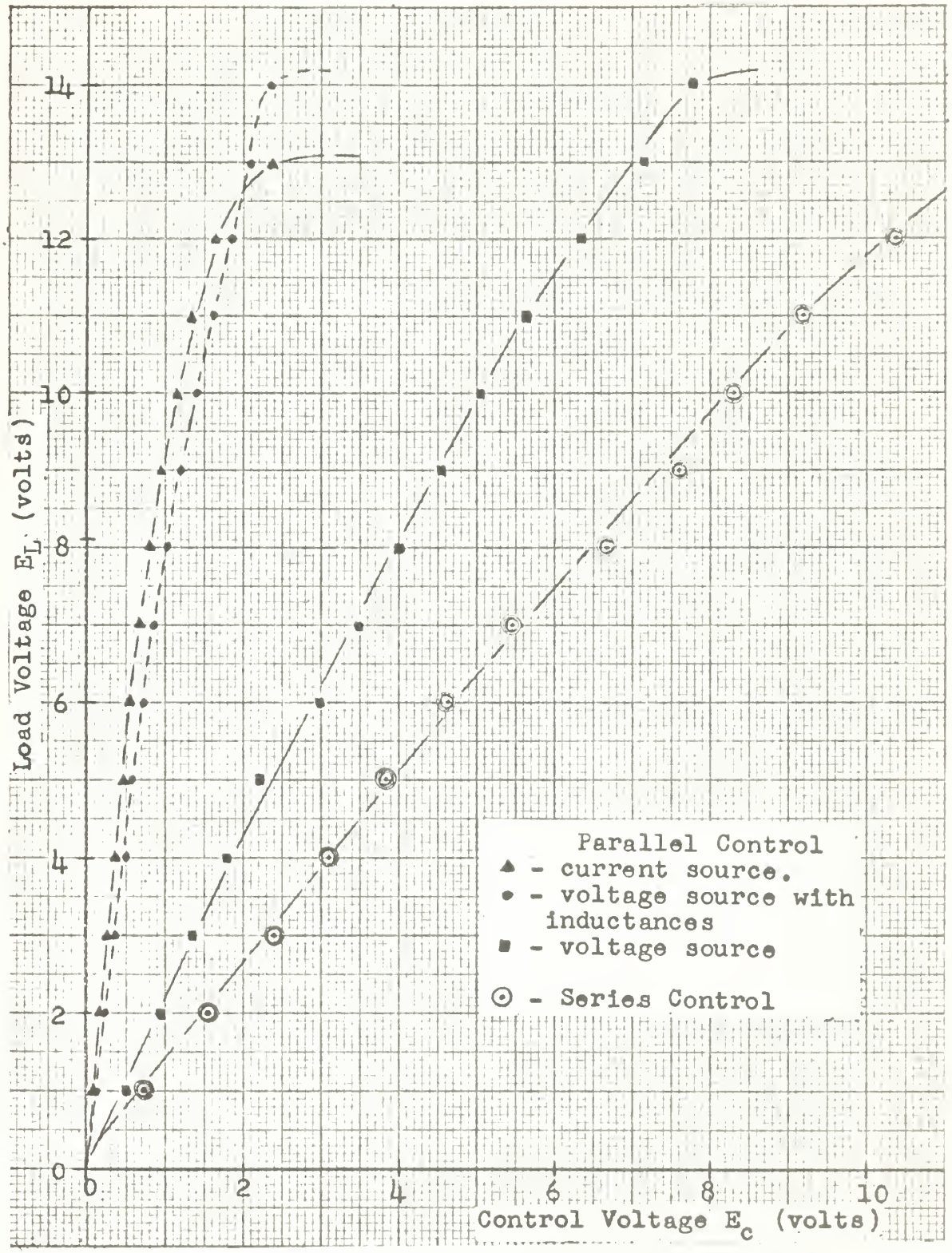


Figure 8.4: Voltage Gain Characteristics for Half-wave Bridge Amplifiers.

allel controlled amplifier was eight times greater than the series controlled amplifier. The voltage gain, considering the control terminal voltage, was about 6.7 times greater for the parallel than for the series controlled amplifier.

The theoretical gains may be determined from equations 5.32 and 5.36.

$$R_o I_L = \frac{NE_j}{2+GN_j^2 R_j} \qquad 8.1$$

$$R_o I_L = \frac{I_r}{GN_r} \qquad 8.2$$

For the bridge $R_o = R_w + 2R_L$. R_w was negligible in this example. The control voltages are related to the control currents by the terminal resistances which were chosen as 200 ohms for both circuits. The dynamic core conductance G, is k divided by the gate turns squared. The gate turns are 630. Then the current gains are:

$$K_{Ij} = \frac{R_j}{2R_L} \frac{N_j}{2 + k\frac{R_j}{N_j^2}} = 0.586 \qquad 8.3$$

$$K_{Ir} = \frac{n_j n_g}{2kR_L} = 4.25 \qquad 8.4$$

The voltage gains are:

$$K_{Vj} = \frac{R_L}{R_c} K_{Ij} = 1.44 \qquad 8.5$$

$$K_{Vr} = \frac{R_L}{R_c} K_{Ir} = 10.6 \qquad 8.6$$

The slopes of the various curves through the origin show that the gains corresponding to expressions 8.3 through 8.6 are 0.5, 4, 1.5 and 10 respectively. The worst prediction occurred for the current gain with series control where the measured value was 17 percent higher than the theoretical value. The others were all within seven percent of theory.

In order to make further comparisons between the series and parallel controlled amplifiers, a voltage source was used to drive the parallel control circuit. The circuit for this case was as in figure 8.2 (c) with $R_x = 0$ and the inductances shorted. It may be shown that the voltage gain for such a circuit is theoretically:

$$K_v = \frac{R_L}{R_o}\left[\frac{N}{1+GN^2R_c}\right] = 2.44 \qquad 8.7$$

Where R_c in this case is the entire 400 ohms. The measured value of gain was 2.15, which is within 12 percent.

It is noted that the current and voltage gains with the voltage drive are substantially greater for parallel control than with series control.

If the impedance of the parallel control circuit is made quite large to the alternating core voltages, while remaining the same to the direct control voltage then the voltage gain can be made to approach that of the current source drive. This was accomplished by placing one henry inductors in series with the control resistors. The resulting voltage gain is shown in figure 8.4 and does become much greater than the case without the inductors. The measured voltage

gain was 8, as compared with 10 for the current source drive.

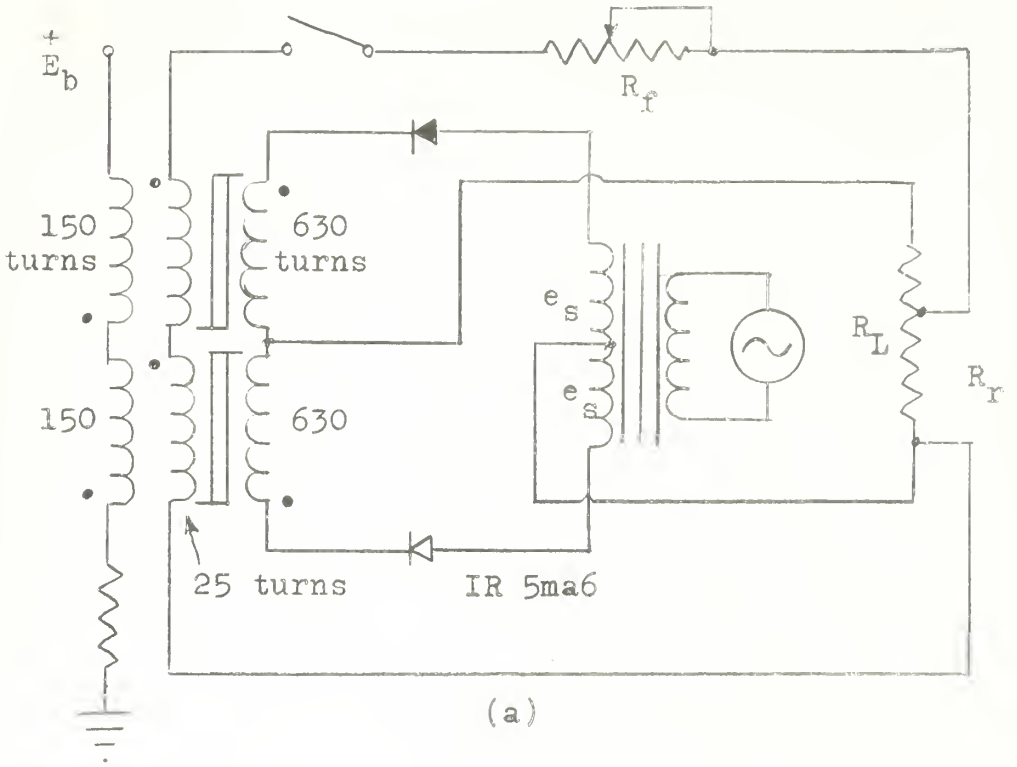
These results verify the analytic technique and demonstrate that the parallel control of these amplifiers is markedly better than the series control from the point of view of gain. The disadvantage of the parallel control is the relatively high circulating current which requires larger control resistance.

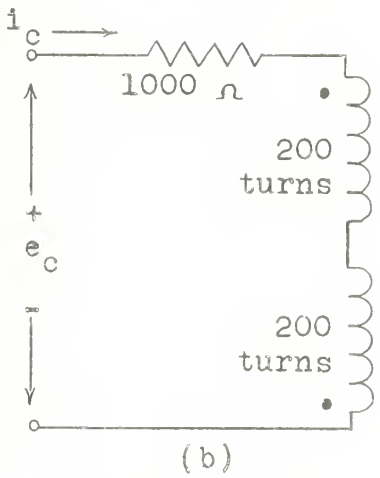
8.3 A.C. Controlled Doublet Amplifiers.

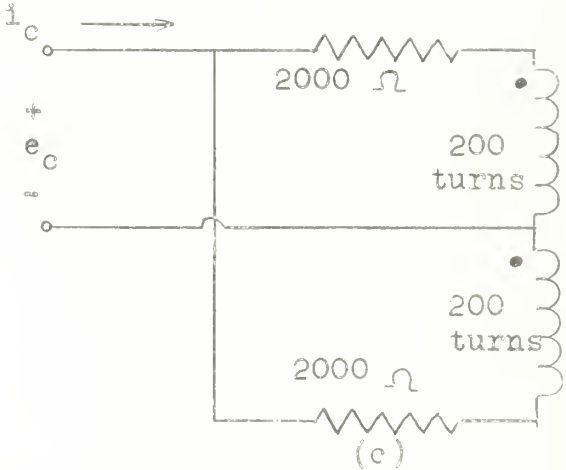
The first new development from chapter seven was that the parallel differential control configuration is superior to series differential control for alternating signals. In order to verify this result two circuits were investigated.

The output circuit chosen for the experiment was the doublet centertap. It was found necessary to supply a direct bias for both cases in order to prevent unfavorable biasing of the output diodes, and achieve minimum output. A positive feedback winding was also included in order to compare the two control configurations in terms of feedback characteristics. The output circuit used for both types of control is shown in figure 8.5 (a).

The series control circuit is shown in figure 8.5 (b) and the parallel control in 8.5 (c). In order to maintain approximately equal control terminal resistances in the two types of control, the parallel resistances were made twice the value of the series control circuit resistance.







R_w = 2 ohms R_L = 200 Ω R_r = 140 Ω

5%. Matched cores: Magnetics Inc. 50425-1A

Figure 8.5: Experimental Circuits for A.C Controlled Doublet Amplifier: (a) Centertap output circuit with bias and feedback windings. (b) Series control circuit. (c) Parallel control circuit.

The control voltage-load current characteristic was measured for both controls and the results are compared in figure 8.6. The parallel controlled amplifier was found to have a voltage gain of about 1.5 that of the series controlled amplifier. The theoretical gain for the parallel controlled amplifier, from equation 7.47 is:

$$K_{\overline{V}r} = \frac{R_L}{R_o}\left[\frac{N_r}{1+GN_r^2R_r}\right] = 2.24 \qquad 8.8$$

A similar expression may be derived for the series controlled amplifier from equation 7.7.

$$K_{\overline{V}j} = \frac{R_L}{R_o}\left[\frac{N_j}{2+GN_j^2R_j}\right] = 1.42 \qquad 8.9$$

The measured voltage gains were 2.17 and 1.41 respectively, which are within four percent of the theoretic values.

The input current-voltage relations were measured as shown in figure 8.7. Over the ranges of linear voltage gain the control terminal impedances are nonlinear. This was indicated in the analysis of chapter seven by the dependence of the input current-voltage relations on the core function G, which is nonlinear, and on the other inputs. The series control current is nearly constant, varying only one and a half milliamperes, which demonstrates that the series controlled amplifier is essentially a voltage controlled device.

The parallel controlled amplifier has a more nearly linear input impedance over the linear range of the amplifier.

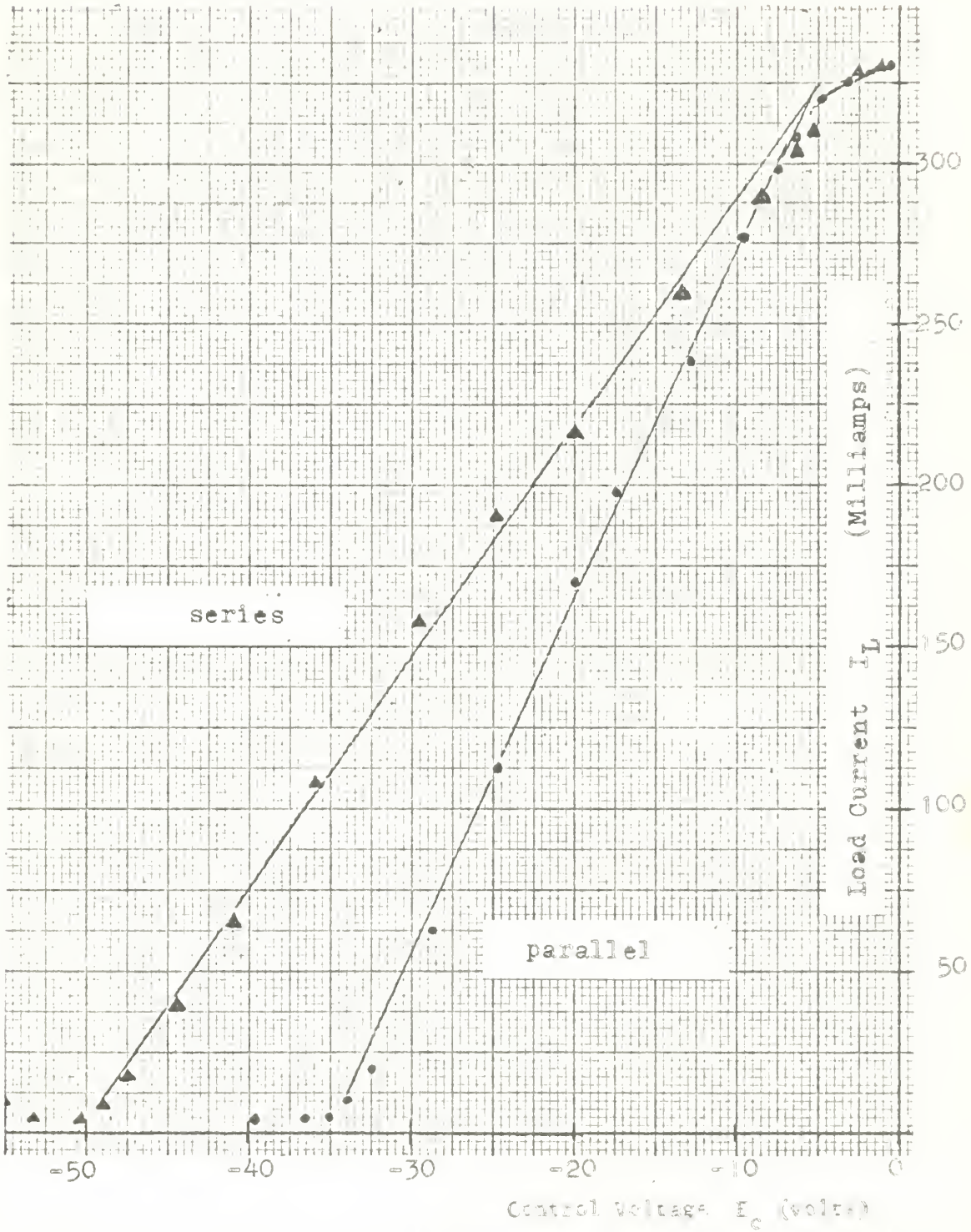


Figure 8.6. Comparison of Gains for Series and Parallel Controlled A.C. Doublet Amplifiers.

For outputs less than two thirds of the maximum it is quite linear. In this region, from 20 to 35 volts of control voltage, the input impedance appears to be 4000 ohms. The corresponding current gain over the region then is 43.4. The theoretical current gain is found from equation 7.46 is

$$K_{Ir} = \frac{1}{2GN_r R_o} = 42.4 \qquad 8.10$$

which is within 2.5 percent.

In order to utilize a magnetic amplifier as an operational amplifier it is necessary to provide very high gain. This can be accomplished with either the series or parallel controlled amplifier by providing positive magnetic feedback. The feedback is most effective when the feedback windings are in series as shown in figure 8.6 (a). If the output were alternating with fixed phase, as in the doubler or semibridge output circuits, then direct feedback may be obtained by using a diode bridge. With either control circuit the positive feedback may be provided to increase the gain up to and beyond infinite gain.

The magnetic feedback was varied by adjusting the feedback resistance R_f of figure 8.6 (a). The results of the magnetic feedback are shown in figures 8.8 and 8.9. The amount of feedback necessary to achieve infinite gain was much less for the parallel than for the series control. In both cases the feedback circuit loads the output circuit as evidenced by the decrease in maximum output with increasing feedback. The necessity of heavier feedback for the series

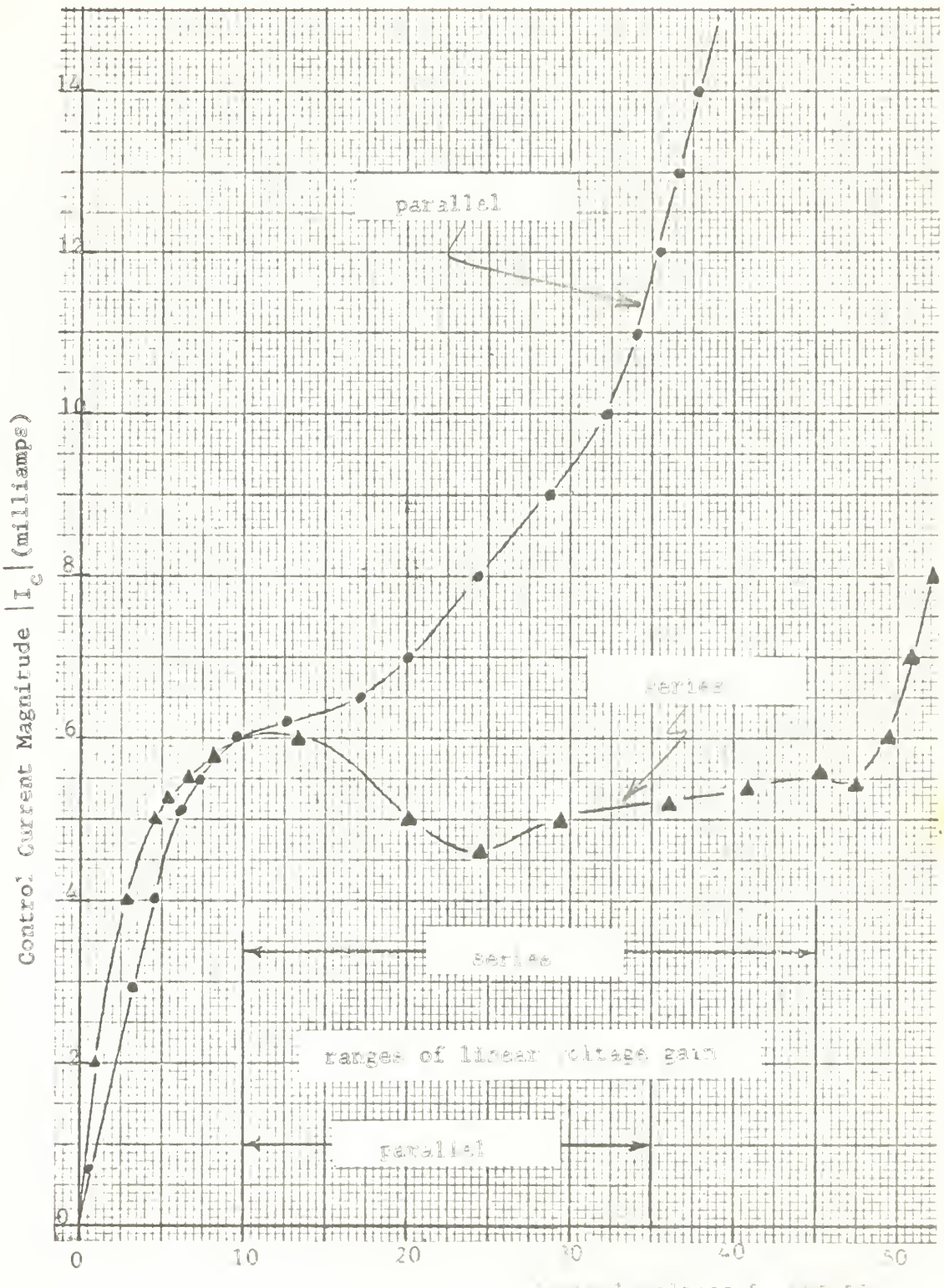


Figure 8.7: Input Characteristics of a Current Controlled Doubler Amplifier

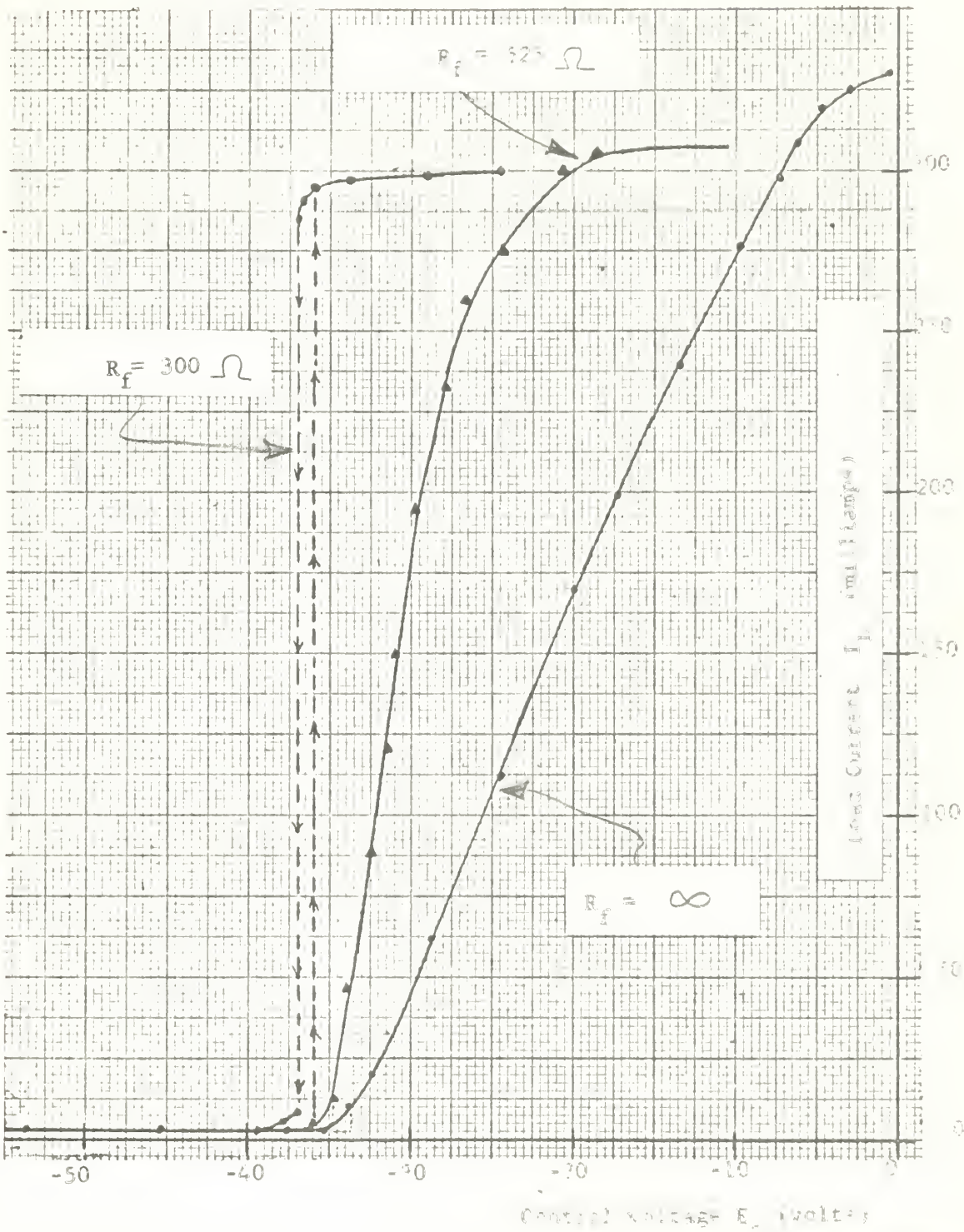


Figure 8.8. Parallel Controlled A.C. Doubler Amplifier Characteristics with Various Amounts of Feedback.

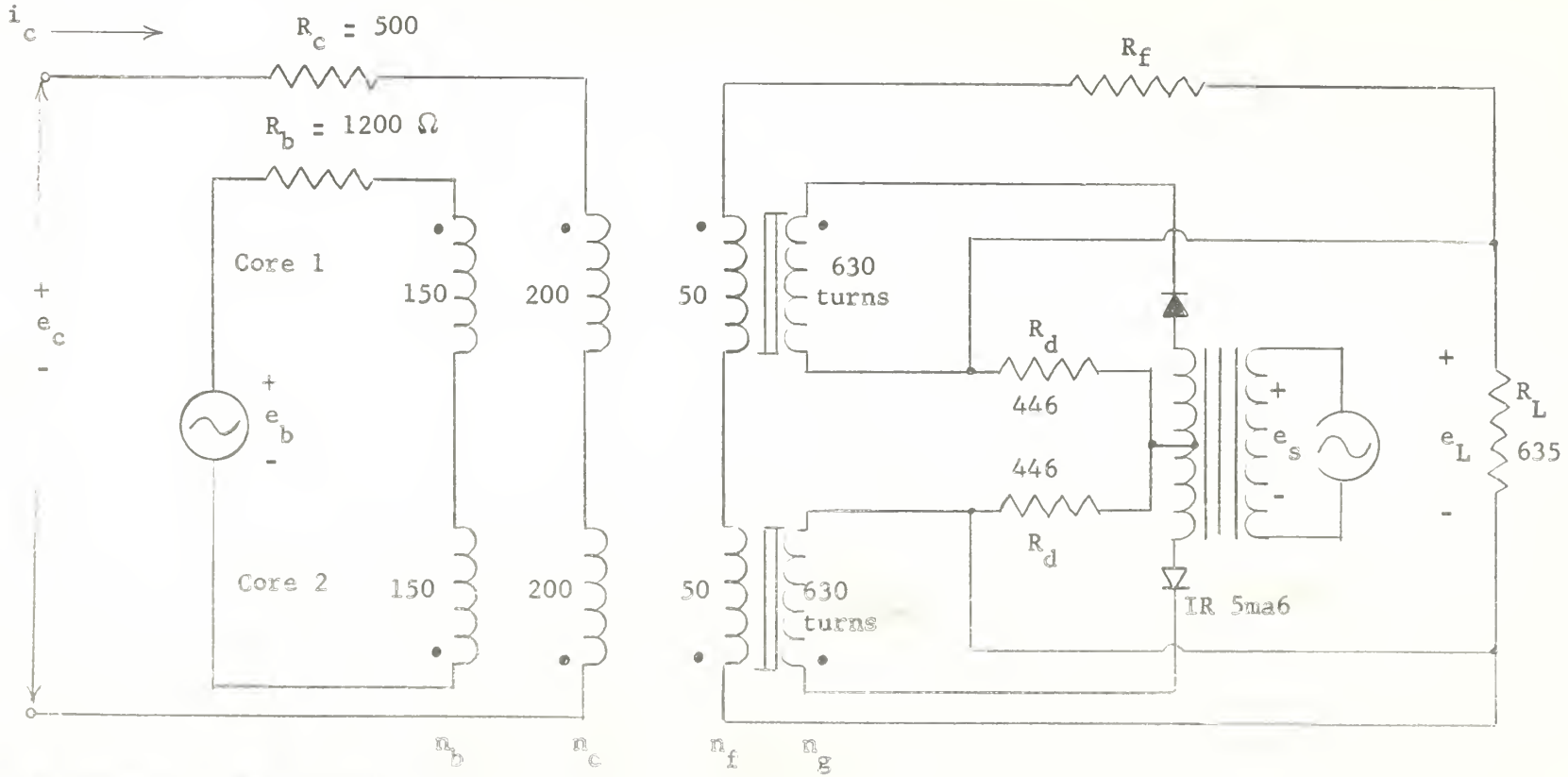
control circuit results in a greater loading and a less efficient circuit than for the parallel control, again demonstrating the superiority of the parallel control for alternating inputs.

8.4 Doublet Differential Amplifiers.

The analysis of doublet differential amplifiers in chapter seven produced the result that, with the use of proper control windings, differential application of doublet amplifiers may produce high gains. Gains of the same order of magnitude as the well known ordinary doublet amplifiers. The analysis indicated that, for direct control the series differential control circuit is the proper circuit, and that bias may be produced with either the series differential control circuit for alternating bias, or the parallel control circuit for direct bias.

The parallel control circuit is a current controlled circuit and requires a very large resistance in series with the bias source in order to attain high gains. For this reason the series differential arrangement was used with alternating bias.

From the point of view of efficiency, the best output circuit for direct polarity reversible output is the doubler circuit. This circuit was first attempted, but was found to operate improperly, as the gate diodes remained forward biased at all times. This phenomenon was predicted in the mode sequence limits of table 7.3. This table also indicates that the bridge circuit is not a use-



57 Matched cores: Magnetics Inc. 50425-1A

R_ω = 30 ohms e_s = 60 volts (half cycle avg.) e_b = 60 volts (half cycle avg.)

Figure 8 10 Experimental Circuit for Doublet Differential Amplifier

ful connection for differential amplifiers.

The doubler circuit may be made to operate properly as a differential amplifier if the diodes are replaced by switching transistors.

For the experimental verification of the analysis the semi-bridge circuit was chosen. The circuit diagram is shown in figure 8.10.

From the analysis of chapter seven the theoretical gain of the circuit is computed from equation 7.98.

$$R'_s \triangle I_L - K_d \triangle R_L = \frac{1}{GN_j R_j} \triangle E_j \qquad 8.11$$

for a resistive load

$$E_L = - I_L R_L \qquad 8.12$$

Then from the definitions of R'_s and K_d from chapter four:

$$\left[R_w (2 + \frac{R_L}{R_d}) + R_L + R_d \right] \triangle I_L = \frac{1}{GN_c R_c} \triangle E_c \qquad 8.13$$

Then the voltage gain is

$$K_v = 19.1 \qquad 8.14$$

The measured value from figure 8.11 with no feedback was 25, which is some 30% higher than the predicted value. With this type of circuit the bias sets the operation point on the flux-mmf characteristic in the higher gain region and a different value of k, somewhat lower than that determined in section 8.1 should be used. If an operating point of 0.1 volt per turn is chosen, the corresponding slope will give a value of 5.6. From this the predicted gain is 23.8 which is about 5% below the measured gain.

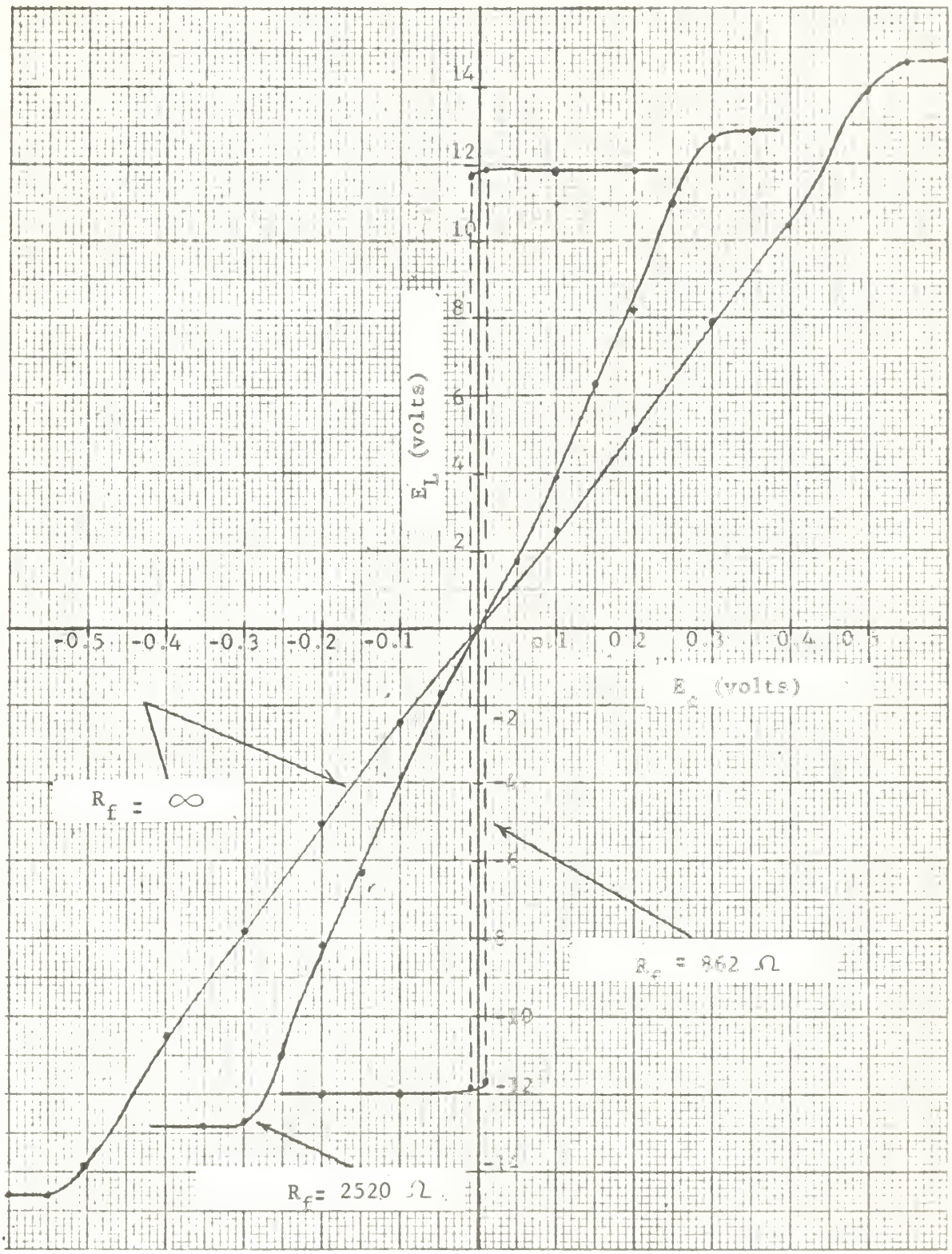


Figure 8.11. Doublet Differential Amplifier with Various Amount of Feedback.

In order to determine the applicability of the circuit as an operational amplifier, positive feedback was examined. The results are shown in figure 8.11. These showed that this circuit may be fed back sufficiently to attain infinite gain. Then the differential amplifier circuit, a result of the general analysis, is a practical push pull arrangement with the same capabilities as the well known single ended doublet circuits.

CHAPTER IX CONCLUSIONS.

From the fundamental operation of a single core self-saturating magnetic amplifier the efficient operating conditions for two core amplifiers were developed. From the topological considerations of two cores, six fundamental control circuits and eight output circuits were developed.

The output circuits were grouped as three half-wave push-pull, and five full-wave configurations. The full-wave circuits may be further classified as three direct and two alternating output circuits.

In considering the half-wave output circuits with various controls, it was found that only control circuits without diodes were applicable. Of these the series and parallel control were determined to be useful only for bias windings, and the differential-series and parallel control suitable only for signal windings. The analysis of the half-wave amplifiers showed that a high gain amplifier was realizable for parallel-differential control and series bias for current source control inputs. This theoretical result was verified in the laboratory.

In order to compare the series and parallel controlled half wave amplifiers under similar signal conditions, both were tested with voltage drive signals. The resulting gains showed the parallel control superior to series control, indicating that the series control should be replaced in practice.

The general analysis of full-wave output, or "doublet"

amplifiers has produced a number of important results. These can be summarized as the best control circuits for various applications. The doublet amplifiers can be divided into two classes, ordinary or single-ended amplifiers, and differential or push-pull amplifiers. Either of these classes may have direct or alternating control, and direct or alternating outputs. In general it was found that for all ordinary amplifiers, regardless of the inputs, the series - parallel-differential control configurations are best. For alternating control the input circuits should be in the parallel-differential form. This was verified experimentally by comparing the parallel-differential with series-differential for alternating controls. The parallel-differential control is capable of providing high gains when the input is a current source, but with a voltage source the gain is still superior to the series-differential connection.

In general parallel-differential control circuits will not yield high gains unless the source impedance is high, and should not be used for bias unless the bias source impedance is comparable to the core dynamic resistance.

In the differential amplifiers the optimum control circuits were found to be the series-differential and parallel connections. The parallel control suffers the same current source restriction as the parallel-differential. It requires high source impedance in order to provide high current gains.

The analysis revealed that for direct control, the dif-

ferential amplifier yields the highest gains when the series differential control is used for signal windings, and the bias should be alternating and applied to a series differential winding. These results were verified in the laboratory and indicate a class of high gain push-pull doublet amplifiers.

Further investigation is needed in several areas. Four core circuits, both single stage push-pull and cascaded two core circuits, should yield to the general analysis presented in chapters four through seven. The effects of active and reactive loading of magnetic amplifiers is not well understood, and design techniques have been limited primarily to laboratory techniques. The general method of analysis should be applicable to these problems. Circuits with active and reactive loads may undergo different mode sequences, which would explain the multiple valued characteristics observed.

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