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DIGITAL ANALYSIS OF THE DELAY-LOCK DISCRIMINATOR

CHARLES S. MULLOY

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OF THE

DELAY-LOCK DISCRIMINATOR

By

Charles S. Mulloy II

Lieutenant, United States Navy

Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

United States Naval Postgraduate School
Monterey, California

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ABSTRACT

The Delay Discriminator, an Optimum Tracking Device, is under current study as a new space tracking system. The transient analysis of this system requires the solution to a non-linear second-order differential equation. The Delay-Lock principle is first explained and the implimentation of this principle is described. Analysis of the system is discussed and a method of digital phase-plane solution is shown. Computer Flow Diagrams and Fortran Source Programs are fully described. With out the aid of a high speed digital computer, the analysis of this system would be difficult, tedious, and inaccurate.

The writer wishes to thank Doctor James J. Spilker and his associates at Lockheed Missle and Space Company for their assistance and encouragement.

The author also wishes to express his appreciation for the many hours of instruction on Computer Systems given him by Professor Mitchel L. Cotton, of the Digital Control Laboratory, U. S. Naval Postgraduate School. In addition, the author desires to express his gratitude to Professor J. B. Turner, Jr., for his helpful comments.

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1. Introduction.

The advent of the space age has created many problems concerned with position measurements and tracking. In this situation, it is sometimes necessary to measure the time delay envolved in sending and receiving a given signal when the target is at great distance and moving at high velocity. The Digital Delay-Lock Discriminator described in this paper is a statistically optimum system which measures the delay between two correlated waveforms and satisfies the above distance and velocity requirements; it mathematically operates in a similar fashion to that of the Phase-Lock System[3]. The Discriminator is a non-linear system incorporating feedback, and attempts to correlate the delay of the return signal with an estimate of the delay generated in the receiver. The Delay-Lock is mathematically described by a second-order non-linear differential equation, whose solution is not readily obtainable by analog methods. The transient analysis of the Delay-Lock Discriminator is the main objective of this paper and will be described fully in a later section.

The following section will present a description of the basic principles of the Delay-Lock System as first described by Spilker[1]; and detail a digital implimentation of this system currently operational at the Lockheed Missle and Space Company's Research Labs. This is followed by an explanation of phase-plane analysis and methods of graphically sketching the transient behavior.

A further section is devoted to a method of dynamic or sequential programming, which allows the computer to step off the operating trajectories in the phase plane. A CDC 1604 High Speed Digital Computer using Fortran Programming provided the transient data which was later plotted.

This paper then describes a new tracking system applicable to many space problems, and presents the transient analysis of its tracking operation.

2. System Operation.

This section is concerned with the basic theory of operation of the Delay-Lock Discriminator as described by Spilker[1]. A description of the basic principles of the Delay-Lock System will first be presented. After this, a method of generating a pseudo-random sequence to represent the signal is described. In conjunction with this signal is the techniques of autocorrelation to obtain the desired discriminator characteristic. The mathematics of the autocorrelation procedure is then completely detailed. All of the above topics are then encompassed in a description of the operating Digital Delay-Lock Discriminator.

2-1 Theory of the DELAY-LOCK DISCRIMINATOR.

The Block Diagram of the Delay-Lock Discriminator is shown in Fig. 2-1. The system is a non-linear discriminator incorporating a multiplier, a low pass filter, and a variable delay element. This delay element may be ultrasonic, fixed ferrite cores with multiple taps, or as in the case that follows, a shift register operating at variable clock rates.

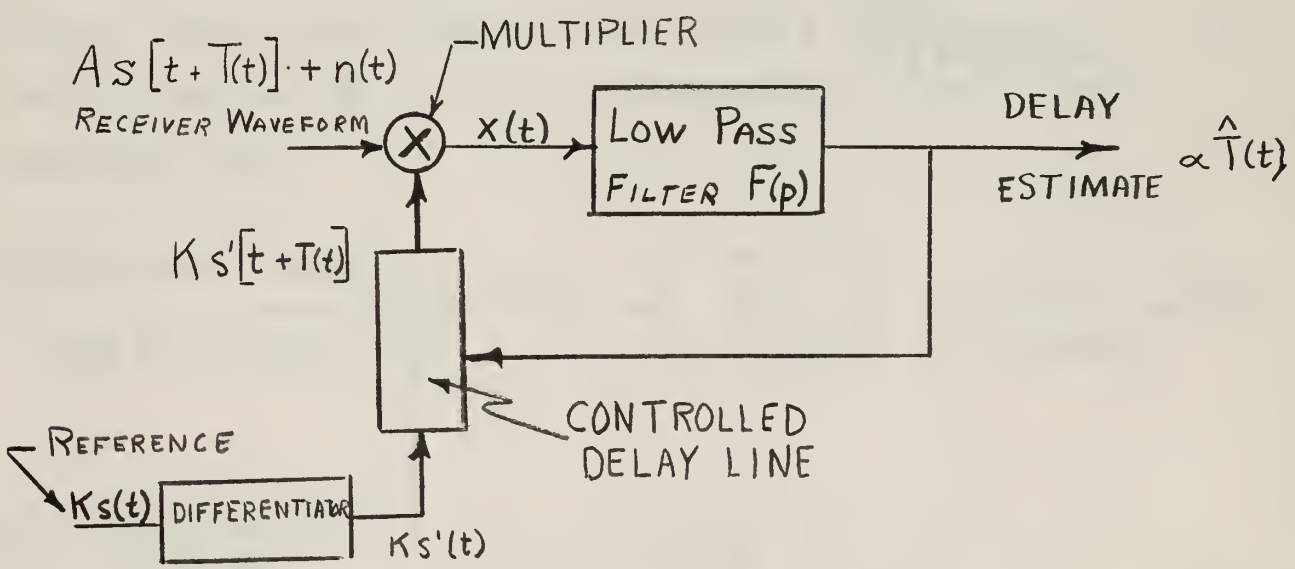

Fig. 2-1 Block Diagram of the Delay-Lock Discriminator. [1]

In an unpublished paper[2], Spilker has shown that this discriminator, or a slightly modified version is a optimum system in that it provides the maximum likelihood (a posteriori, most probable) estimate of delay.

Defining the delay error $\epsilon(t)$ such that $\epsilon(t) = T(t) - \hat{T}(t)$ where $\hat{T}(t)$ is an estimate of $T(t)$ and expanding the delayed signal by Taylor's Expansion produces the following expression:

$$S(t+T) = S(t+\hat{T}) + \epsilon S'(t+\hat{T}) + \frac{\epsilon^2}{2!} S''(t+\hat{T}) + \cdots$$

With $S(t)$ normalized to have unity power it can be shown that the output of the multiplier $\chi(t)$ can be given by:

$$\frac{\chi(t)}{K} = A P_d \epsilon(t) + n_e(t)$$

where $A P_d \epsilon(t)$ is the error correcting term and $n_e(t)$ a noise term.

In viewing the above equation, the basic principle of the discriminator tracking operation is apparent. Consider a sudden increase in the delay time $T(t)$. Such an increase will then increase the initially small delay error $\epsilon(t)$. As $\epsilon(t)$ increases, the correcting term of the multiplier output $\chi(t)$ increases, and thus the estimate of delay $\hat{T}(t)$ will increase and tend to track the input delay.

A partially linearized network in Fig. 2-2 describes the multiplier output. The close loop transfer function $H(P) = \dfrac{F(P)}{1 + KAP_d F(P)/\alpha}$ is linearized when A is constant and describes the locked on region when $\epsilon(t)$ is small.

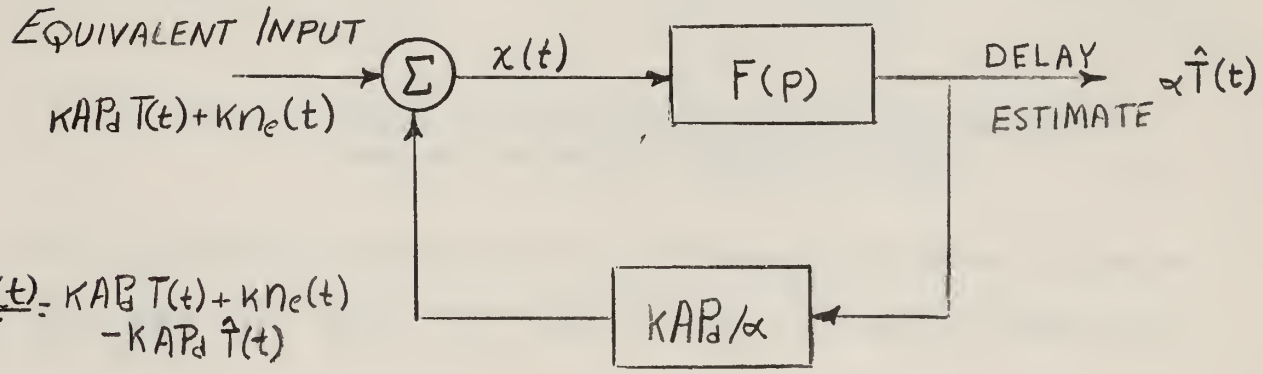

Fig. 2-2 Partially linearized circuit for delay-lock system.[1]

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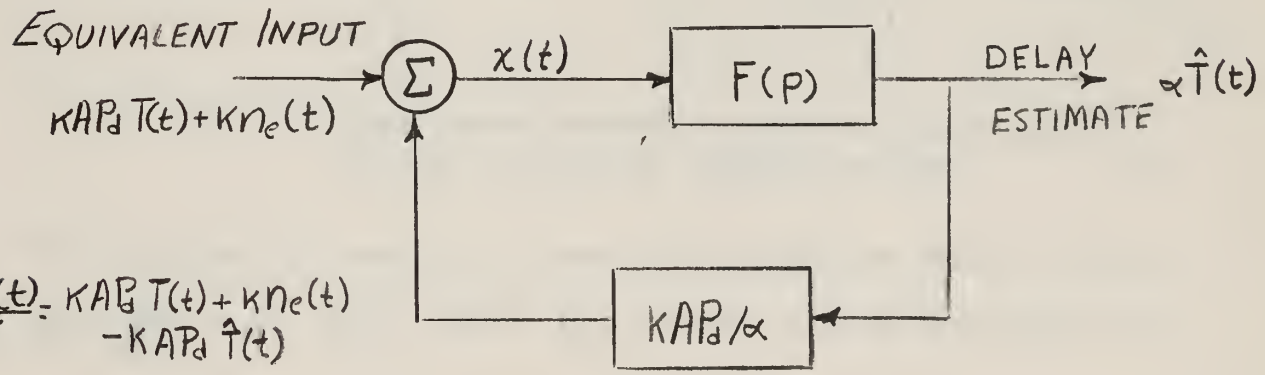


Fig. 2-2 Partially linearized circuit for delay-lock system.[1]

Spilker shows in his paper /1/ that if $S(t)$ is a stationary (wide sense) ergodic random variable with zero mean and slowly varing delays $T(t)$ and $\hat{T}(t)$ the loop filter, when optimized, forms the average of the multiplier output to obtain:

$$E[x(t)] = E\left\{[As(t+T)+n(t)]\, Ks'(t+\hat{T})\right\}$$
$$= -KA R_s'(T-\hat{T})$$

Where $R_s'(T-\hat{T})$ is the derivative of the auto-correlation function of $S(t)$. Hence R_s' is not linearly dependent on the delay error but functionally dependent upon the error through the differentiated auto-correlation function, and thereby causes changes in the effective loop gain.

By considering the discriminator characteristic for a gaussian low-pass signal spectrum, it is possible to examine the threshold of interest. Such a spectrum and corresponding discriminator characteristic is shown in Fig. 2-3.

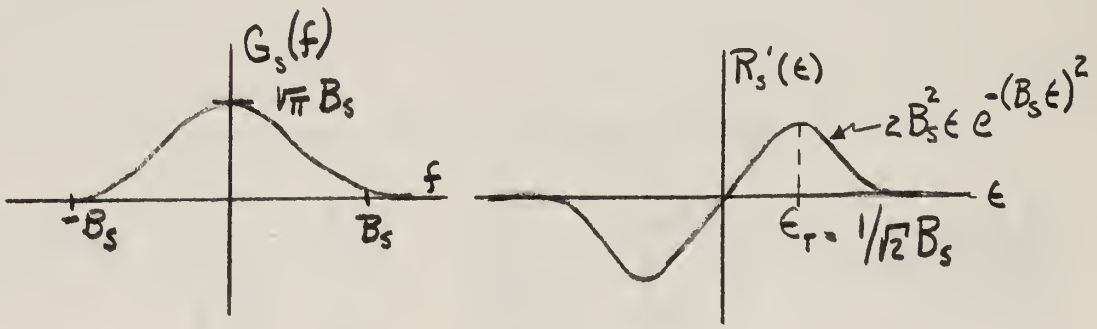


Fig. 2-3 Signal power-spectral density and discriminator function for Gaussian low-pass spectrum. /1/

The discriminator characteristic shows only one lock-on region limited by $|\epsilon_T| = \frac{1}{\sqrt{2} B_s}$. As $\epsilon(t)$ exceeds ϵ_T, the slope becomes negative and

produces a decrease in delay estimate $\hat{T}(t)$; here the system is unlocked and unstable. Since there is only one region of positive slope, there can be no ambiquities in the lock on region and as such, does not possess the limitation in tracking that a sine wave signal contains.

The lock-on performance is more difficult to describe, but when the system contains a simple low-pass RC filter, the mathematics are described by a first-order non-linear differential equation. When neglecting noise terms this equation is as follows:

$$\frac{1}{\omega_f}\frac{d\hat{T}}{\partial t}+\hat{T}=\frac{F(0)}{\alpha}\,z(t)=-gR'_s(T-\hat{T})/P_d$$

In a later discussion, a simplified form of this equation will be used to describe the transient operation of interest. It is well to mention here the loop filter characteristics as proposed by Spilker. The equivalent filter circuit is shown in Fig. 2-4. The loop filter has shown to be optimum for ramp inputs in the presence of white noise, in that is minimizes the total squared transient error plus the mean squared error caused by noise.

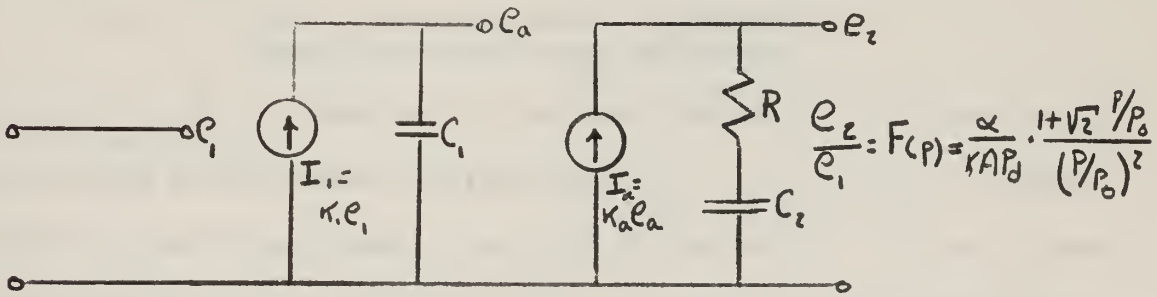


Fig. 2-4 Equivalent loop filter and corresponding transfer function. /1/

The closed loop transfer function for the system is given by:

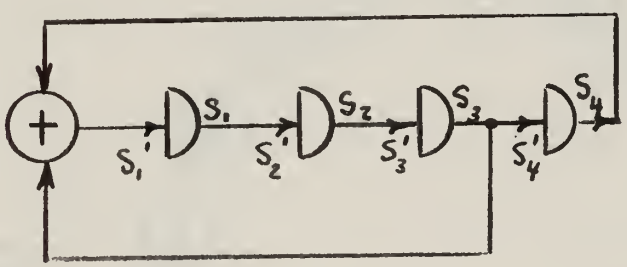
$$H(p)=\frac{\alpha}{KAP_d}\cdot\frac{1+\sqrt{2}\,P/P_0}{1+\sqrt{2}\,P/P_0+(P/P_0)^2}$$

2-2 Generation of the Pseudo-Random Signal.

This section determines to a large extent the form of the digital Delay-Lock System is based on the work of Elspas [4].

A signal with pseudo-random characteristics and of maximum length can be generated with the use of linear feedback shift registers. However, not all feedback shift registers will generate maximum length sequences. The characteristics of various feedback arrangements are contained in a special set of describing polynomials $\phi_i(x)$ which are of particular concern.

In considering the binary linear sequential network as shown in Fig. 2-5, its operating cycle can be expressed by a T matrix.



Half-Adder Operation

1 + 1 = 0
0 + 0 = 0
1 + 0 = 1
0 + 1 = 1
$A*\bar{B} + \bar{A}*B$

Fig. 2-5 Binary linear sequential network with four delay elements and half-adder.

States S_1, S_2, S_3, S_4 describe the internal condition of the network as the four delay element outputs at any time. S_1', S_2', S_3', S_4' describe the inputs to the delay elements, and will be the outputs of these elements, a unit time delay later. Therefore, the S_i' are Mod-2 (half adder) sums of the S_i and the following equations apply:

$$S_1' = S_3 + S_4$$

$$S_2' = S_1$$

$$S_3' = S_2$$

$$S_4' = S_3$$

Expressed in matrix notation, these equations may be represented as follows:

$$\begin{bmatrix} S_1' \\ S_2' \\ S_3' \\ S_4' \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \end{bmatrix}$$

Or, symbolically, as

$$S' = T*S$$

where T is called the T-matrix representation of the network.

Fig. 2-6 shows the state diagram of the present example. The network generates a maximal length sequence (disregarding the all zero state which is trival) representing $2^4 - 1 = 15$ possible states.

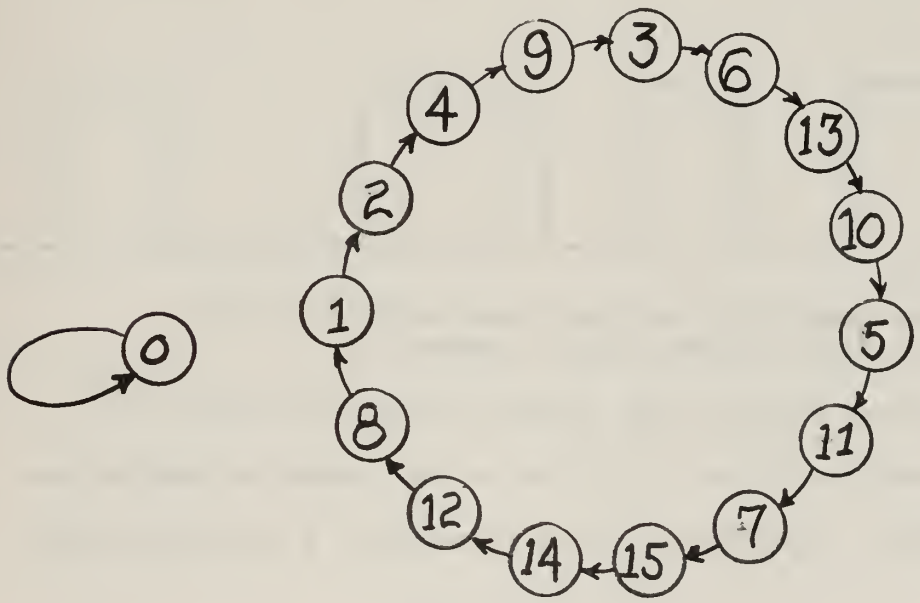


Fig. 2-6 State diagram of network shown in Fig. 2-5.

It is not necessary to examine point by point the different states of the network to determine if any given arrangement will generate maximum length sequences.[4] This important characteristic can be determined from

the network polynomial $\emptyset(x)$, where $\emptyset(x)$ is defined as follows:

$$\emptyset(x) = \left|T - xI\right|$$

or in this present example;

$$\emptyset(x) = \begin{vmatrix} -x & 0 & 1 & 1 \\ 1 & -x & 0 & 0 \\ 0 & 1 & -x & 0 \\ 0 & 0 & 1 & -x \end{vmatrix} = X^4 + X + 1$$

In order for a network to generate a maximal length sequence, its characteristic polynomial $\emptyset(x)$ must be irreducible and not be a divisor of $X^k - 1$ for any interger $k < p^n - 1$ where n is the number of delay elements.

The output of any delay element over the complete cycle period $M\tau$ sec., results in the wave shape shown in Fig. 2-7.

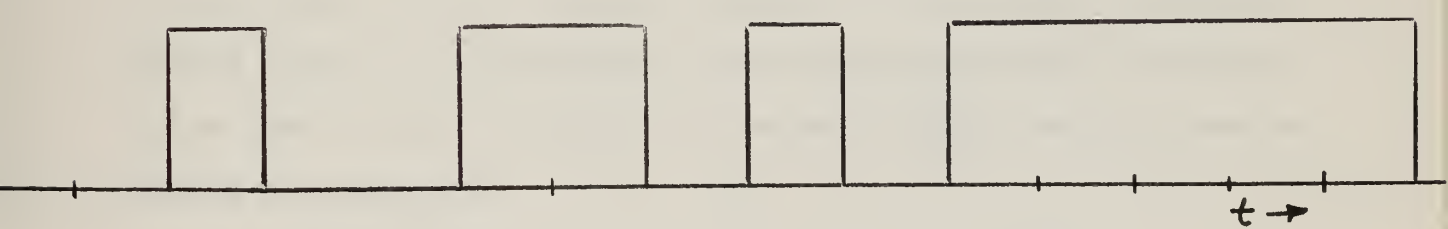


Fig. 2-7 Output wave-form from third delay element of feedback network shown in Fig. 2-5.

It is such a sequential network that provides the desired signal and estimate of delay time in the Digital Delay-Lock Discriminator. This network has a characteristic polynomial $\emptyset(x)$ as follows:

$$\emptyset(x) = X^9 + X^5 + 1$$

This network is shown in Fig. 2-8, and the output from any one delay element constitutes a continuous signal $s(t)$, which has pseudo-random characteristics and a maximum length sequence $M = 2^9 - 1$ or 511 pulses.

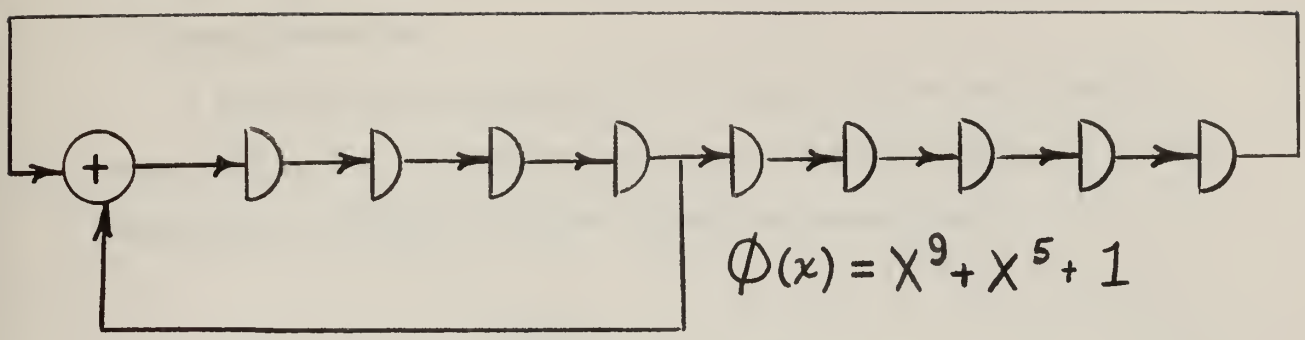


Fig. 2-8 Maximal length sequential network equivalent to linear feedback shift-registers utilized in the Digital Delay-Lock Discriminator.

Although these Sequential Networks have the desirable properties for generating a maximal length pseudo-random signal; there is one characteristic, the auto-correlation function $R_s(\sigma)$, which has yet to be described. The autocorrelation function for the network's sequential output signal will be discussed in the following sub-section and shown to be ideal, in that it results in a unique and highly desirable Discriminator Characteristic.

2-3 Mathematics of the Digital Delay-Lock Discriminator.

The basic delay-lock discriminator tracking system, covered in Section 2-1, can be digitally implemented to track a pseudo-random binary signal generated by linear feedback shift register methods previously mentioned. The advantage of this new system is that the delay line mentioned in the basic delay-lock system, with its limited tracking range, is replaced by shift registers operating at variable clock rates.

As mentioned in Section 2-2, a maximum length $(2^n - 1)$ binary sequence generated by the output of any state m of an n stage linear feedback shift

register is to be the signal, $s_m(t)$. The amplitude of $s_m(t)$ will range from $\pm$ 1, with a pulse width τ producing a sequence period of $M\tau$ seconds. Additive noise effects will in general be ignored in the following discussion.

A simplified block diagram of the digital delay-lock network is shown in Fig. 2-9. The binary sequence plus noise is fed to a limiter network which converts the input signals to binary form.

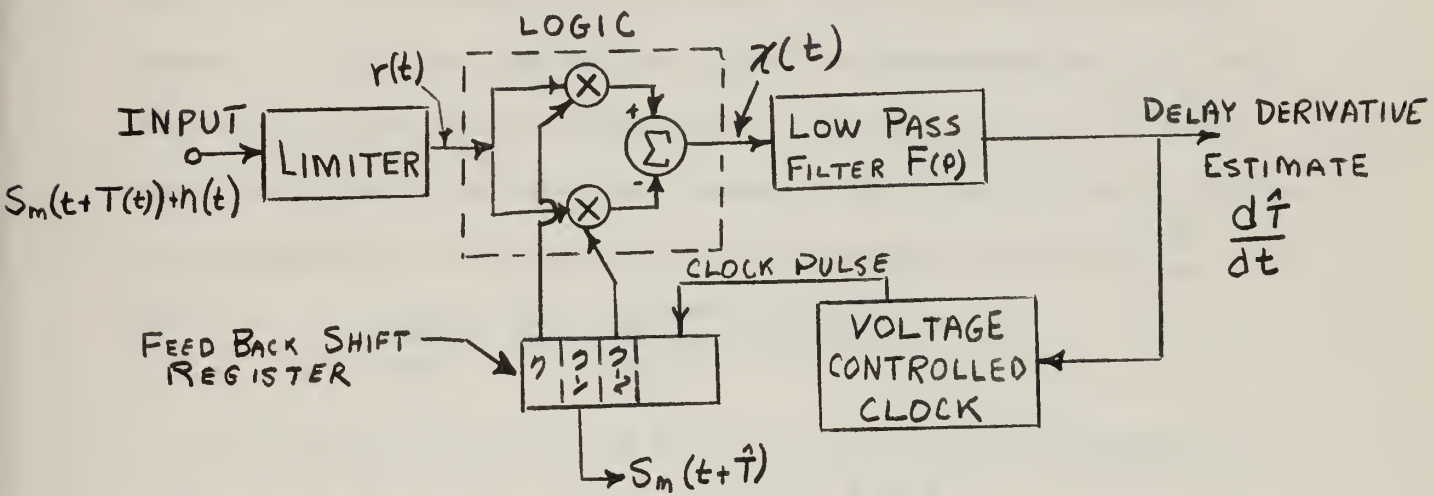


Fig. 2-9 Block diagram of the digital delay-lock discriminator tracking system.

The output of the limiter circuit, r(t), is then fed to the primary logic circuit which consists of two multipliers (AND gates) and a diode resister summing net. The output of the logic circuit, x(t), is basically ternary (+1,0,-1) and has an average value which allows the delay-lock discriminator to track the received signal. The low pass filter following the logic circuit serves to remove as much of the noise and other unwanted signals as possible. The output of the filter, $\dot{\hat{T}}$, is the derivative estimate of the delay time, proportional to the radial velocity of the target reflecting or returning the transmitted signal. This output signal is used to control the clock rate of the receiver shift register.

Comparison of the clock rates of the transmitter and receiver shift registers give a measure of the radial velocity while the Delay is measured directly by comparing the instants when both shift registers go through a specific state, i.e., the [1,0,0,0,0,-----,0,0.] state. Every Mτ seconds a delay measurement is available.

In general, the theory of operation is very similar to that previously mentioned in Section 2-1; that is, the received signal and the derivative of the transmitted signal, having been delayed an estimated time $\hat{T}$, where multiplied to produce an error correcting voltage. However, in this case, the received signal is represented by $s_m(t)$, and the delayed version of it represented by $s_m(t + \tau) - s_m(t - \tau)$; both signals are then to be multiplied together. The delayed signal is similar to the expression of the time derivative of a continuous signal, $\frac{dS}{dt}$ in that:

$$\frac{ds}{dt} = \frac{\lim s(t+\tau) - s(t-\tau)}{2\tau}$$

By defining the delay error $\epsilon(t)$ to be the difference between the True and Estimated delays, $\epsilon(t) = T(t) - \hat{T}(t)$, and neglecting noise, the output of the multiplier logic circuit, x(t), is defined as follows:

$$x(t,\epsilon) = S_m(t+\epsilon(t))\left[S_m(t-\tau) - S_m(t+\tau)\right]$$

Being periodic at intervals $M\tau = 1/f_o$ seconds, the received signal $s_m(t)$ can be represented by a Fourier series such that:

$$S_m(t) = \sum_{n=0}^{\infty} A_{sn}\, Sin(n w_o t) + A_{cn}\, Cos(n w_o t)$$

Corresponding to this expression, the difference $s_m(t + \tau) - s_m(t - \tau)$ can be written as follows:

$$S_m(t+\tau) - S_m(t-\tau) = -2 \sum_{n=0}^{\infty} B_{sn}\, Sin(n w_o t) + B_{cn}\, Cos(n w_o t)$$

where

$$B_{sn} = A_{sn}\, Cos(n w_o \tau) \qquad B_{cn} = A_{cn}\, Sin(n w_o \tau)$$

By combining the three above equations, $x(t, \epsilon(t))$ is as follows:

$$x(t,\epsilon(t)) = D[\epsilon(t)] + y[t,\epsilon(t)]$$

where $D[\epsilon(t)]$ is defined as the Discriminator Characteristic such that:

$$D[\epsilon(t)] \triangleq \sum_{n=0}^{\infty} \left(D_{sn} \sin(n w_0 \epsilon) + D_{cn} \cos(n w_0 \epsilon) \right)$$

and

$$D_{sn} \triangleq -2(A_{sn} B_{cn} - A_{cn} B_{sn}) \; ; \quad D_{cn} \triangleq -2(A_{sn} B_{sn} + A_{cn} B_{cn})$$

The term $y[t, \epsilon(t)]$ can similarly be expressed, and represents the intrinsic noise of the system.

In considering the Discriminator Characteristic, $D(\epsilon)$, it is seen that this delay correction term is not explicitly dependent upon t; its functional behavior is determined by fixing ϵ and averaging $x(t)$. Thus it is apparent that $D(\epsilon)$ is the expected value of the multiplier output such that:

$$D(\epsilon) = E[x(t),\epsilon)] = E\left\{ s_m(t+\epsilon)\left[s_m(t-\gamma) - s_m(t+\gamma) \right] \right.$$

This expected value can be expressed in terms of the autocorrelation function $R_{sm}(\sigma)$ for the binary sequence $s_m(t)$ so that $D(\epsilon)$ becomes:

$$D(\epsilon) = R_{sm}(\epsilon+\gamma) - R_{sm}(\epsilon-\gamma) \; ; \quad \overline{y(t,\epsilon(t))} = 0$$

Thus the Discriminator Characteristic is defined in terms of the auto-correlation functions. As was previously stated, the maximum length sequence has a unique and desirable $R_{sm}(\sigma)$; this function is shown in Fig. 2-10[5]. The Discriminator Characteristic is shown in Fig. 2-11:

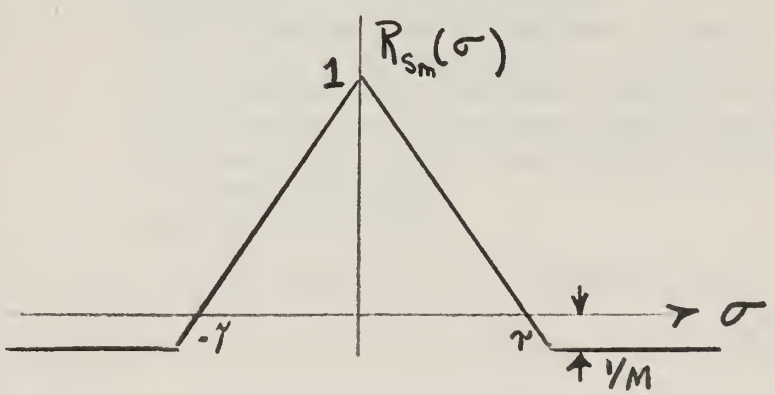


Fig. 2-10 Autocorrelation function for maximal length binary sequence.

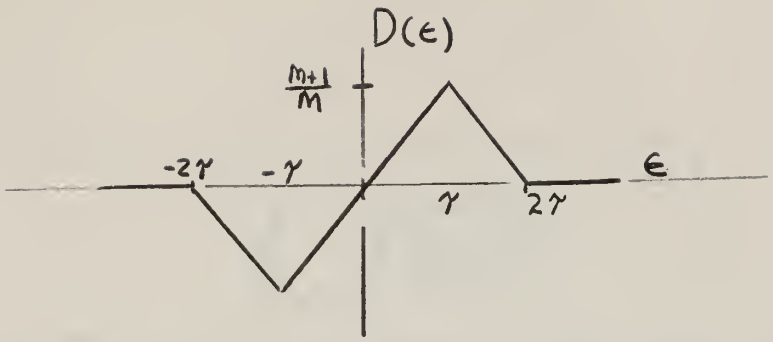


Fig. 2-11 Discriminator characteristic for Digital Delay-Lock Systems

It is apparent that $D(\epsilon)$ provides a correcting voltage in a linear manner when operating in the region $|\epsilon| < \gamma$, decreases to zero at $|\epsilon| = 2\gamma$, and is periodic every $M\gamma$ seconds.

2-4 The Digital Delay-Lock Discriminator

This section describes the operating Digital Delay-Lock Discriminator System built under the direction of Dr. James J. Spilker, Jr., at the Lockheed Missle and Space Company Research Laboratory, Palo Alto, Calif. As shown in Fig. 2-12, the equipment is rack mounted and requires external analog and digital readout for data analysis. The following major components are incorporated in the basic system:

(a) Rack Mounted Oscillascope
(b) Transmitter Output Pannel
(c) Transmitter Shift Register & Logic Circuits
(d) Receiver Output Pannel
(e) Receiver Shift Register & Logic Circuits
(f) Power Control & Voltage Controlled Oscillators
(g) Loop Filter Inputs and Output, and In-lock Tracking Light
(h) Power Supplies

The basic logic cards (AND/OR) which comprise the major portion of the Transmitter and Receiver sections were scrapped from a defunct Polaris Missle check out system and as such do not represent the state of the art

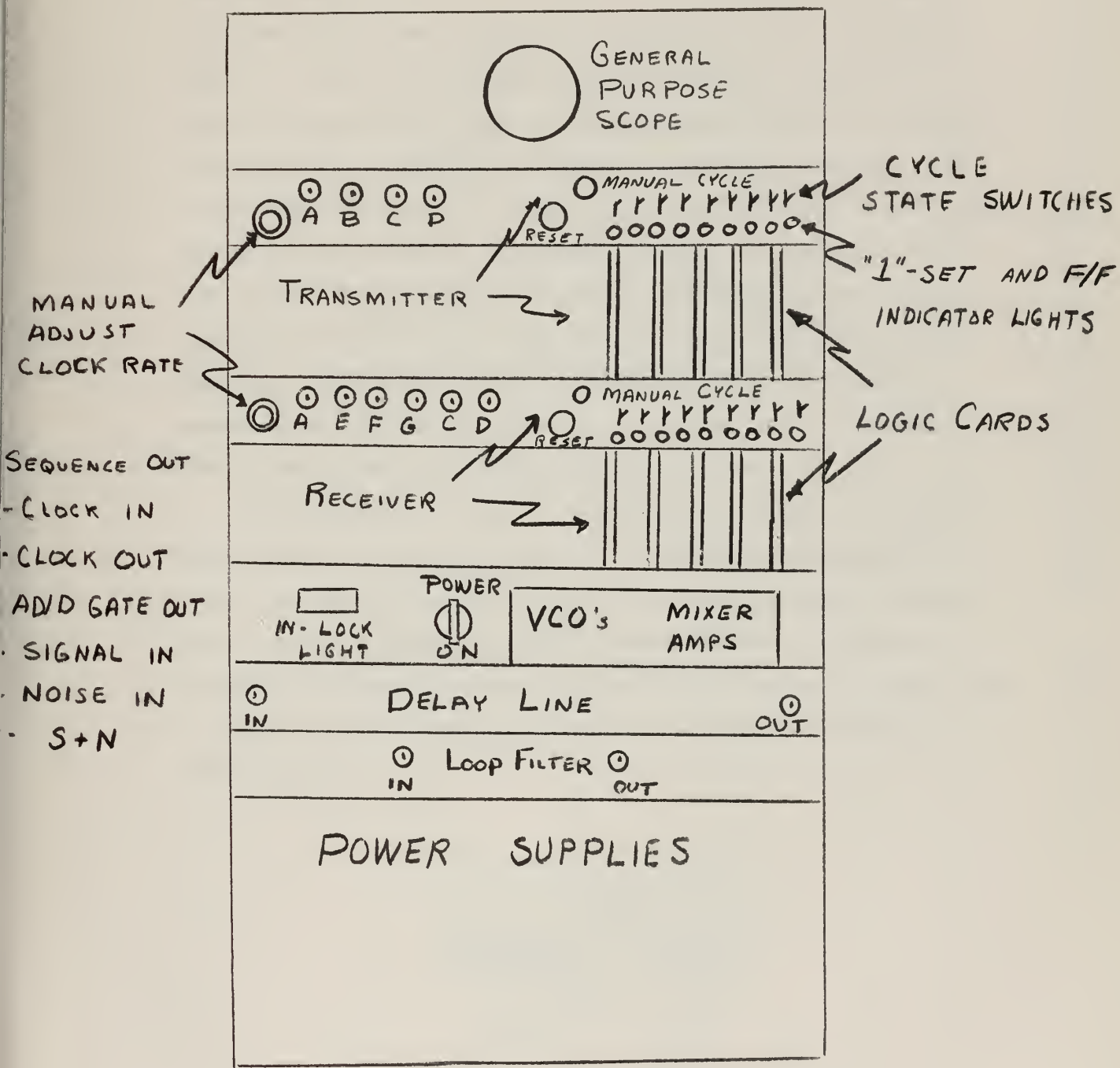


FIG 2-12 DIGITAL DELAY-LOCK SYSTEM

in transistor circuitry; however, they provided an inexpensive method for realizing the delay-lock system. With the exception of the power supplies, the system is completely transistorized; those circuits not available originally were built on blank cards. The basic structure of the Linear Feedback Shift Registers and associated circuits is shown in Fig. 2-14. The primary difference between the two shift registers is that the Transmitter shift register operates with a fixed clock rate while the Receiver Shift register is controlled by a variable clock rate. The clock pulse is generated by a stable crystal oscillator which is fed to a doubler or mixer amplifier. This output is fed to a Schmitt Triger circuit and then fed to a blocking oscillator. The output is then fed to a standard clock-pulse amplifier and then to the clock inputs of the shift register. Although both Voltage Controlled Oscillator networks have a manual control for frequency deviation, the receiver VCO is also adjustable by the voltage from the output of the Loop Filter.

By allowing the difference in clock rates to be large to insure the system would not lock-on and track, the error correcting voltage output from the filter will conform closely to the system discriminator characteristic. When this voltage was fed to an analog plotter, it produced the discriminator characteristic shown in Fig. 2-13. This waveform agrees closely to that predicted for the digital model, the sawtooth discriminator characteristic.

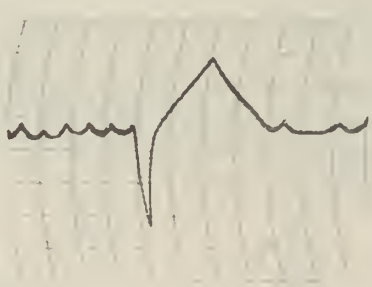


Fig. 2-13 The observed Discriminator Characteristic for the Digital Delay-Lock System

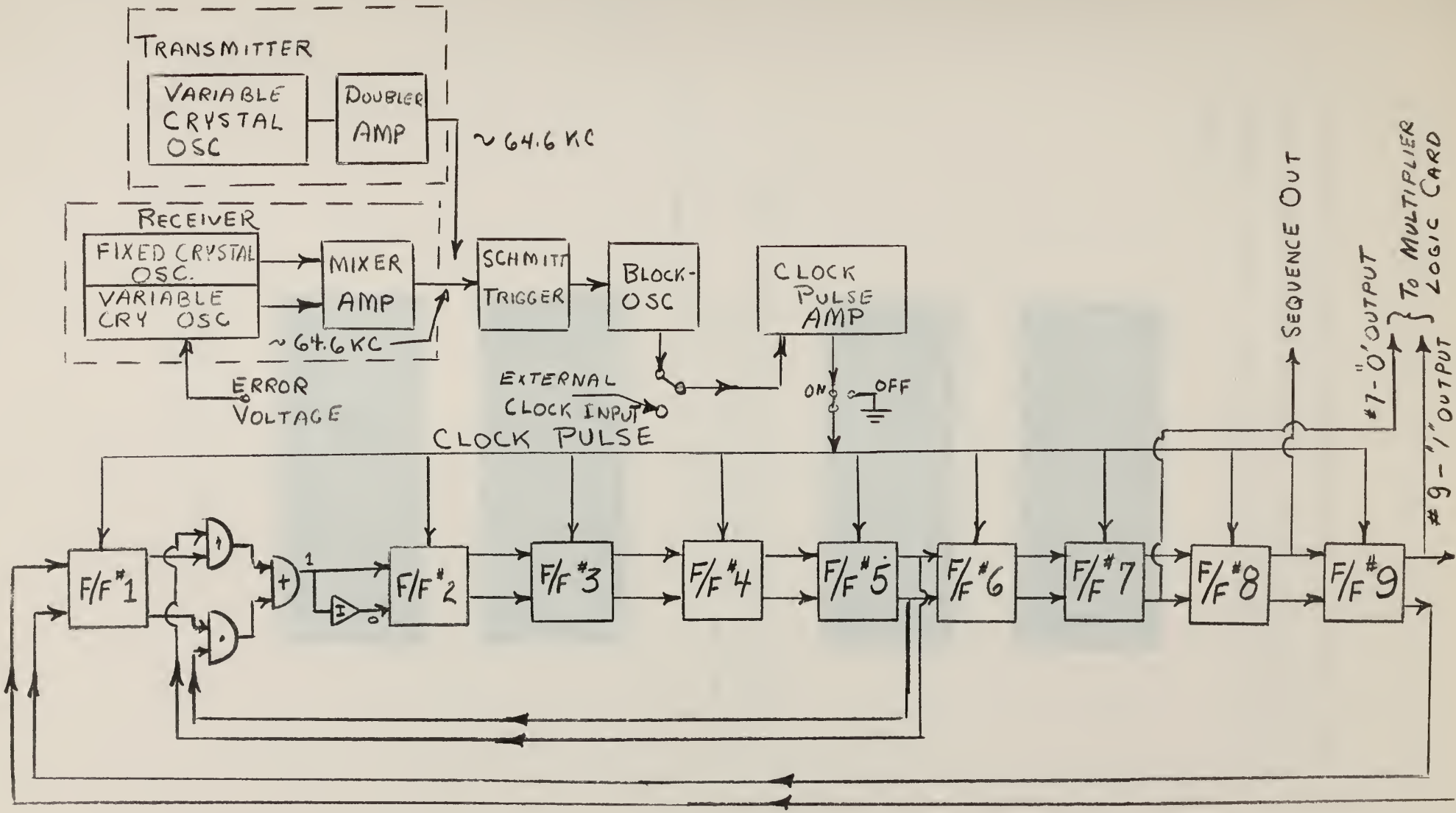


FIG. 2-14 BLOCK DIAGRAM OF LINEAR FEED BACK SHIFT REGISTE

The outputs of both shift registers were fed to a duel-beam oscilla-scope to observe the lock-on and track conditions; Fig. 2-15 shows both binary sequences in an"unlocked" and a locked-on and tracking" condition.

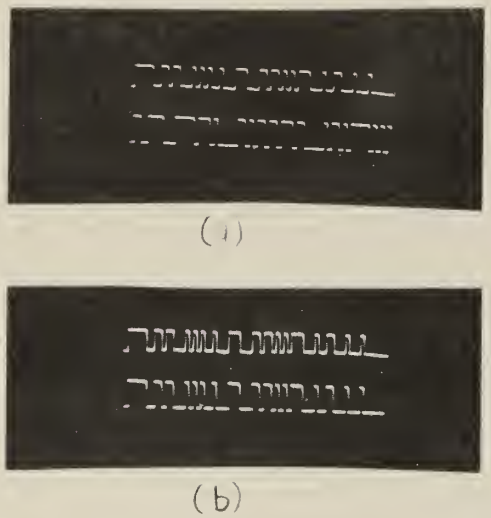


Fig. 2-15 Transmitter and Receiver Binary Sequences;
(a) in an unlocked condition,
(b) in a lock-on and tracking condition.

Fig. 2-16 shows an expanded version of Fig. 2-15

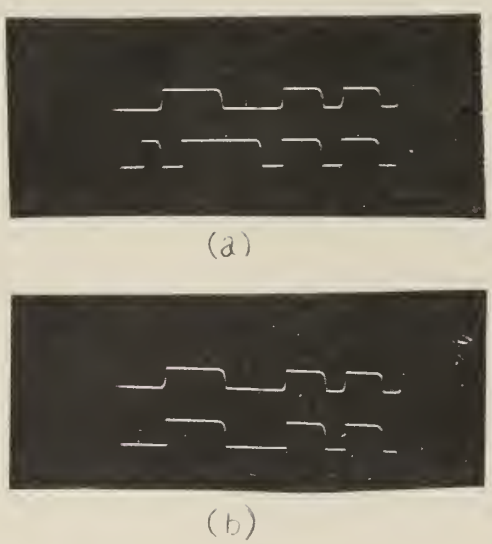


Fig. 2-16 Expanded version of Fig. 2-15.

The block diagram of the complete digital system is shown in Fig. 2-17. The system is operable in the presence of large noise signals and was tracking smoothly with an input Signal to Noise ratio of approximately - 30 db. Spilker has shown the theoretical limit to be -48db.[1]

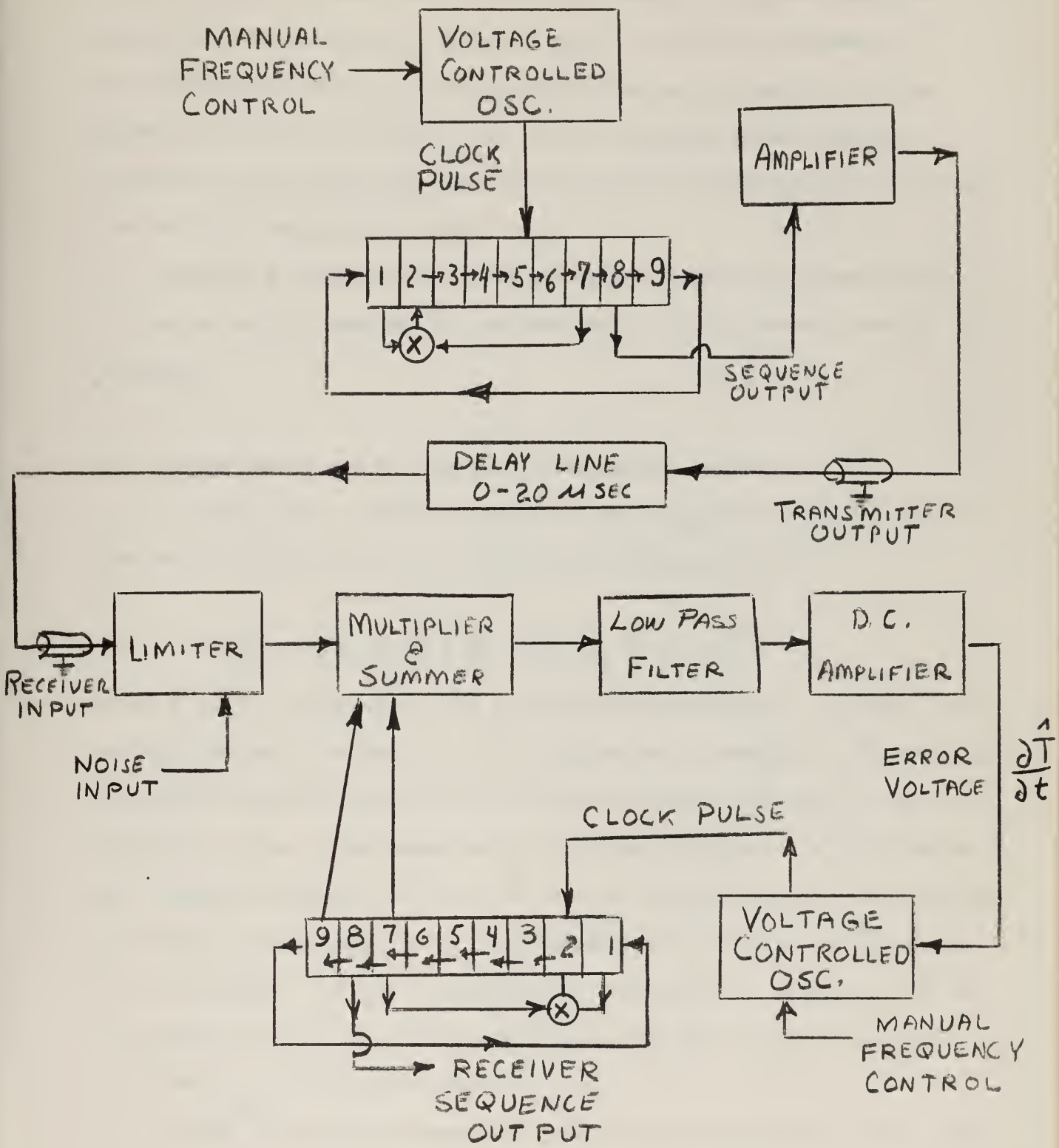


FIG. 2-17 BLOCK DIAGRAM OF DIGITAL DELAY-LOCK SYSTEM

3. Phase Plane Analysis.

This section is concerned with the methods of phase plane analysis to obtain the transient behavior of the Delay-Lock Discriminator. The first topic to be considered is the basic theory of the phase plane and its method of application. Following this will be the development of the differential equation which describes the lock-on operation of the delay-lock system. The final topic to be considered is the computer approach to the phase plane solution for two discriminator characteristics, the saw tooth and gaussian cases.

Appendix A contains the flow diagrams and computer programs written in Fortran Source Language for the construction of the phase planes of interest.

3-1. Basic Theory and Application of Phase Plane Analysis.

A large class of Feedback Control Systems and their operation can be described mathematically by a differential equation such as:

$$\ddot{x} + P(x, \dot{x})\dot{x} + Q(x, \dot{x}) = 0$$

where P and Q are functions of a signal and its derivative. In phase plane analysis methods, the value of $\dot{x}$ is plotted as a function of x with the individual curves or trajectories for the variation of $\dot{x}$ and x an indication of time. When examining the transient response of a given system, the initial conditions of $\dot{x}$ and x are plotted and the trajectory (which is unique) through this point is the response of the system for these initial conditions. If the trajectory path converges to a singular point in the phase plane, and the system has come to rest with a final value the coordinates of the singular point.

Truxel[16] notes three fundamental restrictions on the use of phase plane methods:

1. "The phase-plane is useful for the analysis of second-order systems only....."

2. "The phase-plane can be useful to study only the transient performance of a system subject to initial conditions but other wise un-excited."

3. "The third basic restriction relates to the admissible types of non-linearities. The coefficients of x-dot and x can be functions of x and x-dot, but not of time explicitly."

Phase plane methods are probably best explained by use of a simple example. Consider a second-order differential equation such as:

$$\ddot{x} + \omega_n^2 x = 0$$

The time operator t can be eliminated by expressing variations in $\dot{x}$ in terms of x. Define a new variable $y = \dot{x}$ and the equation becomes

$$\dot{y} + \omega_n^2 x = 0$$

Dividing by $\dot{x}$ gives: $$\frac{\dot{y}}{\dot{x}} = \frac{dy/dt}{dx/dt} = -\omega_n^2 \frac{x}{\dot{x}} = -\omega_n^2 \frac{x}{y}$$

now define a slope α such that $\alpha = \dot{y}/\dot{x}$ and again substituting gives:

$$\alpha = -\omega_n^2 \frac{x}{y} \quad \text{or} \quad -y/\omega_n^2 = \frac{x}{\alpha}$$

$$\text{let } y_1 = y/\omega_n^2 \quad \text{or} \quad -y_1 = -\dot{x}_1 = \frac{x}{\alpha}$$

The phase plane solution to this equation is found by plotting the isoclines[6] or lines of constant slope. This is shown in Fig. 3-1 along with a sample trajectory.

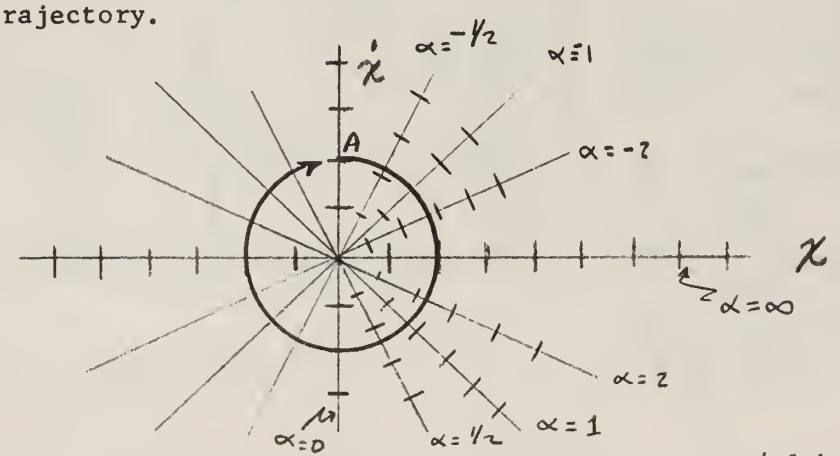


Fig. 3-1 Phase plane solution for equation -y1 = x/alpha.

As shown in the phase plane diagram, the system of concern does not converge but circles the origin. Since the equation was that of an undamped oscillator, its response should be as shown or simple harmonic motion.

3-2 Application of Phase Plane Analysis to the Problem of Transient Response of the Delay-Lock Discriminator.

The differential equation describing the transient response of the Digital Delay-Lock System will now be derived. Figure 3-2 shows a simplified version of the system under consideration.

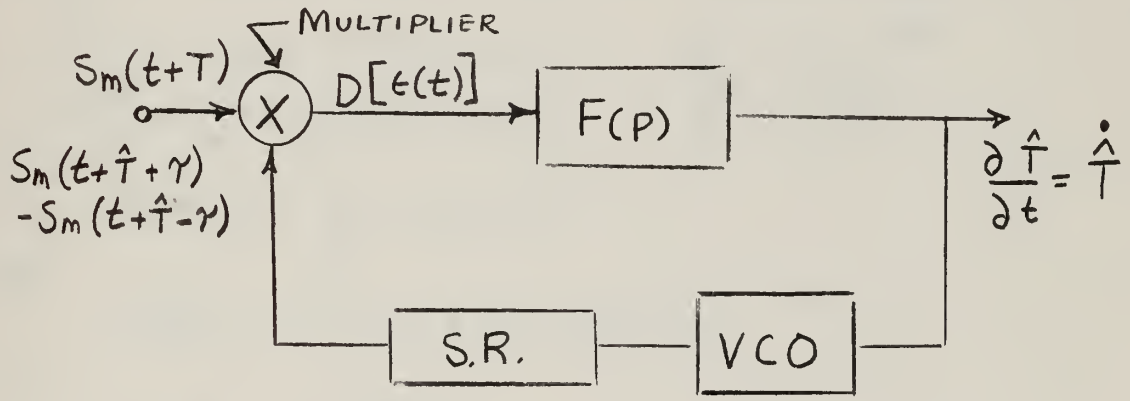
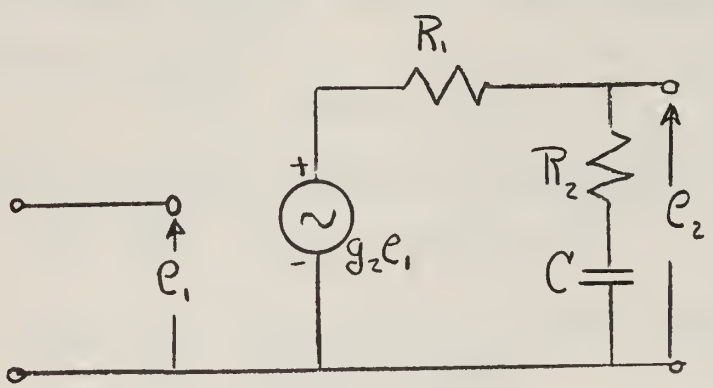


Fig. 3-2 Simplified block diagram of the Digital Delay-Lock Discriminator.

The loop filter for this system is a simple low pass RC network as shown in Fig. 3-3 along with the filter transfer ration.



$$\frac{F(P)}{g_2} = \frac{1 + aP}{1 + a^2 g_0 P}$$

R_2 = ARBITRARY

$C = a/R_2$

$R_1 = (ag_0 - 1)R_2$

g_0 = LOOP GAIN

$ag_0 \gg 1$

Fig. 3-3 Loop Filter.[12]

The system equation can be written in terms of the estimate of the Delay derivative $\dot{\hat{T}}$, and the Discriminator Characteristic $D[\epsilon(t)]$ such that $\frac{\dot{\hat{T}}}{D(\epsilon)} = F(p)$, where $F(p)$ is normalized to be $F(p) = \frac{1+\sqrt{2}\,P}{P}$

Expressed in terms of operator notation, the equation becomes:

$$P\hat{T} = F(p) \circ [D(\epsilon)]$$

where p denotes a time derivative operator $\frac{\partial[\ ]}{\partial t}$.

Expanding the above equation gives:

$$P^2\hat{T} = D(\epsilon) + P[\sqrt{2}\,D(\epsilon)]$$

$$\ddot{\hat{T}} = D(\epsilon) + \sqrt{2}\,D'(\epsilon)\cdot\dot{\epsilon}$$

$$-\ddot{\epsilon} = D(\epsilon) + \sqrt{2}\,D'(\epsilon)\cdot\dot{\epsilon}$$

$$\text{let } \gamma = \frac{\ddot{\epsilon}}{\dot{\epsilon}} = \text{SLOPE}$$

$$T(t) = V_o \cdot t + T_o$$

$$\epsilon(t) = T(t) - \hat{T}(t)$$

$$\dot{\epsilon} = V_o - \dot{\hat{T}}$$

$$\ddot{\epsilon} = -\ddot{\hat{T}}$$

then

$$-\gamma\dot{\epsilon} = D(\epsilon) + \sqrt{2}\,D'(\epsilon)\cdot\dot{\epsilon}$$

or

$$-\dot{\epsilon} = \frac{D(\epsilon)}{\gamma + \sqrt{2}\,D'(\epsilon)}$$

For a finite loop gain system, the filter transfer function was choosen as $F(P) = \frac{1+\sqrt{2}\,P}{.1+P}$ and in terms of operator notation, the system equation becomes:

$$P\,\hat{T} = F(p)\cdot D(\epsilon)$$

$$[P^2 + .1P]\,\hat{T} = D(\epsilon) + P[\sqrt{2}\cdot D(\epsilon)]$$

$$\ddot{\hat{T}} + .1\dot{\hat{T}} = D(\epsilon) + \sqrt{2}\,D'(\epsilon)\cdot\dot{\epsilon}$$

$$-\gamma\dot{\epsilon} + .1(V - \dot{\epsilon}) - \sqrt{2}\,D'(\epsilon)\cdot\dot{\epsilon} = D(\epsilon)$$

or

$$-\dot{\epsilon} = \frac{D(\epsilon) - 0.1V}{\gamma + 0.1 + \sqrt{2}\,D'(\epsilon)}$$

These then are the system equations which when used to construct the phase plane, will describe the transient response of the system. In order to construct a phase plane that will be of use, it is necessary

to evaluate the equation for numerous combinations of slope γ and delay error ϵ . The next topic to be considered describes the use of a high speed computer to construct the required phase planes.

3-3 Construction of Phase-Planes by Digital Methods.

As previously mentioned, construction of the phase plane for a given system can be a time consuming task of point by point evaluation to plot the desired isoclines. When the system is a non-linear one, this task becomes even more difficult as there may be no obvious symetry to the phase plane. Therefore, the problem of evaluating the required isoclines to produce transient response trajectories, is simplified when accomplished on a high speed computer. Before describing the results of the computer program, it is first necessary to further define the Discriminator Characteristics of interest.

As mentioned in section 2, the digital system has a saw tooth characteristic as shown in Fig. 3-4, and is mathematically defined as follows:

$$D(\epsilon) = \begin{cases} -\epsilon - 2 & \text{for } -2 \leq \epsilon < -1 \\ \epsilon & \text{for } -1 \leq \epsilon \leq 1 \\ -\epsilon + 2 & \text{for } 1 < \epsilon \leq 2 \\ 0 & \text{else where} \end{cases}$$

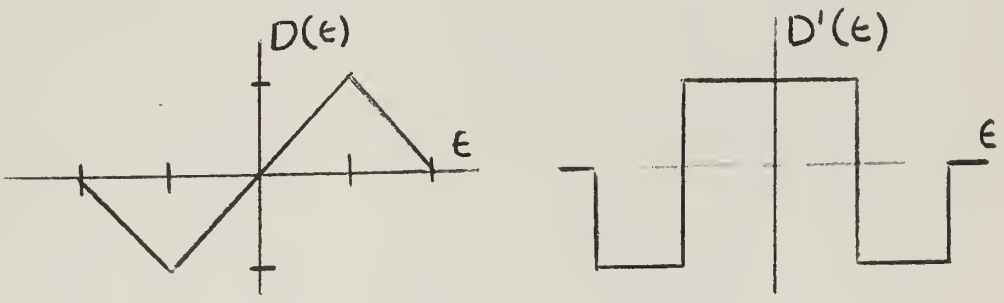


Fig. 3-4 Saw tooth Discriminator Characteristic

The Gaussian Discriminator Characteristic as previously shown in Fig. 2-3 is also of interest in evaluating the basic delay-lock system. This function is mathematically described as follows:

$$D(\epsilon) = \epsilon e^{-\epsilon^2}$$
$$D'(\epsilon) = (1-2\epsilon^2)e^{-\epsilon^2}$$

The computer programs required to evaluate the isoclines are detailed in Appendix A; it is only necessary tc say here that many hundreds of points were required to complete the phase planes. The plot of the isoclines for the saw tooth characteristic is shown in Fig. 3-5. It is apparent that the isoclines of magnitude greater than 5 are concentrated near the ϵ axis and so could not be plotted. A sample trajectory is sketched on the phase plane and shows the lock-on response for one set of initial conditions. It is apparent that unless a greater number of isoclines is plotted, the accuracy of the trajectory is to be deeply suspect. This however is the normal method of solution by phase plane techniques. Clearly, this method leaves much to be desired and the next section will show two levels of improvement by evaluating not only the phase plane but also any specified trajectory, with the digital computer. Fig. 3-6 shows the phase plane constructed for the Gaussian Characteristic.

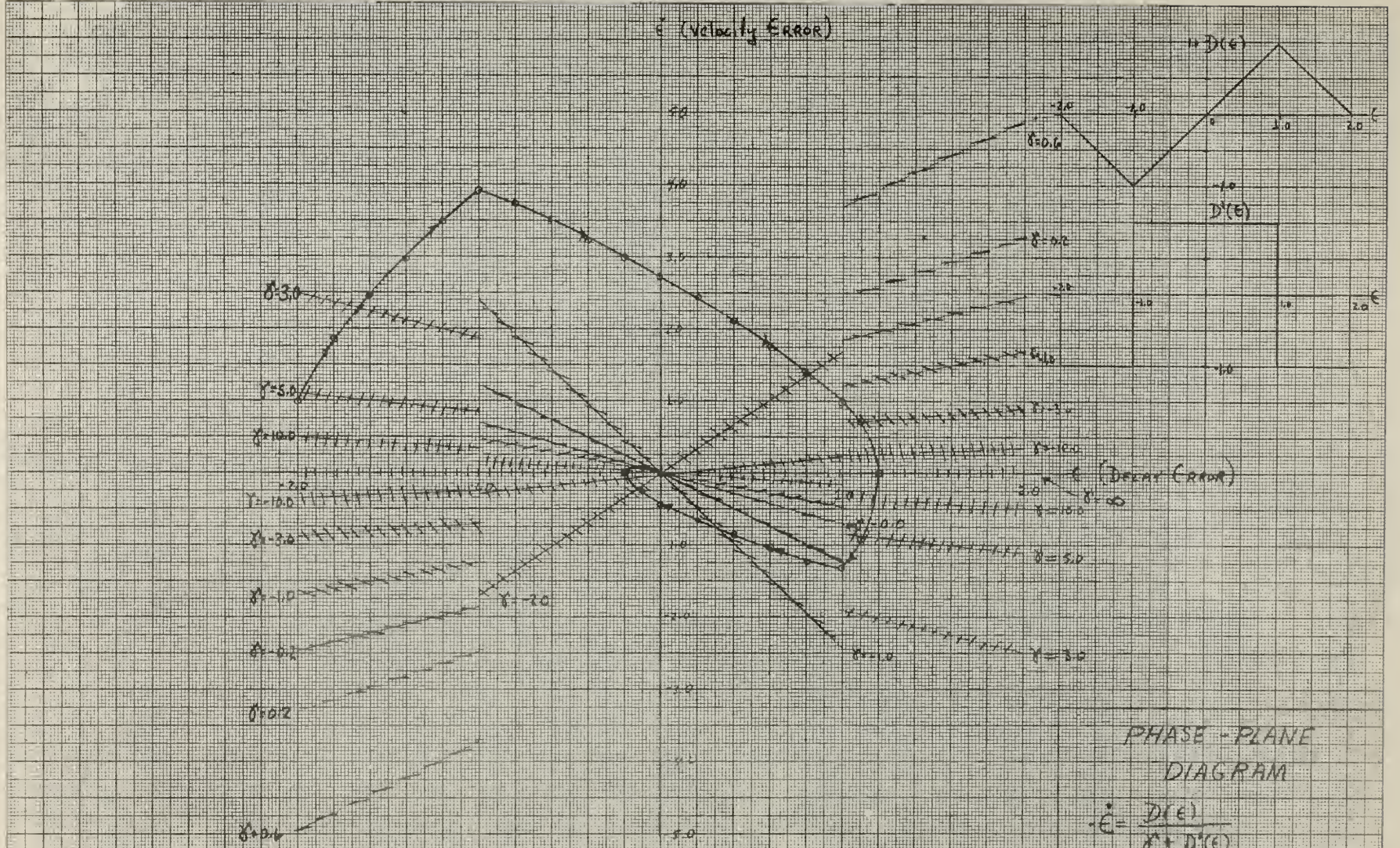

ε̇ (Velocity Error)
D(ε)
D'(ε)
ε (Decay Error)
γ=5.0
γ=10.0
γ=-10.0
γ=-5.0
γ=-3.0
γ=-2.0
γ=-1.0
γ=-0.2
γ=0.2
γ=0.6
γ=1.0
γ=2.0
γ=3.0
PHASE - PLANE
DIAGRAM
$\dot{\varepsilon} = \frac{D(\varepsilon)}{\gamma + D'(\varepsilon)}$
4 MARCH 62
C.S. Hubley

FIG. 3-5

PHASE - PLANE
DIAGRAM
$-\dot{\epsilon} = \frac{D(\epsilon)}{\gamma + D'(\epsilon)}$
S. MACHOVER
C.S. Wallace
$\gamma = 0.2$
$\gamma = 0.6$
$\gamma = 0.6$
$\gamma = 0.2$
$\gamma = -0.2$
$\gamma = -1.0$
$\gamma = -1.0$
$\gamma = -0.2$
$\gamma = 0.2$
$\gamma = 0.2$
$\gamma = 1.0$
$\gamma = 0$
$\gamma = 0.2$
$\gamma = 0.6$
$\gamma = 0.6$
$\gamma = 0.2$
$\gamma = -0.2$
$\gamma = -1.0$
$\gamma = -1.0$
$\gamma = -0.2$
$\gamma = 0.2$
$\gamma = 0.2$
1.0
0.2
1.0
-1.0
-0.2
1.0

FIG. 3-6

4. Transient Analysis By Sequential Programming.

As previously mentioned, the transient response of a given system may be obtained by constructing a phase plane associated with the system and then sketching the required trajectories by faring the curve through the known isoclines. This technique has been recently applied to a system known as the Phase-Lock Discriminator[3]; however, this method is at best adequate in that the errors involved in sketching are acqumulative, and the final value for lock-on lock critical trajectories may be meaningless. Certain problems can be adapted to solution by analog computer methods[7], but here again one has to worry about amplifier drift during solution producing flucuating errors. For the solution of the non-linear equation of the delay-lock, analog methods are not practicable, and some other method is desirable.

This section will present a method of digital analysis by computing the desired trajectories with the aid of a high speed general purpose digital computer, the CDC 1604.

Two levels of improvement will be covered; the fixed increment approach, and the method of Dynamic or Sequential Programming which limits the error to any fixed amount. Actual computer results for the transient response of the Delay-Lock Discriminator will be presented. Although time is not directly available in the phase plane diagram, it is inherently involved and can be obtained by graphical procedures[6]. However, it is available during the computer solution and this method will also be covered.

The Flow Diagram and Fortran Source Language Programs are contained in Appendix B.

4-1 Solution of the Differential Equation by Fixed Increment Method.

The equation to be solved by phase plane methods as described in

section 3 is given by: $-\dot{\epsilon} = \frac{D(\epsilon)}{\gamma + \sqrt{2}\, D'(\epsilon)}$

Rearranging to solve for the slope γ gives: $\gamma = \frac{D(\epsilon) + \sqrt{2}\, D'(\epsilon) \cdot \dot{\epsilon}}{-\dot{\epsilon}}$

This is the main value to be computed as the solution of the trajectory developes. Figure 4-1 shows the basic method of approach. Starting with a known point in the phase plane representing the initial conditions, $[\dot{\epsilon}_0, \epsilon_0]$ the slope γ_0 at this point is evaluated. Using a fixed increment of ϵ, $\Delta\epsilon$, the next value of velocity error $\dot{\epsilon}_1$ is computed in a linear fashion such that $\dot{\epsilon}_1 = \dot{\epsilon}_0 + \gamma \Delta\epsilon$ and the value of delay at this point is determined by $\epsilon_1 = \epsilon_0 + \Delta\epsilon$. This process is continued until the trajectory reaches the stable point (in this case the origin) where the system is then in lock and tracking, or until the trajectory reaches a value of delay error ϵ equal to 2 and the system fails to lock in.

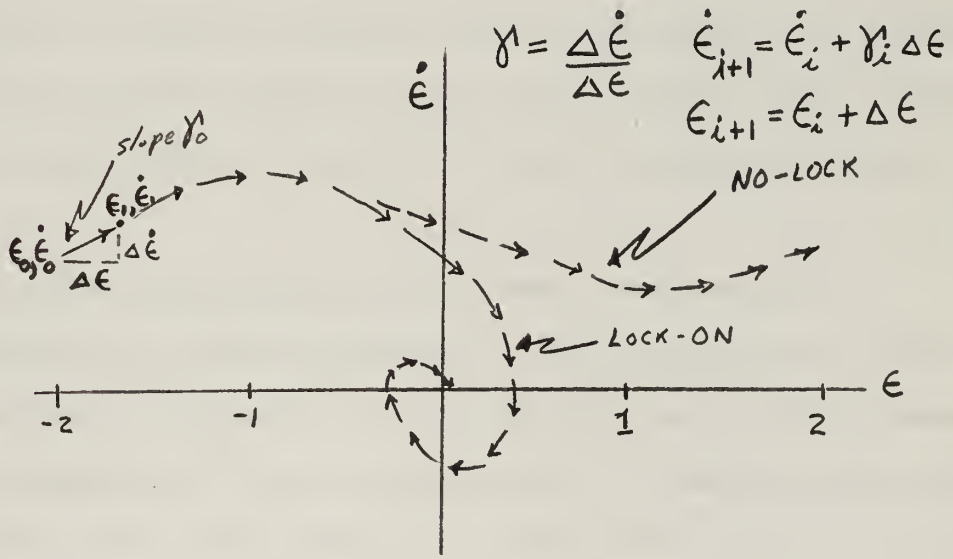


Fig. 4-1 Computer Approach to Evaluation of Trajectory.

In the method just described, the increment value was chosen to be $\Delta\epsilon = 0.01$. Although this method produces satisfactory sets of trajectories, there is a major difficulty involved, in that when the trajectory approaches the ϵ axis, the slopes in the phase plane are

approaching infinity and even with a very small increment, the new value of $\dot{\epsilon}$ will be made to go too far negative and not be the true trajectory. An example of this is shown below and taken from a sample computed trajectory. When the value of $\dot{\epsilon}_i$ first went negative, the routine would set the new value of $\dot{\epsilon}$, $\dot{\epsilon}_{i+1}$, equal to the negative of the old value $\dot{\epsilon}_i$ and then resume the program.

Value of ϵ	Value of $\dot{\epsilon}$	Slope
1.11000	0.29645	-9.07462
1.12000	0.20569	-13.75419
1.13000	0.06815	
	switch over occurs as next value of $\dot{\epsilon}$ is negative	
1.13000	-0.06815	122.299
1.12000	-1.29114	3.83068
	Note this large increase in $\dot{\epsilon}$ in just one value of increment, $\Delta\epsilon$.	

Figure 4-2 shows the results of this first approach to the evaluation of the transient response of the system. Several values of initial conditions were plotted to describe the lock-on region of interest.

4-2 Sequential Programming Applied to Phase Plane Analysis.

Sequential or Dynamic Programming is a basic adaptation of the process developed by Bellman[10]. It is generally described by considering the computer as a adaptive device capable of changing system parameters internally as the solution of a given problem develops. In the case of the computer solution of the phase plane trajectories, this means not operating with a fixed increment, but rather adapting a variable increment to follow the solution as it develops.

Instead of the fixed increment as previously covered, consider a variable increment $\Delta\epsilon_K$, which will take on one value as the slope

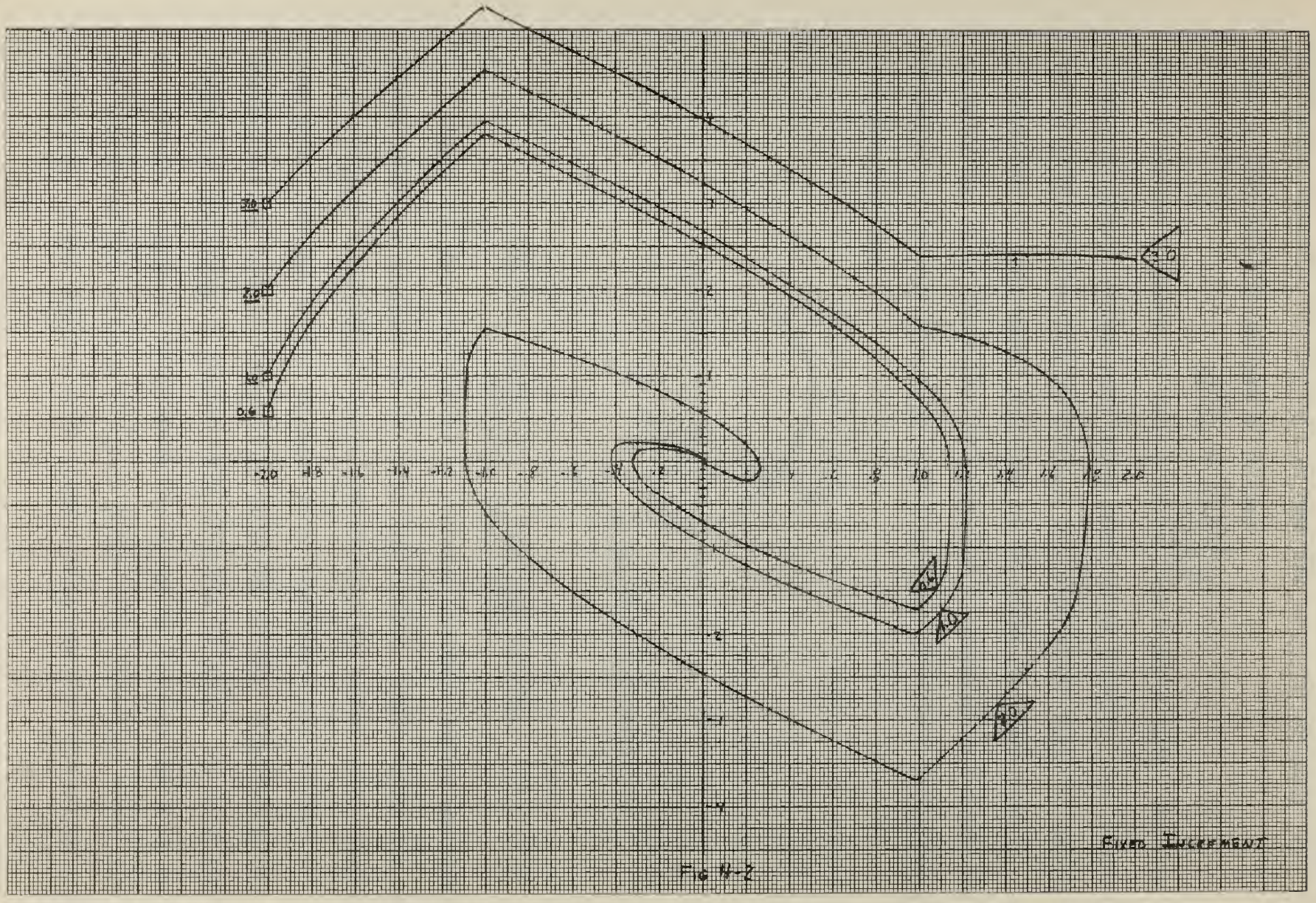


FIG 4-2

in the phase plane becomes zero, and decreases to zero as the slope approaches infinity. It was decided that the variable increment in this problem would be defined as follows:

$$\Delta\epsilon_K = \frac{0.02}{1+|\dot{\epsilon}_K|}$$

This allows an increment to take on values from 0.02 to zero. When the trajectory passes through slope areas approaching infinity, the trajectory starts to move almost vertically until this high slope region is passed. A comparison of this method with that of the fixed increment type is shown in Fig. 4-3. The method of sequential programming then allows the trajectory to recover from these high slope regions without being overly influenced by them.

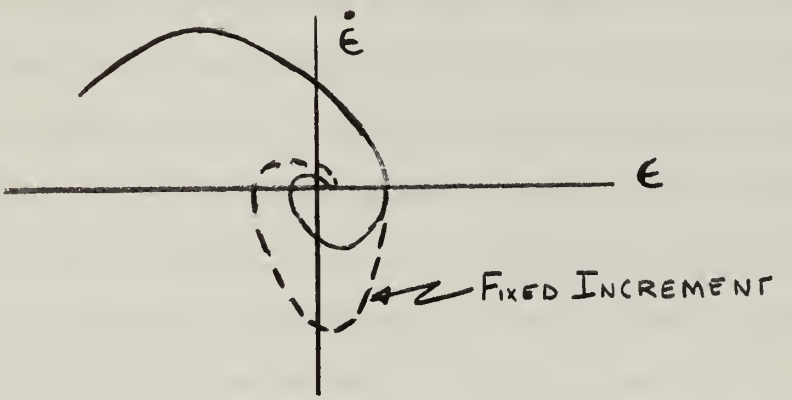


Fig. 4-3 Comparison of fixed and variable increment trajectories.

Figure 4-4 shows the results of variable increment method for determining transient response of the Delay-Lock System. These curves are based on a saw-tooth discriminator characteristic and the system having infinite loop gain. Various initial velocity error conditions were plotted to demonstrate the lock-on characteristics of the system. Considering the trajectory describing an initial velocity error of unity, the curve starts to increase in velocity error while the system is reducing the delay error and correcting the estimate of signal delay. The trajectory starts its spiral towards the singular point which corresponds to a lock-on and track

condition. In this case the system does lock on and so will tolerate a velocity error of this magnitude. However, in the case of an initial velocity error of 2.3, the system attempts to lock-in and track but does not quite make it and assumes a no-lock condition. The system will then remain out of lock until the estimate of the received signal is again in the discriminator region. Fig. 4-5 shows the transient response for the same system discriminator characteristic but concerns the finite loop gain case. The lock-no lock critical trajectory occurs for the same initial velocity error but in this latter case, the system comes to rest with a finite delay error proportional to the initial velocity error. Since a trajectory may be started any where in the phase plane, the computer curves offer a second analysis of the operating system. This concerns the case where the system is in lock and tracking a target with a constant velocity. If the target accelerates (or decelerates), then the target assumes a new velocity and the system is temporarily out of track and must lock on in the manner described above.

The transient response for the delay-lock system with a Gaussian Discriminator Characteristic and infinite and finite loop gains is shown in Fig. 4-6 and 4-7. The phase plane curves are explained in the manner previously mentioned. Although the computer data was hand drawn, the curves could easily be constructed by a high speed digital plotter to give as many trajectories as desired.

The error in the trajectory as it passes through the region of large valued slopes may be approximated in the following manner:

The next value of $\dot{\epsilon}$ may be expanded in a Taylor's series to be:

$$\dot{\epsilon}_1(\epsilon_1) = \dot{\epsilon}_1(\epsilon_0 + \Delta\epsilon_K) = \dot{\epsilon}(\epsilon) + \Delta\epsilon_K \frac{\partial\dot{\epsilon}}{\partial\epsilon} + \frac{\Delta\epsilon_K}{2!} \frac{\partial^2(\dot{\epsilon})}{\partial\epsilon^2} + \cdots$$

Assuming a parabolic trajectory when crossing through the infinite slope area allows the following simplifications:

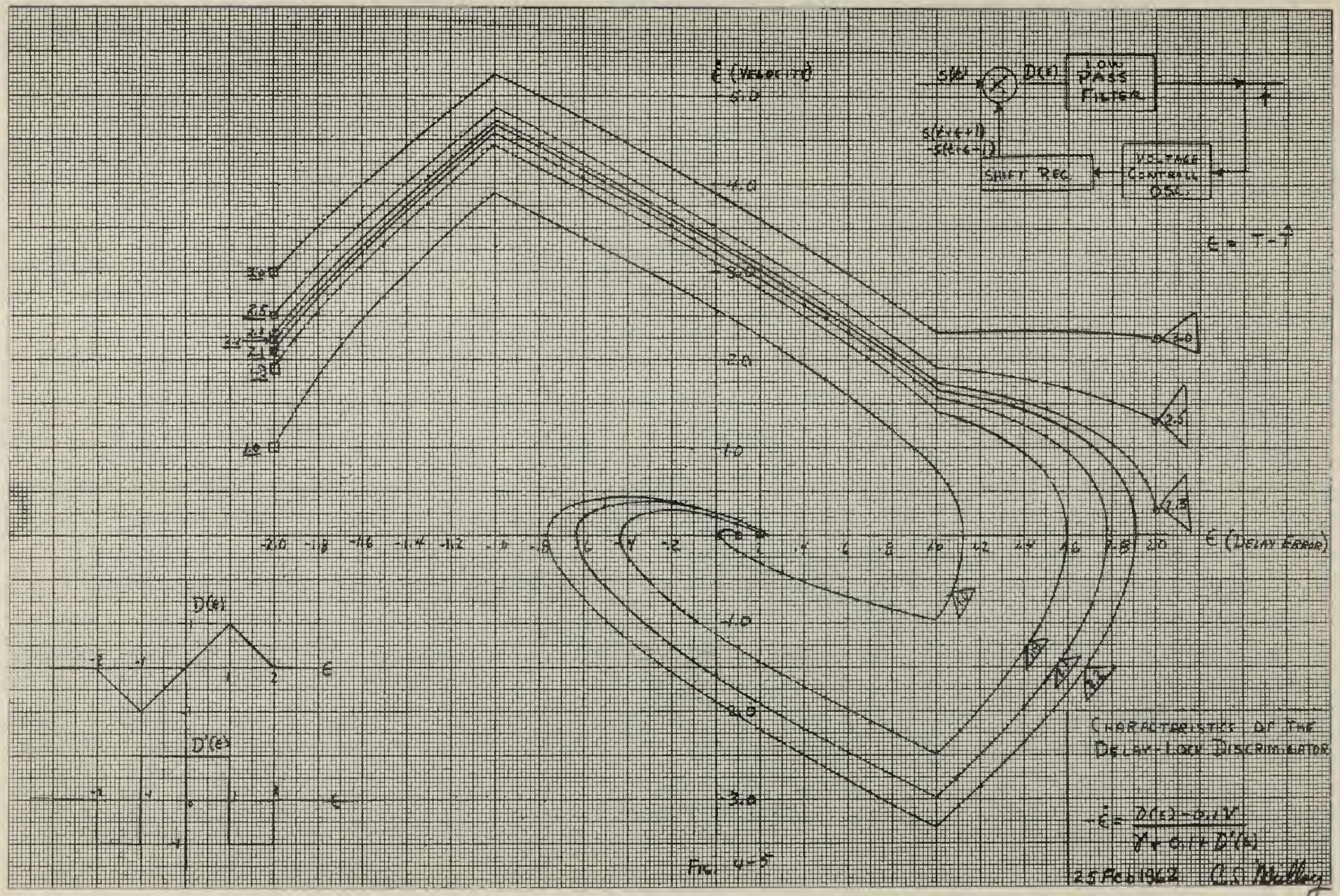

ε̇ (VELOCITY)
S(t)
D(ε)
LOW-PASS FILTER
S(t+1)
-S(t-1)
SHIFT REG.
VOLTAGE CONTROLLED OSC.
ε = T - T̂
ε (DELAY ERROR)
D'(ε)
D'(ε)
CHARACTERISTICS OF THE DELAY-LOCK DISCRIMINATOR
25 Feb 1962

FIG. 4-5

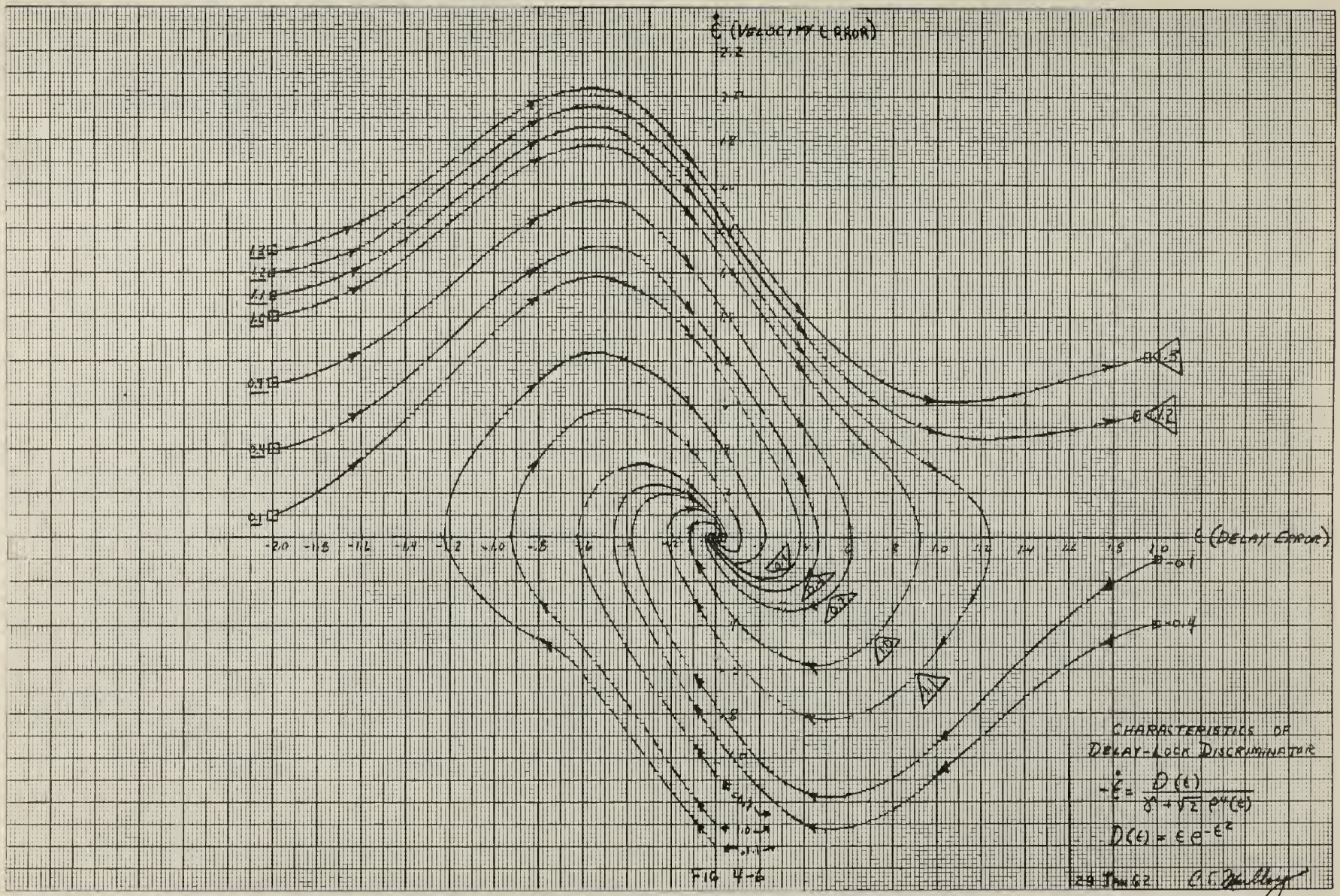
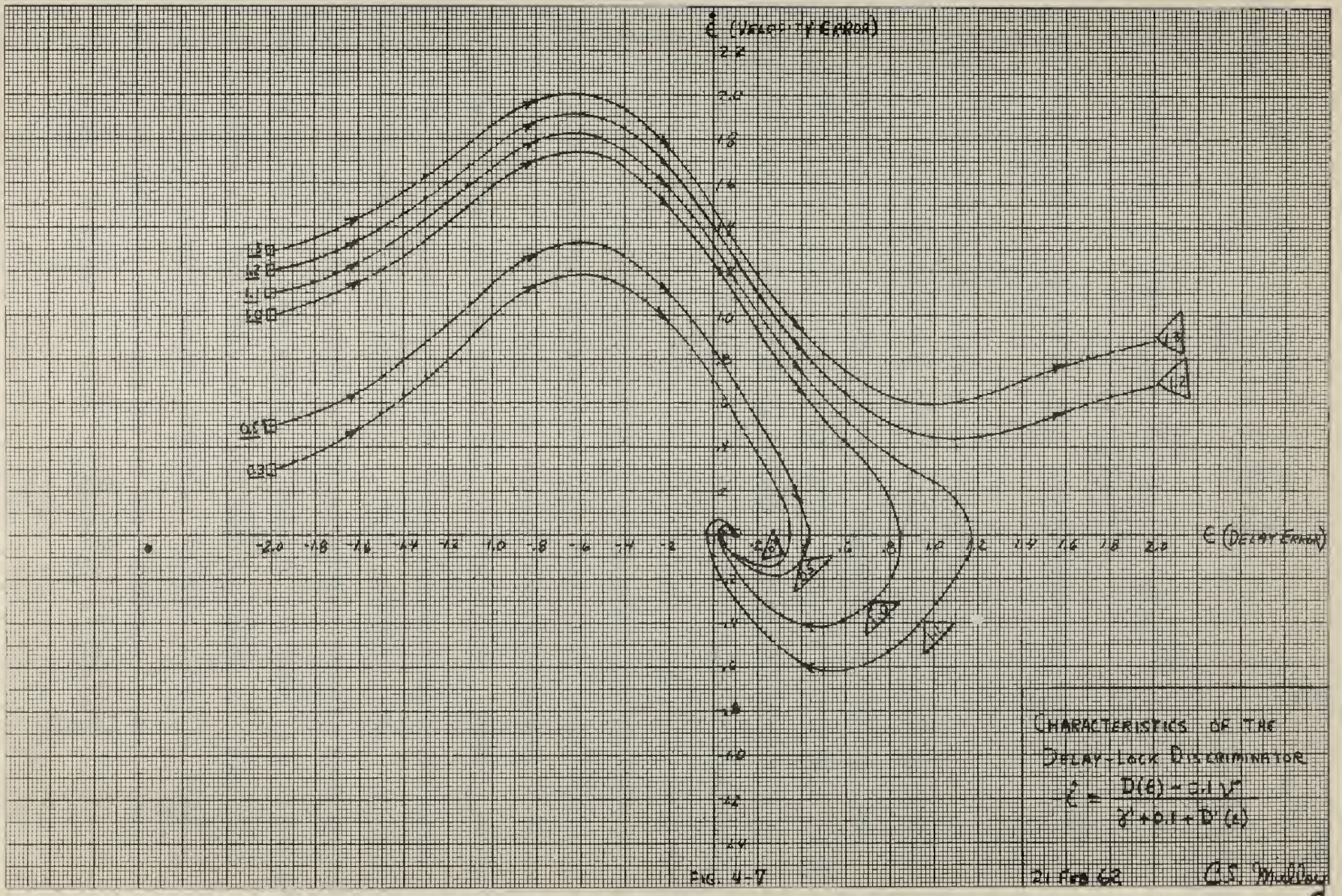

$\dot{\epsilon}$ (VELOCITY ERROR)
ϵ (DELAY ERROR)
B=0.5
B=1.2
B=0.1
B=0.4
CHARACTERISTICS OF
DELAY-LOCK DISCRIMINATOR
$-\dot{\epsilon} = \frac{D(\epsilon)}{\delta' + \sqrt{2}\,\phi''(\epsilon)}$
$D(\epsilon) = \epsilon e^{-\epsilon^2}$
29 JUNE 62

FIG 4-6


$\dot{\epsilon}$ (Velocity of Error)
ϵ (Delay Error)
1.2 B
1.1 B
1.0 B
0.9 B
0.3 B
Characteristics of the
Delay-Lock Discriminator
$\dot{\epsilon} = \frac{D(\epsilon) - 0.1\sqrt{}}{\gamma' + 0.1 + D'(\epsilon)}$
Fig. 4-7
21 Feb 62
C.S. Wallace

$$\dot{\epsilon}_1(\epsilon+\Delta\epsilon_K) = \dot{\epsilon}(\epsilon) + \Delta\epsilon_K\,\gamma + \text{Error Term}$$

$$\dot{\epsilon} = \epsilon^{1/2}$$
$$\ddot{\epsilon} = \tfrac{1}{2}\epsilon^{-1/2} = \gamma\dot{\epsilon} = \gamma\epsilon^{1/2}$$
$$\dddot{\epsilon} = -\frac{1}{4}\epsilon^{-3/4} \qquad \gamma = \frac{1}{2\epsilon}$$

$$\text{ERROR} = e_{\dot{\epsilon}} = \frac{\Delta\epsilon_K^2}{2!}\cdot\frac{\partial(\ddot{\epsilon})}{\partial\epsilon} = \frac{\Delta\epsilon_K^2}{2!}\cdot\dddot{\epsilon}$$

$$\Delta\epsilon_K = \frac{\delta}{1+|\gamma|}$$

The error in $\dot{\epsilon}$ is then $e_{\dot{\epsilon}} = \dfrac{\delta^2}{\left(1+\frac{1}{2}\left|\frac{1}{\epsilon}\right|\right)^2}\cdot\left(-\frac{1}{4}\epsilon^{-3/4}\right)$

and assuming that $\epsilon << 1$, $e_{\dot{\epsilon}}$ is approximately $\frac{1}{2}\delta^2\epsilon^{1/2}$

4-3 Computation of the Lock-On Time Response.

As previously mentioned, time response is not directly available for the phase plane diagram, but may be determined by graphical techniques. However, this procedure is again a tiresome method which is not very accurate. It is possible to compute the time response for a given trajectory while the computer routine is in the process of constructing the trajectory. Fig. 4-9 shows the typical delay error versus time response for several initial velocity conditions along with a typical velocity error versus time response. As is apparent, the delay error term $\epsilon(t)$ starts at a value of -2 and oscillates in a damped fashion converging to zero value delay error when the system has attained Lock-On. These transient responses were observed on a analog plotter for the Digital System and were of the same general appearance as those predicted. Fig. 4-8 shows an observed transient response for the approximate velocity error function when the system was in the process of lock-on. In order to show the method of computing transient times it is necessary to expand the delay error function in a Taylor's Series. Therefore, $\epsilon_1(t) = \epsilon_0 + \Delta t\,\dot{\epsilon}_0 + \frac{\Delta t^2}{2!}\ddot{\epsilon}$ and the increment of time required for the trajectory to pass from ϵ_0 to ϵ_1 is given by: $\Delta t = \left|\dfrac{\epsilon_1-\epsilon_0}{\dot{\epsilon}_0}\right| = \left|\dfrac{\Delta\epsilon_K}{\dot{\epsilon}_0}\right|$

It is only necessary to sum the time increments to find the total time expired at any given point on the trajectory. The small error term $\frac{\Delta t^2 \ddot{\epsilon}}{2!}$ was neglected.

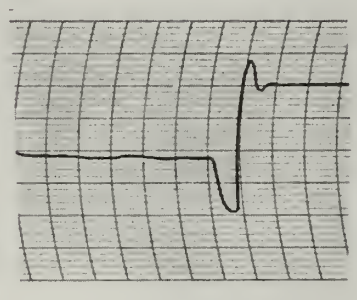


Fig. 4-8 Observed wave-form of velocity error response of Digital Delay-Lock System during lock-on.

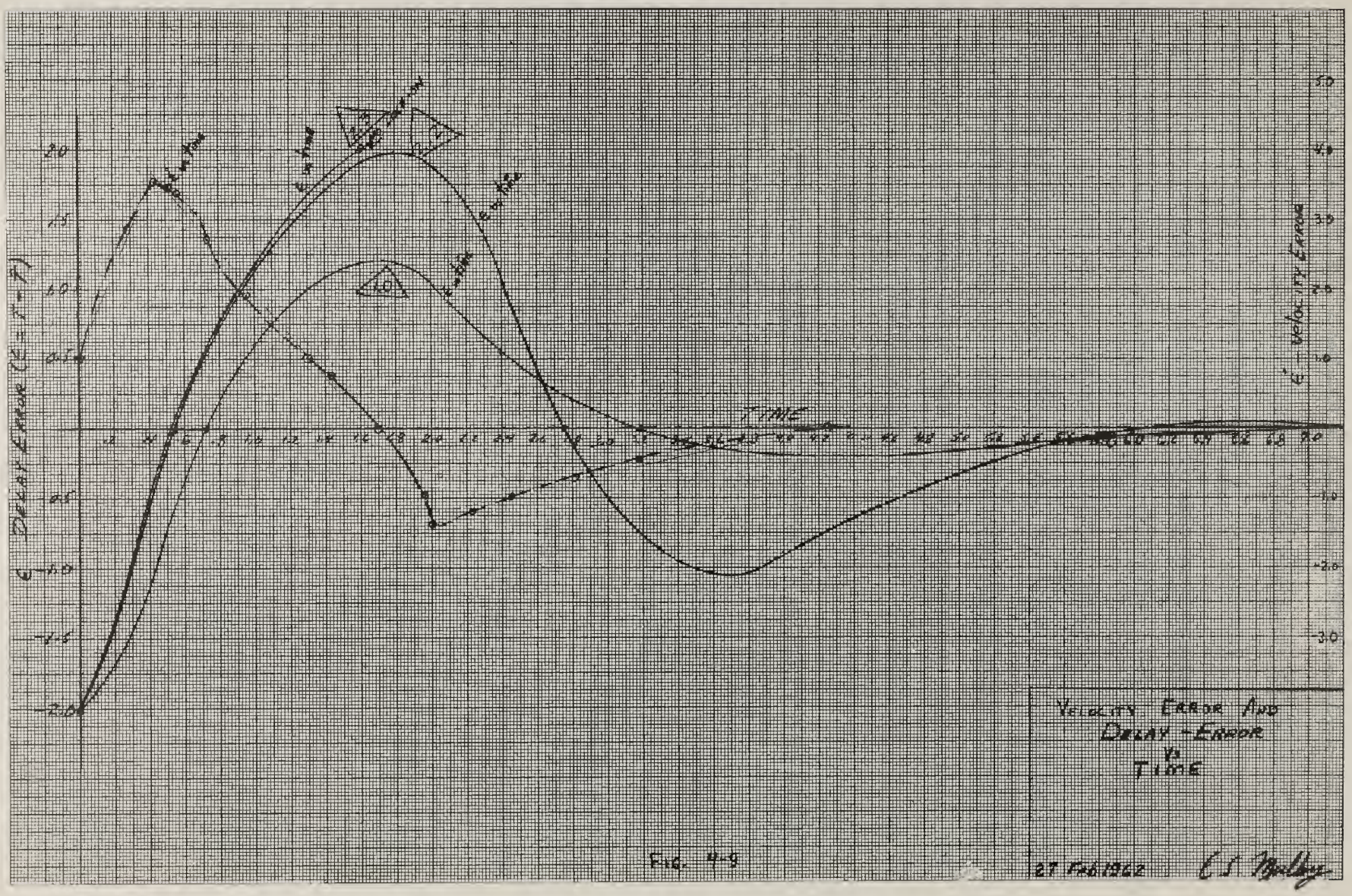

Delay Error (ε = x − x')
Velocity Error
Time
Velocities Error And
Delay - Error
Vs
Time
27 Feb 1962
E S Polhemus

Fig. 4-9

5. Conclusions.

The Digital Delay-Lock Discriminator with its pseudo-random signal characteristics offers a method of tracking targets at great ranges and high velocities, while operating with moderate power requirements. The experimental system is now operating at the Lockheed Missle and Space Company and is under consideration by NASA as a proposed tracking and rondevous system for maned and unmaned satelites. The system has other possibilities such as an underwater tracking system. Since the system has the capability to track targets when the Signal to Noise ratio is in the order of -30db, the power of the transmitted signal could be maintained at a level below that of the ambient noise surrounding the target, and as such, would not give the target an indication it was under survailence.

In order that the system be optimized, it was necessary to determine the transient response of a normalized system during the lock-on process. Phase-plane analysis methods were then utilized to obtain this response. With out the aid of a high speed digital computer, this analysis would not have been easily accomplished. The data obtained from the sequential programming methods demonstrate that this phase plane approach to the analysis problem is applicable to a large number of non-linear systems.

BIBLIOGRAPHY

1. J. J. Spilker, Jr., and D. T. Magill, The Delay-Lock Discriminator-An Optimum Tracking Device, Proc. IRE, vol. 49, pp. 1403-1416, September, 1961.

2. J. J. Spilker, Jr., Threshold Comparison of Phase-Lock, Frequency-Lock and Maximum-Likelihood Types of FM Discriminators, an unpublished paper.

3. A. K. Rue and P. A. Lux, Transient Analysis of a Phased-Locked Loop Discriminator, IRE Trans. on Space Electronics and Telemetry, vo. SET-7, pp. 105-111, December, 1961.

4. B. Elspas, The Theory of Autonomous Linear Sequential Networks, IRE Trans. on Circuit Theory, vol. CT-6, pp. 45-60, March, 1959.

5. B. Elspas, A Radar System Based on Statistical Estimation and Resolution Considerations, Stanford Electronics Laborities, Report No. 361-1, Appendix D, August, 1955.

6. J. G. Truxal, Automatic Feedback Control System Synthesis, McGraw-Hill Book Co., New York, 1955.

7. Proceedings of the Symposium on Non Linear Circuit Analysis, Polytechnic Press, Brooklyn, N. Y., 1957.

8. W. J. Cunningham, Introduction to Non Linear Analysis, McGraw-Hill Book Co., New York, 1958.

9. R. A. Struble, Non Linear Differential Equations, McGraw Hill Book Co., New York, 1962.

10. R. Bellman, Adaptive Control Processes: A Guided Tour, Princeton Press, 1960.

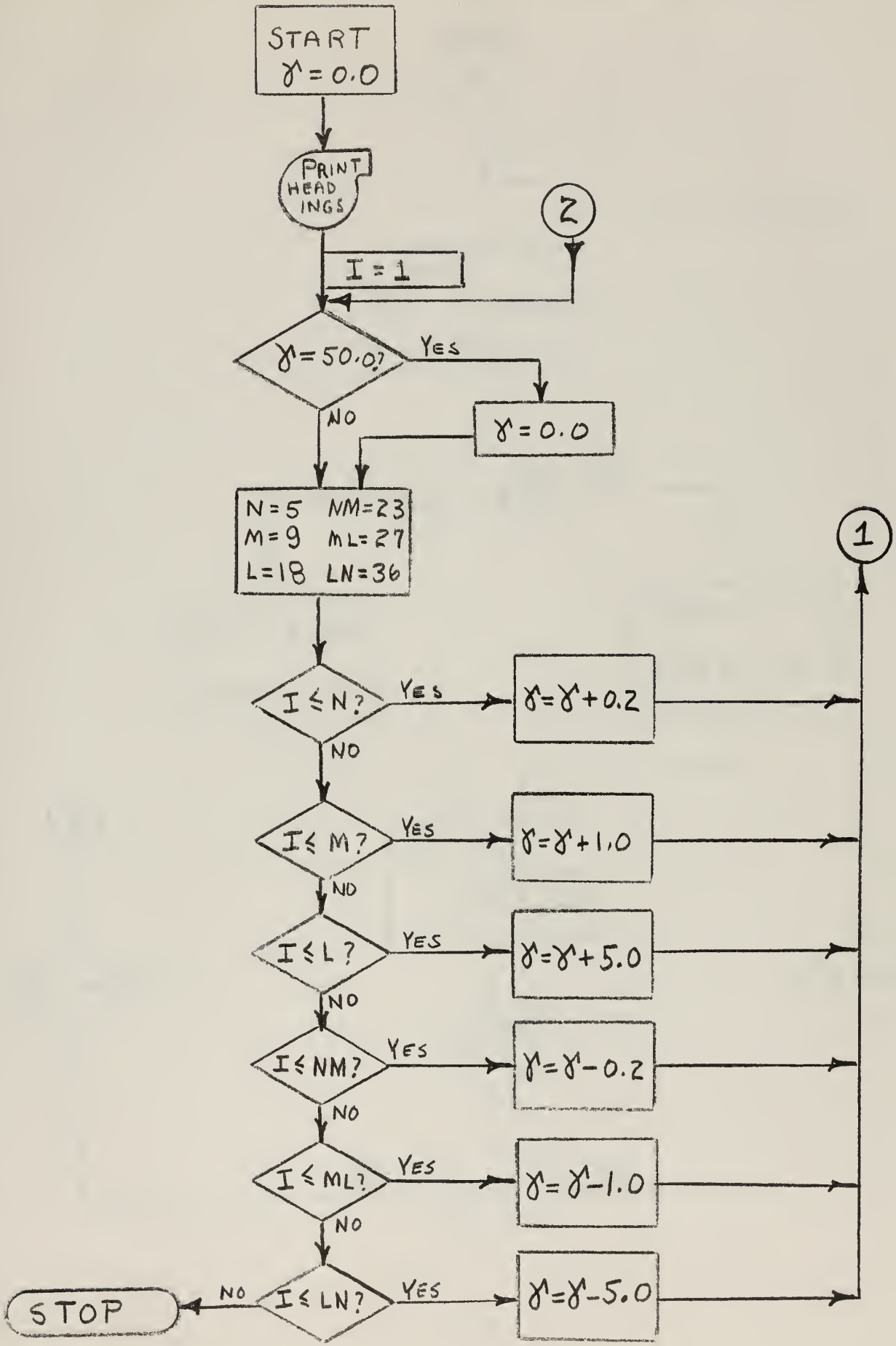
APPENDIX A

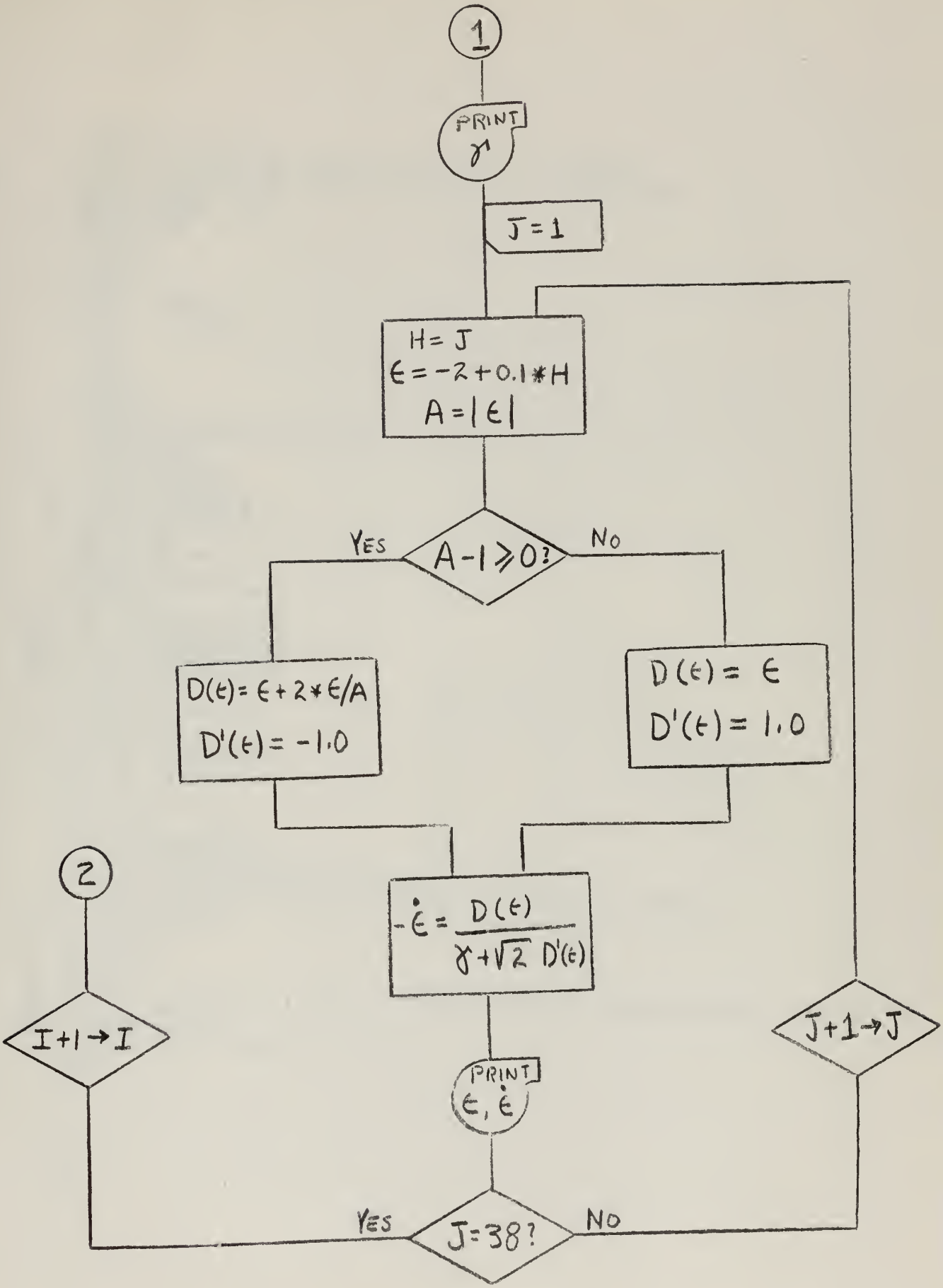
This Appendix contains the Flow Diagram and Fortran Source Programs required to evaluate the isoclines (lines of constant slope) of the phase planes which represent the solution to the differential equation:

$$-\dot{\epsilon} = \frac{D(\epsilon)}{\gamma + \sqrt{2}\, D'(\epsilon)}$$

In this problem, it is necessary to fix a value of slope , and evaluate the above equation for $\dot{\epsilon}$ with ϵ taking on the range $-2 \leq \epsilon \leq 2$; an increment of 0.01 was choosen for . Values of slope γ used were: $\pm$ { 0.2, 0.4, 0.6, 0.8, 1.0, 2.0, 3.0, 4.0, 5.0, 10.0, 15.0, 20.0, 25.0, 30.0, 35.0, 40.0, 45.0, 50.0 } . It was thought that this many values of slope would be required to properly bound the phase plane. As it turned out, only slopes in the region $\gamma \leq 10$ were useful since those of higher value could not be plotted on a useable phase plane. The results of these programs are shown in Section 3, Figures 3-5 and 3-6.

FLOW DIAGRAM
PROGRAM DELAY




1
PRINT γ
J = 1
H = J
ε = -2 + 0.1 * H
A = |ε|
A - 1 ≥ 0?
YES
NO
D(ε) = ε + 2 * ε/A
D'(ε) = -1.0
D(ε) = ε
D'(ε) = 1.0
-ε̇ = D(ε) / (γ + √2 D'(ε))
PRINT ε, ε̇
J = 38?
YES
NO
J + 1 → J
2
I + 1 → I

```
      PROGRAM DELAY1
C     THIS PROGRAM PRODUCES REQUIRED 150 CLINES
C     FOR SOLUTION OF THE DELAY-LOCK DISCRIMINATOR
      DO 50 K=2,12,2
      SLOPE=0.0
      PRINT 22
      V=0.04
      W=K-2
      V=W*V
      PRINT 33,V
      DO 14 I=1,36
      N=5
      M=9
      L=18
      NM=23
      ML=27
      LN=36
      IF(SLOPE-50.0)51,61,51
   61 SLOPE=0.0
   51 IF(I-N)3,3,1
    1 IF(I-M)4,4,2
    2 IF(I-L)5,5,23
    3 SLOPE=SLOPE+0.2
      GO TO 6
    4 SLOPE=SLOPE+1.0
      GO TO 6
    5 SLOPE=SLOPE+5.0
      GO TO 6
   23 IF(I-NM)26,26,24
   24 IF(I-ML)27,27,25
   25 IF(I-LN)28,28,15
   26 SLOPE=SLOPE-0.2
      GO TO 6
   27 SLOPE=SLOPE-1.0
      GO TO 6
   28 SLOPE=SLOPE-5.0
    6 PRINT 55,SLOPE
      DO 13 J=1,81
      H=J
      E=-4.1+0.1*H
      E1=E*E
      C=2.7182818284
      PD1=E*(1.0/C**E1)
      PD2=(1.0-2.0*E1)*(1.0/C**E1)
   12 Y=(PD1+SQRTF(2.0)*PD2*V)/(SLOPE+SQRTF(2.0)*PD2)
   13 PRINT 44,E,Y
   14 CONTINUE
      PAUSE
   50 CONTINUE
   15 STOP
   22 FORMAT(9H VELOCITY,3X,6H SLOPE,3X,8H E-VALUE,15X,8H Y-VALUE,//)
   33 FORMAT(F8.4,/)
   44 FORMAT(25X,F4.2,16X,F9.5,/)
   55 FORMAT(12X,F8.4,/)
      END
      END
```

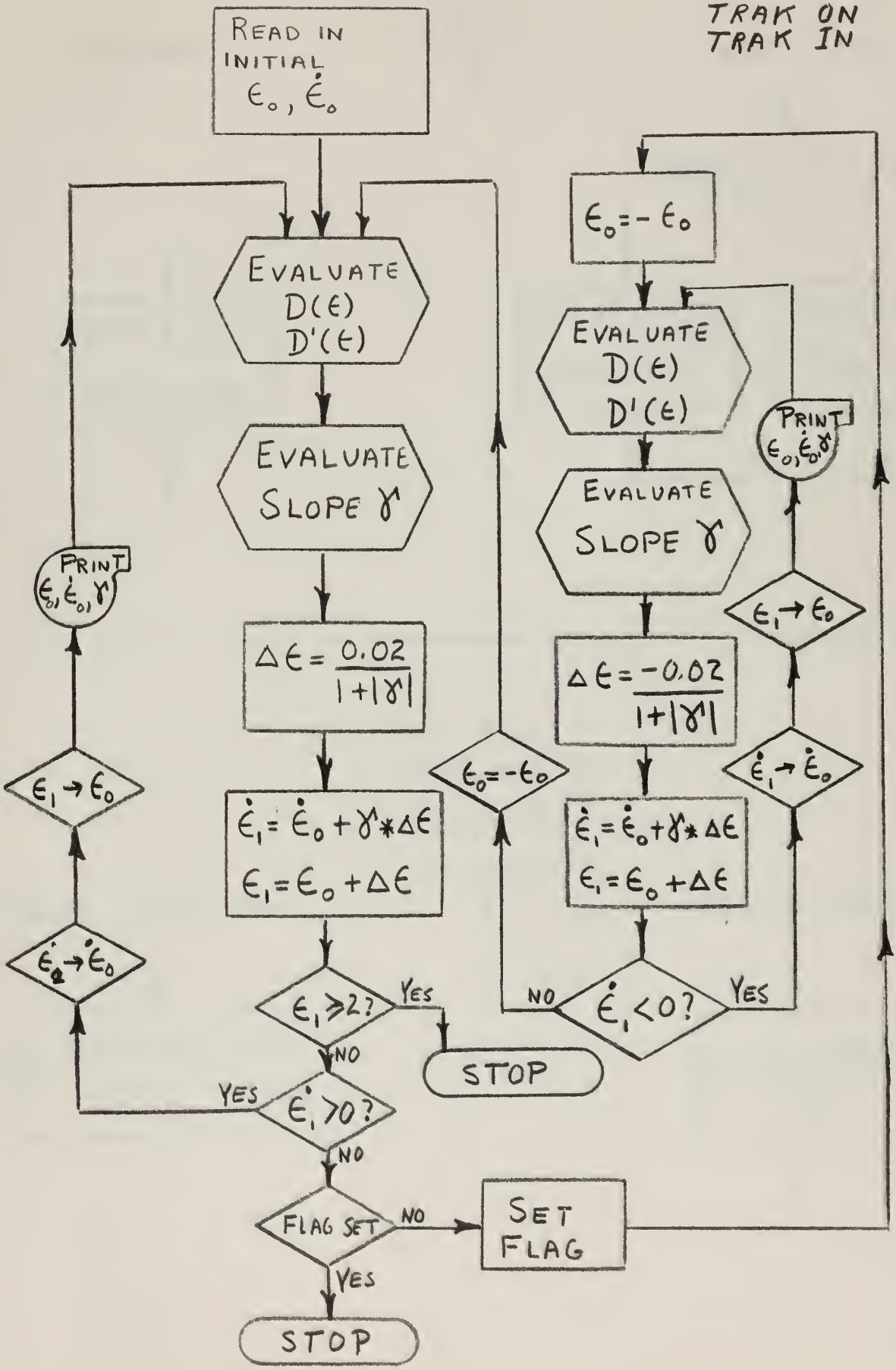
```
      PROGRAM DELAY 2
C     THIS PROGRAM PRODUCES REQUIRED 150 CLINES
C     FOR SOLUTION OF THE DELAY-LOCK DISCRIMINATOR
      DO 50 K=2,12,2
      SLOPE=0.0
      PRINT 22
      V=0.04
      W=K-2
      V=W*V
      PRINT 33,V
      DO 14 I=1,36
      N=5
      M=9
      L=18
      NM=23
      ML=27
      LN=36
      IF(SLOPE-50.0)51,61,51
   61 SLOPE=0.0
   51 IF(I-N)3,3,1
    1 IF(I-M)4,4,2
    2 IF(I-L)5,5,23
    3 SLOPE=SLOPE+0.2
      GO TO 6
    4 SLOPE=SLOPE+1.0
      GO TO 6
    5 SLOPE=SLOPE+5.0
      GO TO 6
   23 IF(I-NM)26,26,24
   24 IF(I-ML)27,27,25
   25 IF(I-LN)28,28,15
   26 SLOPE=SLOPE-0.2
      GO TO 6
   27 SLOPE=SLOPE-1.0
      GO TO 6
   28 SLOPE=SLOPE-5.0
    6 PRINT 55,SLOPE
      DO 13 J=0
      DO 13 J=1,38
      H=J
      E=-2.0 +0.1*H
      TEMP=ABSF(E)
      IF(TEMP-1.0)7,7,8
    7 PD1=E
      GO TO 9
    8 PD1=E+ 2.0*E/TEMP
    9 IF (TEMP-1.0)10,10,11
   10 PD2= 1.0
      GO TO 12
   11 PD2= -1.0
   12 Y=(PD1+SQRTF(2.0)*PD2*V)/(SLOPE+SQRTF(2.0)*PD2)
   13 PRINT 44,E,Y
   14 CONTINUE
      PAUSE
   50 CONTINUE
   15 STOP
   22 FORMAT(9H VELOCITY,3X,6H SLOPE,3X,8H E-VALUE,15X,8H Y-VALUE,//)
   33 FORMAT(F8.4,/)
   44 FORMAT(25X,F4.2,16X,F9.5,/)
   55 FORMAT(12X,F8.4,/)
      END
      END
```

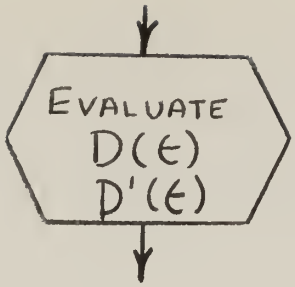
APPENDIX B

This appendix contains the Flow Diagrams and Fortran Source Programs required to generate the desired trajectories describing the lock-on behavior of the system. The results of these programs are shown in Section 4, Figures 4-2 through 4-7.

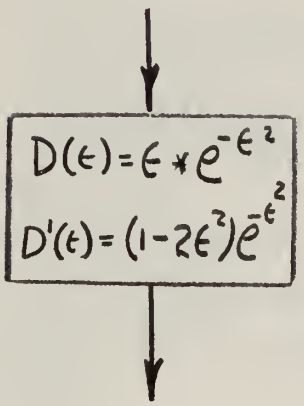
FLOW DIAGRAM
PROGRAMS:

LOCK ON
LOCK IN
TRAK ON
TRAK IN

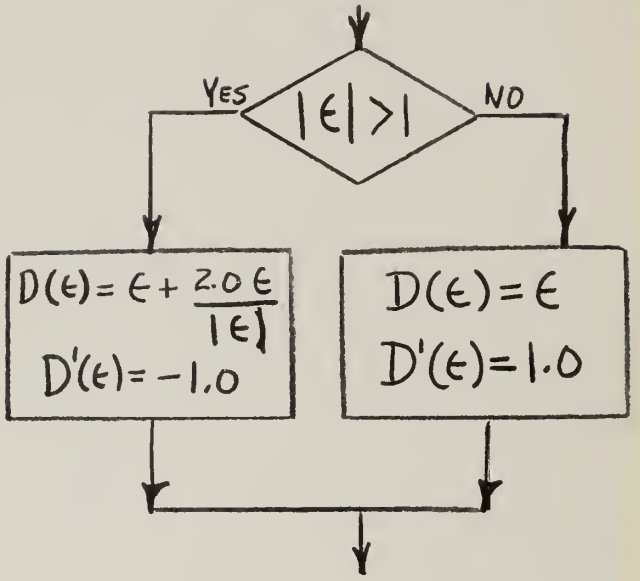




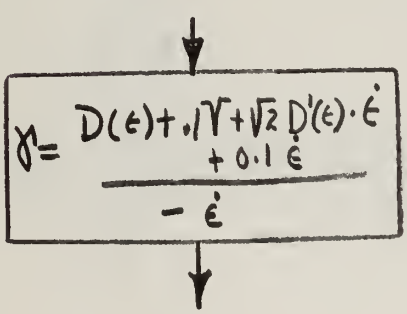
GAUSSIAN



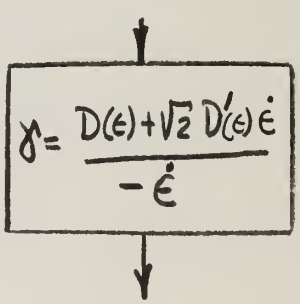
SAW TOOTH



FINITE LOOP GAIN



INFINITE LOOP GAIN



```
      PROGRAM LOCKON
    1 FORMAT(F10.5)
      READ 1,X2
    2 READ 1, Y
      X=X2
      PRINT 40
    3 E1=X*X
      C=2.7182818284
      PD1=X*(1.0/C**E1)
      PD2=(1.0-2.0*E1)*(1.0/C**E1)
      A=SQRTF(2.0)
      BETA=(PD1+(PD2*Y*A))/(-Y)
      TEMP=ABSF(BETA)
      IF(TEMP-0.5)31,31,32
   31 DELTA=0.1
      GO TO 33
   32 DELTA=0.01
   33 Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(X1-2.0)34,34,13
   34 IF(Y1)5,5,4
    4 PRINT 50,X1,Y1,BETA
      Y=Y1
      X=X1
      GO TO 3
    5 IF(DELTA-0.01)7,7,6
    6 DELTA=0.01
      GO TO 3
    7 DELTA=-0.01
      IF(X-0.1)12,12,8
    8 Y=-0.025
   81 E1=X*X
      C=2.718281284
      PD1=X*(1.0/C**E1)
      PD2=(1.0-2.0*E1)*(1.0/C**E1)
      BETA=(PD1+(PD2*Y*A))/(-Y)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(Y1)9,10,10
    9 PRINT 50,X1,Y1,BETA
      Y=Y1
      X=X1
      GO TO 81
   10 IF(X1+0.1)11,12,12
   11 Y=0.025
      DELTA=0.01
      GO TO 3
   12 PRINT 70
      PAUSE
      GO TO 2
   13 PRINT 60
      PAUSE
      GO TO 2
   40 FORMAT(8H X-VALUE,5X,8H Y-VALUE,5X,5H BETA,//)
   50 FORMAT(F8.5,5X,F8.5,5X,F8.5,/)
   60 FORMAT(11H NO LOCK-ON,//)
   70 FORMAT(8H LOCK-ON,//)
      END
      END
```

```
      PROGRAM LOCKIN
      READ 1,X2
    1 FORMAT(F10.5)
    2 READ 1,Y
      X=X2
      PRINT 40
    3 TEMP=ABSF(X)
      IF(TEMP-1.0)4,4,5
    4 PD1=X
      PD2=1.0
      GO TO 6
    5 PD1=X+2.0*X/TEMP
      PD2=-1.0
    6 A=SQRTF(2.0)
      BETA=(PD1+(PD2*Y*A))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(X1-2.0)7,7,19
    7 IF(Y1)9,9,8
    8 PRINT 50,X1,Y1,BETA
      Y=Y1
      X=X1
      GO TO 3
    9 CONTINUE
      IF(X-0.1)18,18,10
   10 Y=-Y
   11 TEMP=ABSF(X)
      IF(TEMP-1.0)12,12,13
   12 PD1=X
      PD2=1.0
      GO TO 14
   13 PD1=X+2.0*X/TEMP
      PD2=-1.0
   14 BETA=(PD1+(PD2*Y*A))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=-0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(Y1)15,16,16
   15 PRINT 50,X1,Y1,BETA
      Y=Y1
      X=X1
      GO TO 11
   16 IF(X1+0.1)17,18,18
   17 Y=-Y
      GO TO 3
   18 PRINT 70
      PAUSE
      GO TO 2
   19 PRINT 60
      PAUSE 2
      GO TO 2
   40 FORMAT(8H X-VALUE,5X,8H Y-VALUE,5X,5H BETA,//)
   50 FORMAT(F8.5,5X,F8.5,5X,F8.5,/)
   60 FORMAT(11H NO-LOCK-ON,//)
   70 FORMAT(8H LOCK-ON,//)
      END
      END
```

```
      PROGRAM TRAKON
    1 FORMAT(F10.5)
      READ 1,X2
    2 READ 1,Y
      V=-Y
      X=X2
      PRINT 40
      FLAG=0.0
    3 E1=X*X
      C=2.7182818284
      PD1=X*(1.0/C**E1)
      PD2=(1.0-2.0*E1)*(1.0/C**E1)
      A=SQRTF(2.0)
      BETA=((PD1+(0.1*V))+(Y*(A*PD2+0.1)))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(X1-2.0)4,4,12
    4 IF(Y1)6,6,5
    5 PRINT 50,X1,Y1,BETA,V
      Y=Y1
      X=X1
      GO TO 3
    6 IF(FLAG)7,7,11
    7 FLAG=1.0
      Y=-Y
    8 E1=X*X
      PD1=X*(1.0/C**E1)
      PD2=(1.0-2.0*E1)*(1.0/C**E1)
      BETA=((PD1+(0.1*V))+(Y*(A*PD2+0.1)))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=-0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(Y1)9,10,10
    9 PRINT 50,X1,Y1,BETA,V
      Y=Y1
      X=X1
      GO TO 8
   10 Y=-Y
      GO TO 3
   11 PRINT 70
      PAUSE
      GO TO 2
   12 PRINT 60
      PAUSE 2
      GO TO 2
   40 FORMAT(8H X-VALUE,5X,8H Y-VALUE,5X,5H BETA,5X,8H V-VALUE,//)
   50 FORMAT(F8.5,5X,F8.5,5X,F8.5,7X,F10.5,/)
   60 FORMAT(11H NO-LOCK-ON,//)
   70 FORMAT(8H LOCK-ON,//)
      END
      END
```

```
      PROGRAM TRAKIN
    1 FORMAT(F10.5)
      READ 1,X2
    2 READ 1,Y
      V=-Y
      X=X2
      PRINT 40
      FLAG=0.0
    3 TEMP=ABSF(X)
      IF(TEMP-1.0)4,4,5
    4 PD1=X
      PD2=1.0
      GO TO 6
    5 PD1=X+2.0*X/TEMP
      PD2=-1.0
    6 A=SQRTF(2.0)
      BETA=((PD1+(0.1*V))+(Y*(A*PD2+0.1)))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(X1-2.0)7,7,19
    7 IF(Y1)9,9,8
    8 PRINT 50,X1,Y1,BETA,V
      Y=Y1
      X=X1
      GO TO 3
    9 IF(FLAG)10,10,18
   10 FLAG=1.0
      Y=-Y
   11 TEMP=ABSF(X)
      IF(TEMP-1.0)12,12,13
   12 PD1=X
      PD2=1.0
      GO TO 14
   13 PD1=X+2.0*X/TEMP
      PD2=-1.0
   14 BETA=((PD1+(0.1*V))+(Y*(A*PD2+0.1)))/(-Y)
      TEMPO=ABSF(BETA)
      DELTA=-0.02/(1.0+TEMPO)
      Y1=Y+BETA*DELTA
      X1=X+DELTA
      IF(Y1)15,16,16
   15 PRINT 50,X1,Y1,BETA,V
      Y=Y1
      X=X1
      GO TO 11
   16 Y=-Y
      GO TO 3
   18 PRINT 70
      PAUSE
      GO TO 2
   19 PRINT 60
      PAUSE 2
      GO TO 2
   40 FORMAT(8H X-VALUE,5X,8H Y-VALUE,5X,5H BETA,5X,8H V-VALUE,//)
   50 FORMAT(F8.5,5X,F8.5,5X,F8.5,7X,F10.5,/)
   60 FORMAT(11H NO-LOCK-ON,//)
   70 FORMAT(8H LOCK-ON,//)
      END
      END
```