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**Digital Signal Processor
for a Test-Bed Ocean-Surveillance Radar**
[Unclassified Title]

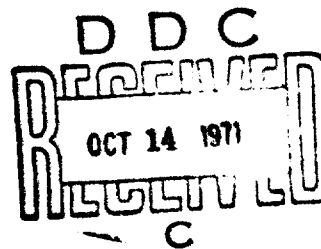
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*Aerospace Radar Branch
Radar Division*

August 26, 1971



NAVAL RESEARCH LABORATORY
Washington, D.C.



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ABSTRACT
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A digital signal processor for a scaled-down test-bed model of a satellite ocean-surveillance radar system has been developed. This processor employs a digital-feedback integrator technique to achieve improved system signal-to-noise-plus-clutter characteristics required for automatic detection. State-of-the-art integrated circuitry is used, including large-scale-integrated (LSI) high-speed shift registers. The radar video is processed and digitally compared to a threshold level adaptively determined from separately processed average clutter-plus-noise data to determine the occurrence of detections. The processor also includes provision for the recording of radar-video, timing, and antenna-rotation data on magnetic tape during flight testing. These tapes then form a library of radar flight data that are subsequently decoded and processed at the laboratory.

PROBLEM STATUS

This is a final report on one phase of the NRL Problem; work on other phases continues.

AUTHORIZATION

NRL Problem R02-46
Project A3705383-652B-1F48111704

Manuscript submitted June 16, 1971.

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DIGITAL SIGNAL PROCESSOR FOR A TEST-BED
OCEAN-SURVEILLANCE RADAR
(Unclassified Title)

INTRODUCTION

(S) The Naval Research Laboratory is engaged in the development of satellite radars for ocean surveillance. This effort includes the design and implementation of signal processors using digital techniques to provide increased probability of detection of ship targets through enhancement of the signal-to-noise-plus-clutter ratio. Digital signal processors are able to provide the high-reliability, dense-packaging, and low-power characteristics inherent in solid state integrated circuitry and required in satellite ocean-surveillance radar systems. Following conversion to digital format, no degradation of the characteristics of the radar signal occurs during subsequent processing or storage. Processed signal data are available in a form applicable to a general-purpose computer for further target evaluation.

(S) An exhaustive parametric study, using computer analysis, of various types of satellite-borne ocean-surveillance radars has been carried out and documented (1). As a result of this study which considered such factors as detection performance, feasibility, cost, reliability, size, weight, and power requirements, a side-looking noncoherent radar was determined to be the most practical for ocean surveillance. Using these results and additional computer analyses, the characteristics of a scaled-down test-bed model of a satellite ocean-surveillance radar were established (2).

(S) The basic specifications of the digital processor for the test-bed system were determined by the required range resolution of 50 ft and pulse repetition frequencies (PRF) of 62.5 and 39.0625 Hz. An overall range-extent processing capability of approximately 77 mi in 15 selectable 10-mi overlapping intervals was chosen to provide adequate coverage while limiting physical hardware requirements. Thus at least 1200 range bins, of 50-ft resolution corresponding to a 10-mi interval, were to be processed at a 10-MHz rate.

DIGITAL FEEDBACK INTEGRATOR

(U) The basic processor unit chosen was a digital feedback integrator, as shown in Fig. 1, analogous to the old-type analog integrator with RC-type delay line. This integrator consists of a digital source representative of the input signal, an input binary adder, a multilevel binary shift register of length equal to the number of range bins to be processed, and a feedback binary multiplier. A digital sample of the radar return from each transmitted pulse is obtained for every range bin to be processed. The sample for a particular range bin is added to the weighted sum of all previous samples for that range bin and shifted into the register. The samples must be obtained and therefore shifted at a rate determined by the desired range resolution, with one shift pulse for each range bin. Each of these sums is shifted through the register and properly weighted with binary multiplication by a feedback factor $k < 1$. This feedback factor has two effects. First, it prevents the stored value for each range bin from exceeding the word size of the shift register. The maximum word size in bits is limited to the input word size plus the quantity $\log_2 (1 - K)^{-1}$. Second, the feedback factor causes nonrecurring samples to decay, thus discriminating against noise while allowing repetitive target returns to accumulate. The number of returns integrated at any point in time is a function of the feedback factor. The implementation of this integrator as employed in the system will be discussed later.

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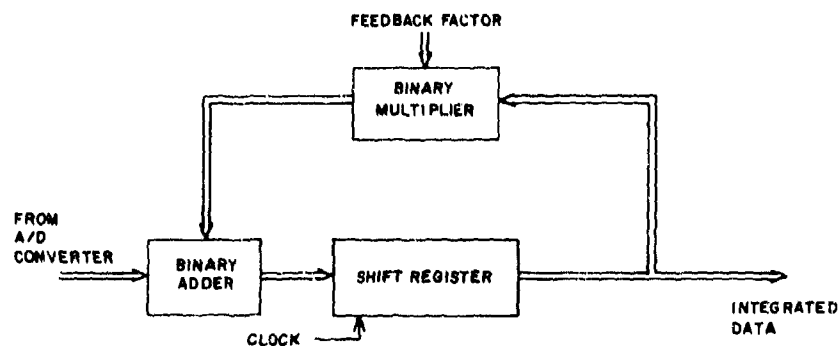


Fig. 1(U) - Digital feedback integrator

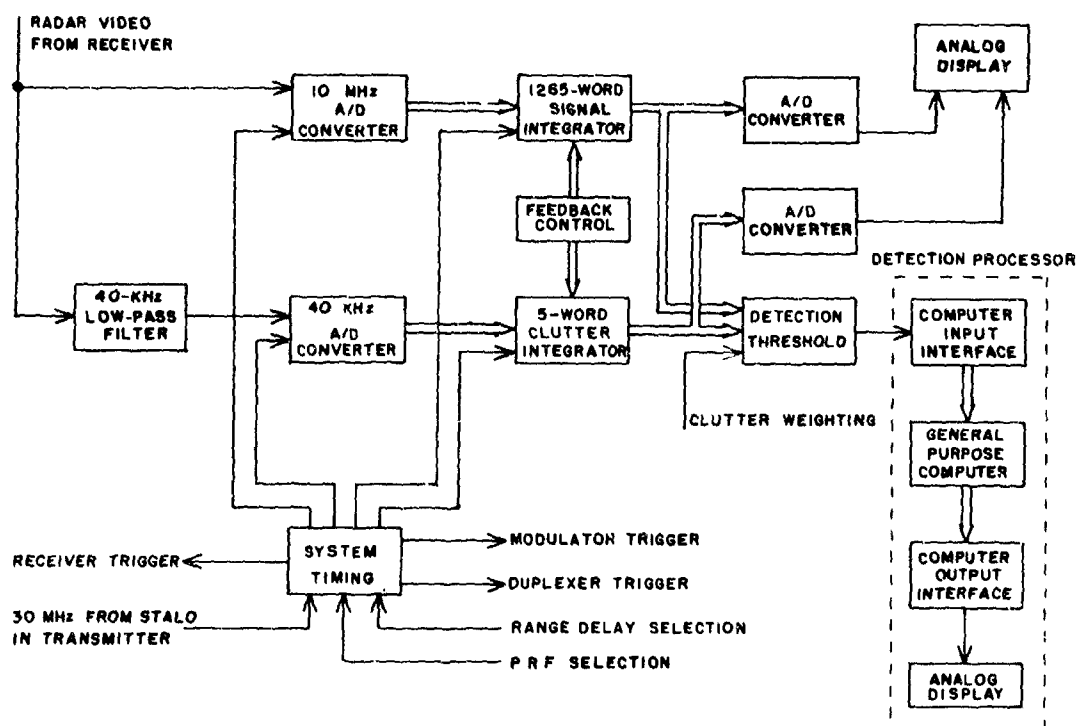


Fig. 2(S) - Digital Signal Processor

DIGITAL SIGNAL PROCESSOR

(S) A block diagram of the overall digital signal processor is shown in Fig. 2. The system timing generates all the timing pulses required by the processor and also generates the triggers for the receiver, duplexer, and modulator components of the radar system. Provision is included for selection of one of two system PRF rates, as well as selection from among the 15 available range delays. All timing signals are derived from the 30-MHz reference supplied by the stable local oscillator in the transmitter. The radar video from the receiver is continuously sampled at a 10-MHz rate by a high-speed A/D converter.

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These samples are applied to a 1265-word integrator which accepts data for integration only over the time interval corresponding to the particular 10-mi-range interval to be processed.

(S) The radar video is also applied to a 40-kHz, low-pass filter to provide an average clutter-plus-noise level, filtering out the effects of any targets which may be present. The output of this filter is applied to an A/D converter and digitized at a rate equal to 1/253 of 10 MHz or approximately 40 kHz. This digitized average clutter is applied to a five-word clutter integrator which performs integration during a selected range interval at a rate equal to 1/253 of that of the signal integration. By means of a front-panel switch, six feedback factors ranging from 0.875 to 0.996 can be selected. Unity feedback is also available as a means of checking integrator operation. The results of the signal-and-clutter integration are converted to analog form and displayed on an oscilloscope. This provides a display for visual analysis of the integrator-enhanced radar video with respect to the integrated average clutter-plus-noise.

(U) Following real-time integration, the feedback factors in the integrators are switched to unity, and the registers are shifted end-around once at 1/10 the integration rate. This provides a real-time integrated output immediately followed by a second stretched-out representation. This lower integrator output rate is more compatible with the speed of the detection threshold circuitry and is more reasonable for subsequent data presentation to the magnetic-core storage medium of the general purpose computer.

(U) In the detection-threshold circuitry, the results of the signal-and-clutter integration are digitally compared. A detection pulse is generated whenever the signal level is above a specified clutter threshold. This threshold is effectively varied by weighting up or multiplying the integrated clutter magnitude by integral factors up to 11 to reduce false alarms.

(S) The results of the digital signal processing will be presented to the detection processor for further processing. In the computer interface the detection results for each range bin across the swath are formatted for direct input to the memory of the general-purpose digital computer. In this computer the detection results are processed using various experimental ship-detection and land-mass-blanking algorithms to determine the feasibility of detecting ship targets from a satellite platform. The results of the computer processing are reformatted and presented to an oscilloscope for visual display. This display presents range bins in delayed-time correspondence, with processed ship targets indicated by pulses.

(U) The system also contains an additional provision for the storage of the radar-video, PRF-timing, and antenna-angle data on video tape during actual flight tests. This provides a library of radar data that can be repeatedly and thoroughly analyzed off-line at the laboratory.

Circuit Utilization

(U) Before discussing the details of the operation and implementation of each of the major components indicated in Fig. 2, the basic circuit utilization will be discussed. With the exception of some analog and switching circuitry used in pulse amplifiers, level detectors, and digital-to-analog converters, transistor-transistor-logic (TTL) integrated circuitry is used throughout. Small-scale, medium-scale, and large-scale integrated circuits, that is, SSI, MSI, and LSI circuits, of full military temperature range capability, are used. The flat-pack format is the one most commonly used, although some dual-in-line plastic

packages are employed where advantageous. These circuits are mounted on printed circuit boards according to logical function. When a particular board is used in sufficient quantity, special-purpose boards are used. When the amount of use does not warrant the costs involved in the layout and fabrication of a special board, so-called standard boards with provisions for up to eight flat-packs or 12 dual-in-line packages are employed.

System Timing

(U) All of the timing signals required by the digital signal processor as well as by the rest of the radar system are supplied by the system timing generator. All timing pulses are developed by counting down from the 30-MHz stable local oscillator in the transmitter. To maintain accurate timing, all timing pulses are generated by means of synchronous counters. Synchronism in this case means exact coincidence (within one flip-flop propagation delay) of the pulse which indicates completion of a count of n with the leading edge of the n th clock pulse. This is in contrast to the counting delay inherent in simple binary counters in which the effects of each updated count must ripple through the various stages. This condition is intolerable in the present case which requires highly accurate timing. The upper diagram in Fig. 3 shows the look-ahead-type synchronous counter, used here for the particular case $n = 10$. This counter consists basically of a simple ripple-through binary counter plus an additional synchronizing flip-flop. The flip-flops are leading-edge-triggered D types. If it is desired to synchronously count to n , the occurrence of the counter state representing $n - 1$ is detected by means of gating. This detection is shifted into the extra flip-flop by the next or n th clock pulse. The pulse output of this flip-flop then indicates the attainment of a count of n and is leading-edge-coincident with the n th clock pulse, within the delay time of the flip-flop. The basic binary counter is reset by the synchronizing flip-flop to prepare for the next count cycle. At the occurrence of the $n + 1$

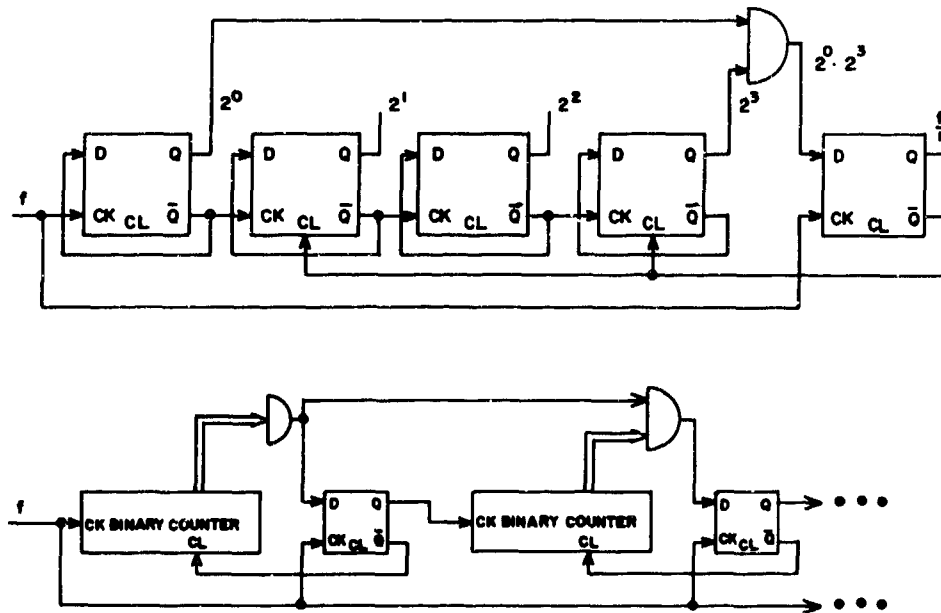


Fig. 3(U) - Look-ahead synchronous counter logic diagram and multistage synchronous counter

clock pulse, the synchronizing flip-flop is reset. The lower part of Fig. 3 shows how these counters can be connected for multistage frequency division. Figure 4 is a simplified diagram showing how the two system PRF's are synchronously obtained using this procedure. Figure 5 shows the standard timing card containing two general-purpose, four-bit synchronous counters.

(S) The block diagram of the system timing generator is shown in Fig. 6. Starting from the 30-MHz reference, the PRF's are developed as described above and are selected by means of a switch on the front panel. Various timing information generated within the counter stages is used as required in generating the system timing. A 100-kHz timing signal with an interpulse period of $10\ \mu\text{s}$ is frequency divided by 6 in a counter which is enabled at $31\ \mu\text{s}$ beyond the PRF pulse. The divided signal with a $60\text{-}\mu\text{s}$ period is applied to a divide-by-n counter, with the final count n designated by the particular range delay selected. This counter is completely synchronous; thus any count n, from 1 to 15, is synchronous with the basic system clock. The output from this divide-by-n counter is a

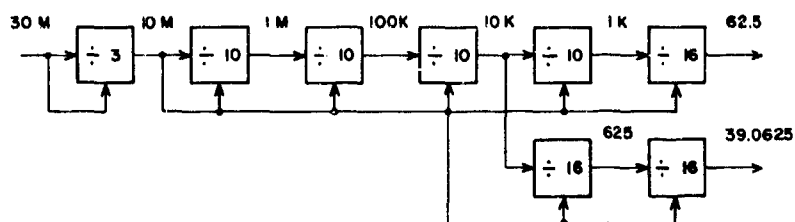


Fig. 4(S) - PRF generator

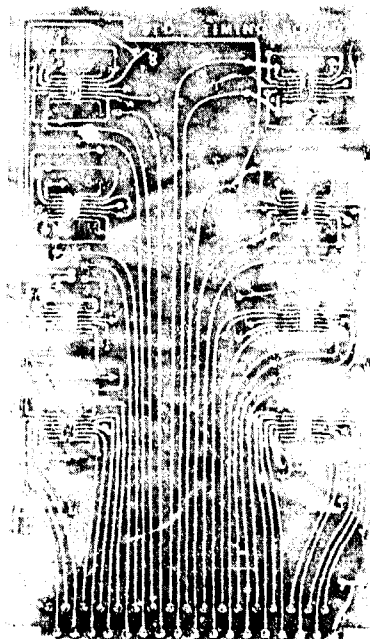


Fig. 5(U) - System timing card

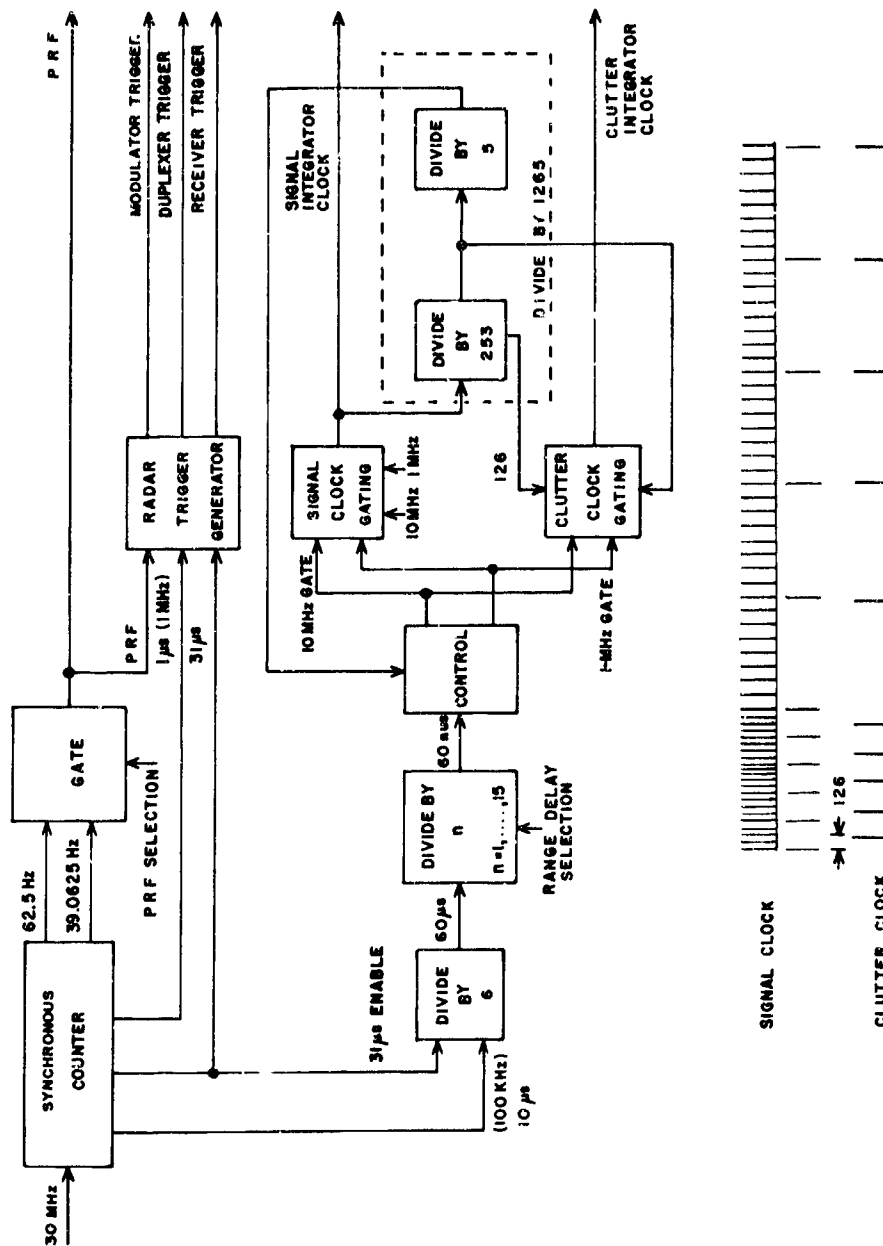


Fig. 6(S) - System timing generator

pulse delayed $(60n + 31) \mu s$ from the PRF pulse. This pulse initiates the generation of the integrator clocks and thus determines the position in range relative to time of the 10-mi swath to be processed. At $(60n + 31) \mu s$ a 10-MHz clock signal is gated to a divide-by-1265 counter consisting of three synchronous stages: a divide-by-5, a divide-by-11, and a divide-by-23 counter, the latter two combined and shown on the block diagram as a divide by 253. After 1265 of these 10-MHz pulses are counted, the 10-MHz signal is gated off, and a 1-MHz clock is gated into the counter. These 1-MHz pulses are counted until 1265 are detected, and then the control gates are inhibited until the next PRF interval. Thus the output of the signal clock gating or the counter input at the selected range delay has a burst of 1265 10-MHz pulses, each of period 100 ns, followed immediately by 1265 1-MHz pulses, each of period $1 \mu s$, to form the signal integrator clock. The higher frequency pulses in the integrator clock train are used during real-time integration, and the lower frequency pulses are used to shift out the integrated data at a reduced rate for further processing. The clutter integrator clock is obtained in two ways, due to a requirement for sampling the clutter in the middle of the corresponding clutter cell. During the 10-MHz portion of the signal integrator clock, certain states of the divide-by-11 and divide-by-23 counters are used to generate pulses at the required positions. A count of 126 is detected in the divide-by-253 counter and gated out as the clutter integrator clock during the 10-MHz portion of the signal integrator clock. During the 1-MHz portion, the output of the divide-by-253 counter forms the clutter integrator clock. The timing diagram of Fig. 6 indicates the relation between signal and clutter integrator clocks. During real-time (10-MHz) processing, the first and subsequent clutter samples are taken and shifted into the integrator in the middle of each of the 253 range-bin segments forming the respective clutter cells. During the data shiftout (1-MHz) portion of operation, the clutter integrator is shifted after 253 signal clock pulses. Thus, in the detection threshold circuit the integrated clutter samples taken at the middle of each clutter cell are used to set the threshold over the entire 253 range bins corresponding to that clutter cell.

(S) The receiver, duplexer, and modulator triggers are synchronously generated using some intermediate timing signals available from within the basic frequency-dividing counter. The time relationships of these triggers as well as the range delay are shown in Fig. 7.

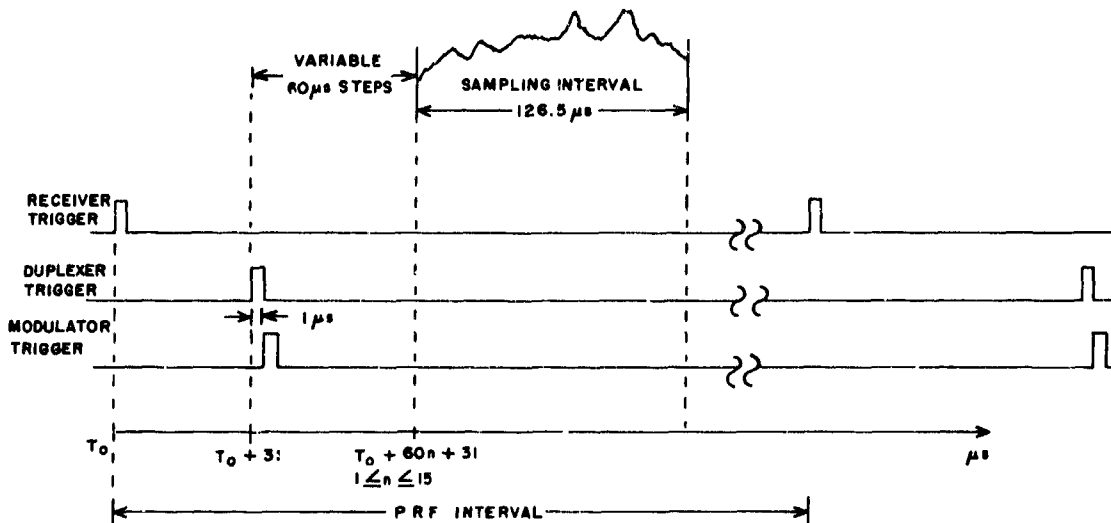


Fig. 7(U) - System timing diagram

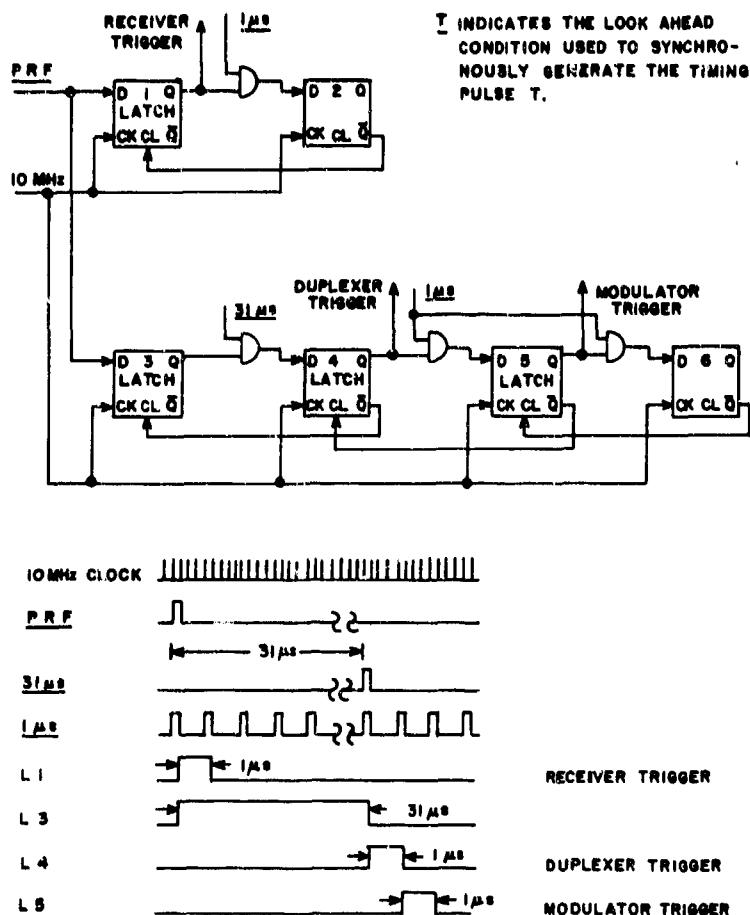


Fig. 8(U) - Radar trigger generator

The radar triggers are generated as shown in the logic and timing diagrams in Fig. 8. The underlined timing signals, as shown, actually occur 100 ns or one 10-MHz clock period earlier than indicated and can be thought of as setup conditions used in anticipation of a particular point in time to produce synchronous operation. The PRF setup condition is clocked into latching flip-flops 1 and 3 by the 10-MHz clock exactly at the start of the PRF interval. At the following 1- μ s setup condition the content of latch 1 is clocked into flip-flop 2, which then clears latch 1. Thus the output of latch 1 is a 1- μ s receiver trigger pulse which is leading-edge coincident with the leading-edge of the PRF pulse. At 31 μ s beyond the PRF pulse the content of latch 3 is clocked into latch 4, which then clears latch 3. The 1- μ s setup condition gates the contents of latch 4 so that it is clocked into latch 5, which resets latch 4, producing a 1- μ s duplexer pulse at its output at exactly 31 μ s beyond the PRF pulse. After another 1- μ s interval the contents of latch 5 is clocked into flip-flop 6, which resets latch 5, producing a 1- μ s modulator pulse which is 32 μ s beyond the PRF pulse. Flip-flops 2 and 6 are reset by subsequent 10-MHz clock pulses.

High-Speed Analog-to-Digital Converter

(U) The high-speed analog-to-digital converter, on command of a sample pulse, generates a four-bit binary representation of the analog input-signal amplitude. The

block diagram of this device is shown in Fig. 9. The input signal is isolated from the sample-and-hold circuitry by an attenuator and an amplifier. On command of the sample pulse the input voltage is sampled by the sample-and-hold circuitry. This sample-and-hold circuitry is used to reduce the error due to a changing input voltage. The sampled voltage is acquired, stored on a capacitor, and isolated from the low-impedance comparators by an FET power buffer. The sampling circuitry must then be rapidly removed from the input signal. The time required to accomplish this is defined as the aperture time and is a measure of sample-and-hold accuracy. It is less than 500 ps for this unit.

(U) The sampled signal level is compared in the comparators to various threshold levels determined by a reference power supply and precision, resistive voltage dividers. The reference threshold at each comparator is spaced so that the input voltage range is divided into 2^n equal segments, where $n = 4$. This requires $2^n - 1$ or 15 comparator circuits. The outputs of the comparators are decoded using combinatorial-logic circuitry to yield the required binary outputs, which are strobed into the output storage register by a delayed sample pulse. With the comparators arranged so that as the input signal level is increased, each higher numbered comparator is triggered, the logical expression for binary output 2^2 for example, is $4 \cdot 8 + 12$. This indicates the condition when the threshold of comparator 4 has been exceeded and that of 8 has not, or when the threshold of comparator 12 has been exceeded. This is equivalent to saying that the 2^2 output bit will be true (logical "1") when the input signal level is between $1/4$ and $1/2$ or above $3/4$ of the full-scale reference voltage (which is +5 V in this case). Figure 10 shows the two printed circuit cards that form the converter. The card on the right consists of the sample-and-hold circuitry as well as the buffer circuits. The card on the left has the comparators, the decoder, and the output storage register.

Signal Integrator

(S) The design of the signal integrator was determined by many factors. The system requirement for 50-ft range bins led to an integration rate of 10 MHz. A 10-mi swath then required at least 1200 range bins. Desire for feedback factors up to 0.996, permitting integration of up to 256 or 2^8 radar pulses, combined with an A/D sample resolution of four bits, led to a necessity for a 12-bit representation of the weighted sum for each integrated range bin. Since the feedback multiplication is done by a binary addition, the overall integrator timing requirements called for two 12-bit binary additions, a register shift, and other gating within 100 ns. After surveying state-of-the-art MOS and bipolar shift-register characteristics, an LSI bipolar shift-register integrated circuit containing two 253-bit registers was selected. This unit was completely compatible with TTL circuitry that would interface with it in the processor. Although the shift register was capable of being shifted within 50 ns at a rate of at least 10 MHz, the fastest binary adders available were limited to a typical 12-bit addition speed of about 40 ns at 25°C. To overcome limited adder speeds and provide a margin for reliable operation, it was decided to divide the integrator into five equal subintegrator segments, each of a 253-bit length, with utilization of data distribution and multiplexing to achieve an overall integrator operation length of 1265 bits. This permits each of the five subintegrators to operate at a rate of 2 MHz. Thus the allowable time between shift pulses in each integrator is then 500 ns, permitting standard TTL adders to be used with a 12-bit capability of 180 ns, maximum.

(S) A block diagram of the signal integrator appears in Fig. 11. The samples from the 10-MHz A/D converter are alternately distributed in time-shared fashion to each of the five subintegrators by five time-multiplexed clocks generated in the clock distributor from the signal-integrator clock. In each of the subintegrators these samples are added to the weighted sum corresponding to the particular range bin sampled. These sums are

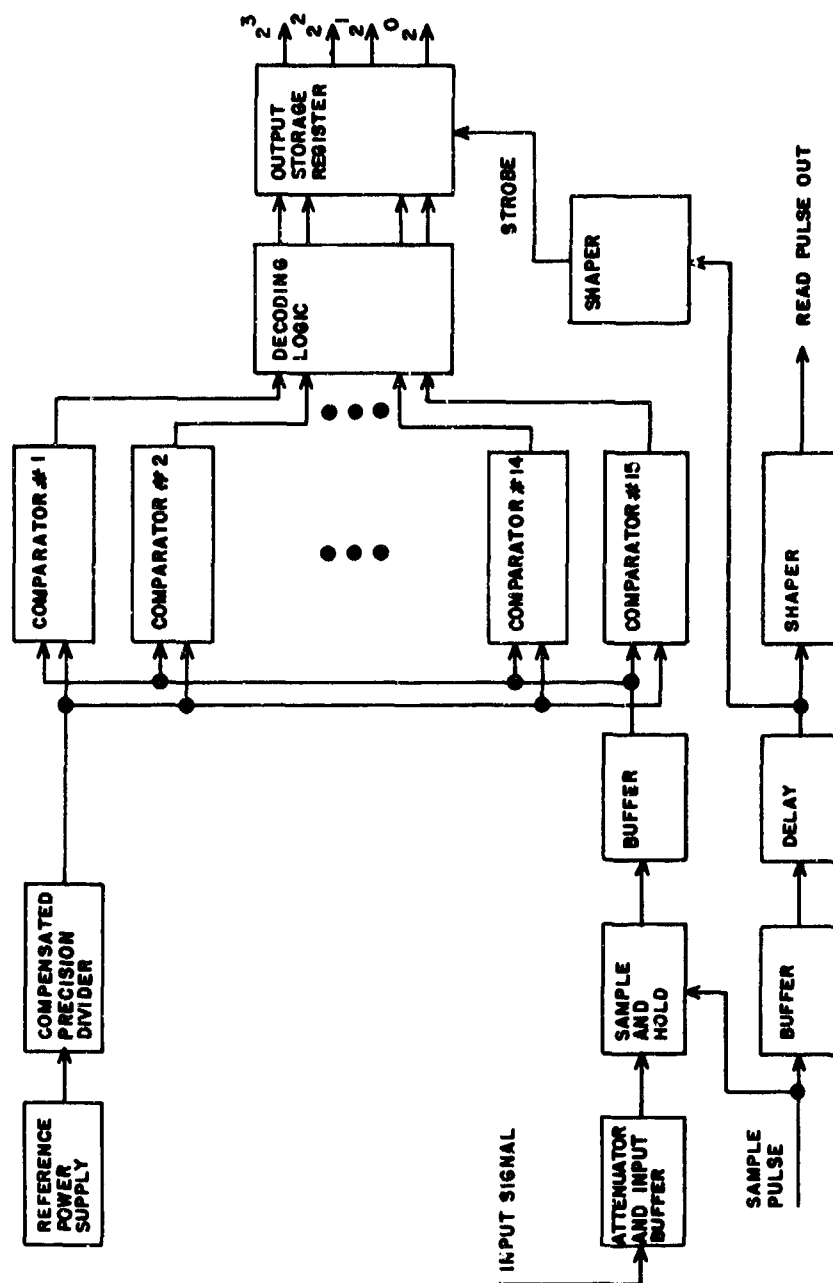


Fig. 9(U) - High-speed analog-to-digital converter

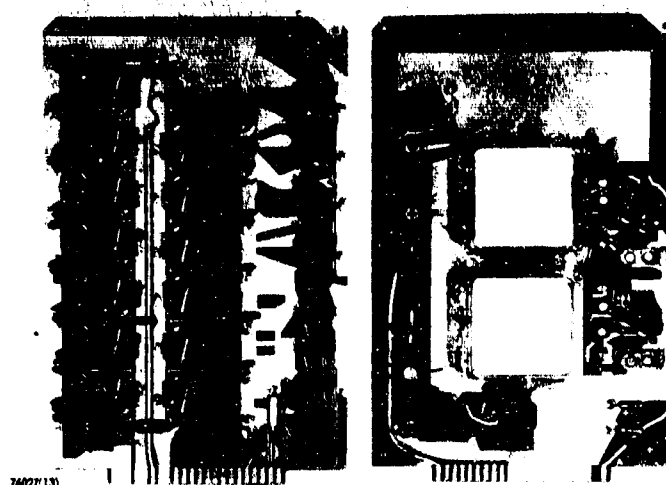


Fig. 10(U) - High-speed analog-to-digital converter circuit cards

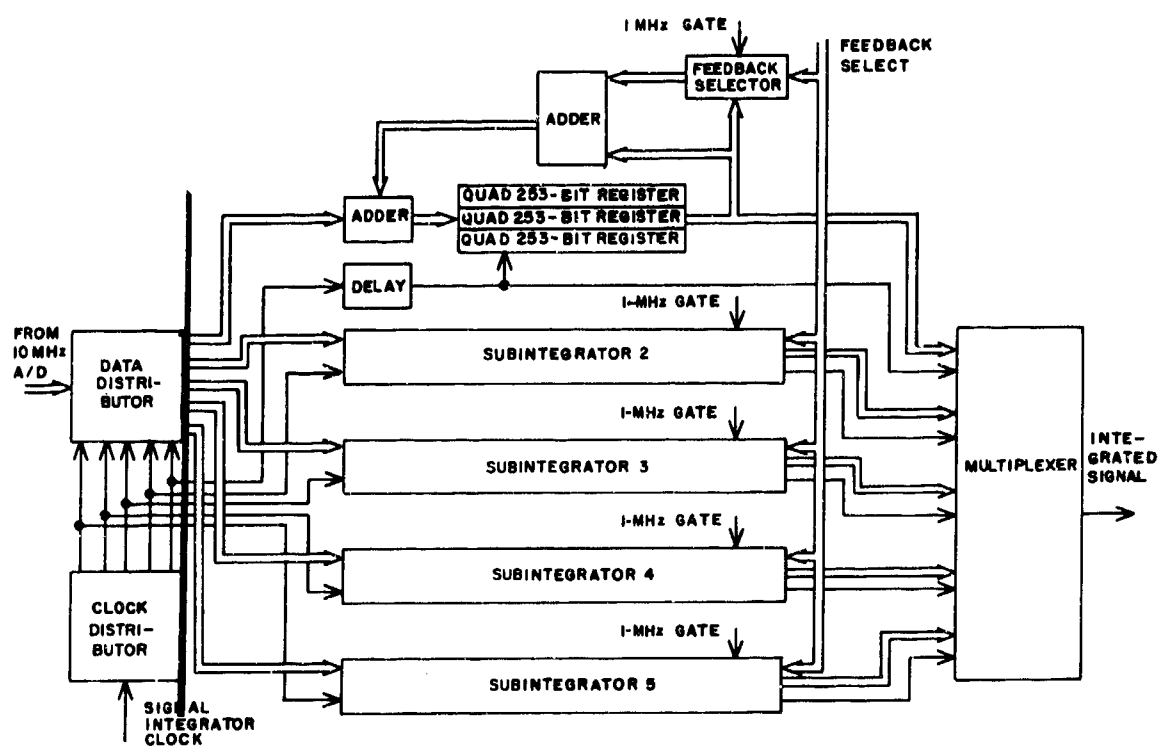


Fig. 11(S) - Signal integrator

shifted into the subregisters by the delayed time-multiplexed clocks. To multiply the output of a subregister S by k , the output is divided by 2^n by a right shift of n bits to form $S/2^n$, complemented to get $-S/2^n$, and added to S to form $S(i - 1/2^n)$, where $k = 1 - 1/2^n < 1$. The number of bits shifted, and thus k , is determined by external switching at the front panel. In the multiplexer each of the 253-bit subintegrators are alternately gated in time correspondence to form the equivalent of the 1265-bit integrator. As mentioned previously, the signal integrator clock consists of 1265 10-MHz pulses followed by 1265 1-MHz pulses. During the lower clock rate, the feedback selector is gated to force the feedback to $k = 1$, thus shifting out the integrated data at the lower rate back into the shift registers, thus readying the integrator for the next radar return. This lower integrator output rate is used in the detection threshold. Lower data rates are also required for subsequent processing in the general-purpose computer.

(U) The shift registers in each subintegrator are made up of twelve 253-bit registers. The LSI packages each contain two registers, and two packages are mounted on a printed circuit card, as shown in Fig. 12. Thus each card forms a quad 253-bit register module with three cards for each subintegrator. The other side of these cards contains clock-phasing, data-complementing, and driver circuitry. Figure 13 shows one of the many adder cards used in the signal integrator.

Clutter-Channel Analog-to-Digital Converter

(U) The clutter-channel analog-to-digital converter* changes the low-pass filtered radar video to digital format. Figure 14 is a block diagram of the converter. The analog



Fig. 12(U) - Quad 253-bit shift register card

*Patent application filed and approved, U.S. Patent Office, Navy Case 49329, "High-Speed Parallel Analog-To-Digital Converter," L.M. Leibowitz and R.K. Baldauf

Fig. 13(U) - Basic adder card



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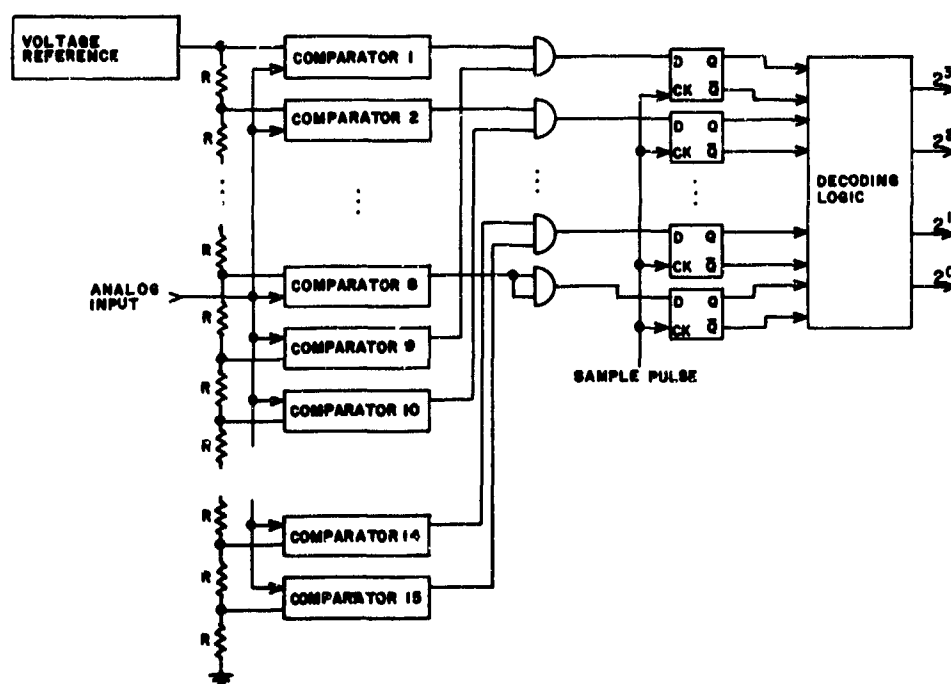


Fig. 14(U) - Clutter-channel analog-to-digital converter

input is compared to each of $2^4 - 1$ or 15 levels, set by means of a voltage reference and a series resistive divider. The results of the k th comparator are combined in a gate with that of the $(k+8)$ th comparator, so that the conversion is performed in two ranges above or below the midpoint, as detected by comparator 8. The sample pulse clocks the combined results of the level comparisons into a parallel register. Using simple combinatorial logic circuitry with two levels of logic to each output line, the four-bit binary representation of the analog input is presented with uniform delays. The comparator card shown in Fig. 15 is one of four cards that make up this A/D converter. It contains eight comparator circuits which are mounted on a general-purpose flat-pack board.

(U) Since this converter does not employ a sample-and-hold circuit, its speed is determined by the comparators, which require a maximum of 40 ns to detect a given level. Thus the fastest varying sine wave that can be resolved in each detected level has a frequency of about 250 kHz.

Clutter Integrator

(U) The block diagram of the clutter integrator is shown in Fig. 16. Because of the low integration rate and the short integrator length, the clutter integrator is relatively simple. Its operation is identical to that of each of the subintegrators in the signal integrator described earlier. The register is composed of 12 five-bit MSI shift registers, which are wired to store five 12-bit words. The clutter-integrator shift register with 12 dual-in-line integrated circuits is mounted on a general-purpose card and shown in Fig. 17.

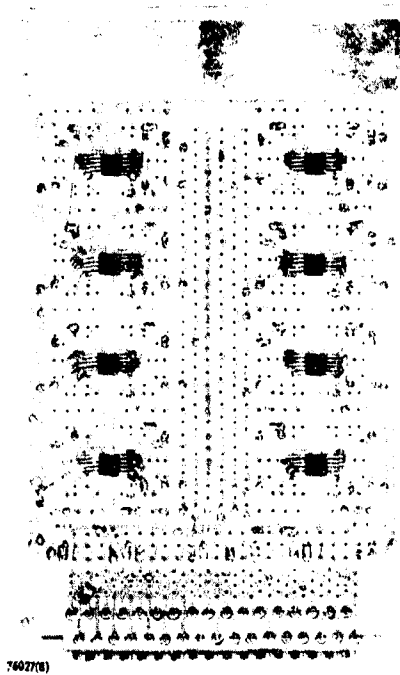


Fig. 15(U) - Comparator Card

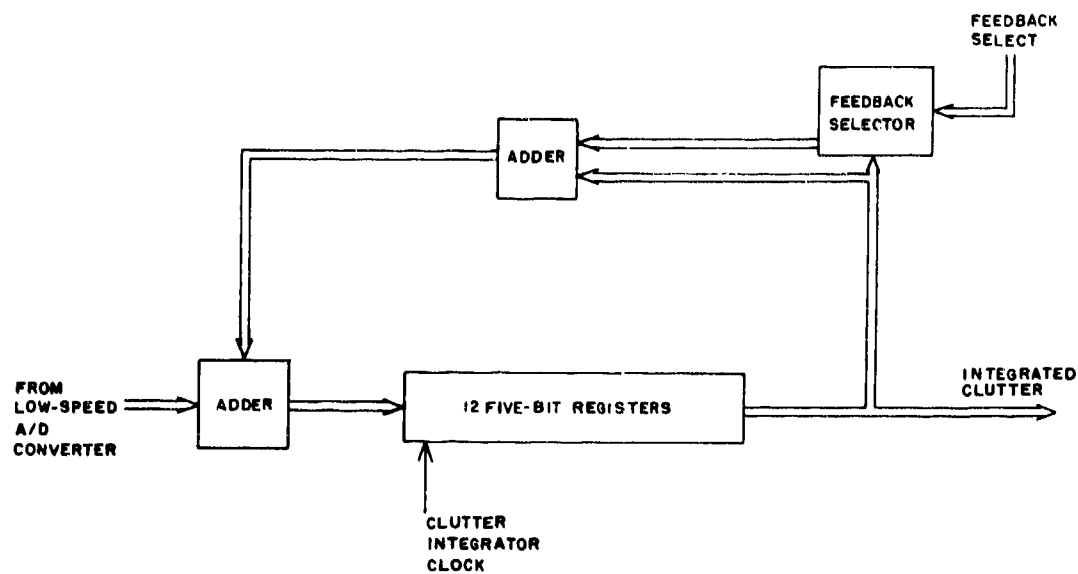


Fig. 16(U) - Clutter integrator

Fig. 17(U) - Clutter-integrator shift-register card



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Digital-to-Analog Converters

(U) The same 12-bit digital-to-analog converters are used in both the signal and clutter channels. Figure 18 is a block diagram of this converter. Each of the input bits is inverted and applied to an analog switch that switches between 0 V and +5 V, depending on the input bit. The output of each of the analog switches is applied to a shunt leg of a binary resistor ladder. In the ladder the output of the analog switch is binary weighted and summed according to the significance of the particular bit. Thus bit 1 is weighted by $1/2^{12}$ and bit 12 by $1/2$. The weighted sum is applied to an emitter-follower circuit to obtain relative impedance isolation with the output.

(U) For accurate conversion the analog-switch output must be capable of full-range switching between the extremes of 0 V and +5 V through a low impedance. The analog switch therefore consists of a switching transistor with low emitter-saturation voltage, with a collector supply of +12 V, and with a collector-catching diode to +5 V. The 12-bit D/A converter card is shown in Fig. 19.

Detection Threshold

(U) The detection threshold circuitry digitally compares the signal integration results with threshold levels derived from the integrated clutter to reduce the probability of false alarms. The threshold is determined by digitally multiplying the integrated clutter by selected factors from 1 to 11 corresponding to 0 to 20.8 dB. Whenever the integrated signal level exceeds the threshold, a detection indication in the form of a logic level is generated. By selecting a higher clutter-weighting factor, the integrated signal level at which a detection occurs will be higher.

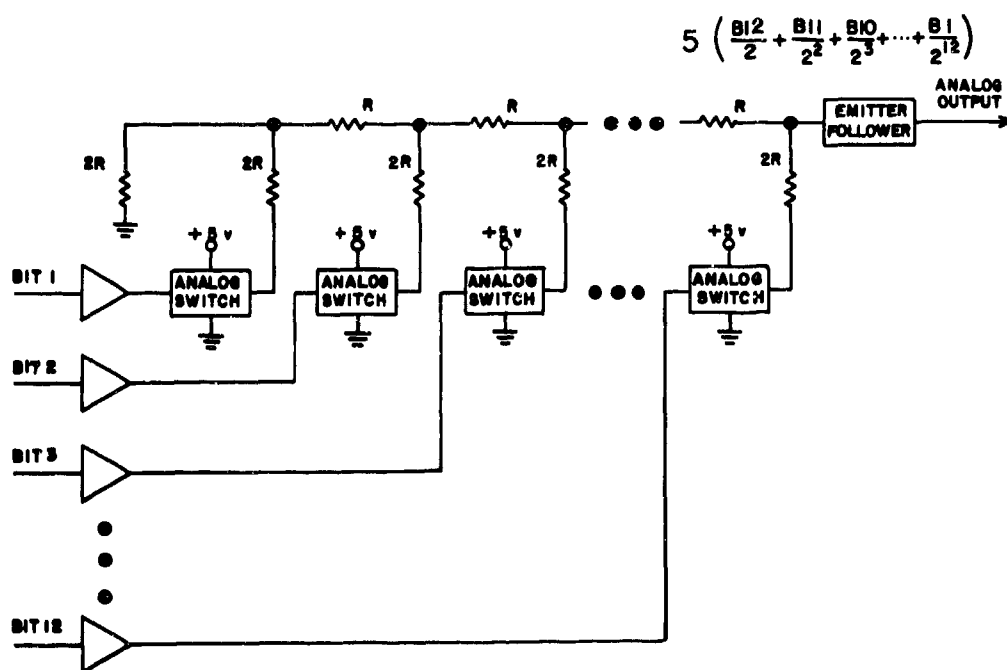
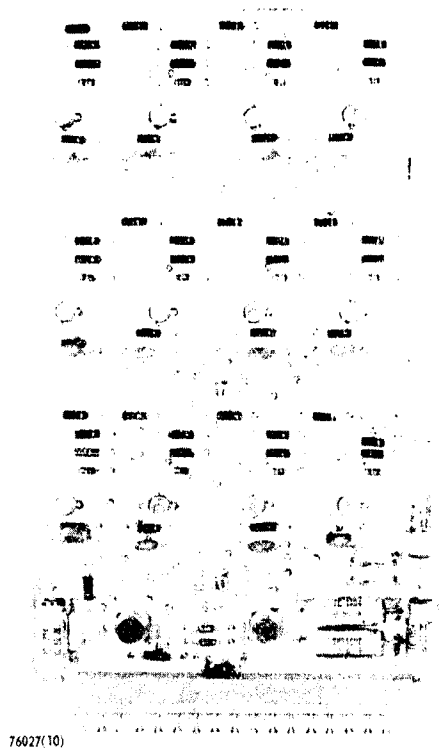


Fig. 18(U) - Digital-to-analog converter

Fig. 19(U) - 12-bit digital-to-analog converter card



(U) Figure 20 is a block diagram of the detection threshold. The digital integrated-clutter data words are presented in parallel form to circuitry that effectively multiplies them by 2, 4, or 8 by shifting them left one, two, or three binary places. These form the various components that must be added to determine the final products. Depending on the front-panel threshold selection, the multiplier select circuitry generates a four-bit binary multiplier representing decimal numbers from 1 to 11. This multiplier selects the components that enter into the product. The selected components are then added to form the weighted clutter product or threshold level. Figure 20 includes two examples in which an integrated clutter level representing the number 51 is multiplied by 5 (14 dB) and 11 (20.8 dB). In the first example the multiplier select circuitry generates the binary number 0101, which gates the $\times 1$ (or unshifted component) and the $\times 4$ components to the adders where they are combined to form the final product. In the second example the binary number 1011 gates the $\times 1$, $\times 2$, and $\times 8$ components to the adders to form the threshold level. In multiplication by factors from 1 to 11 only, the 2^3 and 2^2 bits generated by the multiplier select circuitry cannot both be at logical 1 at the same time. Thus by gating only one of the $\times 4$ or $\times 8$ components, depending on which of these bits is present, a binary adder is saved. The resulting threshold is digitally compared in a comparator circuit that generates an output voltage level whenever the integrated signal exceeds the threshold level.

DETECTION PROCESSOR

(U) The radar data stored on video tape during flight tests is processed by the digital signal processor. The resulting detections are properly formatted and directly stored in the memory of the general-purpose computer, as shown in Fig. 21. Using various experimentally derived ship-detection algorithms on known targets, a determination will be made

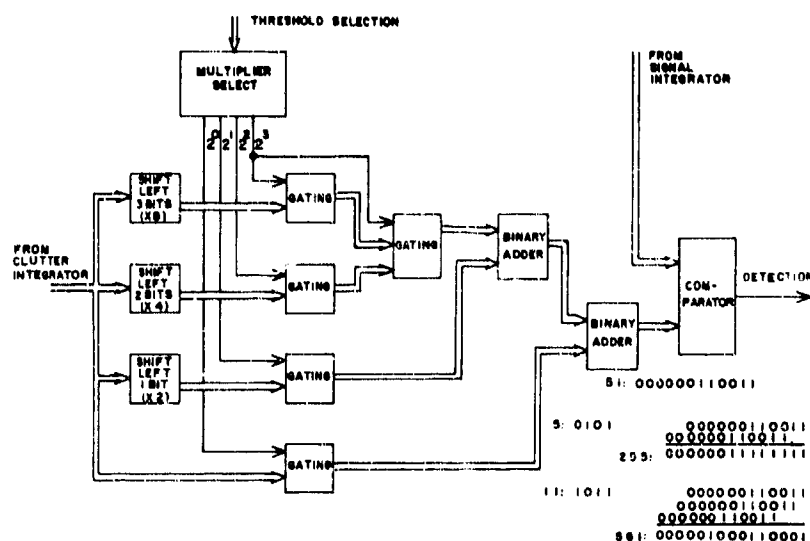


Fig. 20(U) - Detection threshold

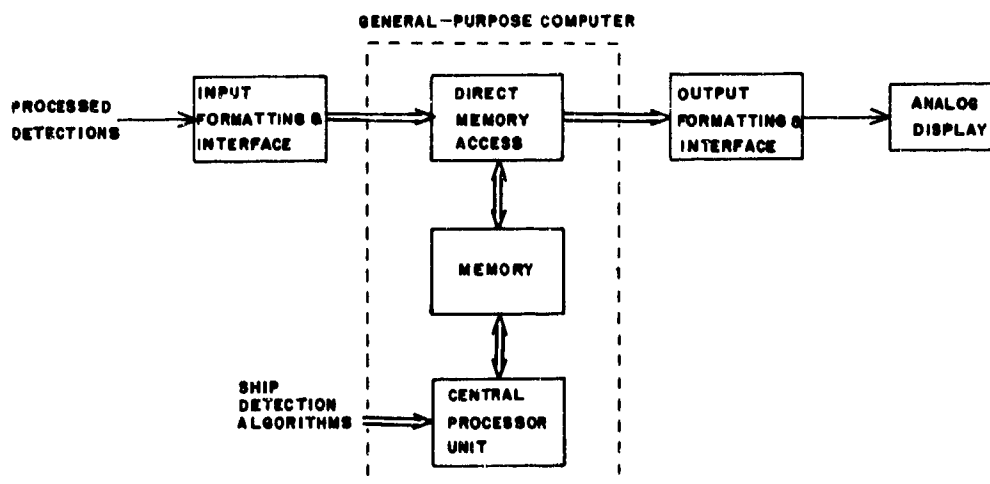


Fig. 21(U) - Detection processor

of the feasibility of reliably processing these detections into ship target determinations. Further details of this processing will be given in subsequent reports.

VIDEO RECORDING OF RADAR DATA

(U) To form a permanent record of the results gathered during flight testing of the radar system, the radar video from the receiver is recorded on video tape along with other required data. The video tape recording equipment consists of an Ampex AR500, single-video-channel, airborne, record-only unit, as shown in Fig. 22, and an Ampex AR900, ground-based, record-and-playback unit, as shown in Fig. 23. These recorders have a 6-MHz bandwidth and are capable of airborne recordings of up to 40 min duration.



Fig. 22(U) - Airborne wide-band video recorder

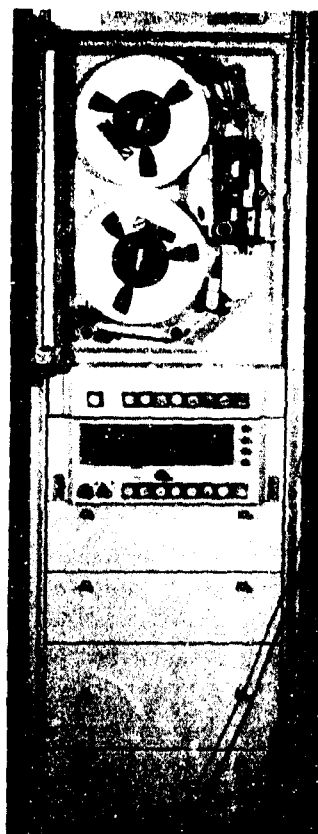


Fig. 23(U) - Ground-based wide-band video
record/playback unit

(S) The digital signal processor includes circuitry that formats the radar data for recording on tape. Besides radar video, the PRF pulse and the azimuth angle of the antenna are recorded on tape. The antenna is rotated to simulate the motion of a satellite with reference to a target on the surface of the earth. This formatting process is shown in Fig. 24. The synchro information from the antenna pedestal is digitized by a synchro-to-digital converter. The parallel digital format is basically a 14-bit binary-coded-decimal code representing $\pm 180.0^\circ$. This digital information is presented on a visual numeric display at the radar control console and is presented to circuitry in the processor for encoding. In the pulse-width encoder the parallel angular data is stored in a register, and each bit is shifted out in serial form as a $2\text{-}\mu\text{s}$ or $8\text{-}\mu\text{s}$ pulse, depending on whether it is a logical 0 or a logical 1 respectively. The start of this angle information is delayed well beyond the end of the gated video by a pulse derived by delaying the PRF pulse.

(U) This pulse-width-coded angle data is combined with the PRF pulse and the gated receiver video. An additional timing marker which precedes the PRF pulse by $10\text{ }\mu\text{s}$ is derived from the processor timing and is combined with the other data to aid in locating the PRF pulse on playback. This combined data is recorded on the airborne recorder. The format of the data recorded on tape is shown in Fig. 25.

(U) The tapes resulting from flight tests are brought back to the laboratory and played back on the ground-based unit. The block diagram of the playback and decoding circuitry is shown in Fig. 26. The output of the recorder is suitably amplified and presented to the PRF pulse detector and antenna-angle decoder. The PRF pulse detector has a circuit that looks for a $1\text{-}\mu\text{s}$ pulse, which should be the marker pulse. If it is found, the PRF pulse is gated out $10\text{ }\mu\text{s}$ later. Any signal or noise pulse detected after the marker pulse but before the PRF pulse inhibits the PRF pulse. The detected PRF pulse generates a delayed gate that enables the antenna-angle decoder beyond the gated video and before the coded angle data. Since the angle data is pulse-width modulated, it has a leading edge for each bit and is self-synchronous. Thus it is not necessary to know its exact location in time to decode it. The decoded angle data is presented to a visual readout and to a digital-to-synchro converter.

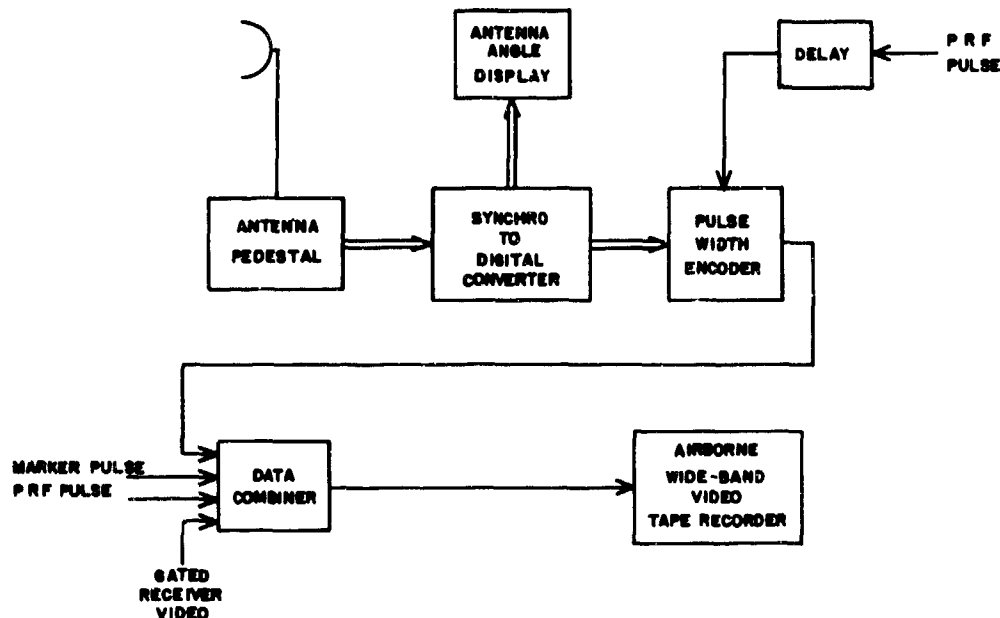


Fig. 24(U) - Data formatting and recording

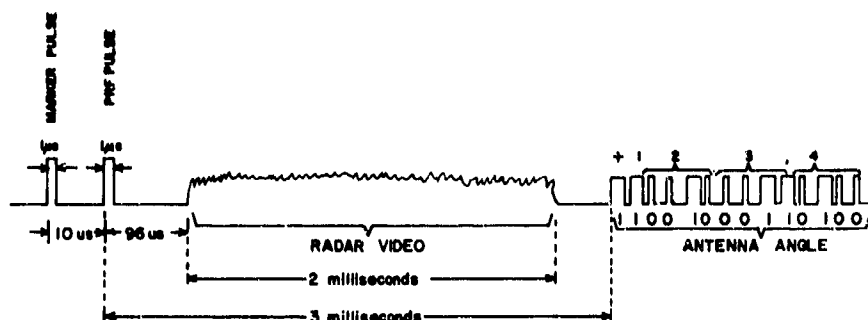


Fig. 25(U) - Format of data recorded on video tape

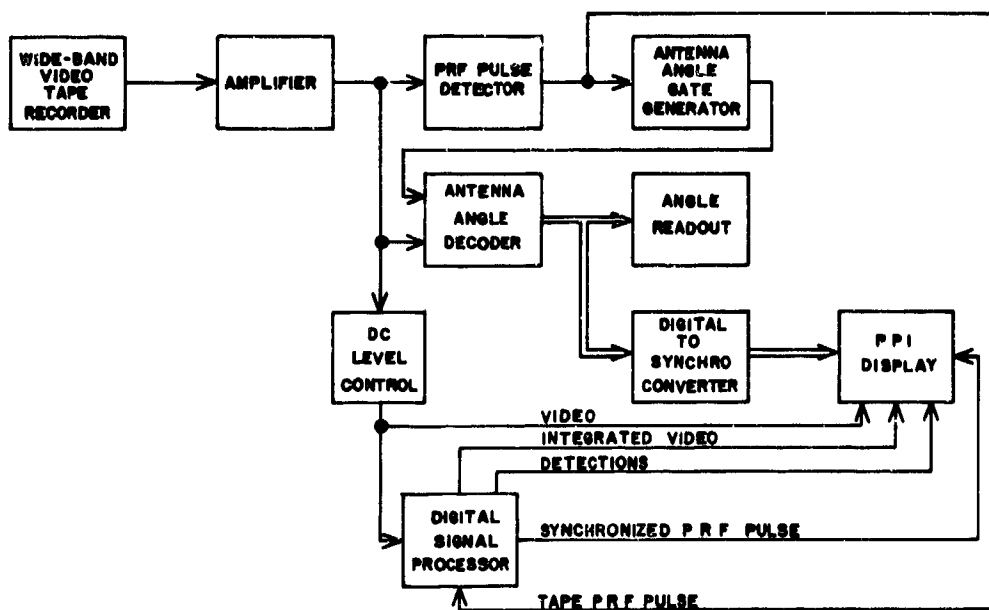


Fig. 26(U) - Video playback and digital decoding

(U) The PRF pulse decoded from the tape is used to synchronize the timing in the digital signal processor with the timing on the tape. This is done by a circuit that inhibits the processor PRF timing until the next tape PRF pulse whenever an asynchronous condition is detected.

(U) After any necessary dc-level setting, the composite data from the tape is presented to the digital signal processor. With synchronized timing the tape video data is processed during one of the selectable 10-mi swaths exactly as in a real-time operation. The video data from the tape, the processor-integrated video, or the processed detections can be presented on a plan-position-indicator (PPI) display for visual analysis. The PPI sweep comes from the digital-to-synchro converter and is derived from the antenna-angle data on the tape. The synchronized PRF pulse from the processor is used to trigger the PPI display.

PACKAGING

(U) The digital signal processor consists of two slide-out drawers, a control panel, and power supplies, all mounted in a 19-in rack, as shown in Fig. 27. Drawer 1, a top view of which is shown in Fig. 28, consists primarily of the signal integrator and high-speed A/D converter, and it contains 54 printed-circuit cards. Drawer 2, shown in Fig. 29, includes the system timing, low-speed A/D converter, clutter integrator, and tape encoding and decoding circuitry, and it consists of 38 printed-circuit cards. Figure 30 shows the intercard wiring in Drawer 1 and gives an indication of the complexity of the processor.

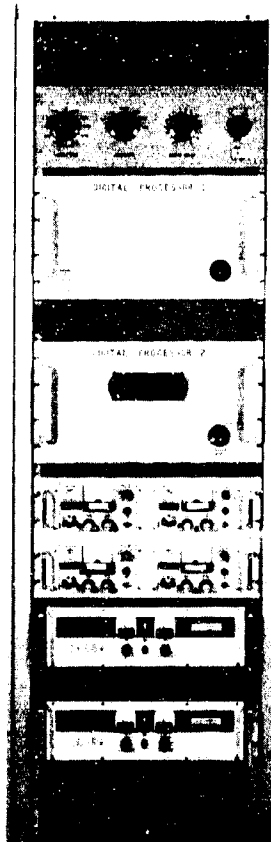


Fig. 27(U) - Digital signal processor rack

Fig. 28(U) - Digital-processor drawer 1

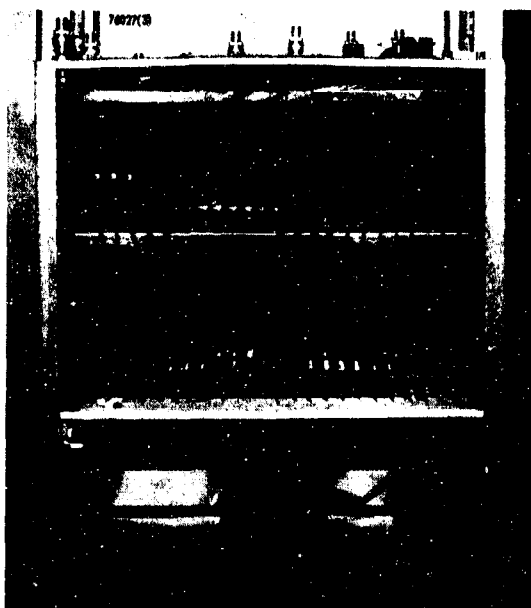
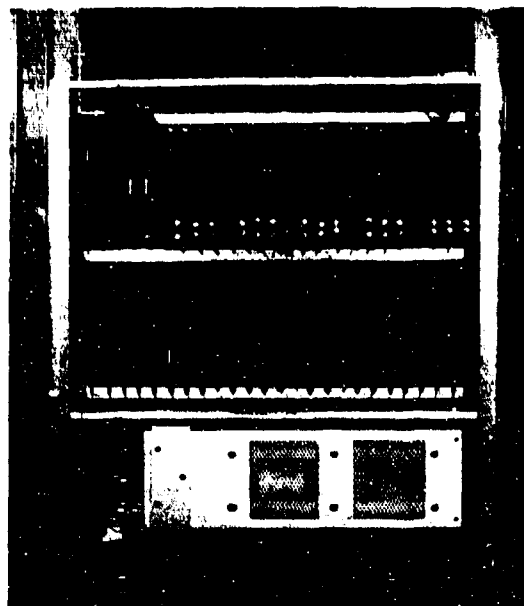


Fig. 29(U) - Digital-processor drawer 2

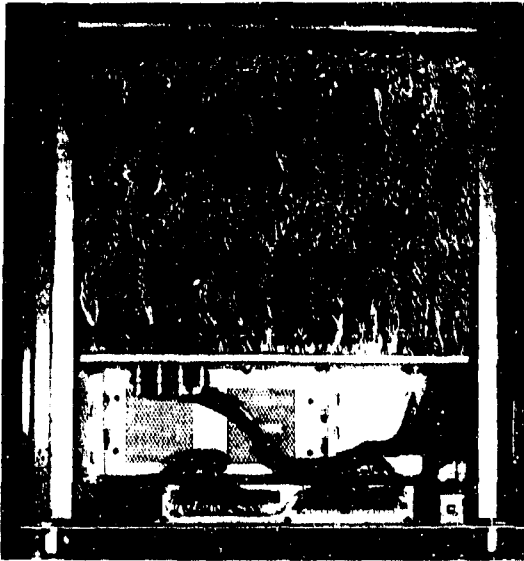


Fig. 30(U) - Intercard wiring drawer 1

SUMMARY

(S) The digital signal processor has recently undergone flight testing in NRL aircraft along with other components of the test-bed ocean-surveillance radar system. Preliminary test results have so far indicated that the processor operates according to expectations and demonstrates a high ability to enhance the signal-to-noise-plus-clutter ratio. This can be seen from Fig. 31 which shows the radar video on the top trace and the digitally integrated video inverted on the lower trace. An improvement of the signal-to-noise-plus-clutter ratio of approximately 20 db has been noted. The tape recording of the radar video during these flight tests has been very successful in providing a library of radar data that will be processed and analyzed in the laboratory. It should be noted that the radar video being processed in Fig. 31 was taken from a video tape recorded over the Atlantic.

(U) The testing of the system has also suggested changes that would lead to improved operation. One of these involves the modification of the A/D converter to give a nonuniform weighting to the various detected voltage increments, putting more increments at the lower analog voltage levels. This will improve the ability of the processor to detect targets in noise.

(U) Future efforts in the digital processing of radar signals include improvements and extension of the type of processor described here and research and development of processors for synthetic-aperture radars. These efforts will involve investigation of such areas as high-speed digital circuitry, such as the new Schottky-clamped TTL circuitry, faster and more densely packaged shift registers, faster binary arithmetic circuitry, and the application of an increasing number of LSI circuits to reduce equipment size and power requirements.

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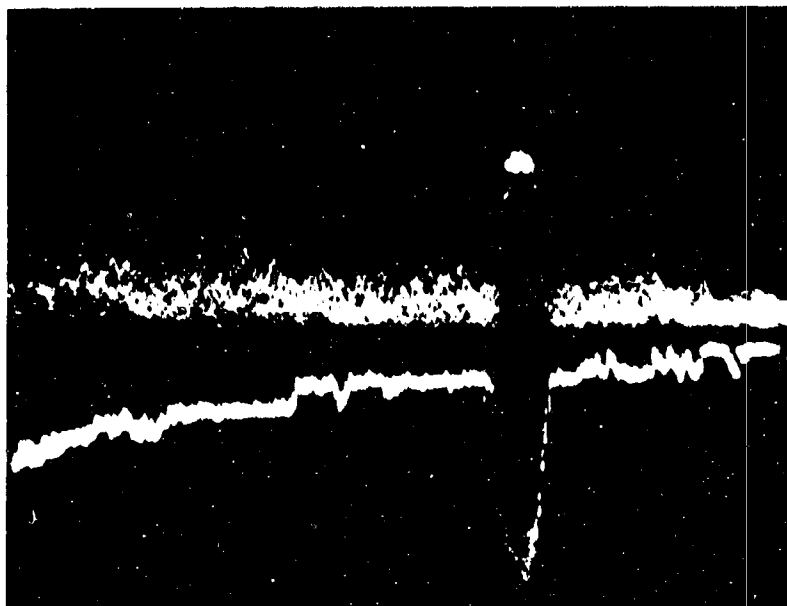


Fig. 31(U) - Upper trace - Raw radar video with ship target in the Atlantic Feb. 25, 1971. Lower trace - Inverted processed video (1000 ft/div)

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2. R.L. Eilbert, "Radar System Scaling for Performance Evaluation," NRL Report 7125 (Secret report, Unclassified title), Aug. 1970

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