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TRACK-WHILE-SCAN DATA PROCESSING INVESTIGATION

(UNCLASSIFIED TITLE)

Dr. Keith H. Norsworthy
THE BOEING COMPANY
Seattle, Washington

D180-14168-1

Technical Report AFAL-TR-71-131

November 1971

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H.

(10) [redacted] Keith Norsworthy
Aerospace Group
The Boeing Company
Seattle, Washington

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Foreword

(U) This final report was prepared by The Boeing Company, Seattle, Washington, in fulfillment of Air Force Contract [illegible], Track-While-Scan Data Processing Investigation.

(U) The program was monitored by the Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio, Captain William [illegible], Project Engineer. This report covers research conducted from May 1970 to April 1971. The work reported in this document represents the concerted efforts of the following Aerospace Group personnel under the direction of Mr. E. H. [illegible] Program Manager:

[illegible]

[illegible]

(U) This document is classified Confidential because it contains information relating to present or future [illegible] surveillance systems.

(U) This report has been reviewed and is approved for publication.

John E. [illegible] Jr

JOHN E. [illegible], JR., Lt.Col., USAF
Chief, Optronics Branch
Reconnaissance Division

UNCLASSIFIED ABSTRACT

(U) This final technical report describes the work accomplished on the Track-While-Scan Data Processing Investigation Contract. The objective of this program was to demonstrate the feasibility of using simple microelectronic shift register circuitry to inhibit detections that do not satisfy appropriate scan-to-scan correlation criteria. In the absence of such rejection circuitry, the TWS digital computer is required to sort and reject frequent noise detections and this substantially influences the size of computer required.

(U) The program entailed the fabrication of noise rejection circuitry and its evaluation in conjunction with the breadboard infrared Track-While-Scan subsystem developed under an earlier contract. The results of the evaluation tests have verified the performance characteristics of the noise rejection circuitry when tracking simulated and moving targets, and have demonstrated that implementation of the noise rejection circuitry can be accomplished with low-cost low-weight microelectronic modules.

(U) The performance gain resulting from the inclusion of the noise rejection circuitry in a typical infrared track-while-scan sensor is shown to correspond to either (1) a 68% easing of the computer load or (2) a 15% improvement in detection sensitivity.

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ILLUSTRATIONS

TABLES

1.0 INTRODUCTION

(U) This Final Report summarizes the work accomplished on the Track-While-Scan Data Processing Contract F33-615-70-C-1635. Approximately 4.3 man months of effort were expended on the contract. All contract objectives were met and measurement data was obtained in sufficient depth to predict operational hardware performance.

(U) The Track-While-Scan Data Processing Investigation has involved the development and evaluation of a concept to reduce the computer load in an infrared system. The reduction in computer load is achieved by using simple microelectronic circuitry to inhibit detector signals that do not satisfy appropriate scan-to-scan correlation criteria. In the absence of such microelectronic circuitry, the TWS digital computer is required to sort and reject frequent noise detections and this substantially influences the size of computer required.

(U) The program entailed the fabrication of noise rejection circuitry and its evaluation in conjunction with the breadboard infrared Track-While-Scan subsystem developed under an earlier contract.

(C) The results of the contract show that the inclusion of noise rejection circuit gives an effect which is equivalent to increasing the aperture diameter by approximately 15%.

2.0 DESCRIPTION OF CONCEPT

In IR Track-While-Scan systems, much of the data processing load is placed on a digital computer which processes the sequential target detections and assembles them into individual smoothed target tracks. The computer operations typically involve data stabilization, scan-to-scan correlation (to reject random noise detections), and track smoothing.

One way to reduce the computer load is to use external circuits to perform noise editing by scan-to-scan correlation. This is the approach evaluated by this contract. Until recently this has not been feasible due to the quantity of circuits required and their high cost. However, recent advances in the microelectronics field have led to the development of low-cost shift registers suitable for directly implementing the required scan-to-scan correlation operation.

In the past six years the cost per bit of microelectronic shift registers has dropped from approximately ten dollars per bit to one cent per bit, and the packing density has improved by approximately three orders of magnitude. A brief discussion of the cost trend for microelectronic shift registers covering the years 1962-1972 is given in Appendix I.

The proposed noise rejection concept utilizes a shift register memory to open a gate in each detector channel at approximately the same azimuth location that a threshold exceedance occurred on the previous scan. In this manner only the data from targets that repeat within preset limits are passed on to the computer.

A block diagram of representative scan-to-scan noise rejection circuitry is shown in Figure 2-1. Activation of the threshold causes a binary "1" to be sent to shift register #1 where it is sequentially clocked through the shift register and appears at its output exactly one scan period later. The output of the shift register #1 is used to open Gate G. If a new threshold exceedance occurs during the time the gate is open, it passes through the gate and is used to initiate the reading of observation data (detector number, azimuth, attitude reference data, and time) from the

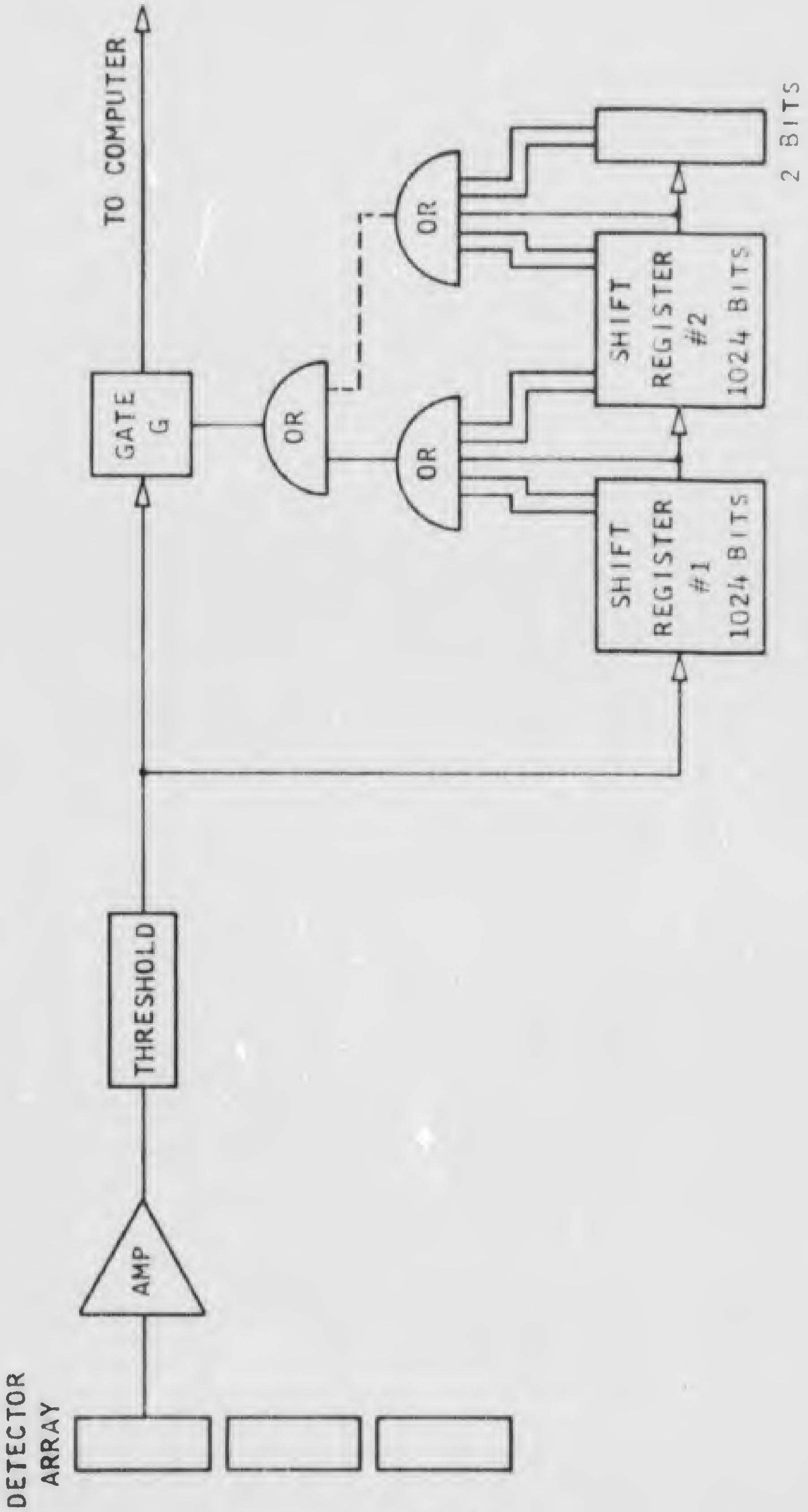


Figure 2-1: BASIC SCAN-TO-SCAN NOISE REJECTION CONCEPT

infrared scanner into the track computer. By using an "OR' circuit to combine the outputs from the last few flip-flops of shift register #1 and the first few flip-flops of shift register #2, the gate time period is extended to correspond to a sufficient azimuth increment to allow for changes in azimuth angle that may occur due to the angular velocity of the target and possible changes in the attitude of the sensor. Control signals from the end of shift register #2 can be used to maintain track through the occurrence of single missed observations.

In the circuitry described above, only a single elevation channel is considered. In practice two complicating factors arise which can cause a target to be observed on different detector channels successively. These factors are; 1) angular instability of the viewing sensor, and 2) target motion in the elevation direction. To ensure satisfactory operation of the noise rejection circuitry under these conditions the gating logic is modified to allow a threshold exceedance to pass to the computer if an exceedance occurred on the previous scan with an acceptable azimuth angle and also within an acceptable elevation field of view. Implementation of this concept is accomplished as shown in Figure 2-2, where the number of separate shift register processing channels equals the number of detectors.

To reduce circuit complexity,one might prefer an arrangement that shares each shift register channel between several output gates,as shown in Figure 2-3. Such an arrangement gives slightly inferior performance to that of Figure 2-2 (see the performance analysis of Section 2.1) but requires substantially less shift register circuitry.

2.1 Performance Analysis

For the scan-to-scan editing process shown in Figure 2-3, the average rate of threshold noise exceedances passed to the computer is related to:

1) the noise exceedance rate at the outputs of the individual thresholds
2) the number of detector channels (D)

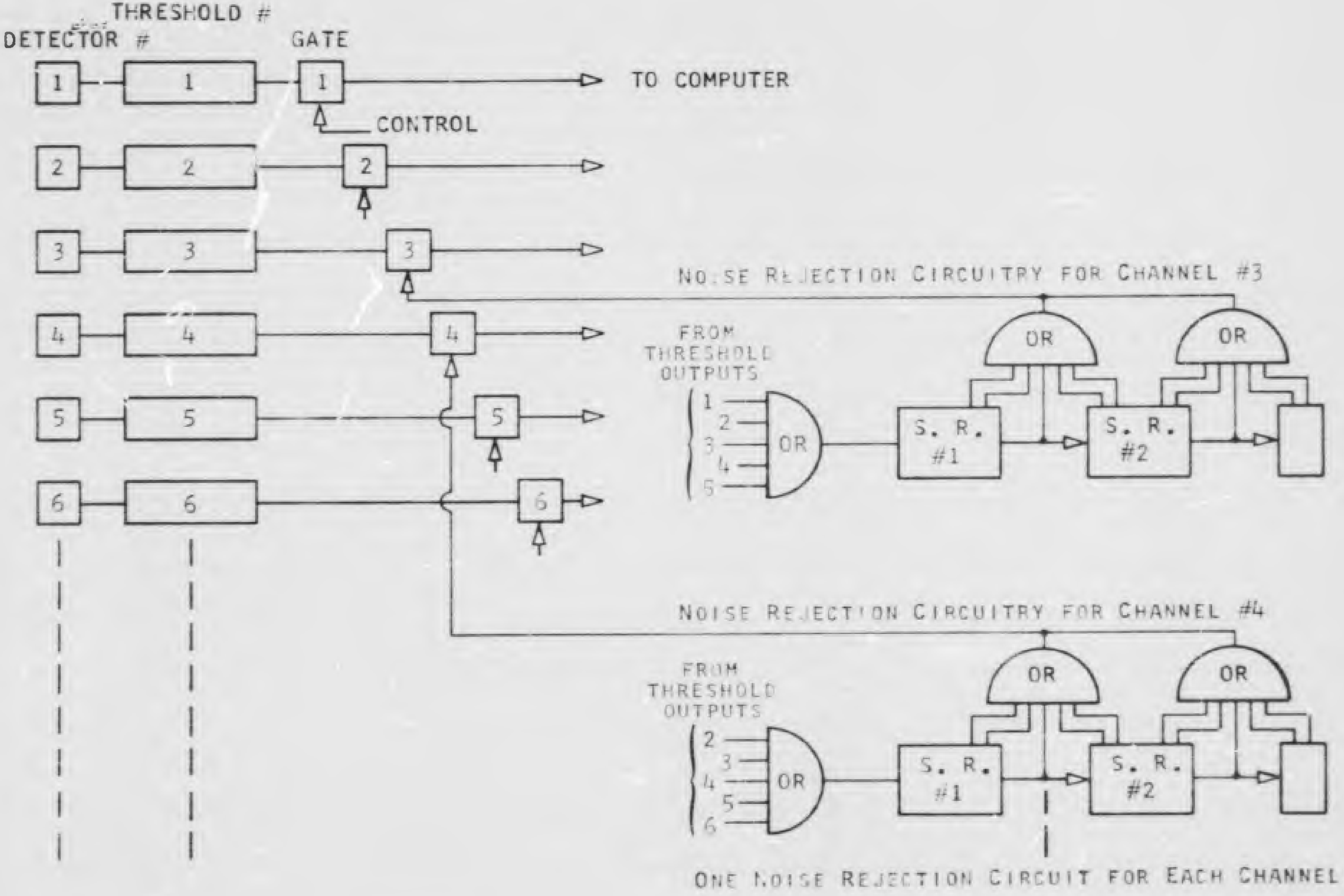


Figure 2-2: MULTICHANNEL NOISE REJECTION CIRCUITRY – INDIVIDUAL GATE CONTROLS

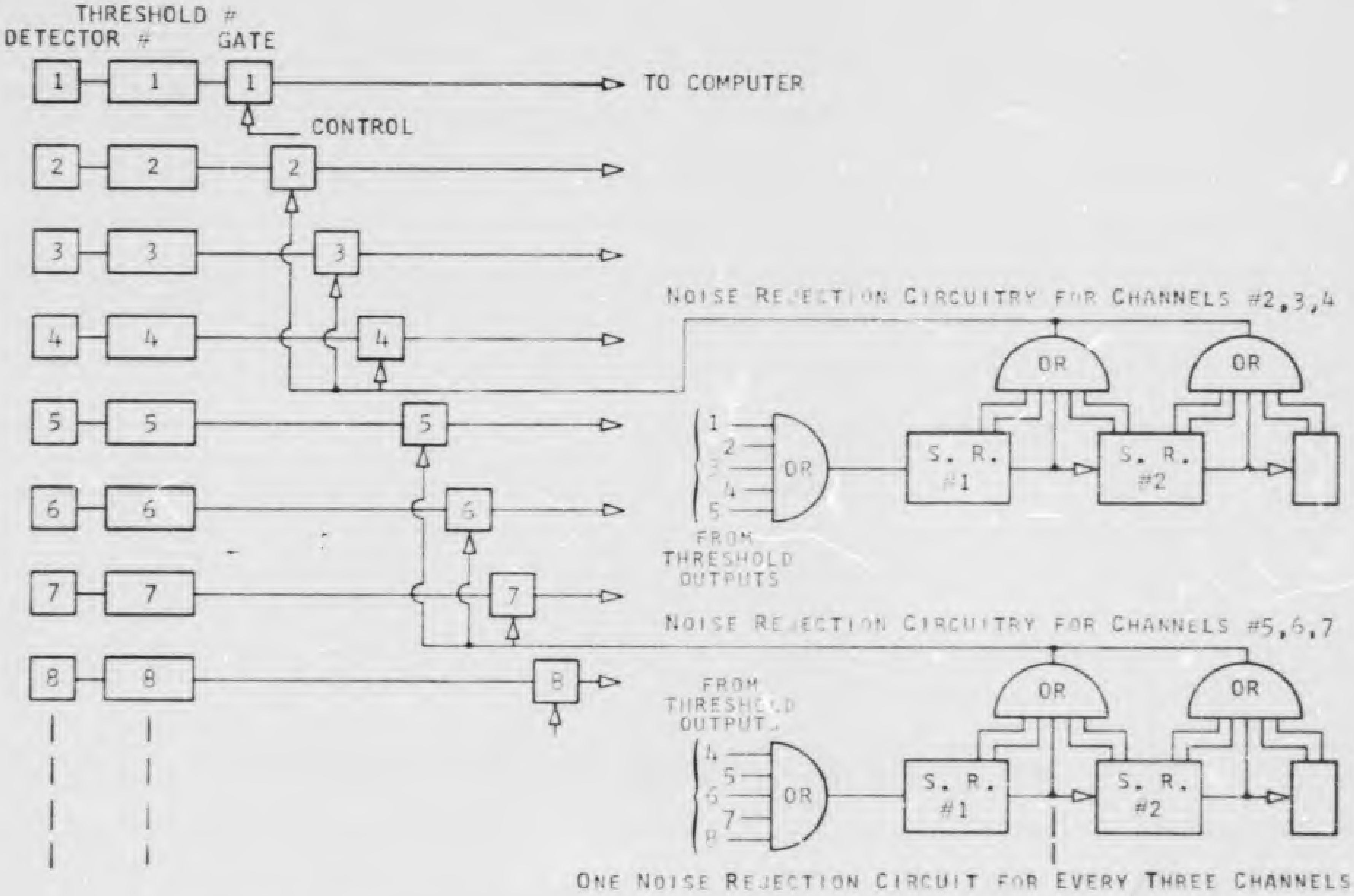


Figure 2-3 MULTICHANNEL NOISE REJECTION CIRCUITRY – PARALLEL GATE CONTROL

3) the number of detector channels paralleled to each shift register processor channel (K)

and 4) the azimuth gate intervals (θ_1 and θ_2)

If the threshold noise exceedance rate in each detector channel is given by N_i, the probability that any specific noise exceedance will pass through its gate is given approximately by P_o

$$P_o = N_i \frac{(\theta_1 + \theta_2)}{\omega} K, \qquad \text{if } \frac{(\theta_1 + \theta_2)}{\omega} K < 0.1 \qquad (2\text{-}1)$$

Thus, the total noise exceedance rate passed to the computer (N_o) is given approximately by

$$N_o = P_o N_i D = N_i^2 \frac{(\theta_1 + \theta_2)}{\omega} K D \qquad (2\text{-}2)$$

This is to be compared with the value ($N_i D$) that would be passed to the computer in the absence of the noise rejection circuitry.

For the configuration considered (Figure 2-3)

$$K = Z + E$$

where Z is number of output gates controlled by each shift register processing channel (a high number for low circuit complexity) and E corresponds to the scan-to-scan elevation uncertainty of a target.

In a typical system the following values may exist:

N_i = 0.5 per second
$\theta_1 = \theta_2$ = 0.017 radian (1 degree)
K = 5
D = 250
ω = 2π radians/second

Substitution in Equation 2-2 gives N_o equal 1.7 per second (compared to 125 per second without noise rejection) so it is seen that, for this example, the noise exceedance rate to the computer is reduced by nearly two orders of magnitude.

Figure 2-4 shows a curve of overall "noise rejection ratio" versus (N_i), for several values of K, and the above typical values of θ_1, θ_2 and K. The term "noise rejection ratio", here refers to the ratio of noise exceedances to the tracking computer with and without use of the noise rejection circuitry.

$$\text{Noise rejection ratio} = \frac{N_i D}{N^2 \dfrac{(\theta_1 + \theta_2)}{\omega} K D} = \frac{\omega}{N_i \, (\theta_1 + \theta_2) \, K}$$

When $\theta_1 = \theta_2 = 1$ degree (.017) radians) and $\omega = 2\pi$ radians/second

$$\text{Noise rejection ratio} = \frac{180}{N_i \cdot K}$$

It must be emphasized that repeating observations, for example those arising from stars or stationary background features, will not be rejected unless appropriate moving target logic is applied.

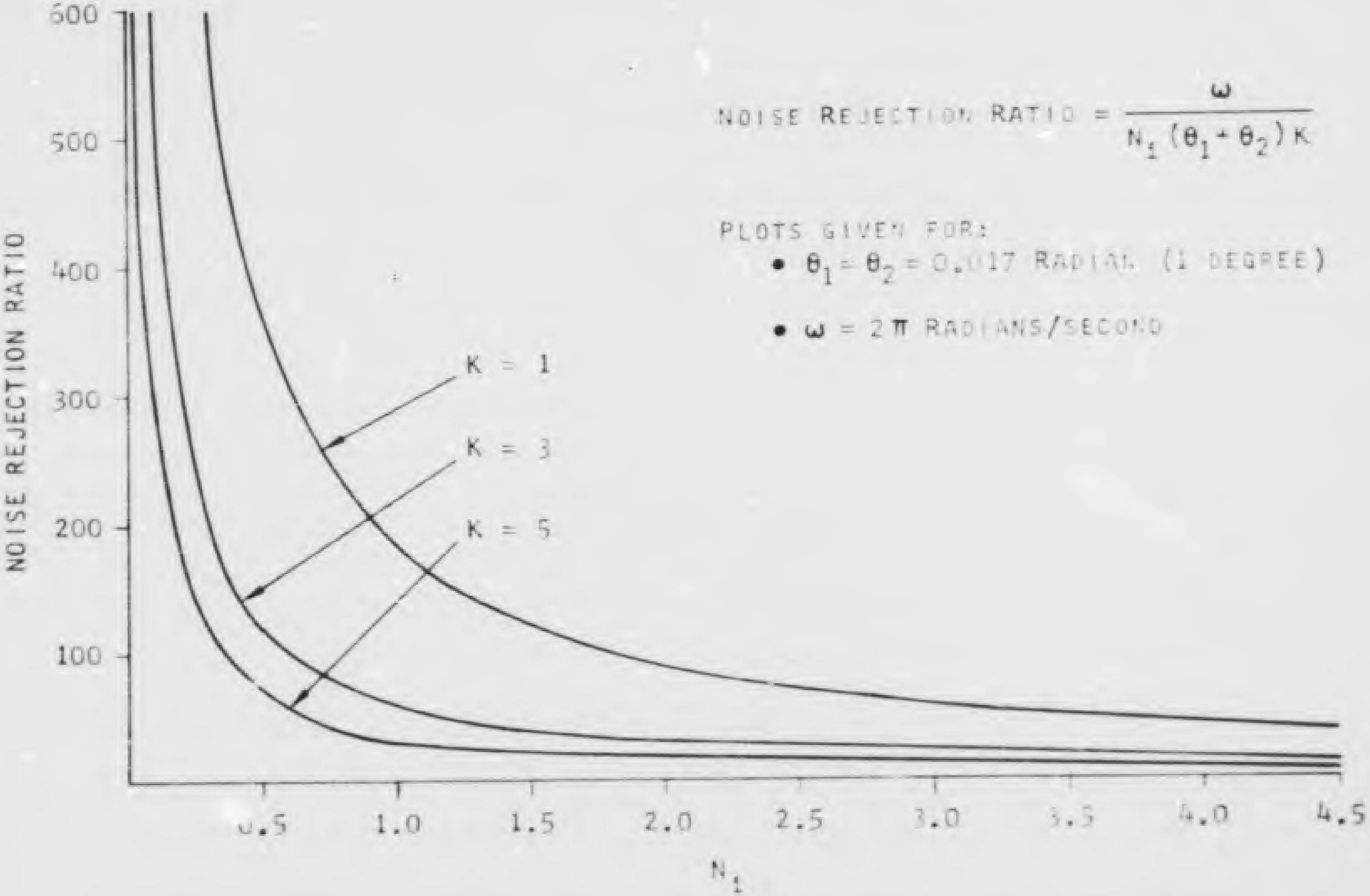


Figure 2-4 NOISE REJECTION RATIO VERSUS INPUT NOISE RATE PER DETECTOR CHANNEL (N_I)

3.0 LABORATORY EVALUATION TESTS

3.1 Description of Test Configuration

The described noise rejection concept was evaluated in the infrared track-while-scan (TWS) subsystem developed earlier under Contract AF33(616)-8496. The major components of the TWS subsystem are shown in Figure 3-1. From left to right in the photograph are the scan unit, the control console, the data processing unit and the magnetic tape unit on which sensor information is stored prior to off-line processing by a laboratory digital computer.

For laboratory tests, the TWS scan unit is rotated at a constant speed of 1 rps and target energy which enters the scan unit through the primary optics is focussed onto an array of optically immersed PbS detectors. Targets at different elevation angles excite different detectors. Each detector output is amplified and frequency filtered before being compared to a preset threshold level. Occurrence of a threshold exceedance results in the transferring of target parameters to the magnetic tape ready for input to the digital computer where target tracks are computed. The data transferred to the computer includes the azimuth angle of the observation, related sensor attitude information, time reference data, and the position in the array of the excited detector.

The detectors used in the scan-to-scan noise rejection tests were fabricated for an earlier contract "Pulse Compression Techniques for Infrared Surveillance," Contract Number F33(615)-67-C-1803. Five such detectors were used, each providing 1.0 mr elevation coverage.

A block diagram of the scan-to-scan noise rejection circuitry used in the laboratory evaluation tests is shown in Figure 3-2 and a photograph of the package is shown in Figure 3-3. By controlling the switches S_1 through S_5 different values of the parameter K (referred to in Section 2.1) are selected in the range $1 \leq K \leq 5$. The threshold exceedance signals from the switches are combined in appropriate "OR" logic and used as input to shift register #1 which is controlled by clock pulses from the azimuth shaft encoder to provide a delay that corresponds to exactly one revolution in azimuth (1024 bits per revolution gives approximately 1/3 degree definition). The scan-to-scan correlation criterion is imposed on the shift

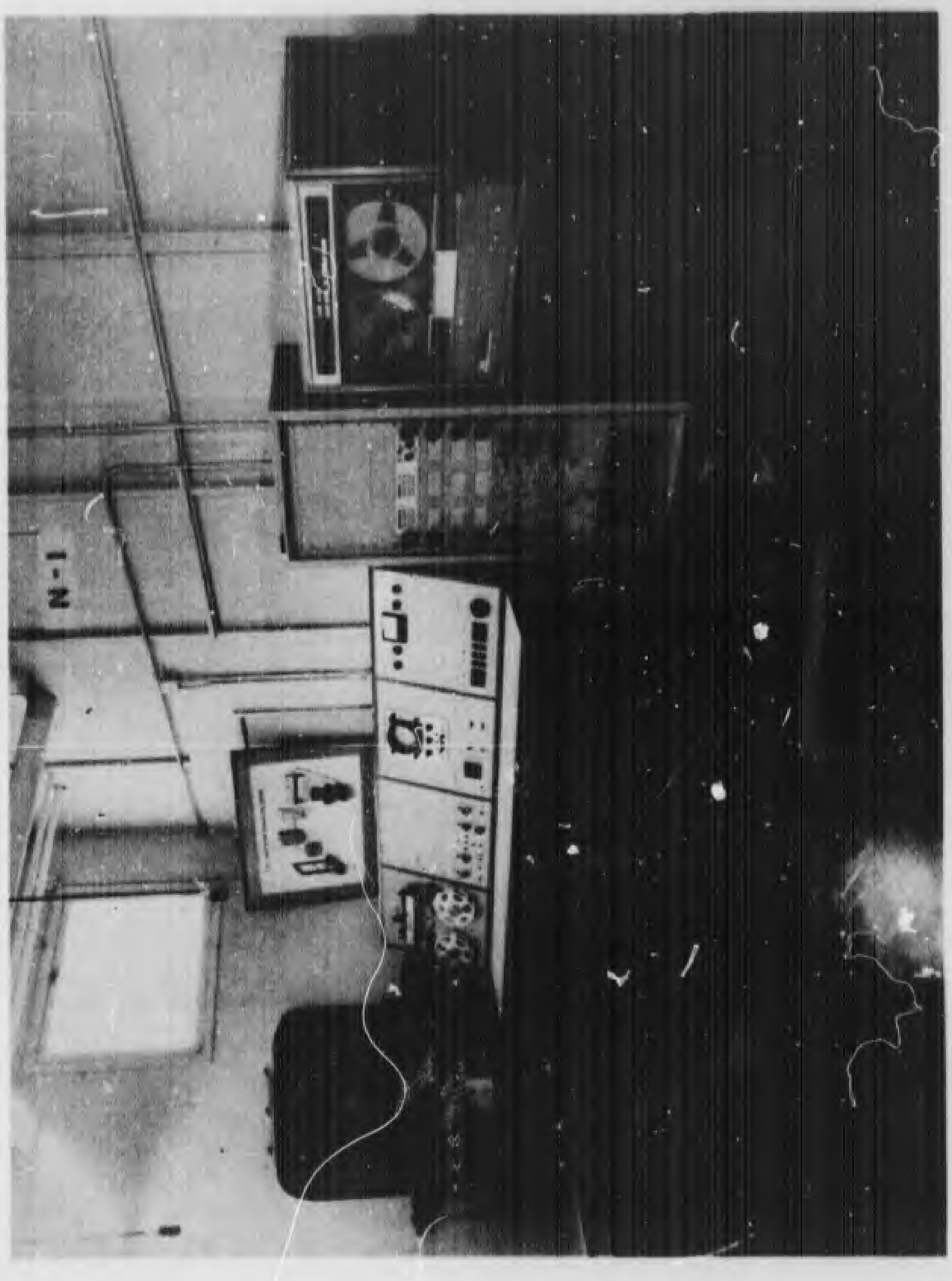


Figure 3-1: TRACK-WHILE-SCAN SUBSYSTEM

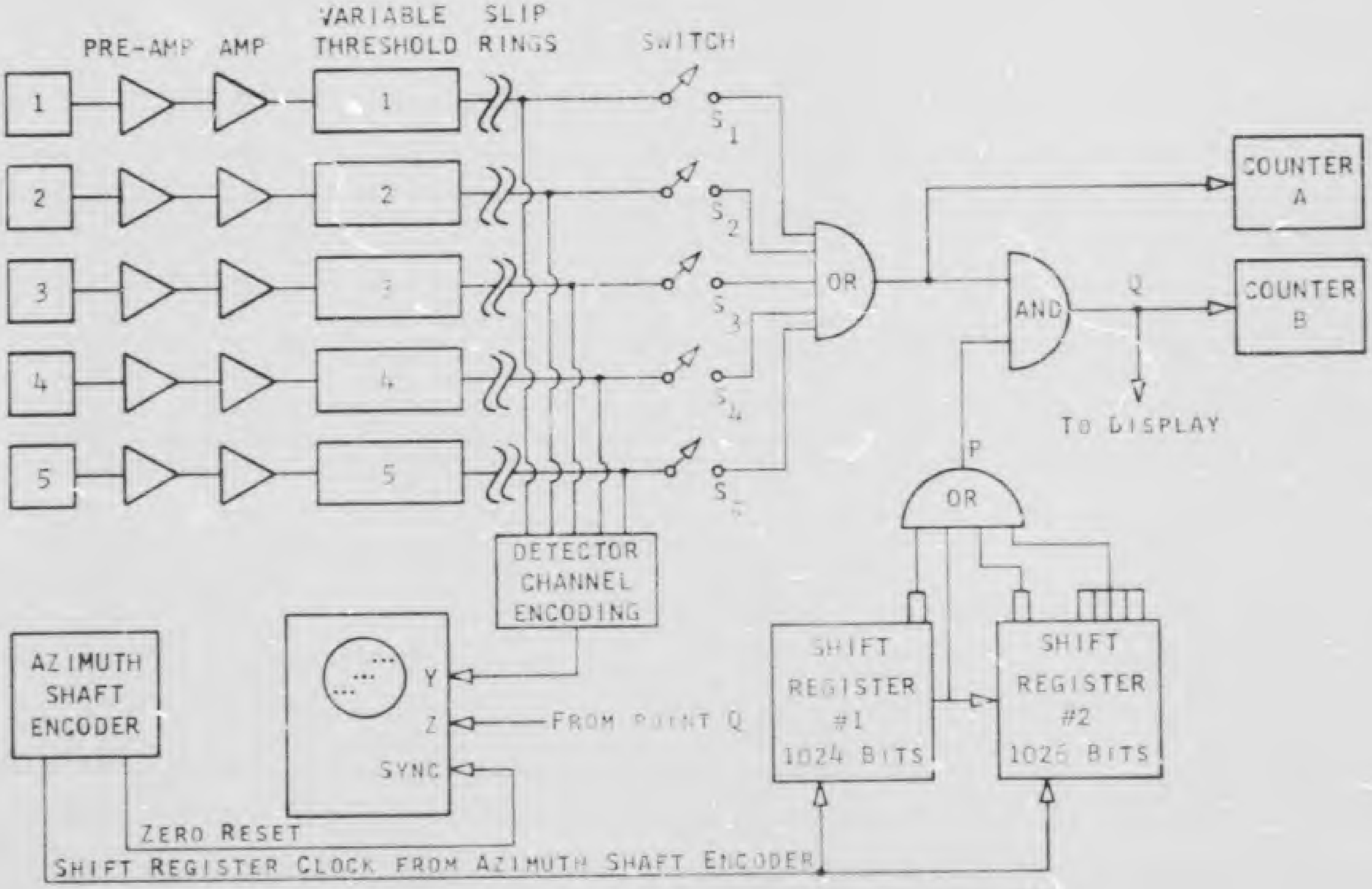


Figure 3-2. SCAN-TO-SCAN NOISE REJECTION CIRCUITRY
(Laboratory Test Configuration)

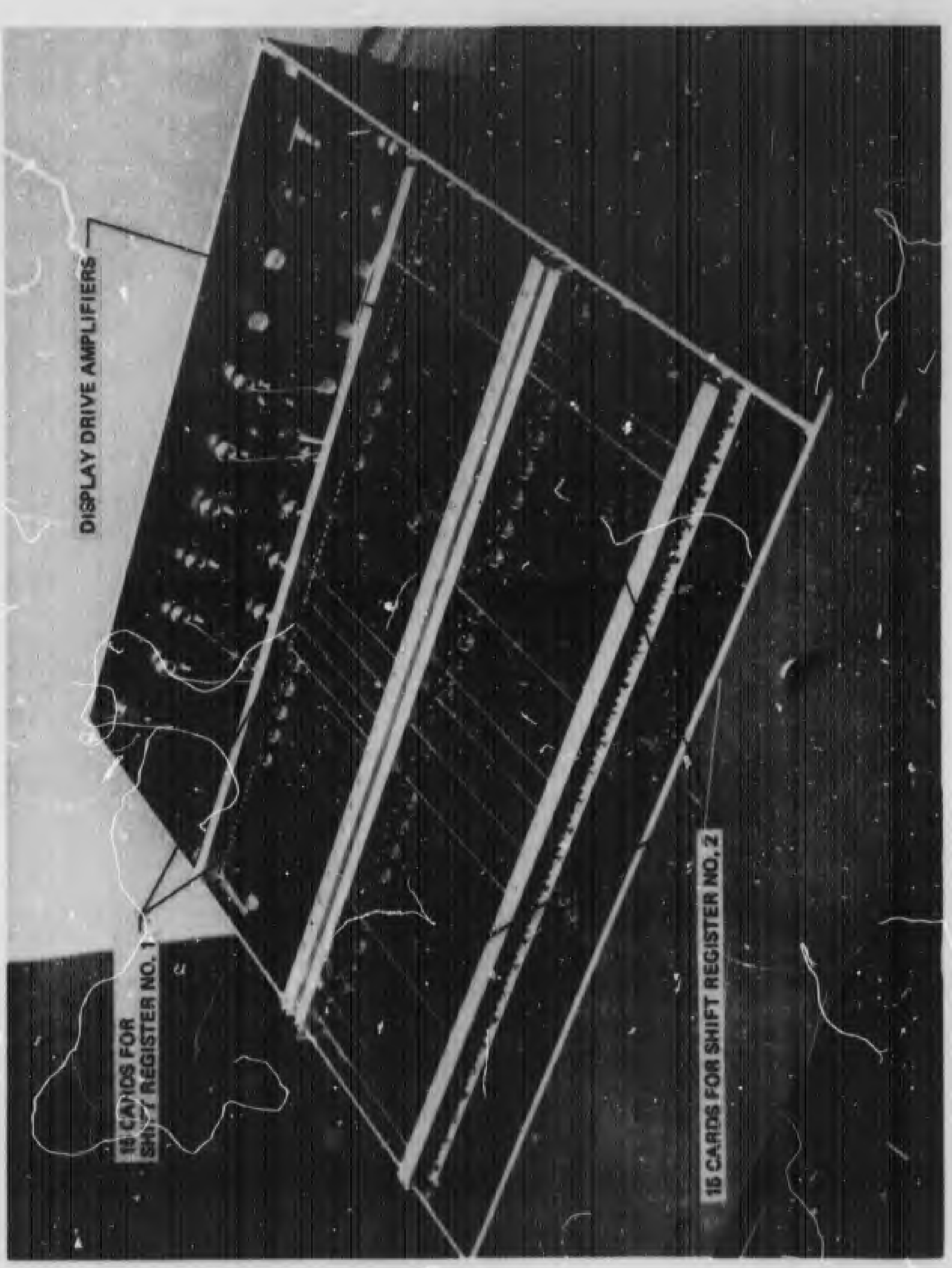


Figure 3-3: SCAN-TO-SCAN NOISE REJECTION CIRCUIT

(U)register signals by means of the logic circuits lettered P and Q. Signals that satisfy the scan-to-scan correlation criterion are transmitted through the AND gate Q and are treated as apparent target sightings, and in an operational system their associated parameters would be passed on to the computer.

(U)For test purposes counter A accumulates the total number of threshold exceedances supplied to the input to the noise rejection circuitry and counter "B" accumulates the number of threshold exceedances that pass the scan-to-scan noise editing process.

3.2 Performance Evaluation Tests

(U)The performance of the noise rejection circuitry was evaluated through a series of laboratory tests. The tests were designed to substantiate the noise rejection theory of Section 2.1 and evaluate performance when tracking stationary and moving targets. Tracks with deliberately missed points were generated to check that the expected reacquisition performance was obtained.

3.2.1 Verification of Noise Rejection Theory

(U) Tests for verifying the noise rejection theory were conducted utilizing the circuit configuration shown in Figure 3-2. Measurements were made for two individual detector channels and the results are shown in Figures 3-4 and 3-5. In each case, the input noise exceedance rate was varied by adjusting the threshold circuit associated with the channel under test, and a 500 second average of the input and output noise rates were recorded by counter A and B, respectively, and used to compute the noise rejection ratio. Agreement between theory and practice is seen to be good.

3.2.2 Stationary Target Tests

(C) The stationary target tests demonstrate the performance of the noise rejection circuitry when detecting stars or fixed background features. For these tests a simulated target source was placed 100' from the scan unit and scanned for nine consecutive scans. The output of the noise rejection circuitry for each scan is shown as a separate trace on the oscilloscope

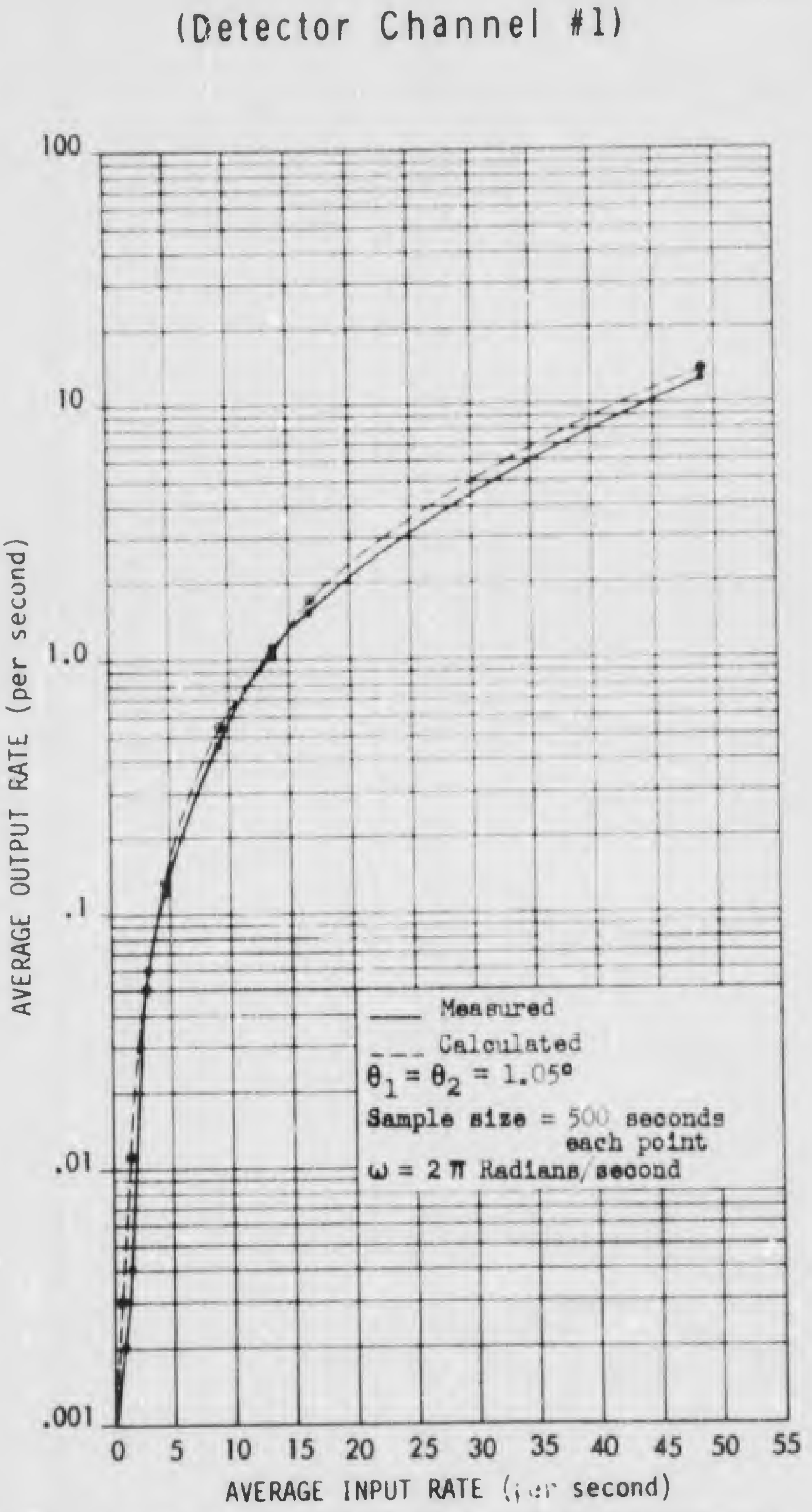


Figure 3-4: NOISE REJECTION MEASUREMENTS (U)

(Detector Channel #3)

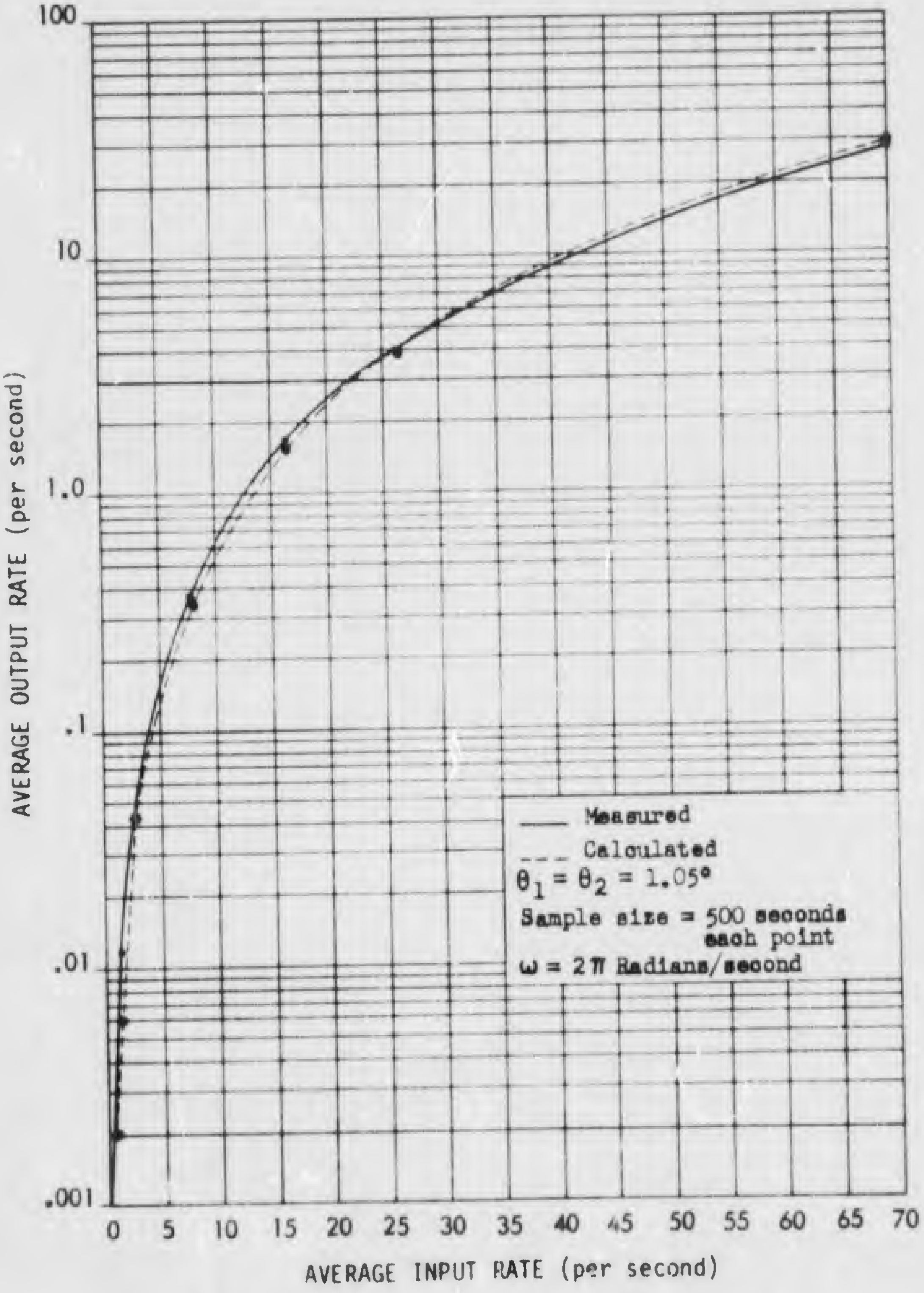


Figure 3-5 NOISE REJECTION MEASUREMENTS (U)

(C) photograph in Figure 3-6. The vertical position of the trace was automatically advanced prior to each scan so the photograph shows a time sequence of the eight scans. Target detections are indicated by the square wave signal on each trace. Figure 3-6B shows the test results for a case where a target detection was deliberately missed on Scan 5 (accomplished by turning off the simulated target source for one scan). The photograph shows that, as expected, the target was reacquired on the scan immediately following the miss.

3.2.3 Moving Target Tests

3.2.3.1 Horizontal Tracks

(C) The moving target tests utilized a Target Simulation Unit, developed under Contract AF33(615)8496, to generate target tracks. Angular velocities were selected in the range 0.5 to 5.0 milliradians per second. Figures 3-7A, 3-7B and 3-7C show the results obtained from three tests involving a track with horizontal angular velocity equal to 4 milliradians per second. The photographs in Figure 3-7 were obtained by using the noise rejection circuitry output to intensity modulate an oscilloscope. The "X" position of the points correspond to the azimuth angle at which the target was detected. Figure 3-7A shows the track correctly detected on nine consecutive scans, Figures 3-7B and 3-7C show results with one, and two, deliberately missed observations. As expected, in the case of two missed observations (Figure 3-7C) the noise rejection circuitry caused one extra miss to occur.

3.2.3.2 Sloping Tracks

(C) The ability to track through several detectors was verified by simulating a target trajectory that had a vertical component of velocity in addition to a horizontal component. The results of two such tests are shown in Figure 3-8. Figure 3-8A shows a continuous sequence of observations while Figure 3-8B shows a deliberate miss of the second observation on detector #5. The detections on channel #1 resulted from a high noise condition on that channel giving rise to some noise leakage.

Figure 6A: CONTINUOUS TRACK

Figure 6B: TRACK WITH MISSED OBSERVATION

Figure 3-6: NOISE REJECTION CIRCUITRY – STATIONARY TARGET TEST RESULTS (U)

Figure 7A: CONTINUOUS TRACK

Figure 7B: TRACK WITH ONE MISSED OBSERVATION

Figure 7C: TRACK WITH TWO MISSED OBSERVATIONS

Figure 3-7: NOISE REJECTION CIRCUITRY
SINGLE CHANNEL MOVING TARGET TEST RESULTS (U)

Figure 8A: CONTINUOUS TRACK

HORIZONTAL VELOCITY = 2 MILLIRADIANS/SEC
VERTICAL VELOCITY = .5 MILLIRADIANS/SEC

Figure 8B: TRACK WITH ONE MISSED OBSERVATION

HORIZONTAL VELOCITY = 4 MILLIRADIANS/SEC
VERTICAL VELOCITY = 1 MILLIRADIAN/SEC

Figure 3-8: NOISE REJECTION CIRCUITRY
MULTIPLE CHANNEL MOVING TARGET TEST RESULTS (U)

(C) In Figure 3-8 it is apparent that detections were received on detector #3 immediately after they were lost on detector #1, this situation arose because the blur circle of the test facility has degraded to approximately 0.9 mr diameter compared to the detector heights of 1.0 mr.

4.0 COMPUTER LOAD REDUCTION AND ALTERNATIVE SYSTEM TRADES

The function of the Noise Rejection Circuitry is to edit the information from an IR sensor prior to processing by the digital track computer. All threshold exceedances that fail to pass a scan-to-scan editing ceriterion are rejected thereby reducing the load on the digital computer.

As an alternative to reducing the computer load, one may elect to work with a reduced threshold-to-noise ratio (increased noise into noise rejection circuitry) and gain either; a) an improve target detection probability, or b) a reduction in aperture size for the same target detection probability.

These alternatives are briefly discussed below.

4.1 Reduced Computer Load

Consider first the consequences of leaving both the target detection probability and aperture size unaltered.

The amount of computer load reduction achieved through the use of the Noise Rejection Circuitry is of course dependant on the specific computation functions implemented by the tracking computer. These functions vary in detail from one system to the next but they typically include functions such as:

- data formating
- data stabilization
- scan-to-scan correlation, and
- track smoothing

The computer load depends on the rate of observation that it must process and on the character of the observations (i.e. do they arise from a true target track , random noise effects, or background clutter).

In considering the computer load reduction it is important to distinguish between the "average" computer load that must be handled on a continuous basis to ensure satisfactory surveillance, and the "peak" computer load which occurs when the surveillance system detects a threat and is called on to simultaneously track a maximum number of targets. In order to give quantitative examples of computer load reductions that can be achieved through the use of the noise rejection circuitry, an IR TWS system with the following characteristics is considered:

Number of detectors (D) - 250

Scan rate (ω) - 2π radians per second

Random noise pulses per scan - 125 (0.5 per detector channel)

Number of detectors per noise rejection shift register (K) - 5

Azimuth Gate Size θ_1 ($=\theta_2$) - .017 radians (1 degree)

and the computation functions of the tracking computer are assumed to be as follows:

Data Input Transfer - Transfer the data associated with each detection (Detector #, azimuth, time, attitude reference information, etc) into the computer. This process typically requires 12 computer instructions per detection.

Data Format - arrange input data into correct word lengths and store in memory. This process typically requires 12 computer instructions per detection.

Detector Array Alignment Corrections - Compensate for minor misalignment of the detectors. This typically requires 24 computer instructions per detection.

Data Stabilization - Perform coordinate transformations from sensor coordinates to inertial coordinates. This requires approximately 1600 computer instructions per detection.

Scan-to-Scan Correlation - Correlate incoming sensor data with stored observations from the previous scan to identify the new observations as; continued target tracks, repeat background observations, or possible track initation points. Data from the

(U) previous scan that does not fit either of the first two catagories is dropped from consideration.

(U) Typically the number of computer instructions for each noise detection is $100 + 200 \left[\frac{\text{total exceedances/scan}}{50}\right]$ and for each star or target detection $100 + 200\left[1 + \frac{\text{total exceedances/scan}}{50}\right]$

(U) The 100 refers to the number of instructions required to establish angular limits around each new detection within which detections from the previous scan will be checked and the 200 refers to the instructions required to compare new detections with data from the previous scan.

(U) <u>Track Smoothing</u> - Smooth through the positional data associated with established tracks. This routine requires approximately 40,000 computer instructions per track.

(U) <u>Output Formatting</u> - Format track information for display and further processing. The routine typically requires 500 instructions per track observation and 1000 for each completed track.

(U) The impact of using the described noise rejection logic is demonstrated by considering two typical operational senerios for the above sensor.

Scenerio	Targets in field-of-View	Stars in Field-of-View	Total Noise Exceedance Rate Per Sec Per Scan (ahead of noise rejection ckt)
1. Average Surveillance Condition	0	20	125
2. Maximum Target Threat	25	20	125

(C) Consider first the average (surveillance) condition. The computer load with and without the noise rejection circuitry is shown in Table I. It is seen that the inclusion of the noise rejection circuitry reduces the average computer load by a factor of 87%.

Table I AVERAGE SURVEILLANCE COMPUTER LOAD REDUCTION (U)

(C)

	Related Number of Computer Instructions	Number of Times Repeated Per Scan		Total Instructions Per Scan	
		Without Noise Rejection Ckt	With Noise Rejection Ckt	Without Noise Rejection Ckt	With Noise Rejection Ckt
Data Input Transfer	12 per Noise Detection	125	1.7	1,500	20
	12 per Star Detection	20	10	240	240
	12 per Target Detection	0	0	0	0
Data Format	12 per Noise Detection	125	1.7	1,500	20
	12 per Star Detection	20	20	240	240
	12 per Target Detection	0	0	0	0
Detector Array Alignment Corrections	24 per Noise Detection	125	1.7	3,000	40
	24 per Star Detection	20	20	480	480
	24 per Target Detection	0	0	0	0
Data Stabilization	1600 per Noise Detection	125	1.7	200,000	2,720
	1600 per Star Detection	20	20	32,000	32,000
	1600 per Target Detection	0	0	0	0
Scan-to-Scan Correlation	Per Noise Detection (1)*	125	1.7	85,000	316
	Per Star Detection (2)*	20	20	17,600	7,700
	Per Target Detection (3)*	0	0	0	0
Track Smoothing	40,000 per Track	0	0	0	0
Output Formatting	500 per Track	0	0	0	0
				341,560	43,776

(C) Total Computer Instructions

(1) *Per Noise Detection $100 + 200\left[\frac{\text{total exceedances/scan}}{50}\right]$

(2) *Per Star Detection $100 + 200\left[\frac{1 + \text{total exceedances/scan}}{50}\right]$

(3) *Per Target Detection $100 + 200\left[\frac{1 + \text{total exceedances/scan}}{50}\right]$

(C) The case described above represents the average computer load condition and does not include any targets. When targets are included, the overall computer load reduction achieved by the noise rejection circuitry is not as great because the computer instructions related to processing target information is, of course, not reduced. For the selected example where a maximum of 25 target tracks are included, the computer load distribution is as shown in Table II. It is seen that inclusion of the noise rejection circuitry results in a 68% reduction in the peak computer load.

4.2 Alternative System Trades

(U) The noise performance improvement resulting from the incorporation of the scan-to-scan noise rejection circuitry can be utilized for system gains other than a reduction in the computer load. For example, if the computer load is to be left unchanged, the inclusion of the noise rejection circuitry permits one to operate with a reduced threshold level (higher noise exceedance rate) and therefore an improved system detection sensitivity.

4.2.1 Improved System Detection Sensitivity

(U) On the assumption that the noise signal into the threshold circuit has a gaussian amplitude distribution (a generally valid assumption due to electronic filtering effects), Figure 4-1 shows a curve that relates threshold exceedance rates to threshold-to-noise ratio for a detector channel that utilizes a typical electronic filter bandwidth 0 to 20 KHz. The plotted curve corresponds to the analytical expression (Ref. 1);

$$N_T = N_o e^{\frac{-T^2}{2\sigma^2}} \qquad (4\text{-}1)$$

where N_T is the exceedance rate of a threshold set at voltage T

σ is the rms noise value, and
N_o is the (single direction) zero crossing gate given by Ref 1 ;

$$N_o = \frac{1}{2\pi} \left(\frac{w_a^2 - w_b w_a + w_b^2}{3}\right)^{\frac{1}{2}} \qquad (4\text{-}2)$$

for electronic filter bandwidth w_a tp w_b.

Ref. (1) J. S. Bendat, "Principles and Applications of Random Noise Theory", John Wiley & Sons Inc. New York pp 127-128.

Table II: MAXIMUM TARGET THREAT COMPUTER LOAD REDUCTION (U)

(C)

	Related Number of Computer Instructions	Number of Times Repeated Per Scan		Total Instructions Per Scan	
		Without Noise Rejection Ckt	With Noise Rejection Ckt	Without Noise Rejection Ckt	With Noise Rejection Ckt
Data Input Transfer	12 per Noise Detection	125	1.7	1,500	20
	12 per Star Detection	20	20	240	240
	12 per Target Detection	25	25	300	300
Data Format	12 per Noise Detection	125	1.7	1,500	20
	12 per Star Detection	10	20	240	240
	12 per Target Detection	25	25	300	300
Data Array Alignment A Corrections	24 per Noise Detection	125	1.7	3,000	40
	24 per Star Detection	20	20	480	480
	24 per Tar Detection	25	25	600	600
Data Stabilization	1600 per Noise Detection	125	1.7	200,000	2,720
	1600 per Star Detection	20	20	32,000	32,000
	1600 per Target Detection	25	25	40,000	40,000
Scan-to-Scan Correlation	Per Noise Detection (1)*	125	1.7	97,500	487
	Per Star Detection (2)*	20	20	19,600	8,740
	Per Target Detection (3)*	25	25	24,500	12,175
Track Smoothing	40,000 per Track	1(4)*	1(4)*	40,000	40,000
Output Formatting	500 per Track Observation	25	25	12,500	12,500
	1000 per Completed Track	1	1	1,000	1,000
				476,260	152,862

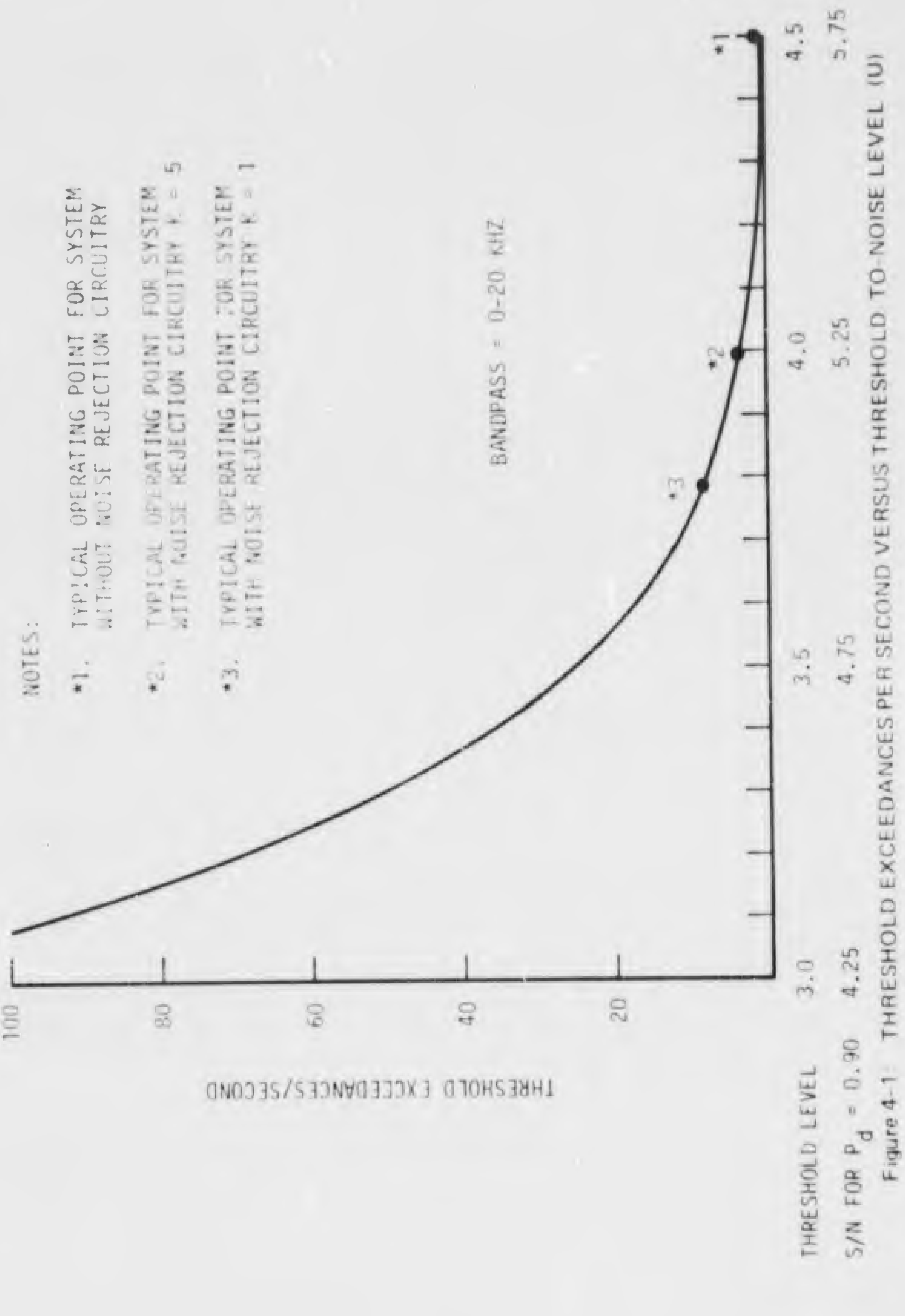
(C) Total Computer Instructions

(1) *Per Noise Detection $100 + 200 \left[\frac{\text{total exceedances/scan}}{50}\right]$

(2) *Per Star Detection $100 + 200 \left[\frac{1 + \text{total exceedances/scan}}{50}\right]$

(3) *Per Target Detection $100 + 200 \left[\frac{1 + \text{total exceedances/scan}}{50}\right]$

(4) *Assumes only one track per scan is completed and smoothed



NOTES:

*1. TYPICAL OPERATING POINT FOR SYSTEM WITHOUT NOISE REJECTION CIRCUITRY

*2. TYPICAL OPERATING POINT FOR SYSTEM WITH NOISE REJECTION CIRCUITRY K = 5

*3. TYPICAL OPERATING POINT FOR SYSTEM WITH NOISE REJECTION CIRCUITRY K = 1

Figure 4-1 THRESHOLD EXCEEDANCES PER SECOND VERSUS THRESHOLD TO NOISE LEVEL (U)

(U) Signal-to-noise ratios for 90% probability of detection are also shown along the axis of Figure 4-1.

$$(S/N)_{P_d = 0.9} = T/N + 1.25 \qquad (4\text{-}3)$$

By way of example, consider a typical system setting

(C)

Thres/N Setting	S/N for 90% Probability or Detection	Single Channel Threshold Exceedance Rate (Bandwidth 0-20 KHz)
4.5	5.75	0.46 per sec

(C) The threshold exceedance rate per detector channel is 0.46 which represents a typical noise rate imposed on a tracking computer. If scan-to-scan noise rejection circuitry is included (with K=1 see Section 2.1) the noise rates into the rejection circuitry can be increased to 9.0 exceedance per sec per detector channel while maintaining the computer load at the initial value. Acceptance of the higher exceedance rates allow the threshold levels to be operated at 3.78 which corresponds to a 14.5% increase in system detection sensitivity because targets with S/N ratios down to 5.03 are now detected with $P_d = 0.9$. (If the noise rejection circuitry is shared between five detector channels, K = 5, see Figure 4-2, the corresponding increase in system detection sensitivity would be 9.6%).

(U) The example taken corresponds to a system that works well into system noise. In cases where high signal-to-noise is required on target detections, for example where multicolor discrimination or high tracking accuracy is required, the threshold will be set higher (to minimize noise load on the computer) and the improvement in system detection sensitivity attributable to the noise rejection then increases over that computed above. Figure 4-2 shows how the system detection sensitivity improvement changes as a function of (S/N) for $P_d = 0.9$.

4.2.2 Aperture Equivalence

(U) An interesting alternative to the inclusion of the scan-to-scan noise rejection circuitry is to consider that the optical aperture is increased to achieve the same result in terms of either reduced computer load (Section 4.1) or increased system detection sensitivity.

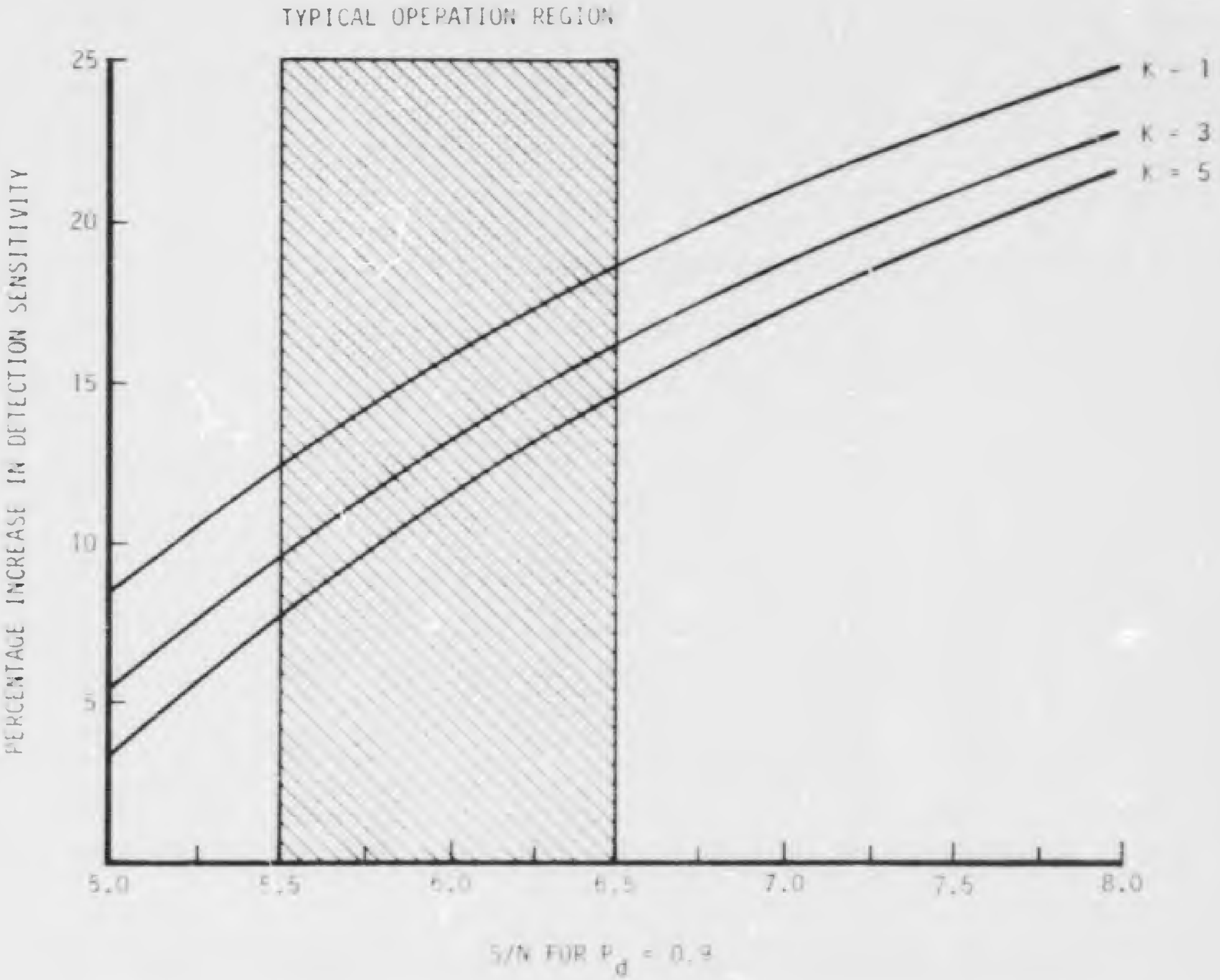


Figure 4-2 SENSITIVITY IMPROVEMENT AS A FUNCTION OF S/N FOR $P_d = 0.9$ (U)

(U) Because the detection sensitivity of a system is proportional to the diameter of the optics, the detection sensitivity improvements plotted in Figure 4-2 can be directly interpreted as equivalent increases in aperture diameter.

(C) It is concluded that the scan-to-scan noise rejection circuitry is an Electronic Alternative to Aperture. Unfortunately the amount of "electronic aperture" can correspond to only about a 15% increase in the physical aperture diameter. The operational significance of this electronic equivalence of aperture clearly depends on the system application being considered. In large cryogenically cooled sensors the noise rejection circuit will probably offer a worthwhile alternative to physical aperture, but in small uncooled sensors the related electronic complexity will be unjustified.

(U) The above described equivalence of noise rejection circuitry and aperture is based on consideration of the detection sensitivity of a system. In terms of other (more complex) system parameters, such as multicolor discrimination performance or tracking accuracy performance, the equivalence of noise rejection circuitry and aperture is not fully maintained. However, in any specific system application one can, by selecting different design alternatives, usually trade improvements in one performance parameter (e.g. detection sensitivity) for improvements in another performance parameter (e.g. tracking accuracy), thus the benefit of the noise rejection circuitry may be traded for selected improvements in one or more of the most critical system parameters. The methods and limits of trading between system performance parameters has not been well documented, and a need exists for a thorough analysis of that subject.

5.0 REJECTION OF STATIONARY BACKGROUNDS

As the evaluation of the scan-to-scan noise rejection circuitry has progressed, it has become clear that a careful modification of the concept may widen its applicability to encompass the rejection of stationary backgrounds in addition to the rejection of random noise effects studied under this contract. The logic so far discussed passes to the computer all detections that have a close detection on the previous scan. Thus the tracking computer is burdened with tracking many unwanted tracks that arise from stars and spatial (cloud) backgrounds. Unlike the random noise effects, an increase in physical aperture size cannot reduce the consequences of a star field or spatial background.

Consider initially a condition where the TWS sensor is well stabilized. In this case, the shift register circuitry can impose the criteria that a detection is passed to the tracking computer only if:

1) there is a close detection on the previous scan,

and

2) that the previous close detection (or one some several scans earlier) possessed a measurably different azimuth angle to the present sighting

This criterion would reject tracks that do not exhibit azimuth rates greater than some selectable minimum rate.

The circuitry is identical to that shown earlier in Figure 2-1 except that the shift register taps that corresponds to exact revolutions are omitted from the gate logic. A conceptual diagram for implementation of the above criteria is shown in Figure 5-1.

To be of greatest value the requirement that the TWS sensor be stabilized should be removed. In this regard, two approaches can be considered. Firstly, by including variable clock delay circuits as shown in Figure 5-2 it should be possible to adaptively correct for the changes in (azimuth) observation angles caused by measured instability of the sensor (equal corrections to small group of detectors should be sufficient in most cases).

In this case it is assumed that azimuth correction magnitudes can be accurately derived from the inertial reference system which accompanies the TWS sensor.

A second, more powerful approach might use pattern recognition technique, to sense and track the angular changes that occur in the background observations (due to the sensor instability) and then pass to the track logic only those detections that are sensibly different from the background motion. Specific methods for implementing the pattern recognition sensing have not been developed, but the overall concept appears to be well suited to the low cost digital pattern recognition capability currently being developed at Boeing under independent research and development funds. Such a concept of background tracking by pattern recognition may be applied in one or two dimensions (azimuth only, or azimuth plus elevation). In either case the concept depends on the requirements that:

1) the majority of detections arise from background, and
2) the background has the property that spatially close detections behave similarly to each other.

The pattern recognition approach can be used to reject both stationary and moving backgrounds. Targets are detected on the basis of their behavior being different from that of the background that surrounds them.

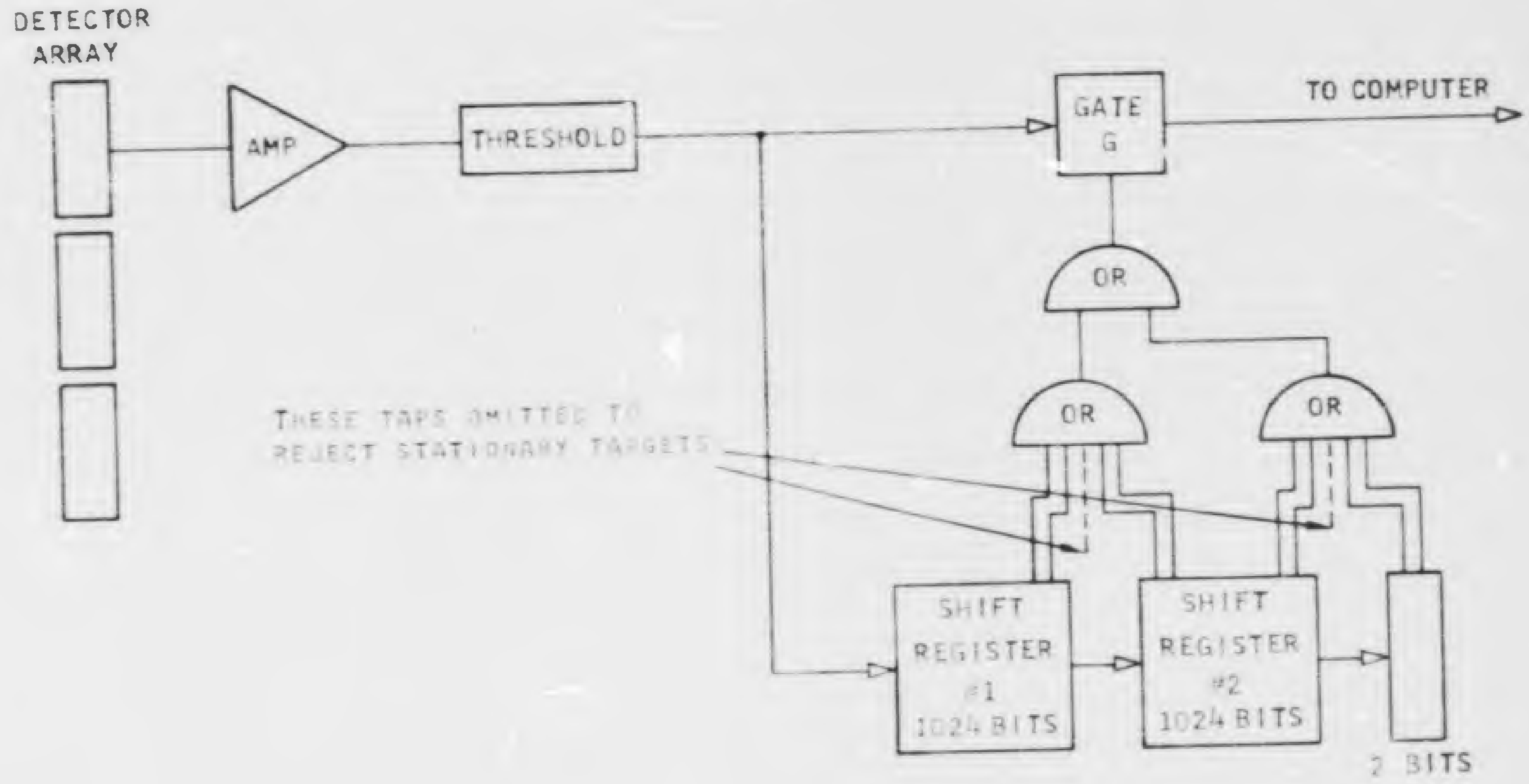


Figure 5-1 BASIC SCAN TO SCAN NOISE REJECTION CONCEPT

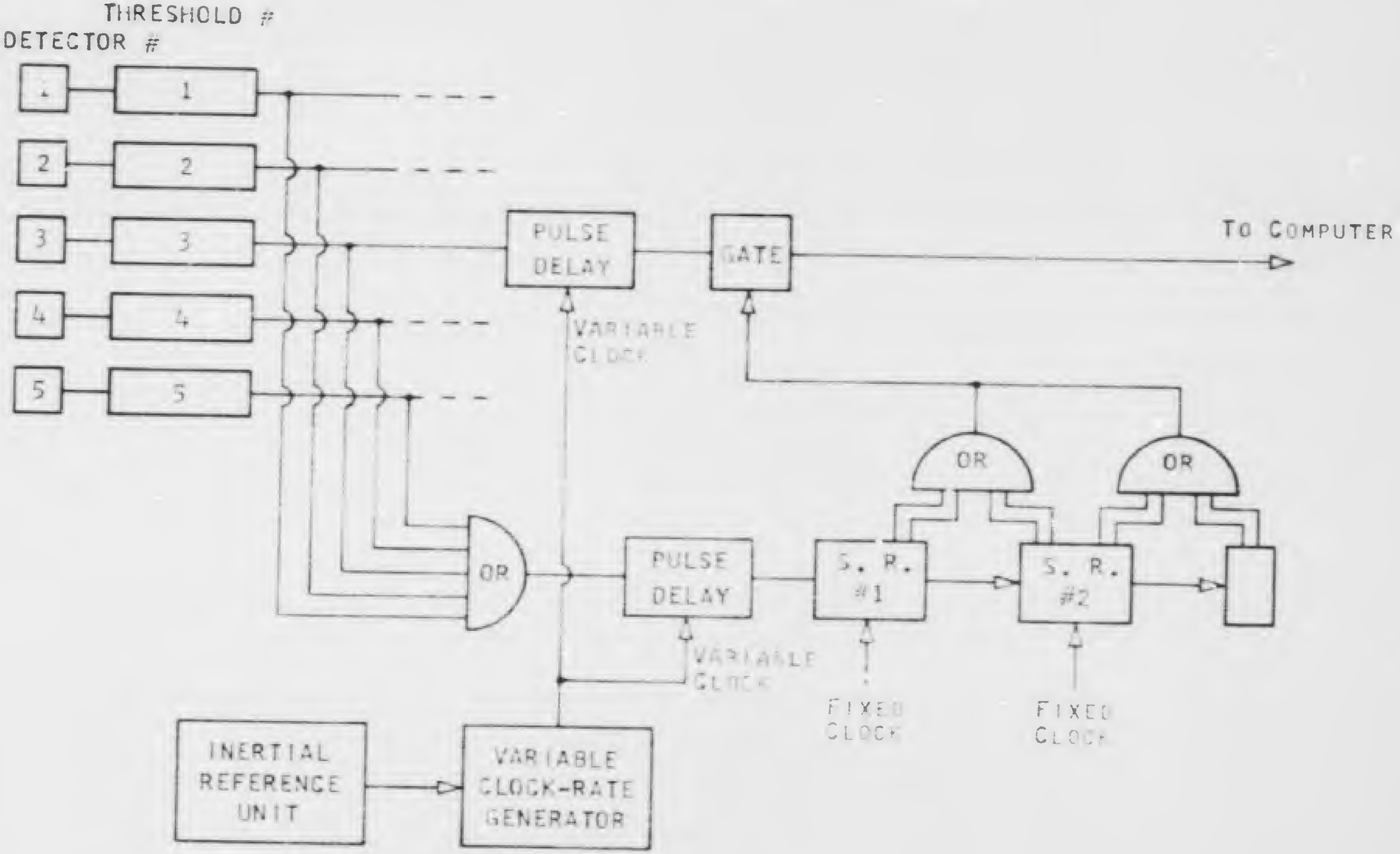


Figure 5-2 NOISE REJECTION CIRCUITRY WITH ADAPTIVE CORRECTION FOR PLATFORM ATTITUDE

Conclusions

(U) A noise rejection concept has been evaluated theoretically and experimentally and it has been shown that inclusion of the noise rejection circuits in an infrared track-while-scan sensor can lead to either an easing of the related computer load or an improvement in system performance.

(C) With the detection threshold level left unaltered, the inclusion of the noise rejection circuitry reduces the average computer load by typically 87 % and reduces the peak load (which occurs when tracking a maximum number of system track) by typically 68 %.

(C) As an alternate to reducing the computer load, the detection threshold can be lowered and the detection sensitivity of the system increased by approximately 15%.

(U) Laboratory tests have verified the performance characteristics of the noise rejection circuitry when tracking simulated stationary and moving targets, and have demonstrated that implementation of the noise rejection circuitry can be accomplished with low-cost low-weight microelectronic modules.

APPENDIX I

Shift Register Technology

The entire field of microelectronics has made very rapid progress since 1962, but in no area has the progress been more rapid than in the field of shift register design. Figure I-1 shows the trend of shift register cost for the period from 1962 to 1972.

Early shift registers were implemented using discrete components resulting in relatively high cost per bit (approximately $10) and low density packaging (1 shift element per 4" by 4" card). The development of Resister-Transistor-Logic (RTL) led to a package density of 1 shift elements per TO-5 package lowered the cost per shift element to approximately $4. The RTL circuits were sensitive to power buss and other system noise making them generally unsuitable for long shift registers. The noise problems were overcome in 1966 with the introduction of Transistor-Transistor Logic (TTL) and the price dropped to approximately $1 per bit and the package density increased to 2 shift elements per package. (TTL technology was used in implementing the test hardware shown in Figure 3-3).

The most dramatic cost and packaging breakthrough came with the development of Metal Oxide Silicon (MOS) circuitry. Only one third as many process steps are needed in the fabrication of MOS circuits as are needed for fabricating TTL circuits which makes MOS ideally suited to Large Scale Integration (LSI). Using current technology LSI it is possible to package a 1000 bit shift register in a single package. Power requirements for the MOS shift registers are typically less than 100 micro watt per bit, compared to 1 milli-watt per bit for TTL circuitry (usually an important consideration in satellite systems). The present cost of MOS shift registers is approximately one cent per bit and is expected to drop to 0.5 cents per bit in the near future.

MOS shift registers are divided into two classifications - static and dynamic. The static shift register uses two inverters in the form of a latch to store the data indefinitely. There is no minimum frequency of operation. The dynamic shift register temporarily stores the data on a

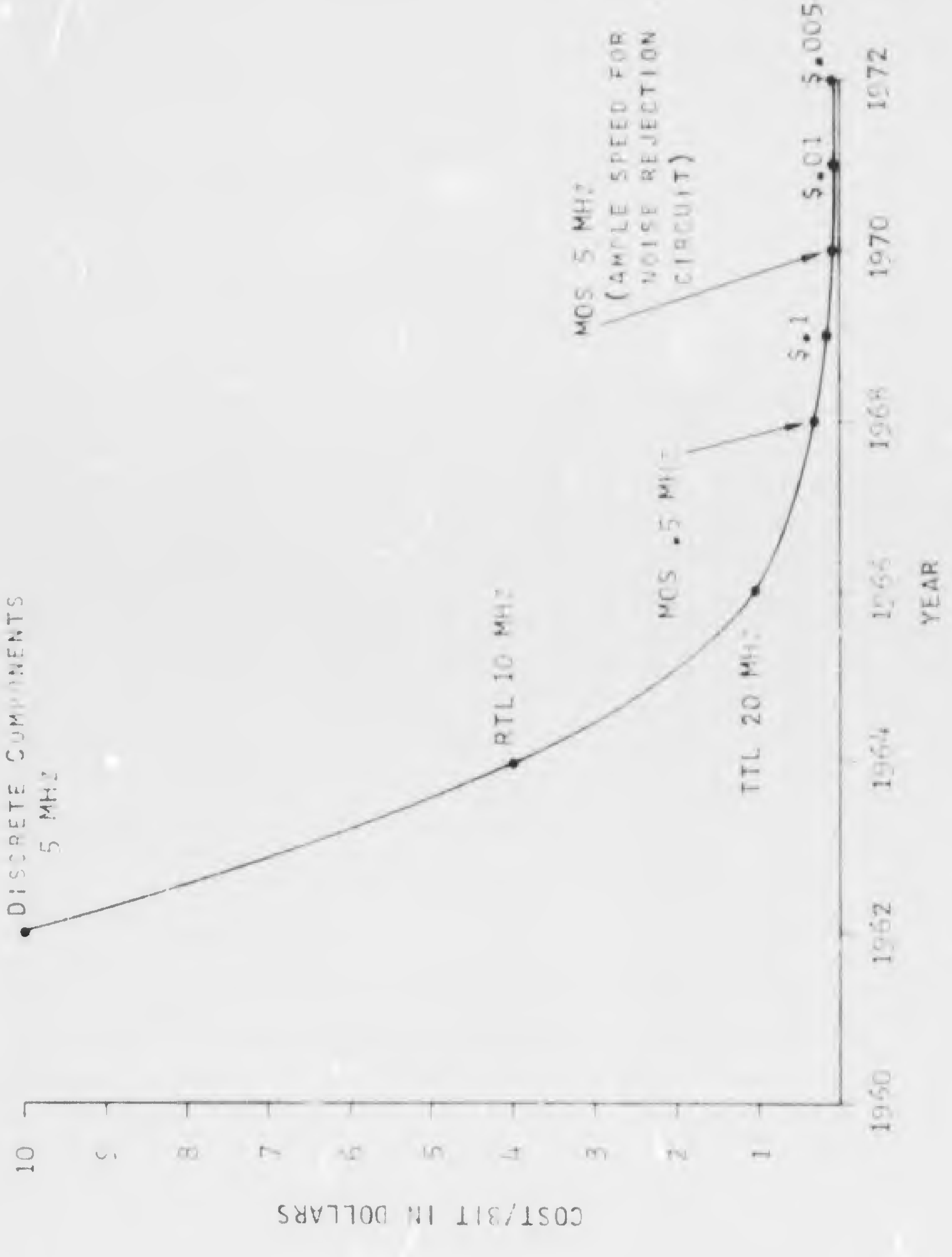


Figure F-1. SHIFT REGISTER COST TRENDS

capacitor inherent to a MOS device and cannot be operated below a certain clock frequency or the data will be lost. The dynamic shift register usually offers a speed advantage over the static registers (typically 5 MHz dynamic compared to 2 MHz static) and consume less power.

An example of a MOS shift register card is shown in Figure I-7 . This shift register card contains eight 1000 bit shift register circuits along with the associated clock drivers and gates and would be representative of the circuitry required to implement four complete noise rejection circuits like that shown in Figure I-2.

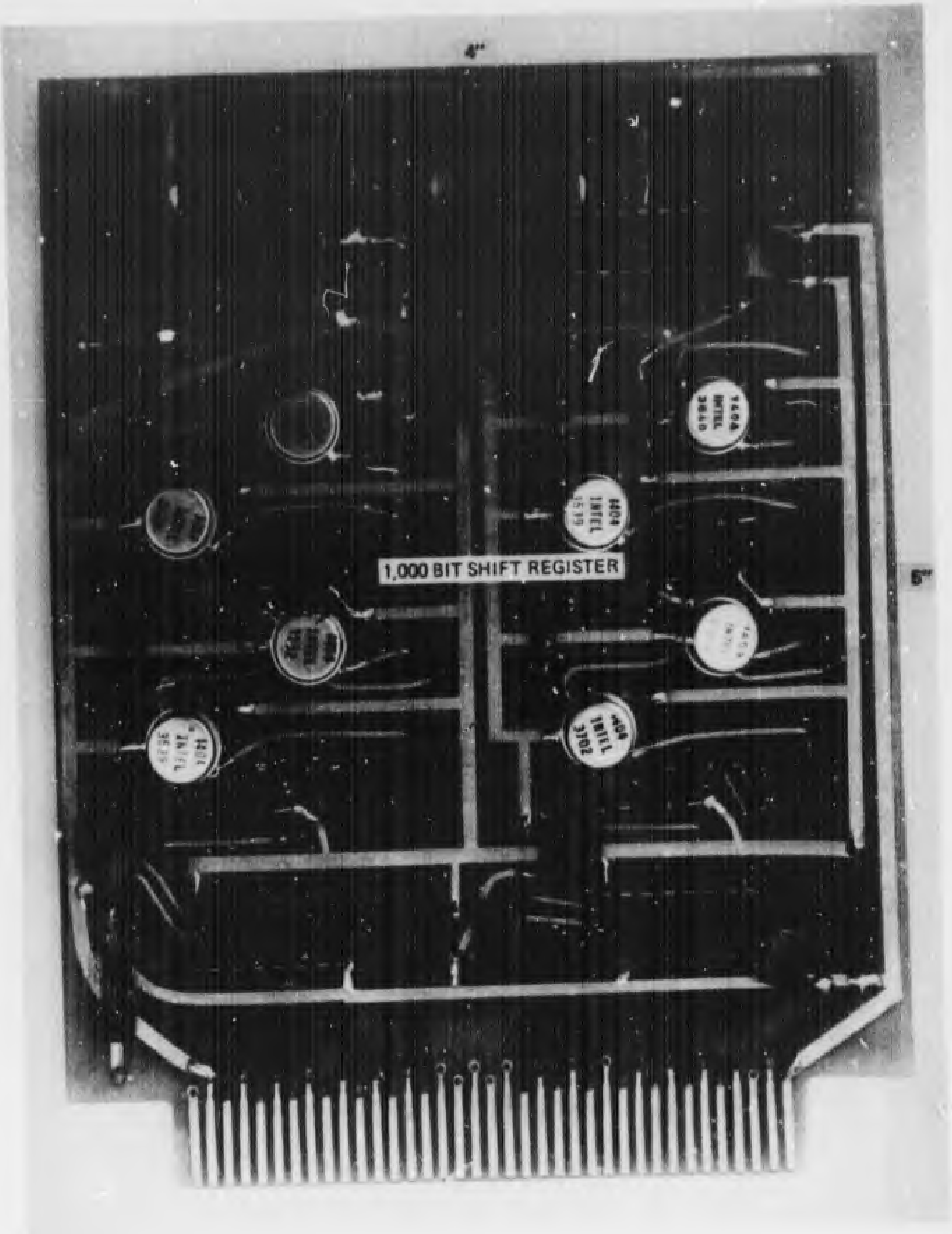


Figure I-2. MOS SHIFT REGISTER CARD

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13 ABSTRACT

This final technical report describes the work accomplished on the Track-While-Scan Data Processing Investigation Contract. The objective of this program was to demonstrate the feasibility of using simple microelectronic shift register circuitry to inhibit detections that do not satisfy appropriate scan-to-scan correlation criteria. In the absence of such rejection circuitry, the TWS digital computer is required to sort and reject frequent noise detections and this substantially influences the size of computer required. (U)

The program entailed the fabrication of noise rejection circuitry and its evaluation in conjunction with the breadboard infrared Track-While-Scan subsystem developed under an earlier contract. The results of the evaluation tests have verified the performance characteristics of the noise rejection circuitry when tracking simulated and moving targets, and have demonstrated that implementation of the noise rejection circuitry can be accomplished with low-cost low-weight microelectronic modules. (U)

The performance gain resulting from the inclusion of the noise rejection circuitry in a typical infrared track-while-scan sensor is shown to correspond to either (1) a 68% easing of the computer load or (2) a 15% improvement in detection sensitivity. (U)

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