BLANK PAGE

TRANSISTOR CHARACTERIZATION AND DERATING FOR SECOND BREAKDOWN

Bernard Reich
Edward B. Hakim

DA TASK NR. 1G622001A056-01

ABSTRACT

Two modes attributing to secondary breakdown in transistors have been found - the current and voltage modes. Localized spots due to current constriction as a result of either mode causes an exponential rise in thermal resistance prior to secondary breakdown. These localized secondary breakdown spots have been calculated to be between 900°- 1100°C in silicon. The study indicates that the maximum secondary breakdown power is a function of the device design and should be considered in light of other device performance requirements.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORIES
FORT MONMOUTH, NEW JERSEY

CONTENTS

FIGURES

LIST OF SYMBOLS

θ = The thermal resistance over entire operating bias range.

θ_o = The thermal resistance over a portion of the operating bias range, where θ is relatively constant.

C = The slope of thermal resistance versus voltage curve.

V_o = The bias voltage at which the slope of capacitance versus voltage curve departs from the normal cube or square root dependence. Also the voltage above which θ rises exponentially with voltage.

T_{crit} = The difference in temperature between the localized hot spot in the junction and the ambient causing second breakdown.

$I_{sb}(I_m)$ = The current at which secondary breakdown occurs.

k = The slope of thermal resistance versus current curve. Also the negative slope of the low frequency small signal current gain versus current curve.

I_o = The bias collector current at which the thermal resistance begins increasing exponentially.

P_{MS} = The maximum secondary breakdown device power.

P_V = The derated secondary breakdown power with applied voltage above V_o.

γ = Emitter efficiency.

β = Base transport factor.

α^* = Collector multiplication ratio.

M = Avalanche-current multiplication factor.

TRANSISTOR CHARACTERIZATION AND DERATING FOR SECOND BREAKDOWN

INTRODUCTION

Second breakdown still appears to be a major limiting factor in the power performance and power handling capability of transistors. This is clearly evidenced by recent specifications on power transistors which have been released by manufacturers supplying devices for large signal applications. In addition, some manufacturers have prepared for their users extensive amounts of data on derating for second breakdown in pulse applications.[1,2] It is, therefore, quite apparent that the second breakdown problem has been recognized in devices intended for audio, switching, and r-f power applications.[3,4,5]

The present state-of-the-art in characterizing transistors for their second breakdown limitation has been by brute force techniques. In order to publish second breakdown derating curves as a function of voltage, temperature, time, etc., manufacturers have been forced to utilize destructive testing. At present it appears that there are no elegant methods developed for predicting the onset of second breakdown.

Although the problem of second breakdown has been with the industry since junction transistors were first made, it was not recognized as such until 1958.[3] Solutions to the second breakdown problem have been few and have been limited to circuit considerations either internal or external to the device.

An interim solution involving device design has been proposed by one of the authors.[6] For devices which lend themselves to this type of voltage limitation, punch-through prior to collector-base avalanche breakdown reduces the voltage effects of second breakdown. This type of design is limited primarily to the homogeneous base transistor, such as the alloy or single diffused junction device.

At the time of this writing, it is felt that while the problem of second breakdown has been widely recognized it is still one of the major limiting factors with respect to power handling ability of transistors. Furthermore, little progress has been made to date on a practical basis toward the solution of the problem with the possible exception of the punch-through limited transistor. Second breakdown cannot be completely eliminated, but device design steps must be taken to extend it beyond the normal operating range of the transistor.

The purpose of this paper is to report the latest findings on second breakdown and to possibly shed some light on a parametric non-destructive characterization of second breakdown.

DISCUSSION

Parametric Indications Related to Second Breakdown

The effectiveness of second breakdown in reducing power dissipation is shown in Fig. 1. In Fig. 1 a plot is made of the second breakdown burnout power; i.e., current and voltage the instant before second breakdown occurs as a function of applied collector voltage for a group of silicon triple diffused transistors (2N1506). It is noted that as the collector voltage increases the burnout power decreases. Between 50 and 90 volts there is almost a two to one reduction in burnout power.

While in Fig. 1 the burnout power is shown as a function of voltage, from other observations it is believed that there exists two second breakdown modes. These modes have been previously identified as the "high current" and "premature" modes.[6] From our recent work, these modes have been recharacterized as simply a "voltage" and "current" mode. This becomes more evident as further data is presented.

In either mode the predecessor to catastrophic failure is a reduction in the power handling capability of the transistor, or more precisely an increase in the thermal resistance of the device. Information on the variation of thermal resistance with applied voltage and current was previously reported by one of the authors.[7] The technique of measurement utilized the sampling of the current gain, h_{FE}, or forward voltage drop, V_{BEF}, on a continuous basis.[6] Utilizing the d.c., current gain, h_{FE}, as the temperature sensitive parameter it appears that the hottest spot in the transistor is sensed. When these techniques of measurement are applied a thermal resistance versus voltage plot is obtained as shown in Fig. 2 (device type 2N2037). While there is a difference in the magnitude of θ and the slope between curves, both curves indicate that above approximately 30 volts the thermal resistance rises more rapidly with voltage. The variation of thermal resistance with voltage can be expressed as:

$$\theta = \theta_o \quad e^{C(V-V_o)} \qquad (1)$$

$$\text{for } V > V_o$$

where θ_o is the thermal resistance which remains relatively constant to some voltage, V_o, C is the upper slope of the discontinuous θ vs V curve, and V is the applied collector-base voltage.

In Fig. 2, $V_o \cong$ 30 volts, and θ_o = 35° C/W (V_{BEF} method) and θ_o = 43° C/W (h_{FE} method). In Fig. 2, C = 0.026 (V_{BEF} method) and C = 0.046 (h_{FE} method). Equation (1) predicts that for the device shown in Fig. 2 the power derating above approximately 30V would be 1.3 - 1.5 for each 10 volts in excess of V_o.

BLANK PAGE

Assuming, at this time, that the applied voltage is the only contributing parameter causing the thermal resistance to rise an expression can be derived linking power dissipation to applied voltage. It is further assumed that the thermal resistance measured indicates the hottest spot in the device and when this spot reaches a critical temperature, second breakdown occurs.

Classically the thermal resistance and junction temperature rise are related by:

$$\Delta T = P\theta$$

where ΔT is the rise in temperature between junction and case or ambient, θ is the appropriate thermal resistance, and P is the applied power.

If now excess heating due to applied voltage is taken into account,

$$\Delta T = P\theta_o e^{C(V-V_o)} \quad .$$

Assuming that the exponent $C\ (V-V_o)$ is small so that $e^{C(V-V_o)}$ can be expanded into a McLaurin series, then

$$\Delta T \cong P\theta_o \left[1 + C\ (V-V_o) \right] \quad .$$

At some critical localized temperature second breakdown occurs so that,

$$\Delta T_{crit} = VI_{sb}\theta_o \left[1 + C\ (V-V_o) \right]$$

$$I_{sb} \cong \frac{\Delta T_{crit}}{\theta_o \left(V\ (1-CV_o) + CV^2 \right)}$$

where: $I_{sb}(I_m)$ = the current at which second breakdown occurs. (2)

If $CV_o = 1$, then

$$I_{sb} = \frac{\Delta T_{crit}}{\theta_o\ (CV^2)} \tag{3}$$

or that the second breakdown current is inversely proportional to the square of the applied voltage.

If $CV_o \ll 1$, then

$$I_{sb} \cong \frac{\Delta T_{crit}}{\theta_o\ (V + CV^2)} \quad . \tag{4}$$

The ultimate in performance from a second breakdown point of view would be to have C = 0 over the operating range of the devices. In the case of the homogeneous base devices the increase of thermal resistance does not appear to occur below BV_{CEO} , i. e., C = 0, equation (4). If punch-through is incorporated into such a device then for all practical purposes C = 0 over the operating voltage range of the transistor.

The above information is now compared to the results of Chang and Turner.[2] Chang and Turner indicate that for single diffused devices,

$$I_{sb} = KV^{-1}$$

where K is a power constant.

From observed results at these Laboratories on single diffused devices (2N1479 & 2N1480), punch-through occurred prior to collector-base breakdown and following punch-through, C = 0, reducing equation (2) to:

$$I_{sb} = \frac{\Delta T_{crit}}{\theta_o V} \quad . \tag{5}$$

For triple diffused devices Chang and Turner indicate that under d.c. conditions,

$$I_{sb} = KV^{-2.2}$$

which again is in good agreement with equations (3) and (4). Chang and Turner's results have been promulgated based on direct device measurements.

All of the above results have been presented assuming that the presence of current had no unusual effects on the second breakdown point. A similar analysis can be presented assuming that the current alone contributes to the onset of second breakdown. Therefore, it is assumed that the applied voltage is below V_o, equation (1). Consider the thermal characteristics of a device operated well below V_o, as in Fig. 3 in which a plot of thermal resistance versus current is shown. As was previously noted with voltage beyond some current level, I_o, the thermal resistance increases with current so that,

$$\theta = \theta_o \; e^{\,k(I - I_o)}$$

where k is the slope of the θ vs I curve (beyond $\theta = \theta_o$) and I_o is the threshold current.

From examination of many devices it has been found that:

$$I_o \cong \left| \frac{1}{k} \right|$$

therefore, $\theta = \theta_o \, e^{(kI - 1)}$

and $\Delta T = P\theta_o \, e^{(kI - 1)}$.

Assuming (kI - 1) to be small,

$$\Delta T = VI \, \theta_o \, (kI) \ .$$

When $\Delta T = \Delta T_{crit}$ second breakdown occurs and

$$I_{sb} \cong \sqrt{\frac{\Delta T_{crit}}{V\theta_o k}} \ . \qquad (6)$$

Equations (3) and (4) describe the transistor for second breakdown in the voltage mode and equation (6) for the current mode. From equation (6) it is clearly indicated that second breakdown in the "current" mode is dependent on the following factors as related to the terms of equation (6):

1. Materials and processing (ΔT_{crit})

2. Area, materials, and effectiveness in contacting for reduced thermal resistance (θ_o)

3. Applied voltage (V)

4. Current crowding factor (k).

Exponential Coefficients "C" and "k"

It is evident from the foregoing discussions that the key parameters in equations (2) and (6) are the exponents "C" and "k". The authors have directed much effort in obtaining an understanding of the factor "k".[9] The factor "k" can be obtained on any given device by examining the current gain, h_{fe}, fall-off with collector current as follows:

$$\frac{h_{fe1}}{h_{fe2}} = \exp - k \ (I_2 - I_1) \qquad (7)$$

where h_{fe1} is the small signal low frequency current gain at the lower current level, I_1, (amperes); h_{fe2} is the small signal low-frequency current gain at the higher current level, I_2, (amperes); and k is the slope of the h_{fe} vs I_c curve.[9]

It has been found that the factors which are necessary to reduce the variation of current gain with increasing collector current at high injection levels also assist in keeping the second breakdown current high. These factors are directed primarily to improving the emitter efficiency at high current levels and are summarized as follows:

(a) Large ratios of emitter peripheral length to emitter area

(b) Highest base conductivity in keeping with other device critical parameters

(c) Minimum base width in keeping with other parameters.

From a group of units of the same geometry, it has been found by this study that the second breakdown current is related to the figure of merit derived in reference 6

$$FM \simeq \left(\frac{J_o}{A}\right) 3 \, (f\alpha)^{-1/2} . \tag{8}$$

The above figure of merit was developed for silicon planar epitaxial transistors but would appear to hold for other diffused devices. It should be clearly pointed out that the above discussion with respect to the factor "k" held only if no unusual voltage effects were present.

The factor "C" in equation (2) relates to the voltage contribution second breakdown. The design considerations related to "C" have been examined, but a simple parametric expression for it has not been developed. Therefore, at present we must rely on the thermal resistance versus voltage measurements to obtain its absolute value. However, it has been found that "C" is related to the build-up of the electric field across the depletion region in the collector junction. Along with the absolute value of "C" it is necessary to obtain an indication of when the voltage V_o is exceeded. The voltage V_o is the maximum voltage which may be applied before the thermal resistance begins to increase. To correlate the voltage at which θ rises with the physical properties of the transistor several areas were investigated.

In the past, many manufacturers of power transistors have assumed by more or less rule of thumb that the maximum "safe" voltage that could be applied to a transistor was BV_{CEO}. From this study, the rule of thumb appears valid for homogeneous base transistors. However, for the more advanced devices, such as triple diffused or epitaxial devices, this rule of thumb does not hold in all instances. Observations on the maximum applied voltage prior to the increase in thermal resistance have been correlated with another parametric measurement.

In Fig. 4 a plot is made of the output capacitance, C_{ob}, as a function of collector-base voltage for a silicon triple diffused and a planar transistor. From Fig. 4 it is noted that the variation of capacitance with voltage is constant up to a particular voltage. Beyond

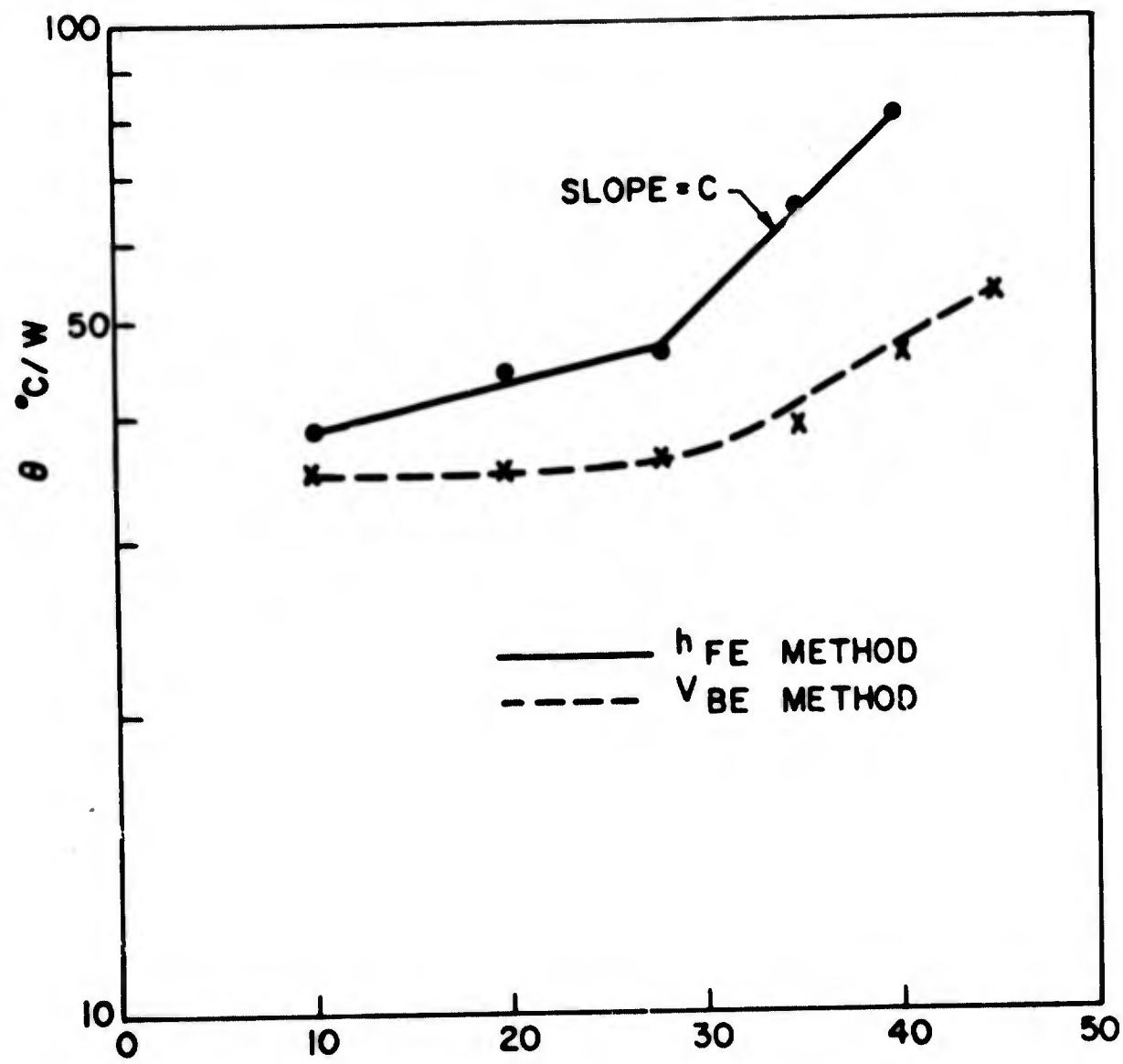

FIG. 2 - VARIATION OF THERMAL RESISTANCE WITH COLLECTOR - BASE VOLTAGE (2N2037)

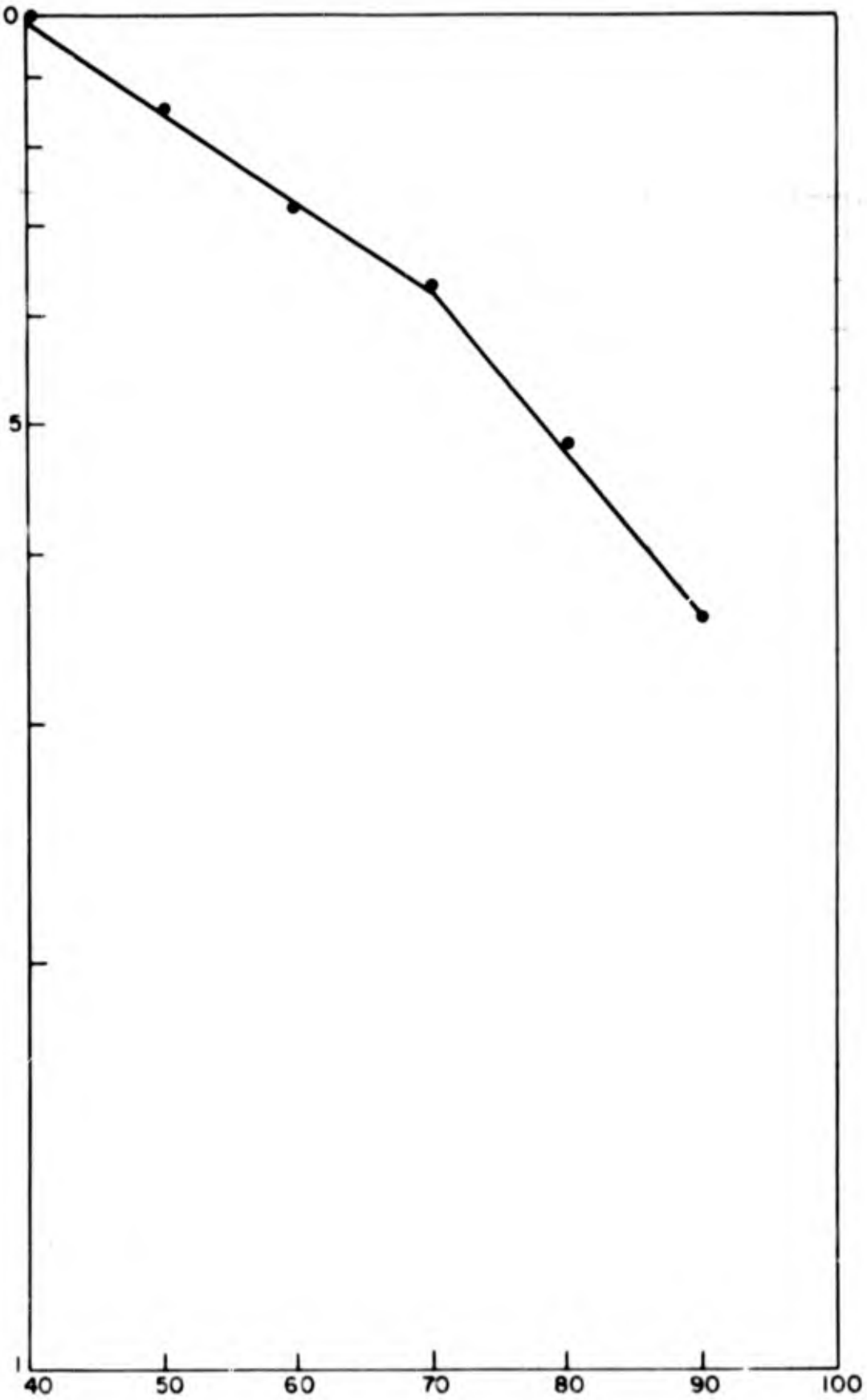

FIG. 1 - BURNOUT POWER VS COLLECTOR - BASE VOLTAGE (2N1506)

6. B. Reich, "New Aspects of Second Breakdown in Transistors," Solid State Design (to be published April 1964). USAELRDL TR 2319, November 1962.

7. B. Reich, "A New Approach to Transistor Reliability Prediction," Semiconductor Products, January 1963. USAELRDL TR 2295, August 1962.

8. B. Reich and E. Hakim, "An Appraisal of Transistor Thermal Resistance and Junction Temperature," USAELRDL TR 2364, November 1963.

9. B. Reich and E. Hakim, "Bulk Reliability Effects in Semiconductor Devices, Current Crowding in Transistors," (to be published). USAELRDL TR 2333, February 1963.

10. A. B. Phillips, "Transistor Engineering," pp 207 - 209, McGraw Hill Book Co.

occur at the emitter edge. In the voltage mode it is conceivable that above the voltage, V_o, that

$$\alpha = \gamma \beta \alpha^* M$$

exceeds unity and that there is base current reversal. The concentration process would then occur toward the center of the emitter rather than the edges which would cause this mode of failure and burnout.

CONCLUSIONS

1. There appears to be two modes causing secondary breakdown--the current and voltage mode. The current mode being the contributing factor for the fall-off of current gain with current, while the voltage mode is related to the voltage V_o.

2. Secondary breakdown in either mode is preceded by an exponential rise in thermal resistance in the device due to current constriction at localized spots.

3. The maximum secondary breakdown power is a function of the device design and should be considered in light of other device performance requirements.

4. The maximum "safe" operating voltage does not necessarily have to be BV_{CEO}.

5. Secondary breakdown spot temperatures are calculated to be between 900°- 1100°C in silicon.

6. Two parametric measurements which can be used for determining device capabilities are the plots of C_{ob} vs V_{cb}, and h_{fe} vs I_c .

REFERENCES

1. R. Greenburg, "Extending Safe Areas for Fast Switching Pulses," Motorola Engineering Report No. 87.

2. Z. F. Chang and C. R. Turner, "Characterization of Second Breakdown in Silicon Power Transistors," RCA Application Note SMA-21.

3. C. G. Thornton and C. D. Simmons, "A New High Current Mode of Transistor Operation," IRE Trans., Vol. ED-5, pp. 6 - 10; January 1958.

4. H. C. Lin, A. R. Hlavacek, and B. H. White, "Transient Operation of Transistor with Inductive Load," IRE Trans., Vol. ED-7, pp. 174 - 178; July 1960.

5. H. A. Schafft and J. C. French, "Second Breakdown in Transistors," PGED, IRE, March 1962.

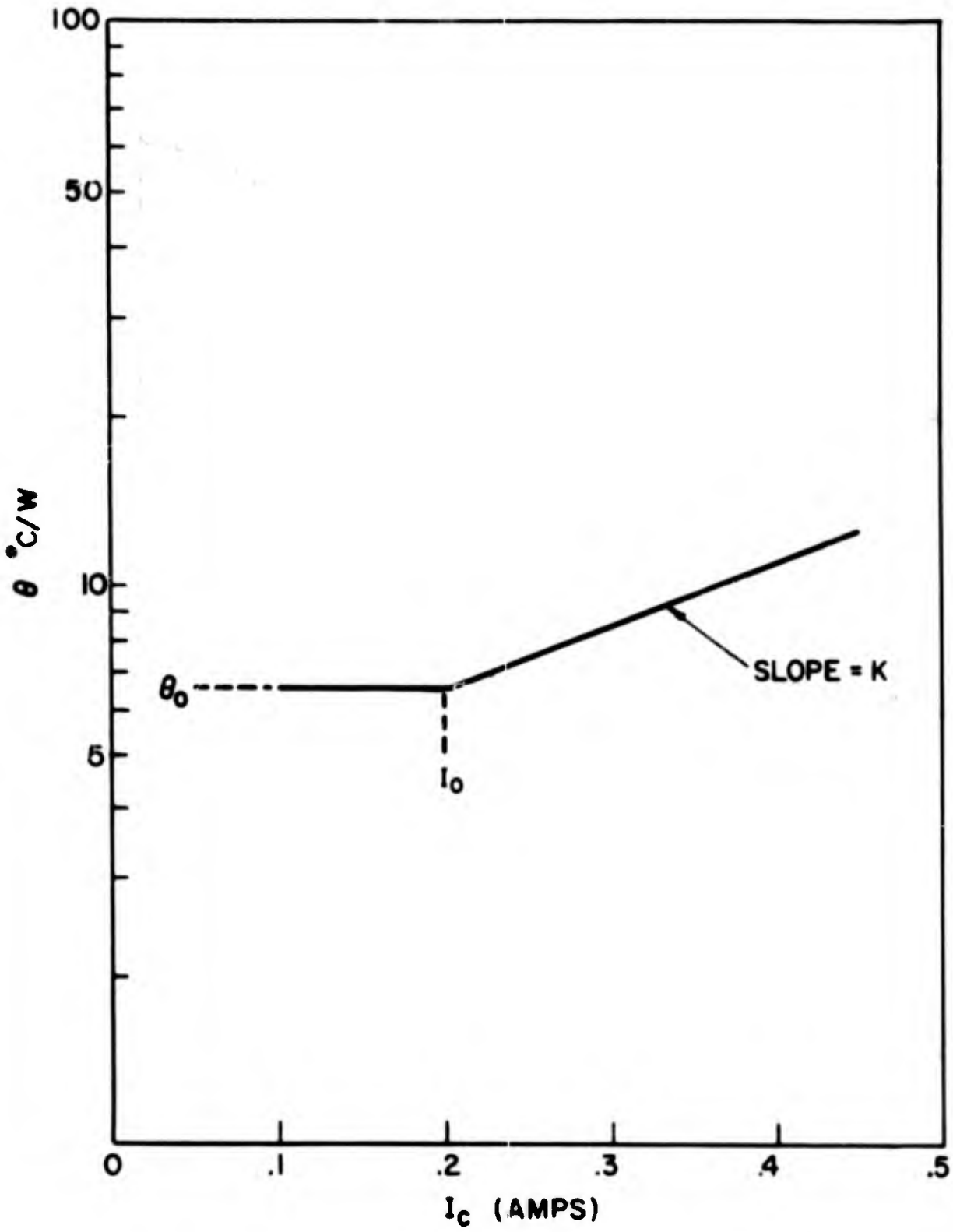

FIG. 3 - THERMAL RESISTANCE VS COLLECTOR CURRENT

this voltage the rate of change varies from the original curve and indeed becomes quite small. From observed data the break in the capacitance-voltage curve is the voltage beyond which the thermal resistance will rise with further increases in voltage and beyond which power is necessary.

A good explanation for what is believed to be occurring in an NPIN or epitaxial device is given by Phillips.[10] In essence, the assumption is made that all of the collector depletion layer goes into the epitaxial or I material for the epitaxial or triple diffused structure. It is assumed that the epitaxial or I thickness is represented by We and depletion layer thickness by X_{mb}. When the voltage is such that $We = X_{mb}$, this would represent V_o in our previously presented second breakdown analysis. Beyond this voltage, the electric field across the depletion region builds up at a more rapid rate causing the unusual observed thermal characteristics as previously shown in Fig. 2. It is apparent, therefore, that the optimum voltage design for epitaxial or triple diffused structures would be to have BV_{CEO} equal to the voltage at which the epitaxial or I region is completely depleted.

Critical Temperatures for Second Breakdown Occurrence

In equations (2) and (6) reference is made to ΔT critical which is the temperature at which second breakdown occurs, usually localized. Utilizing equation (1) and knowing the burnout power, voltage and case or ambient temperature, the temperature at which burnout occurred was calculated. For the silicon triple diffused transistors examined, calculated junction temperatures were between 800-900°C; and for the Si planar epitaxial devices, 1000-1100°C was the critical junction temperature. In germanium, where much less data was taken, the critical temperature was calculated to be 250-400°C for alloy types. The critical temperatures appear to be a function of the basic and ancillary materials necessary to fabricate the transistor, and of course the processing temperatures the devices experience in manufacture. The above calculation of junction temperatures is based on the curves of thermal resistance versus voltage as obtained by the continuous methods.[8]

Second Breakdown, Maximum Power and Voltage Derating

Utilizing equation (6) a comparison can be made of the maximum power handling capability from a second breakdown viewpoint to what is normally specified on a classical basis. Multiplying equation (6) by the applied maximum voltage, V_o, the maximum second breakdown power becomes:

$$P_{MS} = I_{sb} \times V_o \cong \sqrt{\frac{\Delta T_{crit} V_o}{k \theta_o}} . \qquad (9)$$

If $V > V_o$ the power the device can handle is reduced to:

$$P_V = \frac{P_{MS}}{\exp C (V - V_o)} . \qquad (10)$$

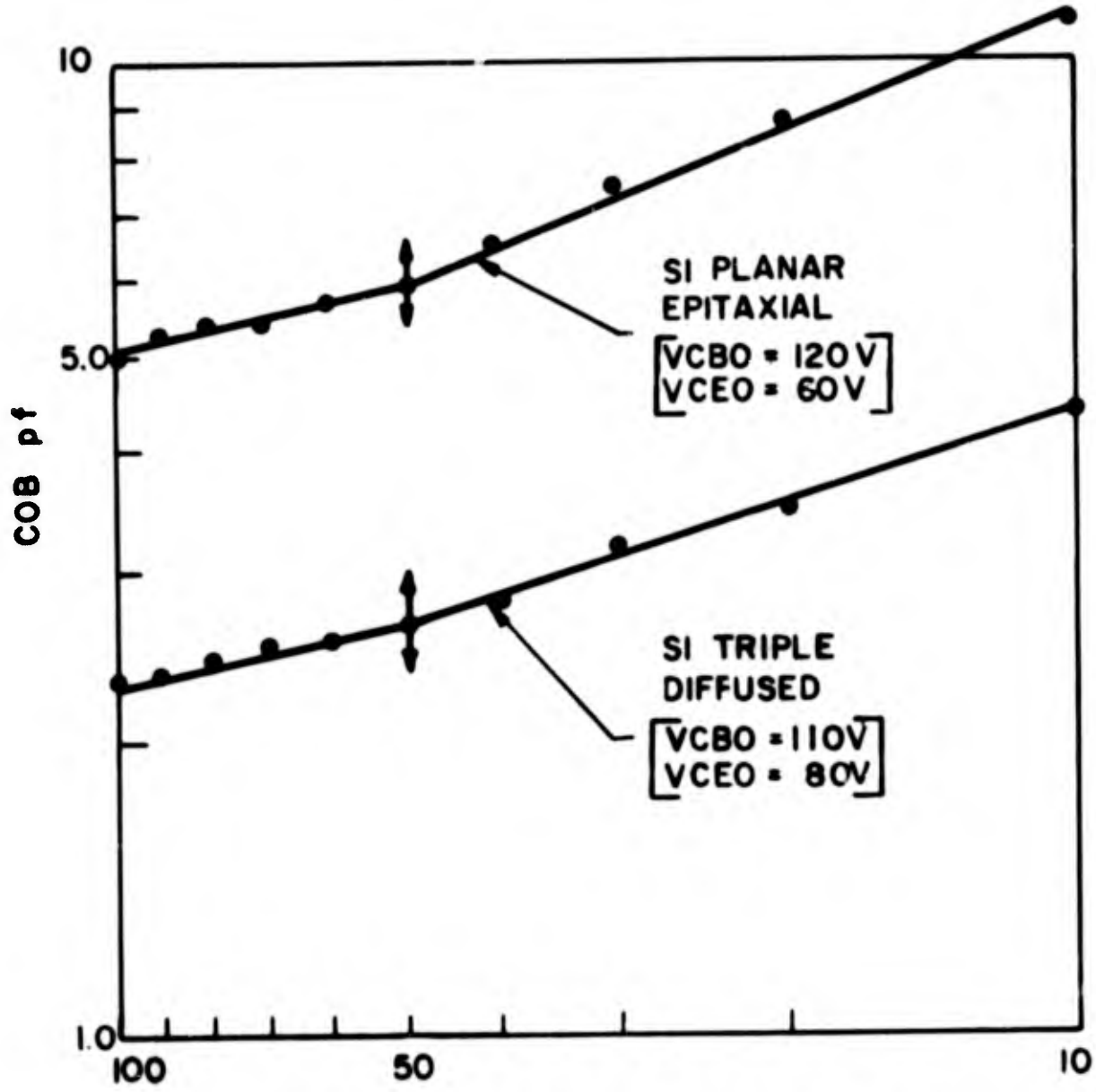

FIG. 4 - C_{ob} VS COLLECTOR - BASE VOLTAGE

For example, let us examine a triple diffused transistor with the following characteristics:

ΔT_{crit} = 900°C

V_o = 35 V

k = 2/amp

C = .024/volt

θ_o, j-c = 5°C/W

T_j max = 200°C

BV_{CEO} = 80 V.

The first point to be noted from the above characteristics is that V_o is approximately 1/2 BV_{CEO}. From classical methods of analysis, the power dissipation for this device at a 25°C case temperature is

$$P_{max} = \frac{\Delta T}{\theta_o} = \frac{175}{5} = 35 \text{ watts} .$$

From a second breakdown viewpoint the maximum power that can be dissipated would be using equation (9)

$$P_{MS} \cong \sqrt{\frac{900 \times 35}{2 \times 5}} \cong 56 \text{ watts.}$$

Utilizing equation (10) the voltage at which the second breakdown power is equal to the classical power is given by:

$$\exp C (V - V_o) = \frac{56}{35} = 1.6$$

$$V - V_c = 20 \text{ V}$$

$$V = 20 + 35 = 55 \text{ V} .$$

At 55 volts the device would fail from second breakdown if enough current were applied to bring the power product to 35 watts.

Second Breakdown and Types of Burnout

It has been previously stated that two secondary breakdown modes are possible (current and voltage modes). In a transistor, if the current mode is considered, i.e., no unusual voltage occurrences, the effects of lateral base current would be such that at high injection levels the center of the emitter would not function and all the current would concentrate at the edges. Therefore, in this mode of failure burnout should

DISTRIBUTION LIST

No. of Copies	Addressee
3	Commanding General U.S. Army Electronics Command ATTN: AMSEL-AD Fort Monmouth, New Jersey
1	Office of the Assistant Secretary of Defense (Research and Engineering) Attn: Technical Library Room 3E1065, The Pentagon Washington 25, D. C.
2	Chief of Research and Development Department of the Army Washington 25, D. C.
1	Chief, United States Army Security Agency Attn: ACofS,G4(Technical Library)Arlington Hall Station, Arlington 12, Virginia
1	Commanding Officer U.S. Army Electronics Research and Development Activity Attn: SELWS-AJ White Sands, New Mexico 88002
1	Commanding Officer U.S. Army Electronics Research Unit P.O. Box 205 Mountain View, California
1	Commanding Officer U. S. Army Electronics Materiel Support Agency(ATTN: SELMS-ADJ) Fort Monmouth, New Jersey 07703
2	Commanding General U.S. Army Materiel Command Attn: R&D Directorate Washington, D. C. 20315

No. of Copies	Addressee
1	USAELRDL Liaison Officer U.S. Army Combat Developments Command CDCLN-EL Fort Belvoir, Virginia
1	C.O., U. S. Army Engineer Research and Development Laboratories Attn: Technical Documents Center Fort Belvoir, Virginia
1	Commanding Officer U. S. Army Chemical Warfare Laboratories Attn: Technical Library, Bldg. 330 Army Chemical Center, Md.
1	Commanding Officer Harry Diamond Laboratories Connecticut Ave. & Van Ness St., N.W. Washington 25, D.C.
2	Headquarters, U.S. Air Force Attn: AFCIN Washington 25, D. C.
1	Rome Air Development Center Attn: RAALD Griffiss Air Force Base New York
1	Headquarters Ground Electronics Engineering Installation Agency Attn: ROZMEL Griffiss Air Force Base New York

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
1	Aeronautical Systems Div. Attn: ASNXRR Wright-Patterson Air Force Base, Ohio
1	U.S. Air Force Security Service Attn: ESD San Antonio, Texas
1	Headquarters Strategic Air Command Attn: DOCE Offutt Air Force Base, Nebraska
1	Headquarters Research & Technology Div. Attn: RTH Bolling Air Force Base Washington 25, D. C.
1	Air Proving Ground Center Attn: PGAPI Eglin Air Force Base, Florida
2	Air Force Cambridge Research Laboratories Attn: CRXL-R L. G. Hanscom Field Bedford, Massachusetts
2	Electronics Systems Div.(AFSC) Scientific & Technical Information Division (ESTI) L. G. Hanscom Field Bedford, Massachusetts 01731
1	Commander U.S. Naval Ordnance Laboratory White Oak Silver Spring 19, Maryland
1	Commanding General U.S. Army Satellite Communications Agency Attn: Technical Documents Center Fort Monmouth, N.J. 07703
1	Chief of Naval Research Attn: Code 427 Department of the Navy Washington 25, D. C.
1	Bureau of Ships Technical Library Attn: Code 312 Main Navy Bldg., Room 1528 Washington 25, D. C.
1	Chief, Bureau of Ships Attn: Code 454 Department of the Navy Washington 25, D. C.
1	Chief, Bureau of Ships Attn: Code 686B Department of the Navy Washington 25, D. C.
1	Director U.S. Naval Research Laboratory, Attn: Code 2027 Washington, D. C. 20390
1	Commanding Officer & Director, U. S. Navy Electronics Lab. Attn: Library San Diego 52, California
20	Commander, Defense Documentation Center Attn: TISIA Cameron Station, Bldg. 5 Alexandria, Virginia 22314

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
1	AFSC Scientific/Technical Liaison Office U.S. Naval Air Development Center Johnsville, Pennsylvania
1	USAELRDL Liaison Officer Naval Research Laboratory Attn: Code 1071 Washington, D. C. 20390
1	USAELRDL Liaison Officer Massachusetts Institute of Technology Bldg. 26, Room 131 77 Massachusetts Avenue Cambridge 39, Massachusetts
1	USAELRDL Liaison Office Aeronautical Systems Division Attn: ASDL-9 Wright-Patterson Air Force Base, Ohio 45433
1	U.S. Army Research Liaison Office, Lincoln Laboratory P.O. Box 73 Lexington, Massachusetts
1	USAELRDL Liaison Officer Rome Air Development Center Attn: RAOL Griffiss Air Force Base New York 13442
1	Chief, Pacific Field Office US Army Electronics Materiel Support Agency, APO 958 San Francisco, California
1	Technical Director, SELRA/CT Headquarters, USAELRDL
1	USAELRDL Liaison Officer U.S. Army Tank-Automotive Center Warren, Michigan 48090
1	Marine Corps Liaison Office SELRA/LNR, USAELRDL
2	USACDC Liaison Office SELRA/LNF, USAELRDL
1	Commanding Officer USA Security Agency Processing Center Vint Hill Farms Station Warrenton, Virginia 22186
1	Mr. A. H. Young Semiconductor Group Code 681A1A Bureau of Ships Department of the Navy Washington 25, D. C.
2	Chief, Technical Information Division, Hq, USAELRDL
1	USAELRDL Technical Documents Center, SELRA/ADT, Hexagon
1	Director, Electronic Components Department, USAELRDL
1	Director, Solid State and Frequency Control Division, EC Department
1	Deputy Director, Solid State & Frequency Control Div., EC Department

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
1	USAELRDA-White Sands Liaison Office SELRA/LNW, USAELRDL
1	AFSC Scientific/Technical Liaison Office SELRA/LNA, USAELRDL
1	Director, USAEGIMRADA Attn: ENGGM-SS Fort Belvoir, Virginia
5	Chief, Microwave & Quantum Electronics Br., Solid State & Frequency Control Division
1	Chief Scientist U. S. Army Electronics Command Attn: AMSEL-SC Fort Monmouth, New Jersey
5	Chief, Technical Staff, Solid State & Frequency Control Division
5	Chief, Piezoelectric Crystal & Circuitry Br, Solid State & Frequency Control Div.
50	Chief, Semiconductor & Microelectronics Br., Solid State & Frequency Control Division
1	Records Holding Area SELRA/ADO-RHA, USAELRDL

Army-Ft Monmouth, NJ-MON 1709-64