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DELAY LINE TIME COMPRESSOR WOX-3A

16 APRIL 1964

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UNITED STATES NAVAL ORDNANCE LABORATORY, WHITE OAK, MARYLAND

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DELAY LINE TIME COMPRESSOR WOX-3A

Prepared by:

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Approved by: _____
Chief, Acoustics Division

ABSTRACT: This report describes in some detail the fully transistorized WOX-3A Delay Line Time Compressor (Deltic). The bit rate is 10 megacycles. This equipment has proven to be very reliable in daily operation. The transistorization has greatly reduced the power required relative to a comparable vacuum tube model.

Since the principles of Deltic operation have been presented fully in earlier reports only a short description of basic principles is given. Instead, the details of circuit operation are briefly treated. Block diagrams, schematics, and photographs showing component layouts are included. Photographs are shown of typical waveforms at various points within the system, and these are keyed to the block diagrams and schematics. All diagrams are grouped at the end of the report to facilitate use in troubleshooting.

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This report presents the design and operation of a digital transistorized circulating memory, commonly called a DELTIC. The work on this task was funded under Task No. RUDC-3B-000-902, Signal Processing. The report will be of interest to anyone concerned with processing acoustic signals in real time.

R. E. ODENING
Captain, USN
Commander

Z. I. SLAWSKY
By direction

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ILLUSTRATIONS

1. INTRODUCTION

1.1 The Delay Line Time Compressor (deltic), originally conceived by V. C. Anderson, has proven to be a very useful and versatile signal processing tool. The early models[1,2] proved that deltics with 10 megacycle bit rates could provide reliable operation in day-to-day service. The desire for even greater reliability with considerably reduced power requirements and physical size led to the transistorization of the deltic by a joint team from the Research and Engineering areas at the Naval Ordnance Laboratory. Since the requirements of the two areas were slightly different, two equipments evolved which were different in some details (e.g., control signal outputs to auxiliary equipment). This report describes the Research area equipment, which has been designated the Delay Line Time Compressor WOX-3A. A good part of the early transistorization work is described in references 3 and 4. The Engineering area equipment is described in reference 5.

1.2 References 1 and 2 present a full discussion of various methods of time compression and a comprehensive description of deltic philosophy and overall design consideration. Familiarity with these two reports will be assumed, and only a brief description of deltic philosophy will be given herein (see Section 2). This report contains system block diagrams, detailed schematics, verbal descriptions of the major component parts, and photographs of both the equipment and waveforms at various points in the system. The purpose of this report is to document the WOX-3A in such a way that it will be useful for maintenance and troubleshooting, and will be sufficient to

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[1] V. C. Anderson, "The Deltic Correlator", Technical Memorandum No. 37, Acoustics Research Laboratory, Harvard University, 5 January 1956.

[2] J. C. Munson and L. E. Barton, "Delay Line Time Compressor XT-1A", NAVORD 4244, 6 September 1956.

[3] H. R. Irons, "Transistor Circuits for a 10 mc Per Second Delay Line Time Compressor (Deltic)", Internal Memorandum, 13 May 1959.

[4] J. L. Evans, "Development of Wideband 60 mc Transistor Amplifier for Use in Deltic", Internal Memorandum, 7 February 1958.

[5] R. D. Hott, "Transistorized Deltic Correlator System", Internal Memorandum, (In preparation).

allow reproduction of the equipment. It should also provide guidance for the circuit modifications which would be required to convert the WOX-3A from one use to another.

2. BASIC PRINCIPLES OF DELTIC OPERATION

2.1 Moving Time Series (MTS)

The Delay Line Time Compressor (deltic) stores single bit samples of a signal under study (e.g., polarity) in a circulating memory. Let the time width of a single circulating sample inside the deltic be Δ. Then if the time between taking samples, T, is Δ longer than the length of the circulating loop, successive samples lie next to each other in the memory loop. The oldest pulse in the loop is dropped at the same time that the newest one is entered. This type of loop is called a Moving Time Series (MTS) because the most recent T/Δ samples become available at the loop output each period T, and in the proper relative sequence. This permits T/Δ operations to be performed on the stored data while still processing all of the samples, so that the so-called "time compression ratio" is T/Δ. If more than single bit characterization of the signal is desired (e.g., amplitude), then several deltics might be used in parallel, with each deltic containing one bit (e.g., 4 deltics would be required to store 8 amplitude levels plus sign).

2.2 Stationary Time Series (STS)

The entire content of a Moving Time Series can be transferred into a loop of length T during a single circulation time by opening the sample gate of the second loop for the period T. This signal is then allowed to circulate without changing any stored samples until the entire content of the second loop is changed on command. Such a loop is called a Stationary Time Series (STS) because the same pulse sequence is repeated at the output of the loop each period T with a constant time relationship to the time of sampling until such time as the contents of the STS are changed. The interval between successive transfer of samples into the STS is usually chosen to be T^2/Δ, since that is just the time period required for the MTS to replace all of its old samples with new ones. For this case the STS handles each sample only once, but all of the data are processed.

2.3 Correlator

In many cases it is desired to produce either the autocorrelation function of a signal under study or the cross-correlation function between two signals. Normally the

polarity-coincidence correlation function $R(\tau)$ is perfectly satisfactory, where $R(\tau)$ is defined as the percent agreements in polarity minus the percent disagreements in polarity for a time displacement of τ. $R(\tau)$ can be generated by comparing the output of an MTS with that of an STS.

The relative time delays between the MTS and STS which are necessary in order to produce the correlation function are generated as a result of the difference in loop circulation time, Δ, between the two types of Time Series. During the period T immediately after loading the STS from an appropriate MTS, the two loops contain polarity information regarding their respective input signals with a given time displacement τ_o (the exact value of which depends on several factors). This relative time displacement remains the same during the period T, so that a sample-by-sample comparison of the outputs of the two loops can be used to define the polarity-coincidence correlation coefficient for that time displacement based on the T/Δ stored samples. During the next period T the output of the MTS will be advanced by Δ with respect to the STS. Thus the two time series will be displaced by one additional sample, which is equivalent to delaying the input to the STS by one sample period T. A comparison of the outputs of the two loops over the second period T then defines the polarity-coincidence correlation coefficient for a delay of $\tau_o + T$. Similarly, comparison during the n^{th} period T after loading the STS will define the correlation coefficient for a delay of $\tau_o + (n-1)T$. Each point on the correlogram generated in this manner is based on T/Δ samples (or a period of T^2/Δ in the original time base). T/Δ points can be plotted and still process all of the data taken.

The degradation in gain due to clipping and sampling depends upon the statistical properties and spectra of the inputs. If the inputs have flat low pass spectra to f_c with Gaussian distributions of amplitudes, however, the degradation is less than 1.5 db referred to the input for sampling rates greater than $3f_c$, decreasing to 0.92 db for infinite sampling rates.[6]

3. WOX-3A

3.1 General Remarks

The sampling interval was chosen because of certain applications requirement equal to 52.0 μs, which provides reasonably

[6] J. C. Munson, "Certain Aspects of the Peformance of Memoryless Nonlinear Systems", NOLTR 62-201, 28 November 1962. See Example 5.3, pp 61-66.

adequate sampling for inputs with low pass bandwidths up to 6.4 kc. All timing in the system is based on the interval between samples, and in order to simplify the control circuits all time intervals are binarily related to that interval. The number of samples in an STS was chosen as $\frac{T}{\Delta} = 2^9 = 512$ pulses. The bit rate in the system, $\frac{1}{\Delta}$, then is $\frac{512}{52\mu s} \approx 9.846$ mc. The interval between successive transfers of samples into the STS if selectable as either $\frac{T2}{\Delta} = 26{,}624$ μs or as $4\frac{T2}{\Delta}$. The effective integration time of the correlator is 26,624 μs. The transfer pulse is 52.0 μs long, and the sample pulse 0.10 μs long.

A number of measures have been taken in order to maximize system reliability. Saturated logic circuits have been used in all gating and control areas. Silvered copper grounding strips have been incorporated into each circuit board. The length of connecting wires between boards has been minimized, the impedance levels have been kept low, and properly terminated coaxial cable has been used where pulses with very fast rise times are present. While the circuits have been designed to perform well over a range of D.C. supply voltages, nevertheless all power supplies are regulated. All outputs to auxiliary equipment external to the WOX-3A are buffered.

Block diagrams of the various deltic components are given in Figures 1-4. Figure 5 shows a front view photograph of the equipment. Figures 6-17 are schematics and photographs of the various deltic components. Figure 18 shows the pin connections in the rack. Figures 19-41 are photographs of the waveforms at various locations within the equipment.

3.2 Deltic Loop

A block diagram of the deltic circulating loop is given in Figure 1. This diagram is equally applicable to the MTS and the STS. Each circulated sample is clocked and shaped before insertion into the delay line. This corrects for errors in loop circulation time and for pulse shape degradation as the samples pass around the loop. The clocking signal is a series of very narrow pulses with a repetition rate of $\frac{1}{\Delta}$. The sample and clocking pulse signals are fed to a saturable gate which generates a standard pulse at the clock time if the sample signal exceeds a certain value at that time. If it is less than that value no pulse is generated. The delay line is glass with a 40 mc center frequency and about a 10 mc bandwidth at the 3 db down points. The MTS and STS lines are 51.72

and 51.82 μs respectively. The delay sensitivity with temperatures is about 25 parts per million per °C. A ±20°C change would then result in only ±0.25 bit change in delay line length, so that a fixed oscillator frequency is permissible. Each rf amplifier stage is transformer coupled with tuned secondary, and has a 3 db bandwidth of 15 mc. The three stage amplifier is synchronously tuned and has an overall bandwidth of about 12 mc. The full wave detector drives a vernier delay line which is adjusted to bring the recirculated pulse to the reclocking gate so that it will be centered on the reclocking signal, thus providing maximum circulation stability. The drop gate is normally open and the add gate normally closed, so that recirculated samples normally reach the reclocking gate. When new samples are introduced, the add gate is opened and the drop gate simultaneously closed until the proper number of samples have been inserted. The symmetrical construction of the add-drop gate pair and the location of the output to the STS makes it possible to connect the input to the STS directly to the output of the MTS with no interloop delay adjustment necessary.

A schematic of the deltic loop is given in Figure 6, while a photograph of the chassis is given in Figure 7. Photographs of waveforms at the locations indicated by the circled letters on both the schematic and block diagrams are given in Figures 19 to 31.

3.3 Control Circuits

The control circuitry is constructed on two boards. The basic timing interval is generated by a crystal oscillator with a frequency of $\frac{512}{52\mu s}$ = 9,846,154 ±50 cps. The high accuracy is not required by the deltic, but it is needed for certain auxiliary equipment which is sometimes used. The oscillator is located on Timing Board No. 2. Timing Board No. 1 has 20 binaries which divide the 9.8 mc down to 9 cps, with buffered outputs available at various intermediate frequencies. In order to realize maximum reliability with a moderate size, three different types of dividers are used, a very high speed binary to divide the 9.8 mc, high speed binaries to divide from 4.8 mc to 0.3 mc, and medium speed binaries for the rest. Block Diagrams of Timing Boards No. 1 and 2 are given in Figure 2 and 3, respectively. The rough timing for the sample and transfer pulses is obtained from this board, and signals are taken directly from Timing Board No. 1 to the dielectric motor drive and for an oscilloscope trigger. There is space left on the board for buffers if additional outputs are desired. Timing Board No. 2 contains, in addition to the oscillator, the circuitry for generating the sample and transfer pulses. Outputs to drive auxiliary equipment are separately buffered to eliminate loading problems.

The output of the 9.846 mc oscillator is shaped in class-C amplifiers to a 14 ns pulse occurring at a 9.846 mc rate. The buffer is capable of generating pulses of 2 volts peak across a 10 Ω load (this is approximately the deltic system load). Normal operating level is about 1 volt, since the deltic system operates best in this range. A photograph of the output waveform is given in Figure 19.

The sample pulse generation is initiated by the 19.2 kc square wave from the divider chain on Timing Board No. 1. Since there may be an intolerable amount of jitter on the 19.2 kc, this is merely used to set a flip flop which is reset by the 2.4 mc from Timing Board No. 1. Since the 2.4 mc is the result of only 2 divisions from the 9.8 mc it is very stable. The reset of the flip flop generates a pulse which is then shaped to be 0.1 μs long by a shorted delay line. The 19.2 kc determines how often this pulse will occur (i.e., every 52 μs), while the 2.4 mc controls the precise timing. The shaped pulse is next delayed such that the final sample pulse has the proper time relationship to the reclock pulse train. The delayed pulse is then put through a phase splitter and buffered to obtain the sample add and drop pulses.

The output then is a simultaneous plus pulse and a minus pulse of 0.1 μs duration each 52.0 μs. The amplitude is about 3.0 volts. Photographs of the output waveforms are given in Figures 20 and 21. The transfer pulse generation is initiated by either a 37 cps or a 9 cps square wave from Timing Board No. 1, the choice depending on the setting of a switch on Timing Board No. 1. The square wave sets a flip flop which is then reset by a delayed sample pulse. The reset time determines the precise timing of the transfer pulse, while the set pulse determines the crude timing (to the nearest 52 μs). Since this is so, the delay for the sample pulse is chosen so that the final transfer pulse has the proper time relationship to the reclock pulse train. The actual transfer pulse is generated by a second flip flop which is set by the reset of the first flip flop and reset by the next sample pulse. The output thus is a 52.0 μs pulse each 26,624 μs or each 106,496 μs. The set and reset outputs of the second flip flop are buffered to act as the transfer add and drop pulses. The amplitude is about 3.0 volts. Photographs of the output waveforms are given in Figures 22 and 23.

The schematic and a photograph of Timing Board No. 1 are given in Figures 8 and 9, respectively, while those for Timing Board No. 2 are given in Figures 10 and 11, respectively.

3.4 Correlator

The polarity coincidence correlation coefficient can be completely determined by measuring either the percent agreements in polarity or the percent disagreements in polarity. In the WOX-3A the disagreements are counted. The output of an MTS is added to the phase inverted output of an STS, and the phase inverted output of the MTS is added to the output of the STS. Assume that the inputs to the adders are either 0 or 1. If the outputs of the MTS and STS agree in polarity then, outputs of both adders will be 1. If the outputs of the MTS and STS disagree in polarity the output of one adder will be 2, while the other will be 0. The outputs of the adders are thresholded (at, for this example 1.5) so that one output line is energized if the MTS and STS disagree in polarity. The threshold outputs are put into an OR circuit so that a 1 output is obtained whenever the MTS and STS disagree in polarity. This output is delayed to put it into the proper time relationship with the reclocking signal. The output is phase split and put into reclocking gates very similar to those used in the deltic loops. One reclocking gate generates a pulse each time the MTS and STS agree in polarity at the reclock time, while the other generates a pulse each time they disagree at the reclock time. The pulses are about 1.0 volt into 100 Ω and are about 14 ns long. These are used by the automatic target tracker and digital post integrator as signal inputs. The disagreement pulses are integrated with an RC product of about 6 μs to give a short time average suitable for display on an oscilloscope or for feeding a dielectric recorder. A block diagram of the correlator is given in Figure 4.

The schematic and a photograph of the correlator are given in Figures 12 and 13, respectively. Photographs of waveforms at the locations indicated by the circled letters on both the schematic and block diagrams are given in Figures 32 to 41.

3.5 Clipper

The clipper which has been used is basically the same as one developed by the Engineering area, and which is described in reference 7. The only changes are the incorporation of an emitter follower input and a small alteration in the output stage. This clipper has rise and fall times of about 0.1 μs, will provide adequate clipping on signals as small as 0.5 mv rms from 25 cps to 25 kc and will handle signals as large as 3 v rms

[7] W. F. Rust, "Preamplifiers and Clippers used in Digital Beam Formers", Internal Memorandum (In preparation).

without zero shift due to overload. The input impedance is approximately 0.1 megohm. A schematic of the clipper is given in Figure 14 and a photograph in Figure 15.

3.6 Rack

All circuits are built on boards which plug into standard 41 pin Elco connectors. These connectors are mounted on the rear of the rack. To increase the reliability of electrical connection and to prevent physical shifting of the boards during shipment, a standard Camloc device is used to lock each board into the rack. Despite these precautions an occasional electrical open circuit occurs. This failure, although infrequent, is the most serious maintenance problem encountered in the WOX-3A. The trouble is confined to the contact between the pins and plug-in connectors. The problem of providing reliable and trouble-free interconnections between various boards should be studied carefully before building another deltic system.

Silvered copper ground bus has been used in the interconnecting wiring on the back of the rack. Coaxial cable has been used for all very fast rise time pulses. A few terminating resistors are located on the back of the rack so that the deltic loop boards can all have identical circuitry.

Front and rear view photographs of the rack are given in Figure 5 and 17, respectively. The rack schematic is given in Figure 16. Pin connections are given in Figure 18.

4. DISCUSSION

4.1 The 10 mc transistorized deltic which has been developed has proven to be very reliable and flexible. It has been used with a variety of peripheral equipment (e.g. dielectric recorder, digital post integrator, automatic tracker). A number of selected buffered clock frequencies are brought out, so that those necessary for the operation of the particular piece of auxiliary equipment either are, or can be made, available.

ACKNOWLEDGEMENTS

The WOX-3A was the result of the efforts of a number of people, both in the Research and Engineering areas of the Laboratory. In particular, T. A. Pendleton designed the rf amplifier, R. D. Hott did much of the general design and the layout of certain critical circuits, and G. W. Cope designed the power supplies.

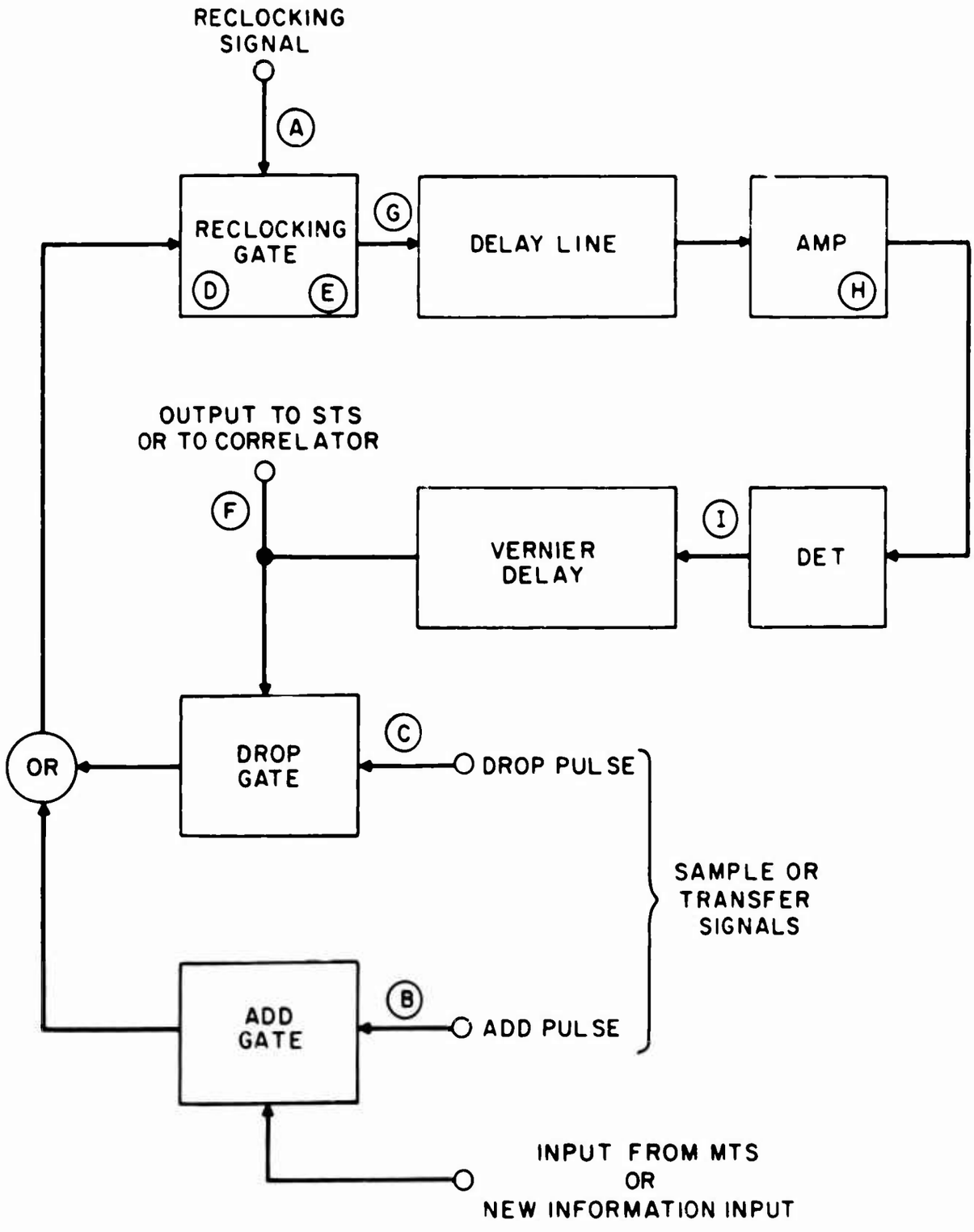


FIG. 1 BLOCK DIAGRAM OF DELTIC LOOP (MTS AND STS)

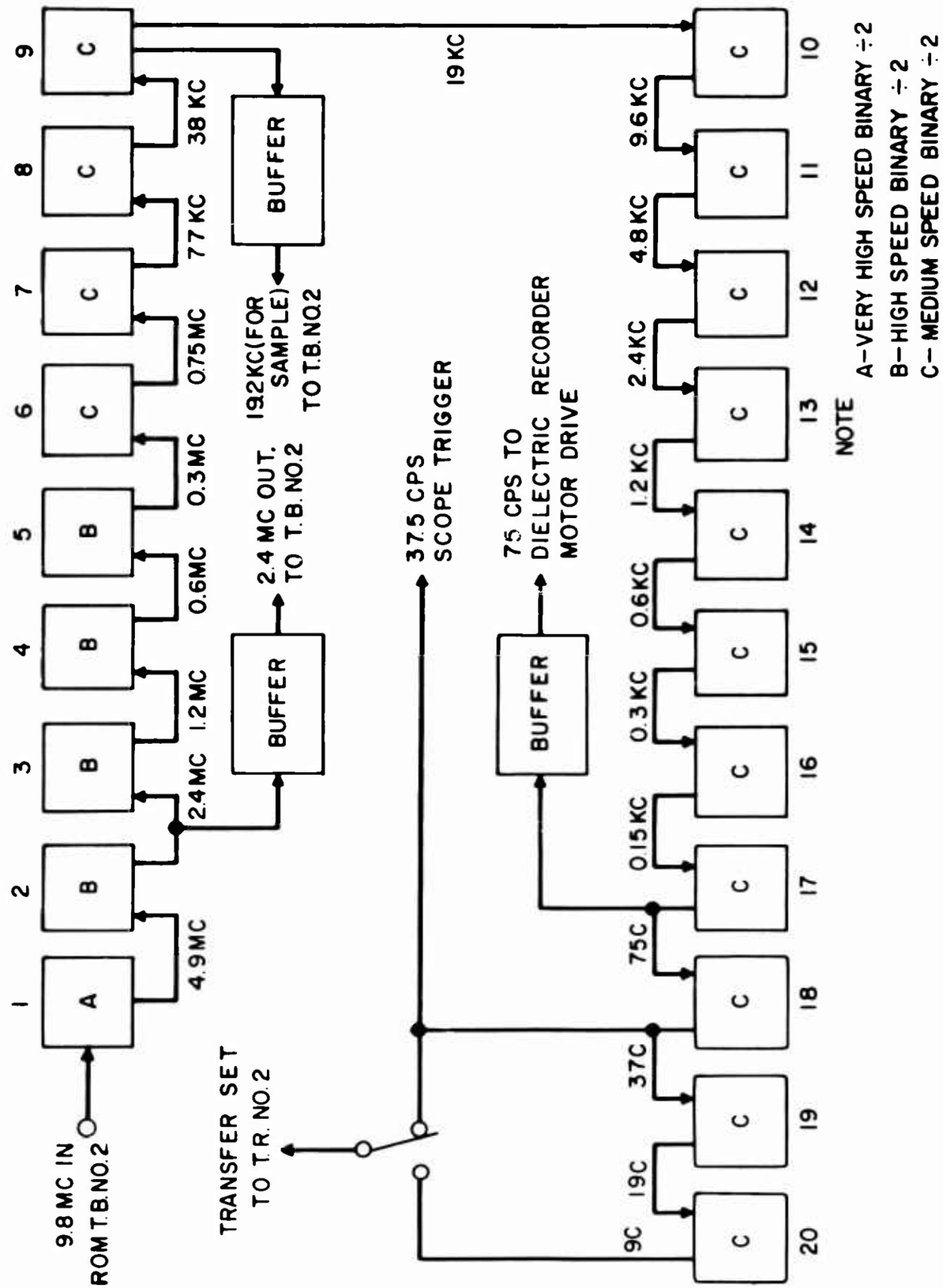


FIG. 2 BLOCK DIAGRAM OF TIMING BOARD NO. 1

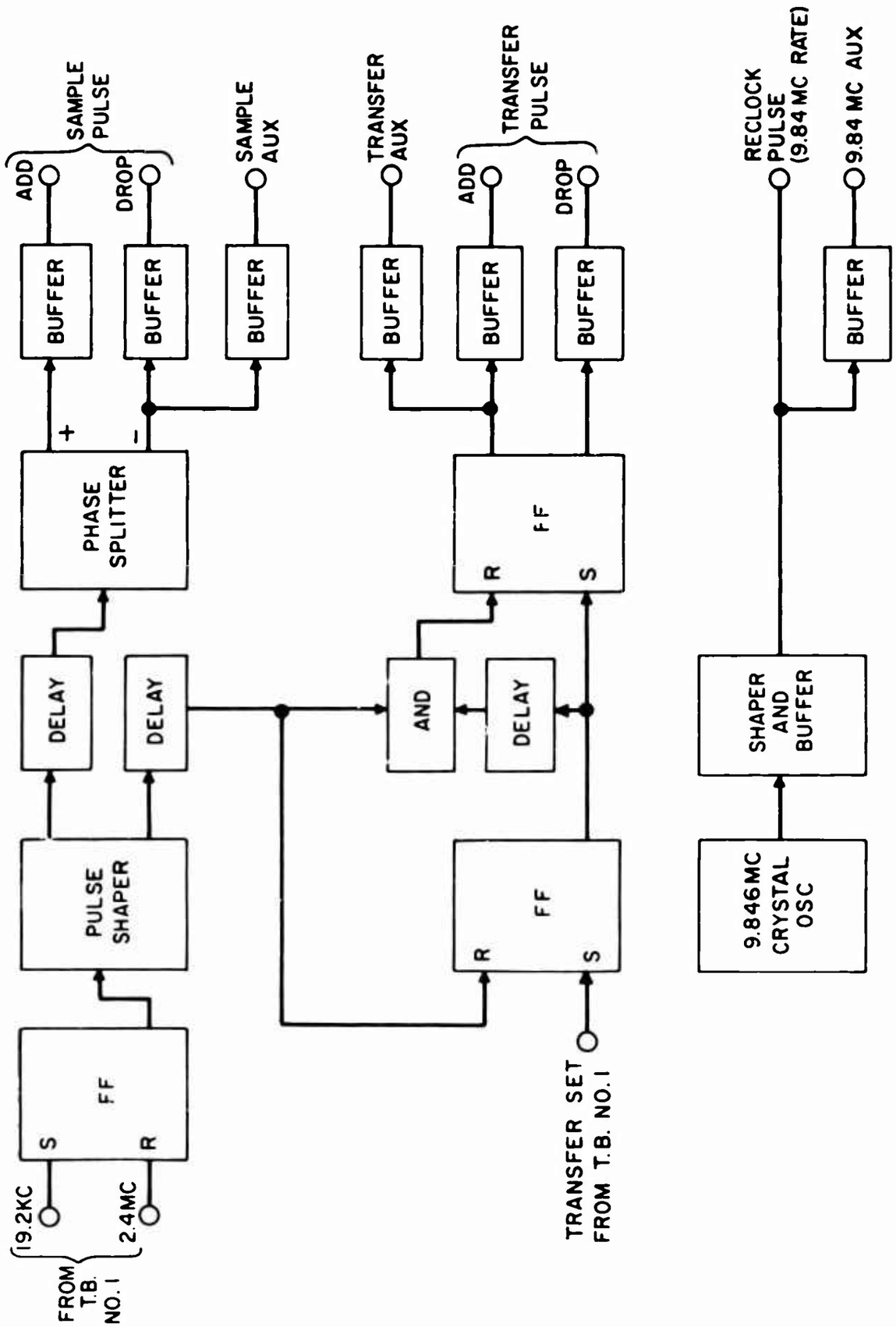
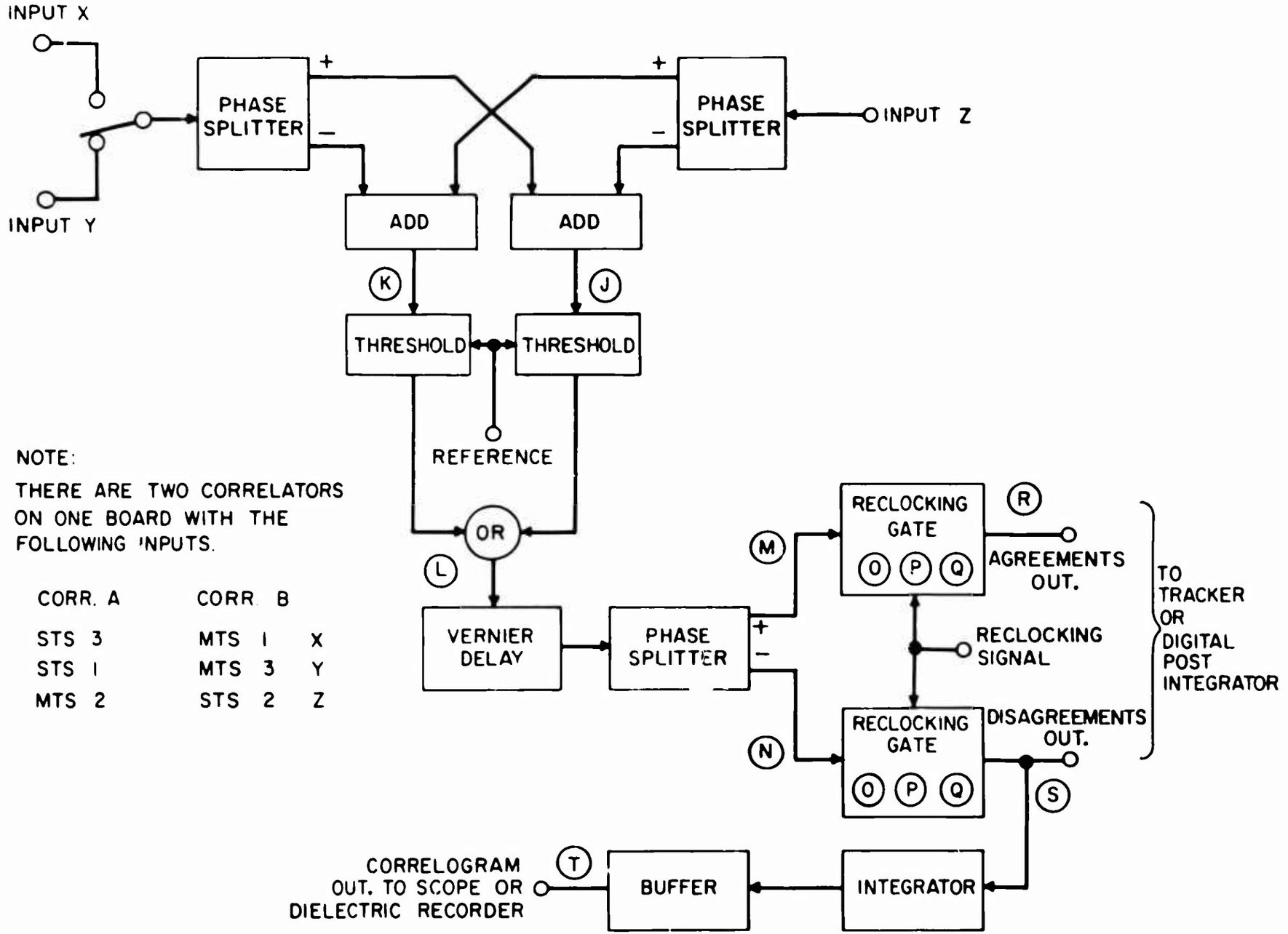


FIG 3 BLOCK DIAGRAM OF TIMING BOARD NO. 2



NOTE:

THERE ARE TWO CORRELATORS ON ONE BOARD WITH THE FOLLOWING INPUTS.

CORR. A	CORR. B	
STS 3	MTS 1	X
STS 1	MTS 3	Y
MTS 2	STS 2	Z

FIG 4 BLOCK DIAGRAM OF CORRELATOR

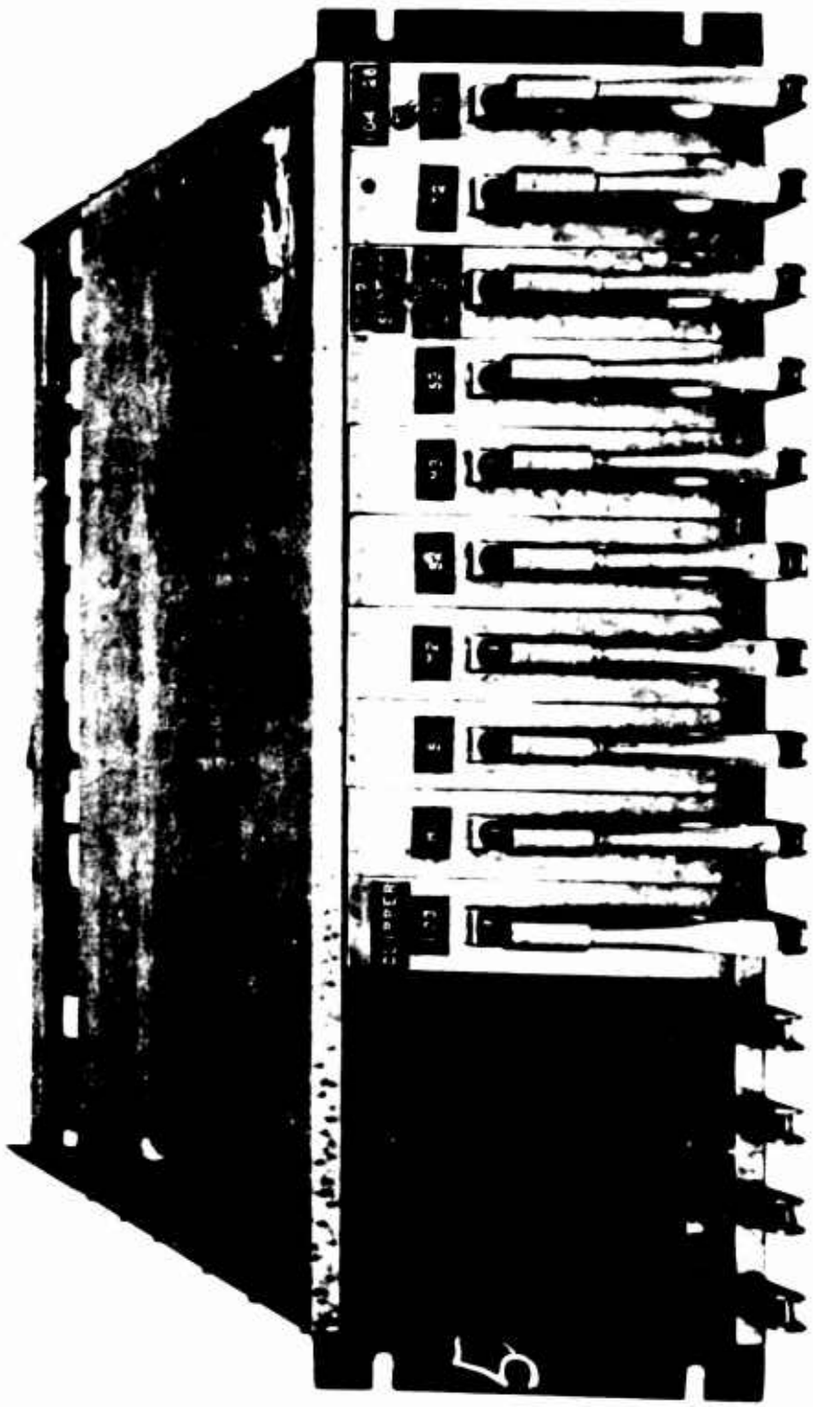


FIG. 5 RACK, FRONT VIEW

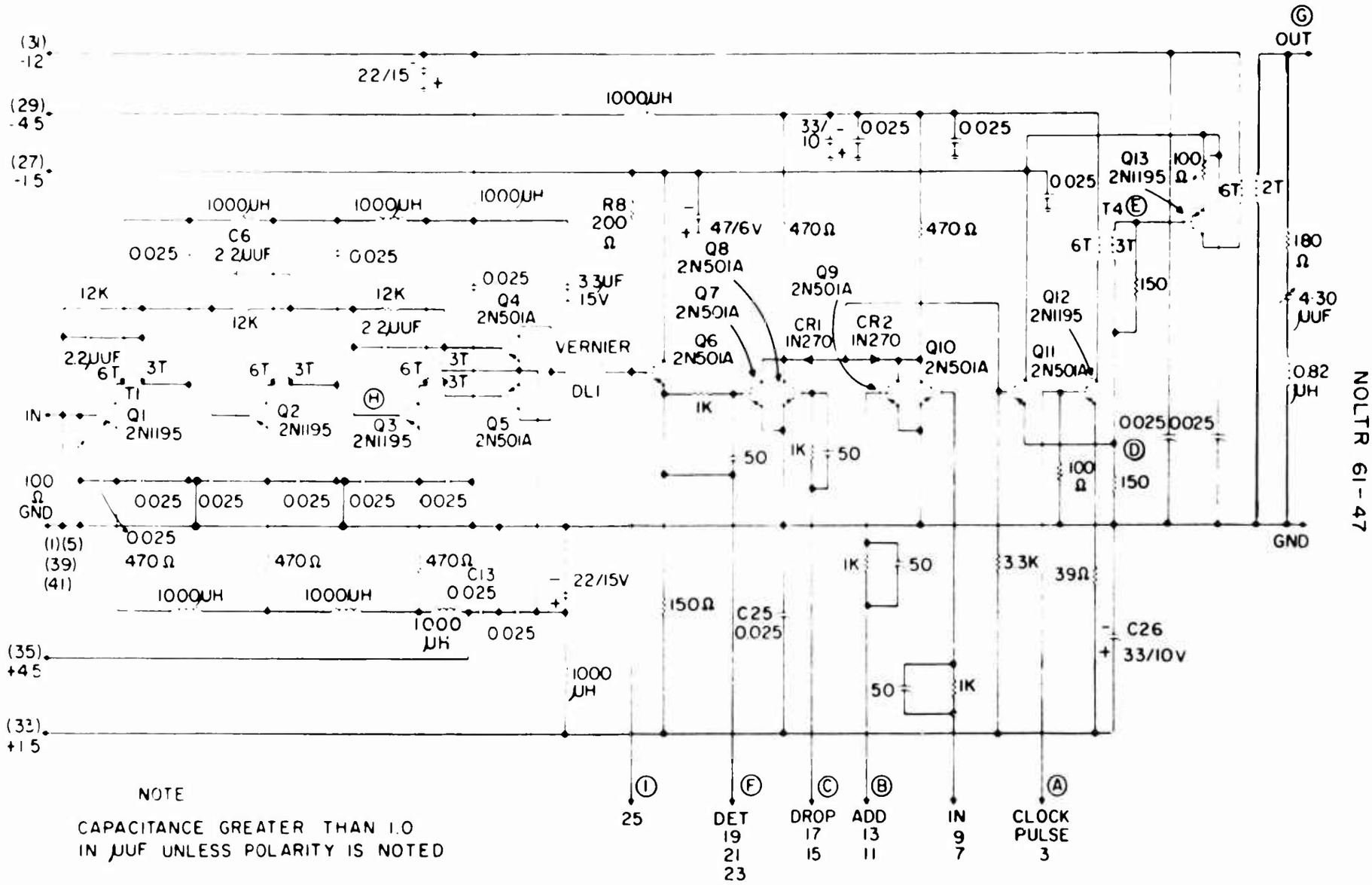


FIG 6 DELTIC LOOP

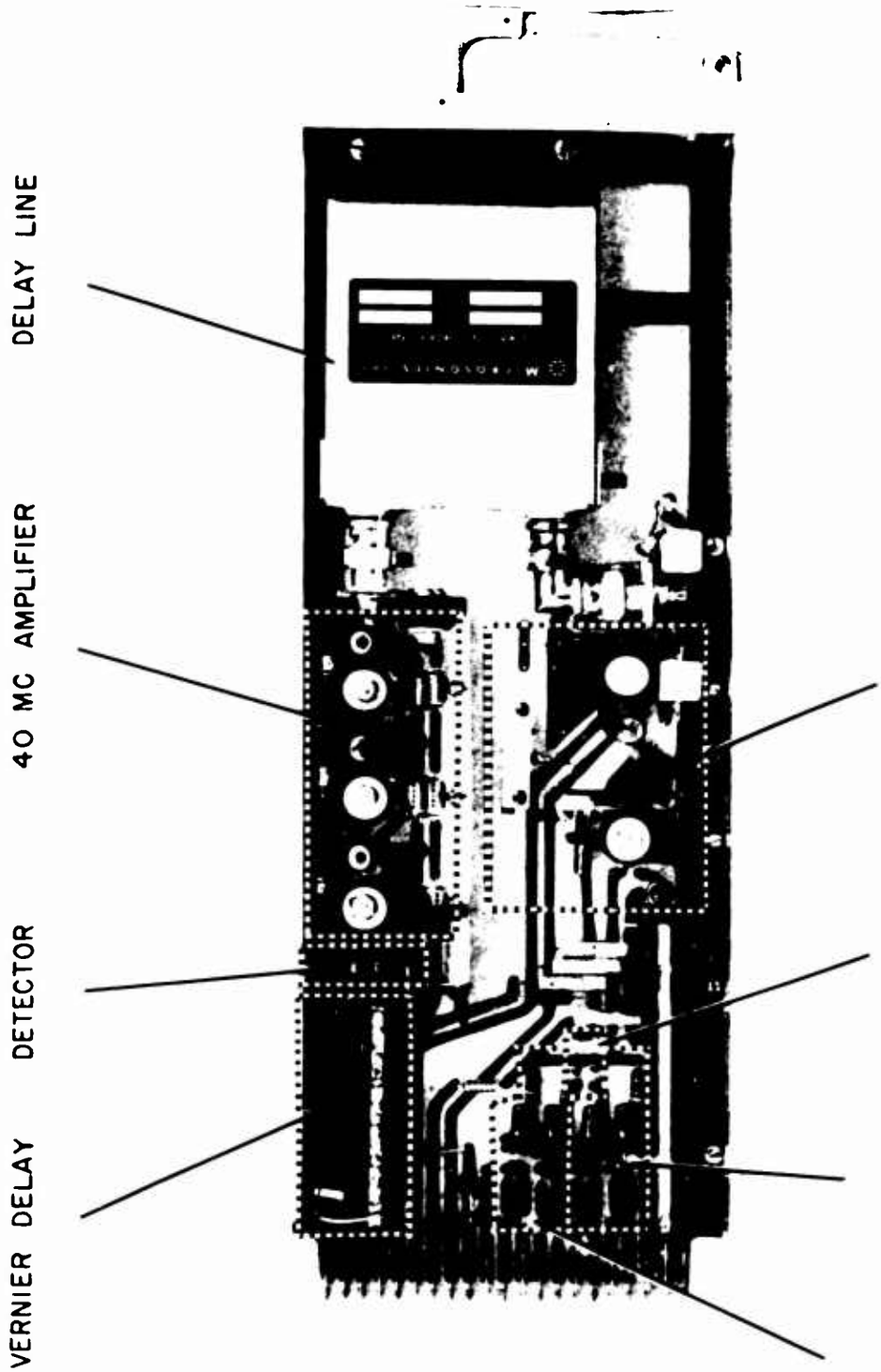


FIG. 7 DELTIC LOOP

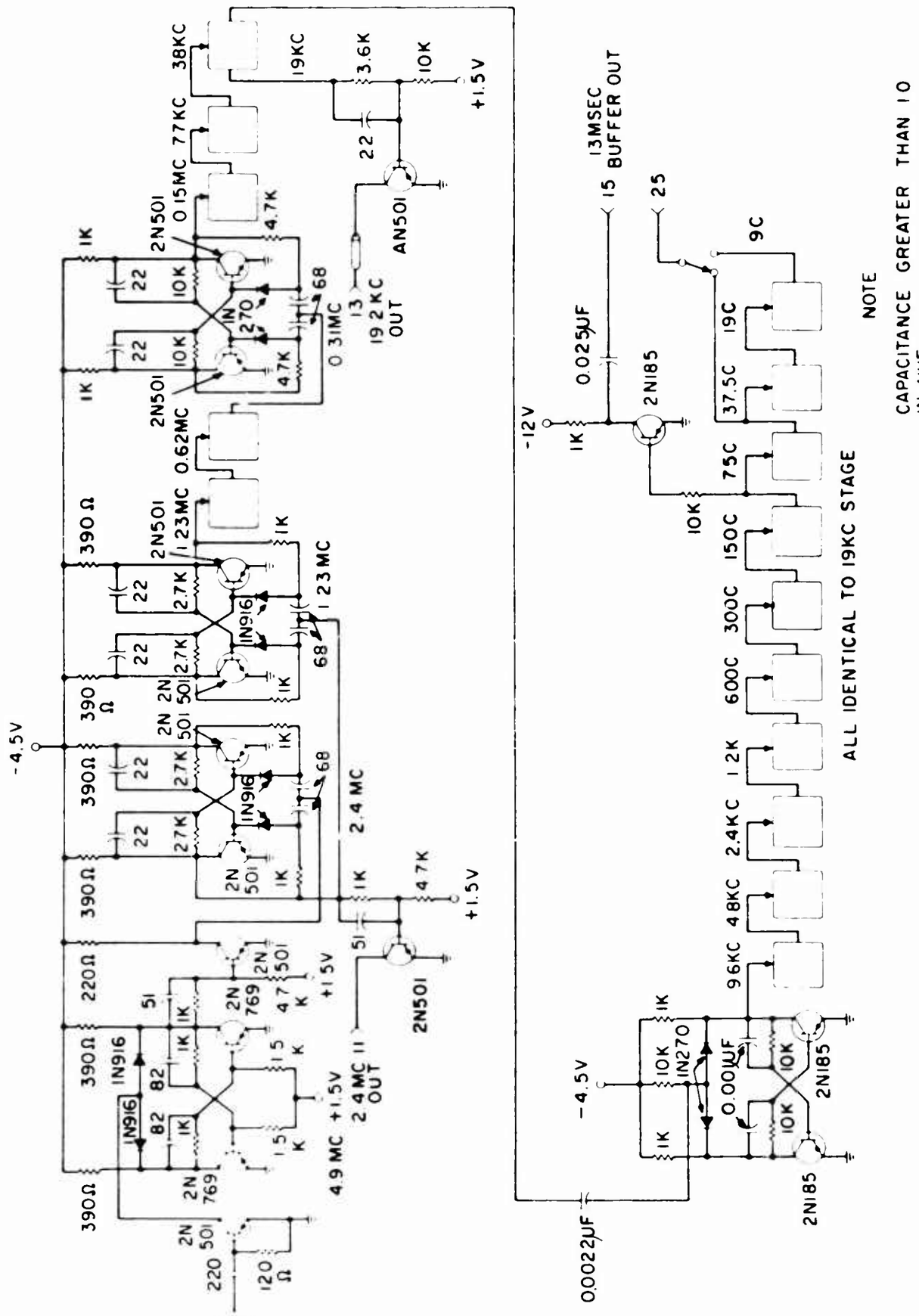


FIG. 8 TIMING BOARD NO. 1

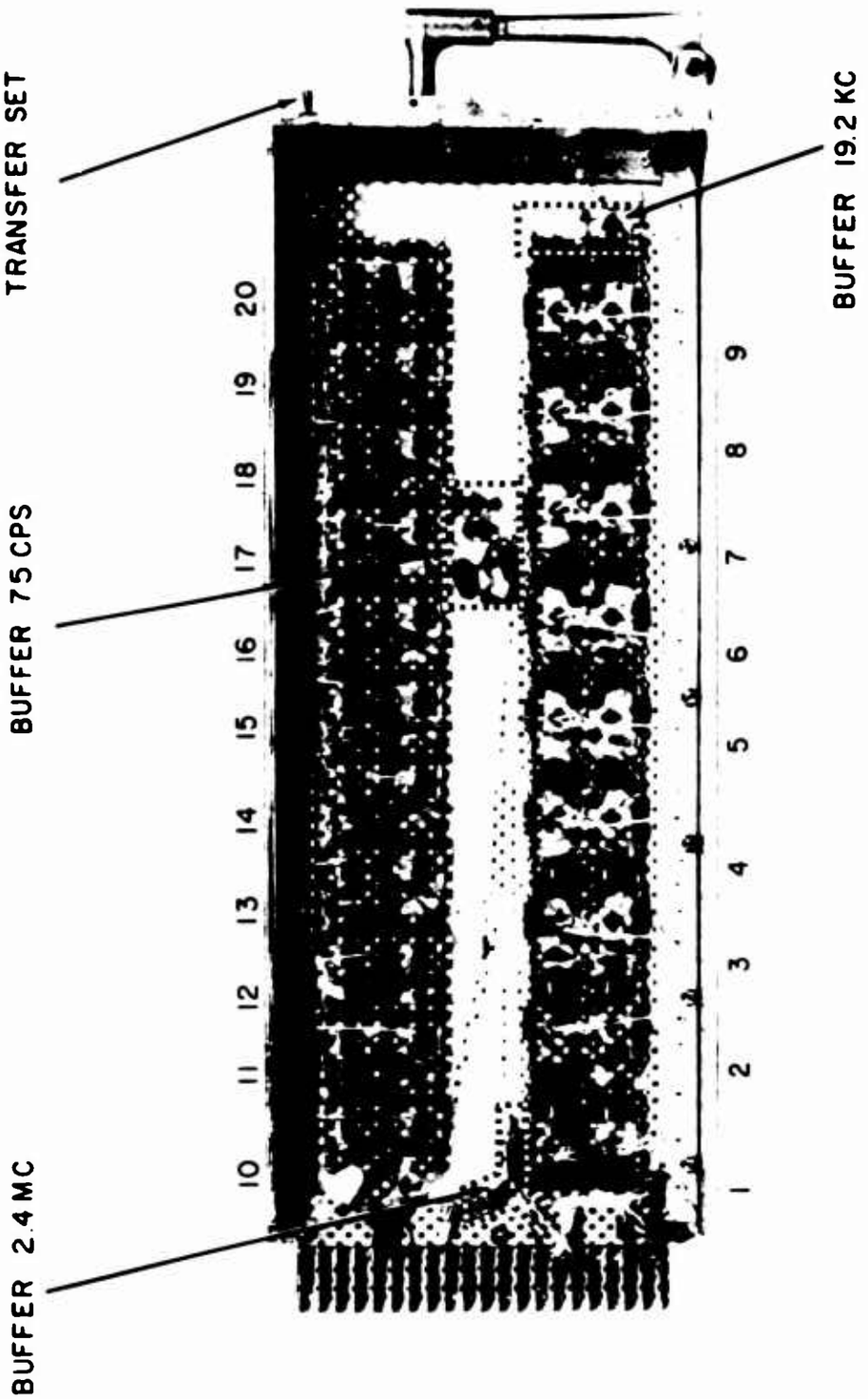


FIG. 9 TIMING BOARD NO. 1

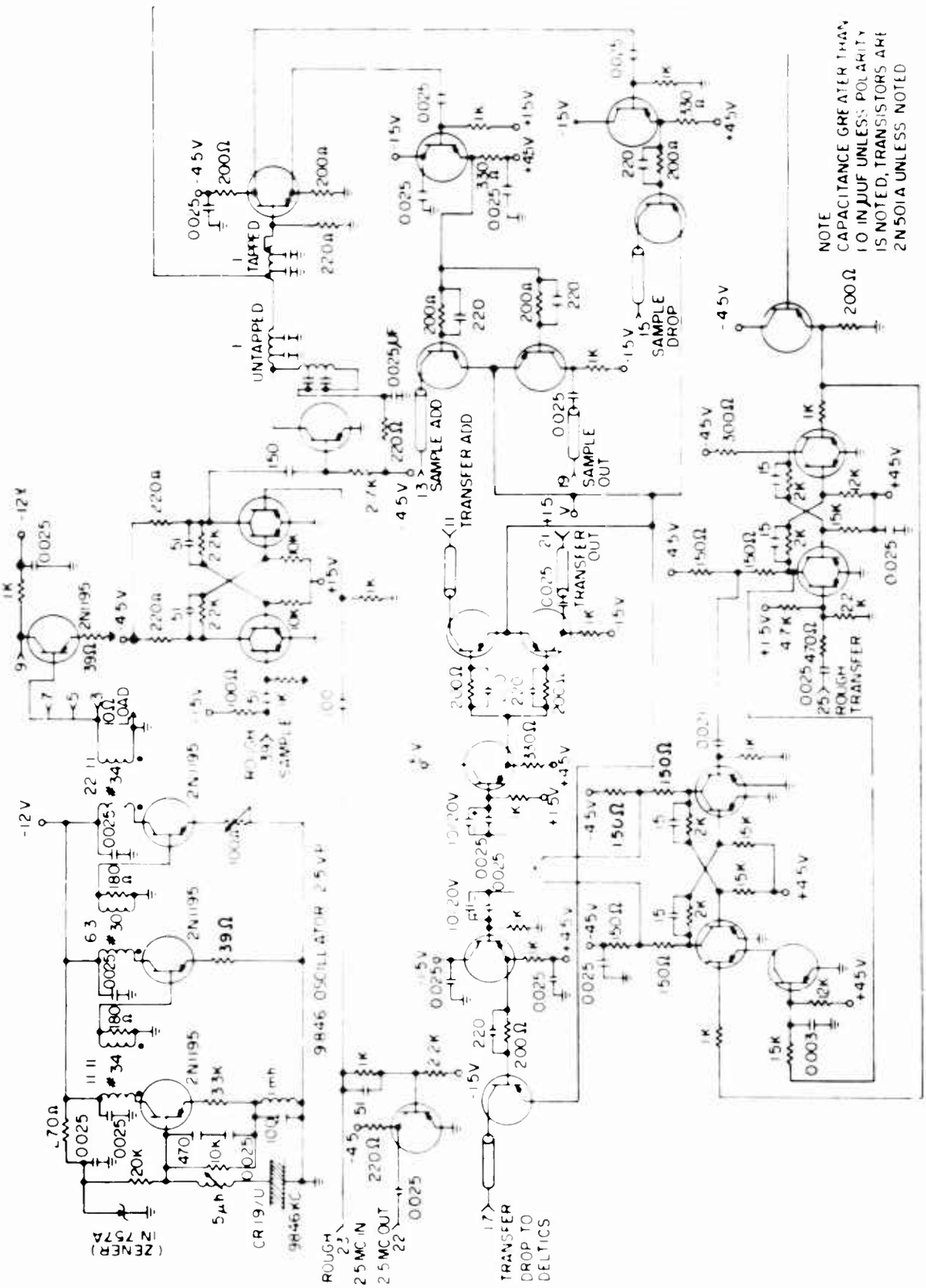


FIG 10 TIMING BOARD NO. 2

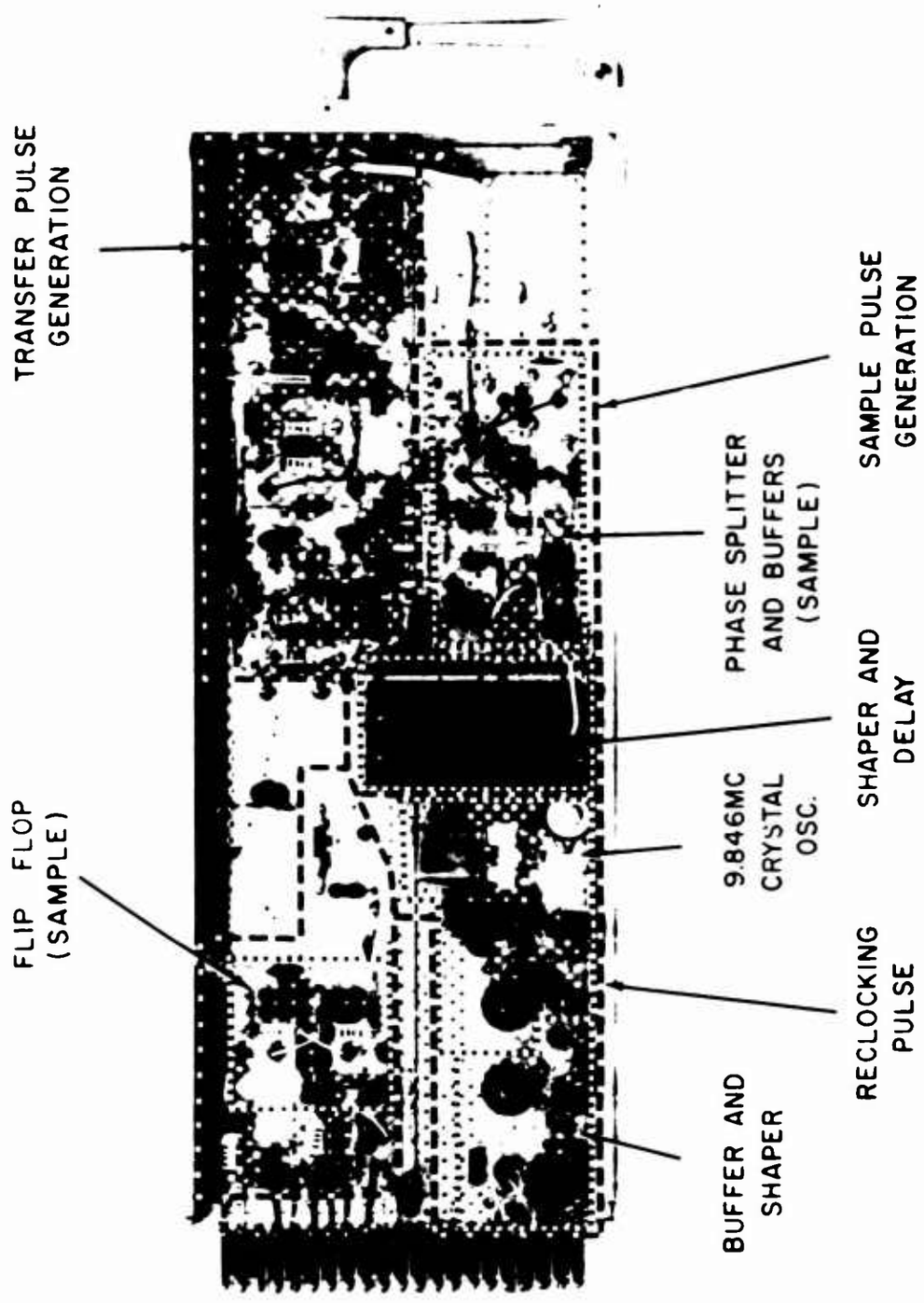


FIG. 11 TIMING BOARD NO. 2

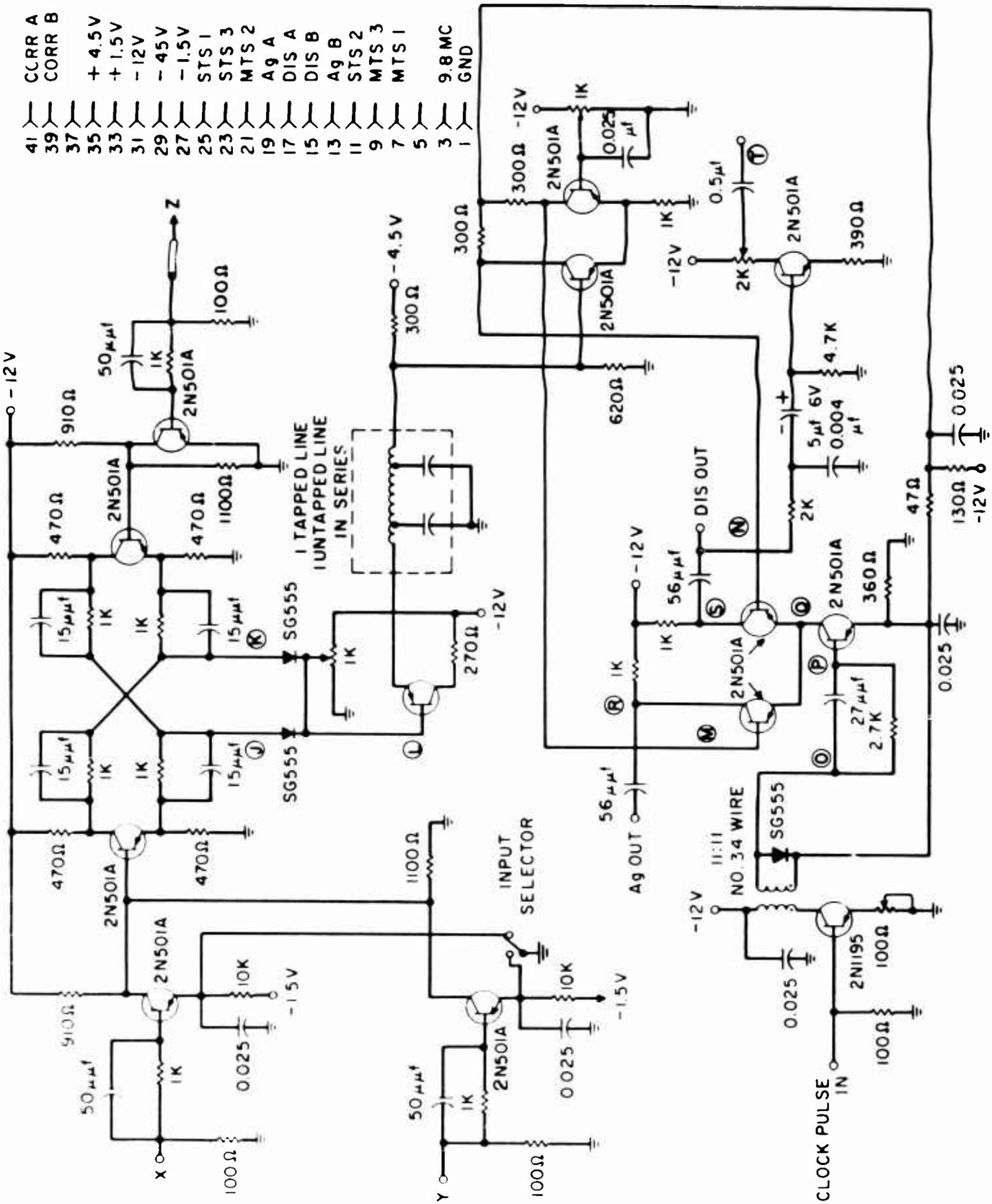


FIG. 12 SINGLE CORRELATOR

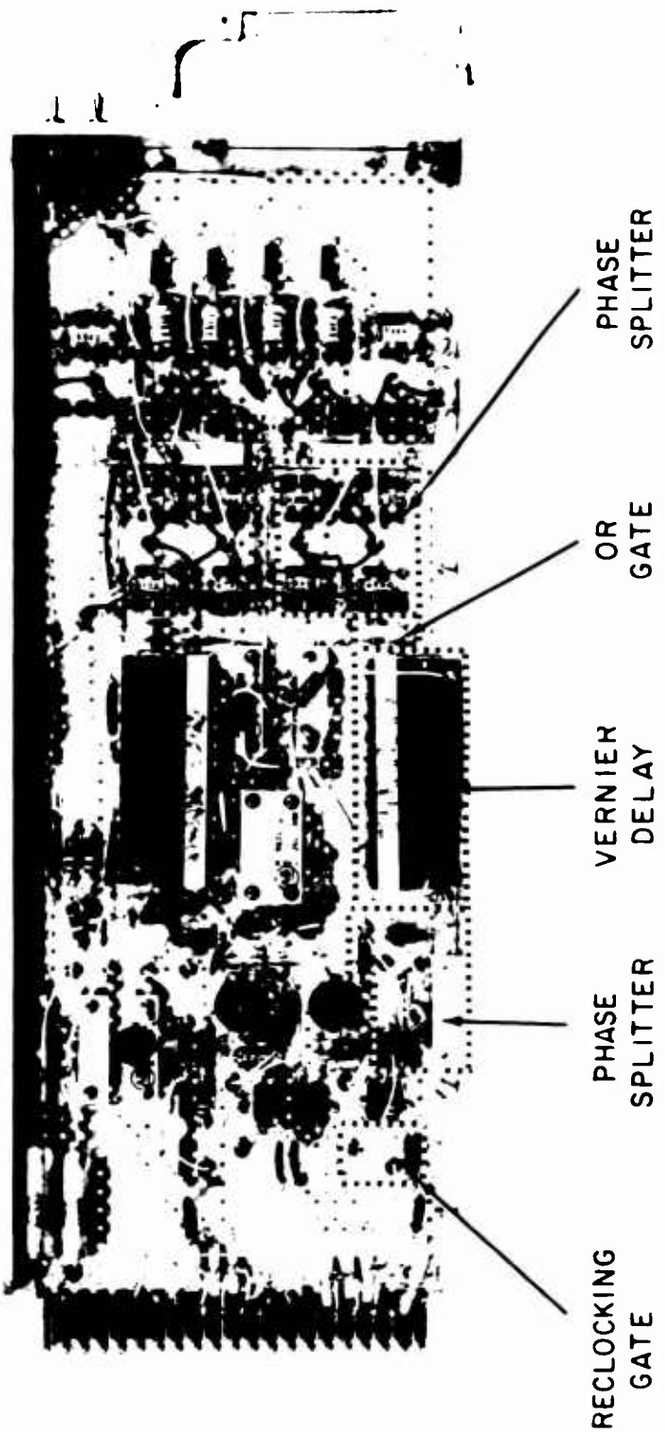
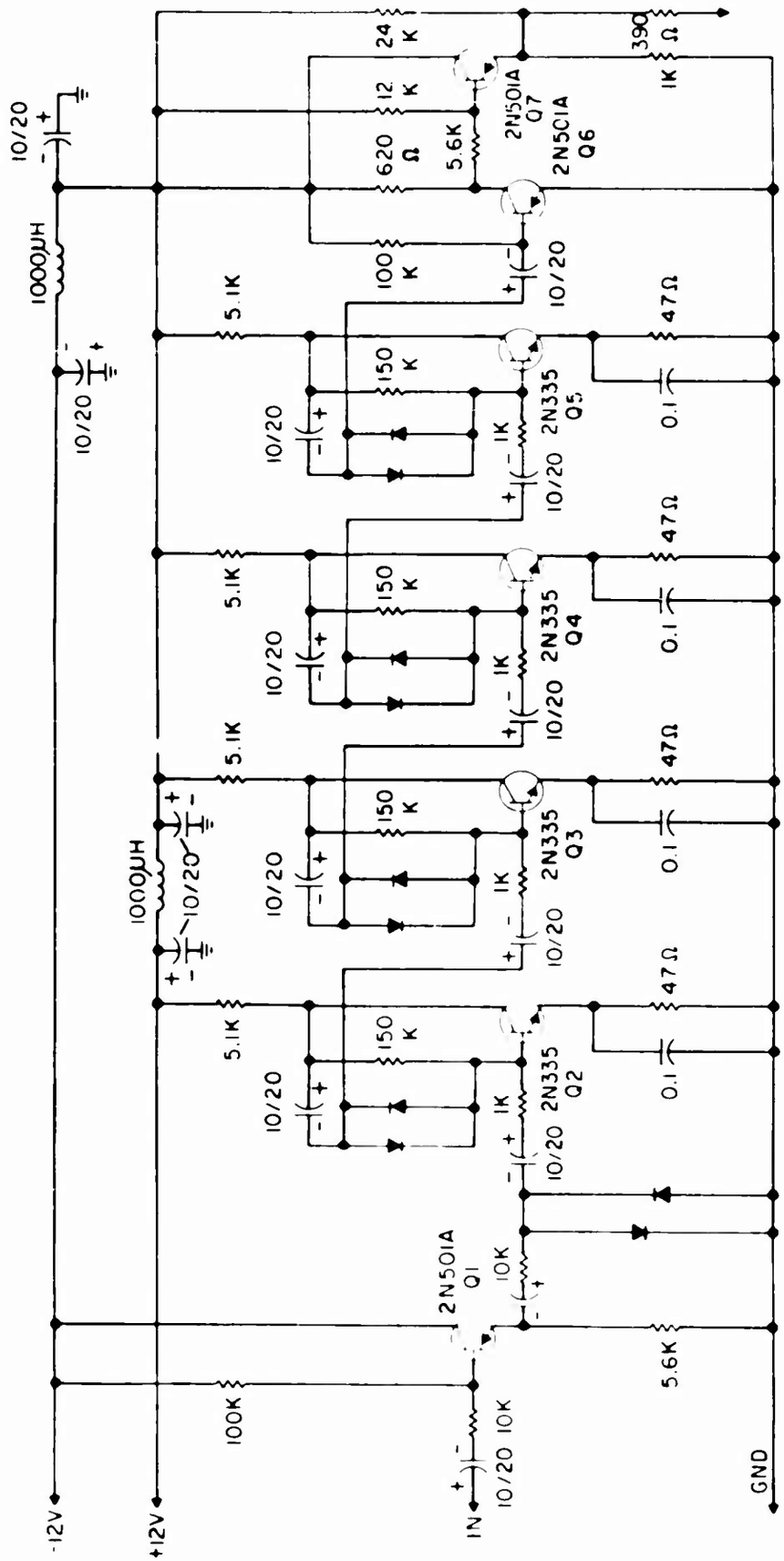


FIG. 13 CORRELATOR



1 ALL DIODES ARE IN625.
2 ALL CAPACITANCE VALUES ARE IN μF

FIG. 14 FEEDBACK CLIPPER

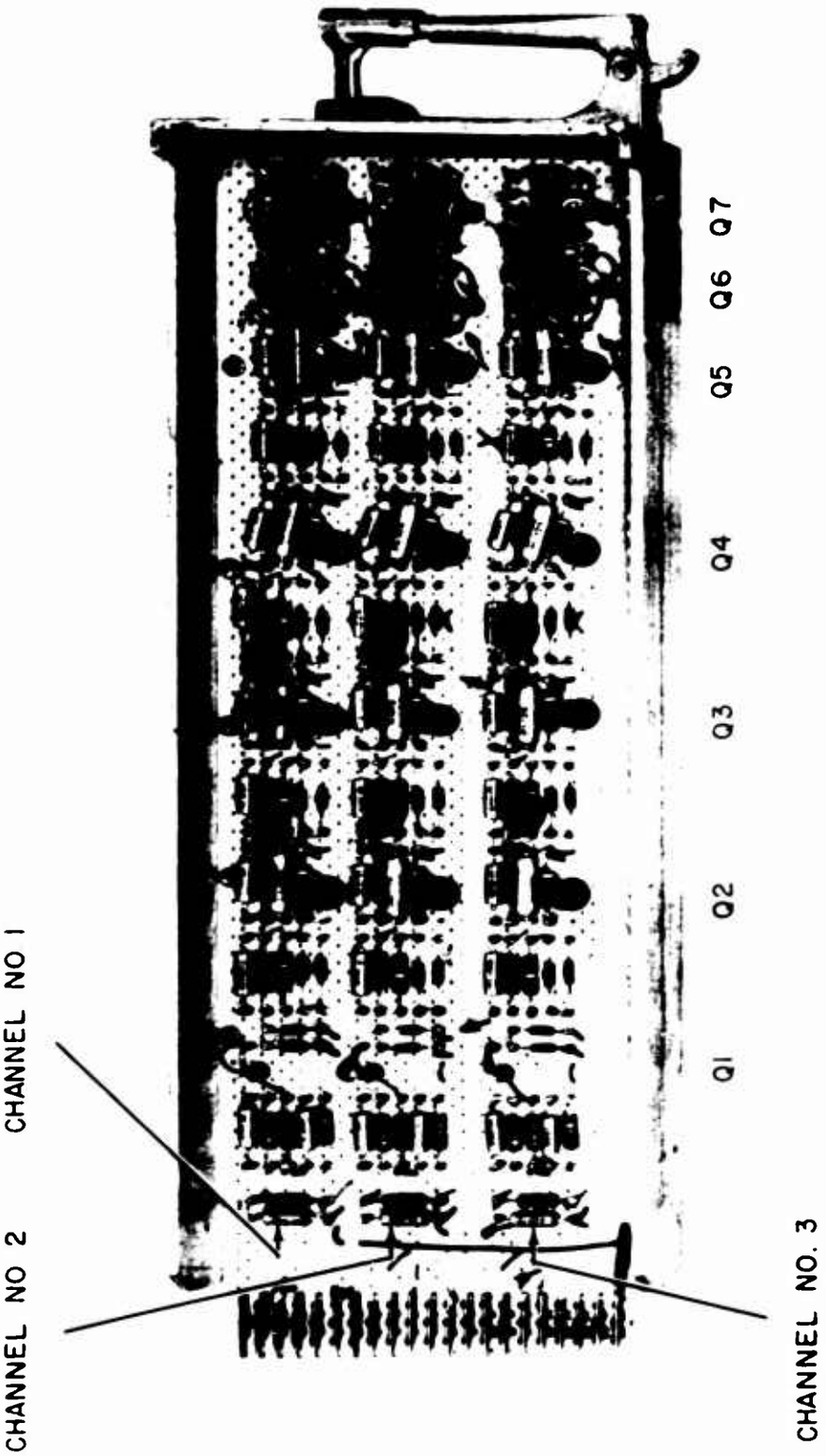


FIG. 15 CLIPPER

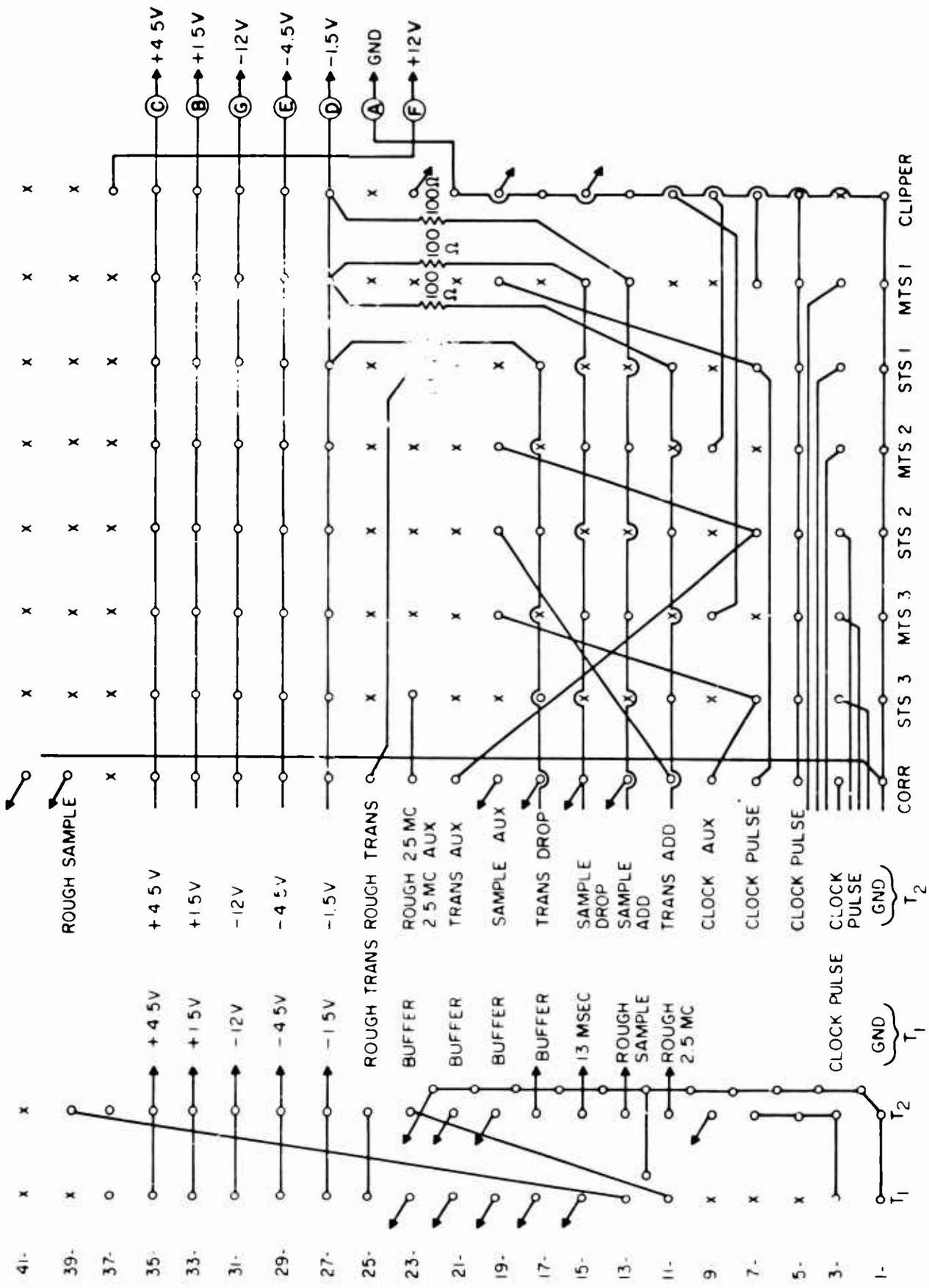


FIG. 16 RACK SCHEMATIC

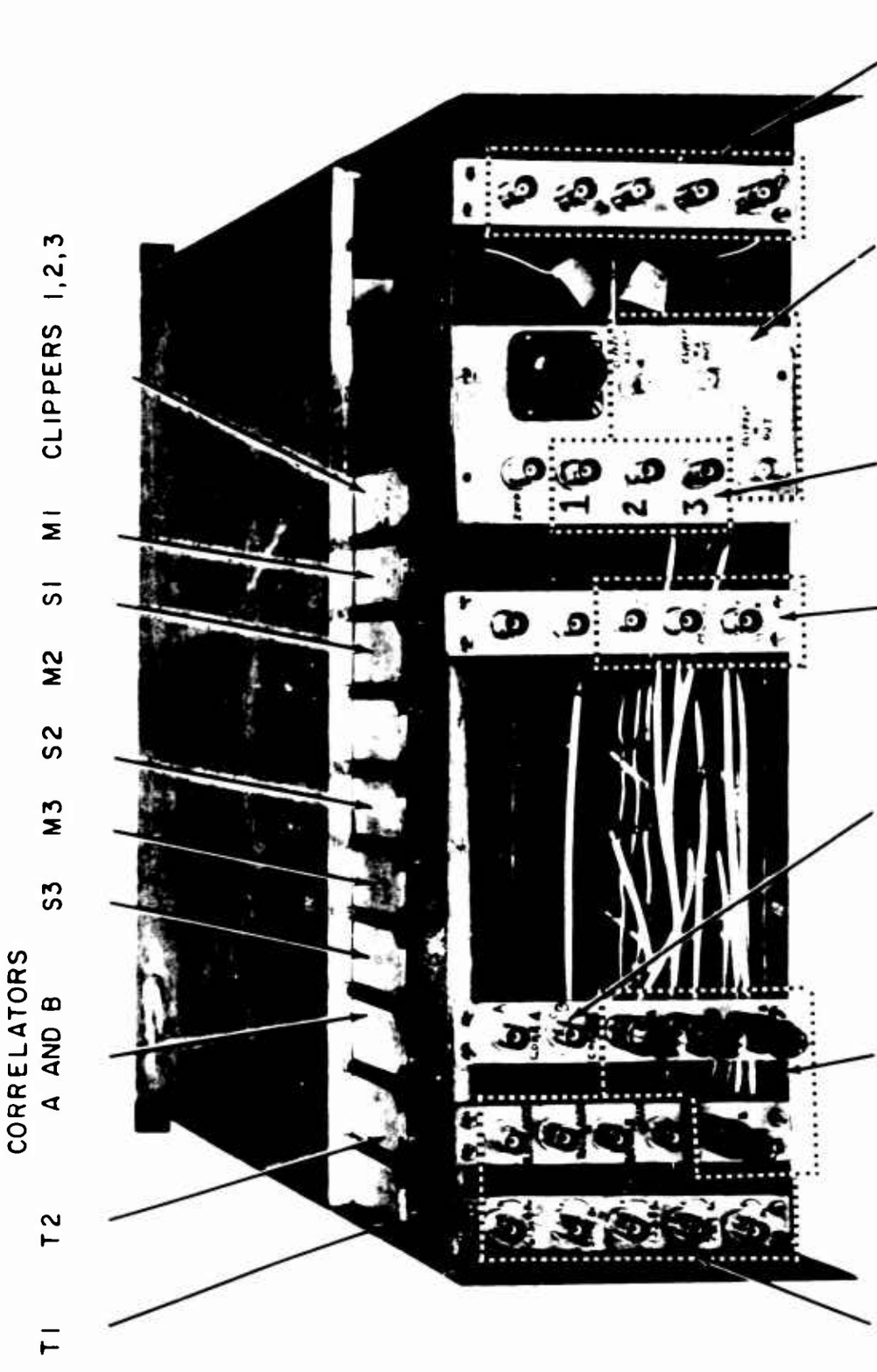


FIG. 17 RACK, REAR VIEW

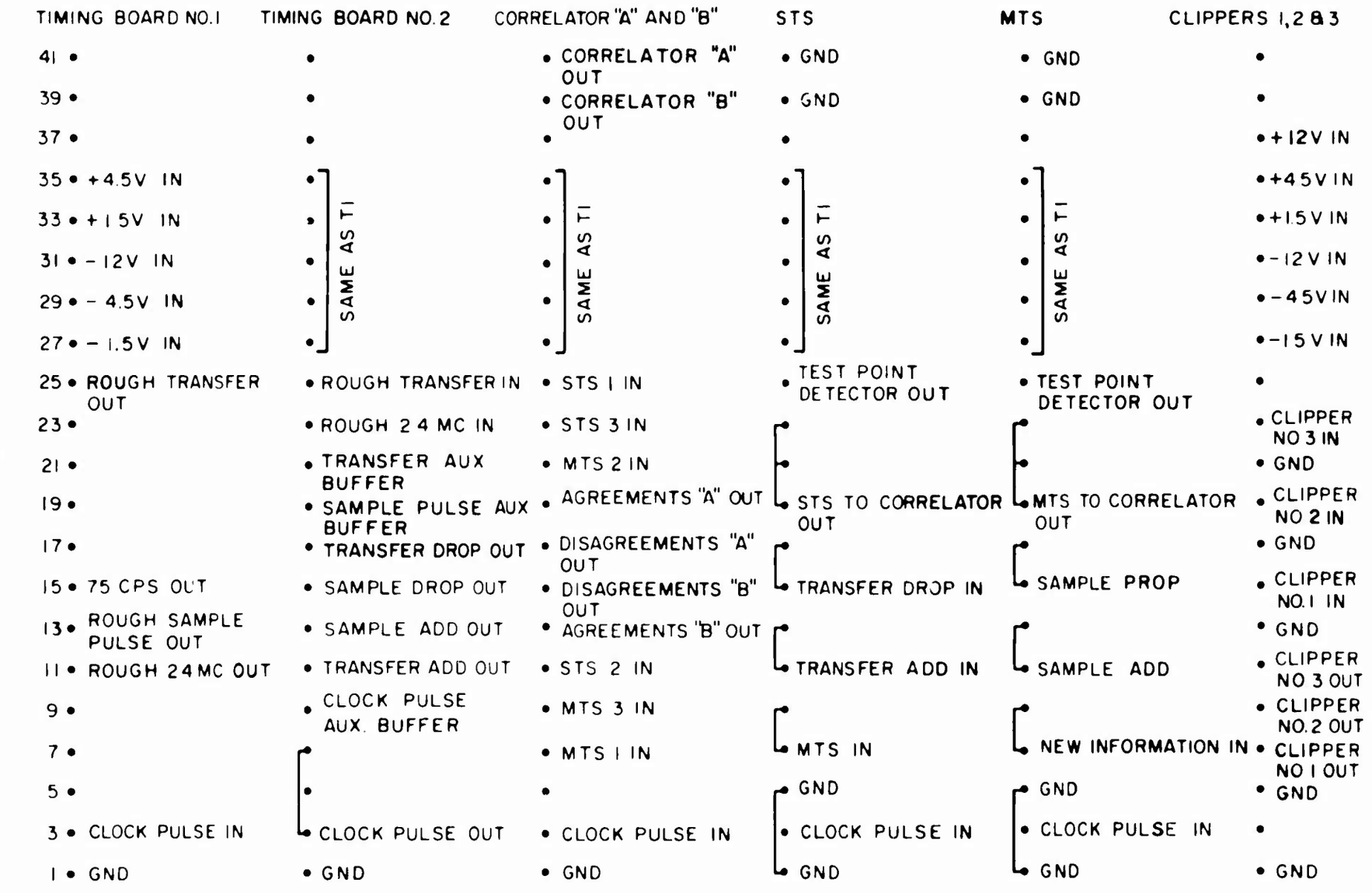


FIG. 18 PIN CONNECTIONS

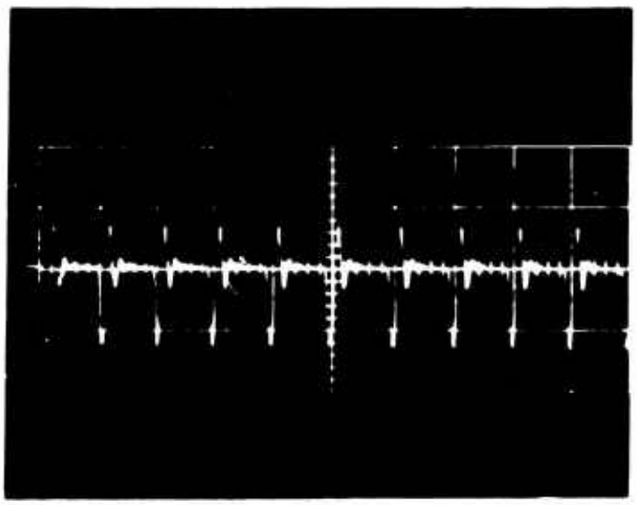


FIG. LOCATION	6
POINT	A
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM	1
CENTER LINE (VOLTS)	0
REMARKS	9.846 MC

FIG. 19 DELTIC RECLOCKING BUFFER INPUT

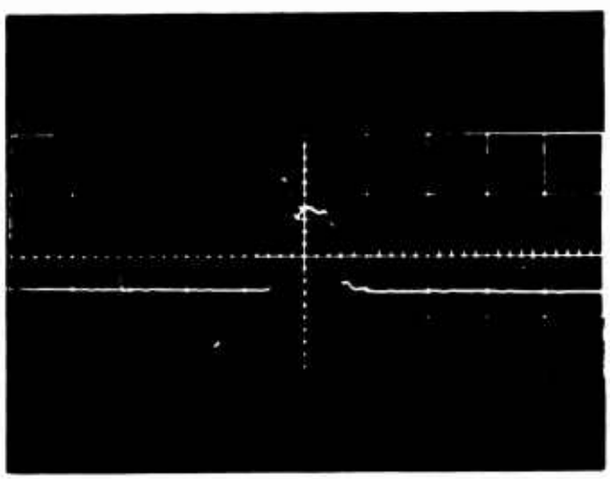


FIG. LOCATION	6
POINT	B
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	2
CENTER LINE (VOLTS)	0

FIG. 20 DELTIC MTS SAMPLING INPUT-GATE INPUT

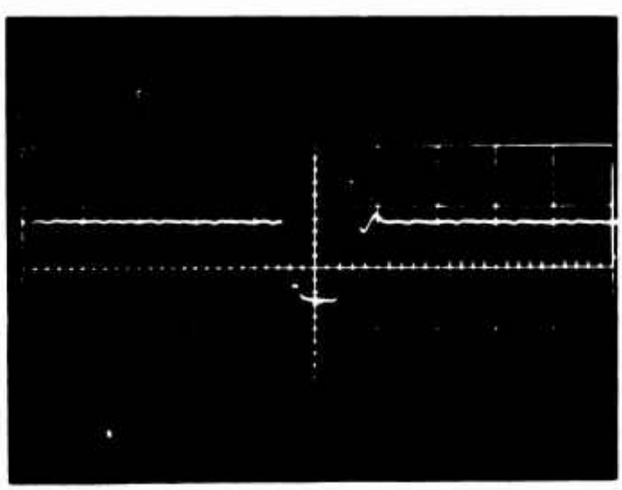


FIG. LOCATION	6
POINT	C
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	2
CENTER LINE (VOLTS)	0

FIG. 21 DELTIC MTS SAMPLING DROP-GATE INPUT

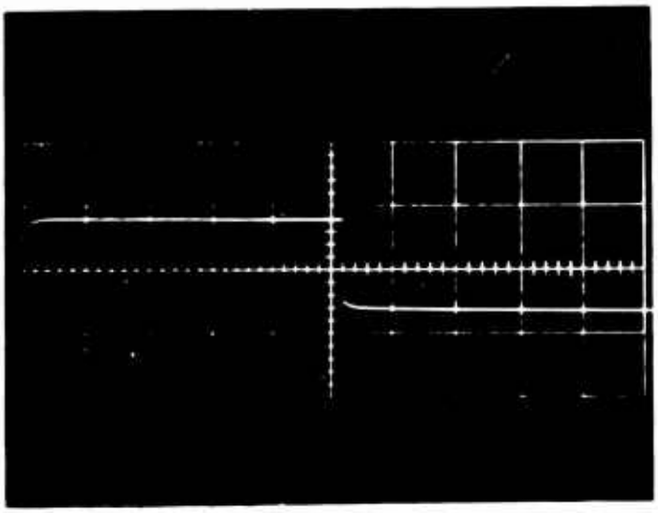


FIG. LOCATION	6
POINT	B
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	10
SENSITIVITY (VOLTS/CM)	2
CENTER LINE (VOLTS)	0

FIG 22 DELTIC STS TRANSFER INPUT-GATE INPUT

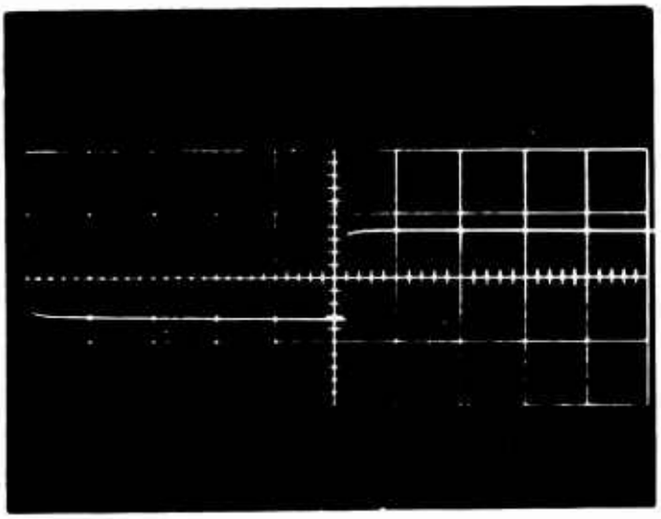


FIG LOCATION	6
POINT	C
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	10
SENSITIVITY (VOLTS/CM)	2
CENTER LINE (VOLTS)	0

FIG 23 DELTIC STS TRANSFER DROP-GATE INPUT

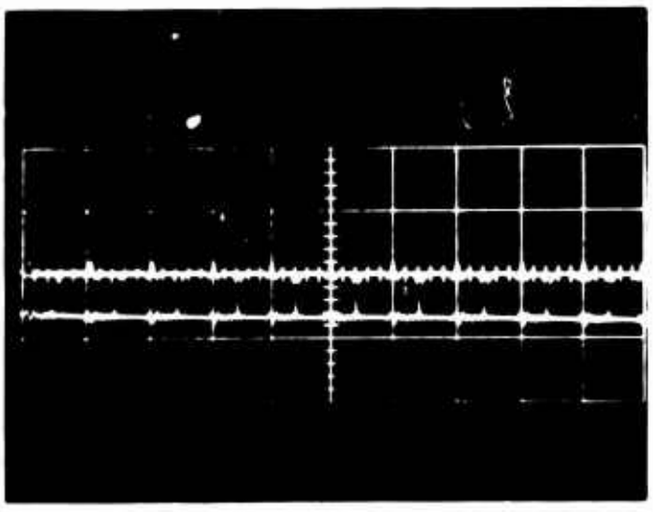


FIG LOCATION	6
POINT	D
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	2
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

FIG 24 DELTIC MTS MODULATOR-CONTROL GATE OUTPUT

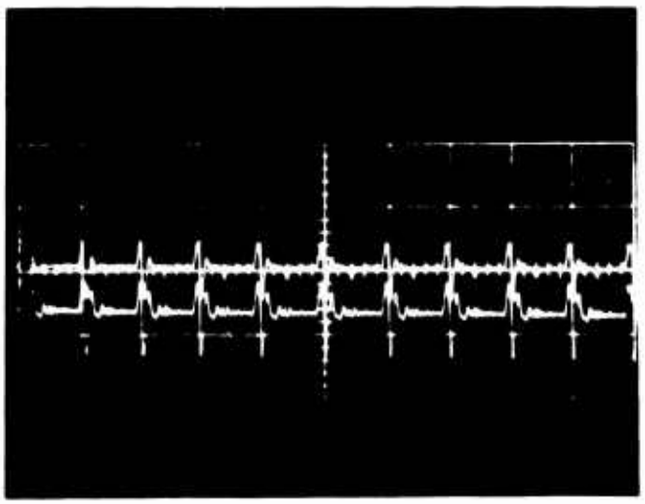
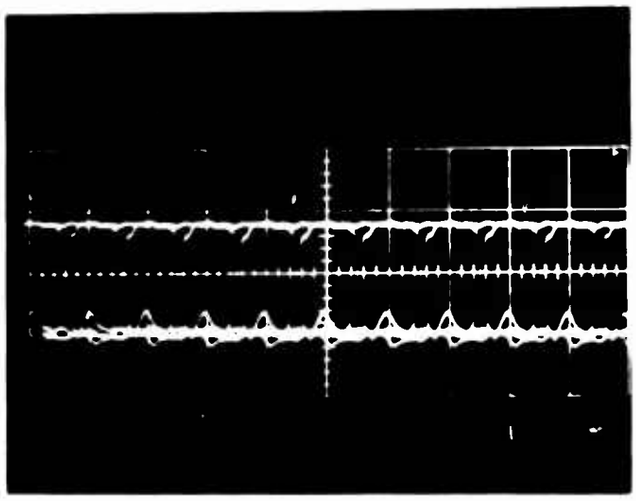


FIG. LOCATION	6
POINT	e
TRIGGER PERIOD(μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY(VOLTS/CM)	2
CLIPPER INPUT FREQ.(KC)	2.4
CENTER LINE(VOLTS)	0

REMARKS

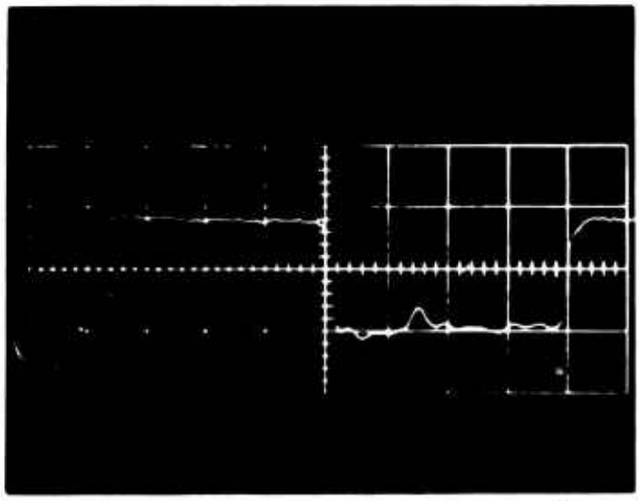
NOTE SIMILARITY TO FIG. 28

FIG. 25 DELTIC MTS MODULATOR INPUT



(a)

FIG. LOCATION	6
POINT	F
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0



(b)

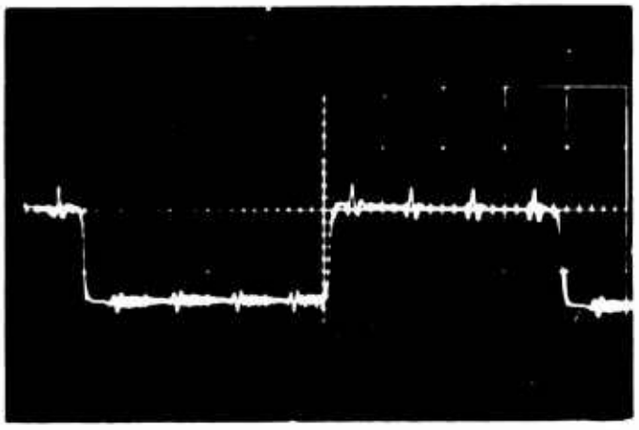
FIG. LOCATION	6
POINT	F
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

(c)

FIG LOCATION	6
POINT	F
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

SAME PICTURE OF EACH OBTAINED AT STS OUTPUT TO CORRELATOR WHEN INTERVAL BETWEEN TRIGGERS IS EITHER 52μS OR 26KμS

FIG.26 DELTIC MTS OUTPUT TO STS AND CORRELATOR



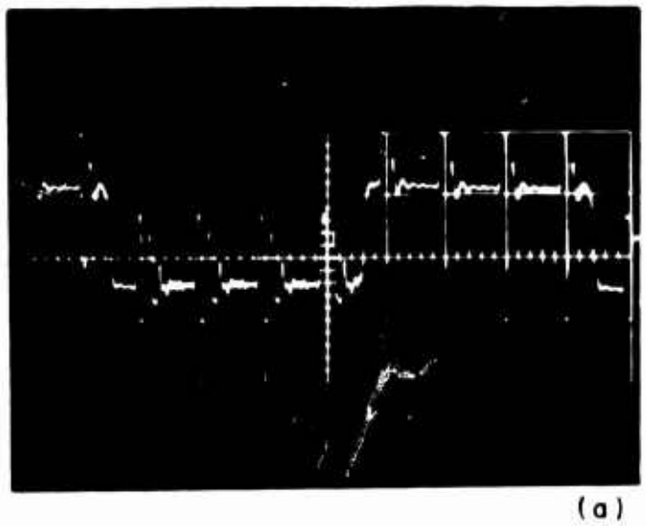
(a)

FIG. LOCATION	6
POINT	D
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ.(KC)	2.4
CENTER LINE (VOLTS)	0

(b)

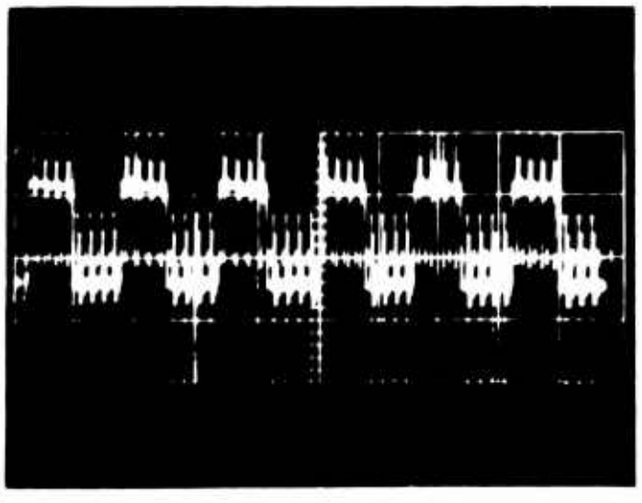
FIG LOCATION	6
POINT	D
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ (KC)	2.4
CENTER LINE (VOLTS)	0

FIG 27 DELTIC STS MODULATOR-CONTROL GATE OUTPOST



(a)

FIG. LOCATION	6
POINT	E
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-1



(b)

FIG. LOCATION	6
POINT	E
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-1

FIG 28 DELTIC STS MODULATOR INPUT

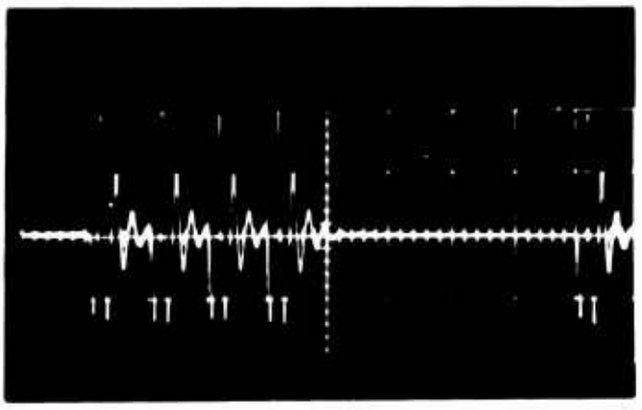


FIG LOCATION	6
POINT	G
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0 1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ (KC)	2 4
CENTER LINE (VOLTS)	0

(a)

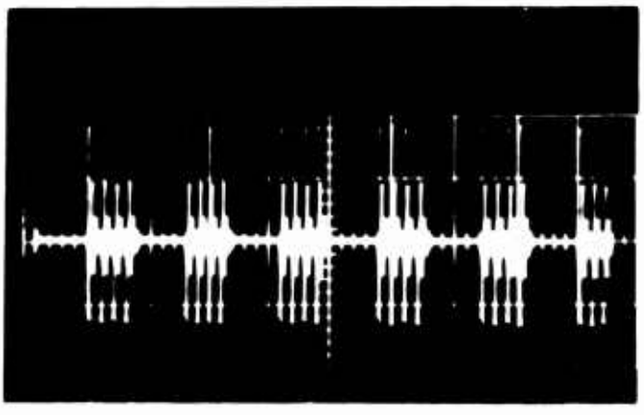
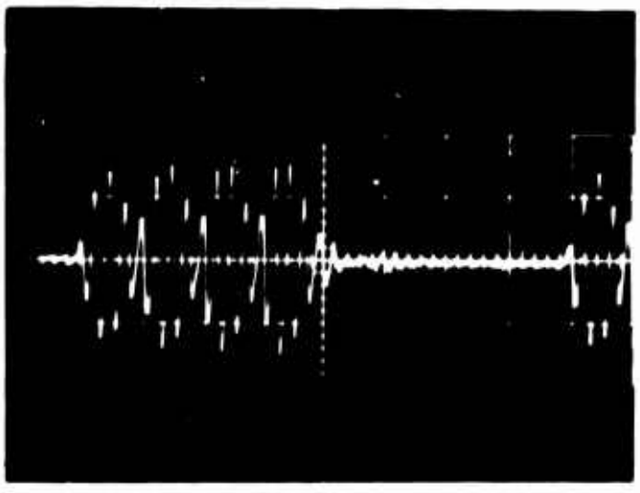


FIG LOCATION	6
POINT	G
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

(b)

FIG 29 DELTIC STS MODULATOR OUTPUT



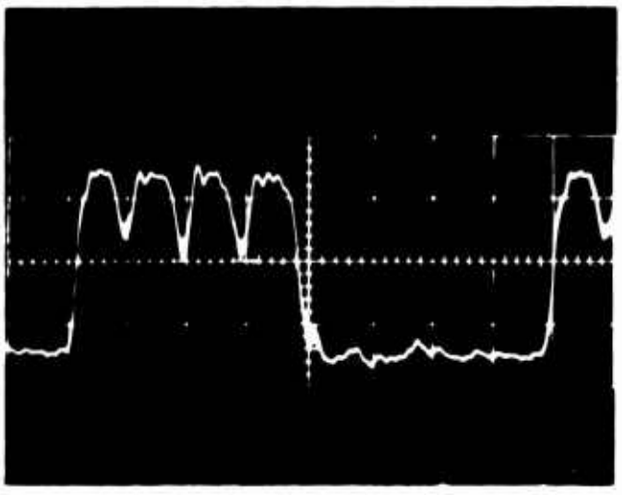
(a)

FIG. LOCATION	6
POINT	H
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	0.1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

(b)

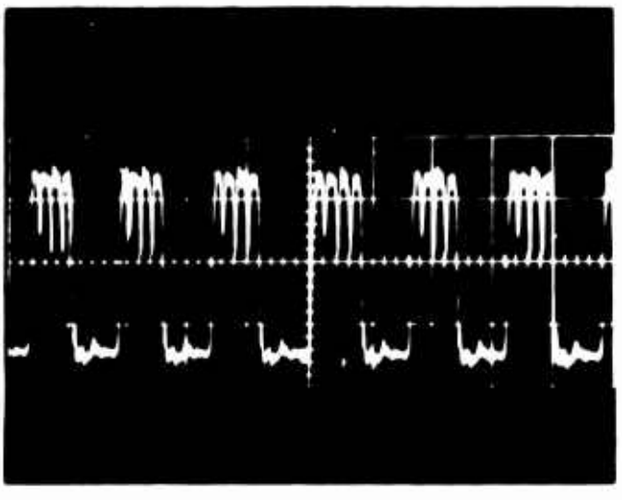
FIG. LOCATION	6
POINT	H
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	0.1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0

FIG 30 DELTIC STS RF AMPLIFIER 3RD BASE



(a)

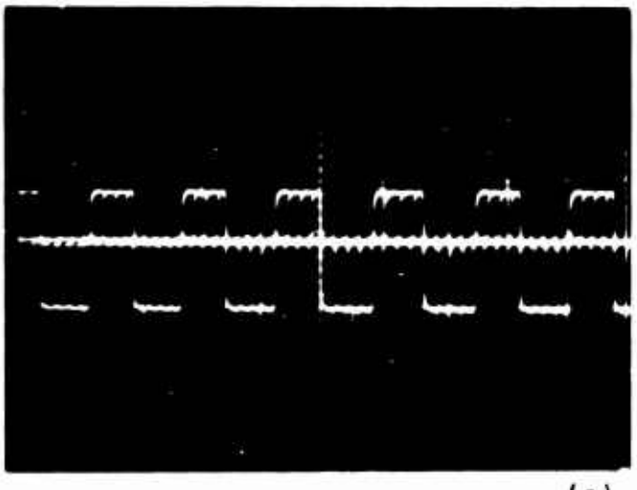
FIG. LOCATION	6
POINT	I
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	I
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	0



(b)

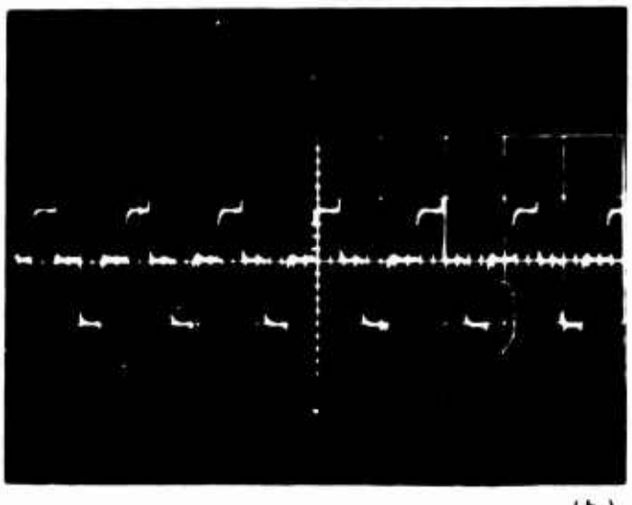
FIG. LOCATION	6
POINT	I
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	I
CLIPPER INPUT FREQ. (KC)	24
CENTER LINE (VOLTS)	0

FIG 31 DELTIC STS DETECTOR OUTPUT



(a)

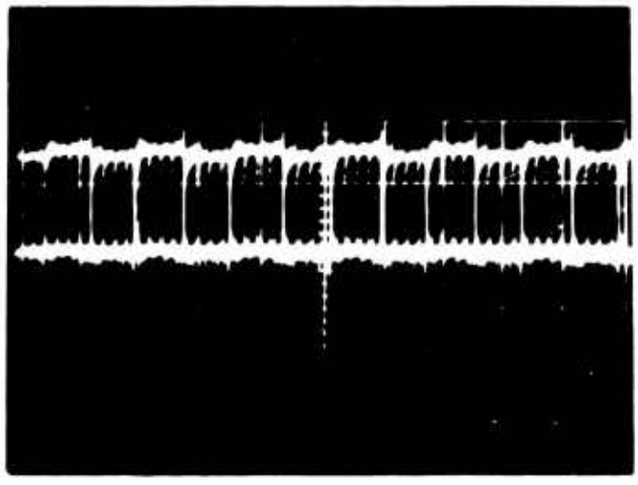
FIG LOCATION	12
POINT	J & K
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	2
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-6
REMARKS	DUAL TRACE



(b)

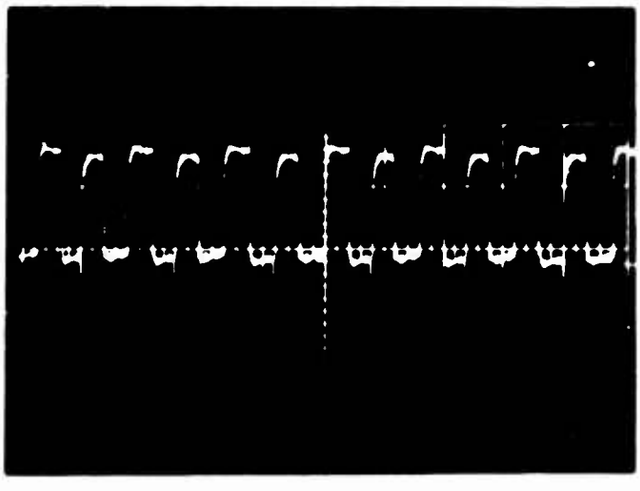
FIG LOCATION	12
POINT	J & K
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	2
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-6

FIG 32 CORRELATOR-COMBINED MTS AND STS SIGNALS



(a)

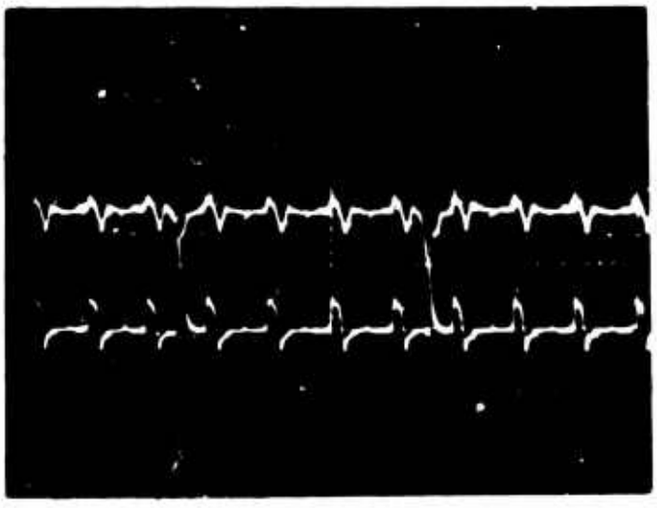
FIG. LOCATION	12
POINT	L
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ (KC)	2.4
CENTER LINE (VOLTS)	-6



(b)

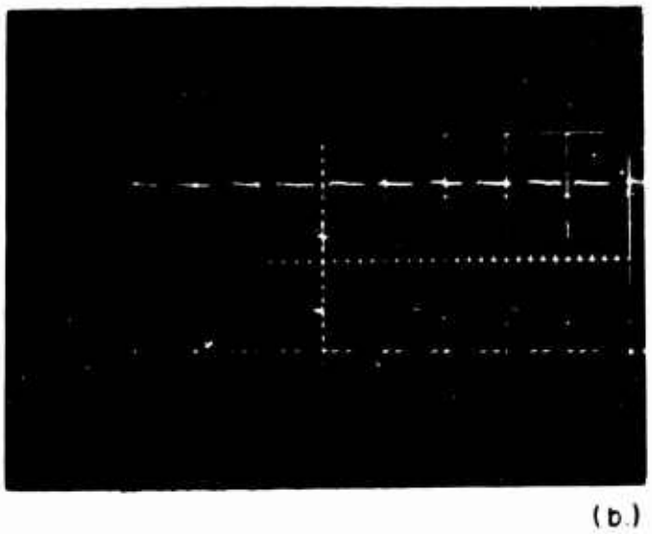
FIG LOCATION	12
POINT	L
TRIGGER PERIOD(μS)	26K
SWEEP RATE (μS/CM)	0.5
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ (KC)	2.4
CENTER LINE (VOLTS)	-6

FIG. 33 CORRELATOR AGREEMENTS AND DISAGREEMENTS



(a.)

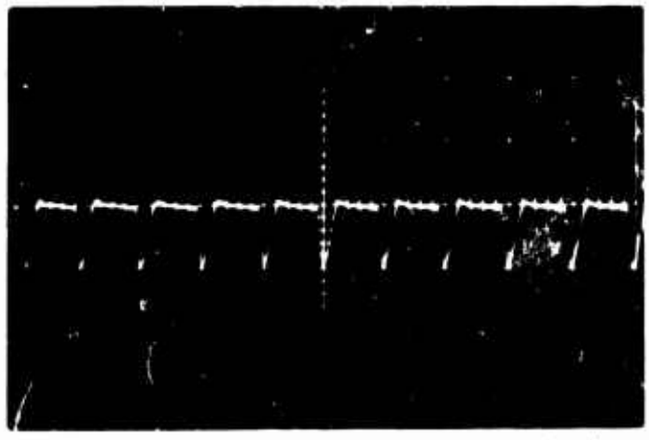
FIG. LOCATION	12
POINT	M & N
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM	1
CLIPPER INPUT FREQ. (KC)	2.4
REMARKS	AC INPUT



(b.)

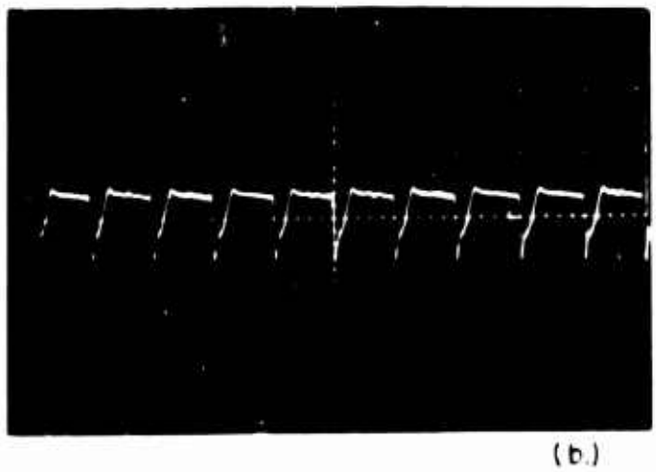
FIG. LOCATION	12
POINT	M & N
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	2
CLIPPER INPUT FREQ. (KC)	2.4
REMARKS	AC INPUT DUAL TRACE

FIG. 34 CORRELATOR AGREEMENTS AND DISAGREEMENTS



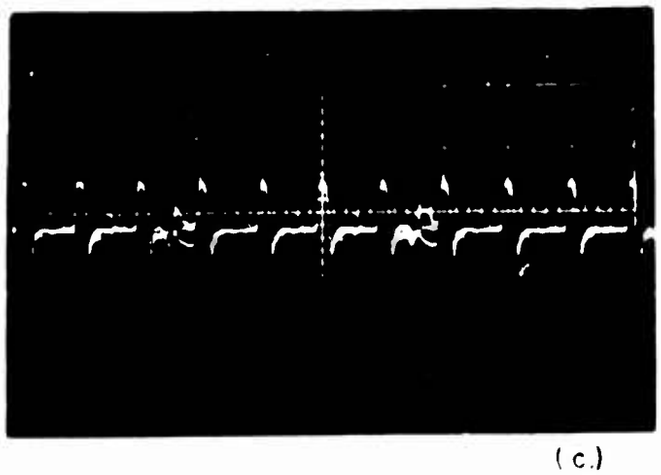
(a.)

POINT	O
TRIGGER PERIOD (μS)	52
SWEEP PERIOD (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-8



(b.)

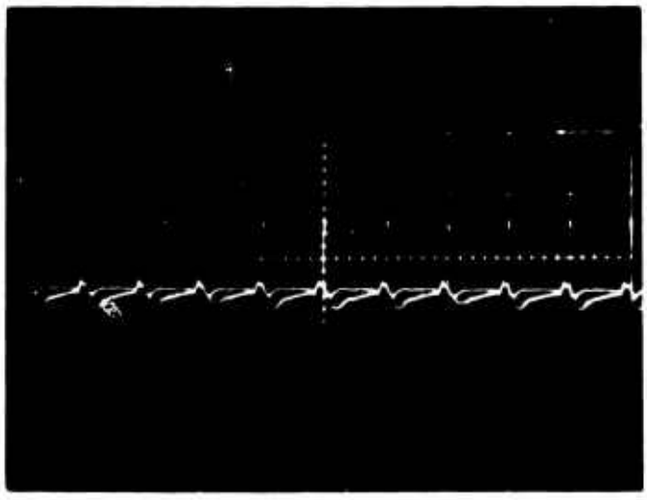
POINT	P
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
CENTER LINE (VOLTS)	-8



(c.)

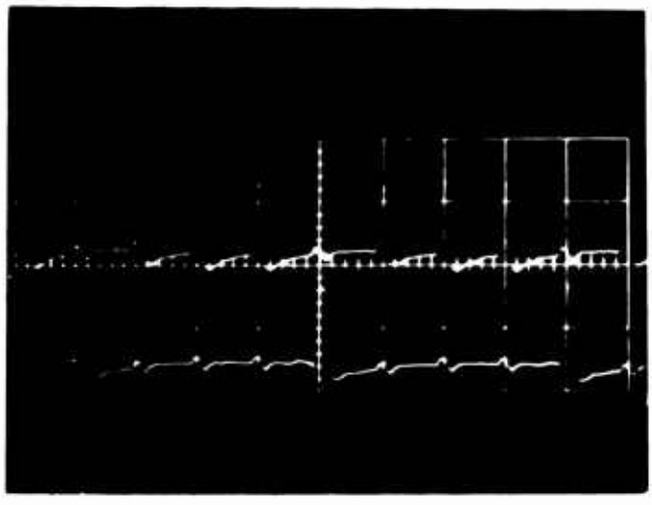
POINT	Q
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	2
CLIPPER INPUT FREQ. (KC)	2.4
REMARKS	AC INPUT

FIG 35 CORRELATOR RELOCKING PULSES



(a)

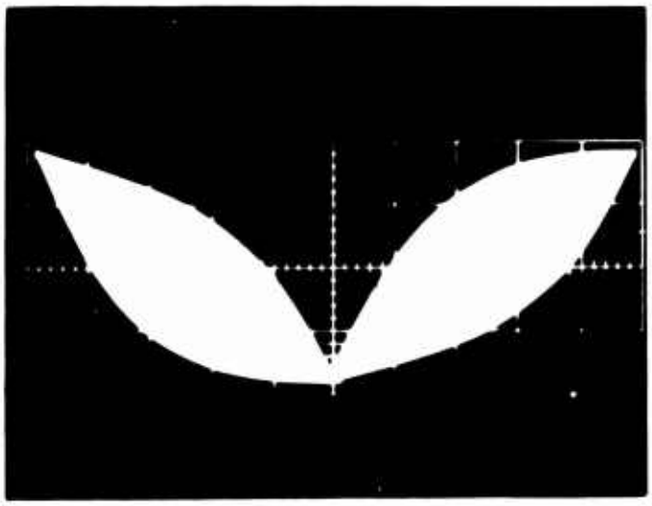
POINT	R & S
TRIGGER PERIOD (μS)	52
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ. (KC)	2.4
REMARKS	DUAL TRACE



(b)

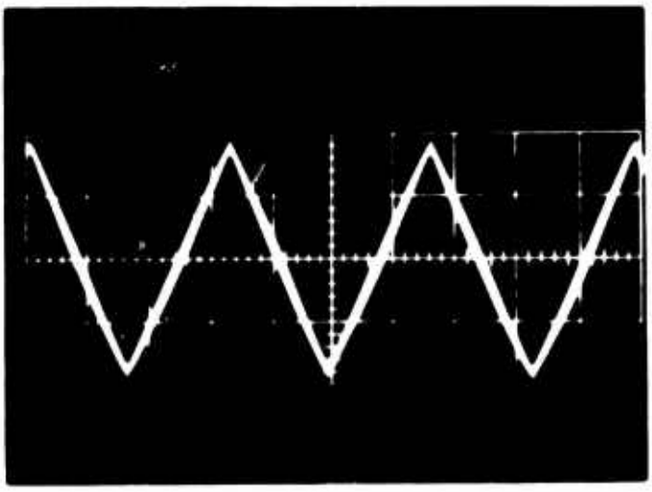
POINT	R & S
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	0.1
SENSITIVITY (VOLTS/CM)	1
CLIPPER INPUT FREQ (KC)	2.4

FIG. 36 CORRELATOR RECLOCKED OUTPUTS



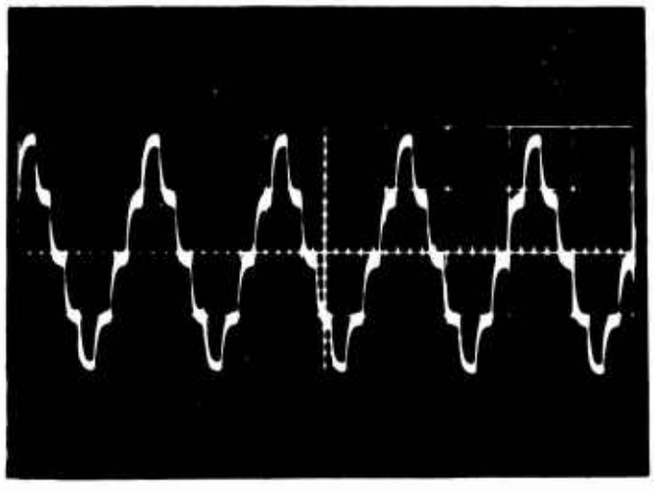
POINT	T
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	2.5K
SENSITIVITY (VOLTS/CM)	0.5
CLIPPER INPUT FREQ.(K.C)	0.038
REMARKS	S/N=∞*

FIG.37 CORRELATOR ANALOGUE OUTPUT



POINT	T
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	1K
SENSITIVITY (VOLTS/CM)	0.5
CLIPPER INPUT FREQ (KC/)	0.30
REMARKS	S/N=∞

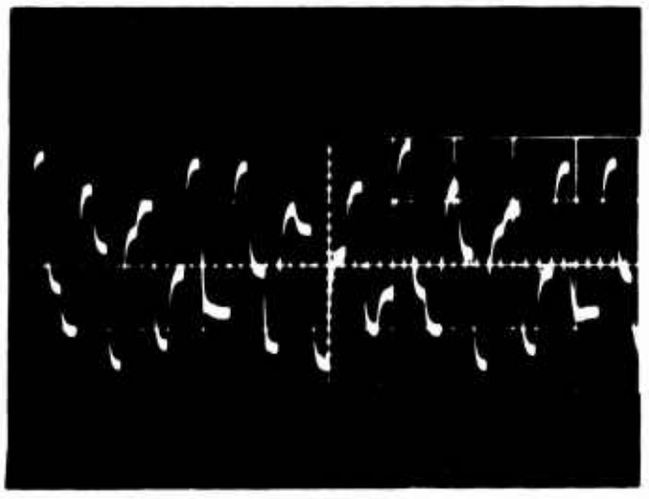
FIG.38 CORRELATOR ANALOGUE OUTPUT



POINT	T
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	200
SENSITIVITY (VOLTS/CM)	0.5
CLIPPER INPUT FREQ.(KC)	2.4
REMARKS	S/N=∞*

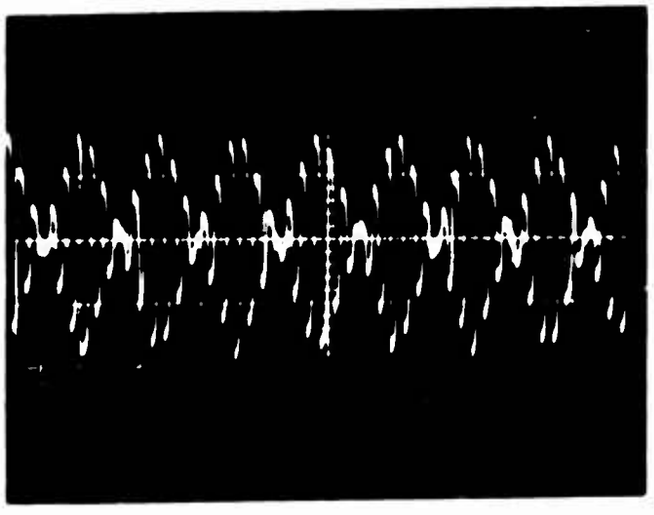
FIG.39 CORRELATOR ANALOGUE OUTPUT

*INPUTS TO CLIPPER MAY BE EITHER SYNCHRONIZED WITH DELTIC CLOCK OR UNSYNCHRONIZED



POINT	T
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	200
SENSITIVITY (VOLTS/CM)	0.5
CLIPPER INPUT FREQ. (KC)	6
REMARKS	S/N=∞*

FIG. 40 CORRELATOR ANALOGUE OUTPUT



POINT	T
TRIGGER PERIOD (μS)	26K
SWEEP RATE (μS/CM)	200
SENSITIVITY (VOLTS/CM)	0.5
CLIPPER INPUT FREQ. (KC)	9
REMARKS	S/N=∞*

FIG. 41 CORRELATOR ANALOGUE OUTPUT

*UNSYNCHRONIZED