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(FINAL REPORT NO. 1)

SOLID STATE TACAN RECEIVER-CODER

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-64- 235

FEBRUARY 1964

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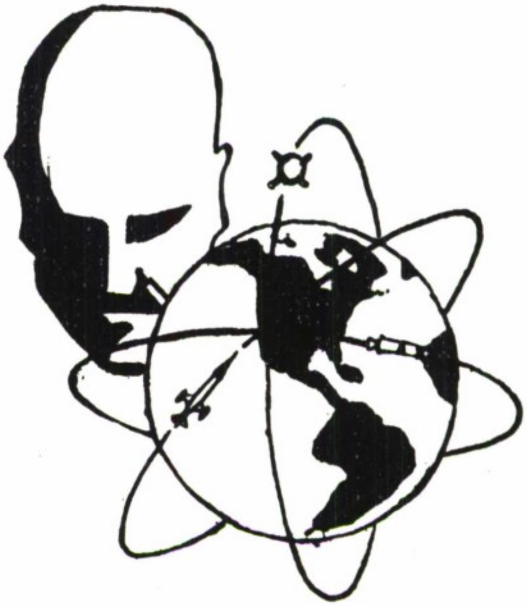

AD607184

(Prepared under Contract No. AF 19 (604)-8352 by Ground Systems Laboratory, ITT Federal Laboratories, 500 Washington Avenue, Nutley 10, New Jersey.)

DDC AVAILABILITY NOTICES

Solid State TACAN Receiver Coder

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SOLID STATE TACAN RECEIVER CODER

ABSTRACT

The design of a solid state receiver coder for use as part of a TACAN ground station is given. A detailed description of the deliverable breadboard from both its physical and electrical aspects is given, together with test results obtained to date and recommendations for further development.

KEY WORD LIST

1. RADIO COMMUNICATION SYSTEMS
2. PULSE COMMUNICATION SYSTEMS
3. TACTICAL AIR NAVIGATION (TACAN)
4. CODING
5. RADIO NAVIGATION
6. RADIO TRANSMITTERS
7. RADIO RECEIVERS
8. TRANSPONDERS

TABLE OF CONTENTS

SUPPLEMENTARY MATERIAL

LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

1.1 The Receiver Coder described in this report was developed under a contract awarded March 16, 1961, for the design and development of a "clean breadboard model of a Solid State TACAN Receiver-Coder". Also included in the report are details of various additional Receiver functions added March 1, 1962, under Mod. #2 to the contract.

1.2 As will be noted, there is considerable variance between modules in so far as their present performance under extreme temperature environment is concerned. The original contract called for operation from 0°C to +70°C when adjusted at +32°C and operation from -40°C to 0°C when adjusted at -15°C. It had been the contractor's intent to up-grade this to a -40°C to +80°C range (+65°C +15°C cabinet rise) in order that an over-all system could be realized which would meet the over-all requirements of the AN/TRN-17. At the end of January, 1963, however, USAF technical personnel in a visit to the contractor's plant decided on a "design freeze" and accordingly the Receiver-Coder herein described reflects this change in approach.

1.3 Work required on Mod.#3 to the contract will be covered under Final Report #2.

SECTION 2

PHYSICAL DESCRIPTION

2.1 The solid state receiver-coder deliverable under this contract is physically interchangeable with the tube-type receiver-coder presently in use in the AN/TRN-17 equipment. Figure 1 shows the solid state receiver-coder, ready for installation in the AN/TRN-17.

2.2 The solid state receiver-coder consists of nine modules. The relative location of each of these modules may be seen by comparing the information given in Table I below, with Figure 1.

TABLE 1

Reference Number	
1.	I. F. Amplifier
2.	Decoder Module
3.	I. F. Amplifier AGC Module
4.	Identity Module
5.	Bearing Circuits
6.	Timing Module
7.	Shaper Module
8.	Delay Line
9.	Low Voltage Power Supplies (see figure 5.)

2.3 The unit has twenty-five adjustable controls, which are used during initial alignment and maintenance. Table 2 below together with Figures 2, 3, and 4, locates all of these controls and also references their location on the proper schematic diagram.

TABLE 2

Reference Number	Function	Component Description	Schematic Number
10	Squitter Rate	R1412	T2319444
11	Identity Tone Equalization Pulse Spacing	R1312	T2319442
12	Output Multivibrator Pulse Width	R1324	T2319442
13	Dead-Time Duration	R1332	T2319442
14	30 Microsecond Pulse Width	R1801	T2319452
15	North Gate Multivibrator Width	R1608	T2319448

Reference Number	Function	Component Description	Schematic Number
16	Auxiliary Gate Multivibrator Width	R1708	T2319443
17	Output Pulse #1 Gate Width	R1907	T2319446
18	Output Pulse #2 Gate Width	R1919	T2319446
19	Shaper Driver Pulse Width	R1933	T2319446
20	Shaper Filter Termination	R2001	T2319449
21	Base Shaping	R2003	T2319449
22	Peak Shaping #1	R2007	T2319449
23	Peak Shaping #2	R2011	T2319449
24	Operational Amplifier Gain Control (Factory Adjusted)	R2023	T2319449
25	Operational Amplifier HF Gain Control (Factory Adjusted)	C2019	T2319449
26	Auxiliary Reference Burst Pulse Spacing	J1	T2319452
27	North Reference Burst Pulse Spacing	J2	T2319452
28	Pulse Spacing Adjustment	J3	T2319452
29	Beacon Response Delay Adjustment	J4	T2319452
30	Ferris Discriminator Primary Tuning	L1119-L1120	D2319450
31	Ferris Discriminator Coupling	C1151	D2319450
32	Ferris Discriminator Secondary Tuning	C1154	D2319450
33	Identity Coding Panel	P/O Keyer	
34	Code Selector Switches	P/O Keyer	

2.4 The unit requires four input connections and two output connections. Table 3 on the next page lists these, and references them to Figure 5. (Note that in almost every case the unit will require no external wiring changes in an AN/TRN-17.)

TABLE 3

Reference Number	Location	Input	Output
35	TB2-30	1350 cps Antenna Tone	-
36	TB3-42	Auxiliary Reference Burst Antenna Trigger	-
37	TB3-43	North Reference Burst Antenna Trigger	-
38	TB4-60	-	Gate Pulse Output to Gate Modulator
39	TB4-61	-	Shaped Pulse Output to Shaped Pulse Modulator
40	J1101	IF Amplifier Input	-

SECTION 3

THEORY OF OPERATION

3.1 System Considerations - The solid state receiver coder described in this report is divided into several modules according to function. The receiver is comprised of a 63 mc IF amplifier and ancillary video circuits, (modules 1 through 4). The coder includes reference burst generators, an encoder and a pulse shaper, (modules 5 through 8). A brief functional description of each of the modules is included below (see Figure 6), a more detailed discussion appearing in sections 3.2 through 3.9.

3.1.1 IF Amplifier - consists of ten double-tuned stages, a video amplifier and a ferris discriminator, the latter providing the adjacent channel rejection.

3.1.2 Decoder - rejects improperly coded interrogations and generates squitter from the IF output.

3.1.3 Identity - generates identity coded pulses from the 1350 cps antenna tone wheel and establishes priority between the identity and squitter pulses as directed by the keyer.

3.1.4 IF Amplifier AGC - counts the decoder squitter output and adjusts the IF amplifier gain so as to maintain an average output pulse rate of 2700 pulses per second.

3.1.5 North Reference Burst Generator - generates the north reference burst and north precedence gate from the north antenna trigger.

3.1.6 Auxiliary Reference Burst Generator - generates the auxiliary reference burst and auxiliary precedence gate from the auxiliary antenna trigger.

3.1.7 Delay Line Driver - processes the reference marker bursts, assigning them priority over the identity/squitter signal obtained from the identity module.

3.1.8 Timing - sets the over-all beacon delay, provides the pulse pair coding and generates a blanking waveform for disabling the receiver during transmission. Also drives the transmitter gate modulator.

3.1.9 Shaper - shapes the video pulses applied to the transmitter shaped pulse modulator in order to minimize the energy transmitted on the adjacent channel.

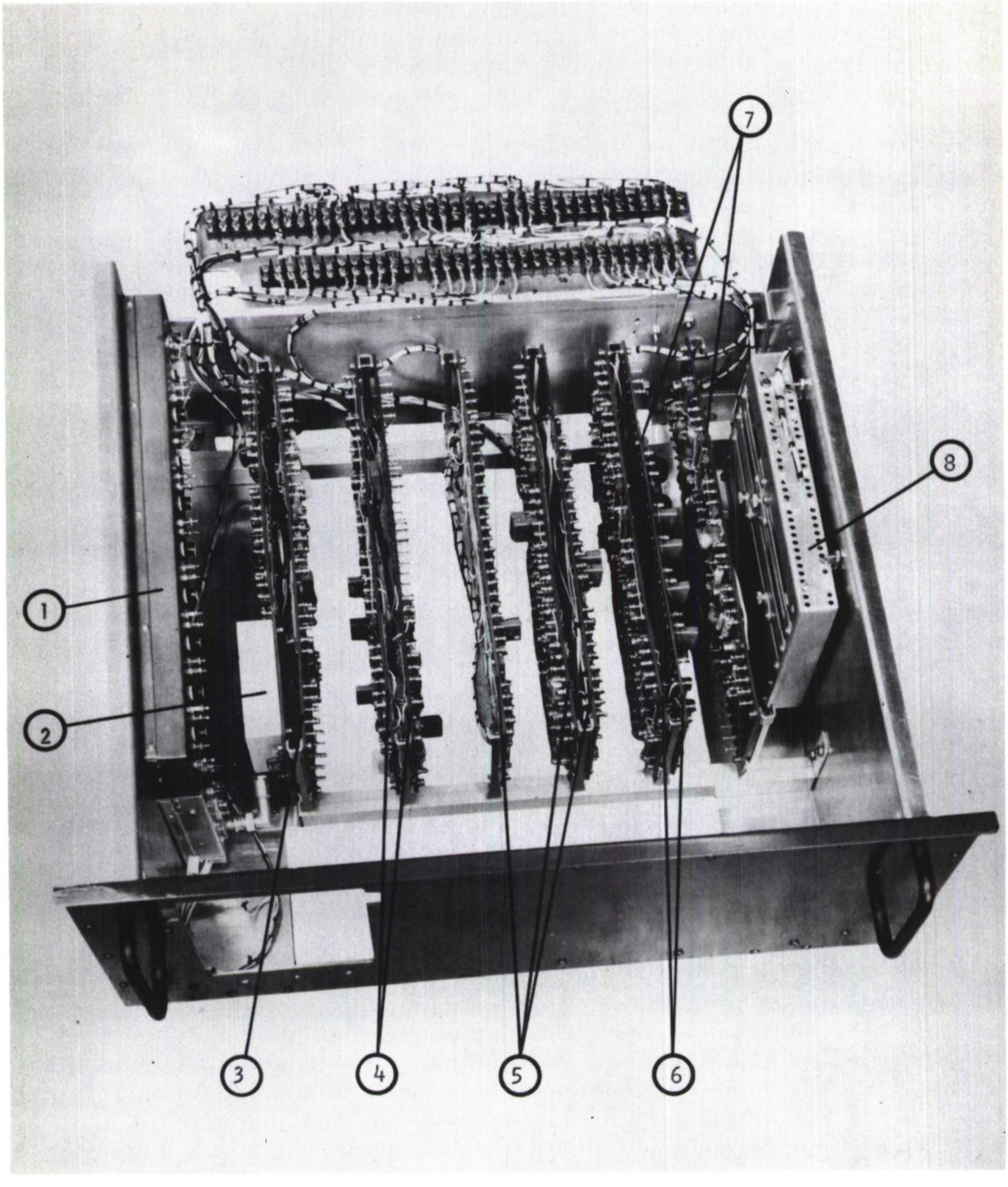


Figure 1. Solid State Receiver Coder

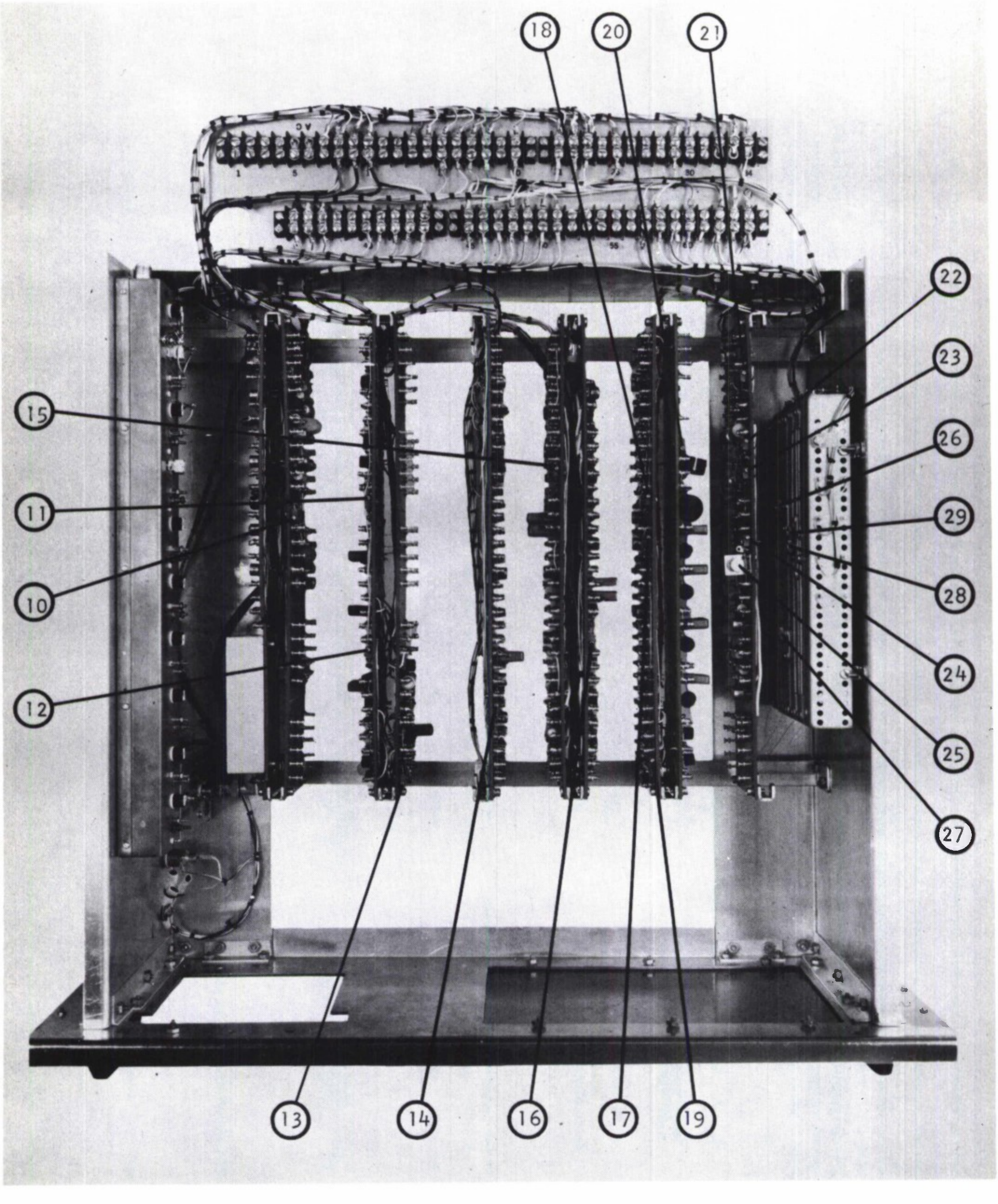


Figure 2. Maintenance Controls - Solid State Receiver Coder

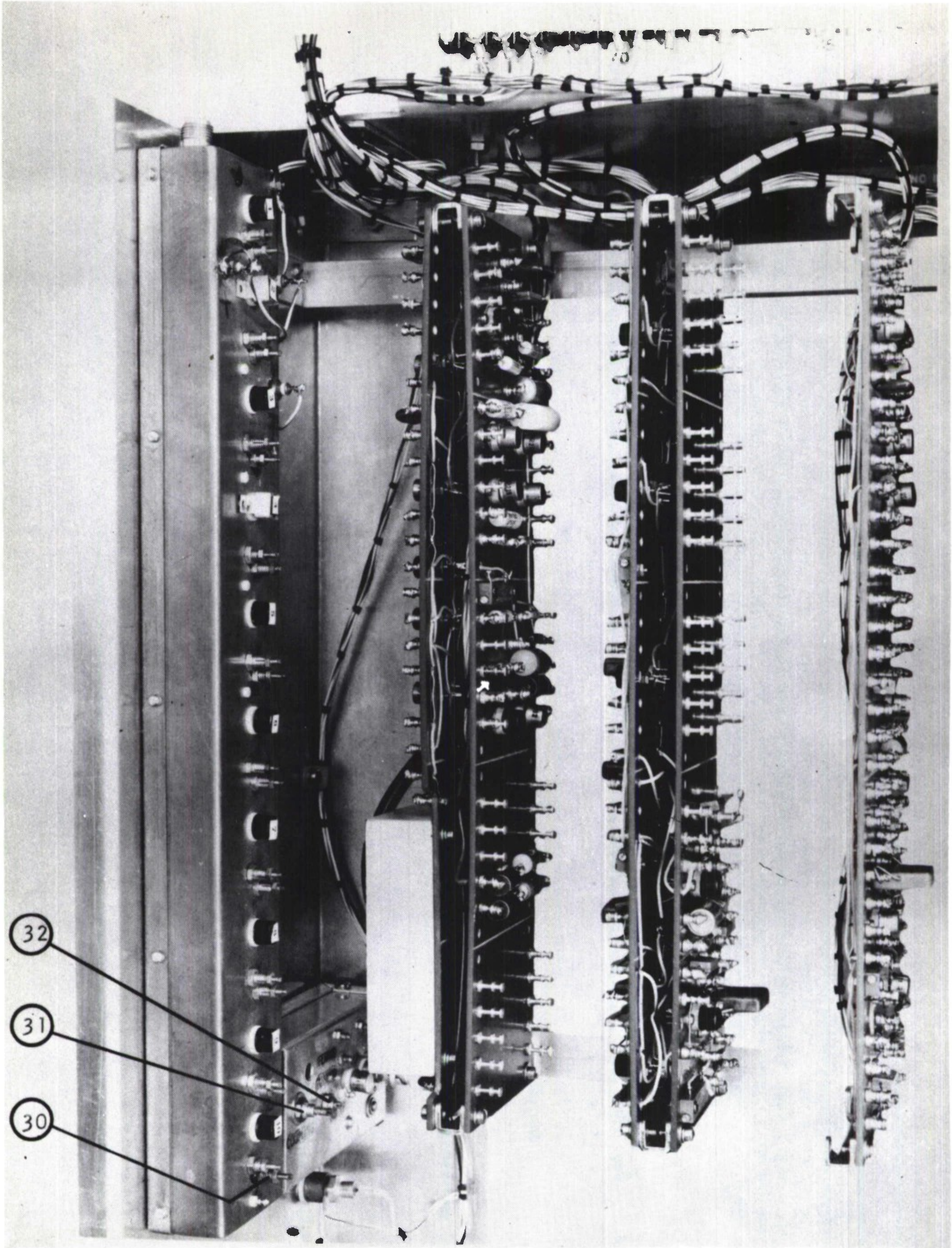


Figure 3. Ferris Discriminator Adjustments - I.F. Amplifier

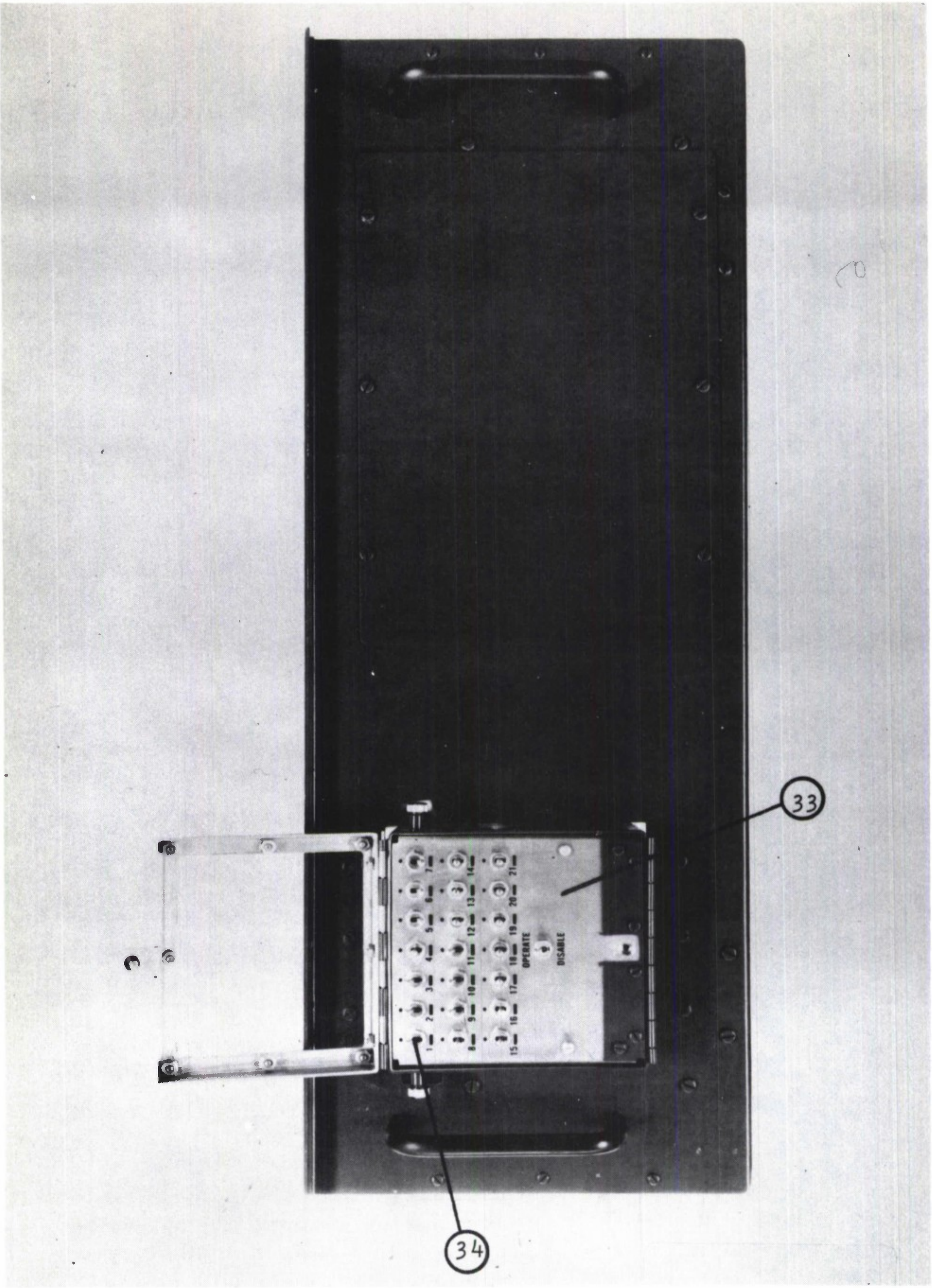


Figure 4. Identification Keyer

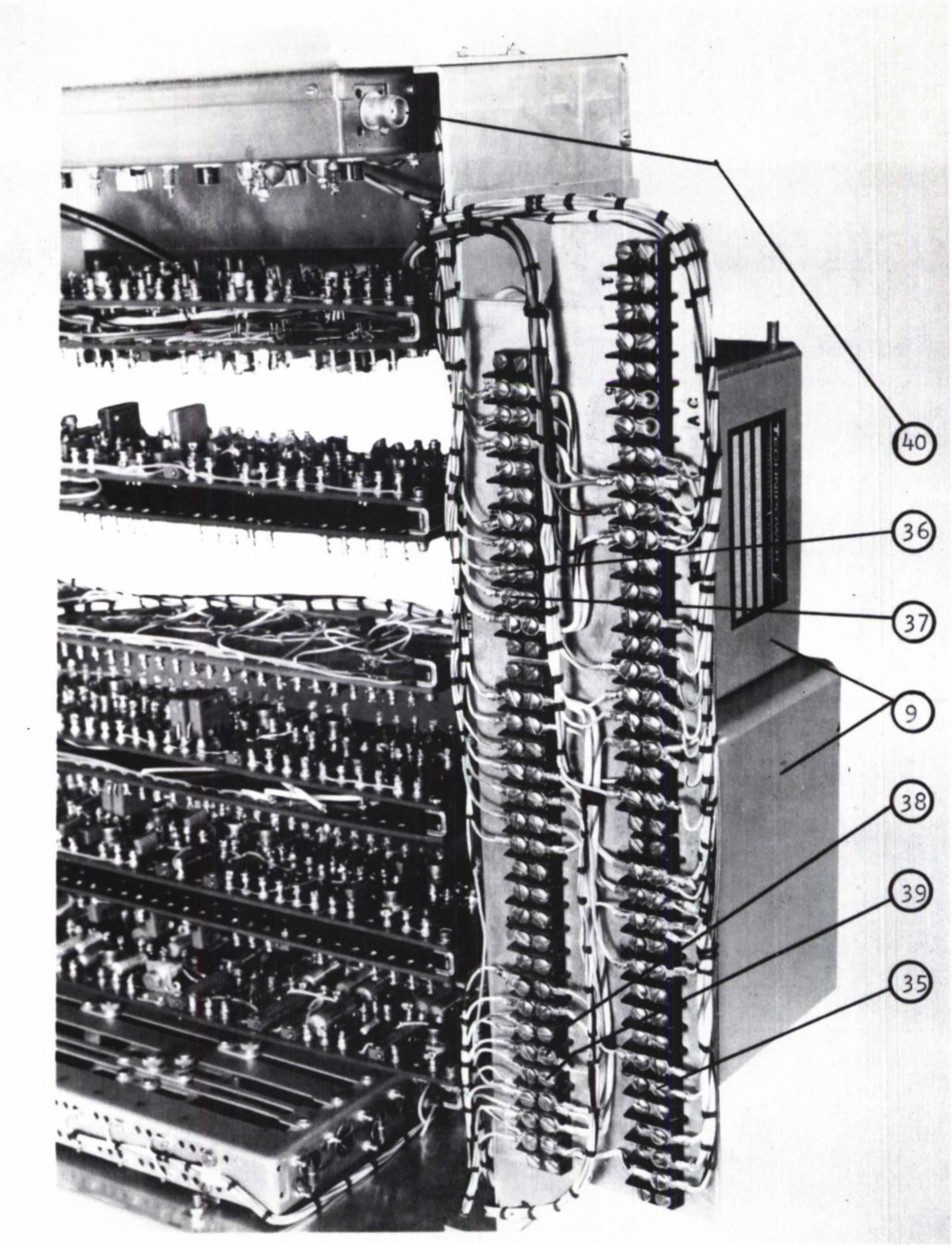


Figure 5. Rear Panel Wiring

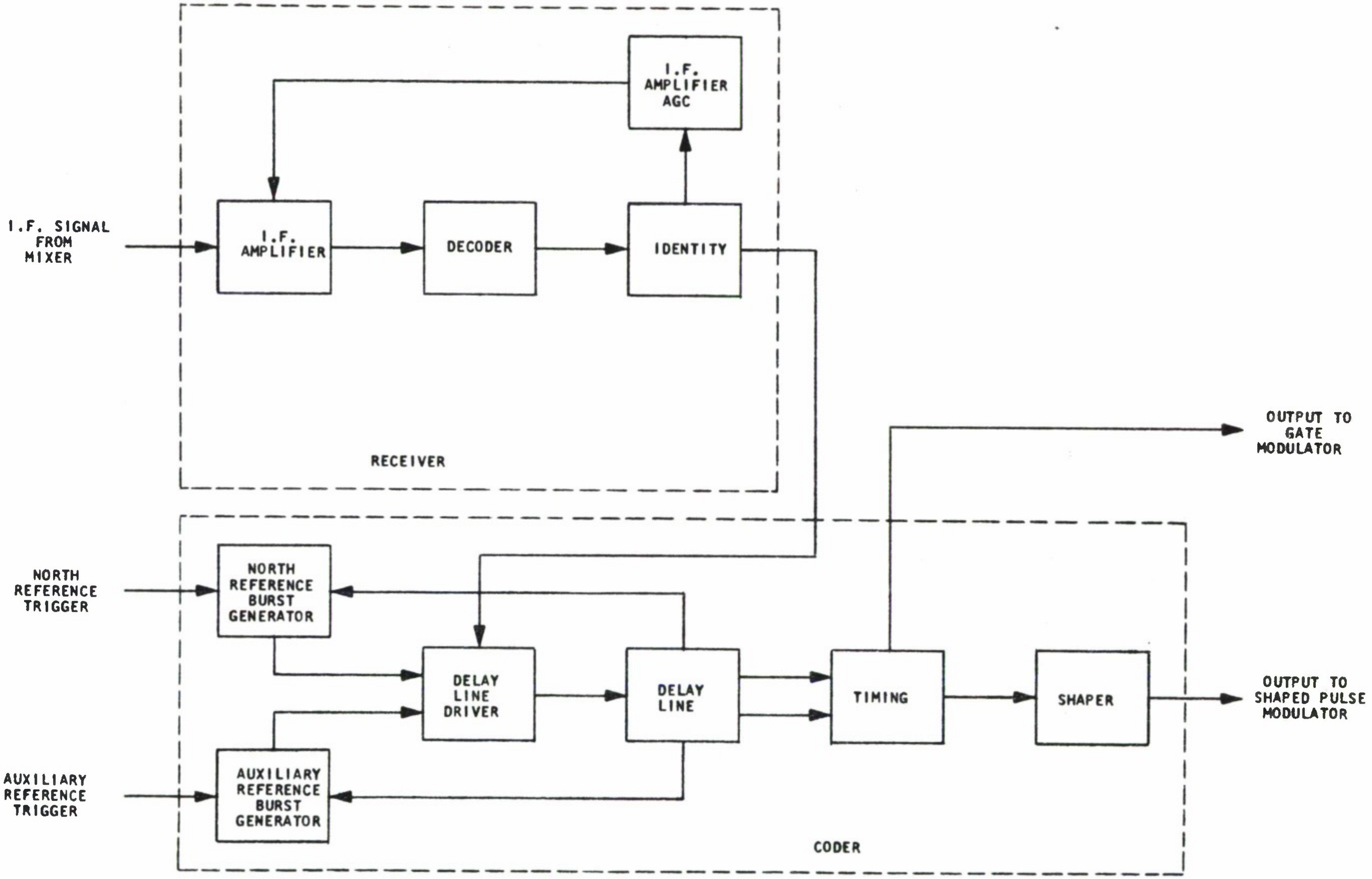


Figure 6. Receiver Coder

SECTION 3.2

IF AMPLIFIER

3.2.1 The IF Amplifier chassis contains ten stages of IF amplification followed by a Ferris frequency discriminator and a stage of video amplification (see Figure 7). Since this unit is essentially an expanded version of a three stage breadboard, the design of which was covered extensively in the Interim Scientific Report, January, 1963, the following discussion is limited to a brief review.

3.2.2 Referring to the schematic diagram, D2319450, it can be seen that the 3N35 silicon tetrode transistor is employed, in the common emitter configuration, for IF amplification. This transistor exhibits good AGC characteristics along with temperature and frequency stability. A collector swamping resistor along with the reflected input resistance of the following stage serve to mismatch the transistor output by a five to one ratio, this intentional mismatch facilitating stabilization without complicated neutralizing networks.

3.2.3 Interstage coupling and bandpass response is accomplished with synchronous double tuned networks. Each of these inductively coupled stages is designed for transitional coupling, the first nine being coupled critically in addition.

3.2.4 The tenth IF stage feeds the Ferris discriminator's low-Q resonant circuit (Figure 8). After detecting and mixing the opposite polarity responses of the high-Q and low-Q circuits, the desired Ferris response is established. The resultant on-channel negative-going output is amplified and inverted in a video amplifier feedback pair.

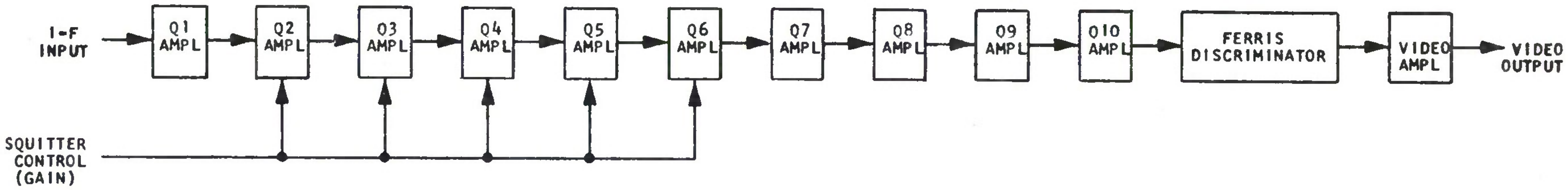


Figure 7. I. F. Amplifier

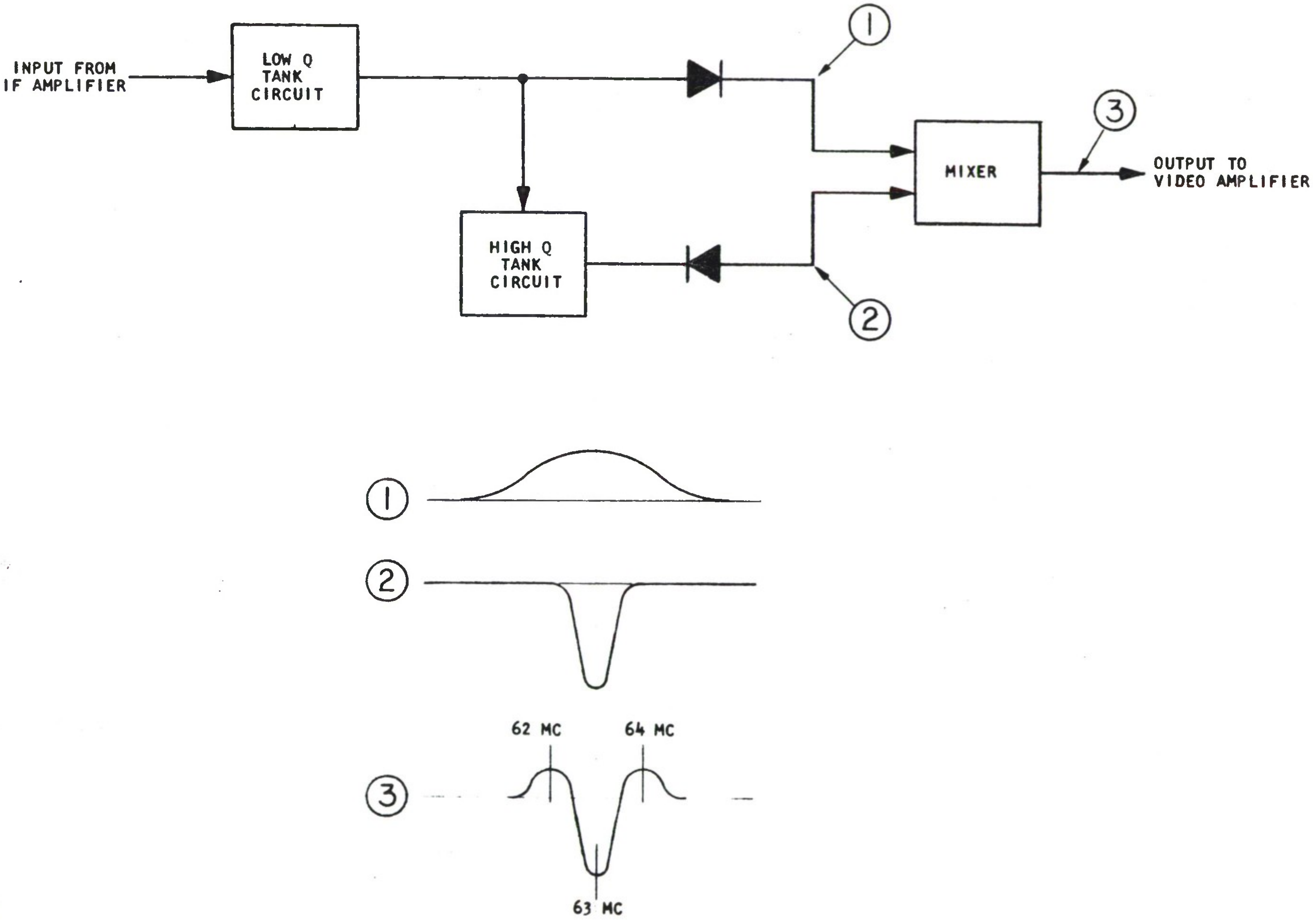


Figure 6. Ferris Discriminator

SECTION 3.3

DECODER MODULE

(See Figure 9 and Schematic G2319440)

3.3.1 The output of the IF amplifier is coupled to the video amplifier Q1201, Q1202, a feedback amplifier pair with negative feedback employed over two stages in order to stabilize the gain. Bias point stabilization for Q1201 is obtained by R1206, the bypassed resistor in the emitter of that stage, while R1210 and R1211 serve the same function for Q1202. In order to obtain adequate bias stabilization without severely restricting the collector swing of Q1202, the emitter resistance is returned to the negative supply.

3.3.2 The video amplifier output is coupled to the pulse-pair decoder DL1201, CR1201 through CR1204 and R1221. The second pulse of each 12 microsecond pair appears at the cathode of CR1201 at the same instant in time that the first pulse, after being delayed 12 microseconds by the line, appears at the cathode of CR1202. With both diodes reverse-biased, the current through R1221 and CR1203 falls to zero and the base voltage of Q1205 increases. Thus, whenever coincidence occurs a negative going signal is produced at the collector of Q1205. Q1204, an emitter follower, serves to isolate the delay line from the low impedance "AND" gate.

3.3.3 Diode CR1204 is normally reverse biased but conducts heavily to clamp the decoder output to ground when the blanking/dead time signal obtained from the dead time generator (located in the identity module) appears. CR1205 is forward biased through R1220, which is returned to B+ by the keyer line, and thus the signal appearing at the collector of Q1205 is coupled to the identity module. During identity tone transmission the keyer line is returned to ground and the series diode, CR1205, reverse biased, thereby killing the squitter signal to the identity module.

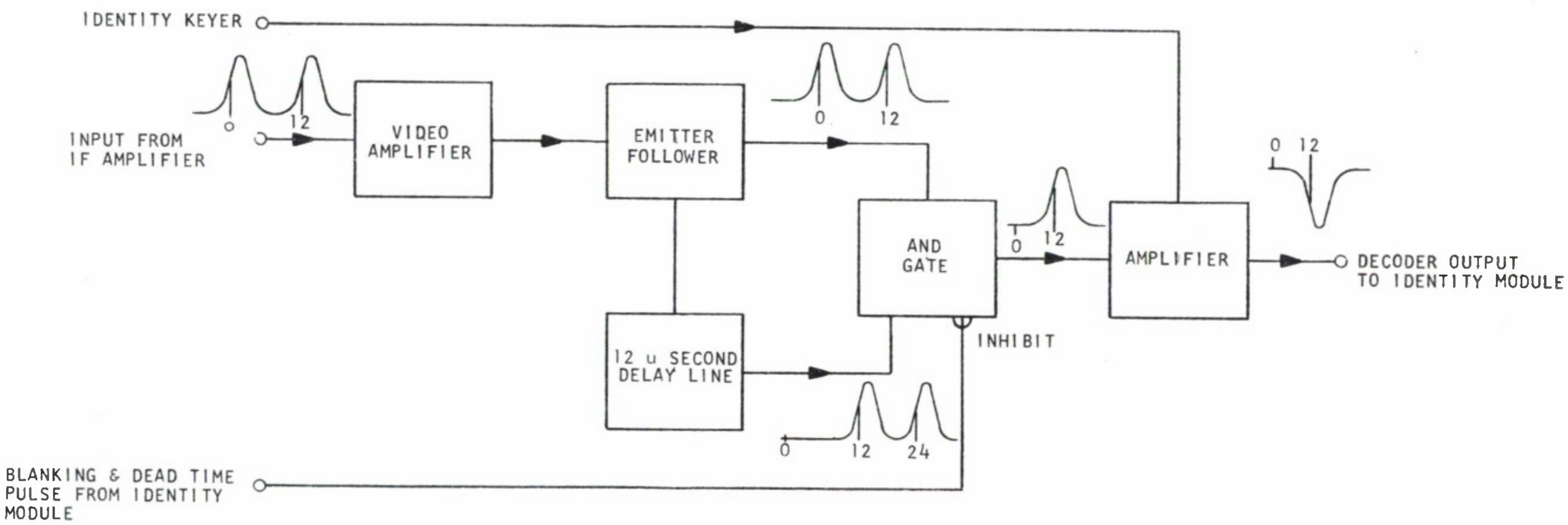


Figure 9. Decoder Module

SECTION 3.4

IDENTITY MODULE

(See Figure 10 and Schematic T2319442)

3.4.1 The 1350 cycle sinusoidal tone generated in the antenna is shaped into a square wave suitable for triggering the equalizing multivibrator by Q1301 and Q1302. Both amplifiers are biased so that symmetrical clipping takes place, bias point stabilization being provided by R1305 and R1310. The square wave output of Q1302 is differentiated by C1305 and R1311 and used to trigger the 100 microsecond identity tone equalization multivibrator, a conventional collector coupled one-shot. CR1301 serves as a triggering diode which disconnects the triggering source from the base of the normally on transistor, Q1303, while CR1302 isolates the base of Q1303 from the full collector swing of Q1304 and thus prevents zenering of the base-emitter junction. Timing is accomplished by C1307, R1313 and R1312, the latter providing precise adjustment of the multivibrator output pulse width.

3.4.2 Differentiated outputs are taken from the leading edge of the collector waveform of Q1304 and the trailing edge of the collector waveform of Q1303, providing a pair of 100 microsecond negative-going triggers with a 1350 cycle rate at the junction of CR1303, CR1304 and R1322. During normal distance/squitter transmission, CR1304 is forward biased through R1322, which is returned to B+ by the keyer line and thus shunts the paired identity tone triggers to ground. When identity is to be transmitted, however, the keyer line is returned to ground so that the shunt diode CR1304 is no longer forward biased. The negative triggers appearing across the now non-conducting diode are then coupled to the output multivibrator.

3.4.3 Q1305 and Q1306 constitute the output multivibrator, a collector coupled one-shot similar to the identity tone equalization multivibrator, diodes CR1305 and CR1306 serving to disconnect the base of the normally conducting transistor from the triggering source and the timing waveform respectively. In order to utilize a more linear portion of the timing exponential and thereby increase timing accuracy, the timing resistors, R1324 and R1325, are returned to the B+ supply, the collector load resistors grounded and the emitters returned to the negative supply. R1324 is adjusted for an output pulse width of precisely 14 microseconds. The positive going pulse appearing in the collector of Q1305 is coupled to both the AGC and bearing modules.

3.4.4 The positive going pulse appearing at the collector of Q1305 is differentiated by C1314, R1331, and the trailing edge used to trigger the dead time generator, basically a collector coupled one-shot, Q1307 and Q1308, and a blanking/dead time amplifier, Q1309.

Since the multivibrator must be capable of being adjusted over such a wide range (6 to 51 microseconds), the timing resistors R1332 and R1333 are AC coupled to the base circuit of Q1307, the base current being supplied by R1334. By this means the multivibrator may be adjusted throughout its range with the DC operating point remaining unaffected. Sequential triggering of the two multivibrators and the addition of their outputs to form the dead-time gate permits each multivibrator to fully recover before the next decoder output pulse appears. This ensures that the minimum dead time is obtained regardless of when the next squitter/distance interrogation pulse occurs.

3.4.5 The positive going collector waveforms of Q1305 and Q1307 are combined in the base circuit of Q1309 with the blanking signal obtained from the timing module. The negative going output of Q1309 forward biases diode CR1204 in the decoder, thereby clamping the pulse pair decoder to ground and providing receiver blanking and dead time.

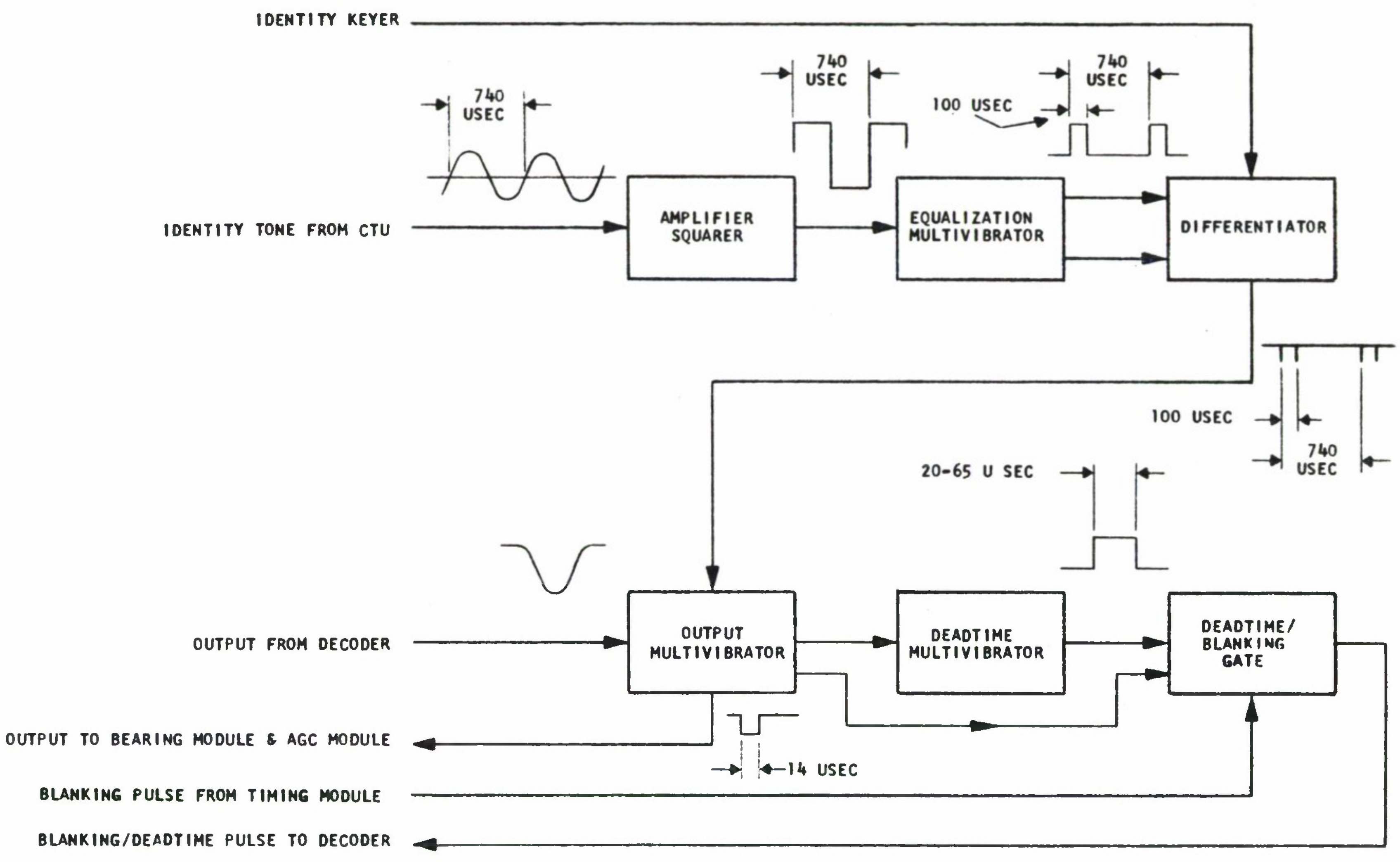


Figure 10. Identity Module

SECTION 3.5

IF AMPLIFIER AGC MODULE

(See Figure 11 and Schematic T2319444)

3.5.1 The squitter rate is maintained by controlling the amplitude of the noise output of the IF amplifier. Basically, the squitter rate is controlled in this manner: the squitter output of the identity module is counted and a control voltage obtained, the control voltage in turn determining the operating gain of the IF amplifier. Should the squitter rate change, the control voltage will attain another value and select a new operating point for the IF amplifier so as to restore the noise output to its former value. By utilizing a high loop gain and designing each element in the loop for good temperature stability, precise control of pulse repetition frequency may be obtained over a wide environmental range.

3.5.2 The IF amplifier AGC circuit consists of a pulse amplifier, Q1401, an integrator and a DC amplifier. The output of the pulse amplifier is directly coupled to the integrator. As the output pulses of the former are all of equal amplitude and width, the DC level obtained after integration is a direct measure of the pulse repetition frequency. Thus, should the squitter rate increase, the integrator output will increase, the end result being a decrease in noise output from the IF amplifier and a consequent reduction in squitter rate.

3.5.3 The DC amplifier, Q1402 through Q1405, uses a differential configuration. Low leakage silicon transistors are utilized throughout so that changes in leakage current with temperature do not appreciably effect the DC operating point, while emitter degeneration (provided by R1408 and R1409) and the compound connection stabilize the DC gain and DC operating point against changes in the common emitter DC current gain, h_{FE}, with temperature and between units. A differential configuration is utilized in order to compensate for the variation of base emitter voltage and its consequent effect on the DC operating point with temperature. The complementary compound connection that is utilized is preferable to a standard Darlington configuration since the number of base emitter junctions in series with the signal is halved. The squitter rate is set at 2700 pps by adjusting the DC voltage in the base circuit of Q1405 by means of potentiometer R1412.

3.5.4 The output of the differential amplifier is coupled through a compound connected emitter follower, Q1406 and Q1407, to the IF amplifier AGC line. As before, a complementary compound configuration is used in order to provide temperature stability for both operating point and gain.

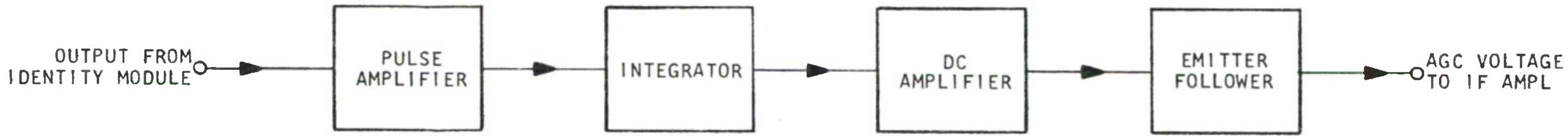


Figure 11. I. F. Amplifier A.G.C.

SECTION 3.6

BEARING CIRCUITS

(See Figures 12, 13, 14 and
Schematics T2319448, T2319443, and T2319452)

3.6.1 The bearing circuits generate the reference bursts and assign them priority over the identity/distance reply signal obtained from the identity module. The reference bursts are generated by means of a ring-round technique using the encoding delay line. This method permits the operation of all transistors as pure switches and can be made considerably less susceptible to temperature variation than the conventional pulsed oscillator type of marker burst generator.

3.6.2 Identity/distance reply pulses from the identity module drive the precedence gate, Q1803, which serves to both invert the signal so that its output is negative and provides a means of inhibiting it during the generation of marker bursts. The output of the precedence gate, differentiated by C1808 and R1816, triggers the delay line driver, a conventional monostable multivibrator, Q1804 and Q1805. CR1806 serves to disconnect the base-emitter junction of Q1804 from the full collector swing of Q1805 and hence prevents zenering of that junction. The multivibrator output is AC coupled through C1811 to the driver amplifier, Q1806, the latter in turn injecting a 50 volt pulse onto the delay line.

3.6.3 In order to obtain a stable bearing reference, it is necessary to select the zero cross-over point of the reference burst trigger obtained from the antenna, and from it produce a fast trigger which can be used to fire the gate multivibrator. Q1601 is biased so that it amplifies and clips the positive portion of the north reference trigger. After further amplification by Q1602, the signal is differentiated and the trailing edge corresponding to the zero cross-over point used to trigger the gate multivibrator and a thirty microsecond multivibrator contained in the delay line driver module.

3.6.4 Both the north gate and the 30 microsecond multivibrator are of the collector coupled RC type used elsewhere in the receiver-coder, but utilize an additional diode in the timing circuit so that a fast negative going pulse can be obtained. The diode isolates the collector of the normally off transistor from the timing capacitor and thus prevents the capacitor charging current from flowing through the load. While this arrangement increases the multivibrator recovery time (the capacitor must charge through R1617 instead of the parallel combination of R1617 and R1618), this is no problem as the duty cycle is low.

3.6.5 As has been stated in paragraph 3.6.2, the negative going output of the north gate multivibrator, Q1603 and Q1604, inhibits the identity/distance reply signal for 375 microseconds by reverse biasing Q1803. As the same delay line is used for system delay, pulse pair coding and reference burst coding, the line must be cleared of all identity/distance reply pulses before the ring-round circuit is enabled. This function is performed by the 30 microsecond multivibrator which inhibits the first 30 microseconds of the north gate in the base circuit of Q1605. The waveform at the collector of Q1605 is a pulse 345 microseconds wide, the leading edge of which is delayed 30 microseconds with respect to the zero cross-over point of the north reference trigger.

3.6.6 The north reference burst is initiated by differentiating the output of the 30 microsecond multivibrator by means of C1607 and Q1607, selecting the trigger corresponding to the trailing edge and injecting it into the north "AND" gate (CR1607 through CR1609). The latter, having been enabled by the north reference gate, couples the trigger to the delay line driver, Q1804 and Q1805. The latter, in turn, impresses a pulse upon the encoding delay line. Thirty microseconds later the pulse appears at the north ring-round tap of the line and after amplification is reinjected into the north "AND" gate. As the enabling north reference burst gating signal is still present, the delayed pulse is permitted to pass through the "AND" gate and retrigger the delay line driver multivibrator. This in turn impresses another pulse upon the encoding delay line and the process is repeated every 30 microseconds until the gate multivibrator turns off. The duration of the north gate multivibrator is set at 375 microseconds and can be allowed to vary ±15 microseconds from this value before losing or gaining a pulse pair in the reference burst. The actual change experienced over the environmental range is far less than the allowable as may be seen from the test data listed in Appendix I.

3.6.7 The auxiliary reference burst is generated in a similar manner using the 24 microsecond tap of the encoding line. The auxiliary gate width is set at 162 microseconds and the same 30 microsecond multivibrator used to clear the delay line. There is no interaction between the two burst generators since the reference burst triggers do not occur simultaneously.

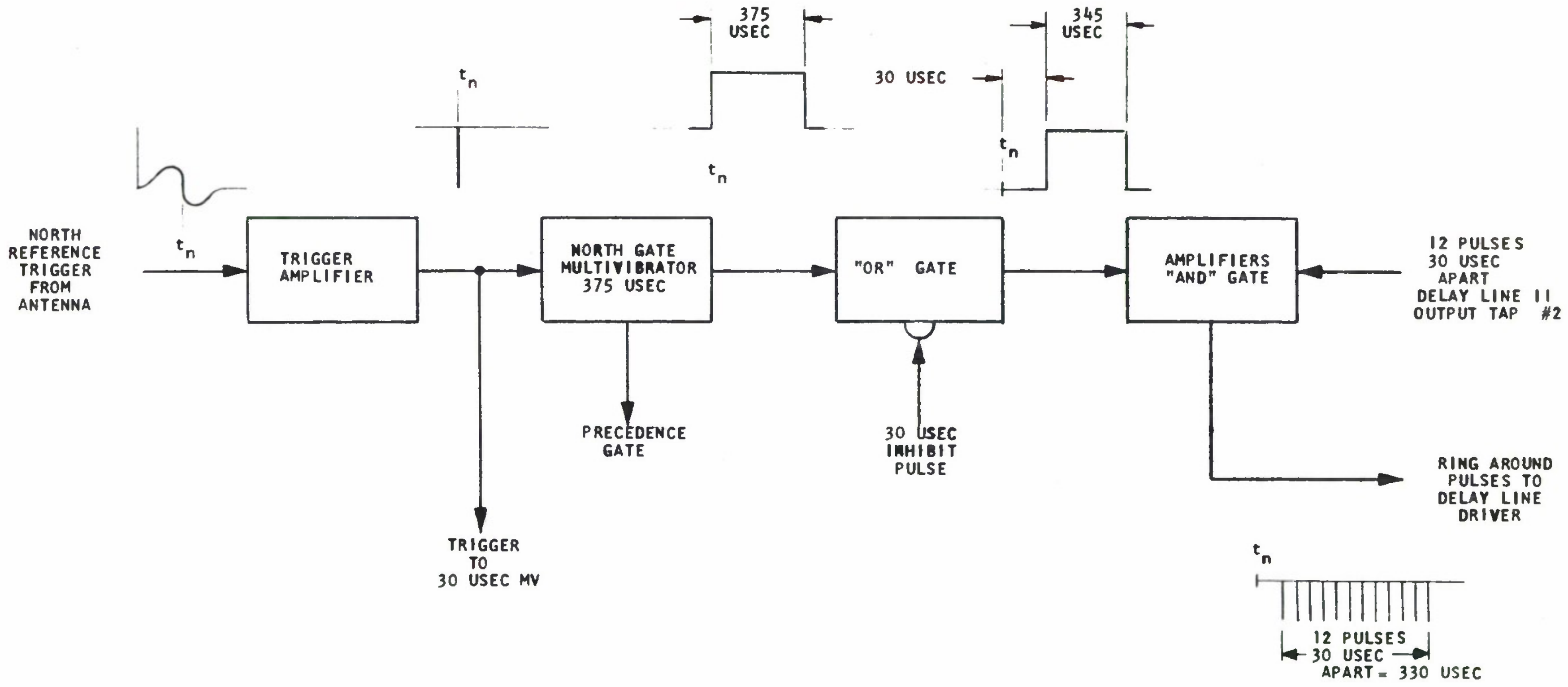


Figure 12. North Reference Burst Generator Module

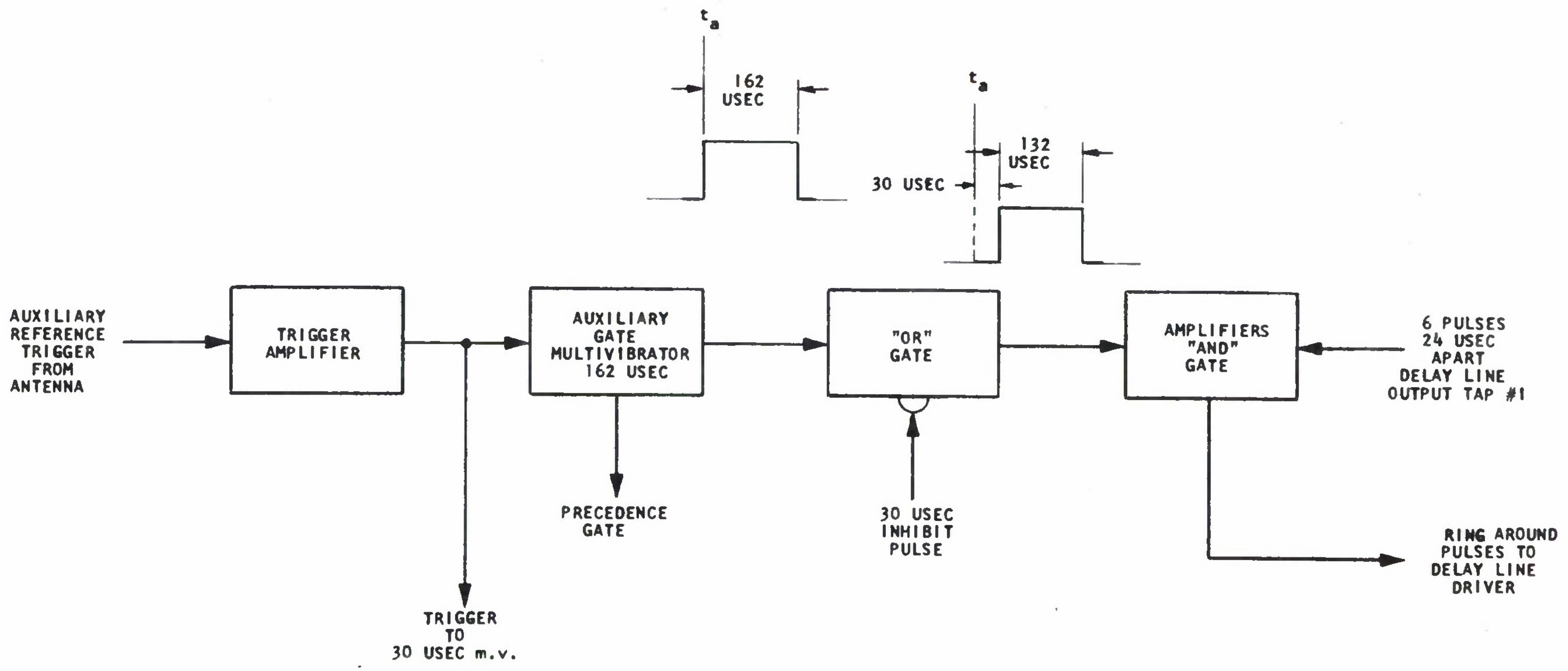


Figure 13. Auxiliary Reference Burst Generator Module

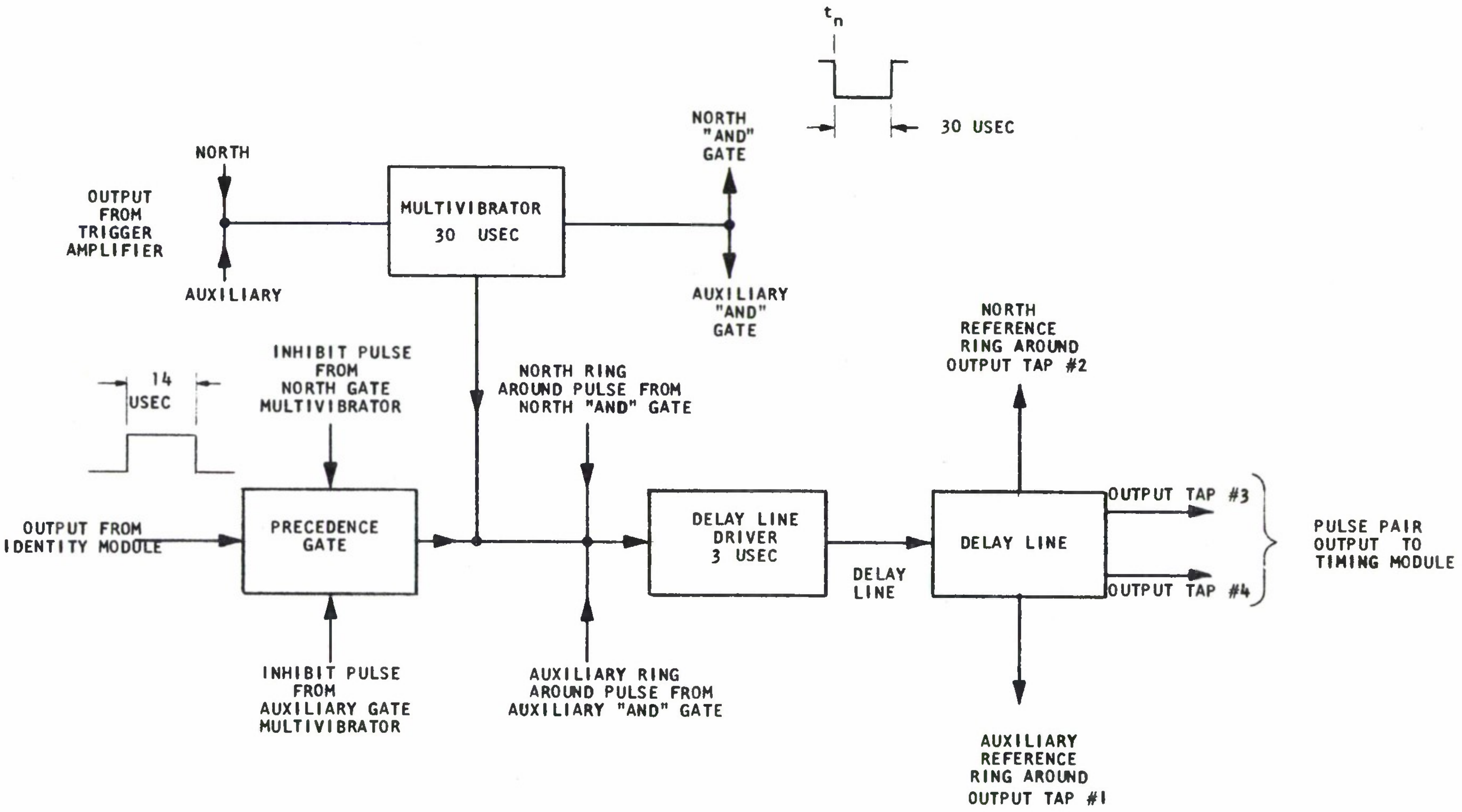


Figure 14. Delay Line Driver Module

SECTION 3.7

TIMING MODULE

(See Figure 15 and Schematic T2319446)

3.7.1 The timing module sets the over-all system delay, provides the pulse pair coding and generates the gate pulse used to blank the receiver and key the transmitter.

3.7.2 In addition to the two output taps required for the generation of the reference bursts, the encoding delay line contains two taps spaced 12 microseconds apart which provide the pulse pair coding and zero distance delay adjustments. These taps are mechanically arranged so that the fourth tap adjusts system delay, while the third, normally ganged with the fourth, can be independently moved to adjust pulse spacing. The output of each tap drives a pulse amplifier whose collector waveform in turn is differentiated and used to trigger independent 14 microsecond collector coupled RC multivibrators. The two 14 microsecond pulses, spaced 12 microseconds apart, are combined in an "OR" gate consisting of CR1904, CR1908 and R1927, to form the 26 microsecond gate pulse. The high output impedance of the "OR" gate makes it unsuitable for driving the gate modulator and thus an emitter follower, Q1910, is used to provide the necessary impedance transformation. Although the individual transmitted shaped pulses have a half-amplitude width of only three to four microseconds, the transmitter is gated on for 26 microseconds so that the skirts of the shaped pulses are not clipped.

3.7.3 The outputs of each of the 14 microsecond multivibrators are also differentiated and combined by an "OR" gate consisting of diodes CR1909, CR1910, and R1936 in order to trigger a 4 microsecond RC coupled multivibrator Q1907, Q1908 and so produce a 12 microsecond spaced pulse pair. The 4 microsecond multivibrator then drives an emitter follower Q1909, the latter providing a low source impedance to the filter in the shaper. This stage was initially biased in a cutoff condition, but it was found that overshoot occurred because of the inductive load. By idling a 2 ma collector current through the transistor and thus ensuring a low impedance source at all times, the percentage overshoot was reduced considerably.

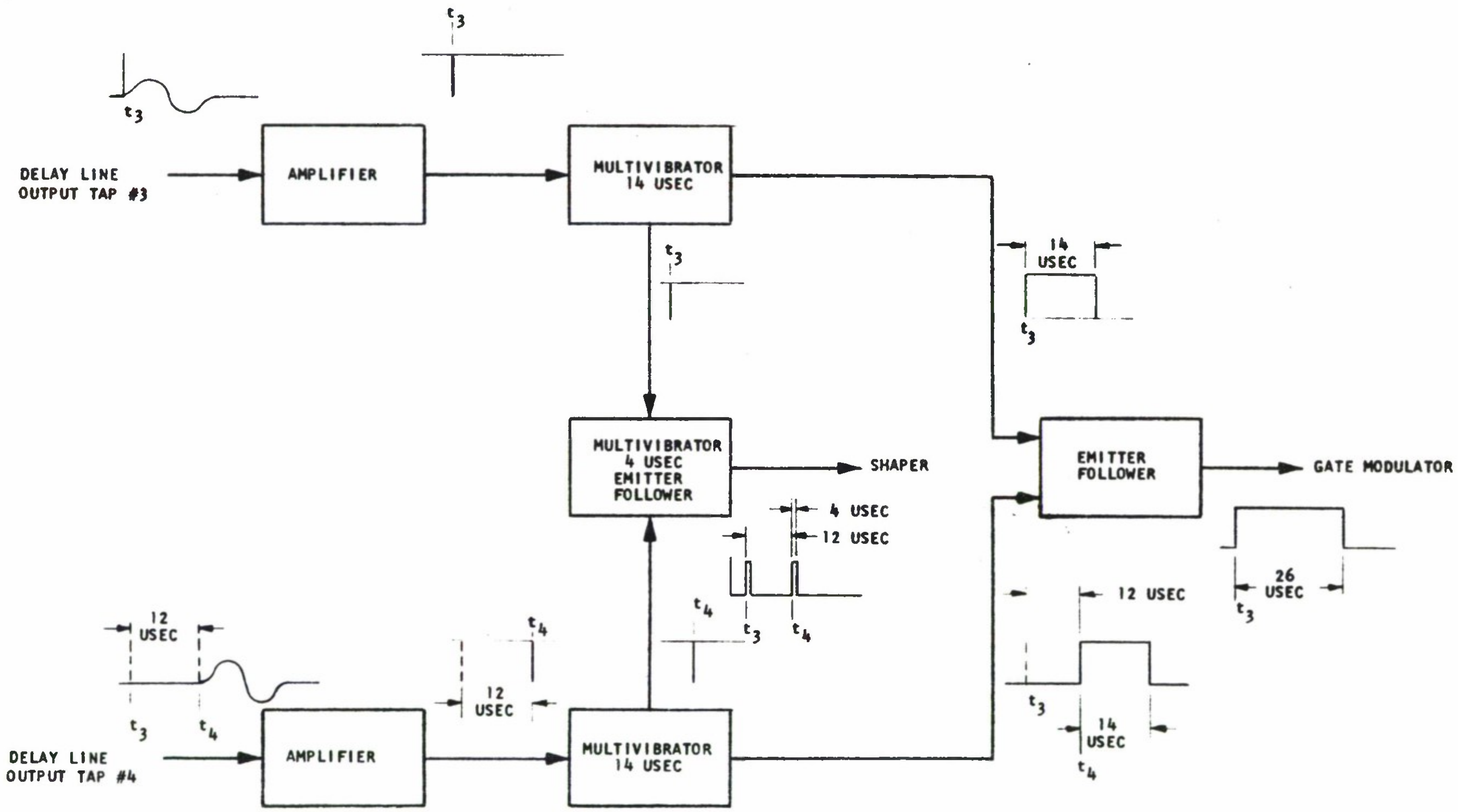


Figure 15. Timing Module

SECTION 3.8

SHAPER MODULE

(See Figure 16 and Schematic G2319449)

3.8.1 The shaper module generates the waveform required by the shaped pulse modulator in order to minimize the sideband energy that is transmitted. Rectangular pulse pairs from the timing module are fed into an 11 pole maximally flat time delay low pass filter, the output of which is a series of gaussian-like pulse pairs that are supplied to the amplitude selector.

3.8.2 The amplitude selector provides 3 outputs, one the entire gaussian pulse, the other two the peak of the gaussian pulse with the base clipped off at adjustable levels. The first output, a tap on the emitter resistor, R2003, of the input emitter follower which isolates the filter, is arranged so that the amplitude of the gaussian pulse available at R2022 can be varied. The other two outputs are formed by the use of diode clippers. Considering CR2003 a short circuit, the operation of the diode clipper CR2001, CR2006 is as follows:

3.8.3 Since the DC voltage across R2004 is determined by R2011 and is larger than that across R2003, CR2001 will normally be back-biased and CR2006 forward-biased. As the gaussian output pulse from the filter rises, the emitter of Q2001 rises until the input voltage to CR2001 exceeds that due to R2011. CR2001 will then conduct and CR2006 disconnect, removing the effective impedance due to R2011 and C2012. The net result is that the peak of the gaussian pulse can be selected from a base line determined by the setting of R2011. (The purpose of CR2003 is to temperature compensate the base-emitter junction of Q2001.) The clipped pulse so produced is then applied through C2007 to R2013, where it is resistively mixed with the gaussian pulse from R2005 and the output of the second diode clipper, then applied to the operational amplifier Q2002 and Q2003.

3.8.4 The amplifier, a feedback amplifier pair, with feedback from the emitter of Q2003 to the base of Q2002, was selected because its inherent low input impedance causes a virtual ground to appear at the base of Q2002. The inputs thus act as current sources, since the values of R2008, R2010 and R2022 are much larger than the input impedance. The output of the operational amplifier is coupled to an emitter follower Q2004 so that the low input impedance of the shaped pulse modulator can be driven.

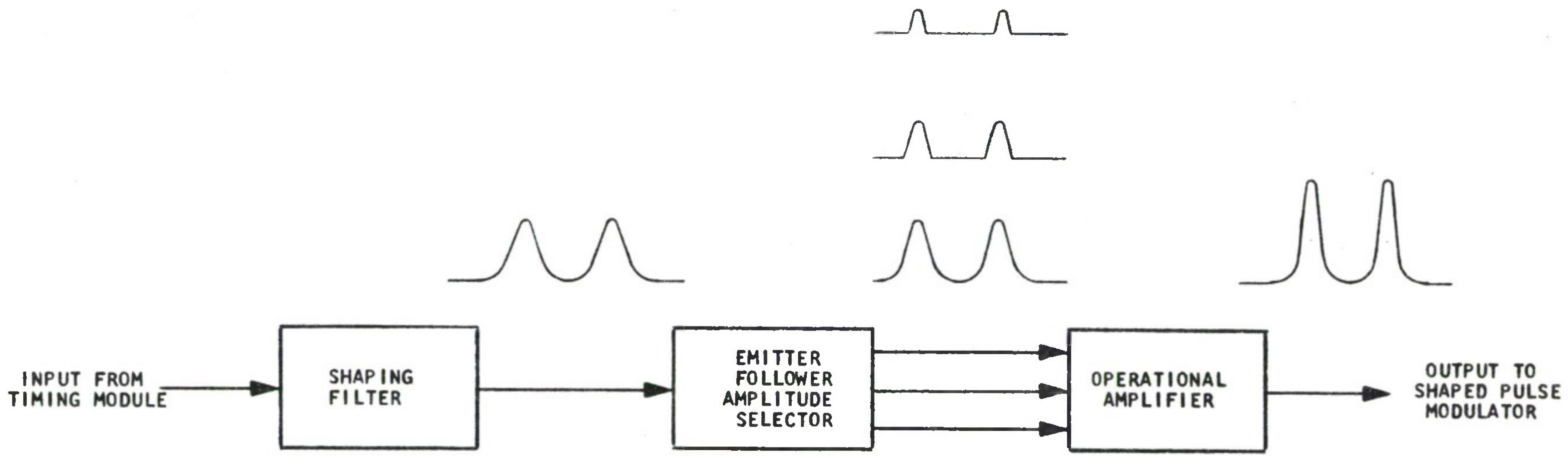


Figure 16. Shaper Module

SECTION 4

TEST RESULTS

4.1 IF Amplifier

4.1.1 A maximum gain of 100 db is available from the ten IF stages. The shrinkage of bandwidth and shift in center frequency with AGC, previously described in the Scientific Report, January, 1963, figure 3, is reduced somewhat by having five stages share the AGC action so that Ferris response, monitored at the narrow-band test point (see schematic D2319450) is relatively unaffected by changes in AGC or by saturation of the IF strip due to overdriving the transistors.

4.1.2 A balanced mixer assembly similar to that used in the AN/TRN-17 receiver was connected to the receiver coder and the system sensitivity determined. During this test, the mixer crystal current was adjusted for maximum sensitivity. The results are indicated below:

TABLE 4

Receiver Sensitivity

Mixer Crystal Type	Crystal Current	Sensitivity (Int. Signal Level for 60% Replies)
1N21B	5 mA	-91 dbm
1N21EM	3 mA	-91.7 dbm

4.2 Decoder

4.2.1 The gain stability of the video amplifier (Q1201 and Q1202) located in the decoder module was tested over the temperature range and the results listed in Table 5 below:

TABLE 5

Video Amplifier - Gain Stability

Temp °C	e_i volts	f kc	e_o volts	K_v e_o/e_i	$\frac{K_v}{K_v\ +25°C}$	ΔK db
+25	0.30	10	7.20	24.0	-	-
-40	0.30	10	6.20	20.7	.863	-1.3
+80	0.30	10	6.60	22.0	.916	-0.8

4.2.2 The ability of the decoder to reject improperly coded interrogations was checked by feeding a rectangularly shaped pulse pair into the decoder and adjusting the pulse spacing until there were no decodes. The results are tabulated in Table 6.

TABLE 6

E_{in} volts	Pulse Width usec	Pulse Spacing Rejected by Decoder
0.5v	2.7	9.7 usec ≤ Spacing ≥ 14.6 usec

4.3 Identity Module

4.3.1 The identity tone must be phase locked to within ±50 microseconds of the auxiliary reference bursts. As the 1350 cps antenna tone is mechanically locked in phase to the reference bursts triggers, any deviations in the triggering point on the input 1350 cycle signal will change the phasing. The shift in the selected triggering point over the temperature range is tabulated below.

TABLE 7

E_{in} Vpk-pk	Temp °C	Change in Triggering Point
20	+25	0 usec
20	-40	-1 usec
20	+80	0 usec

4.3.2 The equalizing pulse spacing is determined by the equalization multivibrator and should be 100 ±10 microseconds.

TABLE 8

Temp °C	Equal. MVB Width usec	ΔW usec	ΔW %
+25	100.0	-	-
-40	100.9	+0.9	+0.9
+80	99.4	-0.6	-0.6

4.4 IF AGC Module

4.4.1 The IF AGC Module maintains the squitter rate at 2700 ±90 pulses per second over the environmental temperature range. The squitter rate was monitored using a Hewlett-Packard 524C counter, the readings being obtained using the 10 second gate.

TABLE 9

Squitter Rate
(AGC Module in Chamber)

	+25°C	-40°C	+80°C
1.	2702 pps	2718 pps	2686 pps
2.	2702	2718	2686
3.	2701	2717	2687
4.	2702	2717	2687
5.	2701	2718	2687
6.	2702	2717	2686
7.	2701	2717	2687
8.	2702	2717	2687
9.	2701	2718	2687
10.	2701	2717	2687
PRF Avg.	2702	2717	2687
Δ PRF	-	+15	-15

TABLE 10

Squitter Rate
(Identity Module in Chamber)

	+25°C	-40°C	+80°C
1.	2702	2684	2703
2.	2703	2684	2703
3.	2702	2687	2701
4.	2702	2688	2700
5.	2703	2683	2704
6.	2704	2687	2703
7.	2702	2690	2704
8.	2703	2684	2706
9.	2702	2686	2704
10.	2702	2685	2703
PRF Avg.	2703	2685	2703
Δ PRF	-	-18	0

TABLE 11

Squitter Rate
(Identity, AGC, and Decoder Modules in Chamber)

	+25°C	-40°C	+80°C
1.	2700	2641	2760
2.	2700	2642	2760
3.	2701	2644	2762
4.	2701	2641	2762
5.	2701	2640	2763
6.	2700	2642	2762
7.	2700	2641	2763
8.	2702	2641	2763
9.	2701	2642	2761
10.	2702	2642	2762
PRF Avg.	2701	2642	2762
Δ PRF	-	-59	+61

TABLE 12

Squitter Rate
(Identity, AGC, Decoder and IF Amplifier in Chamber)

	+25°C	-40°C
1.	2705	2645
2.	2701	2644
3.	2699	2647
4.	2699	2644
5.	2696	2646
6.	2696	2647
7.	2697	2645
8.	2693	2647
9.	2692	2642
10.	2693	2642
PRF Avg.	2697	2645
Δ PRF	-	-52

The loop was inoperative at +80°C and the cause was traced to the IF amplifier whose noise output dropped drastically at +50°C.

4.4 Squitter Distribution - The squitter distribution was checked using the approved AN/TRN-17 First Article Test Plan (ITTFL Spec A2207809). The results are plotted on the standard random pulse distribution curves and may be seen to fall well within the specification requirements.

4.5 Bearing Circuits

4.5.1 Reference Burst Coding - The stability of the reference burst circuits using a ring-round generating technique is basically the stability of the delay line. The bearing circuits were tested with the line both inside and outside the chamber and as may be seen from the data more satisfactory results were obtained with the line outside the chamber. The coding stability of the reference bursts was checked by allowing the circuit under test to free run while counting the frequency of oscillation. The use of this technique and a 10 second counting period results in a resolution at the 30 microsecond tap of about ±1 nanosecond.

TABLE 13

Stability of Auxiliary Reference Burst Coding

Temperature °C	Pulse Count (10 second period)	Pulse Coding usec	Δ Pulse Coding usec	Spec Limit usec
+25	420,525	23.78	-	-
-40	421,778	23.71	-0.07	±0.25
+80	416,140	24.03	+0.25	±0.25

TABLE 14

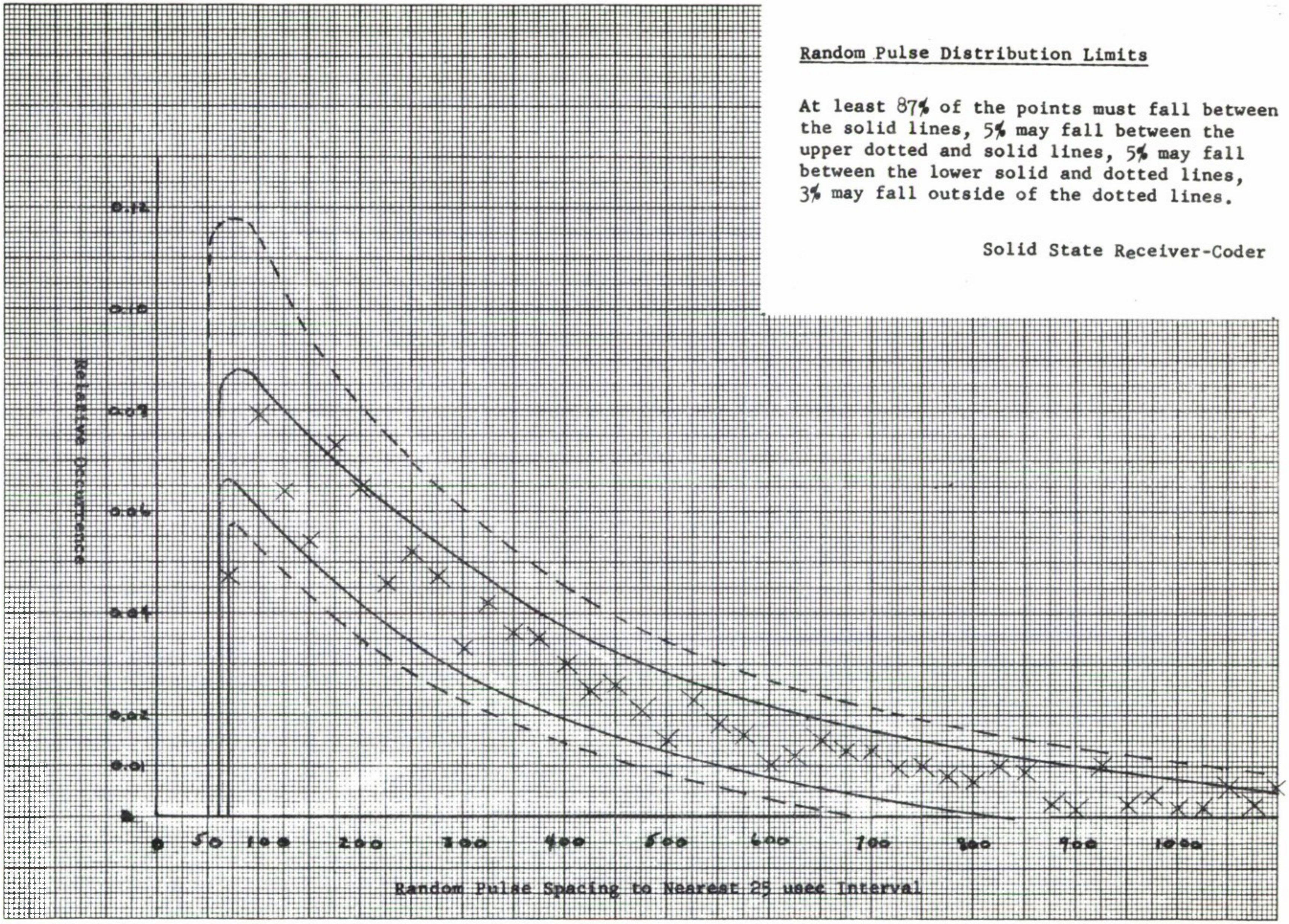
Stability of Auxiliary Reference Burst Coding
(Line Outside Chamber)

Temperature °C	Pulse Count (10 second period)	Pulse Coding usec	Δ Pulse Coding usec	Spec Limit usec
+25	420,477	23.78	-	-
-40	421,269	23.74	-0.04	±0.25
+80	419,608	23.83	+0.05	±0.25

TABLE 15

Stability of North Reference Burst Coding

Temperature °C	Pulse Count (10 second period)	Pulse Coding usec	Δ Pulse Coding usec	Spec Limit usec
+25	336,225	29.74	-	-
-40	337,716	29.61	-0.13	±0.30
+80	331,352	30.18	+0.44	±0.30



Random Pulse Distribution Limits

At least 87% of the points must fall between the solid lines, 5% may fall between the upper dotted and solid lines, 5% may fall between the lower solid and dotted lines, 3% may fall outside of the dotted lines.

Solid State Receiver-Coder

TABLE 16

Stability of North Reference Burst Coding
(Line Outside Chamber)

Temperature °C	Pulse Count (10 second period)	Pulse Coding usec	△ Pulse Coding usec	Spec Limit usec
+25	336,128	29.750	-	-
-40	336,182	29.746	-0.004	±0.30
+80	335,764	29.78	+0.03	±0.30

4.5.2 Due to the method of burst generation, there are no severe stability requirements on the gate generators. The north gate multivibrator may drift by ±15 microseconds before effecting the pulse count in the reference burst.

TABLE 17

Stability of North Reference Gate MVB

Temperature °C	Pulse Width usec	△ PW usec	Allowable △ PW (usec)
+25	383.1	-	-
-40	387.7	+4.6	±15
+80	382.8	-0.3	±15

TABLE 18

Stability of Auxiliary Reference Gate MVB

Temperature °C	Pulse Width usec	△ PW usec	Allowable △ PW (usec)
+25	168.3	-	-
-40	167.2	-1.1	±12
+80	167.5	-0.8	±12

4.5.3 Since it is the trailing edge of the delay line clearing multivibrator (30 microsecond MVB) which initiates the generation of the reference bursts, a change in the width of the multivibrator will cause an apparent bearing shift.

TABLE 19

Stability of 30 Microsecond MVB

Temperature °C	Pulse Width usec	△ PW usec	Apparent Shift in Bearing degrees
+25	31.53	-	-
-40	31.68	+0.15	0°0'2.9"
+80	31.40	-0.13	0°0'2.5"

4.6 Timing Module

4.6.1 System Delay and Coding - In conjunction with the encoding delay line, the timing module sets the over-all system delay and provides the pulse pair coding. Hence, taps III and IV of the delay line were tested using the same ring-round technique used in measuring the stability of the bearing circuits. Again this test was performed with the line both inside and outside the chamber.

TABLE 20

Delay and Pulse Pair Coding Stability

	Tap III		Tap IV				
Temp °C	Pulse Count (10 sec Period)	Delay usec	Pulse Count (10 sec Period)	Delay usec	Δ Delay (at Tap IV) usec	Pulse Pair Coding usec	Δ Pulse Pair Coding usec
+25	391,354	25.55	266,692	37.50	-	11.95	-
-40	392,752	25.46	267,253	37.42	-0.08	11.96	+0.01
+80	386,550	25.87	263,333	37.97	+0.47	12.10	+0.15

TABLE 21

Delay and Pulse Pair Coding Stability
(Line Outside Chamber)

	Tap III		Tap IV				
Temp °C	Pulse Count (10 sec Period)	Delay usec	Pulse Count (10 sec Period)	Delay usec	Δ Delay (at Tap IV) usec	Pulse Pair Coding usec	Δ Pulse Pair Coding usec
+25	391,475	25.54	266,594	37.51	-	11.97	-
-40	393,049	25.44	266,850	37.47	-0.04	12.03	+0.05
+80	390,323	25.62	266,406	37.54	+0.03	11.92	-0.05

4.6.2 The timing module also generates the gate pulses used for keying the transmitter and provides a rectangular pulse pair to the shaper. The results of temperature tests performed on these circuits are tabulated in the following tables:

TABLE 22

Gate MVB #1 Stability

Temperature °C	Pulse Width usec	Δ Pulse Width usec	% $\frac{\Delta PW}{PW\ +25°C}$
+25	14.28	-	-
-40	14.25	-0.03	-0.2
+80	14.25	-0.03	-0.2

TABLE 23

Gate MVB #2 Stability

Temperature °C	Pulse Width usec	Δ Pulse Width usec	% $\frac{\Delta PW}{PW\ +25°C}$
+25	14.22	-	-
-40	14.26	+0.04	+0.28
+80	14.10	-0.12	-0.85

TABLE 24

Shaper Input Stability

Temperature °C	Pulse Width usec	Δ Pulse Width usec	% $\frac{\Delta \text{PW}}{\text{PW} +25°\text{C}}$
+25	3.00	-	-
-40	3.04	+0.04	+1.33
+80	3.03	+0.03	+1.00

4.7 Shaper Module - The shaper module generates the waveform required by the shaped pulse modulator in order to minimize the sideband energy that is transmitted. The results of temperature tests performed on this module are summarized in the table below.

TABLE 25

Shaper Filter Output Pulse

Temperature °C	Shaped Pulse Amp. volts	Shaped Pulse Width usec	Change in Delay Through Shaper usec
+25	16.3	3.95	-
-40	16.1	3.90	-.05
+80	16.4	4.00	0

SECTION 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Since completion of the work described in this report early in 1963, ITTFL has been engaged in the development of a solid state TACAN receiver coder for the U. S. Navy as part of NObsr 89181 (the AN/URN-20 program). This work has taken the design techniques developed during AF19(604)-8352 to the point where a manufactured unit using printed circuit cards and meeting a temperature range requirement of -28 to +80°C is available. In order to meet the extremely demanding requirements of NObsr 89181, a rather sophisticated approach had to be employed, and there is no doubt that if some relaxations in the area of delay stability and CW rejection could be made that a simpler IF amplifier could be developed. For tactical situations where small size and simplicity are of importance, this is considered to be desirable.

5.2 With the successful development of solid state circuitry for TACAN ground equipment on this and other programs, it appears that the USAF, as the prime users of tactical TACAN ground equipment, is now in a good position to exploit the possibilities inherent in solid state circuitry for a truly tactical equipment.

5.3 Since the requirements for a tactical TACAN ground equipment are different from those of a fixed (terminal area) TACAN ground equipment, it appears that the USAF should also undertake developments in the latter area, with particular emphasis upon the development of a terminal area TACAN antenna.

APPENDIX I

INSTALLATION AND ALIGNMENT OF RECEIVER CODER

1. Installation

1.1 The solid state TACAN receiver-coder described in this report has been made physically and electrically interchangeable with the existing AN/TRN-17 receiver-coder. To install this unit in an AN/TRN-17 cabinet the following procedure should be followed:

1.2 Remove the cabinet cable harnesses from the terminal strips located at the rear of the AN/TRN-17 receiver coder drawer and at the meter panel at the front of the drawer.

1.3 Disconnect the coaxial cable from the IF amplifier input jack, J1, located in the timing module.

1.4 Remove the nuts at the bottom of the receiver coder which secures the slides to the frame of the drawer.

1.5 Lift the AN/TRN-17 receiver coder out of the slide brackets.

1.6 Remove the meter panel assembly from the AN/TRN-17 receiver coder and install it in the solid state TACAN receiver coder. A mounting hole has been provided for this purpose.

1.7 Place the solid state TACAN receiver coder in the vacated slide brackets and secure it in place using the nuts previously removed from the slides.

1.8 Reconnect both cabinet cable harnesses as required to the appropriate terminal boards. The wiring at the rear panel of the solid state receiver coder is schematically represented in drawing B2319453.

2. Operation

2.1 The solid state receiver coder has been designed to operate within the existing AN/TRN-17 transponder cabinet and as such can be made to operate in conjunction with the AN/TRN-17 Control and Transfer unit.

3. Alignment and Field Adjustment

3.1 The solid state receiver coder has been pre-aligned and may be operated immediately upon installation. As an aid in field maintenance of the receiver coder as installed in an AN/TRN-17, the following alignment procedures are included:

3.2 IF Amplifier

3.2.1 Tuning of the IF amplifier may be accomplished by the use of a swept frequency oscillator as shown in Figure 17. A demodulator probe, with low shunt capacity and a flat frequency response, Figure 18, is used to observe the base signal of each stage, starting at the input stage and advancing down the strip, the variable attenuator being adjusted at each step in order to keep the signal small enough to prevent saturation of all stages prior to that being tuned. Both coils of the interstage network feeding into the base of the stage being observed are adjusted alternately for the desired response shape, while occasionally the coupling networks have to be readjusted based on the response observed in subsequent stages. The output stage is aligned by detuning the Ferris high-Q resonant circuit and adjusting the last coupling network for a transitional response as observed at the wide-band test point.

3.2.1.1 The Ferris discriminator is aligned using the test setup shown in Figure 19. By measuring the detected DC level at the narrow-band test point and adjusting the tuning capacitor for f_o = 63 MC ±5 KC and the coupling capacitor for BW 3 db = 400 KC ±10 KC the Ferris response is established. Operational experience to date indicates, however,that the BW at -6 db should be changed to a nominal value of 700 KC.

3.2.1.2 Due to the complexity of the procedure, the alignment of the IF amplifier cannot be considered a field adjustment. Since the replacement of any one of the 3N35 transistors requires that the strip be realigned, field maintenance should be reduced to replacement of the entire defective IF amplifier chassis with a pre-aligned unit.

3.3 Decoder - No field adjustments are necessary.

3.4 Identity

3.4.1 The identity module contains three monostable multivibrators, the widths of which must be adjusted. In each case the AN/TRN-17 oscilloscope may be internally synchronized and the collector waveform of the normally conducting transistor viewed.

3.4.1.1 Equalization MV - place the oscilloscope probe on the collector of Q1303 and adjust R1312 for a pulse width of 100 microseconds (measured at the 50% amplitude points of the leading and trailing edge).

3.4.1.2 Output MV - place the oscilloscope probe on the collector of Q1305 and adjust R1324 for a pulse width of 14.0 microseconds.

3.4.1.3 Dead-Time MV - the dead time may be adjusted over a 20 to 65 microsecond range. Place the oscilloscope probe on the collector of Q1307 and adjust R1332 for a pulse width of (60 - 14) or 46 microseconds.

3.5 IF Amplifier AGC Module - Adjust R1412 for an identity output pulse repetition frequency of 2700 pps using an external digital counter. (Provision for checking this internally as in the AN/TRN-17 has not been provided.)

3.6 Bearing Module

3.6.1 In the bearing module there are three monostable multivibrators which must be adjusted. In each case the collector waveform of the normally conducting transistor is observed by means of the AN/TRN-17 oscilloscope.

3.6.1.1 North Gate Multivibrator (North Reference Burst Generator) - Turn the sync selector switch on the AN/TRN-17 test unit to the north trigger position. Place the oscilloscope probe on the collector of Q1603 and adjust R1608 for a pulse width of 375 microseconds.

3.6.1.2 Auxiliary Gate Multivibrator (Auxiliary Reference Burst Generator) - Turn the sync selector switch to the auxiliary trigger position. Place the oscilloscope probe on the collector of Q1703 and adjust R1708 for a pulse width of 162 microseconds.

3.6.1.3 30 microsecond Multivibrator (Delay Line Driver) - Turn the test unit sync selector switch to the auxiliary trigger position. Place the oscilloscope probe on the collector of Q1801 and adjust R1801 for a pulse width of 30 microseconds with the aid of 6 microsecond markers from the test unit.

3.6.2 The two taps on the delay line which control the pulse spacing in the burst can now be positioned with the use of 6 microsecond markers from the test unit. Place the oscilloscope probe on the collector of Q1806 (delay driver output).

3.6.2.1 Auxiliary Reference Burst - Turn the test unit sync selector switch to the auxiliary trigger position. The pulse spacing, measured from the leading edge half-amplitude point of one pulse to the leading edge half-amplitude point of the next is adjusted to 24 microseconds by moving tap J1 on the delay line.

3.6.2.2 North Reference Burst - Turn the test unit sync selector switch to the north trigger position. The pulse spacing should be adjusted to 30 microseconds by moving tap J2.

3.7 Timing Module

3.7.1 There are three multivibrators in the timing module which must be adjusted. In each case the AN/TRN-17 oscilloscope is internally synchronized and the collector of the conducting transistor observed.

3.7.1.1 14 microsecond Multivibrators - Place the oscilloscope probe on the collector of Q1902 and adjust R1907 for a pulse width of 14 microseconds. Place the probe on the collector of Q1905 and vary R1919 for a width of 14 microseconds.

3.7.1.2 4 microsecond Multivibrator - Place the oscilloscope probe on the collector of Q1907 and adjust R1933 for a pulse width of 4 microseconds.

3.7.2 The taps J3 and J4 in the delay line adjust the pulse pair spacing and beacon delay respectively. Turn the test unit sync selector to the auxiliary trigger position. Place the probe on the collector of Q1907 and adjust pulse pair spacing with the aid of 6 microsecond markers by changing the position of tap J3. The beacon delay adjustment is the same as that used on the AN/TRN-17.

3.8 Shaper - The only controls in the shaper to adjust are those in the amplitude selector. The detected RF is viewed on the oscilloscope, and R2003, R2007 and R2011 adjusted for the desired RF envelope. R2003 adjusts the skirts of the pulse while R2007 and R2011 provide peak shaping.

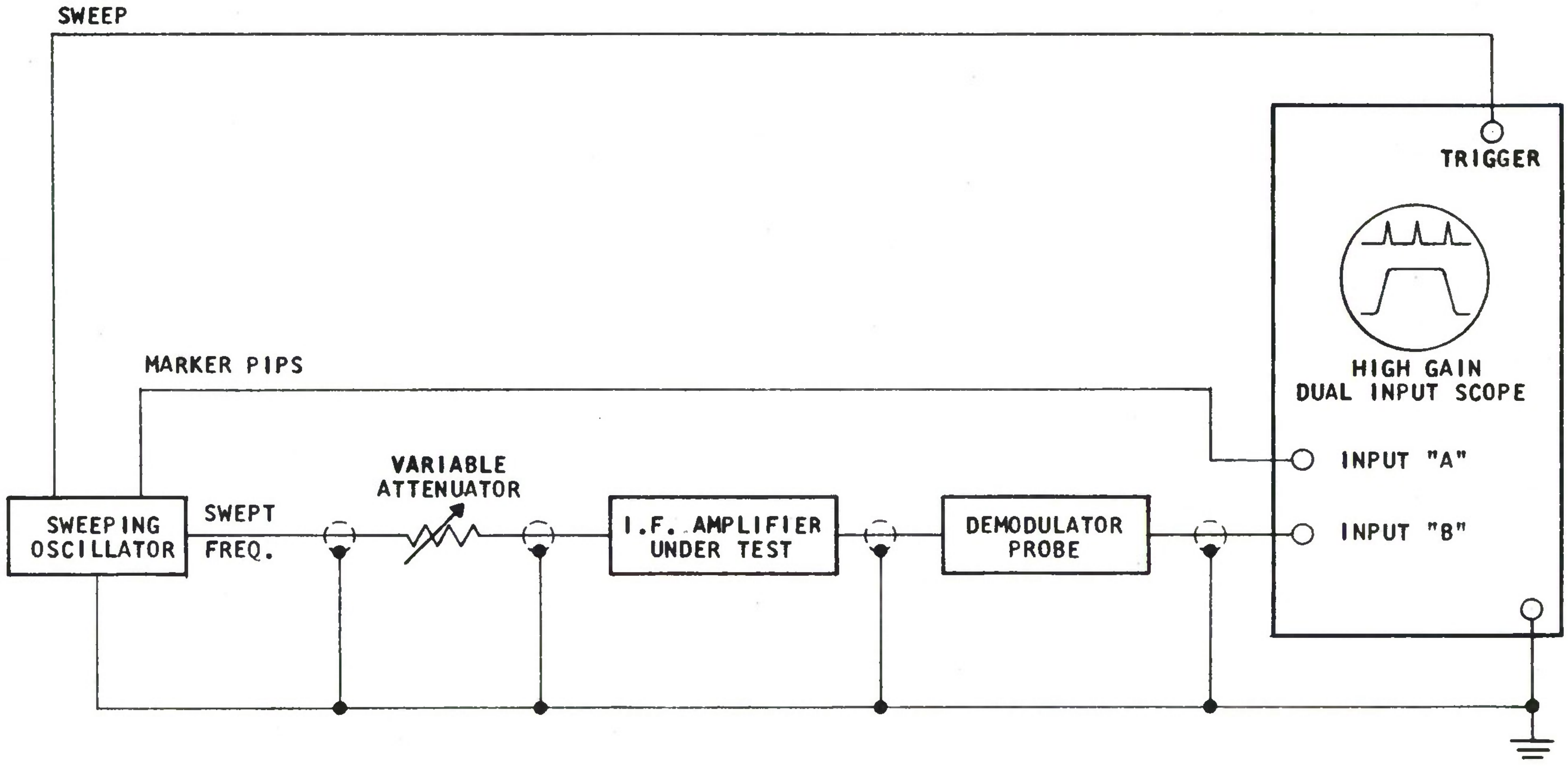


Figure 17. I. F. Amplifier Alignment Set Up

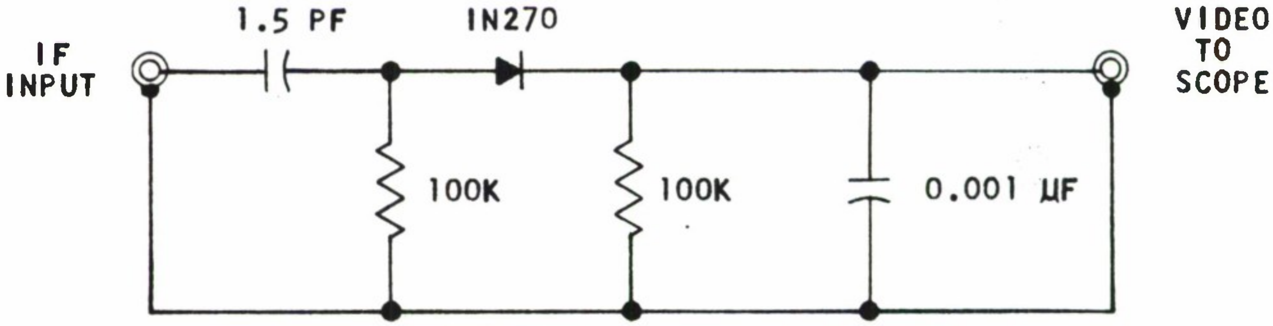


Figure 18. Demodulator Probe

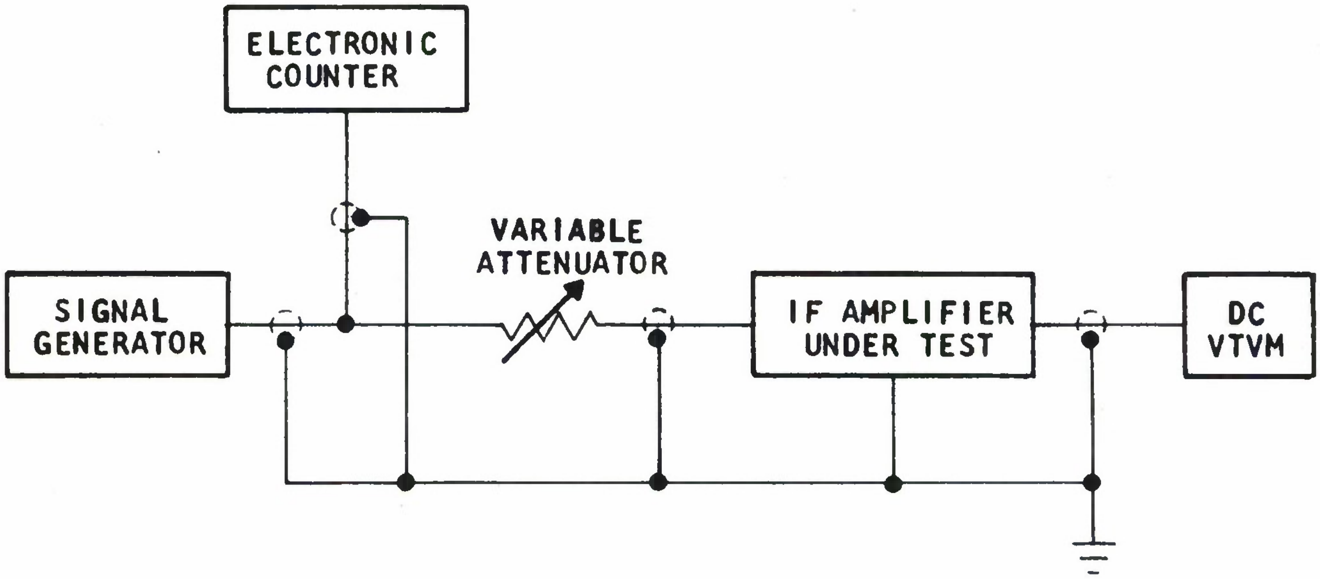
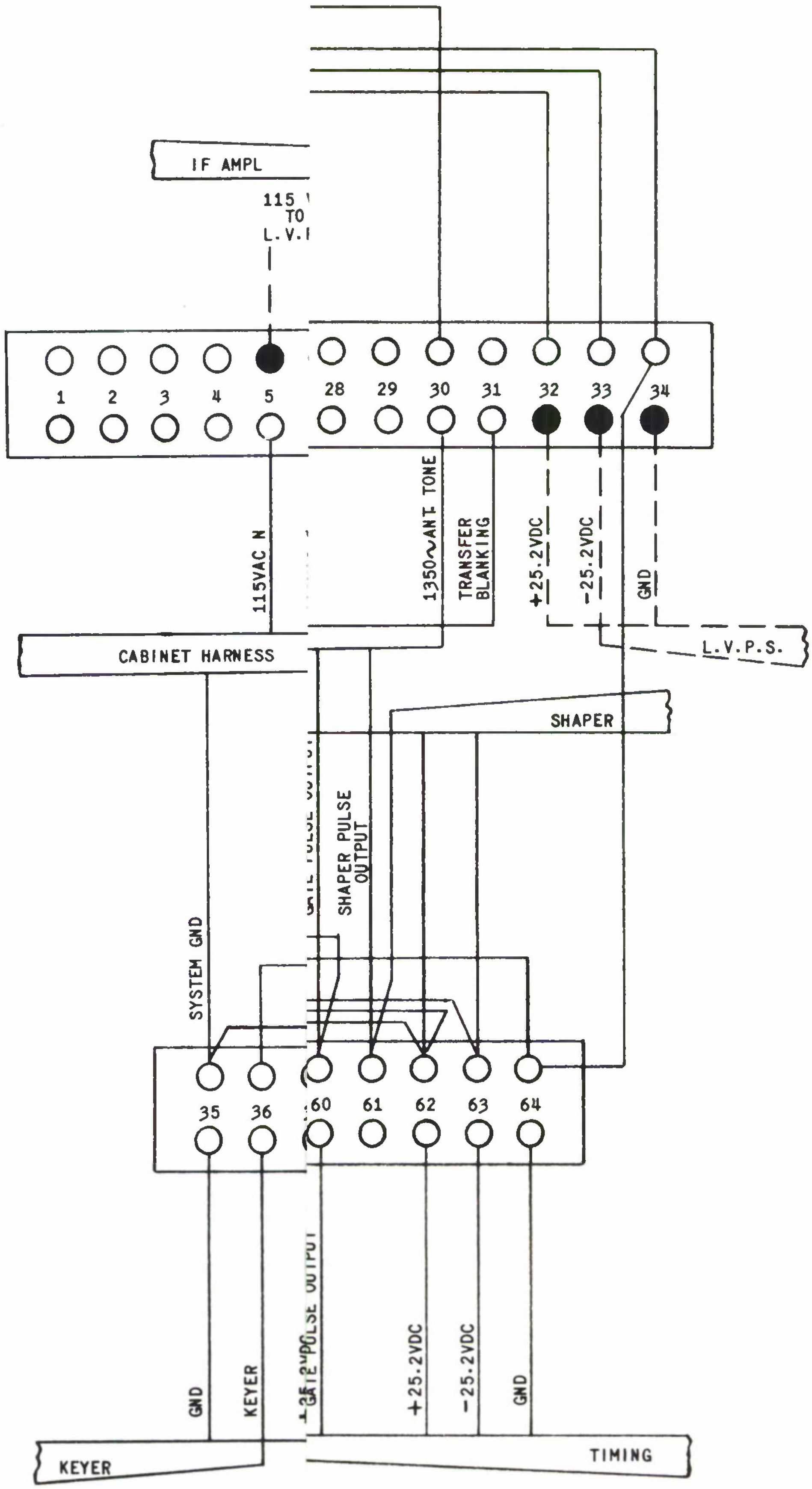
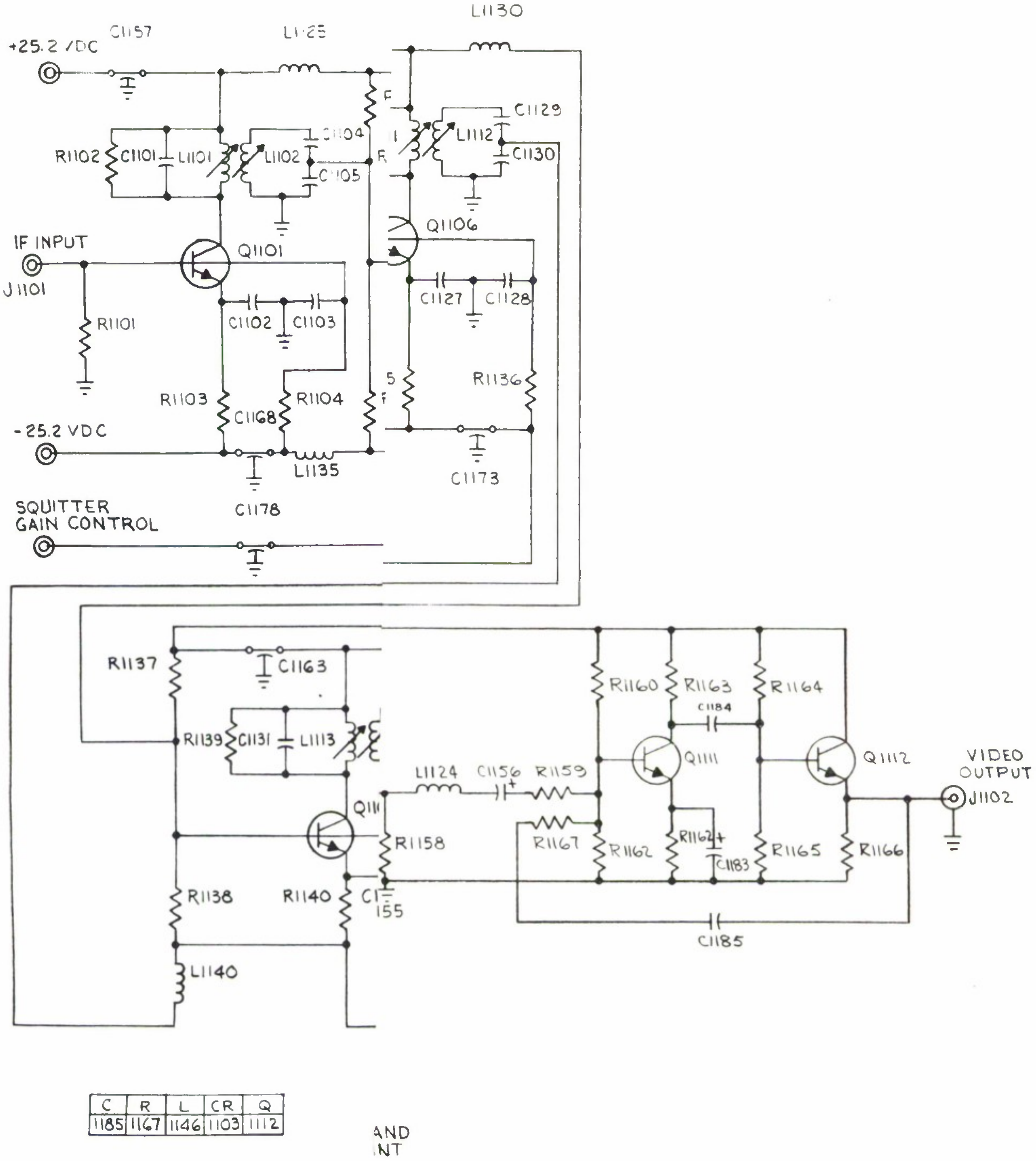


Figure 19. Ferris Discriminator Alignment Set Up



Solid State Tacan Receiver Coder Rear
Panel, Wiring Diagram B2319453



C	R	L	CR	Q
1185	1167	1146	1103	1112

63 MC I.F. Amplifier D2319450

PARTS LIST

IF AMPLIFIER

C1101	MIN-C-15-J	Glennite
C1102	CK60AW821M	
C1103	CK60AW821M	
C1104	MIN-C-39-J	Glennite
C1105	MIN-C-68-J	Glennite
C1106	MIN-C-15-J	Glennite
C1107	CK60AW821M	
C1108	CK60AW821M	
C1109	MIN-C-39-J	Glennite
C1110	MIN-C-68-J	Glennite
C1111	MIN-C-15-J	Glennite
C1112	CK60AW821M	
C1113	CK60AW821M	
C1114	MIN-C-39-J	Glennite
C1115	MIN-C-68-J	Glennite
C1116	MIN-C-15-J	Glennite
C1117	CK60AW821M	
C1118	CK60AW821M	
C1119	MIN-C-39-J	Glennite
C1120	MIN-C-68-J	Glennite
C1121	MIN-C-15-J	Glennite
C1122	CK60AW821M	
C1123	CK60AW821M	
C1124	MIN-C-39-J	Glennite
C1125	MIN-C-68-J	Glennite
C1126	MIN-C-15-J	Glennite
C1127	CK60AW821M	
C1128	CK60AW821M	
C1129	MIN-C-39-J	Glennite
C1130	MIN-C-68-J	Glennite
C1131	MIN-C-15-J	Glennite
C1132	CK60AW821M	
C1133	CK60AW821M	
C1134	MIN-C-39-J	Glennite
C1135	MIN-C-68-J	Glennite
C1136	MIN-C-15-J	Glennite
C1137	CK60AW821M	
C1138	CK60AW821M	
C1139	MIN-C-39-J	Glennite
C1140	MIN-C-68-J	Glennite
C1141	MIN-C-15-J	Glennite
C1142	CK60AW821M	
C1143	CK60AW821M	
C1144	MIN-C-39-J	Glennite
C1145	MIN-C-68-J	Glennite
C1146	MIN-C-15-J	Glennite
C1147	CK60AW821M	
C1148	CK60AW821M	
C1149	MIN-C-43-J	Glennite
C1150	CB86PD101J	

C1151	VCJ105A JFD Electronics
C1152	MIN-C-33-J Glennite
C1153	MIN-C-47-J Glennite
C1154	VC5 JFD Electronics
C1155	MIN-C-86-J Glennite
C1156	2 ufd, 50 WVDC, Cornell-Dubilier, Type NLW2-50
C1157 thru C1182	321-102 Erie Capacitor
C1183	30 ufd, 50 WVDC, Cornell-Dubilier, Type NLW30-50
C1184	10 ufd, 50 WVDC, Cornell-Dubilier, Type NLW10-50
C1185	0.1 ufd, 50 WVDC, Good-All, Type 601PE

CR1101	1N3066 Fairchild Semiconductor
CR1102	1N3066 Fairchild Semiconductor
CR1103	1N25 Texas Instruments

L1122 thru L1146	10203-20 Jeffers

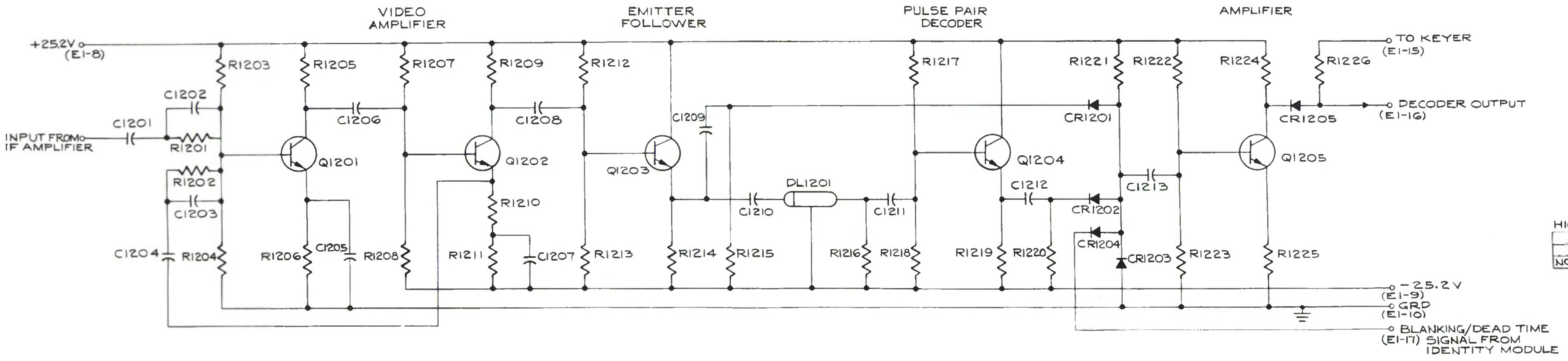
Coils L1101 thru L1121 were wound at ITTFL as follows:

L1101 L1103 L1105 L1107 L1109 L1111 L1113 L1115 L1117 L1119	8 Turns of 911016 Magnet Wire on Type PLST-P Coil Form - Cambridge Thermionic Corp.
L1102 L1104 L1106 L1108 L1110 L1112 L1114 L1116 L1118	6 Turns of 911018 Magnet Wire on Type PLST-P Coil Form - Cambridge Thermionic Corp.
L1120	4 Turns of 911018 Magnet Wire on Type PLST-P Coil Form - Cambridge Thermionic Corp.
L1121	CGW 681159 Corning Glass Works

Q1101 thru Q1110	3N35	Texas Instrument
Q1111	2N338	Texas Instrument
Q1112	2N338	Texas Instrument

XQ1101 thru XQ1110	69012-0424	Garlock
XQ1111	69012-0423	Garlock

R1101	RC07GF101J	R1135	RC07GF153J
R1102	RC07GF332J	R1136	RC07GF224J
R1103	RC07GF153J	R1137	RC07GF103J
R1104	RC07GF224J	R1138	RC07GF103J
R1105	RC07GF103J	R1139	RC07GF332J
R1106	RC07GF103J	R1140	RC07GF153J
R1107	RC07GF332J	R1141	RC07GF264J
R1108	RC07GF472J	R1142	RC07GF103J
R1109	RC07GF224J	R1143	RC07GF103J
R1110	RC07GF563J	R1144	RC07GF332J
R1111	RC07GF103J	R1145	RC07GF153J
R1112	RC07GF103J	R1146	RC07GF264J
R1113	RC07GF332J	R1147	RC07GF103J
R1114	RC07GF153J	R1148	RC07GF103J
R1115	RC07GF472J	R1149	RC07GF332J
R1116	RC07GF224J	R1150	RC07GF153J
R1117	RC07GF563J	R1151	RC07GF264J
R1118	RC07GF103J	R1152	RC07GF103J
R1119	RC07GF103J	R1153	RC07GF103J
R1120	RC07GF332J	R1154	RC07GF153J
R1121	RC07GF153J	R1155	RC07GF264J
R1122	RC07GF472J	R1156	RC07GF103J
R1123	RC07GF224J	R1157	RC07GF822J
R1124	RC07GF563J	R1158	RC07GF103J
R1125	RC07GF103J	R1159	RC07GF822J
R1126	RC07GF103J	R1160	RC07GF823J
R1127	RC07GF332J	R1161	RC07GF103J
R1128	RC07GF153J	R1162	RC07GF102J
R1129	RC07GF472J	R1163	RC07GF103J
R1130	RC07GF224J	R1164	RC07GF473J
R1131	RC07GF563J	R1165	RC07GF103J
R1132	RC07GF103J	R1166	RC07GF222J
R1133	RC07GF103J	R1167	RC07GF184J
R1134	RC07GF332J		



HIGHEST REFERENCE DESIGNATIONS

	C	CR	Q	R	DL
	1213	1205	1205	1226	1201
NOT USED					

Decoder Module, Schematic Diagram
G2319440

PARTS LIST

DECODER

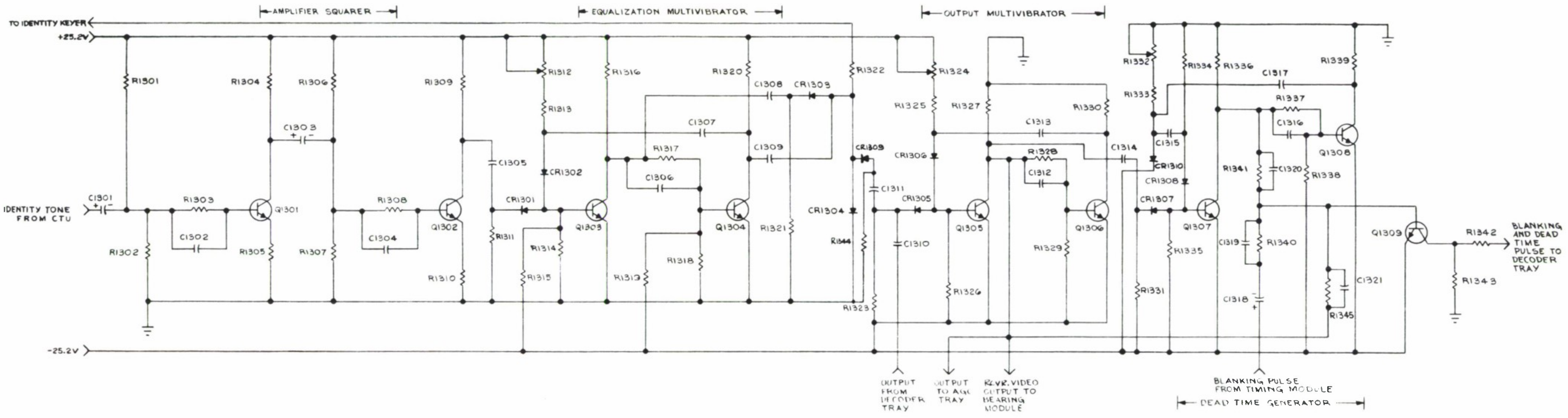
C1201	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1202	33 pf, ±5%, Glenco Corp, Type MIN-C-33J
C1203	6 pf, ±5%, Glenco Corp, Type MIN-C-6J
C1204	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1205	47 uf, ±20%, 35 VDCW, Sprague Type 150D
C1206	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1207	47 uf, ±20%, 35 VDCW, Sprague Type 150D
C1208	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1209	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1210	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1211	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1212	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE
C1213	0.1 uf, ±5%, 50 VDCW, Good-All Type 601PE

CR1201	1N251
CR1202	1N251
CR1203	1N251
CR1204	1N251
CR1205	1N251

DL1201	ITTFL #SK-TRN-17-2 PCA #DL2200L-12T-2255

Q1201	2N2219
Q1202	2N2219
Q1203	2N338
Q1204	2N338
Q1205	2N2219

R1201	RL07AD103J	R1214	RC07GF103J
R1202	RL07AD393J	R1215	RC20GF222J
R1203	RC07GF513J	R1216	RC20GF222J
R1204	RC07GF103J	R1217	RC07GF223J
R1205	RC07GF332J	R1218	RC07GF273J
R1206	RC07GF332J	R1219	RC07GF123J
R1207	RC07GF273J	R1220	RC20GF222J
R1208	RC07GF223J	R1221	RC07GF472J
R1209	RL20AD332J	R1222	RC07GF333J
R1210	RL07AD301J	R1223	RC07GF102J
R1211	RC07GF302J	R1224	RC07GF332J
R1212	RC07GF223J	R1225	RC07GF331J
R1213	RC07GF273J	R1226	RC07GF223J



NOTES
HIGHEST COMPONENT NUMBER

C	R	CR	Q
1321	1345	1309	1310

Identity Module, Schematic Diagram
T2319442

PARTS LIST

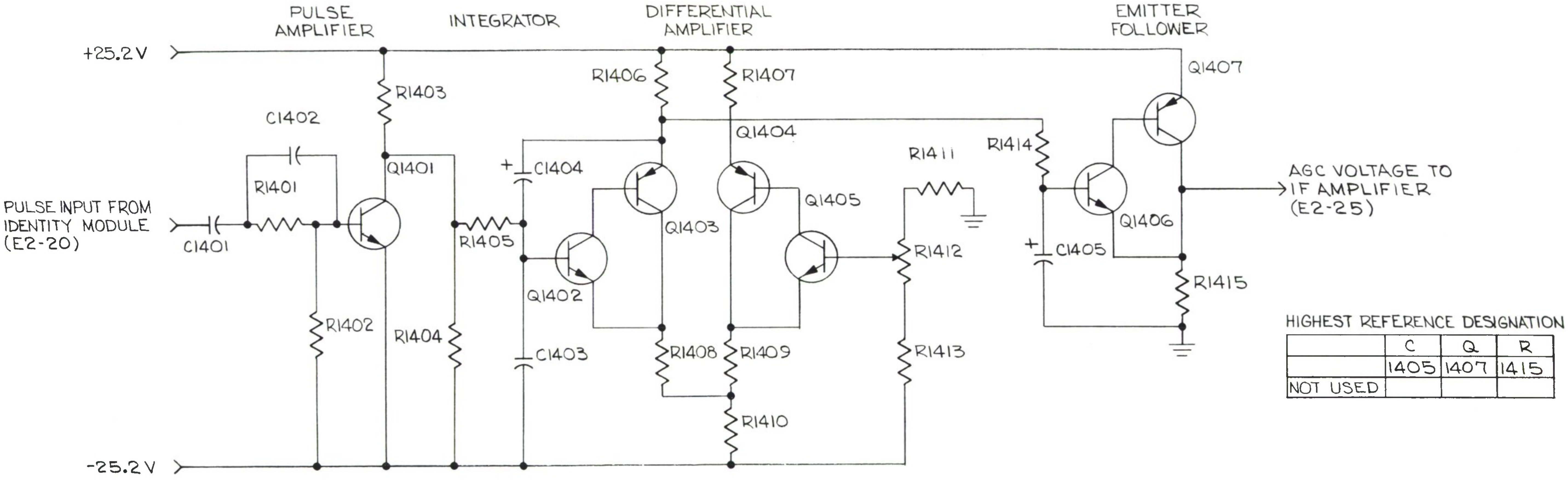
IDENTITY MODULE

C1301	Electrolytic, Tantalum, 1.7 uf, ±20%, 125 VDCW, CL65BP1R7MP3
C1302	CM15C330J
C1303	Electrolytic, Tantalum, 1.7 uf, ±20%, 125 VDCW, CL65BP1R7MP3
C1304	CM15C330J
C1305	CM15D471J
C1306	CM15C151J
C1307	CM30E332G
C1308	CM15D511J
C1309	CM15C181J
C1310	CM30E102G
C1311	CM15D221J
C1312	CM15C330J
C1313	CM30E102G
C1314	CM15D471J
C1315	Metallized Mylar, 1.0 uf, 100 VDCW, Good All Type X663FR
C1316	CM15C330J
C1317	CM30E222G
C1318	Electrolytic, Aluminum, 30 uf, 50 VDCW, Cornell Dubilier Type NLW 30-50
C1319	CM15C330J
C1320	CM15C330J
C1321	CM15C330J

CR1301	1N251
CR1302	1N251
CR1303	1N251
CR1304	1N457
CR1305	1N251
CR1306	1N251
CR1307	1N251
CR1308	1N251
CR1309	1N251
CR1310	1N251

Q1301	2N2219
Q1302	2N2219
Q1303	2N2219
Q1304	2N2219
Q1305	2N2219
Q1306	2N2219
Q1307	2N2219
Q1308	2N2219
Q1309	2N2219

R1301	RC07GF683J
R1302	RC07GF103J
R1303	RC07GF103J
R1304	RC07GF332J
R1305	RC07GF331J
R1306	RC07GF683J
R1307	RC07GF103J
R1308	RC07GF103J
R1309	RC07GF332J
R1310	RC07GF331J
R1311	RC07GF103J
R1312	Trimpot Bourns Type 224P-1 103, 10K, ±5%
R1313	RN60C3922F
R1314	RC07GF103J
R1315	RC07GF224J
R1316	RC20GF272J
R1317	RC07GF333J
R1318	RC07GF103J
R1319	RC07GF224J
R1320	RC07GF272J
R1321	RC07GF333J
R1322	RC07GF472J
R1323	RC07GF103J
R1324	Trimpot Bourns Type 224P-1-103
R1325	RN60C3922F
R1326	RC07GF103J
R1327	RC20GF222J
R1328	RC07GF333J
R1329	RC07GF103J
R1330	RC07GF222J
R1331	RC07GF103J
R1332	Trimpot Bourns Type 224P-2-104
R1333	RN65C3321F
R1334	RC07GF473J
R1335	RC07GF103J
R1336	RC20GF272J
R1337	RC07GF333J
R1338	RC07GF103J
R1339	RC07GF272J
R1340	RC07GF333J
R1341	RC07GF333J
R1342	RC07GF332J
R1343	RC07GF103J
R1344	RC07GF103J
R1345	RC07GF333J



HIGHEST REFERENCE DESIGNATION

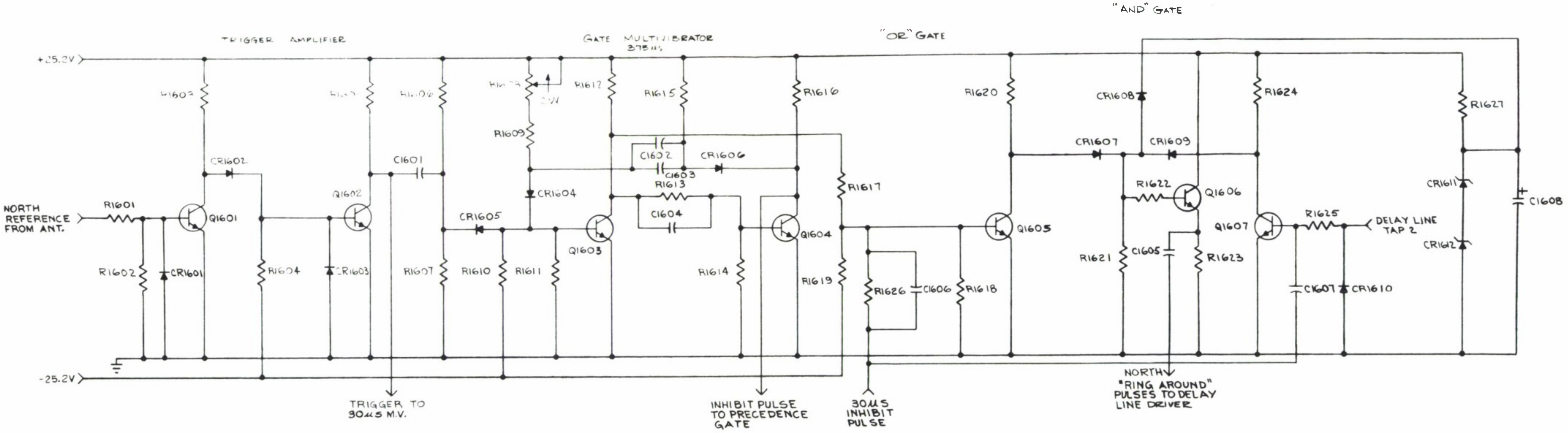
	C	Q	R
	1405	1407	1415
NOT USED			

I.F. Amplifier A.G.C. Module, Schematic Diagram T2319444

PARTS LIST

AGC MODULE

C1401	Mylar, 0.1 uf, 50 WVDC, Good-All Type 601PE
C1402	CM15C101J
C1403	CL65BK500MP3
C1404	Metallized Mylar, 1.0 uf, 100 WVDC, Good-All Type X663FR
Q1401	2N2219
Q1402	2N2219
Q1403	2N1132
Q1404	2N1132
Q1405	2N2219
Q1406	2N2219
Q1407	2N1132
R1401	RL07GF183J
R1402	RL07GF223J
R1403	RN60C1001F
R1404	RN60C1471F
R1405	RN60C1001F
R1406	RN70C4751F
R1407	RN70C4751F
R1408	RN60C1000F
R1409	RN60C1000F
R1410	RN65C1211F
R1411	RN60C3551F
R1412	Trimpot Bourns Type 224P-1-201
R1413	RN60C2741F
R1414	RC07GF222J
R1415	RC42GF331J



NOTE:
HIGHEST COMPONENT NUMBER.

C	R	CR	Q
1608	1627	1612	1607

North Reference Burst Generator Module,
Schematic Diagram T2319448

PARTS LIST

NORTH REFERENCE BURST GENERATOR

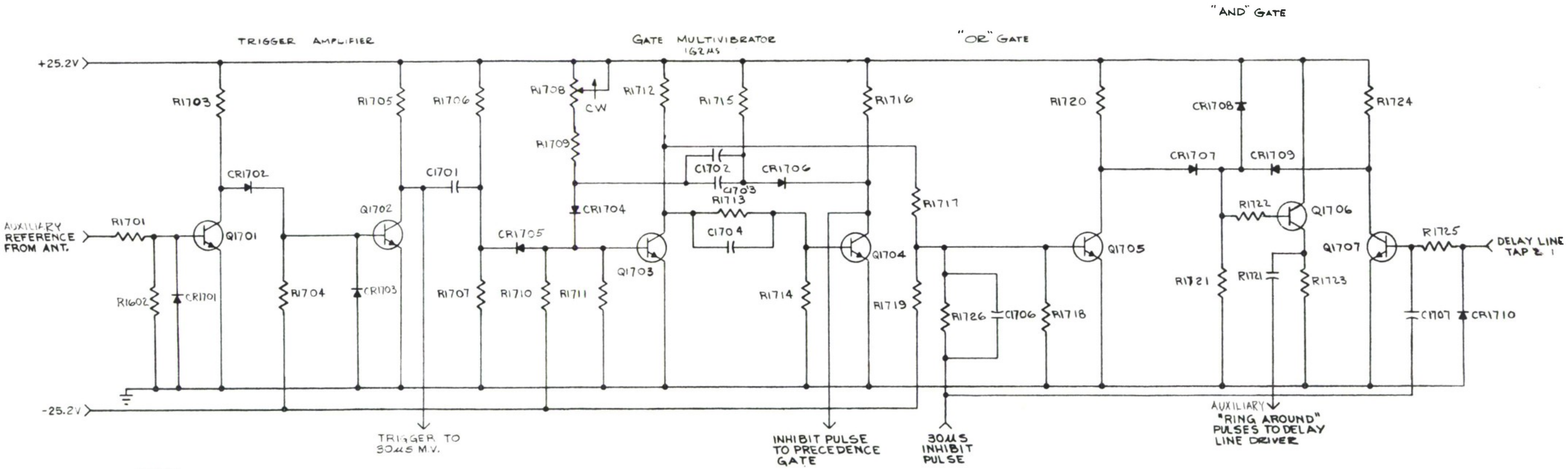
C1601	150 pf	CM15C151J
C1602	3300 pf	CM30E332G
C1603	10,000 pf	CM35D103J
C1604	100 pf	CM15C101J
C1605	220 pf	CM15D221J
C1606	22 pf	CM15C220J
C1607	33 pf	CM15C330J
C1608	50 uf	CL65BK500MP3

CR1601	1N251
CR1602	1N251
CR1603	1N251
CR1604	1N251
CR1605	1N251
CR1606	1N251
CR1607	1N251
CR1608	1N251
CR1609	1N251
CR1610	1N251
CR1611	1N753
CR1612	1N751

Q1601	2N338
Q1602	2N338
Q1603	2N2219
Q1604	2N2219
Q1605	2N2219
Q1606	2N2219
Q1607	2N2219

R1601	47K	RC07GF473J
R1602	10K	RC20GF103J
R1603	22K	RC07GF223J
R1604	47K	RC07GF473J
R1605	4.7K	RC07GF472J
R1606	220K	RC07GF224J
R1607	10K	RC07GF103J
R1608	10K	Bourns Model 224 Terminal P, 224-1-103
R1609	33.2K	RN60C3322F
R1610	220K	RC07GF224J

R1611	10K	RC07GF103J
R1612	2.2K	RC32GF222J
R1613	39K	RC20GF393J
R1614	10K	RC07GF103J
R1615	10K	RC07GF103J
R1616	2.2K	RC07GF222J
R1617	47K	RC07GF473J
R1618	10K	RC07GF103J
R1619	100K	RC07GF104J
R1620	6.8K	RC07GF682J
R1621	27K	RC07GF273J
R1622	10K	RC20GF103J
R1623	2.2K	RC20GF222J
R1624	6.8K	RC07GF682J
R1625	4.7K	RC20GF472J
R1626	68K	RC07GF683J
R1627	330 ohms	RC42GF331J



NOTE:
HIGHEST COMPONENT NUMBER.

C	R	CR	Q
1707	1725	1710	1707

Auxiliary Reference Burst Generator,
Module, Schematic Diagram T2319443

PARTS LIST

AUXILIARY REFERENCE BURST GENERATOR

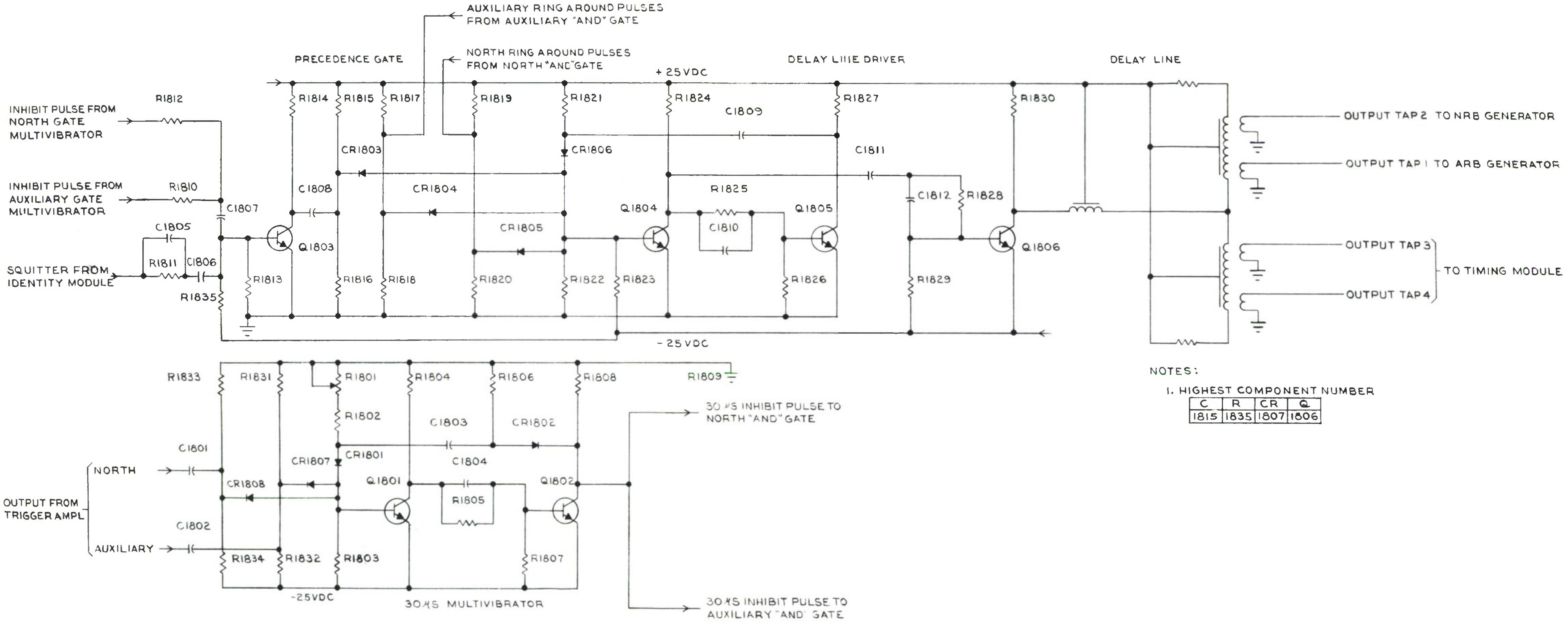
C1701	150 pf	CM15C151J
C1702	3300 pf	CM30E332G
C1703	3000 pf	CM30E302G
C1704	100 pf	CM15C101J
C1705	220 pf	CM15D221J
C1706	22 pf	CM15C220J
C1707	33 pf	CM15C330J

CR1701	1N251
CR1702	1N251
CR1703	1N251
CR1704	1N251
CR1705	1N251
CR1706	1N251
CR1707	1N251
CR1708	1N251
CR1709	1N251
CR1710	1N251

Q1701	2N338
Q1702	2N338
Q1703	2N2219
Q1704	2N2219
Q1705	2N2219
Q1706	2N2219
Q1707	2N2219

R1701	47K	RC07GF473J
R1702	10K	RC20GF103J
R1703	22K	RC07GF223J
R1704	47K	RC07GF473J
R1705	4.7K	RC07GF472J
R1706	220K	RC07GF224J
R1707	10K	RC07GF103J
R1708	10K	Bourns Model 224 Terminal P, 224-1-103
R1709	33.2K	RN60C3322F
R1710	220K	RC07GF224J
R1711	10K	RC07GF103J
R1712	2.2K	RC32GF222J
R1713	39K	RC20GF393J
R1714	10K	RC07GF103J
R1715	10K	RC07GF103J

R1716	2.2K	RC07GF222J
R1717	47K	RC07GF473J
R1718	10K	RC07GF103J
R1719	100K	RC07GF104J
R1720	6.8K	RC07GF682J
R1721	27K	RC07GF273J
R1722	10K	RC20GF103J
R1723	2.2K	RC20GF222J
R1724	6.8K	RC07GF682J
R1725	4.7K	RC20GF472J
R1726	68K	RC07GF683J



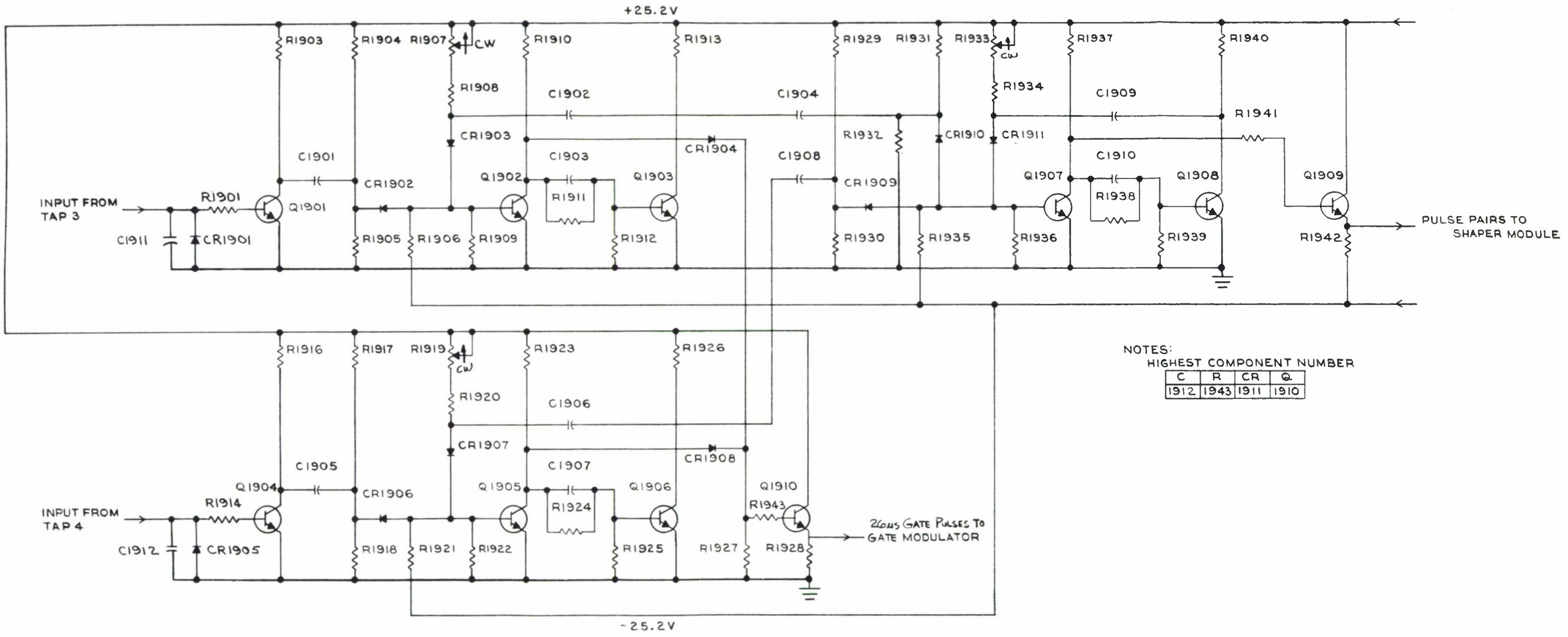
Delay Line Driver Module, Schematic Diagram T2319452

PARTS LIST

DELAY LINE DRIVER

C1801	100 pf	CM15C101J
C1802	100 pf	CM15C101J
C1803	1200 pf	CM30E122G
C1804	100 pf	CM15C101J
C1805	39 pf	CM15C390J
C1806	11 uf	CL65BN110MP3
C1807	11 uf	CL65BN110MP3
C1808	180 pf	CM15C181J
C1809	100 pf	CM15C101J
C1810	0.1 uf	Good-All 601 PE, 50 WVDC
C1811	22 pf	CM15C220J
C1812	100 pf	CM15C101J
CR1801	1N251	
CR1802	1N251	
CR1803	1N251	
CR1804	1N251	
CR1805	1N251	
CR1806	1N251	
CR1807	1N251	
Q1801	2N338	
Q1802	2N2219	
Q1803	2N2219	
Q1804	2N2219	
Q1805	2N2219	
Q1806	2N2219	
Q1807	2N699	
R1801	10K	Bourns Model 224 Terminal P, 224-1-103
R1802	33.2K	RN65C3322F
R1803	3.3K	RC07GF332J
R1804	2.2K	RC32GF222J
R1805	39K	RC07GF393J
R1806	10K	RC07GF103J
R1807	10K	RC07GF103J
R1808	2.7K	RC07GF272J
R1809		Not Used
R1810	39K	RC07GF393J
R1811	39K	RC07GF393J
R1812	39K	RC07GF393J
R1813	10K	RC07GF103J

R1814	10K	RC07GF103J
R1815	150K	RC07GF154J
R1816	10K	RC07GF103J
R1817	150K	RC07GF154J
R1818	10K	RC07GF103J
R1819	150K	RC07GF154J
R1820	10K	RC07GF103J
R1821	33.2K	RN65C3322F
R1822	10K	RC07GF103J
R1823	220K	RC07GF224J
R1824	1.8K	RC32GF182J
R1825	39K	RC07GF393J
R1826	10K	RC07GF103J
R1827	2.2K	RC07GF222J
R1828	18K	RC07GF183J
R1829	3.9K	RC07GF392J
R1831	220K	RC07GF224J
R1832	10K	RC07GF103J
R1833	220K	RC07GF224J
R1834	10K	RC07GF103J
R1835	220K	RC07GF224J



NOTES:
HIGHEST COMPONENT NUMBER

C	R	CR	Q
1912	1943	1911	1910

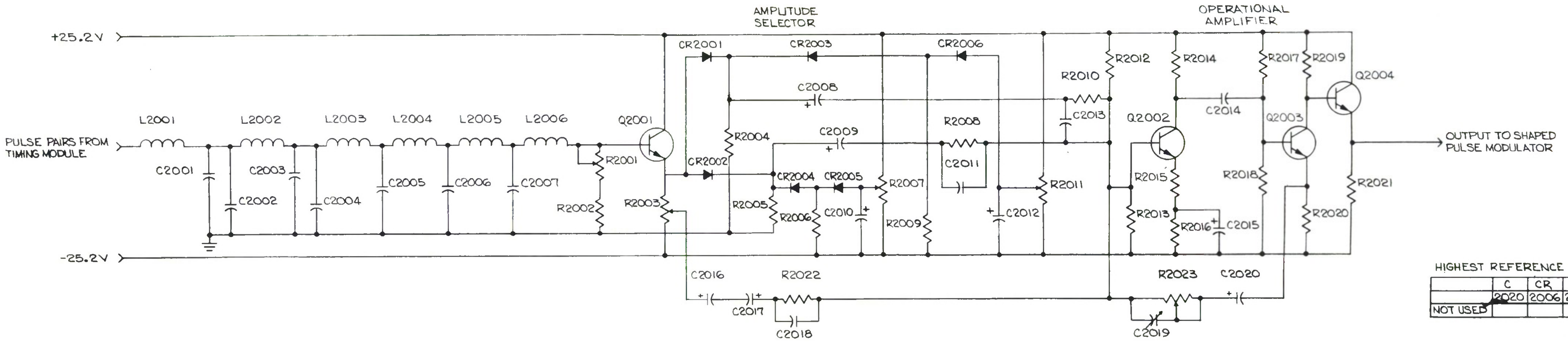
Timing Module, Schematic Diagram
T2319446

PARTS LIST

TIMING MODULE

C1901	100 pf	CM15C101J
C1902	510 pf	CM15D511J
C1903	47 pf	CM15C470J
C1904	100 pf	CM15C101J
C1905	100 pf	CM15C101J
C1906	510 pf	CM15D511J
C1907	47 pf	CM15C470J
C1908	100 pf	CM15C101J
C1909	120 pf	CM15C121J
C1910	47 pf	CM15C470J
C1911	47 pf	CM15C470J
C1912	47 pf	CM15C470J
CR1901	1N251	
CR1902	1N251	
CR1903	1N251	
CR1904	1N251	
CR1905	1N251	
CR1906	1N251	
CR1907	1N251	
CR1908	1N251	
CR1909	1N251	
CR1910	1N251	
CR1911	1N251	
Q1901	2N2219	
Q1902	2N2219	
Q1903	2N2219	
Q1904	2N2219	
Q1905	2N2219	
Q1906	2N2219	
Q1907	2N2219	
Q1908	2N2219	
Q1909	2N2219	
Q1910	2N2219	
R1901	4.7K	RC07GF472J
R1902		Not Used
R1903	4.7K	RC07GF472J
R1904	220K	RC07GF224J
R1905	10K	RC07GF103J
R1906	220K	RC07GF224J
R1907	10K	Bourns 224P-2-103

R1908	33.2K	RN60C3322F
R1909	10K	RC07GF103J
R1910	2.2K	RC32GF222J
R1911	39K	RC07GF393J
R1912	10K	RC07GF103J
R1913	2.2K	RC07GF222J
R1914	4.7K	RC07GF472J
R1915		Not Used
R1916	4.7K	RC07GF472J
R1917	220K	RC07GF224J
R1918	10K	RC07GF103J
R1919	10K	Bourns 224P-2-103
R1920	33.2K	RN60C3322F
R1921	220K	RC07GF224J
R1922	10K	RC07GF103J
R1923	2.2K	RC32GF222J
R1924	39K	RC07GF393J
R1925	10K	RC07GF103J
R1926	2.2K	RC07GF222J
R1927	22K	RC07GF223J
R1928	1K	RC07GF472J
R1929	220K	RC07GF224J
R1930	10K	RC07GF103J
R1931	220K	RC07GF224J
R1932	10K	RC07GF103J
R1933	10K	Bourns 224P-2-103
R1934	33.2K	RN65C3322F
R1935	220K	RC07GF224J
R1936	10K	RC07GF103J
R1937	2.2K	RC32GF222J
R1938	39K	RC07GF393J
R1939	10K	RC07GF103J
R1940	2.2K	RC07GF222J
R1941	1K	RC07GF102J
R1942	22K	RC07GF223J
R1943	1K	RC07GF102J



HIGHEST REFERENCE DESIGNATION

	C	CR	L	Q	R
	2020	2006	2006	2004	2023
NOT USED					

Shaper Module, Schematic Diagram
G2319449

PARTS LIST

SHAPER MODULE

C2001	1500 pf	CM30E152G
C2002	82 pf	CM15C820J
C2003	1000 pf	CM30E102G
C2004	150 pf	CM15C151J
C2005	910 pf	CM30E911G
C2006	620 pf	CM30E621G
C2007	270 pf	CM15D271J
C2008	11 uf	CL65BN110MP3
C2009	11 uf	CL65BN110MP3
C2010	50 uf	CL65BK500MP3
C2011	6 pf	CC50CH060C
C2012	50 uf	CL65BK500MP3
C2013	6 pf	CC50CH060C
C2014	11 uf	CL65BN110MP3
C2015	50 uf	CL65BK500MP3
C2016	11 uf	CL65BN110MP3
C2017	11 uf	CL65BN110MP3
C2018	6 pf	CC50CH060C
C2019	0.8 - 10.0 pf	Johanson, Series 2900; JMC 2902
C2020	11 uf	CL65BN110MP3

CR2001	1N251
CR2002	1N251
CR2003	1N251
CR2004	1N251
CR2005	1N251

L2001	2.37 mh
L2002	1.30 mh
L2003	1.03 mh
L2004	765 uh
L2005	447 uh
L2006	91 uh

Q2001	2N2219
Q2002	2N2219
Q2003	2N699
Q2004	2N699

R2001	200 ohms	Bourns Model 224 Terminal P; 224-1-201
R2002	909 ohms	RN60C9090F
R2003	2000 ohms	Bourns Model 224 Terminal P; 224-1-202
R2004	10K ohms	RN60C1002F
R2005	10K ohms	RN60C1002F
R2006	10K ohms	RN60C1002F
R2007	10K ohms	Bourns Model 224 Terminal P; 224-1-103
R2008	21500 ohms	RN60C2152F
R2009	10K ohms	RN60C103F
R2010	21500 ohms	RN60C2152F
R2011	10K ohms	Bourns Model 224 Terminal P; 224-1-103
R2012	22K ohms	RC07GF223K
R2013	10K ohms	RC07GF103K
R2014	2700 ohms	RC07GF272K
R2015	100 ohms	RC20GF101K
R2016	2700 ohms	RC07GF272K
R2017	68100 ohms	RN70C6812F
R2018	10K ohms	RN60C1002F
R2019	6810 ohms	RN70C6811F
R2020	1000 ohms	RN65C1001F
R2021	2200 ohms	RC20GF222K
R2022	21500 ohms	RN60C2152F
R2023	10K ohms	Bourns Model 224 Terminal P; 224-1-103

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Bedford, Mass.

13. ABSTRACT

The design of a solid state receiver coder for use as paer of a TACAN Ground station is given. A detailed description of the deliverable breadboard from both its physical and electrical aspects is given, together with test results obtained to date and recommendations for further development.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Coding						
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