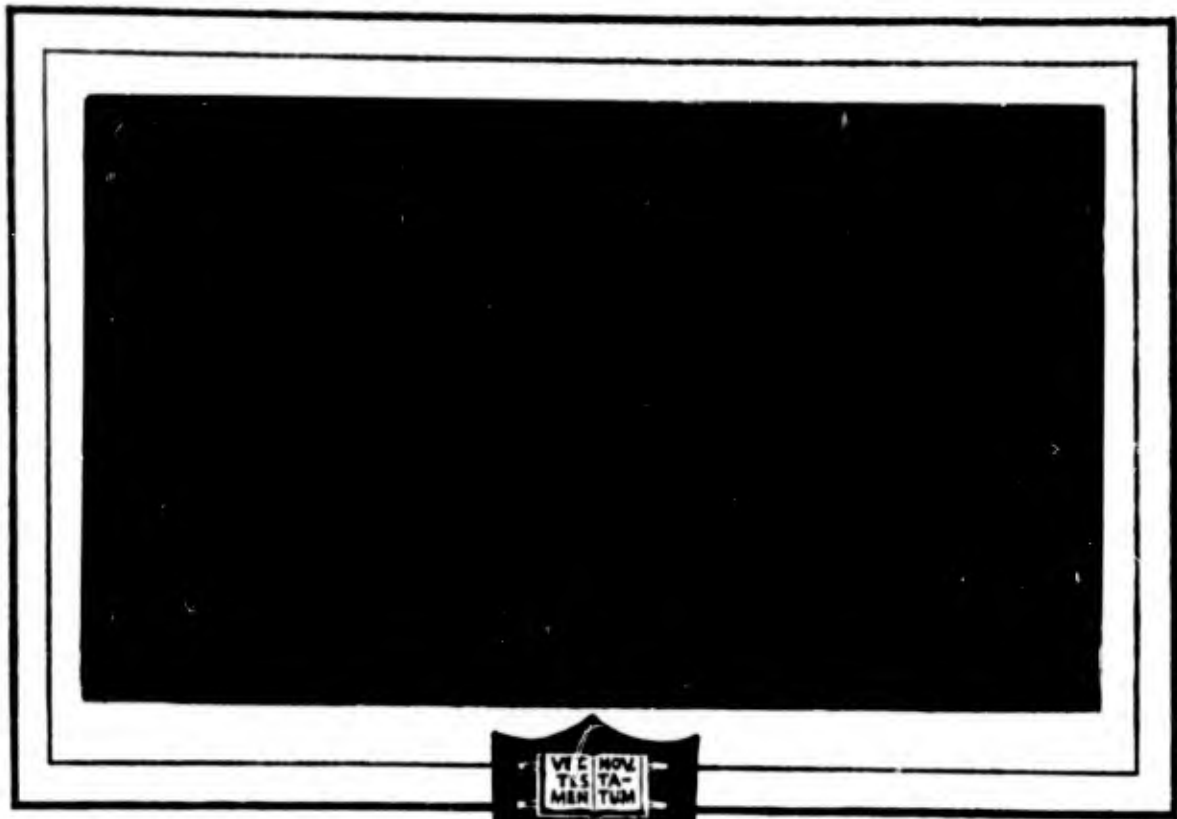


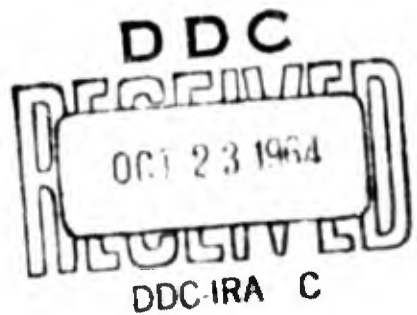
B ✓ AD 607229



COPY	1	OF	1	cat
HARD COPY	\$.	1.00		
MICROFICHE	\$.	0.50		

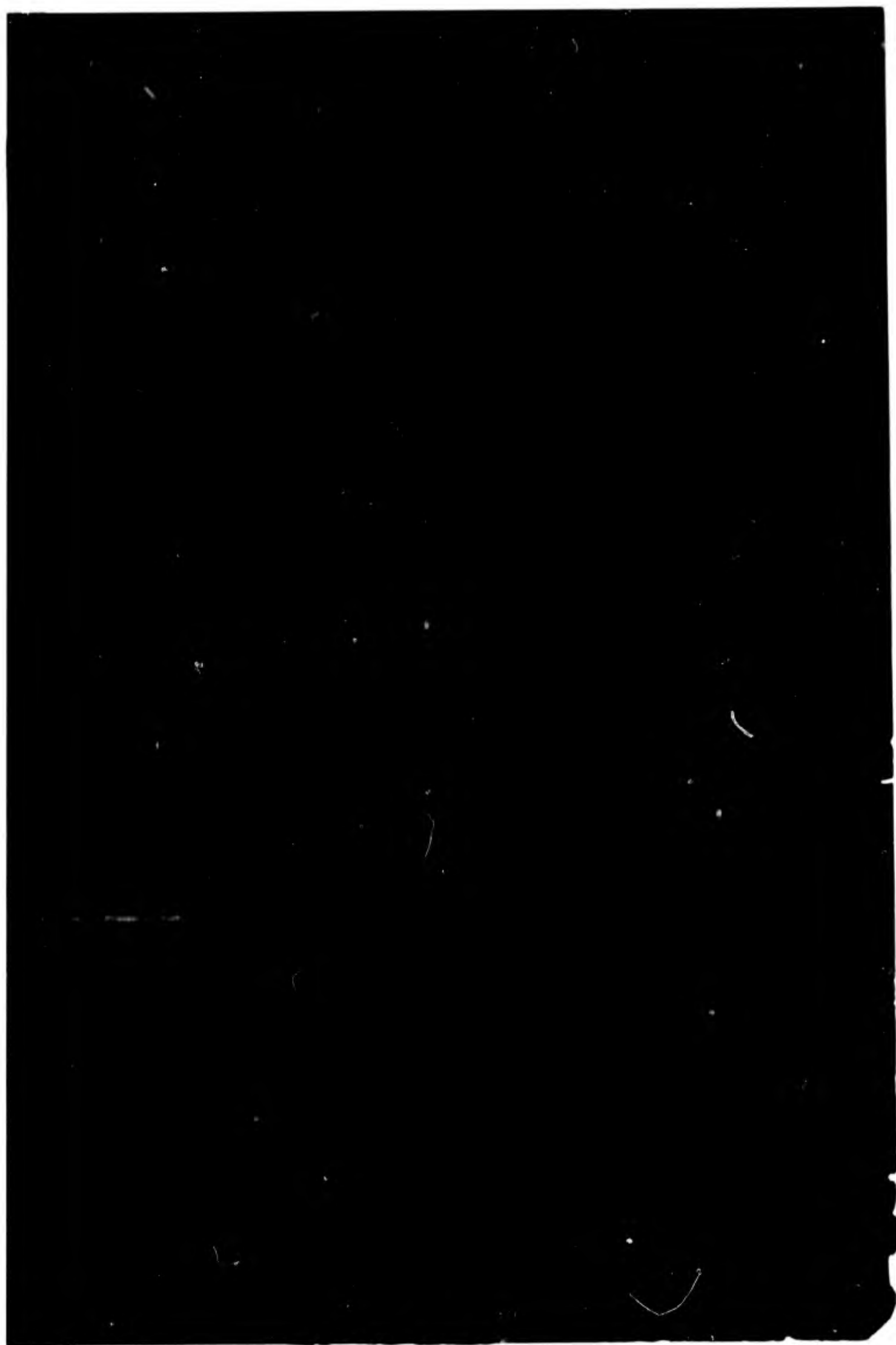
14p

PRINCETON UNIVERSITY



H

(1)



PRINCETON UNIVERSITY

Department of Electrical Engineering
Digital Systems Laboratory
✓ Technical Report Number 38
(August 1964)

ON THE MINIMUM STAGE REALIZATION
OF SWITCHING FUNCTIONS USING LOGIC
GATES WITH LIMITED FAN-IN

G. L. Hicks and A. J. Bernstein

ON THE MINIMUM STAGE REALIZATION OF SWITCHING FUNCTIONS USING LOGIC GATES WITH LIMITED FAN-IN

G. L. Hicks and A. J. Bernstein
Digital Systems Laboratory
Department of Electrical Engineering
Princeton University, Princeton, New Jersey

ABSTRACT

In this paper a method is presented for reducing the number of stages of logic in the realization of an arbitrary Boolean function when an upper bound exists on the fan-in at each gate. A procedure for obtaining the minimum stage realization of the function in sum of products form is first developed. The use of factoring to reduce the number of stages below this minimum is then described.

1. INTRODUCTION

This paper is concerned with reducing the number of stages of logic in a switching circuit when AND and OR gates with limited fan-in are to be used. Such a reduction is desirable since it results in a reduction of both the delay and degeneration of the signal as it traverses the circuit.

When AND and OR gates without fan-in limitations are available, an arbitrary switching function can always be realized by a circuit with no more than two stages of logic. The standard form for such a realization corresponds to the normal or sum-of-products form of the switching function. The circuit has a level of AND gates followed by a single OR gate. The number of input leads to the OR gate is equal to the number of conjunctions in the sum of products expression of the switching function plus the number of literals occurring alone. The number of input leads on a particular AND gate is the number of literals in the conjunction realized by that gate. Such a circuit realization is impractical since in most technologies (e.g. diode, transistor) there is an upper bound on the number of inputs which can be accommodated by a single gate. Due to this fan-in limitation, it is no longer possible to realize all switching functions in two-stage circuits. Thus, if the number of literals in a conjunction exceeds the fan-in on AND gates, it will require more than one level of AND logic to realize that conjunction. Similarly, if the number of conjunctions exceeds the fan-in on OR gates, it will require more than one level of OR logic to sum the conjunctions. The purpose of this paper is to present a method for reducing the number of levels of logic in a circuit under arbitrary fan-in restrictions.

The authors are not aware of any results that have been obtained on this specific problem. Work has been done on minimizing the number

of AND and OR gates necessary to realize Boolean functions by using multi-level realizations^{1,2,3,4,5}. These techniques have been extended to networks using other types of gates (NOR gates, etc.)^{6,7}. Other minimization procedures include restrictions on the number of stages without being concerned with the specific problem of fan-in limitations.⁸

It is clear that there is a natural correspondence between the form of a switching function and the particular switching circuit which realizes the function. Thus, if a function is expressed in sum of products form, the corresponding circuit realization would have the property that on any path from an input to the output the AND gates precede the OR gates. On the other hand, if the common literals in a subset of the conjunctions are factored in the switching function, then in the corresponding circuit there will be at least one path from input to output along which an AND gate follows an OR gate.

In the first part of this paper a method for realizing an unfactored switching function in a minimum number of stages is presented. The method involves a simple arithmetic procedure and does not necessitate the drawing of a circuit diagram. The method can be extended naturally to allow one to determine the effect of a factorization on the number of stages in the circuit. In the second part of the paper the minimum number of stages necessary to realize the unfactored function is used as the starting point for a method of reducing the delay of the circuit below this minimum by factoring. A necessary and sufficient condition is developed which determines whether or not a proposed factorization will reduce the number of stages by a given amount.

THE MINIMUM STAGE CIRCUIT REALIZATION WITHOUT FACTORING

When no factoring is performed, the basic concepts of the two-level realization must be fol-

lowed. That is, the individual conjunctions are formed with AND gates in the initial stages of the circuit and their disjunction is formed with OR gates in the final stages.

The delay of each of the constituent conjunctions must be determined before the total circuit delay of the function can be considered. If the maximum fan-in for each AND gate is designated by "a", then in y stages the conjunction of at most a^y literals can be realized. In other words, a conjunction is of delay y if the number of literals, N, in the conjunction satisfies the following condition:

$$a^{(y-1)} < N \leq a^y \quad (1)$$

The problem now reduces to finding the optimum method of combining the conjunctions on OR gates (summing them) so as to minimize the total delay, given the delay of the conjunctions.

It will be convenient to introduce some notation before proceeding. Let F be the given switching function and let f be the sum of products expression for F. Let n be the maximum fan-in for all OR gates, and let k_i be the number of conjunctions of delay i. Let m be the largest and s the least delay of any of the constituent conjunctions. It is clear that any function involving more than one product term has a minimum delay of (m+1) if no factorization is performed, since at least one additional stage for a concluding OR gate is necessary.

Definition 1. If the sum of products expression of a function can be realized in (m+1) stages, it will be said that the function can be realized optimally.

The following theorem is concerned with conditions under which a switching function can be realized optimally.

Theorem 1. Sufficient conditions for a function F to be realized optimally are that $k_s \leq n$ and $k_i \leq (n-1)$ for $s < i \leq m$.

Proof: Assume the worst case, i.e., that $k_s = n$ and $k_i = n-1$ for $s < i \leq m$. It is clear that if F can be realized optimally in this case, any function with smaller values of the k_i can also be realized optimally. The conjunctions will be considered according to increasing values of delay. The n conjunctions of delay s can be summed by a single OR gate to form a subcircuit of delay (s+1). This subcircuit of delay (s+1) can then be summed with the (n-1) conjunctions of delay (s+1) to form a subcircuit of delay (s+2) which in turn can be summed with the (n-1) conjunctions of delay (s+2) to form

a subcircuit of delay (s+3) etc. It is thus seen that in the general case the (n-1) conjunctions of delay i are summed with a circuit of delay i that realizes the disjunction of all the conjunctions of delay less than i. The result of forming the new disjunction is a circuit of delay (i+1). When the conjunctions of delay m are considered, a circuit of delay (m+1) is formed. Hence, F is realized optimally. The OR logic for the above realization of F is shown in Fig. 1.

Example 1. Let $a = 2$ and $n = 3$ and

$$f = \overline{A}\overline{B} + \overline{A}B + \overline{H}\overline{G} + CDE + \overline{C}\overline{D}E\overline{H}G + C\overline{D}\overline{E}H\overline{G}$$

Since $k_1 = 3$, $k_2 = 1$, and $k_3 = 2$, the conditions of Theorem 1 are satisfied and an optimal realization is possible. The circuit is shown in Fig. 2.

When the conditions on the number of conjunctions, as expressed in Theorem 1, are violated, it may no longer be possible to realize F optimally. The problem then becomes that of realizing f with the minimum possible number of stages. Theorem 2 is concerned with one method of so realizing f.

Definition 2. An input of delay i is a connection in a circuit which has the property that the maximum number of stages of logic on any path between this point and a circuit input is i.

Theorem 2. Given a function F with some $k_i > (n-1)$ where $s \leq i \leq m$, there exists a realization of f of minimum delay which has an OR gate whose inputs are n conjunctions of delay i.

Proof: Consider a realization of f with minimum delay. Let $G_1, G_2, \dots, G_M$ be the OR gates which have as inputs conjunctions of delay i, $M \leq k_i$. Let L_j be the number of levels of logic encountered in traversing a path from the input of G_j to the output of the circuit (see Fig. 3), let L be the delay of the entire circuit, and let the gates be labeled such that

$$L \geq L_1 \geq L_2 \dots \geq L_M$$

The label on each input to a gate in Fig. 3 represents the delay of that input. The essence of the proof is to show that conjunctions of delay i can be appropriately transferred to G_1 without increasing the delay of the total circuit.

Consider interchanging the input of delay i on G_2 with the input of delay a_1 on G_1 . Since G_1 already has an input of delay i, the maximum number of stages on any path through the circuit traversing G_1 has not increased. Also, since $L \geq L_1 + a_1$, it follows that $L \geq L_2 + a_1$ and thus the paths in the new circuit which traverse G_2

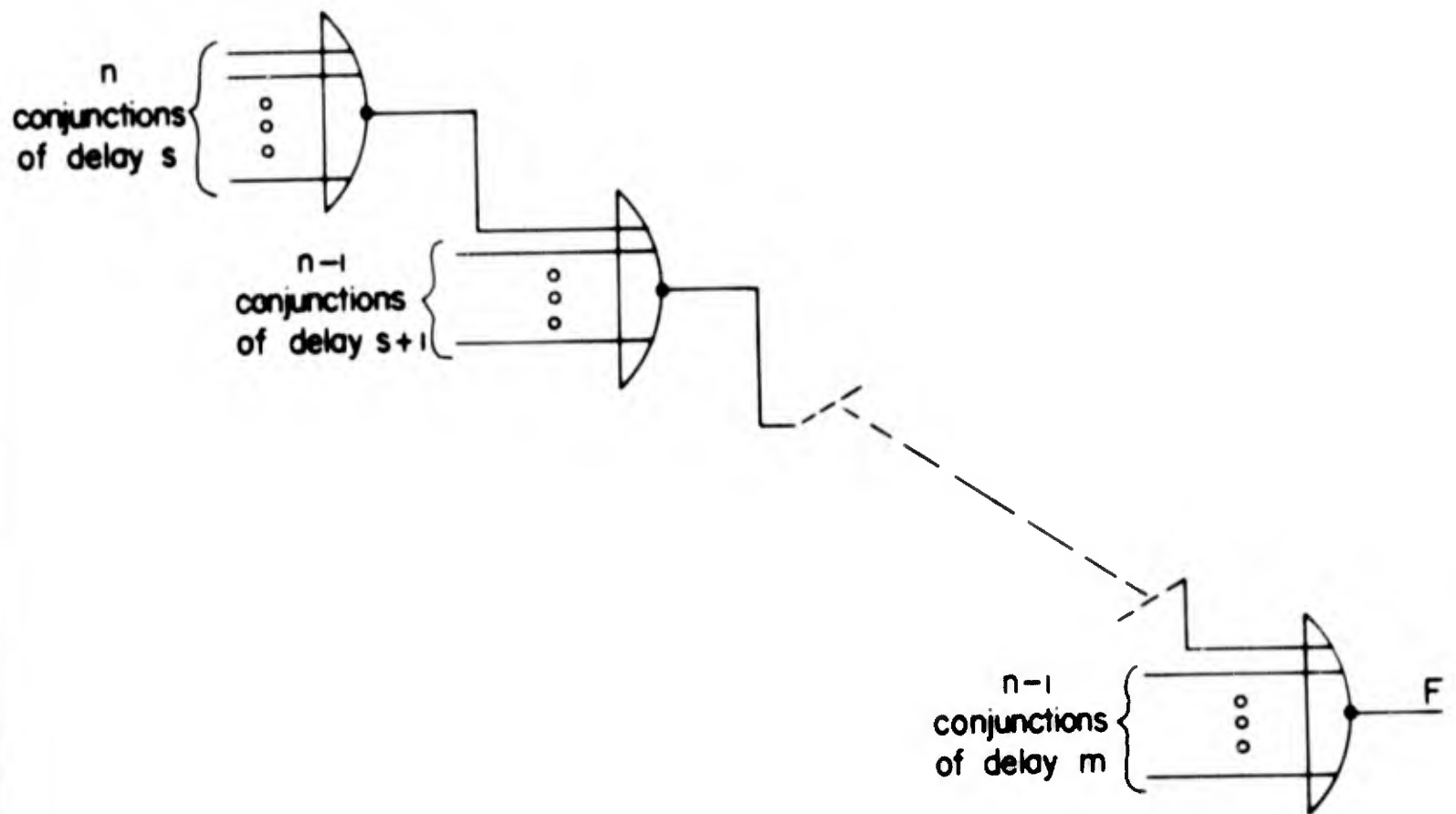


Figure 1.

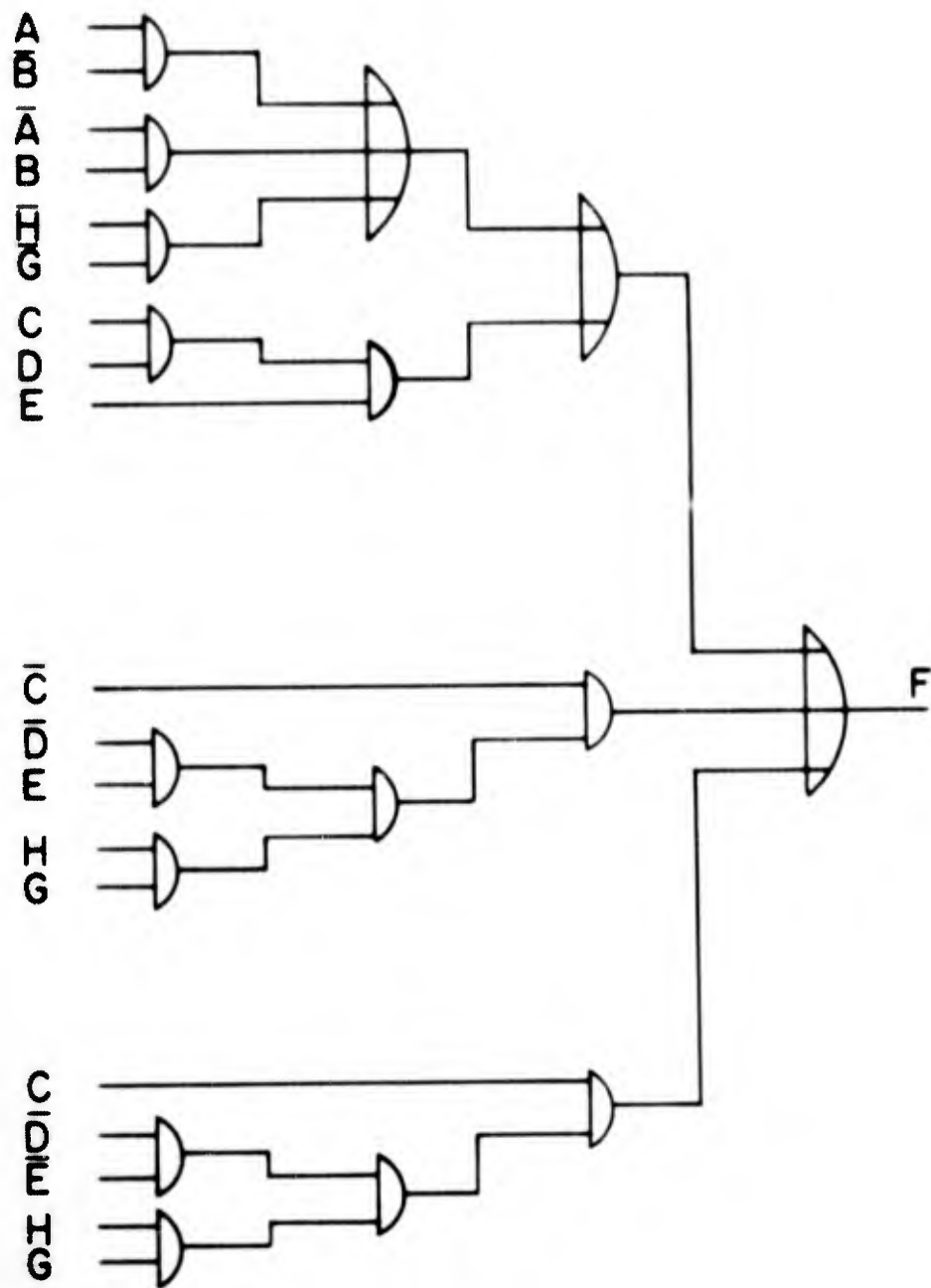


Figure 2.

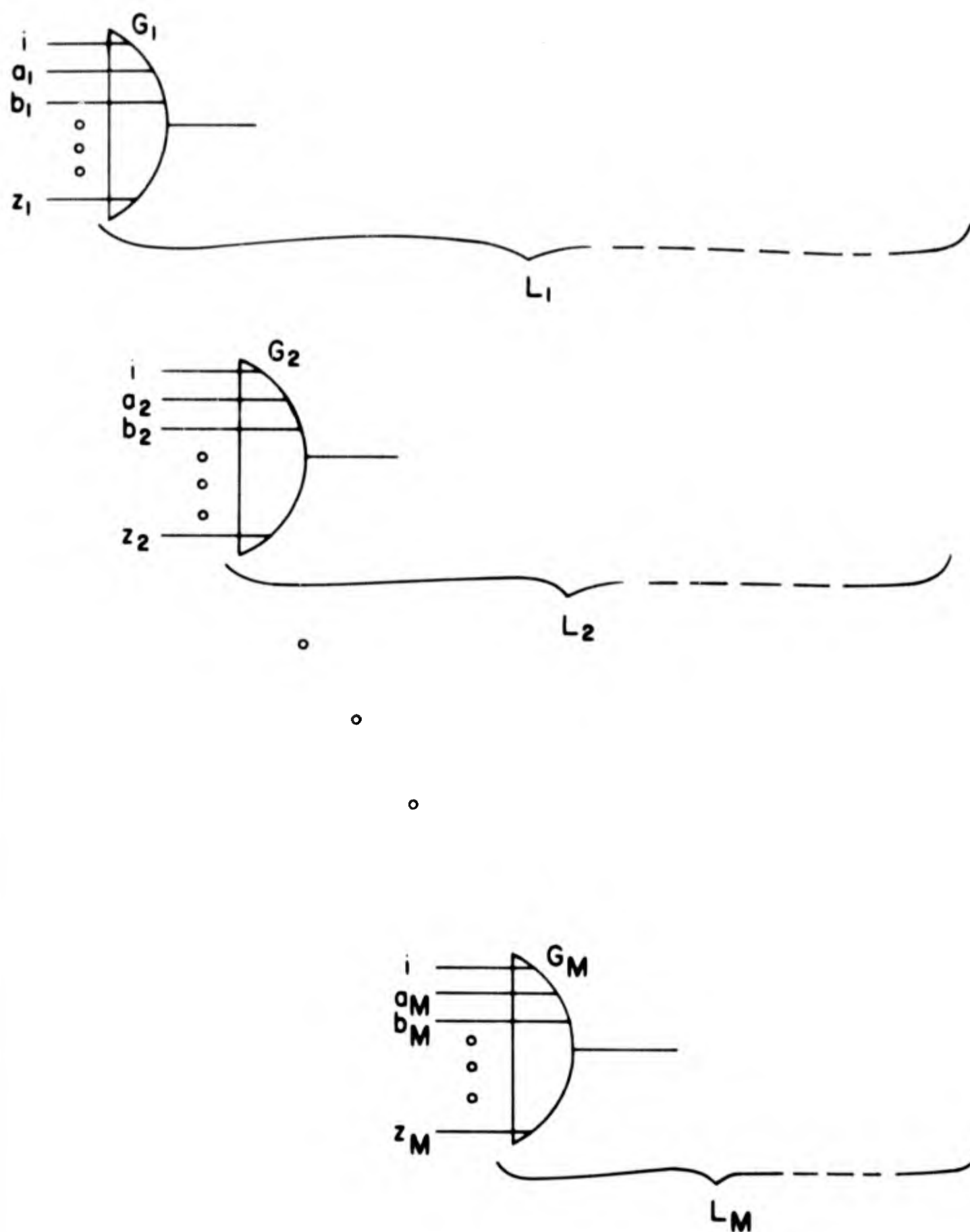


Figure 3.

will encounter no more than L levels of logic. It follows that the over-all delay of the new circuit is less than or equal to L . This process can be repeated for each of the gates G_j until finally all inputs of G_1 have delay i . Thus a new circuit realization for the function f has been constructed whose over-all delay is no more than that of the original circuit and which has an OR gate whose inputs are n conjunctions of delay i . Thus the theorem is proved.

As a result of Theorem 2 we have that if $k_i \geq n$, the first step in the construction of a minimum stage realization can be the formation of the disjunction of n conjunctions of delay i on a single OR gate.

Note 1. From the above proof it is evident that the same procedure can be repeated for n conjunctions of another delay, j . j can also equal i if there are $2n$ or more conjunctions of delay i . Hence, in a minimum delay realization there can be many OR gates all of whose inputs are of the same delay.

Example 2: Suppose a switching function, F , consists of two conjunctions of delay 2, seven conjunctions of delay 4, and two conjunctions of delay 5. The delay of these conjunctions is listed below:

2 2 4 4 4 4 4 4 4 5 5

Let the fan-in for OR gates, n , be equal to three. In accordance with Note 1 and Theorem 2, the conjunctions of delay 4 can be summed as indicated below without sacrificing the minimal delay of the resulting circuit.

2 2 4 4 4 4 4 4 4 5 5
 5 5

or 2 2 4 (5) (5) 5 5

Each of the circled fives represents the delay of the disjunction of three conjunctions of delay 4.

Note 2. In the proof of Theorem 2 the relocation of an input was not dependent on how that input was formed (i.e., whether the input realized a conjunction or a disjunction of conjunctions). This means that the same process can be used to combine conjunctions and disjunctions of like delay on a single OR gate without sacrificing the minimal delay of the resulting circuit. Later in the paper subcircuits representing the factored form of the disjunction of some of the conjunctions will be treated in the same fashion, simply as inputs of some known delay.

Consider again Example 2. It is now apparent that three of the conjunctions and disjunctions of delay 5 can be summed to form a disjunction of delay 6. This is shown symbolically below:

2 2 4 5 (5) (5) 5
 6
2 2 4 5 (6)

The function now "consists" of two conjunctions of delay 2, one conjunction of delay 4, one conjunction of delay 5, and one disjunction of delay 6.

There are now less than n subcircuits (which realize conjunctions or disjunctions or both) of any one delay. The conditions are thus similar to those given in the statement of Theorem 1. In the proof of Theorem 1, the conjunctions were treated as basic elements and the only concern was the proper way of summing these conjunctions to form the total disjunction. As far as the proof was concerned, some of the conjunctions could have been replaced by disjunctions of the same delay. For this reason, Theorem 1 can be applied in the case under consideration. Thus the total circuit delay is just one greater than the largest delay of any of the conjunctions or disjunctions that appear. Therefore, the minimum delay without factorization is $6+1$ or 7.

A general mathematical procedure for executing these steps can be stated as follows.

Rule: Form the summation, $\sum_{i=s}^m k_i \cdot n^i$, using base n arithmetic. The minimum number of stages required to physically realize f is equal to the number of places in the resulting sum unless the sum is of the form 1000-----00. In this case the number of stages is one less than the number of places in the sum.

This procedure is followed below for Example 2.

delay (i)	k_i (base 10)	k_i (base 3)	$k_i \cdot 3^i$ (base 3)
2	2	2	200
4	7	21	210000
5	2	2	200000
		2	0 0 $k_2 \cdot 3^2$
	2	1	0 0 0 0 $k_4 \cdot 3^4$
	2	0	0 0 0 0 0 $k_5 \cdot 3^5$
	1	1	1 0 2 0 0 0

Since there are 7 places in the sum, the minimum number of stages is 7.

We will call the sum resulting from the above addition the delay number of the circuit, D . Thus

$$D = \sum_{i=0}^m k_i \cdot n^i = d_p d_{p-1} d_{p-2} \dots d_1 d_0 \quad (2)$$

The justification for the above procedure is simple. Writing k_i as a base n number exhibits the way conjunctions of delay i are combined in accordance with Theorem 2. Thus, in the example $k_4 = 21$ indicates that of the seven conjunctions of delay 4, six have been absorbed into two disjunctions of delay 5, while the seventh remains untouched. Multiplication of k_i by n^i serves to give positional significance in the summation. Thus every digit in the i^{th} column represents conjunctions or disjunctions of the same delay. Forming the sum combines the circuits of like delay, again in accordance with Theorem 2. A carry generated in the i^{th} column indicates the formation of the disjunction of n subfunctions (conjunctions or disjunctions or both) of delay i . This new disjunction will be of delay $i+1$. Since each digit in the sum is less than n , the conditions of Theorem 1 hold and the minimum number of stages required for the entire circuit is equal to the number of digits in D . The one exception occurs when D is of the form 100-0 since a concluding OR gate is not needed in this case. The minimum number of stages is thus one less than the number of digits in D .

A circuit realization for the above example is shown in Fig. 4. The numbers at various points in the circuit represent the delays at those points. In particular, the numbers on the left-hand side of the diagram represent the delays of the conjunctions connected at those points. The underlined delays represent those conjunctions or disjunctions which are exhibited explicitly in D .

INTRODUCTION TO FACTORING

As stated in the Introduction, it may be possible to reduce the total circuit delay below the minimum obtained in the previous section by factoring common literals out of some of the conjunctions of F . Let f_1 and f_2 be expressions for F as follows:

$$f_1 = A_1 + \dots + A_w + A_{w+1} + \dots + A_r \quad (3)$$

$$f_2 = X(A_1^* + \dots + A_w^*) + A_{w+1} + \dots + A_r \quad (4)$$

and let

$$f_3 = A_1 + \dots + A_w \quad (5)$$

$$f_4 = A_1^* + \dots + A_w^* \quad (6)$$

Here f_1 denotes the sum of products expression for F with conjunctions A_i , and f_2 denotes a particular factored expression in which the conjunctions of some subset of literals, X , has been factored out of the conjunctions $A_1, A_2, \dots, A_w$. A_i^* denotes the conjunction originally designated A_i with the common literals removed. Since the circuit realization for Xf_4 may require fewer stages than does the realization for f_3 , the total circuit delay may be reduced.

The conjunctions involved in the factoring may originally be of like or different delays. In the case of like delay, the factoring will be referred to as in-group factoring while in the second case it will be called out-of-group factoring.

The minimum stage circuit realization of f_2 can be obtained using the results of the previous section. The procedure is to obtain the minimum stage realization of f_4 (which is a sum of products expression) and form its conjunction with X . This circuit will be contained as a unit in the circuit for f_2 and, for the minimization procedure can be characterized simply by its delay, which is known. Thus the expression

$$f_2 = Xf_4 + A_{w+1} + \dots + A_r \quad (7)$$

can be treated as a sum of products expression in which the delay of each of the terms is known and thus the minimization procedure can again be used.

If either an in-group or out-of-group factorization causes a reduction in the total circuit delay, the factorization must, in effect, decrease the delay number. The original delay number, D , will be represented as before by $(d_p d_{p-1} d_{p-2} \dots d_1 d_0)$. If a factorization reduces the total number of stages by g , the new delay number, D' , must be such that $D' \leq n^{(p+1-g)}$. In Example 2, $D = 1110200$ and thus $p = 6$. If the total circuit delay is to be reduced from 7 stages to 5 stages (i.e., $g = 2$) then $D' \leq 3^5$ or $D' \leq 100000$.

If D is equal to n^p (i.e., $d_p = 1$ and $d_{p-1} = d_{p-2} = \dots = d_1 = d_0$) the condition on D' is $D' \leq n^{(p-g)}$.

Definition 3. The critical delay number, $D_c(g)$, is the minimum amount by which D must be decreased if the total number of stages is to be reduced by g .

Thus,

$$\begin{aligned} D_c(g) &= D - n^{(p+1-g)} \quad \text{for } D \neq n^p \\ D_c(g) &= D - n^{(p-g)} \quad \text{for } D = n^p \end{aligned} \quad (8)$$

For Example 2 we have

$$D_c(2) = D - n^5 = 1010200$$

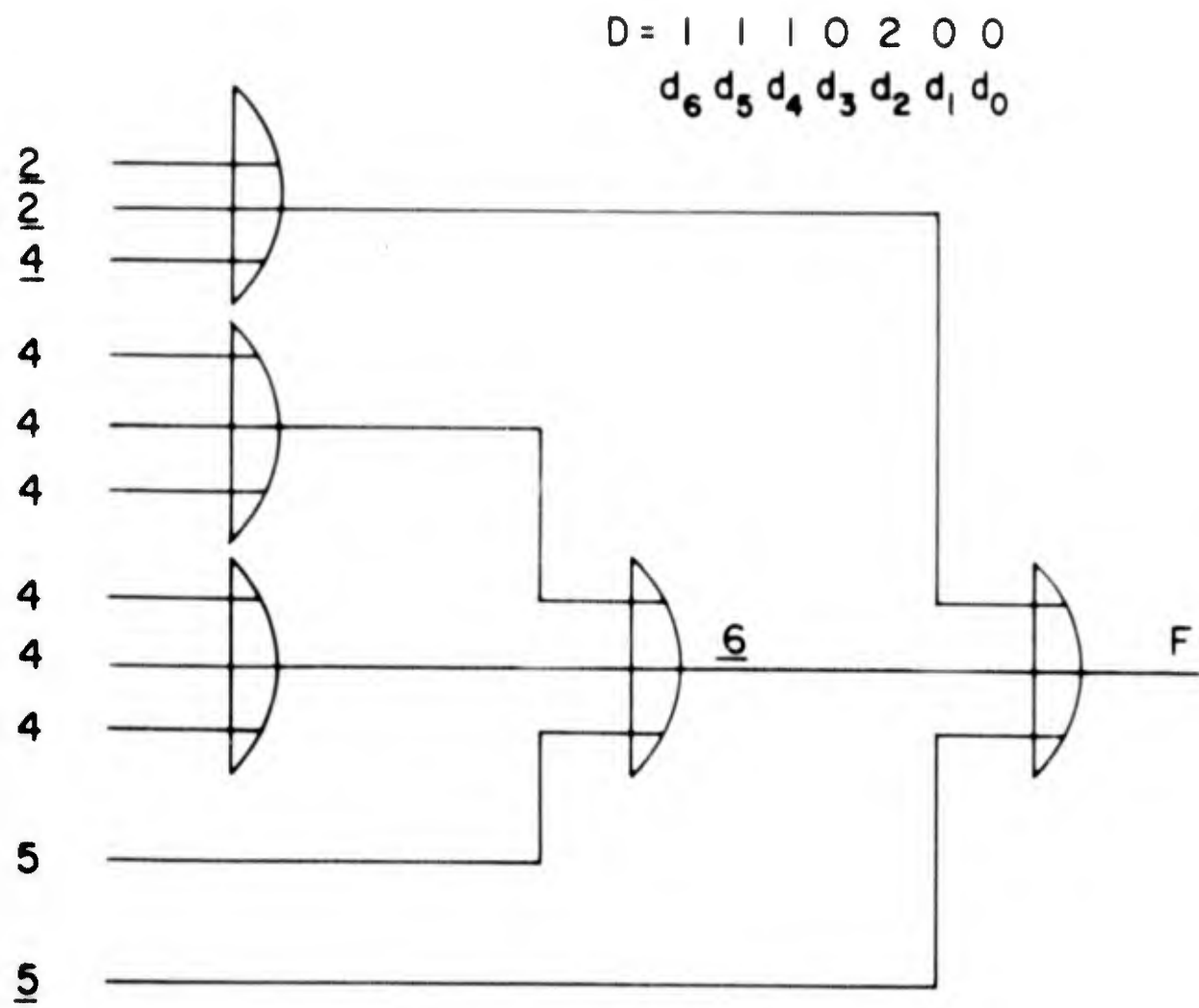


Figure 4.

IN-GROUP FACTORING

In an in-group factorization the common literals, X , are removed from a group of conjunctions all of which are characterized by the same delay i , where $s \leq i \leq m$. The subcircuit realizing this group of conjunctions is shown in Fig. 5. The delay of the new circuit realization will be denoted by $(i+q)$ where $q \geq 0$. The condition on q is as noted since it can be proven (see Appendix) that the number of stages necessary to realize a switching function, F , is at least as great as the number of stages necessary to realize any product term of the sum of products expression for F .

After the common literals are removed from the involved conjunctions (A_1 to A_w), the delays of the resulting conjunctions (A_1^* to A_w^*) will be i or less. The difference in these delays is due to the fact that conjunctions of the same delay (i in this case) may contain different numbers of literals. When the same number of literals are removed from each conjunction, the resulting conjunctions can be of different delays. Since different delays are involved, the method of the previous section must be used to find the proper realization for the part of Fig. 5 labeled AA. The AA portion refers only to the levels of OR logic.

Let k'_i be the number of conjunctions of delay i not involved in the factorization. Once a factorization is carried out, the disjunction of the $(k_i - k'_i)$ involved conjunctions is formed in the circuit shown in Fig. 5. This is a subcircuit of the total circuit, and since a single disjunction or conjunction of delay b is represented by the number n^b in the base n addition procedure, this subcircuit of delay $(i+q)$ is accounted for by adding $n^{(i+q)}$. If the $(k_i - k'_i)$ involved conjunctions are not to be considered twice, $(k_i - k'_i)n^i$ must be subtracted. Thus

$$D' = D - ((k_i - k'_i)n^i - n^{(i+q)})$$

Therefore, if a factorization is to reduce the total circuit delay by the desired number of stages, the following condition must be satisfied:

$$(k_i - k'_i)n^i - n^{(i+q)} \geq D_c(g) \quad (9)$$

If

$$n^{t-1} < (k_i - k'_i) \leq n^t$$

then it follows that the expression f_3 of (5) requires $i+t$ stages for its realization. If the factorization is to reduce the number of stages in the total circuit, it is clear that q must be less than t . Also, the number of levels of OR logic

in the AA portion of the circuit of Fig. 5 must be at least t since otherwise there would not be sufficient input leads to AA to accommodate $(k_i - k'_i)$ conjunctions. It therefore follows that if the expression Xf_4 as realized in Fig. 5 is to have fewer stages than the circuit realization for f_3 , at least two of the conjunctions involved in the factorization must be reduced in delay by at least two. Thus a lower bound on the number of common literals that must be factored out is $a^{(i-1)} + 1 - a^{(i-2)}$. Also, it follows from the above that the minimum value of i which should be considered for an in-group factorization is two.

Even though in a particular problem no one in-group factoring may by itself reduce the total circuit delay by g stages, the sum of the individual reductions of several such factorizations may effect the necessary reduction. From (9) we have that R_i , the reduction caused by a factorization involving only conjunctions of delay i , is

$$R_i = (k_i - k'_i) \cdot n^i - n^{(i+q_i)} \quad (10)$$

If the sum of the reductions caused by several in-group factorings is sufficient to reduce the total circuit delay by the desired amount, then the following relationship must be true:

$$R_{i_1} + R_{i_2} + \dots + R_{i_v} \geq D_c(g) \quad (11)$$

where i_1 is the smallest delay and i_v is the largest delay of the conjunctions involved in the factoring. Thus a tabulation may be kept of the reductions, R_{i_j} , obtained by the possible factorizations. If the sum of any subset of these numbers is greater than or equal to $D_c(g)$, the corresponding factorizations will effect the required reduction in delay. Note that if the indices i_j of the individual factorizations are all different, we are guaranteed that the sets of conjunctions involved are all disjoint.

OUT-OF-GROUP FACTORING

The treatment of out-of-group factoring is quite similar to that of in-group factoring. In this case, however, the conjunctions of (5) are of different delay. Let i_1 be the smallest and i_v be the largest delay of the conjunctions involved in the factorization. If the factorization effects the required reduction in the number of stages of logic then

$$(k_{i_1} - k'_{i_1})n^{i_1} + \dots + (k_{i_v} - k'_{i_v})n^{i_v} - n^{(i_v+q)} \geq D_c(g) \quad (12)$$

where $i_v + q$ is the delay of the subcircuit which realizes Xf_4 .

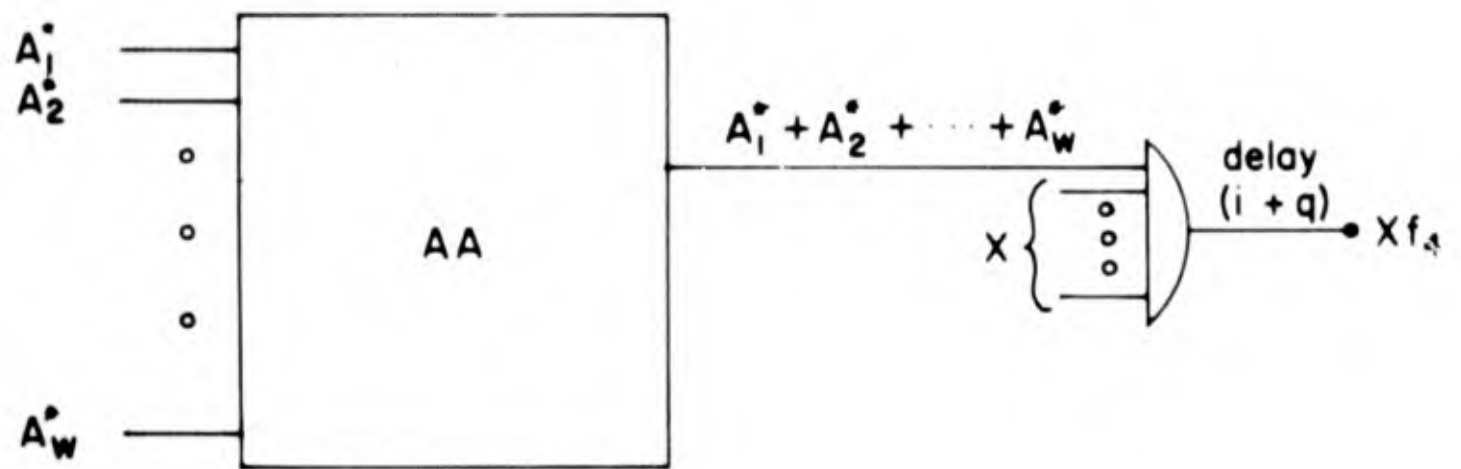


Figure 5.

Using reasoning similar to that employed in the case of in-group factorization, bounds can be obtained for the corresponding parameters in this case. Thus $q < t$ where $i_q + t$ is the minimum number of stages necessary to realize (5). Also $i_1 \geq 2$ and the minimum number of common literals which must be factored is $a^{(i_1-1)} + 1 - a^{(i_1-2)}$.

CONCLUSION

A method has been presented for minimizing the number of stages of logic required to realize the sum-of-products expression for a switching function when the logical gates to be used have fan-in limitations. The method is easily extended to provide the basis for a test which determines the effect of a given factorization on the number of stages of logic required. It should be noted that the method is most useful for situations in which either the number of literals or the number of conjunctions or both is large compared with the fan-in limitations of the gates used.

ACKNOWLEDGMENT

The authors would like to thank Professor E. J. McCluskey of the Department of Electrical Engineering, Princeton University, who suggested this problem.

APPENDIX

Theorem 3. The number of stages necessary to realize a switching function, F , is at least as great as the number of stages necessary to realize any product term of the sum of products expression for F .

Proof: Assume F is a function of x variables. Let $\mathcal{C}$ be a circuit realization of F which requires the minimum number of stages when the fan-in for both AND and OR gates is limited. Let c be the delay of $\mathcal{C}$. The circuit realization, $\mathcal{C}$, may be based on a particular factoring of the sum of products form, f , of the function F , where

$$f = A_1 + A_2 + \dots + A_r$$

Consider any of the product terms, for example A_1 . Suppose a minimum stage realization of A_1 requires h stages where $h > c$. For purposes of this proof, it is necessary to show that by merely changing the signals on some of the input leads, the circuit $\mathcal{C}$ can be changed to realize only A_1 . The procedure for making this change will be carried out in two steps.

Step 1. Suppose A_1 is a product of u literals. If the x input variables of F are $v_1, v_2, \dots, v_u, \dots, v_x$, then A_1 can be expressed, without loss of gen-

erality, as $A_1 = A_1(v_1, v_2, \dots, v_u)$. A_1 then covers 2^{x-u} minterms and at least one of these minterms is not covered by another product term of f . Call this particular minterm A_{11} . A_{11} is sometimes referred to as a distinguished fundamental product.

Consider the following assignment of values, λ , to the variables $v_{u+1}, \dots, v_x$ which do not appear in A_1 .

$$\lambda \begin{cases} \text{let } v_j = 0 \text{ if } \bar{v}_j \text{ is a literal of } A_{11} \\ \text{let } v_j = 1 \text{ if } v_j \text{ is a literal of } A_{11} \\ u+1 \leq j \leq x \end{cases}$$

The sum of products expression f under the assignment λ , denoted $f|_\lambda$, is a function of only the variables $v_1, \dots, v_u$ and has the form

$$f|_\lambda = A_1 + A_2|_\lambda + \dots + A_r|_\lambda$$

Note that A_1 is a minterm of $f|_\lambda$. A circuit which realizes $f|_\lambda$ can be obtained from $\mathcal{C}$ by setting all input lines of $\mathcal{C}$ which correspond to the variables $v_{u+1}, \dots, v_x$ to the appropriate DC levels in accordance with the assignment λ . Call this new circuit $\mathcal{C}'$.

Step 2. Suppose some product term $A_i|_\lambda$ of $f|_\lambda$ consists of a subset of the literals of A_1 . This is not possible since it implies that A_i covers A_{11} . Therefore, every product term in $f|_\lambda$, other than A_1 , contains some literals not contained in A_1 . That is

$$\begin{aligned} A_i|_\lambda &= v_j^* \hat{A}_i|_\lambda \\ \text{and} \\ A_1 &= \overline{v_j^*} \hat{A}_1 \end{aligned}$$

where $1 \leq j \leq u$ and v_j^* is a literal. In the circuit $\mathcal{C}'$ disconnect all input leads connected to the complement of literals contained in A_1 and set them to the DC level corresponding to zero. Call this new circuit $\mathcal{C}''$.

As a result of Step 2, at least one literal in every product term of $f|_\lambda$ other than A_1 is set equal to zero. The literals of A_1 , however, are untouched in both Step 1 and Step 2 and thus $\mathcal{C}''$ will have an output of one only when all the literals of A_1 are equal to one. Thus $\mathcal{C}''$ realizes the function A_1 . However, the number of stages in $\mathcal{C}''$, c'' , satisfies

$$c'' \leq c < h$$

which is a contradiction.

REFERENCES

1. S. Abhyankar, "Absolute Minimal Expressions of Boolean Functions," IRE Transactions on Electronic Computers, vol. EC-8, no. 1, pp. 3-8; March 1959.
2. E. L. Lawler, "Minimal Boolean Expressions With More Than Two Levels of Sums and Products," Proceedings of the Third Annual Symposium on Switching Circuit Theory and Logical Design, Chicago, Ill., Oct., 1962, AIEE Publication no. S-141, pp. 49-59; Sept. 1962.
3. A. R. Meo, "On the Minimal Third Order Expression of a Boolean Function," Proceedings of the Third Annual Symposium on Switching Circuit Theory and Logical Design, Chicago, Ill., Oct. 1962, AIEE Publication no. S-141, pp. 5-24, Sept. 1962.
4. T. J. Beatson, "Minimization of Components in Electronic Switching Circuits," AIEE Transactions, vol. 77, part 1, pp. 283-291, July, 1958.
5. E. L. Lawler, "An Approach to Multilevel Boolean Minimization," Journal of Assoc. for Computing Machinery, vol. 11, no. 3, pp. 283-295; July, 1964.
6. J. P. Roth and R. M. Karp, "Minimization Over Boolean Graphs," IBM Journal of Research and Development, vol. 6, no. 2, pp. 227-238; April, 1962.
7. E. J. McCluskey, Jr., "Logical Design of NOR Gate Networks with No Complemented Inputs," Tech. Report No. 34, Digital Systems Laboratory, Dept. of Electrical Engineering, Princeton University, Princeton, New Jersey. Also in Proceedings of Fourth Annual Symposium on Switching Circuit Theory and Logical Design, Chicago, Ill., Oct. 1963, AIEE Publication no. S-156, pp. 137-148; Sept. 1963.
8. E. L. Lawler and G. A. Salton, "The Use of Parenthesis-Free Notation for the Automatic Design of Switching Circuits," IRE Transactions on Electronic Computers, vol. EC-9, pp. 342-352; Sept. 1960.

BLANK PAGE