

ESTI PROCESSED☐ SEC TAB ☐ PROJ OFFICER☐ ACCESSION MASTER FILE

DATE _____

ESTI CONTROL NR **AL 44000**CY NR 7 OF 1 CYB**ESD RECORD COPY**RETURN TO
SCIENTIFIC & TECHNICAL INFORMATION DIVISION
ESTI, BUILDING 1211

COPY NO. _____

COPS

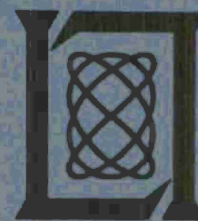
Group Report**1964-31****Input Current Compensation
for Transistor
Operational Amplifiers****J. N. Harris
R. S. Orr****28 October 1964**

Prepared under Electronic Systems Division Contract AF 19(628)-500 by

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts



AD608819

The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the U.S. Air Force under Contract AF 19(628)-500.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

INPUT CURRENT COMPENSATION
FOR TRANSISTOR OPERATIONAL AMPLIFIERS

J. N. HARRIS

R. S. ORR

Group 62

GROUP REPORT 1964-31

28 OCTOBER 1964

LEXINGTON

MASSACHUSETTS

ERRATA SHEET
for Group Report No. 1964-31

The authors have detected the following errors in Group Report No. 1964-31 (J. N. Harris and R. S. Orr, "Input Current Compensation for Transistor Operational Amplifiers," 28 October 1964). Kindly insert this page into your copy of that report.

Page iii

ABSTRACT

The input current of transistor operational amplifiers limits their application for some uses. Several techniques are described which can be employed to reduce this input current to as little as 1 % of the base current of the input transistor. This reduction in input current is maintained over a wide range of temperature. The percentage reduction and the operating temperature span is related to the degree of complexity and precision of the compensating circuit used.

One type of compensation uses a thermistor-resistor circuit. This technique is developed in detail — both analytically and experimentally, and various examples are given. For the case of a transistor having an input current of 50 nA, it is possible to design circuits to reduce this value to as little as 0.5 nA over a 50°C temperature span.

Accepted for the Air Force
Stanley J. Wisniewski
Lt Colonel, USAF
Chief, Lincoln Laboratory Office

Library and Publications
M.I.T. Lincoln Laboratory
P.O. Box 73
Lexington, Massachusetts 02173

ABSTRACT

The input current of transistor operational amplifiers limits their application for some uses. Several techniques are described which result in a substantial reduction of this input current. The resulting input current can range from 20% of the original current over a wide temperature span. The percentage reduction depends on the degree of complexity and precision of the compensating circuit used.

One type of compensation uses a thermistor-resistor circuit. This technique is developed in detail — both analytically and experimentally, and various examples are given. For the case of a transistor having an input current of 50 nA, it is possible to design circuits to reduce this value to as little as 0.5 nA over a 50°C temperature span.

Accepted for the Air Force
Stanley J. Wisniewski
Lt Colonel, USAF
Chief, Lincoln Laboratory Office

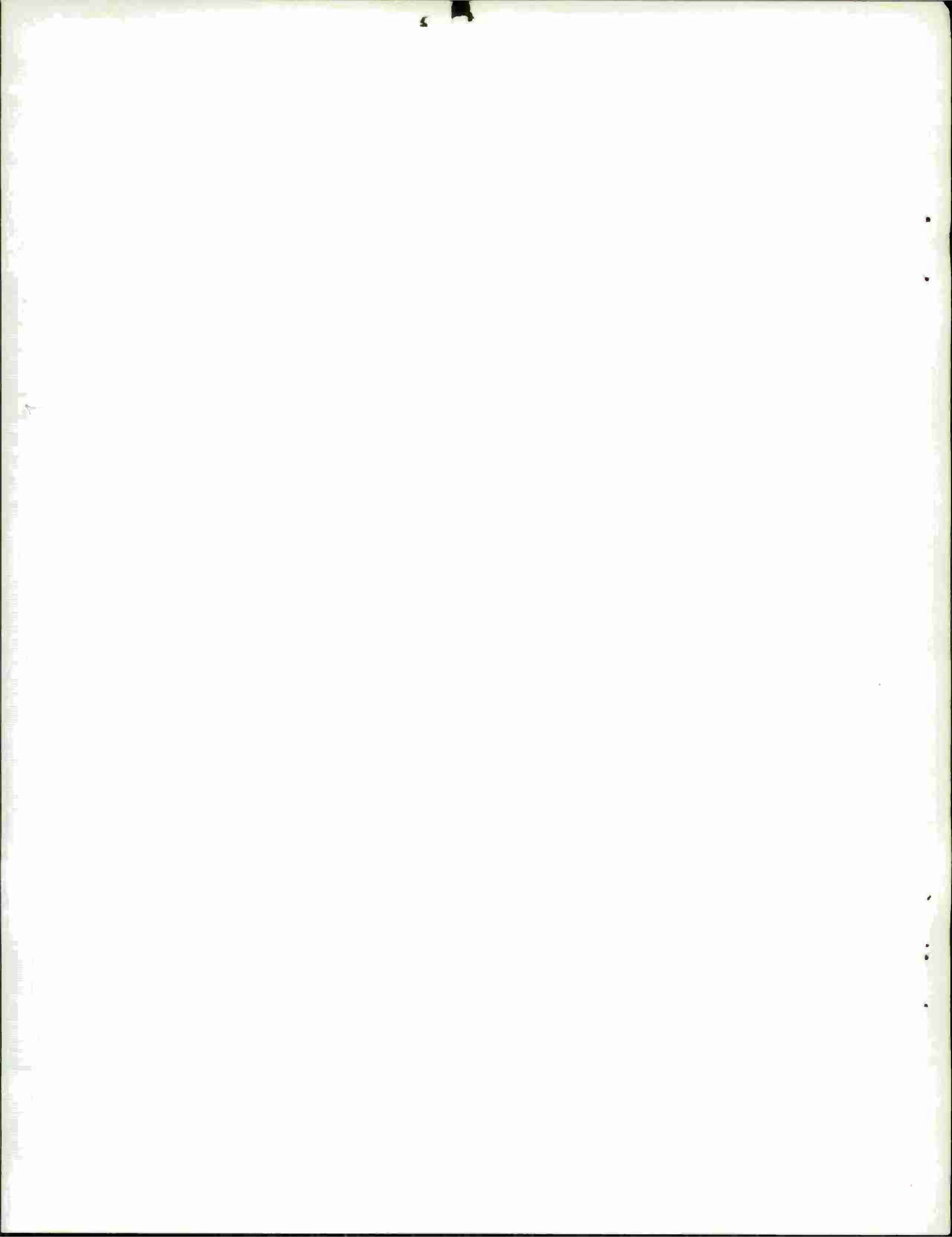


TABLE OF CONTENTS

<u>CHAPTER</u>	<u>PAGE</u>
I SOME CHARACTERISTICS OF TRANSISTOR OPERATIONAL AMPLIFIERS - - - - -	1
II EXAMPLES OF THE EFFECT OF INPUT CURRENT- - - - -	3
A. INVERTING AMPLIFIER - - - - -	3
B. INTEGRATOR - - - - -	4
C. SAMPLE AND HOLD CIRCUIT- - - - -	5
III DESCRIPTION OF TRANSISTOR BASE CURRENT- - - - -	7
A. TRANSISTOR ACTION - - - - -	7
B. TYPICAL BASE CURRENT DATA - - - - -	8
C. COLLECTOR-BASE LEAKAGE CURRENT - - - - -	9
IV TECHNIQUES FOR TEMPERATURE COMPENSATION OF BASE CURRENT- - - - -	11
A. INTRODUCTION - - - - -	11
B. RESISTIVE (CONSTANT-CURRENT) COMPENSATION - - - - -	11
C. CONSTANT TEMPERATURE OVEN- - - - -	12
D. COMPLEMENTARY COMPENSATION - - - - -	14
E. DIODE COMPENSATION- - - - -	15
F. TEMPERATURE SENSITIVE RESISTORS - - - - -	16
1) Resistance Alloy Wire- - - - -	17
2) Silicon Resistors - - - - -	17
3) Silicon Carbide- - - - -	17
4) Thermistors - - - - -	17
G. THERMISTOR COMPENSATION- - - - -	17
H. ADDITIONAL CONSIDERATIONS- - - - -	18
1) Self Heating of Sensor- - - - -	18
2) Increasing the Effective Temperature Coefficient - - - - -	18

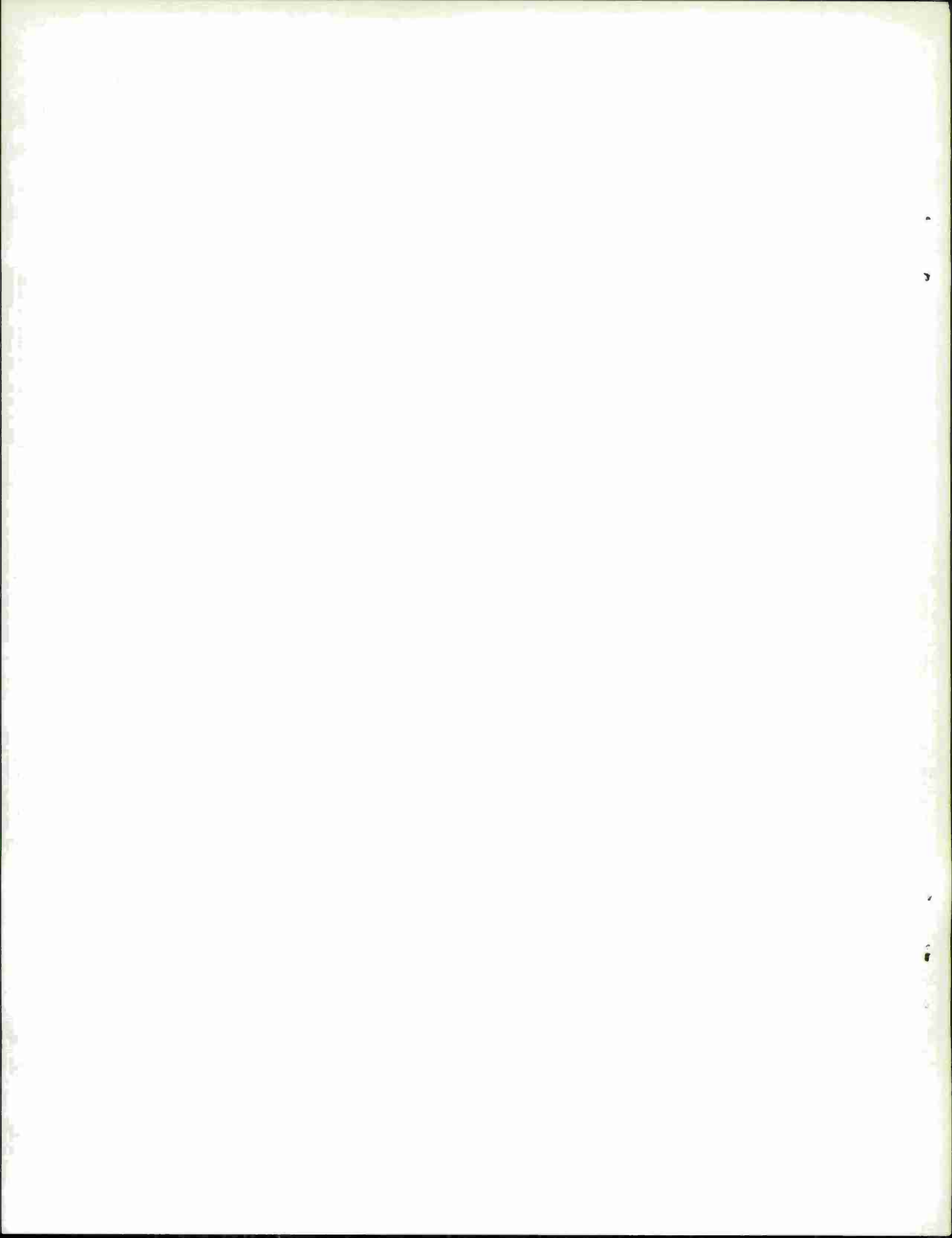


TABLE OF CONTENTS

<u>CHAPTER</u>	<u>PAGE</u>
3) Thermal Contact -----	18
4) Voltage Follower Problem -----	19
I. SUMMARY OF TECHNIQUES -----	19
V ANALYSIS OF RESISTOR-THERMISTOR COMPENSATION -----	21
A. TEMPERATURE TRACKING -----	21
B. CIRCUIT COMPONENTS -----	21
C. CIRCUIT ANALYSIS -----	23
D. SOLUTION PROPERTIES -----	26
E. SUMMARY OF ANALYTIC RESULTS -----	29
VI MEASUREMENT TECHNIQUES -----	31
A. INTRODUCTION -----	31
B. DIODE VOLTAGE -----	31
C. THERMISTOR RESISTANCE -----	31
D. TRANSISTOR BASE CURRENT -----	32
E. OVEN TEMPERATURE STABILITY -----	34
1) Temperature Control -----	34
2) Temperature Gradient -----	35
3) Electrical Noise -----	36
4) Low Temperature Measurements -----	36
F. PARAMETER STABILITY -----	37
1) Introduction -----	37
2) Diode Voltage -----	38
3) Thermistor Resistance -----	38
4) Transistor Base Current -----	38
5) Thermal Time Constant -----	38
6) Conclusion -----	39

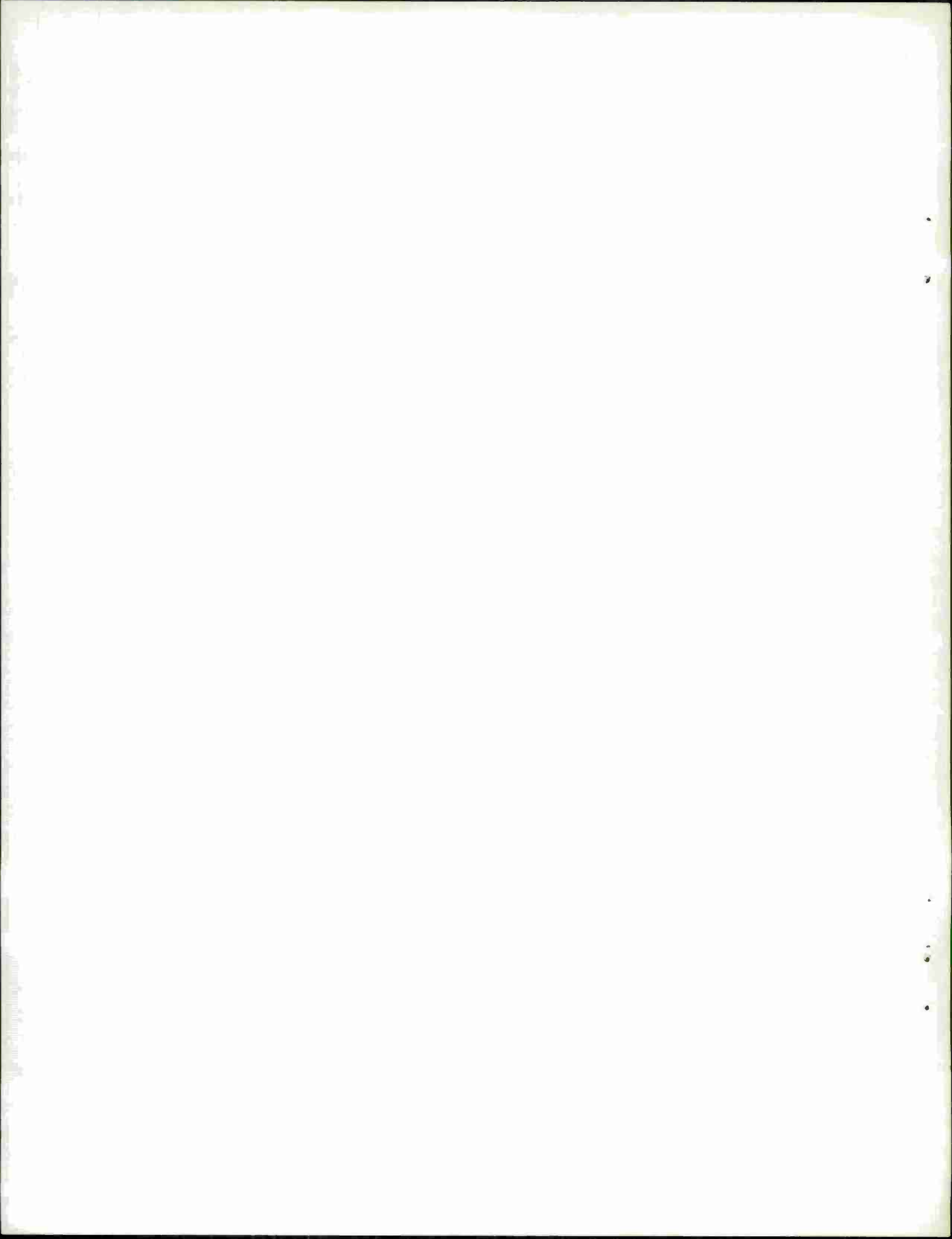
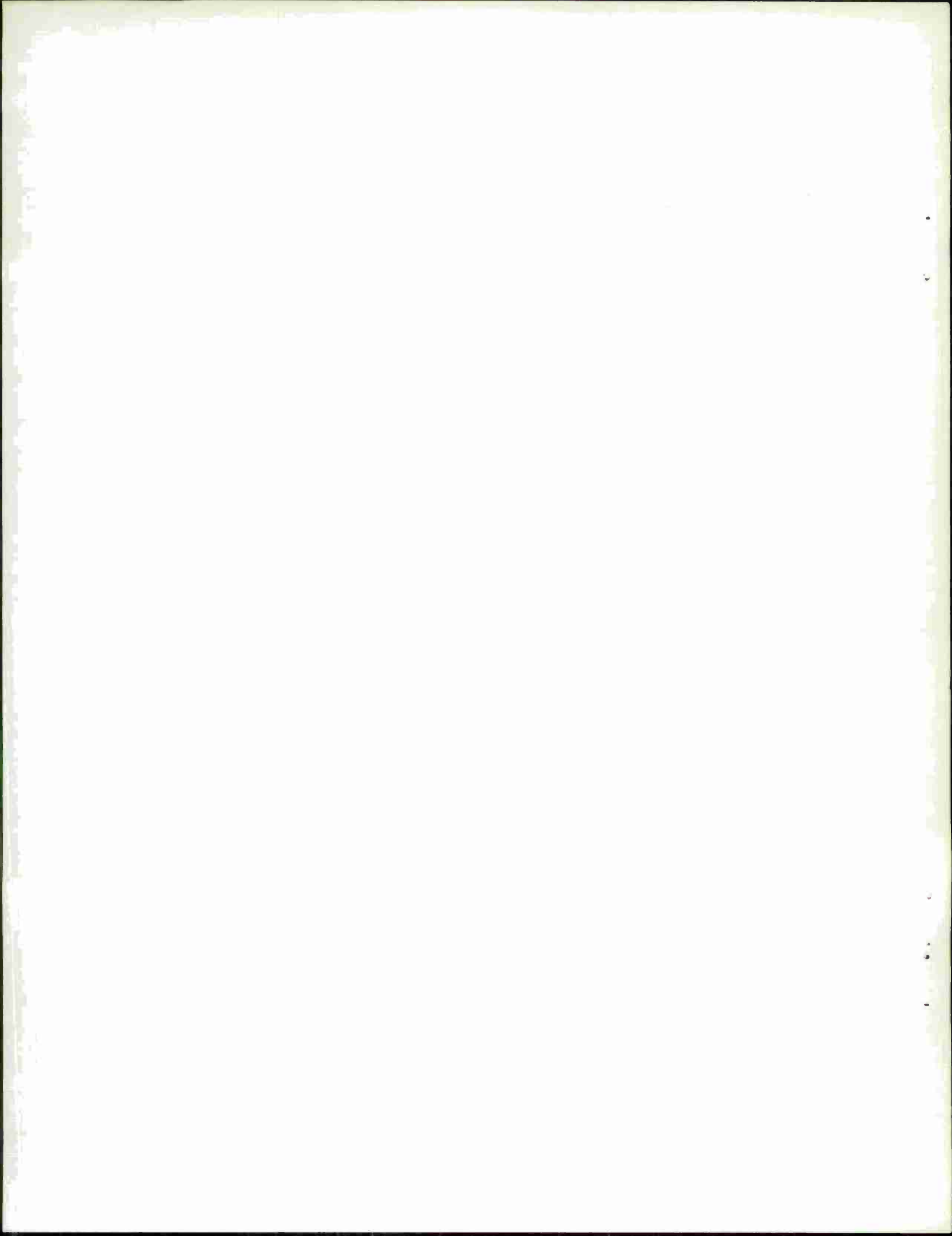


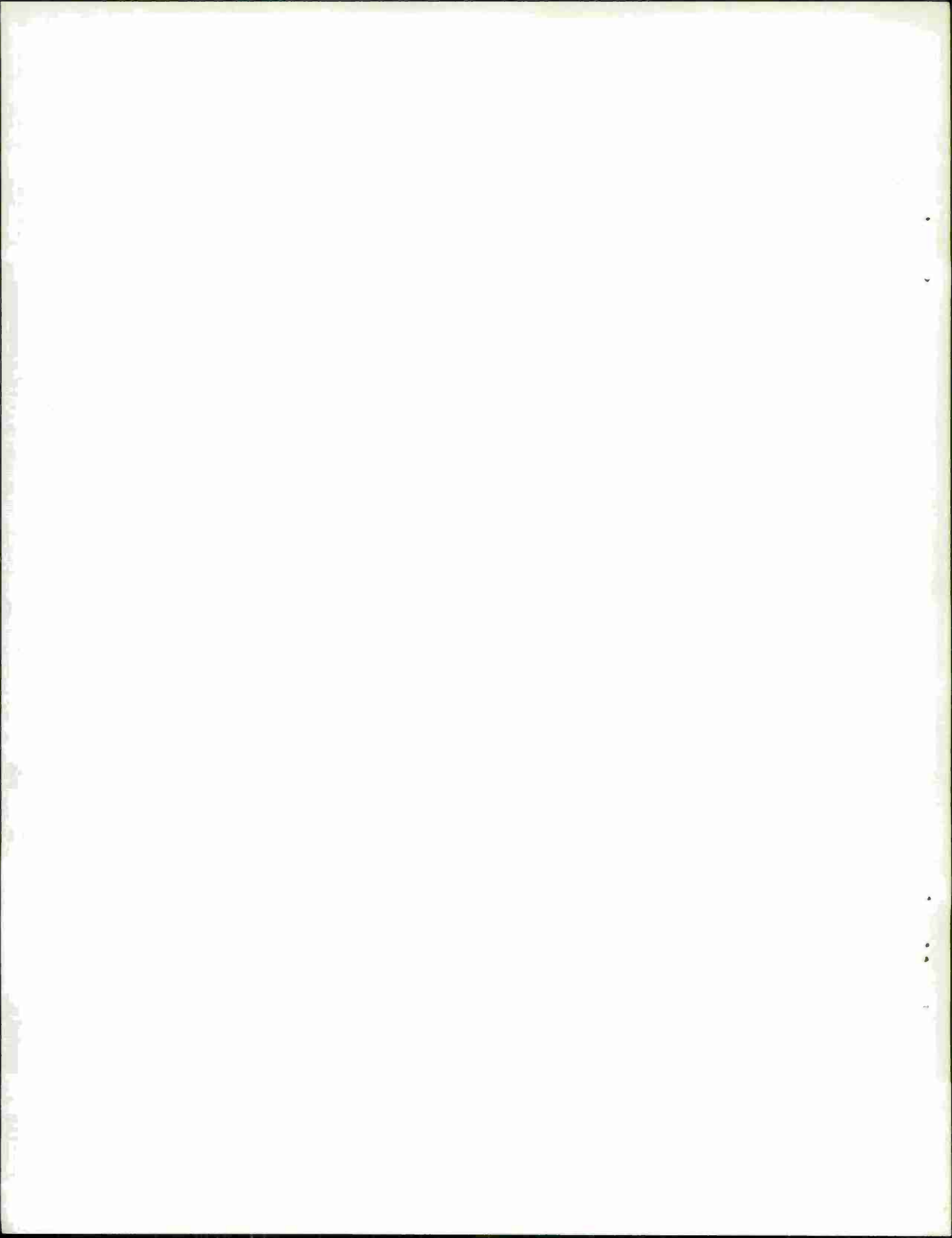
TABLE OF CONTENTS

<u>CHAPTER</u>	<u>PAGE</u>
VII PRACTICAL RESISTOR-THERMISTOR COMPENSATION CIRCUITS - - - - -	41
A. DESIGN CONSIDERATIONS - - - - -	41
1) Scaling Factors and Operating Levels - - - - -	41
2) Self-Heating - - - - -	43
3) Temperature Range - - - - -	44
4) Parameter Variations - - - - -	45
B. PRACTICAL CIRCUITS - - - - -	46
1) Individual vs. Average Compensation - - - - -	46
2) Symmetric vs. Asymmetric Design - - - - -	48
3) Individual-Symmetric Example - - - - -	48
4) Individual-Asymmetric Example - - - - -	54
5) Average-Symmetric Example - - - - -	55
C. SHARED CIRCUITS - - - - -	56
D. VOLTAGE FOLLOWER APPLICATION - - - - -	57
E. CONCLUSIONS - - - - -	60
APPENDIX I Mathatron Program - - - - -	61
APPENDIX II IBM 7094 Program - - - - -	65
REFERENCES - - - - -	73
BIBLIOGRAPHY - - - - -	75
FIGURES - - - - -	77
DISTRIBUTION LIST - - - - -	121



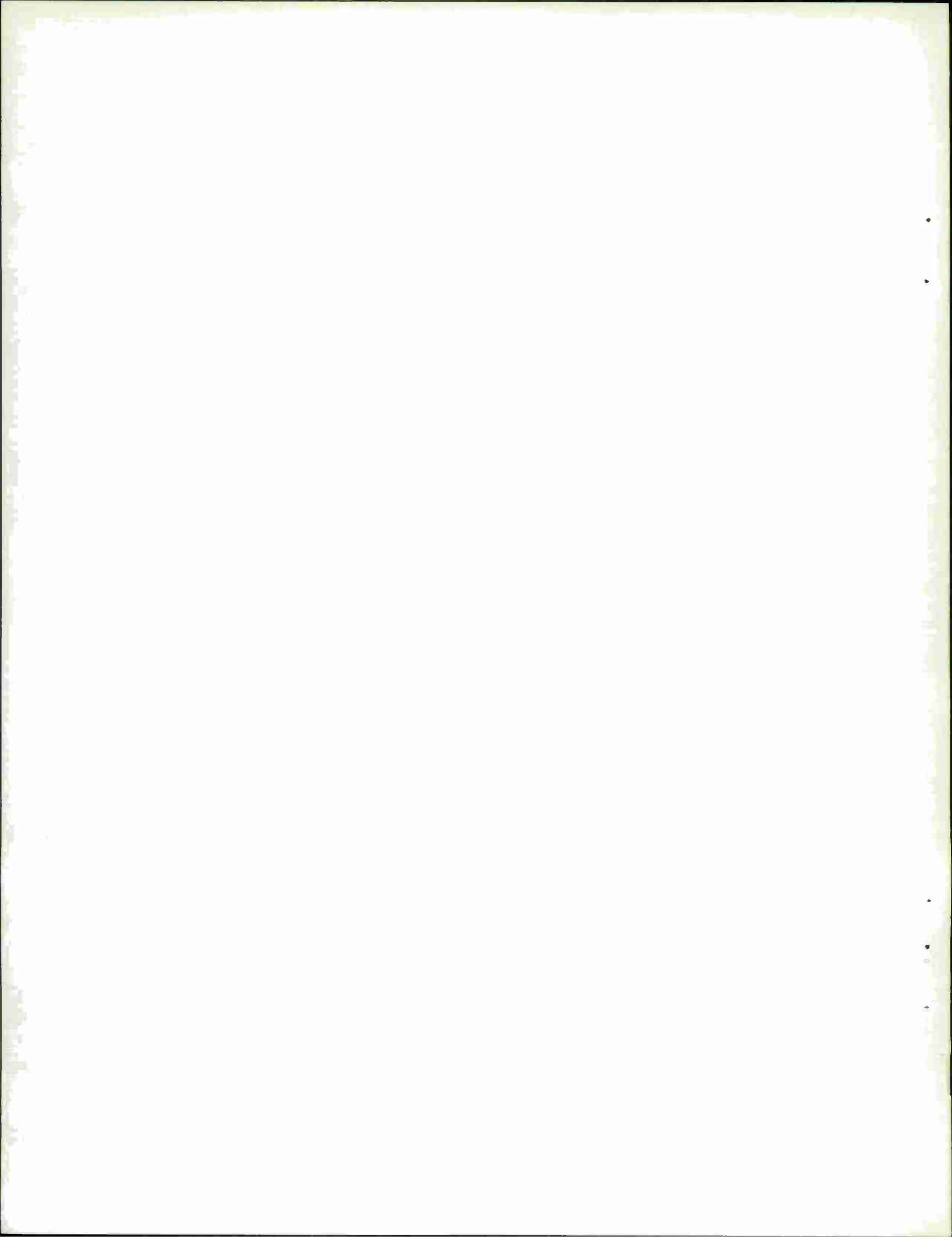
LIST OF FIGURES

Figure No.		Page No.
1.	Inverting Amplifier with Input Leakage Current - - - - -	77
2.	Integrator with Input Leakage Current - - - - -	78
3.	Sample and Hold Circuit with Input Leakage Current - - - -	79
4.	The Ebers-Moll Large Signal Model - - - - -	80
5.	Base Current for the 2N2920 Transistor - - - - -	81
6.	Base Current for the 2N2920 Transistor ($I_C = 10\mu A.$) - - - -	82
7.	Resistive (Constant-Current) Compensation - - - - -	83
8.	Schematic for T0-5 Constant Temperature Oven - - - - -	84
9.	Temperature Variation for T0-5 Oven - - - - -	85
10.	Power Dissipated in T0-5 Oven - - - - -	86
11.	Complementary Compensation Circuit - - - - -	87
12.	Error Current for Complementary Compensation - - - - -	88
13.	Diode Forward Voltage vs. Current - - - - -	89
14.	Diode Forward Voltage vs. Temperature - - - - -	90
15.	Diode, Voltage Temperature Coefficient vs. Forward Current - - - - -	91
16.	Diode Compensation Circuit - - - - -	92
17.	Error Current for Diode Compensation - - - - -	93
18.	Compensation Circuits Using Temperature Sensitive Resistors - - - - -	94
19.	Resistor-Thermistor Compensation Circuit - - - - -	95
20.	Cascade for Increasing the Effective TC - - - - -	96
21.	Compensation for the Voltage Follower Configuration - - - -	97
22.	Comparison of Base Current and Compensating Current - - -	98
23.	Resistance vs. Temperature Curve for a 10K Thermistor - -	99
24.	Analytical Model for Resistor-Thermistor Compensating Circuit - - - - -	100
25.	R_2 and R_p vs. α and γ (Resistor-Thermistor Model) - - -	101
26.	Diode Voltage Measurement - - - - -	102



LIST OF FIGURES (CONTINUED)

Figure No.		Page No.
27.	Thermistor Resistance Measurement - - - - -	103
28.	Transistor Base Current Measurement - - - - -	104
29.	Emitter Current Sources for Input Stage - - - - -	105
30.	Scatter Plot of ℓ , and u Values - - - - -	106
31.	Individual-Symmetrical Compensation Circuit - - - - -	107
32.	Input Current for Individual-Symmetrical Compensation - -	108
33.	Input Current for Individual-Symmetrical Compensation vs. Temperature Span - - - - -	109
34.	Variation of Maximum Input Current vs. Temperature Span - - - - -	110
35.	Input Current for Individual-Asymmetrical Compensation - -	111
36.	Input Current for Average Symmetrical Compensation - - - -	112
37.	Resistive Emitter Current Source, V. F. Application - - - -	113
38.	Improved Resistive Emitter Current Source - - - - -	114
39.	Active Emitter Current Source - - - - -	115
40.	Common-Mode Feedback Emitter Current Source - - - - -	116
41.	Signal Effect on Diode Current - - - - -	117
42.	Active Current Source for Diode - - - - -	118
43.	Alternative Compensation Circuit for V. F. Application - - -	119



CHAPTER 1

SOME CHARACTERISTICS OF TRANSISTOR OPERATIONAL AMPLIFIERS

The availability of well matched transistor differential pairs mounted so that they share a common thermal environment has made possible very high performance transistor operational amplifiers. In addition, the introduction of the passivation technique to transistors, guarantees extremely low reverse currents and long-term stability of the transistor parameters. Together, these two developments permit the design of transistor operational amplifiers which rival and even surpass in some respects the performance of the high quality chopper stabilized vacuum tube amplifier which was once the standard for high performance analog circuits.^{1, 2}

The effects of most amplifier parameters (such as gain, stability, common mode rejection, etc.) are reasonably well understood. Contemporary circuit design of commercial models clearly demonstrates the results of this understanding. A parameter which is often neglected, despite the fact that it causes a certain non-ideal amplifier behavior, is the dc input current. Few amplifiers available today have input current specifications less than ± 10 nA, and frequently the value is as high as ± 100 nA over a reasonable temperature range. Obviously this current may be completely canceled at a fixed temperature by a simple constant current source. However, the strong temperature dependence displayed by the input current, degrades the effectiveness of this technique, when reasonable temperature excursions are considered.

At least two techniques exist which minimize the input current problem — usually at the expense of one or more of the other parameters. Modulation schemes can reduce the input current. The Philbrick P2 amplifier,³ having less than 0.1 nA input current, represents a good example of this technique. However, in this case both bandwidth and noise considerations are sacrificed. Field-effect transistors^{4, 5} (FET) could also be used, with a reduction of input current by one or more orders of magnitude. The FET

probably offers the ultimate solution to this problem. At the present, however, commercial FET models are not available. The difficulty of matching the relevant FET parameters usually results in poorer dc voltage stability than can be obtained with high quality conventional transistors.

This report contains the results of an investigation of the problem of compensating the input current of standard transistorized operational amplifiers over a moderate temperature range. Several practical circuits are presented which compensate the input current so that the maximum remaining error current is less than 10% of its original value. In addition, one technique, which has been employed, has consistently resulted in 1% compensation.

CHAPTER II

EXAMPLES OF THE EFFECT OF INPUT CURRENT

In order to understand the importance of input current compensation, three typical problems will be given. In each case it will be assumed that the input current of the operational amplifier is 10 nA, a typical value for good commercial models.

A. INVERTING AMPLIFIER

Figure 1 shows a common use for an operational amplifier, namely, a fixed-gain, inverting amplifier. As shown in the figure, the input voltage, E_1 , and the currents I_1 , I_2 and ΔI give rise to a node voltage e_n . This in turn is multiplied by the gain of the amplifier, $-K$, to give the output voltage, E_2 . The following equations must hold.

$$I_1 - I_2 = \Delta I$$

$$I_1 = (E_1 - e_n)/R_1$$

$$I_2 = (e_n - E_2)/R_2$$

$$e_n = -E_2/K \quad (2.1a, b, c, d)$$

Solving these equations for E_2 yields

$$E_2 = \frac{-(E_1 - \Delta I_B R_1)}{\left(\frac{R_1}{R_2} + \frac{R_1}{R_2 K} - \frac{1}{K}\right)} \quad (2.2)$$

For the usual case of $K \gg 1$ we get

$$E_2 \approx - \frac{R_2}{R_1} (E_1 - \Delta I_B R_1) \quad (2.3)$$

The output error voltage due to ΔI_B may be expressed as

$$\Delta E_2 = \Delta I_B R_2 \quad (2.4)$$

As a practical example assume,

$$\begin{aligned} K &= 10^4 \\ R_1 &= 10^5 \Omega \\ R_2 &= 10^6 \Omega \\ \Delta I_B &= 10^{-8} \text{ A} \end{aligned}$$

From Eq. (2.4), $\Delta E_2 = 10^{-8} \times 10^{-6} = 10 \text{ mV}$.

B. INTEGRATOR

Figure 2 shows the connection for an integrator. The output voltage will be a function of both the signal current and the input current as indicated below:

$$e_o = -\frac{1}{C} \int (i_s - \Delta I_B) dt \quad (2.5)$$

It is immediately apparent that any input current will result in an error in the output voltage. Assuming a relatively constant signal current and, that $i_s \gg \Delta I_B$, the percent error will be directly related to the ratio $\Delta I_B/i_s$. Thus if the signal current is $1 \mu\text{A}$ and the input current is 10 nA as before, an output voltage error of approximately 1% would be expected.

The input current may represent a more serious error when the integrator is used in a signal detection process. Under the "no signal"

condition, the input current alone will charge the capacitor. If the time interval is long enough, the resulting current may drive the output voltage to full value. An example will illustrate this fact.

Let

$$\Delta I_B = 10^{-8} \text{ A}$$

$$\Delta t = 1 \text{ sec}$$

$$C = .001 \text{ } \mu\text{f}$$

then

$$e_o = \frac{1}{C} \cdot \int_0^1 \Delta I_B dt = \frac{10^{-8}}{10^{-9}} = 10 \text{ volts.} \quad (2.6)$$

C. SAMPLE AND HOLD CIRCUIT

Figure 3a shows a portion of a typical sample and hold circuit. Here the amplifier is used in the voltage follower mode. The capacitor C has been charged to a voltage V through the analog gate which is assumed to have zero open-circuit leakage. When the gate is open circuited, it is desired to hold the charge on the capacitor for an interval of time, Δt . During this time, the voltage will decrease (or increase, depending on the current direction) by an amount, ΔV , due to the finite input current, ΔI_B , as shown in Fig. 3b. If it is assumed that ΔV represents no more than 10% of V, a linear discharge (or charge) rate may be used as a good approximation to the actual exponential rate. Under these conditions the following relation holds:

$$\Delta V = \frac{\Delta I_B \Delta t}{C} \quad (2.7)$$

A practical example will now be given.

$$\begin{aligned}
 \text{Let } \Delta I_B &= 10^{-8} \text{ A} \\
 \Delta t &= 10^{-2} \text{ sec} \\
 C &= 0.01 \mu\text{f} \\
 \text{then } \Delta V &= \frac{10^{-8} \times 10^{-2}}{10^{-8}} = 10^{-2} \text{ volts} = 10 \text{ mV.}
 \end{aligned}$$

One way of decreasing this error voltage due to the input current is to use a larger capacitor. Thus if C is increased to $0.1 \mu\text{f}$, the error would be decreased to 1 mV . This however requires that the charging current through the analog gate be increased by ten times or that the charging time be increased by a factor of ten. If neither of these parameters can be altered, then the only recourse is to reduce the input current ΔI_B . Thus in order to reduce the offset voltage error to 1 mV it is necessary that the input current not exceed 1 nA over the temperature range of interest. This is a most stringent requirement since this may represent as little as 2% of the original uncompensated base current.

CHAPTER III

DESCRIPTION OF TRANSISTOR BASE CURRENT

A. TRANSISTOR ACTION

The V-I characteristics of a transistor are governed by the distribution of minority carriers in the three physically distinct regions. Under ordinary low-injection conditions, the emitter-base and collector-base junctions contain a narrow space-charge region across which the entire V_{EB} and V_{CB} drops may be assumed to occur. The charge motion in the remainder of the regions may thus be described by the field-free diffusion equation, whose solutions depend only upon the minority carrier concentrations at the edges of the space-charge regions. The voltages V_{EB} and V_{CB} cause both the emitter and collector currents to behave as the sum of two terms, the first of which is identical to the ideal diode equation with saturation current I_{ES} (I_{CS}) and the second of which represents a coupling effect whereby the emitter (collector) current depends upon the diode action of the collector (emitter) junction. This behavior is well described by the Ebers-Moll large signal model⁶ (Fig. 4). The consequent equations, specialized to the case of active operation (forward biased emitter and reverse biased collector), are given below:

$$I_E = I_{ES} (e^{qV_{EB}/kT} - 1) + \alpha_R I_{CS}$$

$$I_C = -\alpha_F I_{ES} (e^{qV_{EB}/kT} - 1) - I_{CS}$$

(3.1 a, b)

The resulting input base current is given by

$$I_B = -(I_E + I_C)$$

$$= -(1 - \alpha_F) (e^{qV_{EB}/kT} - 1) I_{ES} + (1 - \alpha_R) I_{CS}$$

(3.2)

The temperature dependence of I_B at constant I_C is obscured by the fact that both the leakage currents (I_{ES} , I_{CS}) and the alphas are functions of temperature. The dependence of the leakage current is fairly well understood, and although there are about six physical components of it which exhibit temperature dependence, the principle contributor is the square of the intrinsic carrier concentration, which can be shown to be proportional to

$$T^3 e^{-E_g/kT}$$

where E_g is the hole-electron ionization energy.

Unfortunately, there is little theoretical understanding of the gain versus temperature characteristic of transistors. Obviously the forward alpha, α_F , affects $I_B(T)$ greatly, since its value is so close to unity in high gain transistors. At high temperatures the $(1 - \alpha_R) I_{CS}$ term may also become significant. This leakage component is in the opposite sense to the beta component of the base current as Eq. 3.2 indicates.

B. TYPICAL BASE CURRENT DATA

The data presented in Fig. 5 show the average base current versus temperature curve at several collector current levels for the 2N2920. The linearity of the curves suggest that the percentage temperature coefficient

$$TC = \frac{1}{I_B} \frac{\alpha I_B}{\alpha_T} I_C \quad (3.3)$$

is very nearly constant with temperature, and decreases slightly with increasing collector current. Data on the leakage current is also included to show its effect at high temperature.

The uniformity of the base current curves over two orders of magnitude change in collector current, indicates that the percentage accuracy of input current compensation should be unaffected by factors such as amplifier gain and frequency response, which tend to influence the

selection of collector current levels. Applications which require an upper limit to the input current also place an upper bound on the collector current.

Figure 6 shows the same base current on a linear scale for $I_C = 10 \mu A$. The temperature coefficient of I_B is about $-1 \%/^{\circ}C$ at this level. Thus the temperature coefficient of β , at constant I_C , is about $+1 \%/^{\circ}C$. However, the coefficient for any one transistor may vary appreciably from this value, a fact which demonstrates the difficulty of the compensation problem and the need for fairly sophisticated solution techniques when the performance criteria are stringent.

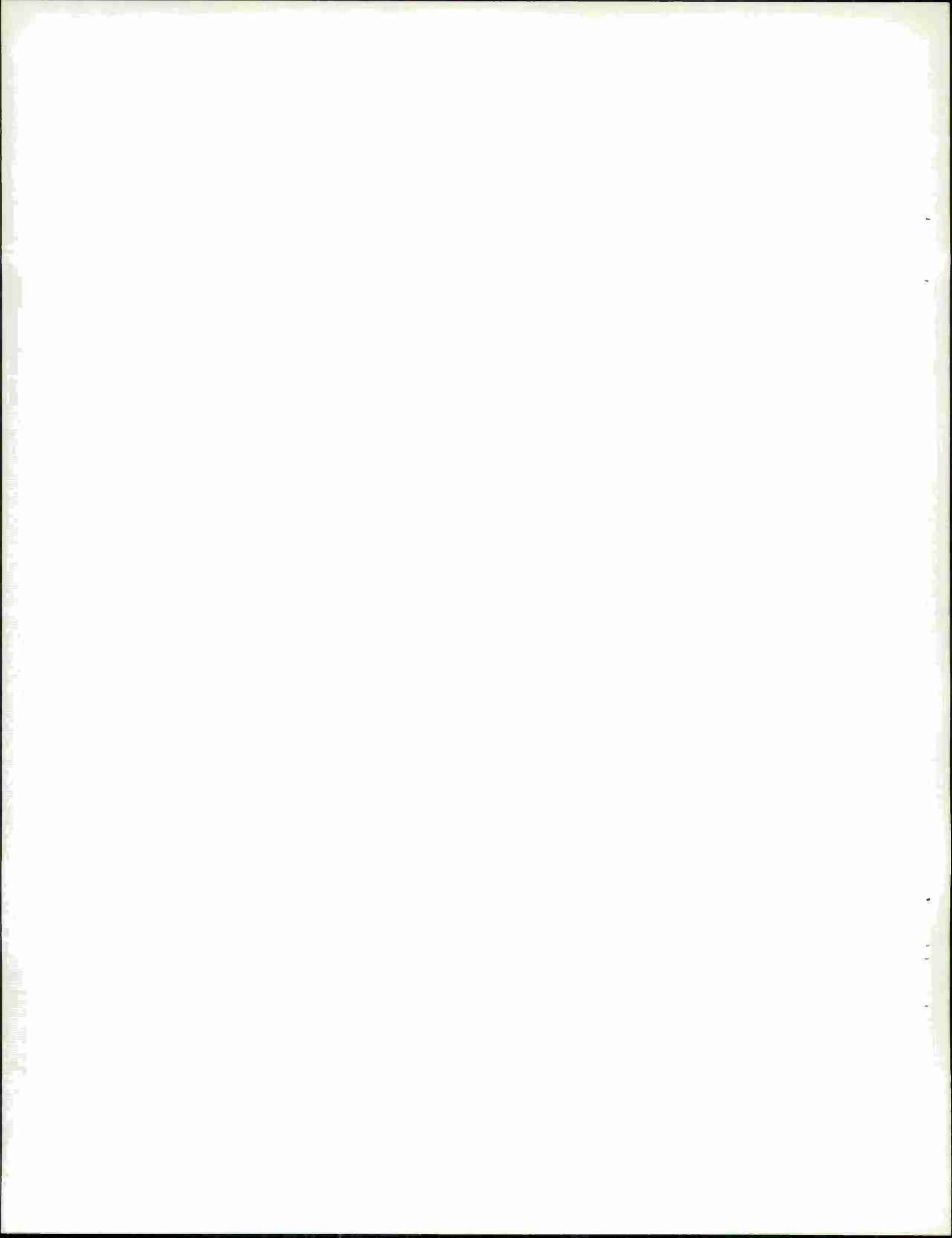
C. COLLECTOR-BASE LEAKAGE CURRENT

Even though it is the total base current which is of concern in the compensating problem, the results of using high leakage transistors are a reduced uniformity of characteristics and poorer long-term stability. The reason for this is that the leakage current is a poorly controlled parameter and hence is more subject to short and long term fluctuations than is β .

In general, the leakage current should be some fraction of the specified final error current, at the highest temperature considered. A rule of thumb for silicon devices is that the leakage current doubles for each $8^{\circ}C$ rise in temperature. Thus from $25^{\circ}C$ to $60^{\circ}C$ the increase in leakage will be about 20 times.

Many high quality, high β transistor pairs will have a leakage of 0.1 nA or less at room temperature. This would result in a leakage of 2 nA or less at $60^{\circ}C$. It is thus apparent that for compensation circuits to be most effective, only transistors with 0.1 nA leakage current at $25^{\circ}C$ should be used.

Traditionally, transistor manufacturers specify a maximum value of 2 to 10 nA at $25^{\circ}C$. However, with modern passivation techniques it would now appear feasible for manufacturers to specify a maximum of 0.1 nA. For precise applications, the user should reject those units which do not meet these stringent specifications.



CHAPTER IV

TECHNIQUES FOR TEMPERATURE COMPENSATION OF BASE CURRENT

A. INTRODUCTION

Figures 5 and 6 show the variation of input base current with temperature. The temperature coefficient is approximately -1% per degree centigrade. One can infer from this fact, that for any temperature compensating circuit to be fully effective, the circuit should contain a temperature sensing element having a temperature coefficient not less than 1% per degree centigrade. In addition, since Fig. 6 indicates a non-linear relationship, either the sensing element must have an essentially identical non-linear characteristic, or it must be incorporated into a network such that its natural characteristic can be modified to conform to the required curve. It should be noted that incorporating a sensor in such network can only serve to decrease its effective temperature coefficient. Thus, to be used in this manner, the sensor should have temperature coefficient larger than the nominal transistor base current temperature coefficient of $1\%/^{\circ}\text{C}$.

B. RESISTIVE (CONSTANT-CURRENT) COMPENSATION

The simplest technique for compensation is to employ a constant current source to supply the input current; adjusting it so that the resulting "error" current is zero at a single fixed temperature. As an example of this technique, consider an input transistor having a beta of 200 and operating at a collector current of $10\text{ }\mu\text{A}$. Figure 7 shows the compensation arrangement. R is very large so as not to shunt the input impedance of the amplifier. For any fixed temperature, exact compensation can be made. At temperatures other than the reference temperature, the uncompensated current will change at a rate of approximately $3/4$ to 1% of the original base current per $^{\circ}\text{C}$. Let us assume a $\pm 20^{\circ}\text{C}$ temperature variation, which would not be unreasonable for a laboratory condition or a controlled field environment. If exact compensation is made at, let us say, 30°C by appropriately adjusting the

compensating current, then at 50°C and at 10°C the uncompensated input current, ΔI_B , would assume values of approximately -10 nA and +10 nA, respectively. The 10 nA value agrees reasonably well with many high quality amplifiers now available. Obviously, by decreasing or increasing the collector current, the net input current will also be decreased or increased with corresponding changes in the other characteristics such as gain, frequency response and input impedance. The 10 nA value represents 20% of the original input current and for many applications may be acceptable. A lower input current over a larger temperature range would, however, greatly increase the utility of the amplifier. This goal can be accomplished by any one of the following techniques, some of which are only slightly more complex than the simple one given above.

C. CONSTANT TEMPERATURE OVEN

Perhaps the most obvious approach to a wide range compensating circuit is to simply avoid the problem by enclosing the input transistor in an oven whose temperature is controlled at a temperature higher than the maximum expected environmental temperature. Unfortunately, for today's miniature circuits and low power requirements, this approach is usually impracticable — at least for most component ovens available today. The size of these ovens and their power requirements are outrageously incompatible with the size of an input stage.

For a constant-temperature oven to be practical in this application, the volume probably should be no larger than 0.01 cu. in. and the heater requirements a fraction of a watt. This amounts to be an order of magnitude improvement over most small enclosures available today. It would appear that a completely different approach is required to reach a solution to this problem.

One such approach is to use the heat dissipated in a reverse biased collector junction as a heater for the oven.* The collector current thus

*This idea was suggested by P. R. Drouilhet, Jr., of Lincoln Laboratory.

determines the total heat dissipated. The temperature sensor may be either a forward biased diode which has $\approx 2 \text{ mv}/^{\circ}\text{C}$ temperature sensitivity or a silicon resistor which has a temperature coefficient of $+0.7\%/^{\circ}\text{C}$. The dc control amplifier can easily be an integrated circuit occupying a single "chip". The heater and temperature sensor described above may be mounted on a TO-5 header in close proximity to the differential input pair. Thus, the entire arrangement may be contained in a TO-5 enclosure ($\approx 3/8''$ dia., $1/4''$ high). The dc control amplifier may be contained in a similar enclosure. It is even possible that the single chip containing the dc control amplifier could also be included in the "oven" enclosure. In either case, the reduction in size and power requirement has been achieved — the latter because of the close proximity of the heater to the input stage, and because of the low thermal mass of the assembly.

Although the exact set-up as described above has not been attempted, a reasonable approximation to it has been tried and the performance determined. The approach was to use a dual transistor pair in a TO-5 enclosure. One transistor of the pair was used for the heater described above; the base-emitter diode of the other transistor was used as the temperature sensor. The dc control amplifier was built externally using standard components. (See Fig. 8.)

Initially, the forward voltage of the base-emitter diode was measured over a wide temperature range. Using this data, the reference voltage of the dc control amplifier was set to give the desired temperature. Conversely, the temperature of the diode (and the oven assembly) may be determined by measuring the diode voltage during operation.

Figure 9 shows the actual temperature variation of this "oven" as the ambient temperature is varied over a range of $0 - 70^{\circ}\text{C}$. As can be seen, the variation is $\pm 2^{\circ}\text{C}$ over a 55°C range. The virtue of this solution is quite apparent. In addition, we have the elegance of proportional control which gives rapid and smooth control of the temperature with no switching transients to upset sensitive circuitry.

The power required to operate this oven varied from nearly 1 watt at 0°C ambient to zero power at an ambient temperature of 75°C, which was the maximum heater operating temperature. (See Fig. 10.) In the usual transistor assembly, the object is to remove heat from the inside to the outside. In this application, however, the object is to reduce the heat loss by an appropriate design. A small insulating cover over the transistor would reduce the heat loss considerably. With these techniques, it should be possible to reduce the power requirements to a fraction of that indicated on the graph.

It is conceivable that all of the circuitry could be realized as a hybrid multi-chip assembly or a single-chip integrated structure. The isolated differential pair would be located so as to share the relatively stable temperature environment created by the heater and control circuitry.

The above solution permits the simple resistive compensation circuit of Fig. 15 to be used. Since the oven temperature is controlled to $\pm 2^\circ\text{C}$ over a 55°C range in ambient temperature, the input current could be compensated and maintained to within approximately $\pm 2\%$ of the nominal base current at the controlled temperature. This would result in an input current of about $\pm 1\text{ na}$, assuming a controlled temperature of 75°C and a base current of 50 na at 25°C . Even if other factors increased this input current by several times it still would be less than that usually specified for standard operational amplifiers. The improvement for integrated operational amplifiers is potentially greater since compensation usually is not employed.

Because of the high operating temperature, the beta of the transistor will increase approximately 50% above the room temperature value. The corresponding decrease in base current relaxes the compensation problem. This advantage may be partially offset by the increase in leakage current which contributes to current instability. (See III C.)

D. COMPLEMENTARY COMPENSATION

A common technique for any temperature compensation is to use an identical component which has a temperature coefficient of the opposite sense. The base current of all transistors decreases with temperature.

For a complementary transistor, the base current decreases in the opposite sense. This leads to an arrangement which may be used as a compensating circuit. Figure 11 shows a circuit incorporating this approach. Both transistors should have similar temperature coefficients of beta in order to achieve close compensation.

By adjusting R in Fig. 11, the base current of the PNP transistor may be varied so as to match the base current of the NPN transistor (the input stage) at one temperature — usually room temperature. The match between their respective temperature coefficients of beta will then determine the degree of "tracking" which may be attained over a given temperature range.

To illustrate this technique, an input stage consisting of an NPN SA2320, operated at a collector current of $10\text{ }\mu\text{A}$, was compensated by a PNP 2N3251, transistor. A number of different SA2320 transistors were tried. The total range of beta for these units was about 2:1. A representative family of error currents for five of these transistors is shown in Fig. 12. The shapes of the curves and the resultant error currents are apparently related to the variations of the temperature coefficients with temperature. The data does not seem to be correlated with beta — at least with this small sample.

This technique illustrates a very simple and economical method for achieving compensation. The "error" current is less than 5 nA or 10% of the original base current over a temperature range of at least 60°C . Because of its simplicity, this method would lend itself admirably to integrated operational amplifiers where an order of magnitude reduction in input current might be achieved.

E. DIODE COMPENSATION

The forward voltage of a diode decreases as the forward current decreases and as the temperature increases. These relationships are shown in Figs. 13 and 14 for an SG22 diode. The voltage temperature coefficient, dV_f/dT , may range from 1.8 to $3.0\text{ mV}/^{\circ}\text{C}$ depending on the

bias current, temperature and the particular diode design. At room temperature, the voltage temperature coefficient for an SG22 diode is a decreasing function of the forward bias current as shown in Fig. 15.

At room temperature and with $I_f = 1 \text{ ma}$, the percentage temperature coefficient, $(1/V_f)(dV_f/dT)$, is about $1/3\%/^{\circ}\text{C}$. As I_f decreases, both $(1/V_f)$ and (dV_f/dT) become larger as indicated in Figs. 13 and 15. For $I_f = 1 \mu\text{A}$, the percentage temperature coefficient can become as high as $3/4\%/^{\circ}\text{C}$, depending on the particular diode. This is large enough to match dI_B/dT of many transistors. The magnitude of the diode current exercises a control over the temperature coefficient. This fact can prove most useful in compensation circuits, as will be seen below.

Figure 16 shows a practical circuit using a diode for compensation. The 15 megohm resistor sets the forward bias of the SG22 diode to approximately $1 \mu\text{A}$. The 1 megohm potentiometer permits adjustment of the compensating current to exactly match I_B at one temperature. At other temperatures, there will be approximate tracking. Figure 17 shows the resulting error current for five different SA2320 transistors. From these curves it can be seen that very good compensation can be achieved with this simple circuit.

It is apparent that this technique becomes less effective if I_B is so great that it becomes an appreciable percentage of the diode current. This is the principal restriction upon this method. It might also be noted that by careful adjustment of the diode current, its temperature coefficient could be made to match that of a particular transistor quite well over a limited temperature range. This could permit an even better compensation than that shown above.

F. TEMPERATURE SENSITIVE RESISTORS

Temperature sensitive resistors may be employed in temperature compensating networks. They are available with both negative and positive temperature coefficients. Figure 18 indicates the generalized circuits which are used in each case. There are a number of components of each type available today, a partial list is given below.

- 1) Resistance alloy wire may have a temperature coefficient ranging from practically zero to about $1/2\%/^{\circ}\text{C}$. The range of values is from a few ohms to perhaps a megohm. The principle disadvantage is the relatively large size, the low temperature coefficient, and the large thermal time constant. The advantage is predictability and long term stability.
- 2) Silicon resistors⁷ have a resistance temperature coefficient of about $+0.7\%/^{\circ}\text{C}$. The temperature coefficient and resistance are quite stable. Resistance values range from about 10Ω to 10 K .
- 3) Silicon Carbide, in the single crystal form (carborundum), has a temperature coefficient of about $-2.4\%/^{\circ}\text{C}$ at 25°C . The nominal resistance value available at present is 2600 ohms . Silicon carbide has the advantage of good electrical stability and inertness to most environmental conditions.
- 4) Thermistors^{8,9,10,11} are usually made from the oxides of manganese, nickel and cobalt, mixed with a binder which is then molded into an appropriate form. The most common thermistors have a negative temperature coefficient which normally ranges from $3-6\%/^{\circ}\text{C}$ although they can be made as low as $0.3\%/^{\circ}\text{C}$. The resistance range is from 100Ω to $10\text{ M}\Omega$. Thermistors with a positive temperature coefficient of about $8\%/^{\circ}\text{C}$ are also available with a resistance range of approximately 10Ω to $100\text{ K}\Omega$. The principle advantages of thermistors are the wide range of values, large temperature coefficient and the great variety of physical shapes which are available (e.g., beads, rods, discs, probes, etc.).

G. THERMISTOR COMPENSATION

The resistor-thermistor circuit shown in Fig. 19 has a voltage transfer function which can have a temperature coefficient ranging from nearly zero up to the temperature coefficient for the thermistor, depending upon the

relative values of the resistors. Due to the great flexibility of this circuit and because its temperature dependent transfer functions can be readily controlled by the use of precision resistors, it was decided to investigate this circuit in detail and to determine the limit of effective compensation possible with it. The remaining chapters of this report will deal with the analysis and application of this circuit to various compensation requirements.

H. ADDITIONAL CONSIDERATIONS

- 1) Self Heating of Sensor. In all of the temperature sensitive elements described above, self-heating is a factor which must be taken into account. In general, the current which operates the TC device should not raise its temperature by more than 1°C above the ambient temperature and preferably much less for accurate compensation. Manufacturers normally list the power ratings of these devices so that the temperature rise may be calculated quite accurately. Self-heating may also become more important at the extremes of the temperature range where the sensing element has extreme values. Such conditions should be investigated for critical circuits. Thermal contact with other circuit elements will alter the self-heating effects. This subject is discussed further in VII-A-2.
- 2) Increasing the Effective Temperature Coefficient. The effective temperature coefficient of resistance of the above devices may be increased by means of a ladder-cascade as shown in Fig. 20. A three stage ladder is shown. By properly choosing the values of R_1 , R_2 , and R_3 the temperature coefficient may be tailored to the value necessary to match that of I_B of the transistor under consideration. The more "stages" which are used, the higher will be the effective temperature coefficient.
- 3) Thermal Contact. It is apparent that good thermal contact between the sensing element and the transistor is desirable.

Ideally the sensing element should be included within the transistor can, but fairly good contact can be made by using epoxy cement to attach the sensing element to the outside of the can or to the bottom side of the header. For less critical circuits it can be mounted in the near vicinity of the transistor. For completely integrated circuits the thermal contact problem can probably be neglected.

- 4) Voltage Follower Problem. When the amplifier is used in the voltage follower (unity gain) configuration (see Fig. 21), the input terminal is no longer a voltage node but will vary directly with the input signal. This use imposes particular constraints on the compensating circuits. It is apparent that first of all the input stage should have an active current source (common-base configuration) in the emitter circuit. This is so that the input current will not vary appreciably with the signal voltage. In addition, the compensating circuit itself must be referenced to the signal voltage. Since the output voltage is a replica of the input, the compensating circuit may be connected to it for reference, thus making the input current correction nearly independent of the signal level. A later section (XII-D) will treat the practical aspects of the voltage follower problem.

I. SUMMARY OF TECHNIQUES

Four distinct methods for temperature compensation of transistor base current have been given, 1) the TO-5 oven with resistive (constant-current) compensation, 2) complementary compensation, 3) diode compensation and 4) resistor-thermistor compensation.

The first three techniques are distinguished by having only one degree of freedom and hence the base current may be cancelled at only one temperature. Above and below this temperature, the error current is very much a function of the characteristics of the particular transistor and compensating element used.

The TO-5 oven technique, which maintains a more or less constant, elevated temperature avoids the problem and very good results can be gotten with it. However the more complex circuitry required can probably only be justified if additional benefits are gained, such as stability of the V_{BE} match of a differential pair. For this case, an improvement of ten times in voltage stability over a wide temperature range could be obtained. This technique could also be used for TC zener diodes, matched diodes, etc., to obtain unusually good voltage stability.

The complementary and diode compensation techniques are particularly valuable because of the simplicity and economy in components and size, thus making them useful for integrated circuits.

The resistor-thermistor compensation has three degrees of freedom, realized by adjustment of R_1 , R_2 and R_3 (or R_F). Figure 16. The base current may thus be cancelled at three different temperatures. If a circuit is matched to the exact measured values of a particular transistor (individual-compensation), precise compensation may be obtained at these three temperatures. If the base current is a smooth, monotonic function of temperature, as is normally the case, good compensation may be expected for in-between temperatures.

If a single circuit is designed for the average transistor characteristics (average-compensation), the compensation will obviously be poorer because of the variability of transistor characteristics. However, because of the three separate design temperatures, a reasonably flat compensation can be expected over this range of temperatures. As a result, the performance is more predictable than that for the single-temperature compensation techniques. These results are equivalent to those obtained in any approximation problem, where the goodness-of-fit improves with the degrees of freedom available.

Because of the flexibility of the three-temperature compensation circuit, this problem is treated in detail in the remainder of the report. Chapter V provides the analytical basis for the design, while Chapter VII gives the results of a number of practical designs, which gives convincing proof of the validity of this design technique.

CHAPTER V

ANALYSIS OF RESISTOR-THERMISTOR COMPENSATION

A. TEMPERATURE TRACKING

The particular configuration of the circuit in Fig. 19 has been chosen because its temperature tracking characteristic may be directly determined. It is apparent that for all "reasonable" component values, the potentiometer, R_3 , may be set so that the base current is exactly matched at one temperature, T_0 . If, in addition, the resistors R_1 and R_2 are appropriately chosen, the compensating current can be made to match the input current at two additional temperatures. The diode in Fig. 19 approximates an ideal voltage source which drives the compensating circuit. As the temperature increases, the net effect of the thermistor is to decrease the voltage across R_3 and hence the compensating current through R_f . This temperature behavior approximates that of the transistor base current over a temperature range which may be specified in the design.

At temperature extremes (relative to T_0), the thermistor approaches either zero or infinite resistance, causing the voltage applied to R_3 to become essentially constant. This results in over compensation at high temperatures, and under compensation at low temperatures. The slope of the compensation at these extremes approaches that of the resistive compensation (see IV-B), but in the vicinity of T_0 , the curve closely tracks that of the base current. This effect is shown in Fig. 22. The remainder of this chapter treats the problem of choosing component values to achieve this type of compensation for a given temperature range.

B. CIRCUIT COMPONENTS

In the previous chapter several possible choices for a temperature sensor have been suggested. The thermistor is selected because of its large temperature coefficient and the degree of manufacturing quality control.

The thermistor resistance vs. absolute temperature behavior is given by

$$R_T = R_{T_0} e^{-\beta \left(\frac{1}{T_0} - \frac{1}{T} \right)} \cong R_{T_0} e^{-\beta(T - T_0)/T_0^2} = R_{T_0} e^{-\beta \Delta T/T_0^2} \quad (5.1)$$

The temperature coefficient of resistance is

$$\alpha = \frac{1}{-R_T} \frac{\partial R_T}{\partial T} \approx \frac{\beta}{T_0^2} \quad (5.2)$$

A typical value⁹ of β , expressed in $^{\circ}\text{K}$, is about 4000. For operation near room temperature ($T_0 \approx 300^{\circ}\text{K}$), a value of .045 (4.5%/ $^{\circ}\text{C}$) is typical for α . Figure 23 shows a typical resistance vs. temperature curve for a 10K thermistor. References 8, 9, 10, 11 discuss some of the electrical properties of thermistors.

In the circuit of Fig. 19, the silicon diode is included not out of necessity but because it provides a convenient voltage source to drive the network. The temperature coefficient of the diode voltage is easily derived from the ideal diode equation.

$$I = I_S (e^{qV/kT} - 1) \quad (5.3)$$

and is

$$\left. \frac{1}{V} \frac{\partial V}{\partial T} \right|_I = \frac{1}{T} - \frac{kT}{qVI_S} \frac{\partial I_S}{\partial T} \quad (5.4)$$

The second term usually predominates, giving a temperature coefficient of about $-.3$ to $-.4\%/^{\circ}\text{C}$ for a silicon planar diode. At a current of 1 mA, the diode voltage decreases about 2.0 mV/ $^{\circ}\text{C}$. This temperature dependence can be absorbed into the model and need not significantly affect the performance.

The dynamic impedance of the diode is given by

$$Z_d(I) = \frac{qV}{kTI} \approx \frac{25 \text{ (mV)}}{I \text{ (mA)}} \text{ ohms at } T = 300^\circ\text{K} \quad (5.5)$$

The diode current and the impedance level of the compensating circuit should be chosen so that the circuit represents a sufficiently small load on the diode. If this is not possible, the dynamic impedance of the diode, which acts as the series impedance of the voltage generator, must be taken into account by a second-order correction. Since this impedance is in series with R_1 , it is necessary to correct for this fact by subtracting Z_d from the calculated value of R_1 giving $R_1'' = R_1 - Z_d$ as the actual resistance used.

C. CIRCUIT ANALYSIS

A detailed study of the analytical model in Fig. 24 is given below. By neglecting both source and load impedances, we effectively assume a cascade of stages isolated by a proper selection of impedance levels in the analysis. Justification for this is provided in Chapter VII.

Consider the voltage transfer function of the network, which is

$$H(T) = \frac{V_f(T)}{V_d(T)} = \frac{1}{1 + \frac{R_1}{R_3} \left(1 + \frac{R_3}{R_2 + R_T} \right)} \quad (5.6)$$

In order to force the input and compensating currents to be equal at the three temperatures T_ℓ , T_o and T_u , the following equations must hold:

$$\begin{aligned} i_\ell &= \frac{V_f(T_\ell)}{R_f} = \frac{V_d(T_\ell) H(T_\ell)}{R_f} \\ i_o &= \frac{V_f(T_o)}{R_f} = \frac{V_d(T_o) H(T_o)}{R_f} \\ i_u &= \frac{V_f(T_u)}{R_f} = \frac{V_d(T_u) H(T_u)}{R_f} \end{aligned} \quad (5.7a, b, c)$$

The subscripts ℓ , o and u indicate lower, middle and upper temperatures, respectively in the above equations.

Equations (5.7a, b, c) may be written in the simplified form

$$\begin{aligned} H(T_\ell) &= \ell H(T_o) \\ H(T_u) &= u H(T_o) \end{aligned} \quad (5.8a, b)$$

by defining

$$\ell \equiv \frac{I_\ell}{I_o} \frac{V_d(T_o)}{V_d(T_\ell)} > 1 \quad (5.9a, b)$$

$$u \equiv \frac{I_u}{I_o} \frac{V_d(T_o)}{V_d(T_u)} < 1. \quad (5.9a, b)$$

The inequalities on ℓ and u arise from the fact that the base current exhibits stronger temperature dependence ($\approx 1\%/^{\circ}\text{C}$), than does the diode voltage ($1/3\%/^{\circ}\text{C}$).

By using the definition of $H(T)$ given in Eq. (5.6), the requirements of (6.8a, b) can be written as

$$\begin{aligned} \ell \left[1 + \frac{R_1}{R_3} \left(1 + \frac{R_3}{R_2 + R_\ell} \right) \right] &= 1 + \frac{R_1}{R_3} \left(1 + \frac{R_3}{R_2 + R_o} \right) \\ u \left[1 + \frac{R_1}{R_3} \left(1 + \frac{R_3}{R_2 + R_u} \right) \right] &= 1 + \frac{R_1}{R_3} \left(1 + \frac{R_3}{R_2 + R_o} \right) \end{aligned} \quad (5.10a, b)$$

where the notation

$$R_o = R_{T_o}; R_u = R_{T_o} e^{-\beta\left(\frac{1}{T_o} - \frac{1}{T_u}\right)}; R_e = R_{T_o} e^{-\beta\left(\frac{1}{T_o} - \frac{1}{T_\ell}\right)} \quad (5.11a, b, c)$$

has been introduced.

If we attempt to eliminate either R_1 or R_3 from either of the above equations, we obtain the following two equivalent forms:

$$\begin{aligned} \frac{R_1 R_3}{R_1 + R_3} = R_1 \parallel R_3 &= \frac{(\ell - 1)(R_2 + R_o)(R_2 + R_\ell)}{R_2 + R_\ell - \ell(R_2 + R_o)} \quad (5.12a, b) \\ &= \frac{(u - 1)(R_2 + R_o)(R_2 + R_u)}{R_2 + R_u - u(R_2 + R_o)} \end{aligned}$$

Thus it is seen that R_1 and R_3 affect the fractional change in voltage transfer function only through their parallel combination

$$R_p = R_1 \parallel R_3 = \frac{R_1 R_3}{R_1 + R_3} \quad (5.13)$$

The minimum value of the transfer function occurs for the case $R_3 = R_p$, $R_1 = \infty$, and it increases monotonically with R_3 from zero to a maximum at $R_3 = \infty$, $R_1 = R_p$. This circumstance permits a degree of freedom in the choice of voltage level (and hence the value of R_f) in the compensating current feedback scheme. Some considerations which influence this choice will be discussed in Chapter VII, A-1.

By equating the two expressions for R_p , an expression for R_2 can be obtained which can in turn be used to derive an explicit formula for R_p . The results of these manipulations are:

$$R_p =$$

$$\frac{(\ell - 1)(1 - u)(\ell - u)(R_\ell - R_o)(R_o - R_u)(R_\ell - R_u)}{[(1 - u)R_\ell + (\ell - 1)R_u - (\ell - u)R_o][\ell(1 - u)R_\ell + u(\ell - 1)R_u - (\ell - u)R_o]} \quad (5.14a, b)$$

and

$$R_2 = \frac{\ell(1 - u)R_o R_u + u(\ell - 1)R_o R_\ell - (\ell - u)R_u R_\ell}{\ell(1 - u)R_\ell + u(\ell - 1)R_u - (\ell - u)R_o}$$

In general, numerical solutions are most easily obtained by solving (5.14b) for R_2 , and substituting into either (5.12a or b) to get R_p .

D. SOLUTION PROPERTIES

The complexity of the expressions for R_p and R_2 obscures some salient properties of the compensation network behavior. These expressions can be simplified considerably by introducing a few simple, and quite realistic assumptions. Assume that the thermistor resistance and the input current vary exponentially with temperature. If we restrict ourselves to symmetric compensation, i. e.

$$T_u - T_o = T_o - T_\ell = t \quad (5.15)$$

then we will have

$$\ell = e^{\gamma t}; u = e^{-\gamma t}; (\gamma > 0) \quad (5.16a, b)$$

and

$$R_\ell = R_o e^{\alpha t}; R_u = R_o e^{-\alpha t}; (\alpha > 0) \quad (5.17a, b)$$

The solutions reduce to

$$R_p = R_o \frac{(e^{2\gamma t} - 1)(e^{\alpha t} - e^{-\alpha t})}{(e^{\gamma t} - e^{-\alpha t})(e^{\alpha t} - e^{\gamma t})}$$

$$R_2 = R_o \frac{1 - e^{(\gamma - \alpha)t}}{e^{\gamma t} - e^{-\alpha t}} \quad (5.18a, b)$$

Of primary concern is the requirement that R_p and R_2 be positive. The only factors in R_p and R_2 which can be negative are $(e^{\alpha t} - e^{\gamma t})$ and $(1 - e^{-(\gamma - \alpha)t})$. However, the simple solution

$$\alpha \geq \gamma \quad (5.19)$$

is both necessary and sufficient to guarantee that both R_p and R_2 are positive. This result confirms the intuitive notion that the temperature sensor in the compensating circuit must have at least as large a temperature coefficient as the current to be compensated.

In the special case, $\gamma = \alpha$, R_1 approaches ∞ , and the combination of V_d and R_1 must therefore appear to be a current source. For these conditions, R_2 goes to zero, and R_3 becomes infinite. The result is that thermistor voltage drives R_f directly. Practically, it is sufficient that both R_1 and R_3 be large relative to R_T for the above conditions to be satisfied.

In many cases, we may wish to ask the question: what should the relationship between alpha and gamma be? The two problems stated below are different ways of asking this question; fortunately, the answer is the same in either case.

The problem statements are:

1. Given a particular transistor (hence a fixed value of γ), what value of α will minimize the dependence of R_2 and R_p on variations in α ?

2. Given a particular thermistor (hence a fixed value of α) what value of γ will minimize the dependence of R_2 and R_p on variations in γ ?

The two problems are equivalent to minimizing compensation sensitivity to variations in the thermistor and transistor characteristics, respectively.

The curves of Fig. 25a, b give the answer to the first problem. For a given γ_0 , both derivatives

$$\left. \frac{\partial R_2}{\partial \alpha} \right|_{\gamma_0} \quad \text{and} \quad \left. \frac{\partial R_p}{\partial \alpha} \right|_{\gamma_0}$$

approach zero monotonically as $\alpha \rightarrow \infty$. Hence we desire an alpha as large as possible.

The corresponding curves of Fig. 25c, d indicate that for fixed α_0 , we prefer γ as small as possible. The general result is that sensitivity to errors in component values is minimized when the temperature sensor has a much larger temperature coefficient than does the current to be compensated. A similar result could be expected for asymmetric compensation.

An implication of this result relates to the "average compensation" problem, which involves the selection of a compensation circuit based upon some typical figures for particular lot of transistors. The circuit is to perform reasonably well for any of these transistors. Figure 25c, d implies that a circuit designed for the average ℓ and u should perform reasonably well if the thermistor has a large temperature coefficient. Although Eq. (5.2) indicates a variation of α with the temperature, T_0 , the magnitude of this variation over the usual range of operating temperatures is sufficiently small that the choice of T_0 is not significantly restricted.

E. SUMMARY OF ANALYTIC RESULTS

The major result of the above analytic work has been to derive equations for the resistor values required by the compensating network, given the following necessary parameters:

Crossover Temperatures	T_ℓ	T_o	T_u
Thermistor Resistance	R_ℓ	R_o	R_u
Diode Voltage	$V_d(T_\ell)$	$V_d(T_o)$	$V_d(T_u)$
Transistor Base Current	I_ℓ	I_o	I_u
Shunt Potentiometer		R_3	

An orderly computational procedure is as follows:

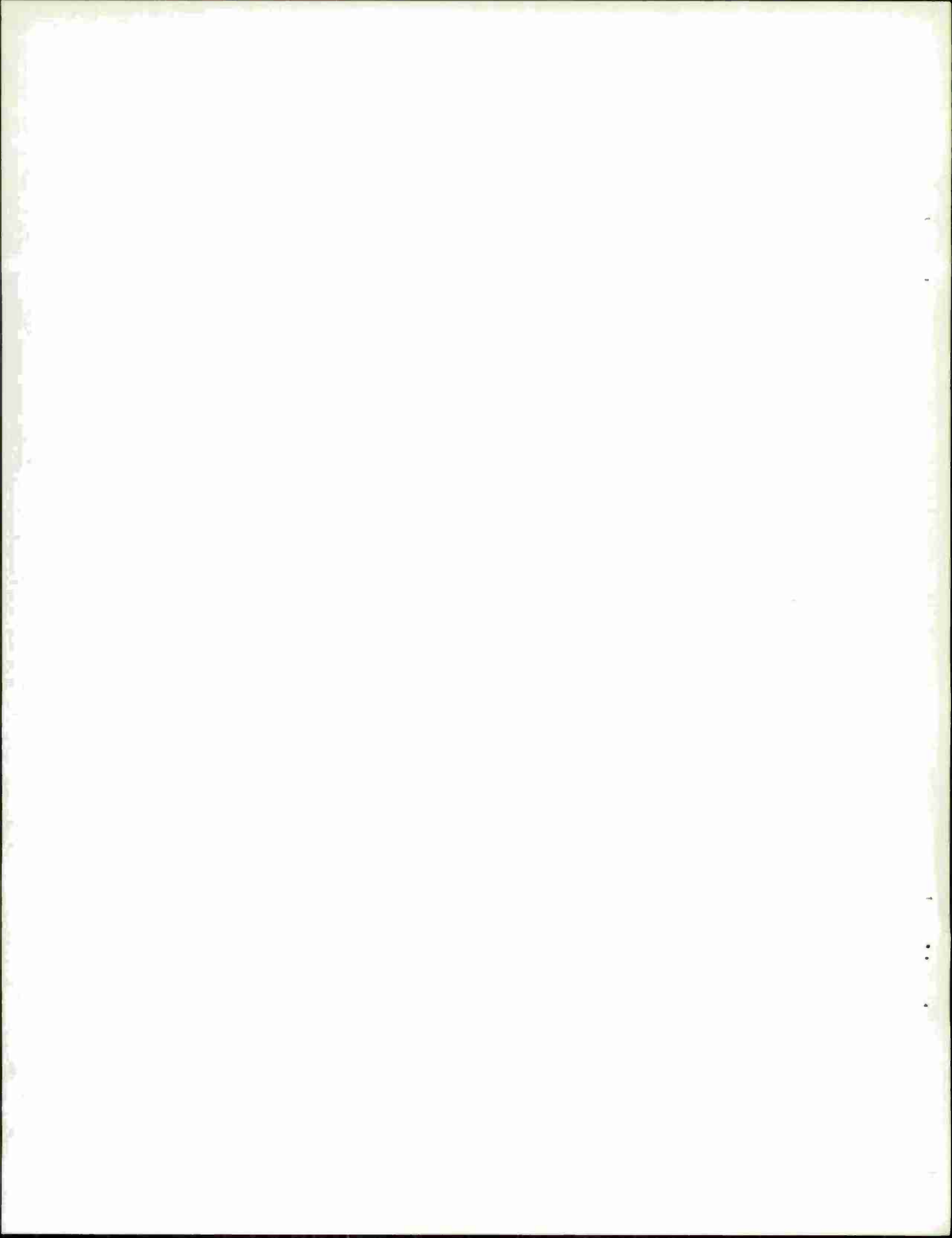
$$\begin{aligned}
 1. \quad \ell &= \frac{I_\ell}{I_o} \frac{V_d(T_o)}{V_d(T_\ell)} \\
 u &= \frac{I_u}{I_o} \frac{V_d(T_o)}{V_d(T_u)}
 \end{aligned} \tag{5.9a, b}$$

$$2. \quad R_2 = \frac{\ell(1-u)R_oR_u + u(\ell-1)R_oR_\ell - (\ell-u)R_uR_\ell}{\ell(1-u)R_\ell + u(\ell-1)R_u - (\ell-u)R_o}$$

$$3. \quad R_p = \frac{(\ell-1)(R_2 + R_o)(R_2 + R_\ell)}{R_2 + R_\ell - \ell(R_2 + R_o)} \tag{5.12a}$$

$$4. \quad R_1 = \frac{R_3 R_p}{R_3 - R_p} \tag{5.19}$$

$$5. \quad R_1'' = R_1 - Z_d \text{ (correction for the diode impedance)} \tag{5.20}$$



CHAPTER VI

MEASUREMENT TECHNIQUES

A. INTRODUCTION

In order to achieve the most accurate compensation, it is necessary to measure the relevant electrical parameters rather carefully. If 1% compensation is desired, it is apparent that measurements must be made to better than 1%. Although this presents no problem as far as the diode measurement is concerned, the measurement of the thermistor resistance and the transistor base current is more difficult. The former because of self heating and the latter because of the very small current involved. These matters will be discussed more fully below.

B. DIODE VOLTAGE

The simplest method for measuring the diode voltage is to connect it to a constant current power supply (or the actual current source which is to be used) and simply measure the forward voltage with a potentiometer or a digital voltmeter. It is easy to achieve an accuracy of a fraction of a mV which represents better than 0.1%, more than enough accuracy for all conceivable circuits. Figure 26a, b shows this set-up.

C. THERMISTOR RESISTANCE

The problem arising in the measurement of the resistance of the thermistor is due to self-heating. Usually the thermistor is measured in a bridge circuit. The current in the arm of the bridge, containing the thermistor, will cause a slight rise of the thermistor temperature due to the I^2R loss which is dissipated in it. Since the temperature coefficient of the thermistor is so large, this rise in temperature may cause an appreciable "error" in the value of the resistance measured. Actually, what is being measured is the resistance at a temperature somewhat higher than the ambient.

This effect may be reduced to a negligible amount by reducing the current in the bridge. This, however, also reduces the sensitivity of the bridge so that it may be necessary to employ a much more sensitive detector. This, in turn, increases the sensitivity to noise pick-up, so that shielding may be required.

The actual amount of temperature rise due to self-heating can be approximately determined by measuring the voltage across the thermistor, while in the bridge, with a high input impedance voltmeter, Fig. 27. The power dissipated in the thermistor is E^2/R and the temperature rise is calculated by multiplying this power by a constant, k , which is given by the manufacturer for that particular thermistor. The amount of temperature rise is dependent on the temperature coefficient, the mass of the thermistor element, its resistance and the current through it. An additional fact which must be considered is the thermal time constant. This is governed by the thermal capacity of the entire thermistor, including any inert material surrounding the actual element, such as glass or epoxy, and the thermal properties of the immediate environment. This effect is seen as a "time lag" between the adjustment of the bridge and the reading of the null detector.

Finally, it should be pointed out that although the above considerations suffice to determine the "absolute" resistance-temperature function of the thermistor, in actual use, the thermistor always has some current through it and hence some self-heating. Thus it would appear that the measurement which is really needed is that of the thermistor resistance when it has approximately the same voltage drop and thermal surroundings as in the compensating circuit. Only a calculation or measurement of these various effects can give assurance of the desired results for a given degree of compensation.

D. TRANSISTOR BASE CURRENT

Assume, as in previous examples, that the base current of the transistor is approximately 50 nA. It would be desirable to measure this current to an accuracy of 0.1 nA or 0.2%. Because of the inherent noise of the transistor it is necessary that some degree of averaging or integrating

technique be used to permit consistent measurements. A time constant of somewhat less than one second, which is typical of some dc meter movements, has proven to be most useful.

Direct reading micro-micro ammeters are available, but their accuracy is limited to about $\pm 3\%$ of full scale reading. Even with overlapping scales and accurate calibration, it may be hard to improve upon this accuracy.

A more reliable and accurate technique is to use a null or balancing technique. Figure 28 indicates the method used. A 4-decade millivolt standard power supply operates into a 10:1 voltage divider to give a standard voltage adjustable in 0.1 mV steps, up to 1.0000 volts and accurate to $\pm 0.05\%$. The series, precision, wire-wound, 10 megohm resistor, also accurate to $\pm 0.05\%$, becomes the precision current source which will supply the base current. The null meter, referenced to ground, indicates when the standard source current, I_S , exactly equals the input base current I_B . By adjustment of the millivolt standard, current balance may be achieved. The first decade (with the 10:1 divider) thus becomes $10^{-1}/10^7$ or 10 nA per step. The last decade is $10^{-4}/10^7 = 10^{-11}$ or 10 pA per step. Both the accuracy and resolution are thus seen to be sufficient. At peak sensitivity, the null meter has only 1 mV for full scale deflection, so that any small error voltage on this scale may be neglected completely when compared to the other voltages involved.

One matter which must be taken into consideration is the emitter current source for the transistor under test. For the most precise compensation circuits, this current source should duplicate the source in the actual circuit. The reason for this is that practical current sources are non-ideal and can contribute an appreciable "error" to the measured input current. The simplest current source is a precision resistor returned to a negative supply as shown in Fig. 29a. For this case, the "error" is due to the temperature coefficient of V_{BE} , which is approximately $2 \text{ mV}/^\circ\text{C}$, of the transistor. For $\Delta T = 25^\circ\text{C}$ this effect will cause a change of 50 mV out of approximately 15 volts across the emitter resistor. This is a change of $1/3\%$. In the current source of Fig. 29b, a common base connection is used.

This merely transfers the problem to the V_{BE} temperature coefficient of the current source transistor. Since the drop across the emitter resistor is now only about 5 volts, the "error" becomes 50 mV out of 5 volts or 1%. Figure 29c shows a method for reducing this "error" to a second-order effect. The temperature coefficient of the diodes approximately tracks the temperature coefficient of V_{BE} . This is the circuit which is preferred for accurate compensation. In any case, for precision compensation, the current source which is to be used in the final circuit should also be the one used in the test circuit so that any resulting "error" current will be included in the measurements. The design of the compensating circuit will thus automatically take into account this "error" current and treat it as part of the total input current. It is apparent that the current source should be in the oven with the transistor under test in order that the most meaningful results be obtained. For less accurately compensated circuits this may not be necessary.

Inasmuch as the currents are so small, it is necessary to be especially careful of current leakage paths and pick-up problems. It is usually advisable to use shielded cable with Teflon insulation for all connections. To reduce pick-up problems due to ground currents, each piece of equipment may need to be individually isolated with an isolation transformer. In addition, it may be necessary to provide an electrical shield around the transistor if electrical noise pick-up proves troublesome.

E. OVEN TEMPERATURE STABILITY

Although it might seem to be a trivial problem to maintain a constant elevated temperature with a controlled oven, such is not the case. In practice, a number of problems arise, and must be dealt with according to the degree of severity.

(1) Temperature Control

The first problem is simply constant temperature control. This problem is mainly one of thermal and time response of the sensor and the total effective gain in the control loop. Proportional control is preferred, since it reduces the fluctuations due to an on-off thermostat. Some

manufacturers claim an "electronically controlled" oven, inferring proportional control. Frequently it turns out that the oven is still really an on-off control variety, but with the sensing element in a bridge circuit and with a control amplifier which operates a relay controller. A further degree of control results when the bridge circuit controls the firing angle of a silicon controlled rectifier (SCR). The SCR usually then supplies the oven current directly or through a relay for higher power operation.

The best control results from the use of a high power DC amplifier which delivers dc current to the oven. This is true proportional control, and with adequate loop gain can give very accurate temperature control. Unfortunately, for practical reasons it is limited to applications which require a maximum of a few hundred watts. The larger precise ovens nearly always use SCR controllers.

(2) Temperature Gradient

The second requirement in an oven is the need to maintain a sufficiently small temperature gradient throughout the interior of the oven. This is so that the location of the component being measured is not critical. If only one component is being measured, a thermometer can be placed at that location to monitor the temperature. However, if a number of components are being tested, the problem may become acute. The temperature gradient is caused by two principal effects. First, there is the necessary gradient through the walls of the oven. Since heat flows continually through the walls, it follows that the temperature near the walls is likely to be somewhat different than in the center of the enclosure. At the corners, this effect is even worse. The only cure for this difficulty is to select an oven which has very adequate insulation in the walls and with a guaranteed, suitably small gradient. The second effect is the uneven heating and mixing of the air as it is forced past the heating element. The partial cure for this lies in good engineering design of the air-flow pattern and the baffling associated with the heater-blower system.

(3) Electrical Noise

A third requirement for an oven is low electrical noise. The principal source of noise is that due to arcing at thermostat contacts. A proper R-C network will suppress some of this. In SCR controllers there is still the high frequency pulses at the SCR. The output of the SCR can, however, be filtered, thus reducing this noise to a minimum. DC controllers of course have no inherent noise. Blowers, relays, solenoids valves (for CO₂ low temperature operation), are all potential sources of electrical noise. For most precise measurements, these elements should be carefully considered. Traditionally, oven manufacturers pay scant attention to some of these details since they seem to be peripheral to the temperature stability problem.

(4) Low Temperature Measurements

Low temperature measurements result in a special problem — viz., condensation and frosting due to either leakage of room air into the chamber or the room air which was originally in the chamber. This effect is particularly noticeable during transistor base current measurements, because of the very small currents involved and the close spacing of the leads on the transistor header. Condensation and frosting is quickly indicated when the current measurements become erratic or change continuously. A cure for this effect is to introduce dry nitrogen at low pressure (2 - 3 PSI) into the chamber prior to lowering the temperature of the oven. The nitrogen should be allowed to flow long enough so that any residual moisture is completely removed from the components, oven walls, wiring, and associated equipment. This is best done at an elevated temperature. A separate entrance for the nitrogen should be provided so as not to interfere with the cooling valves. This treatment does not last indefinitely, since a small amount of moisture invariably remains and will eventually find its way into the circulating stream, to be condensed or frozen. For periods of time less than an hour, however, this procedure will permit low temperature measurements with little difficulty. If liquid CO₂ is used to reduce the temperature, it is important that it be manufactured from dry gaseous CO₂.

An additional problem arises in the use of the temperature chamber at low temperature. This is the temperature gradients created by the puffs of cold CO_2 entering each time the solenoid control valve opens. Although the momentary change in temperature is not seen on most thermometers because of their long thermal time constant, the effect is clearly noted with thermistors and transistors which are being monitored with extremely sensitive instrumentation. Reasonably consistent results can be gotten by taking the readings just before the valve opens. Once the period of opening is roughly established, it is easy to estimate the time at which the reading should be taken. An obvious solution to this problem would be to use an electronically controlled, proportional valve. The expansion valve would be roughly preset to give a somewhat larger quantity of cooled CO_2 gas than is needed. The proportional valve would meter this into the chamber in proportion to the demand, the remaining portion being vented to the outside. Thus smooth temperature control could be obtained. An additional luxury would be to have this pre-cooled CO_2 to pass first through an additional compartment where a proportionally controlled heater (perhaps the same one which was used at high temperatures) would bring the temperature of the CO_2 up to precisely the temperature required. This latter technique would prove particularly useful for measurements near room temperature where temperature control is very difficult.

F. PARAMETER STABILITY

(1) Introduction

Close compensation has meaning only to the extent that one can depend on the stability — either short-term or long-term — of the various parameters. The only final way to determine stability is by measuring the various parameters repeatedly over a long period of time. Experience to date has extended over a period of 1 - 2 years with certain circuits. In addition, manufacturers have considerable data on certain parameter stabilities. The following are some of the results of these experiences.

(2) Diode Voltage

As far as diode voltage is concerned, a long term stability of 1 mV or about 0.2 percent has been observed for planar-passivated diodes. Because the temperature coefficient of the diode is lower than that of the other components, the diode stability contributes to the stability of the compensating circuit to a lesser extent.

(3) Thermistor Resistance

Manufacturers of thermistors claim that a glass sealed and stabilized thermistor will have a resistance stability of better than one percent long-term and somewhat better than this figure for short-term stability.

(4) Transistor Base Current

The experience to date has been mainly with high quality, silicon, passivated, planar transistors. A stability of 1 - 2 percent over a period of a few months has been obtained. For the examples previously cited, 2 percent represents 1 nA out of 50 nA. Short-term stability for days or weeks may be as low as 1/2 percent.

(5) Thermal Time Constant

Another factor which must be considered is the thermal time constant of the various components used in the circuit arrangement. The overall effect is to produce a short-term instability, the magnitude of which is determined by the size and physical arrangement of the components, the thermal contact between them and the temperature fluctuations and gradient of the environment. Typical fluctuations are due to a moving stream of air and/or nearby heat dissipating components. Accurately compensated circuits should be shielded from rapidly moving air currents (particularly if the air is apt to be fluctuating rapidly in temperature) and large heat sources. If these precautions are not taken, the resulting accuracy of the compensation may be considerably less than that which the design is capable of giving.

(6) Conclusion

When all of the above factors are considered, it would seem hazardous to guarantee an overall, long-term stability better than 2 percent, even for the most accurately compensated circuit. If, however, R_3 in Fig. 19 is adjusted every few days or weeks, a second-order correction is then applied which may provide a short-term stability of 1/2 to 1 percent for a period of a week or so.

CHAPTER VII

PRACTICAL RESISTOR-THERMISTOR COMPENSATION CIRCUITS

A. DESIGN CONSIDERATIONS

The simple model used for the analysis of resistor-thermistor compensating circuits purposely suppresses some of the problems which arise in building the circuits. In the paragraphs below we point out the more important of these and their implications with regard to design.

1) Scaling Factors and Operating Levels

As indicated previously, thermistors are available in a range of values from $100\ \Omega$ — $10\ \text{M}\Omega$, and therefore many orders of magnitude are possible for component values. The voltage transfer function (Eq. 5.6) of the network is naturally independent of any impedance scaling factor, so the coupling to the external circuitry must dictate the constraints on the operating level.

On the input of the compensating circuit, the characteristics of the voltage source must be considered; on the output of the circuit, the resistor which supplies the compensating current to the input transistor base is important. If the impedance level of the compensating network is roughly the geometric mean between the input and load impedances, then the "cascade-with-isolation" type of analysis used (see V-C) used will adequately model the situation.

Whatever the voltage source, it is necessary that the loading of the circuit does not change its temperature behavior, since this temperature data is incorporated into the analysis. In the case of the forward biased diode source, a change in the diode voltage will alter these characteristics. A reasonable requirement, then, is that the current drawn from the diode by the circuitry be such that the diode voltage is not appreciably changed. For a diode current of $1\ \text{mA}$, the forward voltage is $\approx 600\ \text{mV}$. If the circuit is restricted to draw at most 1% of the diode current, ($10\ \mu\text{A}$), then the circuit impedance seen by the diode must be $\geq 60\ \text{K}\Omega$. At $1\ \text{mA}$, the diode is

theoretically expected to have about 25Ω incremental impedance; in practice, the value may more nearly be 50Ω . A change of $10\mu\text{A}$ in diode current gives a voltage decrease of $\approx 0.5\text{ mV}$, which is less than 0.1% of the diode drop. This is sufficiently small for all practical purposes.

All three resistors (R_1 , R_2 , R_T) in the compensating circuit are essentially of the same value at room temperature, so a choice of a thermistor having a value of $20\text{ K}\Omega$ at 25°C would seem to be about right.

Now consider the effect of the loading resistor R_f . It must not be too small, since it effectively shunts the amplifier input to ground; however, it cannot be too large, or it will fail to supply sufficient current to the input. Assume that the average input transistor has a beta of 200, and a collector current of $10\mu\text{A}$. To allow for a variation in beta with different transistors only a fraction of the total voltage, V_f , should be used for the average case. A design which assumes the potentiometer to be set to give 50% of V_f would seem to represent a conservative design. With the design referred to above, V_f is 400 mV , so that 50% of this value, or 200 mV , is available to drive the resistor R_f for the average transistor. The required value for R_f is therefore

$$R_f \approx \frac{200\text{ mV}}{50\text{ nA}} = 4\text{ M}\Omega$$

As shown in Chapter V, R_1 can be adjusted to compensate for the inclusion of R_3 in the circuit.

The $4\text{ M}\Omega$ shunting impedance at the amplifier input is not too severe in many cases. One is nevertheless tempted to avoid the problem by raising the overall impedance level of the compensating circuit, thus permitting a larger R_f to be used. This may be accomplished by using several diodes in series or a zener diode as a voltage source. For the case of the zener diode, the voltage, V_f , may become ten or twenty times the voltage given above, and R_f may be as high as $100\text{ M}\Omega$. The zener diode is stable and has good temperature behavior, but will introduce one new problem. The power level in the transistor may be increased to such an extent that the circuit may have an error resulting from self heating of the

transistor. The resulting non-linear behavior may be at wide variance with that desired. The self-heat problem is discussed below in some detail.

2) Self-Heating

Self-heating in a thermistor manifests itself as a temperature differential between the device and the ambient temperature. In order to limit self-heating, the maximum allowable rise in temperature of the thermistor above ambient temperature must be specified. Since thermistor measurements need to have an accuracy of only 0.5%, there is no reason to require that the resistance change due to self-heat be much smaller. Since the resistance varies at about 5% /°C, a deviation from ambient of 0.1°C is certainly tolerable.

Published data for a thermistor which may be considered as typical of those considered for this application, indicate that a dissipation of 700 microwatts should raise the thermistor 1°C above ambient near 25°C. A value of 70 μW should therefore produce about 0.1°C offset. The resulting thermistor current limit (for the 20 KΩ thermistor) is

$$I < \sqrt{\frac{P}{R}} = \sqrt{\frac{70 \times 10^{-6}}{20 \times 10^{-3}}} \approx 60 \mu A \quad (7.2)$$

Because of the resistance change due to temperature variations, the threshold may be lower than this. For the parameters chosen, a 10 μA current appears to be a very conservative value.

The self-heating problem with a zener diode source is best illustrated by example. Suppose a 12 volt zener replaced the silicon diode as a source; the impedance level of the circuit would be raised by a factor of 20, as would the power dissipated in the thermistor. For many thermistors, the power required to raise the thermistor temperature 0.1°C above ambient is fairly insensitive to the 25°C resistance. Using the pertinent numbers from the above example, the thermistor would be about 400 KΩ, and would dissipate 40 μW at 10 μA current. This dissipation is much closer to the self-heat threshold of 70 μW specified above. At temperatures other than 25°C a noticeable gradient might appear.

It should be noted that if the impedance level had remained the same as before, the power dissipated in the thermistor would have increased as the square of the diode voltage. However, by raising the impedance level proportionally as the voltage is increased, the power dissipated in the thermistor will increase directly with the diode voltage. This provides some flexibility in choosing the impedance level, but eventually the self-heating of the thermistor will enter as a limiting condition.

3) Temperature Range

The choice of temperature range over which compensation is to be effective is sometimes dictated quite specifically by the operating conditions of the particular application. More often, however, only a rough idea of the range is given in advance, and the designer is free to adjust some of the temperature parameters of his solution. The reader should recall that the significance of the temperature points T_u , T_o , and T_l in the solution, is that of pin-pointing zero crossings of the error current curve. In the regions (T_l, T_o) and (T_o, T_u) the current is finite and has a maximum magnitude which increases monotonically, but nonlinearly, with the intervals $\Delta T_+ = T_u - T_o$ and $\Delta T_- = T_o - T_l$. Experimental data indicate that the slope of the maximum error current increases with ΔT , and for this reason it is often wise to restrict ΔT_+ and ΔT_- to be as small as possible to cover the desired range. There is, as could be expected, a trade-off involved here. As the width of the temperature range is decreased, the slope of the error current immediately outside the extremes of the range is increased in magnitude. This is important because errors due to component tolerance and misadjustment may cause the currents near the end points to exceed the desired limit. The relative importance of these two effects must be considered for precision design cases.

For many applications, the criterion which sets the values of ΔT_+ and ΔT_- is the maximum allowable magnitude of the error current. The maxima occur at temperatures $T_o + 1/2 \Delta T_+$ and $T_o - 1/2 \Delta T_-$, approximately. If we have symmetric compensation ($\Delta T_+ = \Delta T_-$), then the two maxima are approximately equal, but opposite in sign. No analytic result for the values

of these maxima has been obtained but data presented in the following section indicate that approximately $|I_{\max}| (\Delta T)^3$. For asymmetric design ($\Delta T_+ \neq \Delta T_-$), the greater of (ΔT_+ , ΔT_-) provides the limiting factor. Mild asymmetry does not seem to affect component values significantly. Outside the range specified by ΔT_+ and ΔT_- , there is a few degrees leeway before the error current approaches the maximum value in the opposite sense. This leeway is usually about 5°C at each end of the range and thus provides some freedom in the choice of the end points.

4) Parameter Variations

It is important to know how the parameters of transistors, thermistors and diodes vary over a given assortment. This knowledge will assist in giving estimates of our confidence in the compensation. The parameters of interest for the transistors and diodes are the values of ℓ and u . For the thermistors, the parameters of concern is the temperature coefficient, α , and the 25°C resistance.

The base currents of 30 Amelco SA2320 transistors were measured at the symmetrical temperature points of 10, 30, and 50°C , with $I_C = 10 \mu\text{A}$, and the parameters ℓ and u were computed according to Eq. 5.9a, b (assuming the diode ratio to be unity). Figure 30 shows a scatter plot of the data. The resulting locus can be fit to a straight line, but it is perhaps more illuminating to observe that the curve $\ell u = 1.00$ provides an excellent fit for this symmetrical case. Certainly this is reasonable from the definitions of ℓ and u (see Chapter V). If such a relationship were found to hold for various temperature ranges, temperature increments and transistor types, then the average parameter locus for a given transistor batch could be specified by this one number. Unfortunately, there do not exist non-trivial solutions (R_p , R_2) to Eqs. 6.14a, b which are constant along a given $\ell u = K$ locus, so that in theory every transistor of a batch will require a unique compensation circuit, even if it does conform to the $\ell u = K$ curve.

The spread of values in u is .82 to .88, with a corresponding range of 1.14 to 1.23 in ℓ . This can also be expressed as a spread in the transistor temperature coefficient, γ , of .0065 to .0104 (0.65 to $1.04\%/^\circ\text{C}$), about a

1.6:1 spread. The ℓu product ranges from .980 to 1.015, giving evidence that the exponential model for base current is quite valid. It should be quite apparent that temperature coefficients vary sufficiently from unit to unit, that only limited compensation can be expected from an "average" compensating circuit designed to be used with any transistor of the group. For best results, individual compensation must be used. A good comparison of these two techniques will be found in Section B of this Chapter.

The parameters ℓ and u for silicon diodes have also been computed. The diode parameters turn out to be far more stationary than the transistor ones, and will therefore contribute little to the error in the average compensation case. For a sample of FD171 diodes, the values of ℓ and u varied only about $\pm 1\%$ around their average values, which were $\ell_{av} \approx 1.07$, $u_{av} \approx .93$. The ℓu product remains equal to 1.00 for all practical purposes. This data was taken as before, with symmetrical temperatures of 10° , 30° and 50°C .

Ordinary thermistors are available with tolerances for the 25°C resistance, ranging from 20% down to 1%, with 5% being typical for the thermistors considered here. A class of "Iso-curve"* thermistors is also available; these have R-T characteristics guaranteed to be within $\pm 0.1^\circ\text{C}$ of standard curves. For most applications, standard thermistors are suitable in both the individual design and the average design compensating circuits. However, when exceptionally accurate and predictable compensation is desired, the "Iso-curve" thermistors should be considered.

B. PRACTICAL CIRCUITS

1. Individual vs. Average Compensation

Individual compensation requires that each variable component (transistor, thermistor and diode) which is part of the compensation circuit be individually measured at the required three temperatures. The resistor values are then computed as described in Section V. Each circuit is thus tailored to the exact measured values of the components involved. This approach certainly will give the most precise compensation. Experience indicates that up to 99% of the input current may be reliably compensated in

* Manufactured by Fenwal Electronics, Inc.

this way. For the example previously cited this would result in 0.5 nA of resulting input current. Although it might seem that this is a rather complicated procedure, it is worth the trouble where a very low input current is required. Furthermore, it is a simple matter to make these measurements on an "assembly line" basis. The relevant data are punched on cards and a simple computer program then yields the required resistor values. This method has actually been used in design of a large number of operational amplifiers. A computer program is given in Appendix II.

Average compensation results when the compensation circuit is designed using the average parameter values for the components — transistor, thermistor and diode. Only one circuit is thus designed. The resulting compensation is, of course, dependent on the variations in the parameters of the components. Experience indicates that with $\pm 5\%$ thermistors, ± 50 mV diodes and quality transistors having a maximum beta spread of 2:1, up to 90% of the input current may be compensated over a 50°C range in temperature. In the example cited, this would represent 5 nA of input current. Of course, the success in compensation is really dependent on the temperature coefficient of these parameters rather than their absolute value. It would seem reasonable, however, that close component tolerance would tend to be correlated with close tolerance for the temperature coefficient too. Data which has been accumulated to date seems to verify this fact sufficiently to make this selection process reasonable.

In summary, individual compensation is called for whenever the very lowest value of input current is required and where the additional required measurements can be justified. For somewhat less critical requirements, average compensation will provide fairly low input current. It is only necessary to have average values for the parameters involved. It should be noted that in a system design where both types of compensation circuits are needed, the average values are easily obtained once the measurements have been made for the individually compensated circuits.

2) Symmetric vs. Asymmetric Design

The temperature span will determine the maximum expected input current over this range. The temperatures may be evenly or unevenly spaced. Symmetric design means that $T_u - T_o = T_o - T_l$. Asymmetric design means that $T_u - T_o \neq T_o - T_l$.

Ordinarily, circuit adjustments are made at room temperature. It is hence useful to make T_o equal to the room temperature so that adjustment of R_3 can be made at the center cross over point where the current should theoretically be zero. Actually a small difference in room temperature from T_o will not affect the final performance by a great deal.

If only operation above room temperature is expected, T_l may be set equal to the room temperature and T_o and T_u chosen to be some elevated temperatures. Similarly if the operating temperature is always below room temperature, T_u may be set equal to room temperature and T_o and T_l chosen to be some low temperatures.

The choice of T_l and T_u is dictated by the anticipated range in operating temperature. As mentioned before, the designated compensation will hold for about 5°C beyond these extreme cross over points for reasonable temperatures. If the expected rise in operation temperature exceeds the expected drop in temperature or vice-versa, an asymmetric design may be indicated. There is, however, little advantage, in asymmetric design having only 10 - 20% asymmetry.

For many applications the choice of symmetrical temperatures of 0°, 25° and 50°C for T_l , T_o and T_u is convenient. In the practical examples to be given below, the range has purposely been kept above 0°C to avoid the problems associated with condensation and frosting as described in Section VI. These examples were selected to demonstrate the effects of temperature span, asymmetry, and average compensation.

3) Individual-Symmetric Example

Figure 3 is the schematic of an individual-symmetric compensation circuit for a SA-2320 transistor. The critical temperatures were 20° - 40° - 60°C. The table of parameter values and the results of the computation are

given below. The very large number of decimal places for l and u are used in the computation only because of the way in which they enter into Equations 5. 14 a and b and not because of any inherent extreme accuracy requirements.

TABLE I

$T(^{\circ}\text{C})$	$V_d(\text{mV})$	$I_B(\text{nA})$	$R_t(\Omega)$
20	722.0	53.92	7300
40	687.6	44.87	3346
60	652.6	37.25	1700

$$l = \frac{I_l}{I_o} \left(\frac{V_d(T_o)}{V_d(T_l)} \right) = 1.14443856$$

$$u = \frac{I_u}{I_o} \left(\frac{V_d(T_o)}{V_d(T_u)} \right) = 0.87469975$$

$$R_2 = 1543.51370 \approx 1544 \Omega$$

$$R_p = 1923.04293 \approx 1923 \Omega$$

$$R_1 = \frac{R_3 R_p}{R_3 - R_p} = 1960.7489 \approx 1961 \Omega$$

(No correction has been made for Z_d)

The resultant input current for this circuit is plotted in Fig. 32. A maximum current of ± 0.1 nA over 45°C in temperature is shown. Of course, it cannot be expected that such extreme compensation would be stable over long periods of time. In accordance with the remarks concerning parameter stability, (Section VI, F), one might more conservatively expect a total variation of ± 0.5 nA. short term, and ± 1.0 nA long term.

It is important to know what happens to the maximum error current and the shape of the error curve when the temperature span is changed. The pertinent data are given in the tables below:

TABLE II
Measured Data

$T(^{\circ}\text{C})$	$V_d(\text{mV})$	$I_B(\text{nA})$	$R_t(\Omega)$
0	755.8	65.57	17,265
10	739.7	60.24	11,265
20	722.0	55.14	7,240
30	704.4	50.27	4,853
40	687.1	45.89	3,333
50	668.6	41.69	2,300
60	650.4	37.84	1,621
70	633.6	34.23	1,203
80	615.4	30.66	884

TABLE III
Table of ℓ Values

$T_{\ell} (^{\circ}\text{C})$	ℓ
0	1.30857232
10	1.22836881
20	1.14348759
30	1.06854158

$$T_o = 40^{\circ}\text{C}$$

TABLE IV
Table of u Values

$T_u (^{\circ}\text{C})$	u
50	0.93361412
60	0.87110897
70	0.81487532
80	0.75147423

$$T_o = 40^{\circ}\text{C}$$

TABLE V
Table of R Values

Experiment Number	$T_l - T_o - T_u$	$R_1(\Omega)$	$R_2(\Omega)$
1	30 - 40 - 50	1999	1745
2	20 - 40 - 60	2071	1701
3	10 - 40 - 70	2234	1663
4	0 - 40 - 80	2301	1483

(No correction has been made for Z_d)

The circuit which is used is identical to Fig. 31 except for the different values for R_1 and R_2 . The results of these variations in temperature span are shown in Fig. 33. It is seen that as the span becomes greater, the maximum error increases as would be expected. Table VI indicates these results.

TABLE VI
Table of $I_{\max}$ vs. ΔT

$\Delta T(^{\circ}\text{C})$	$ I_{\max}(+) $ (pA)	$ I_{\max}(-) $ (pA)	$I_{\max \text{ ave.}}$ (pA)
10	20	0	10
20	150	80	115
30	600	460	530
40	1200	1000	1100

$$\Delta T = (T_u - T_l)/2 \text{ }^{\circ}\text{C}$$

$$I_{\max \text{ ave.}} = 1/2 \left[|I_{\max}(+)| + |I_{\max}(-)| \right] \text{ pA.}$$

Note that the value of $|I_{\max}(+)|$ is always greater than $|I_{\max}(-)|$. The reason for this dissymmetry is not understood. Since these results are based on only one experiment, further speculation is unwarranted.

A plot of the average maximum error current vs. temperature span is shown in Fig. 34. Because of the complexity of the design equations, no analytical expression has yet been derived for the maximum error current. The specific data contained in Table VI can however be used to derive an empirical relationship. A fourth degree polynomial can obviously be made to fit the four values for $I_{\max \text{ ave.}}$, in the table. The resulting equation however obscures the principal behavior of the function due to the presence of large terms of opposite sign. A less accurate, but more revealing, fit is obtained by the simple equation

$$I_{\max \text{ ave.}} = \frac{1}{40} (\Delta T)^{2.9}, \text{ pA.} \quad (7.1)$$

where $\Delta T = (T_u - T_l)/2$ °C. Considered on a point-to-point basis, this error current will vary approximately as the cube of the temperature span, ΔT . This information permits a quick estimate of the maximum temperature span, ΔT , which is possible for a given maximum error current. It may be remembered that ΔT will be augmented by about 5°C at each end of the temperature span. See VII-A-3. Also, the error current which is used in the above relationships is the short-term "laboratory value". This provides an insight into the design problem and hence is useful in the initial circuit design. However a safety factor of 2 or 3 should be used to predict the long-term behavior, of the error current, in practical circuits.

Since these remarks apply specifically to the particular circuit design given, some variance might be expected for cases where the components and operating levels are markedly different from the example cited. Further generalizations are not warranted from the limited experimental data. However, an analytical expression derived from the original design equations, would be completely general in application.

4) Individual - Asymmetric Example

Using the data in Table II, III and IV above, the component values may be calculated for two separate asymmetric cases where the ratio of temperature spans is 3:1. The results are given below.

TABLE VII
Table of R Values

Experiment Number	$T_l - T_o - T_u$	$R_1(\Omega)$	$R_2(\Omega)$
5	10 - 40 - 50	2771	2374
6	30 - 40 - 70	1704	1299

(No correction has been made for R_d)

Figure 35 shows the resulting input current variations over a wide temperature range. As might be expected, the maximum error occurs at approximately midway of the largest temperature span regardless of whether this is above or below the middle crossover temperature T_o . These results are shown in Table VIII.

TABLE VIII
Table of $I_{\max}$ vs. ΔT

Experiment Number	ΔT	$ I_{\max}(+) $ (pA)	$ I_{\max}(-) $ (pA)
5	10	—	100
6	10	70	—
5	30	350	—
6	30	—	350

Because only one set of experiments has been conducted, no conclusions can be reached concerning the comparison of values in Tables VI and VIII. The main purpose was to demonstrate the approximate behavior of these compensating networks which have been designed in accordance with the analysis previously given.

5) Average - Symmetric Example

A network designed to match the average values for the transistor, thermistor and diode is of considerable interest since this approach is very practical for a majority of uses. The relevant data for the average - symmetric case (20 - 40 - 60 °C) is given below in Table IX

TABLE IX

T(°C)	V _d (mV)	I _B (nA)	R _t (Ω)
20	722.0	51.79	7300
40	687.6	43.53	3346
60	652.6	36.30	1700

$$l = 1.13306784$$

$$u = 0.87863147$$

$$R_1 = 1634 \Omega \quad (\text{No correction has been made for } R_d)$$

$$R_2 = 1368 \Omega$$

In this example, fixed values are used for the diode and thermistor, while the average value of I_B for a group of twenty seven SA 2320 transistors is used. Since I_B is a less well controlled parameter, it might be expected that one should be able to predict reasonably well, the performance of a "true" average circuit based on the results obtained even with the above restrictions.

All 27 transistors were tried with this "average" circuit and the resultant input current plotted for each case. The result was a scattered family of curves; fifteen curves, or nearly half, fell within ± 1 nA over the designed temperature range. The remaining transistors fell within the limits of ± 2.5 nA. Because of the variability of $\frac{dI_B}{dT}$ for the transistors, the curves had a variety of shapes. Figure 36 shows the range of variability for these curves. In some cases the expected "S" does not seem to occur. However, if the range of measurements is sufficiently extended, the "S" shape will reveal itself. The non-optimum design results in the shape being obscured within the designed temperature range. Note that the maxima are considerably greater than for the individual design case and the cross over points may occur remotely from the design temperatures.

The principle conclusion one can draw from this example is that although the shape of the $I_{\max}$ curve may not be the ideal "S" shape, the maximum input current is still below 6% of the original average base current. It may be concluded that 10% is a conservative figure for average compensation, assuming a reasonable control on the relevant parameters.

C. SHARED CIRCUITS

If the compensation requirements are only nominal, it is sometimes possible to effect an economy in components and hence space and cost by sharing a single, centrally located compensation circuit, with several amplifiers. This of course assumes that the thermal environment is reasonably uniform, such as might be the case for a single printed circuit board containing a number of operational amplifiers. Either a number of paralleled R_3 potentiometers may be used or the potentiometer, R_3 , may be entirely eliminated, with each R_f being chosen to match the input current for the amplifier to which it is connected. Although some of the versatility and accuracy of the separate circuits will be lost, the compromise may be worth while for certain applications.

Another possible variation exists whenever a number of amplifiers are to be used in the normal or resistive feedback sense (not the voltage

follower connection) a single voltage source for a number of compensation circuits may be derived by one of two methods. 1) A diode may be operated at a suitable current level so that it can drive a number of compensation circuits simultaneously. This requires that, as above, the diode be located centrally so as to share the average thermal environment. 2) A temperature compensated zener diode and/or a resistive divider driven from a stable voltage can be connected to a voltage regulator circuit or a feedback operational amplifier, to yield a very low impedance, temperature-stable voltage source. With this arrangement, the terms $\frac{V_d(T_o)}{V_d(T_\ell)}$ and $\frac{V_d(T_o)}{V_d(T_u)}$ of the design equations are equal to unity. The design equations will then contain only the thermistor resistances and the base currents at T_ℓ , T_o , T_u .

D. VOLTAGE FOLLOWER APPLICATION

The voltage follower application has already been mentioned in Section IV-H-4. It was shown that since the voltage on the base of the transistor varies directly with the signal voltage, it is necessary to reference the compensation current to the signal. This is done by "floating" the compensation circuit on the amplifier output voltage, which follows quite accurately the input signal; see Fig. 21.

In addition, the emitter current and hence the input base current will change as a result of the input signal unless there is a perfect constant current source in the emitter circuit. Figure 37(a) shows an idealized circuit using a transistor with a beta of 200 and a collector current of 10 μA . A large resistor, returned to -15 volts provides the emitter current source. Assuming perfect compensation at zero signal; at an input signal level of +5 volts, Fig. 37(b), the emitter current increases to $10(19.5/14.5) = 13.5 \mu\text{A}$. The base current now becomes 67.5 nA, only 50 nA of which, is supplied by the compensation circuit. The remaining amount of 17.5 nA is an "error" current which must be supplied by the signal source.

By returning the emitter resistor to a larger negative voltage, say 100 volts, this emitter current change can be reduced; see Fig. 38. For this case the emitter current with +5 V input becomes $10(104.5/99.5) = 10.5 \mu\text{A}$.

This is now an increase of only $0.5 \mu\text{A}$. Hence, the resulting error current becomes only $500/200 = 2.5 \text{ nA}$. Such a solution to the problem is, however, unattractive because of the large voltage required.

Equivalent results may be obtained by using a grounded-base transistor as a current source. See Fig. 39(a). The output conductance, h_{oe} , of most silicon small-signal transistors is specified as $1 \mu\text{v}$ max. However, actual measurements indicate that a value of $0.1 \mu\text{v}$ is not an unreasonable value. In such a case, this value represents an output resistance of 10 megohms. For a current of $10 \mu\text{A}$, this is equivalent to a source voltage of 100 volts. Hence, results identical to the former example will be obtained — namely, an error current of 2.5 nA . The principal restriction is that the base voltage, V , of the current source transistor, be at such a level, that with the most negative signal voltage, the collector-base junction remains reverse biased by at least 2 volts.

An even greater improvement may be obtained by common-mode negative feedback.¹² With this arrangements whenever the signal conditions are such as to increase the net emitter current a common-mode signal is generated. A negative dc signal derived from the common-mode signal is applied to the base of the current source transistor so as to decrease the emitter current. The result of using this technique is to increase the equivalent resistance to as high as 100 to 1000 megohms. This effectively eliminates the current source as a contributor to the input current change with signal level.

The particular method of obtaining the common-mode signal depends on the circuit arrangement. One method is shown in Fig. 40. A detailed discussion of this technique is given in Reference 12.

There remains one final source of difficulty. Figure 41 shows the circuit connection for the compensation circuit which has been previously discussed in detail. Inasmuch as this circuit is referenced to the output signal of the amplifier, the current through the diode will change with the signal level. This changing current results in a change in the diode voltage and hence in a variational driving voltage for the rest of the network. The

extent of this effect may be seen by considering a signal swing from +5 to -5 V. This results in a diode current of 0.67 mA and 1.34 mA respectively, the zero signal case being approximately 1 mA. The dynamic resistance of an average signal diode is about 50 ohms. The change in diode voltage is thus about ± 17 mV. Since the nominal diode voltage at 1 mA is about 600 mV, the change in compensation current, assuming as before a nominal value of 50 nA, will be:

$$\Delta I = \frac{\pm 17}{600} \times 50 = \pm 1.4 \text{ nA.}$$

Using a common base connected transistor, a relatively constant current can be supplied to the diode, resulting in an improvement of about ten times. The variational input current then becomes about 0.15 nA.

It should be pointed out that in the use of the voltage follower in a sample and hold application as described in II-B, one normally requires the extremely low input current only at low signal levels. As the signal increases, a larger amount of input current may be tolerated, because one is usually concerned with a percentage variation in the "held voltage". In the integrator case (II-B), however, a very small current may be integrated over a long period of time to give a final large signal voltage. In such a case, it is necessary to examine the input current requirements more carefully.

One specialized example will be given of a compensation circuit which has been used in the voltage follower application. Figure 42 shows this circuit.

This amplifier has the compensation circuit directly in its output. The principal disadvantage of this approach is that the voltage drop across the diode is now a function of the total output current of the amplifier. This output current includes the current which goes through the 7.5 K emitter resistor. Since both of these currents are a function of the signal level, there would seem to be no particular advantage to this circuit. It is given here simply to show a variation in circuit possibilities for voltage follower applications.

One final problem must be considered in the voltage follower application. Since the compensating circuit is connected to the output of the amplifier, the entire current flowing through the compensating circuit must be "absorbed" by the amplifier. This requirement determines the minimum current rating for the amplifier — the proper current sense being noted. It is important to keep this condition in mind when deciding on the impedance level of the circuit. See VII A 1. In most designs, the current through the diode represents nearly the entire current requirement. It is necessary that the amplifier be capable of supplying this current under conditions of maximum signal in either sense. Depending on whether a forward biased diode or a zener diode is used, and on the impedance of the network, the current requirements could range from 1 — 5 mA. For most practical circuits a figure of 1 — 2 mA has proven to be quite adequate.

E. CONCLUSIONS

In conclusion it can be said that practical input current compensation circuits can be designed to give a variety of results. The resulting input current may range from 1% to 20% of the original input current, depending on the degree of sophistication of the circuit employed. Although the examples have been based on one kind of transistor, the conclusions should also be valid for similar high quality transistors.

ACKNOWLEDGEMENT

The authors express appreciation to Arthur Olson and John Drobot who so patiently made the many careful measurements required in the course of this investigation.

APPENDIX I

Mathatron (Model 513) Program for calculating R_1'' and R_2 in a Resistor-Termistor Temperature Compensating Circuit.

Parameters to be used

T_ℓ Lower temperature

T_o Middle temperature

T_u Upper temperature

R_ℓ Resistance of thermistor at T_ℓ (high resistance)

R_o Resistance of thermistor at T_o (medium resistance)

R_u Resistance of thermistor at T_u (low resistance)

I_ℓ Base current at T_e

I_o Base current at T_o

I_u Base current at T_u

V_ℓ Diode voltage at T_e

V_o Diode voltage at T_u

V_u Diode voltage at T_u

R_3 Divider resistance

R_d Dynamic resistance of diode

APPENDIX I (CONTINUED)

Clear all Registers

Learn Mode:

$$S1 \times S4 - S2 \times S5(S6 - S3 \times S4 \times S5) \div (S1 \times S5 - S2 \times S4 - S3 \times S6) =$$

Normal Mode:

$$R_u \text{ } \text{f} \text{ } 4 \text{ (Low resistance)}$$

$$R_o \text{ } \text{f} \text{ } 5 \text{ (Medium resistance)}$$

$$R_\ell \text{ } \text{f} \text{ } 6 \text{ (High resistance)}$$

Compute:

$$l = \frac{I_\ell}{I_o} \frac{V_o}{V_\ell} \text{ } \text{f} \text{ } 7$$

$M \text{ } \text{f} \text{ } N$ means to store the number M
in Register N

$$u = \frac{I_u}{I_o} \frac{V_o}{V_u} \text{ } \text{f} \text{ } 8$$

$$S7 - S8 \text{ } \text{f} \text{ } 1$$

$$S7 - 1)S8 \text{ } \text{f} \text{ } 2$$

$$1 - S8)S7 \text{ } \text{f} \text{ } 3$$

Press AUTO KEY, Machine prints out R_2

$$R_2 \text{ } \text{f} \text{ } 2$$

$$S7 - 1)(S2 + S5)(S2 + S6) \div (S2 + S6 - S2 \times S7 - S5 \times S7) \text{ } \text{f} \text{ } 1$$

$$S1 = R_p$$

Compute (correction for divider resistance R_3)

$$R_1 = R_p R_3 \div (R_3 - R_p)$$

APPENDIX I (CONTINUED)

Compute (correction for R_d)

$$R_1'' = R_1 - R_d$$

To Check

$$S1 \div (S2 + S5) + 1)(S2 + S6) \div (S1 + S2 + S6) = \underline{\hspace{2cm}} \quad S7 = \underline{\hspace{2cm}}$$

$$S1 \div (S2 + S5) + 1)(S2 + S4) \div (S1 + S2 + S4) = \underline{\hspace{2cm}} \quad S8 = \underline{\hspace{2cm}}$$

These corresponding pairs of numbers should agree to within a few digits in the last place.

APPENDIX II

IBM 7094 Program (Fortran) for Computing the Values of R_1'' and R_2

The IBM 7094 program is arranged to carry out the identical computational steps shown in the Mathatron program, Appendix I. The data is read in on punched cards with the format shown below. The print out includes the input data and problem statement as well as the calculated resistance values.

The notation used in this program corresponds to that used in the text as shown below.

Text	Program
R_1	R1PRM
R_2	R2
R_3	R3
R_p	R1
Z_d	RD
R_1''	R12PRM

APPENDIX II (CONTINUED)

Data Card, 72 Entries

(1 Card Per Circuit)

Punch Position No.		
1	}	Problem Number, 3 digits
2		
3		
4	}	Dynamic Resistance of diode, R_d , (Ω), 3 digits
5		
6		
7	←	Sign, $\pm$, of lower temperature
8	}	Lower temperature ($^{\circ}\text{C}$), T_l , 2 digits
9		
10	}	Middle temperature ($^{\circ}\text{C}$), T_o , 2 digits Assumed to be (+)
11		
12	}	Upper temperature ($^{\circ}\text{C}$), T_u , 3 digits Assumed to be (+)
13		
14		
15	}	Base current, I_l , in nA, 3 digits, plus 2 decimals
16		
17		
18		
19	←	Decimal Place
20	}	Base current, I_o , in nA, 3 digits, plus 2 decimals Decimal Place
21		
22		
23		
24		

APPENDIX II (CONTINUED)

Punch Position No.	
25	Base current, I_u , in nA, 3 digits, plus 2 decimals Decimal Place
26	
27	
28	
29	
30	Diode Voltage, V_ℓ , in mV, 4 digits, plus 1 decimal Decimal Place
31	
32	
33	
34	
35	Diode Voltage, v_o , in mV., 4 digits, plus 1 decimal Decimal Place
36	
37	
38	
39	
40	Diode Voltage, V_u , in mV., 4 digits, plus 1 decimal Decimal Place
41	
42	
43	
44	
45	Thermistor Resistance, R_ℓ is Ω , 6 digits, plus 1 decimal Decimal Place
46	
47	
48	
49	
50	
51	

APPENDIX II (CONTINUED)

Punch Position No.	
52	{ Thermistor Resistance, R_o, in Ω, 6 digits, plus 1 decimal
53	
54	
55	
56	
57	
58	← Decimal Place
59	{ Thermistor Resistance, R_u, in Ω, 6 digits, plus 1 decimal
60	
61	
62	
63	
64	
65	← Decimal Place
66	{ Divider Resistance, R_3, in Ω, 7 digits
67	
68	
69	
70	
71	
72	

```

*      DATE 09/28/64
*      WHITE,S. , HARRIS PROBLEM
*      XEQ
*      LIST8
31 K=3
      WRITE OUTPUT TAPE 3,32
32 FORMAT(1H1)
10 READ INPUT TAPE 2,1,IRN,RD,TL,TO,TU,XIL,XIO,XIU,VL,VO,VU,RL,RO,RU,
      1R3
1  FORMAT(I3,F3.0,I3,I2,I3,F5.2,F5.2,F5.2,F5.1,F5.1,F5.1,F7.1,F7.1,F7
      1.1,F7.0)
      XL=(XIL/XIO)*(VO/VL)
      U=(XIU/XIO)*(VO/VU)
      XLU=XL*U
      ALPHA=XL*(1.-U)
      BETA=U*(XL-1.)
      GAMMA=(XL-U)
      R2=((RO*RU*ALPHA)+(RO*RL*BETA)-(RU*RL*GAMMA))/((RL*ALPHA)+(RU*BETA
      1)-(RO*GAMMA))
      SIGMA=(R2+RO)
      TAU=(R2+RL)
      R1=((SIGMA*TAU)*(XL-1.))/(TAU-(XL*SIGMA))
      R1PRM=(R3*R1)/(R3-R1)
      R12PRM = R1PRM-RD
      WRITE OUTPUT TAPE 3,20
20 FORMAT(1H0)
      WRITE OUTPUT TAPE 3,21,IRN
21 FORMAT(1H0,28H
      PROBLEM 13)
      WRITE OUTPUT TAPE 3,2
2  FORMAT(1H0,51H      TL =      IL =      VL =      RL =)

```

Appendix II Listing of Fortran Program (IBM 7094)

```

WRITE OUTPUT TAPE 3,3,TL,XIL,VL,RL
3 FORMAT(1H+,9XI4,9XF5.2,11XF5.1,11XF6.0)
WRITE OUTPUT TAPE 3,4
4 FORMAT(1H0,83H      TO =          IO =          VO =          RO =
1          R3 =          RD = )
WRITE OUTPUT TAPE 3,103,TO,XIO,VO,RO,R3,RD
103 FORMAT(1H+,9XI4,9XF5.2,11XF5.1,11XF6.0, 6X,F8.0,11X,F3.0)
WRITE OUTPUT TAPE 3,5
5 FORMAT(1H0,51H      TU =          IU =          VU =          RU =)
WRITE OUTPUT TAPE 3,3,TU,XIU,VU,RU
WRITE OUTPUT TAPE 3,8
8 FORMAT(1H0,44H      L =          U =          LU =)
WRITE OUTPUT TAPE 3,9,XL,U,XLU
9 FORMAT(1H+,11XF10.7,7XF10.7,8XF10.7)
WRITE OUTPUT TAPE 3,6
6 FORMAT(1H0,122H      R1 =          R1/ =
1          R1// =
2R2 = )
WRITE OUTPUT TAPE 3,7,R1,R1PRM,R12PRM,R2
7 FORMAT(1H+,6XF15.4,10XF15.4,45X,F15.4,10XF15.4)
K=K-1
IF(K)30,31,30
30 GO TO 10
END
* DATA

```

Appendix II Listing of Fortran Program (IBM 7094) Continued

NO.	R_d	T_2	T_o	T_u	I_2	I_o	I_u	V_2	V_o	V_u	R_2	R_o	R_u	R_3
1	50+0025060	5656	4463	3340	6724	6224	5520	305700	102730	28250	107910			
2	50+0025060	6840	5499	4085	6702	6204	5507	308100	104720	29240	094505			
3	50+0025060	6212	4908	3592	6867	6372	5662	295000	099180	27340	095564			
4	50+0025060	6850	5274	3668	6642	6127	5417	283000	096280	26920	093242			
5	50+0025060	5221	4394	3437	6697	6184	5468	299700	102290	28750	097859			
6	50+0025060	5903	4797	3524	6695	6186	5480	293400	099920	28000	098559			
7	50+0025060	5587	4457	3322	6767	6254	5517	293000	099850	28010	103080			
8	50+0025060	5429	4416	3260	6727	6220	5502	284950	097150	27250	100610			
9	50+0025060	5889	4830	3665	6746	6241	5528	300000	102110	28600	097054			
10	50+0025060	5769	4639	3396	6668	6171	5488	298500	101100	28160	094882			
11	50+0025060	6450	5200	3887	6601	6089	5378	315200	104840	28450	092205			
12	50+0025060	6419	5037	3356	6833	6337	5630	288200	098330	27630	096559			
13	50+0025060	5151	4147	3132	6595	6084	5372	303300	100800	27360	091503			
14	50+0025060	6285	5051	3753	6793	6277	5533	292900	099430	27710	103750			
15	50+0025060	6410	5230	3986	6693	6184	5484	299900	102260	28730	098758			
16	50+0025060	5584	4559	3496	6643	6134	5428	306800	104680	29430	095396			
17	50+0025060	6345	5161	3760	6614	6100	5383	292200	099100	27600	095772			
18	50+0025060	6025	4839	3437	6640	6138	5451	303200	101900	28090	092953			
19	50+0025060	6445	5153	3834	6852	6357	5649	285200	095400	26110	096652			
20	50+0025060	6501	5044	3471	6854	6358	5653	286100	095960	26330	098928			
21	50+0025060	5184	4348	3424	6610	6104	5404	296200	100050	27760	098896			
22	50+0025060	7618	5914	4076	6851	6340	5608	292000	098860	27490	104360			
23	50+0025060	5433	4644	3606	6724	6204	5491	299500	102140	28680	097103			
24	50+0025060	5951	4730	3456	6615	6102	5414	309900	103790	28380	104940			
25	50+0025060	6062	5162	3997	6868	6334	5555	308100	104690	29240	096100			
26	50+0025060	6162	5364	3919	6724	6203	5497	284700	097370	27410	101900			
27	50+0025060	6112	5014	3796	6870	6357	5627	292900	100300	28270	099872			
28	50+0025060	6183	5006	3685	6577	6064	5370	286200	097950	27630	093564			
29	50+0025060	5930	4869	3526	6860	6334	5597	291300	098900	27630	107180			
30	50+0025060	5921	4825	3566	6827	6287	5523	286200	098290	27760	098284			

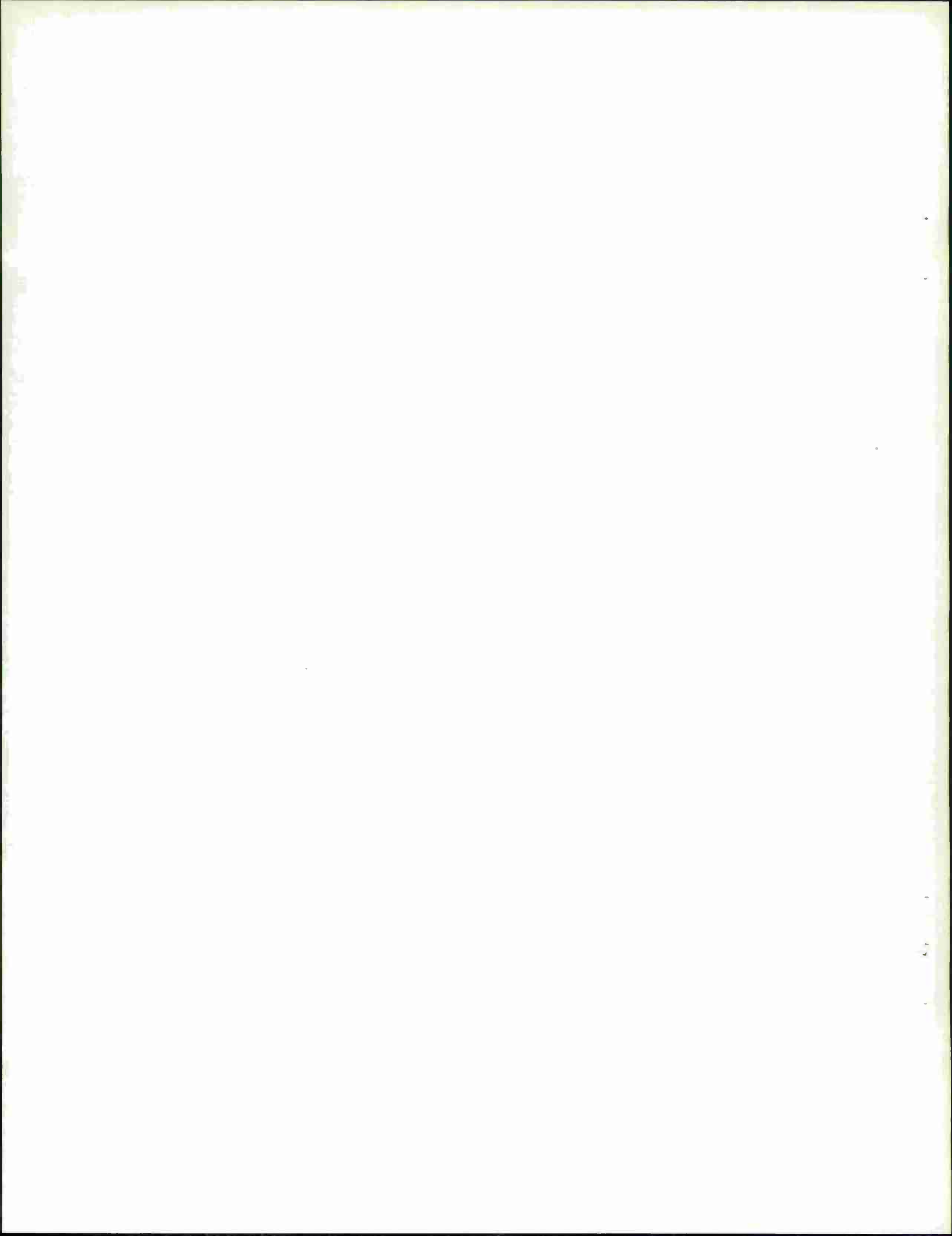
Appendix II Listing of Typical Data for 30 Transistors (SA2320)

PROBLEM 1										
TL =	0	IL =	56.56	VL =	672.4	RL =	38570.	R3 =	107910.	
TC =	25	IO =	44.63	VO =	622.4	RO =	10273.	RD =	50.	
TU =	60	IU =	33.40	VU =	552.0	RU =	2825.			
L =	1.1730712	U =	0.8438285	LU =	0.5858615					
R1 =	7543.1645	R1/ =	8110.0702					R1// =	08060.0702	
									R2 =	8645.8644
PROBLEM 2										
TL =	0	IL =	68.40	VL =	670.2	RL =	38810.	R3 =	94505.	
TC =	25	IO =	54.99	VO =	620.4	RO =	18472.	RD =	50.	
TU =	60	IU =	40.85	VU =	550.7	RU =	2924.			
L =	1.1514358	U =	0.8368836	LU =	0.5636177					
R1 =	5342.4581	R1/ =	5662.5685					R1// =	5612.5685	
									R2 =	6392.4775
PROBLEM 3										
TL =	0	IL =	62.12	VL =	686.7	RL =	25500.	R3 =	95564.	
TC =	25	IO =	49.08	VO =	637.2	RO =	5910.	RD =	50.	
TU =	60	IU =	35.92	VU =	566.2	RU =	2734.			
L =	1.1744529	U =	0.8236405	LU =	0.5673265					
R1 =	6100.0203	R1/ =	6525.9957					R1// =	6475.9957	
									R2 =	6483.4988
PROBLEM 4										
TL =	0	IL =	60.50	VL =	664.2	RL =	28300.	R3 =	93242.	
TC =	25	IO =	52.74	VO =	612.7	RO =	5620.	RD =	50.	
TU =	60	IU =	36.68	VU =	541.7	RU =	2692.			
L =	1.1981176	U =	0.7866440	LU =	0.5424928					
R1 =	5906.7896	R1/ =	6397.5575					R1// =	6347.5575	
									R2 =	4085.4763
PROBLEM 5										
TL =	0	IL =	52.21	VL =	669.7	RL =	25978.	R3 =	97859.	
TC =	25	IO =	43.94	VO =	618.4	RO =	18229.	RD =	50.	
TU =	60	IU =	34.37	VU =	546.8	RU =	2875.			
L =	1.0971925	U =	0.8046275	LU =	0.5786066					
R1 =	3213.9579	R1/ =	3323.0975					R1// =	3273.0975	
									R2 =	6382.9390
PROBLEM 6										
TL =	0	IL =	59.03	VL =	669.5	RL =	25348.	R3 =	98559.	
TC =	25	IO =	47.97	VO =	610.6	RO =	5992.	RD =	50.	
TU =	60	IU =	35.24	VU =	540.0	RU =	2800.			
L =	1.1370050	U =	0.8292692	LU =	0.5428832					
R1 =	3902.5003	R1/ =	4063.4013					R1// =	4013.4013	
									R2 =	4575.3671
PROBLEM 7										
TL =	0	IL =	55.87	VL =	676.7	RL =	25300.	R3 =	103000.	
TC =	25	IO =	44.57	VO =	625.4	RO =	5985.	RD =	50.	
TU =	60	IU =	33.22	VU =	551.7	RU =	2801.			
L =	1.1585845	U =	0.8449128	LU =	0.5788353					
R1 =	6086.1161	R1/ =	6460.0042					R1// =	6410.0042	
									R2 =	7363.4764
PROBLEM 8										
TL =	0	IL =	54.29	VL =	672.7	RL =	28495.	R3 =	100610.	
TC =	25	IO =	44.16	VO =	622.0	RO =	5715.	RD =	50.	
TU =	60	IU =	32.60	VU =	550.2	RU =	2725.			
L =	1.1367363	U =	0.8345615	LU =	0.5406763					
R1 =	3931.7014	R1/ =	4091.5954					R1// =	4041.5954	
									R2 =	4753.2052
PROBLEM 9										
TL =	0	IL =	58.09	VL =	674.6	RL =	38000.	R3 =	97854.	
TC =	25	IO =	48.30	VO =	624.1	RO =	18211.	RD =	50.	
TU =	60	IU =	36.65	VU =	552.8	RU =	2868.			
L =	1.1279822	U =	0.8566689	LU =	0.5663273					
R1 =	4330.0934	R1/ =	4533.1799					R1// =	4483.1799	
									R2 =	6276.9764
PROBLEM 10										
TL =	0	IL =	57.09	VL =	666.8	RL =	25850.	R3 =	94882.	
TC =	25	IO =	46.39	VO =	617.1	RO =	18118.	RD =	50.	
TU =	60	IU =	33.96	VU =	546.8	RU =	2816.			
L =	1.1500961	U =	0.8231609	LU =	0.5473727					
R1 =	4577.1713	R1/ =	4809.1600					R1// =	4759.1600	
									R2 =	5855.5770
PROBLEM 11										
TL =	0	IL =	64.50	VL =	680.1	RL =	31520.	R3 =	92205.	
TC =	25	IO =	52.00	VO =	680.9	RO =	18484.	RD =	50.	
TU =	60	IU =	38.07	VU =	537.8	RU =	2845.			
L =	1.1441754	U =	0.8463234	LU =	0.5603425					
R1 =	5156.7443	R1/ =	5462.2302					R1// =	5412.2302	
									R2 =	6815.5640
PROBLEM 12										
TL =	0	IL =	64.19	VL =	683.3	RL =	28820.	R3 =	96559.	
TC =	25	IO =	50.37	VO =	633.7	RO =	5831.	RD =	50.	
TU =	60	IU =	33.56	VU =	563.0	RU =	2763.			
L =	1.1010645	U =	0.7499379	LU =	0.8063258					
R1 =	4270.4507	R1/ =	4460.0564					R1// =	4418.0564	
									R2 =	2643.4752
PROBLEM 13										
TL =	0	IL =	51.51	VL =	659.5	RL =	38330.	R3 =	91503.	
TC =	25	IO =	41.47	VO =	600.4	RO =	18080.	RD =	50.	
TU =	60	IU =	31.32	VU =	537.2	RU =	2736.			
L =	1.1450609	U =	0.8553442	LU =	0.5801055					
R1 =	5547.6771	R1/ =	5985.7319					R1// =	5855.7319	
									R2 =	7624.9751
PROBLEM 14										
TL =	0	IL =	62.85	VL =	679.3	RL =	25290.	R3 =	103750.	
TC =	25	IO =	50.51	VO =	627.7	RO =	5943.	RD =	50.	
TU =	60	IU =	37.53	VU =	553.3	RU =	2771.			
L =	1.1407897	U =	0.8429322	LU =	0.5651948					
R1 =	5224.3306	R1/ =	5501.3599					R1// =	5451.3599	
									R2 =	6586.6543
PROBLEM 15										
TL =	0	IL =	64.10	VL =	669.3	RL =	25998.	R3 =	98750.	
TC =	25	IO =	52.30	VO =	618.4	RO =	18226.	RD =	50.	
TU =	60	IU =	39.06	VU =	548.4	RU =	2873.			
L =	1.1324134	U =	0.8594243	LU =	0.5722236					
R1 =	4804.5420	R1/ =	5050.2341					R1// =	5000.2341	
									R2 =	6952.0546

Appendix II Printout Solution for the First 15 Problems

REFERENCES

1. J. N. Harris and K. E. Perry, "Characteristics and Applications of Solid State Operational Amplifiers," Group Report 62G-2, Lincoln Laboratory, M. I. T., (July 1963).
2. Handbook of Operational Amplifier Applications, Burr-Brown Research Corporation, Tucson, Arizona.
3. "Data Sheets on Model P2 Operational Amplifier," (George A. Philbrick Researches, Inc., Boston, Massachusetts).
4. "Field Effect Transistor Theory and Applications," report by Texas Instruments Incorporated, Dallas, Texas.
5. S. W. Holcomb, "Dual Transistors in Low-Level Circuits," Texas Instruments Incorporated, Dallas, Texas, (July 20, 1963).
6. J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," Proc. IRE 42, No. 12, pp. 1761-1772 (December 1954).
7. "Transistor Bias Compensation with Silicon Resistors," Application Notes, Texas Instruments, Inc., (April 1960).
8. "Considerations in the Testing of Thermistors," Fenwal Electronics, Inc.
9. "Thermistor Manual," EMC-5, Fenwal Electronics, Inc.
10. "Thermistors," EMC-1, Fenwal Electronics, Inc.
11. M. Sapoff and R. M. Oppenheim, "Theory and Application of Self-Heated Thermistors," Proc. IEEE 51, No. 10, pp. 1292-1305.
12. R. D. Middlebrook, Differential Amplifiers, (John Wiley and Sons).



BIBLIOGRAPHY

1. P. J. Beneteau, "The Design of High Stability DC Amplifiers," Semiconductor Products, (February 1961), pp. 27-30. Also available as APP-23, Fairchild Semiconductor, Mountain View, California.
2. P. H. Beneteau, L. Blaser and R. Q. Lane, Transistor Operational Amplifiers. IRE Convention Record, Part 9, (March 1962), pp. 173-185.
3. J. R. Biard and W. T. Matzen, "Drift Considerations in Low Level Direct-Coupled Transistor Circuits," (Texas Instruments, Inc.).
4. F. H. Blecher, "Transistor Circuits for Analog and Digital Systems", BSTJ, (March 1956), pp. 295-332.
5. Richard D. Brugger, "Extending An Operational Amplifier's Bandwidth to 50-Mc.," Electronic Design, pp. 50-55 (25 May 1964).
6. Burr-Brown Research Corporation, Engineering Manual, "Transistorized Amplifiers".
7. C. M. Cundall, et al, "D. C. Amplifiers for Use in Analog Computers", Proc. IEE, (April 1960), pp. 1354-1364.
8. W. M. DeMatters, "A Direct-Coupled Differential Amplifier", Application Lab Report 713, Philco Corp.
9. R. O. Gregory, "Design Considerations in a Chopper-Stabilized Transistor Operational Amplifier", presented at IRE Maecon, Kansas City, Mo., (Nov. 15-16, 1960).
10. E. A. Goldberg, "Stabilization of Wide-Band Direct-Current Amplifiers for Zero and Gain", RCA Review, (June 1950), pp. 296-300.
11. J. W. Halligan, "Silicon Transistor Operational Amplifier Circuits", Application Lab. Report 720, Philco Corp.
12. J. W. Halligan, "A Compact Direct Coupled Utility Amplifier", Application Lab Report 746, Philco Corp.
13. D. F. Hilbiber, "New D-C Transistor Differential Amplifier", presented at solid state circuits Conference, Philadelphia, Pa., (15 Feb. 1961). Also available as TP-16, Fairchild Semiconductor, Mountain View, California.

BIBLIOGRAPHY (CONTINUED)

14. S. Hochwald and F.H. Gerhard, "A Drift-Compensated D. C. Operational Amplifier Employing a Low-Level Silicon Transistor Chopper", Proc. IRE, NEC, Chicago, Ill. (1958) Computers, 14, pp 798-810.
15. A.H. Hoffait and R. D. Thornton, "Limitations of Transistor DC Amplifiers", Proc. IEEE 52, No. 2, pp. 179-184 (February (1964).
16. R. M. Howe, Van Nostrand, Analog Computer Components, (1961) Chapter 3.
17. Hunter, Handbook of Semiconductor Electronics, (McGraw-Hill 1956), Section 13.
18. Korn and Korn, Electronic Analog Computers, (McGraw-Hill 1956), Chapter 5.
19. Landee, Davis, Albrecht, Electronic Designer's Handbook, (McGraw-Hill 1957) Chapter 19.
20. W. T. Matzen and J. R. Biard, "Differential Amplifier Features D-C Stability Electronics" (16 January 1959).
21. R. H. Okada, Stable Transistor Wideband DC Amplifiers, (Transactions of the AIEE), (March 1960), p. 26.
22. George A. Philbrick Researches, Inc. , Boston, Massachusetts, "Data Sheets on the Model P45 Operational Amplifier".
23. George A. Philbrick Researches, Inc. , Boston, Massachusetts "Design of a Modern High-Performance Amplifier", Lightning Empiricist 11, No. 2, p. 3. (1 April 1963)
24. George A. Philbrick Researches, Inc. , "Application Manual".
25. Texas Instruments Incorporated, Engineering Staff, (McGraw-Hill 1963), Chapter 8, Transistor Circuit Design.
26. Valley and Wallman, Vacuum Tube Amplifiers, (McGraw-Hill 1948).

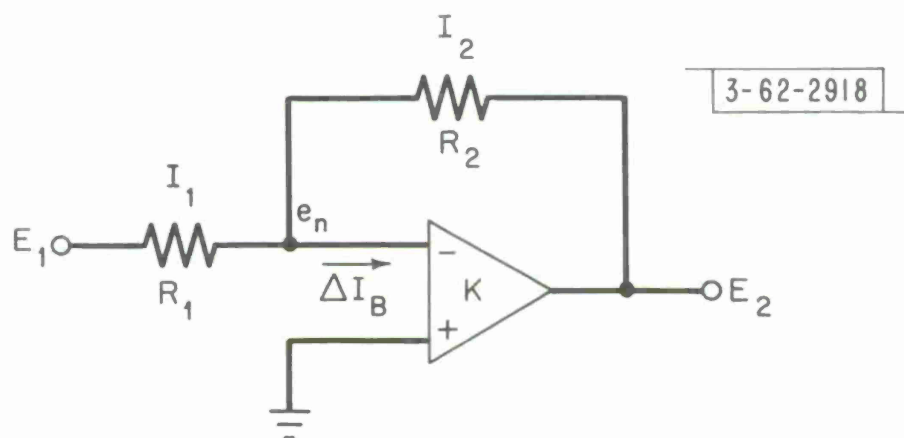


Fig. 1. Inverting amplifier with input leakage current

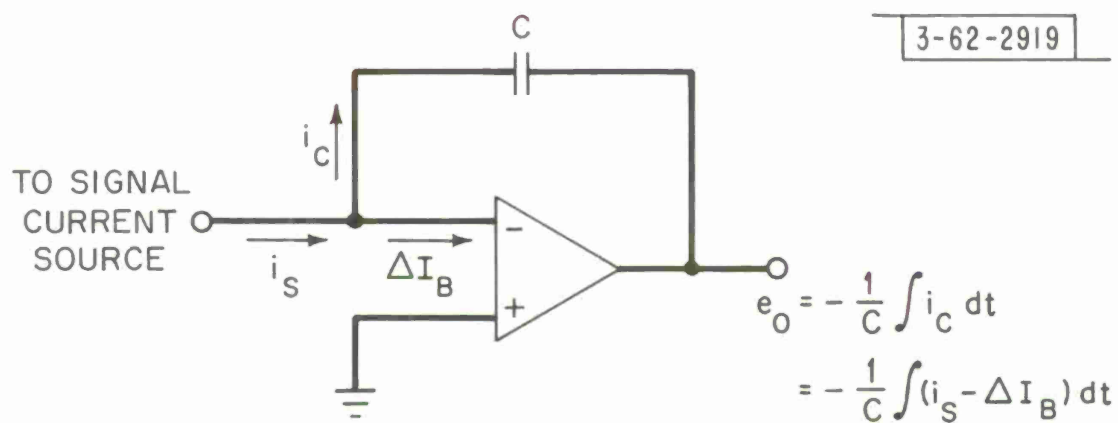


Fig. 2. Integrator with input leakage current

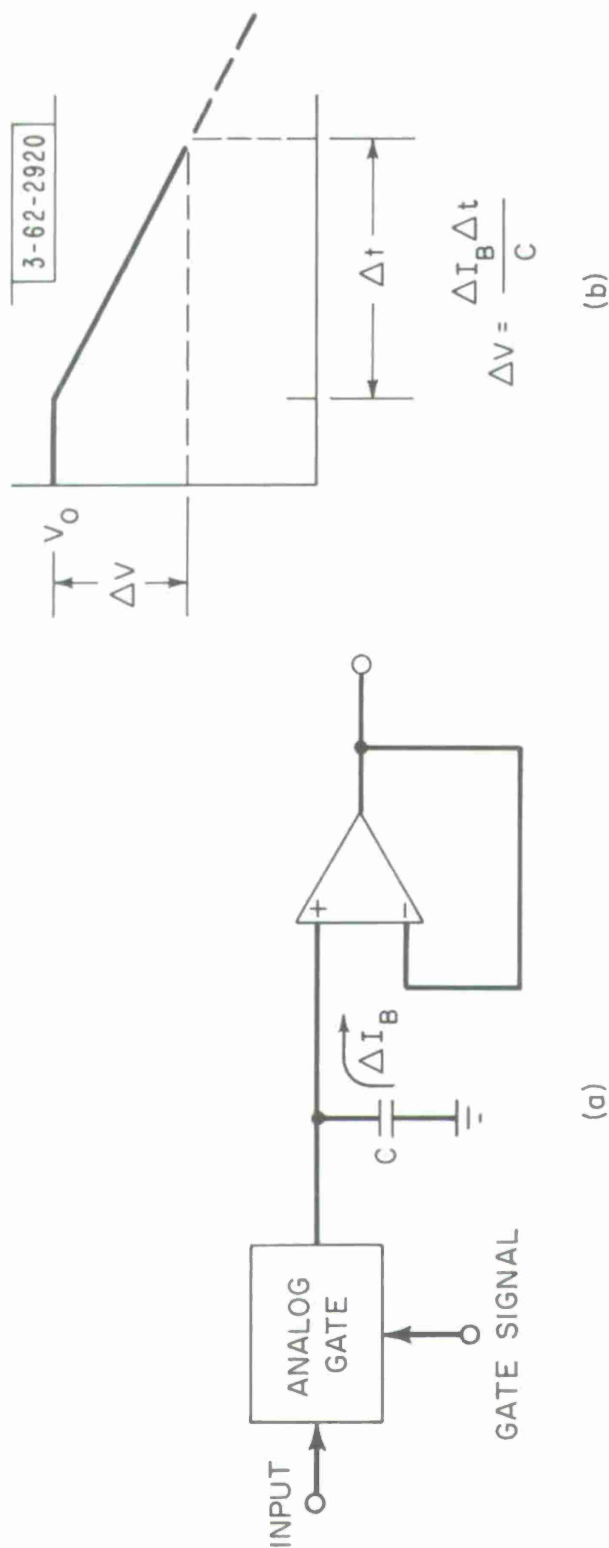


Fig. 3 (a) Sample and hold circuit with input leakage current
(b) Voltage decay due to the input leakage current discharging the capacitor, C.

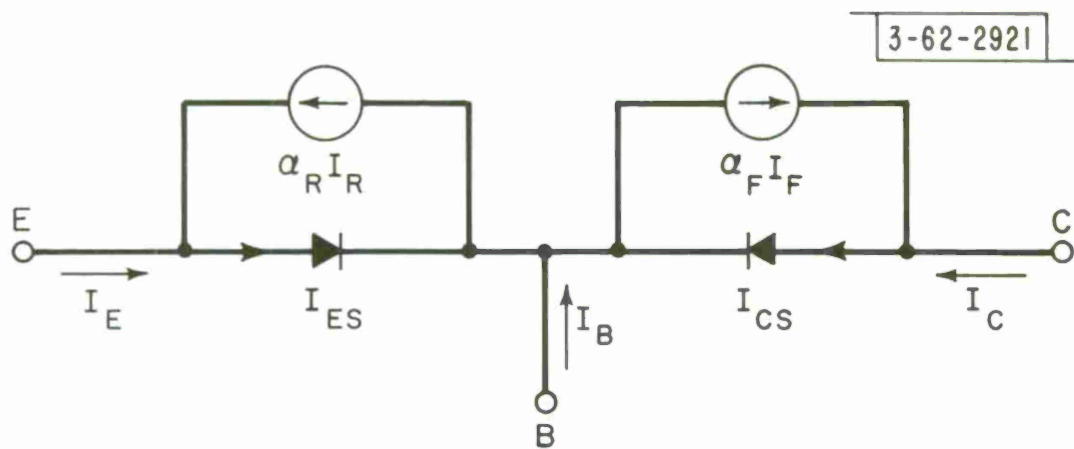


Fig. 4. The Ebers-Moll large signal model

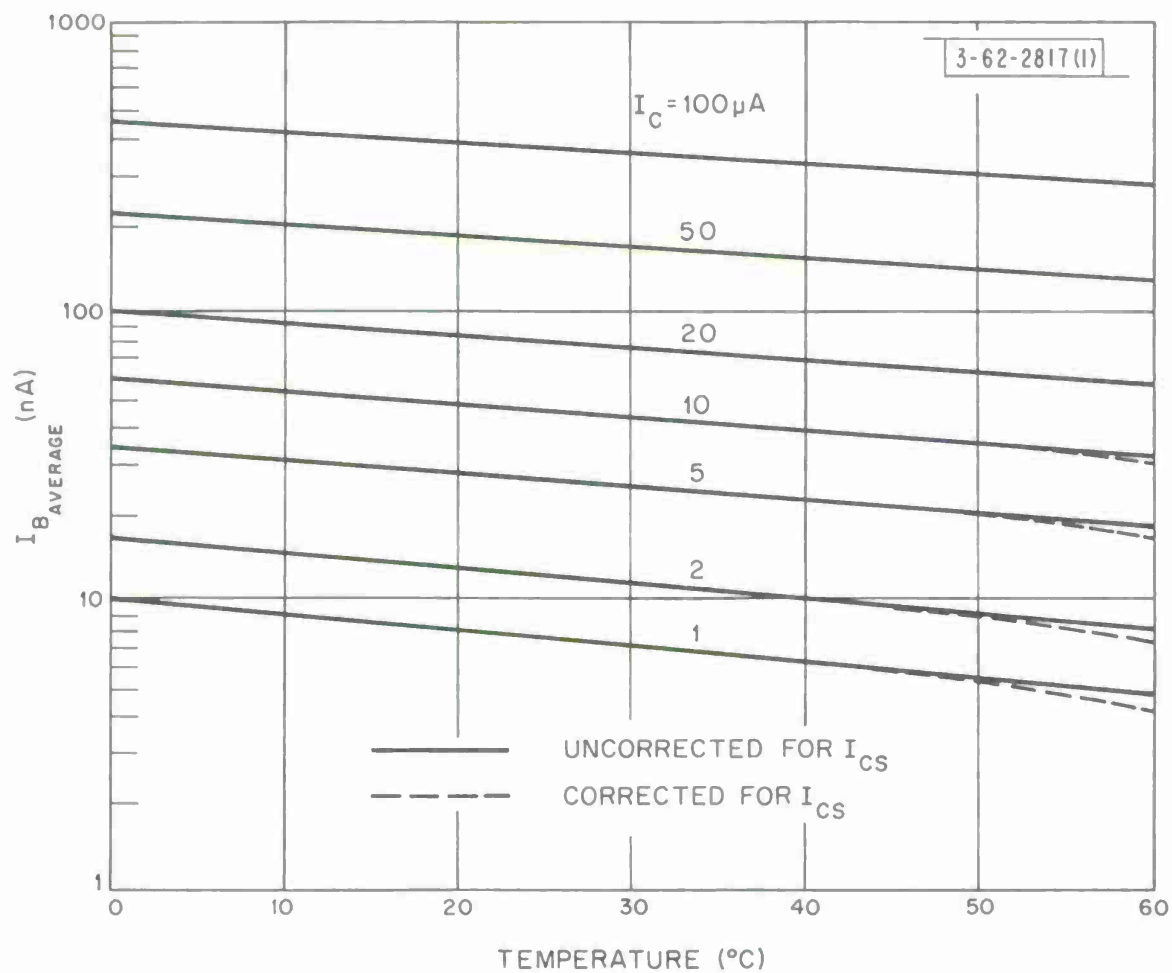


Fig. 5. Base current for the 2N2920 transistors. The average value for 20 samples is shown. Note the increase in the influence of collector leakage current at low collector currents.

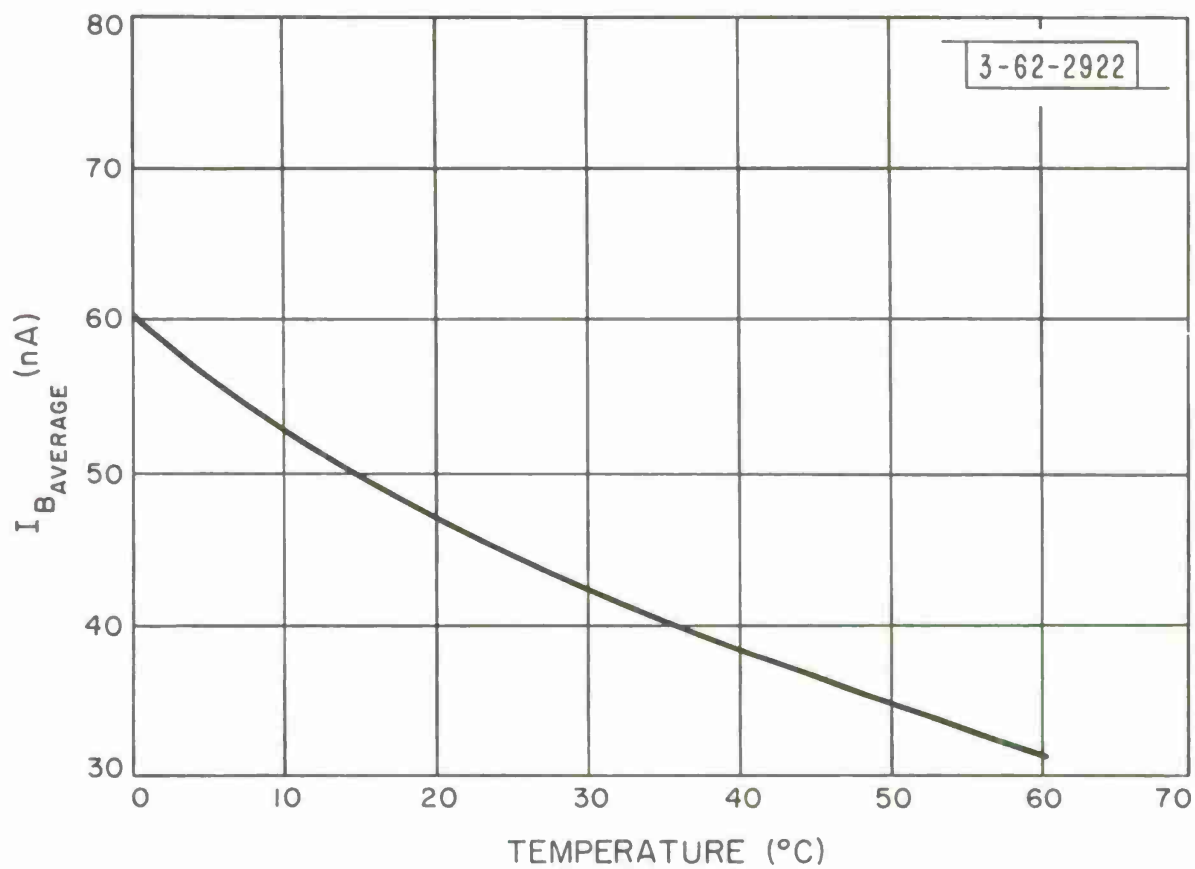


Fig. 6. A detailed plot of the variation of base current with temperature at a collector current of $10 \mu\text{A}$. The same 20 samples of 2N2920 transistors have been used.

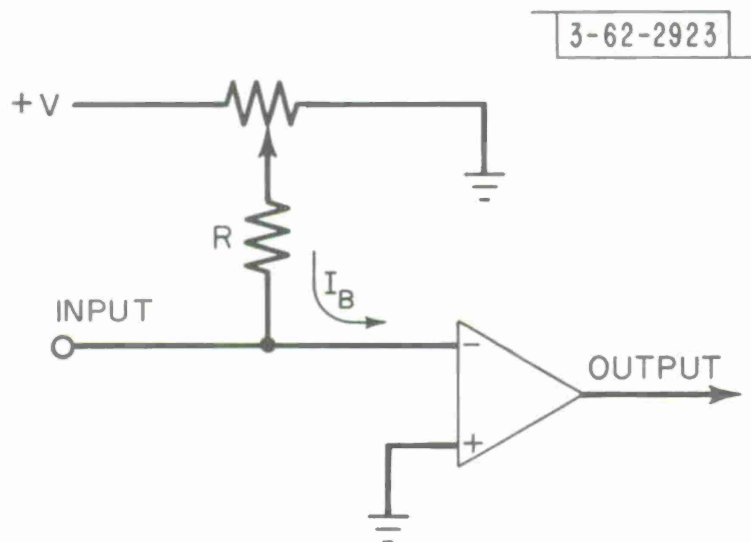


Fig. 7. Resistive (constant-current) compensation

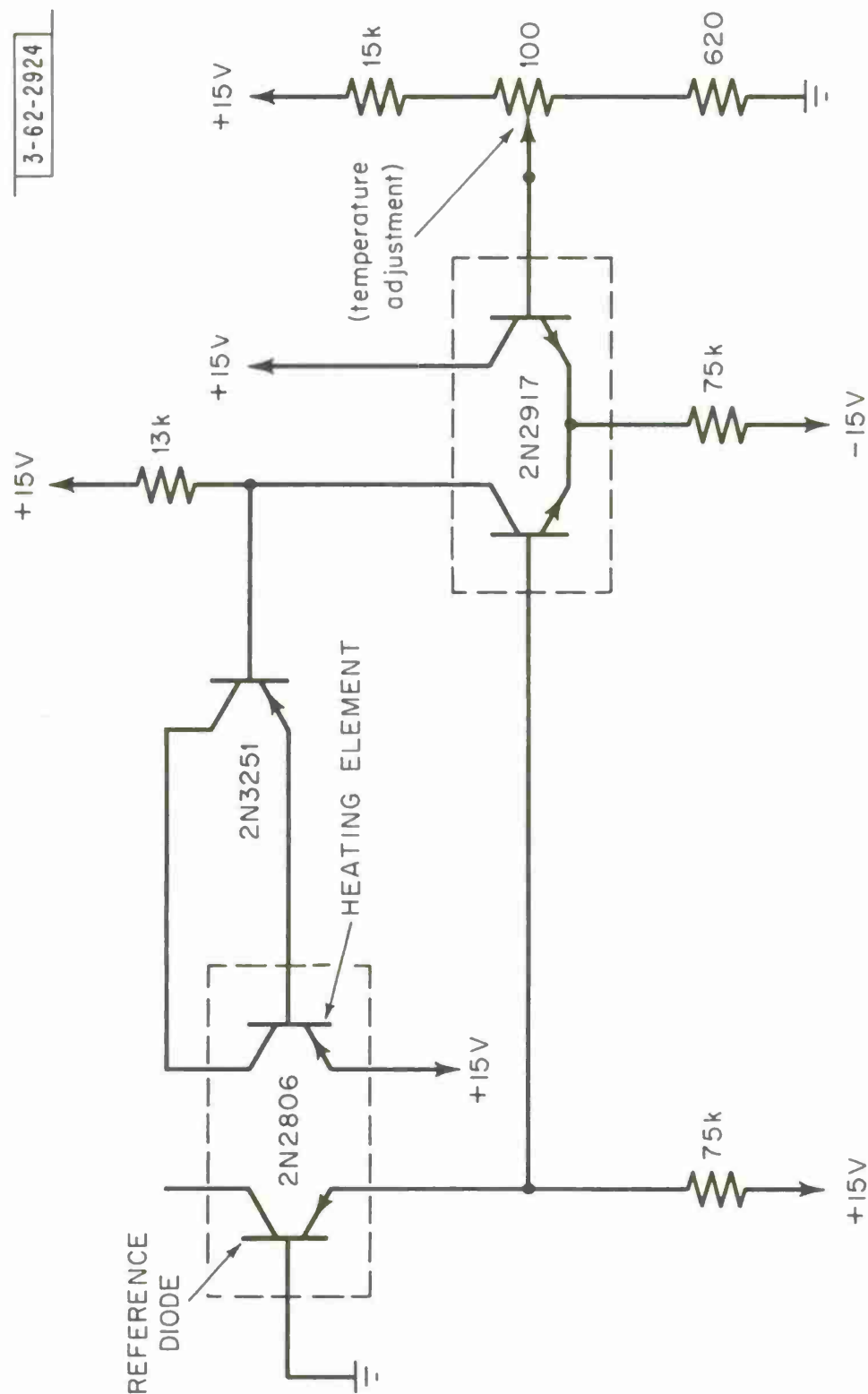


Fig. 8. Schematic for the T0-5 constant temperature oven which is described in the Text, VI C.

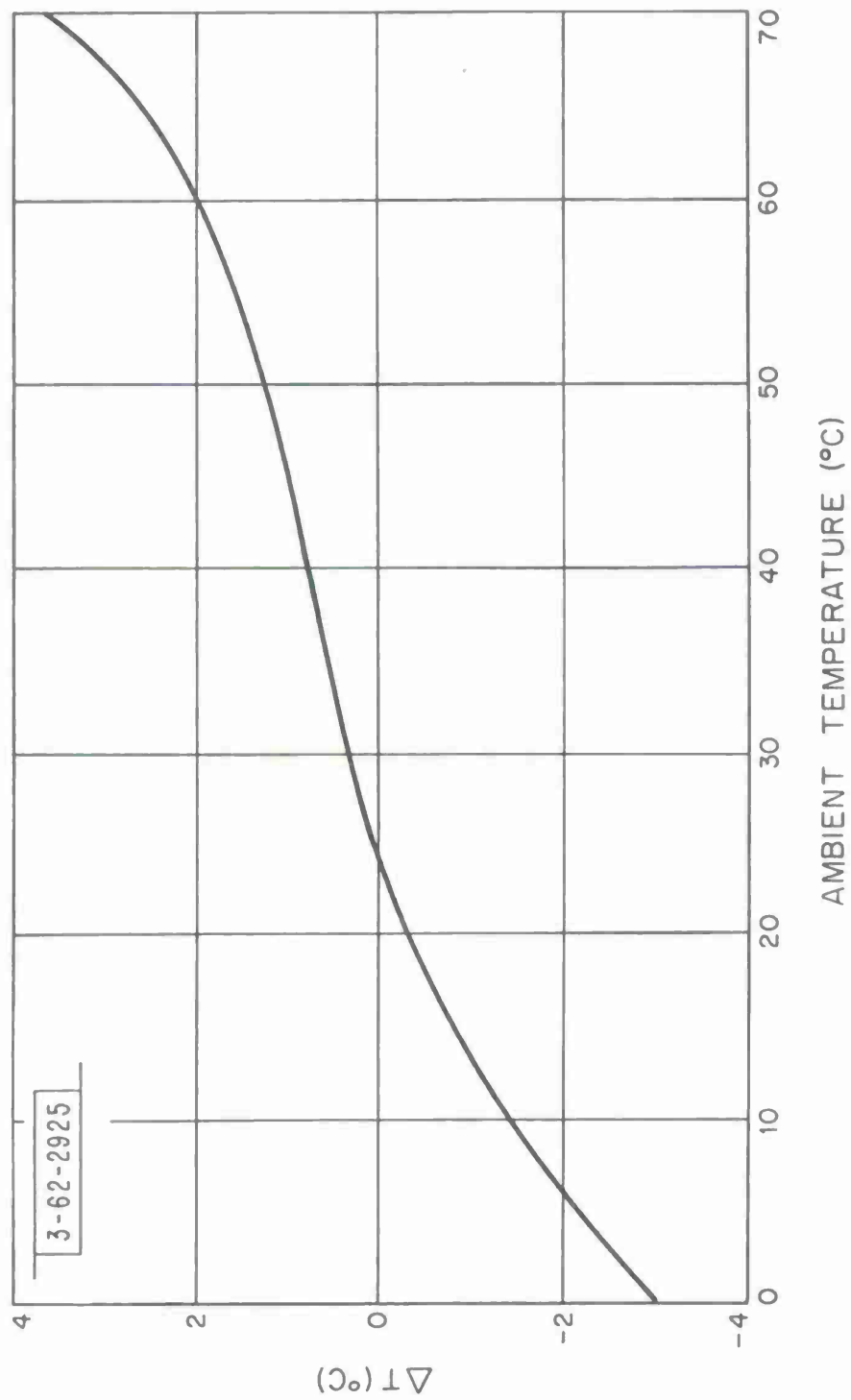


Fig. 9. Temperature variation of the interior of the T0-5 oven with a 70 $^{\circ}\text{C}$ variation in ambient temperature.

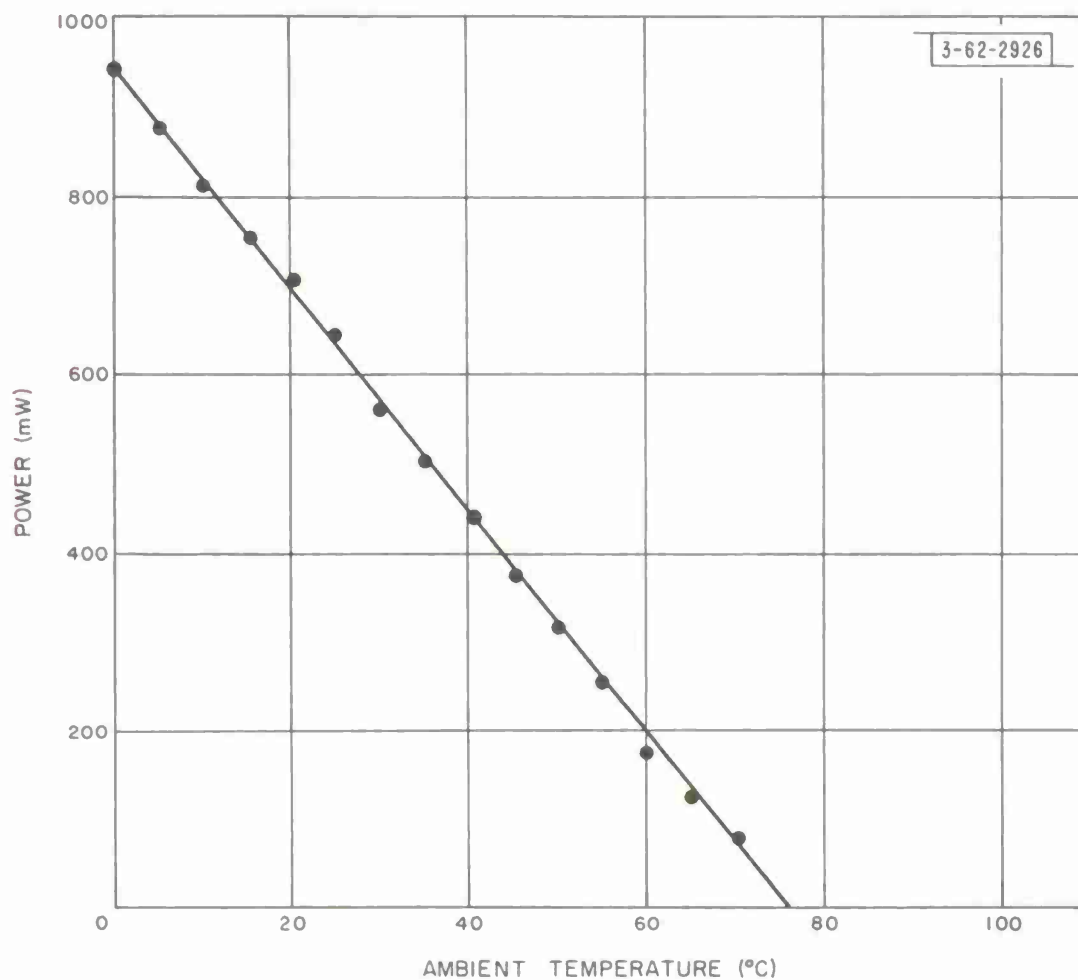


Fig. 10. Power requirement for the T0-5 oven as the ambient temperature is varied from 0 to 75°C. No insulation was used to reduce the heat loss.

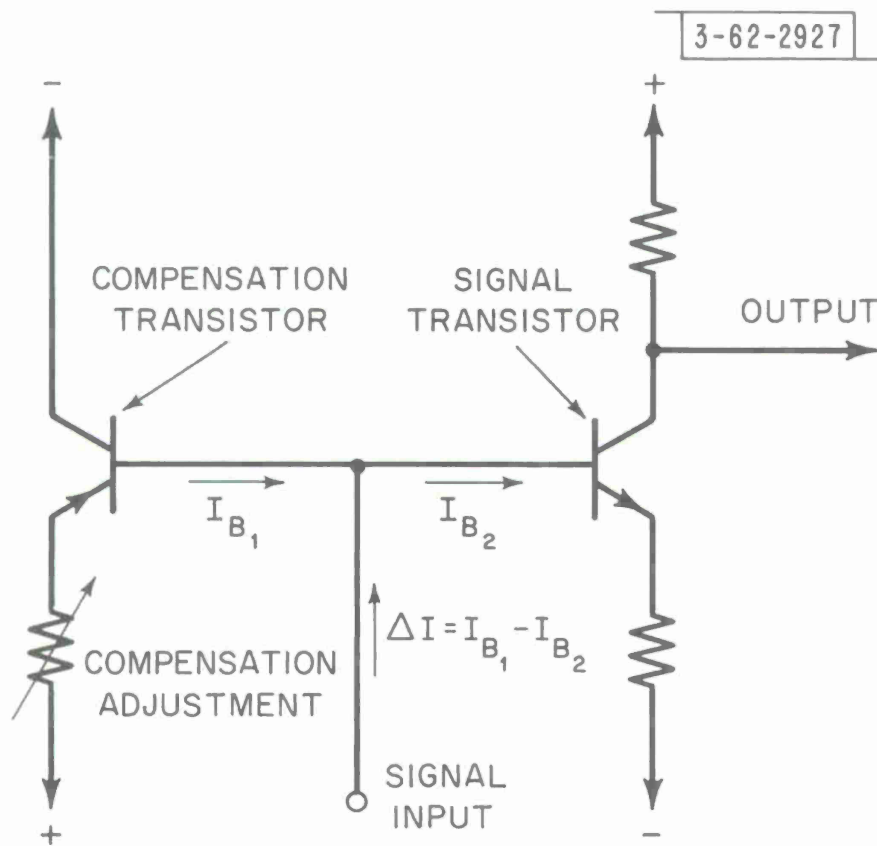


Fig. 11. Complementary compensation circuit

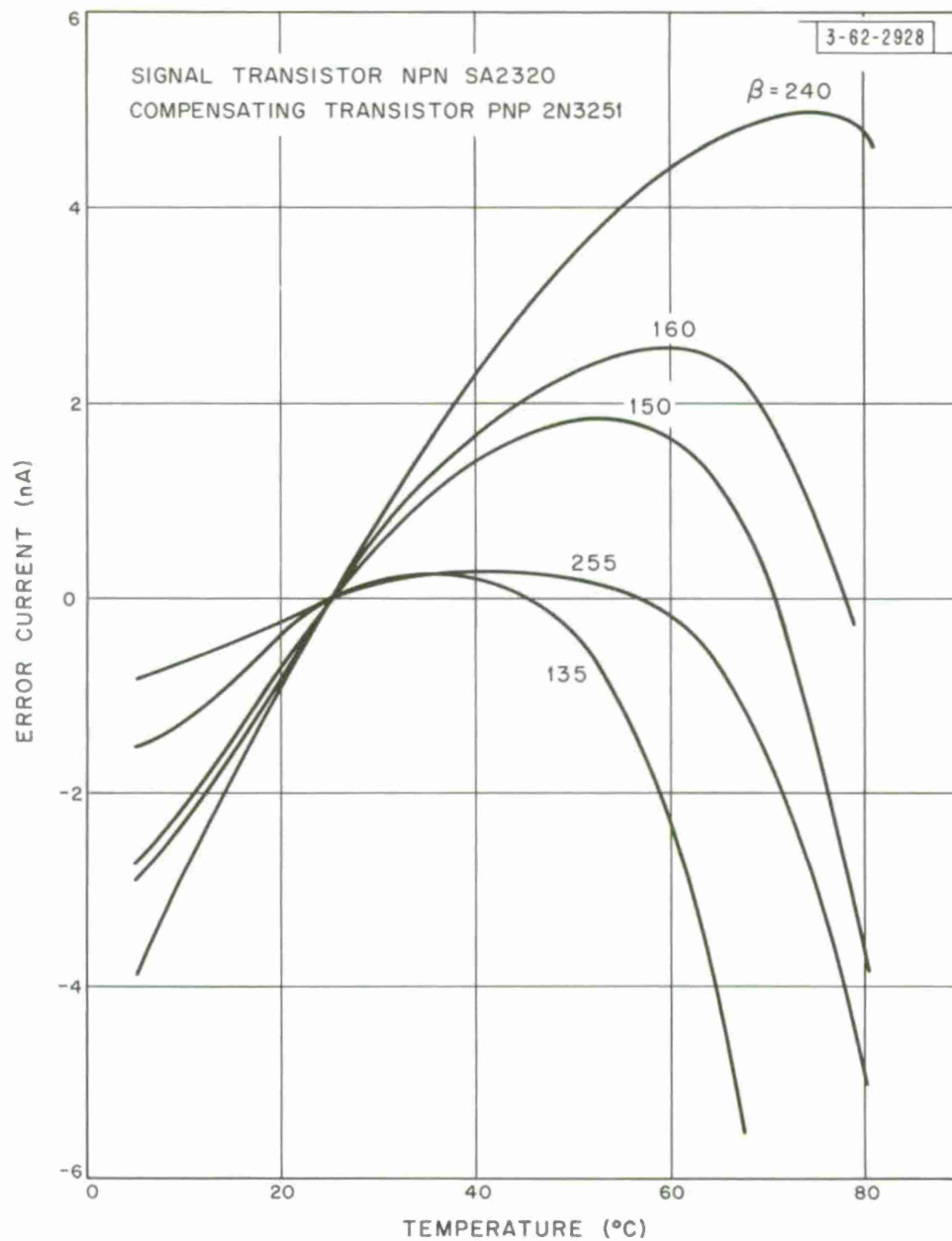


Fig. 12. Error current for complementary compensation. Curves for five different NPN transistors are shown. Note that there is apparently no correlation between the shape of the curve and the beta of the transistor.

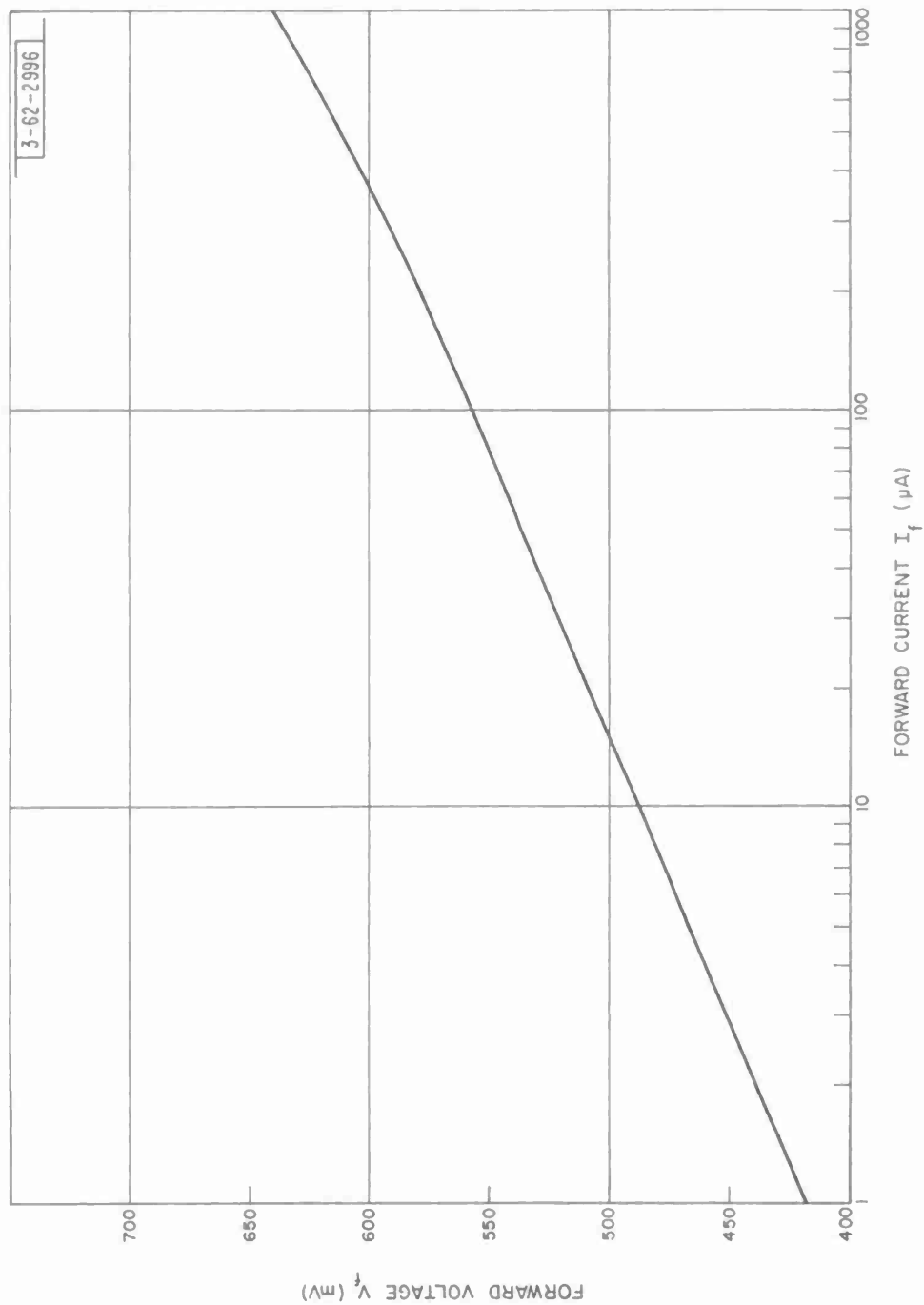


Fig. 13. Diode forward voltage vs. current for a SG-22 diode at 25°C. Note the very good logarithmic relation.

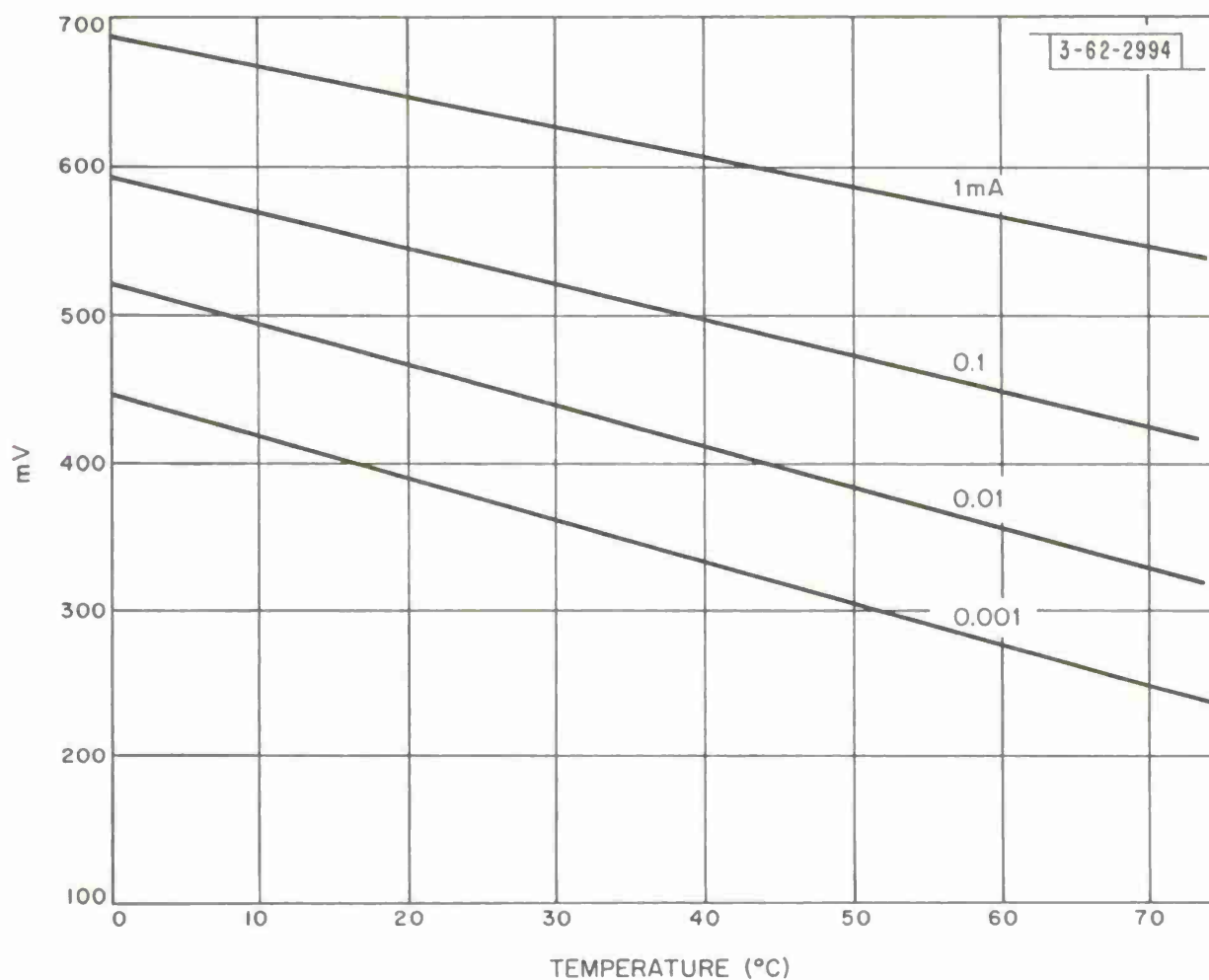


Fig. 14. Diode forward voltage vs. temperature for different forward current levels. Note the increase in slope as the current becomes smaller. (SG-22 diode)

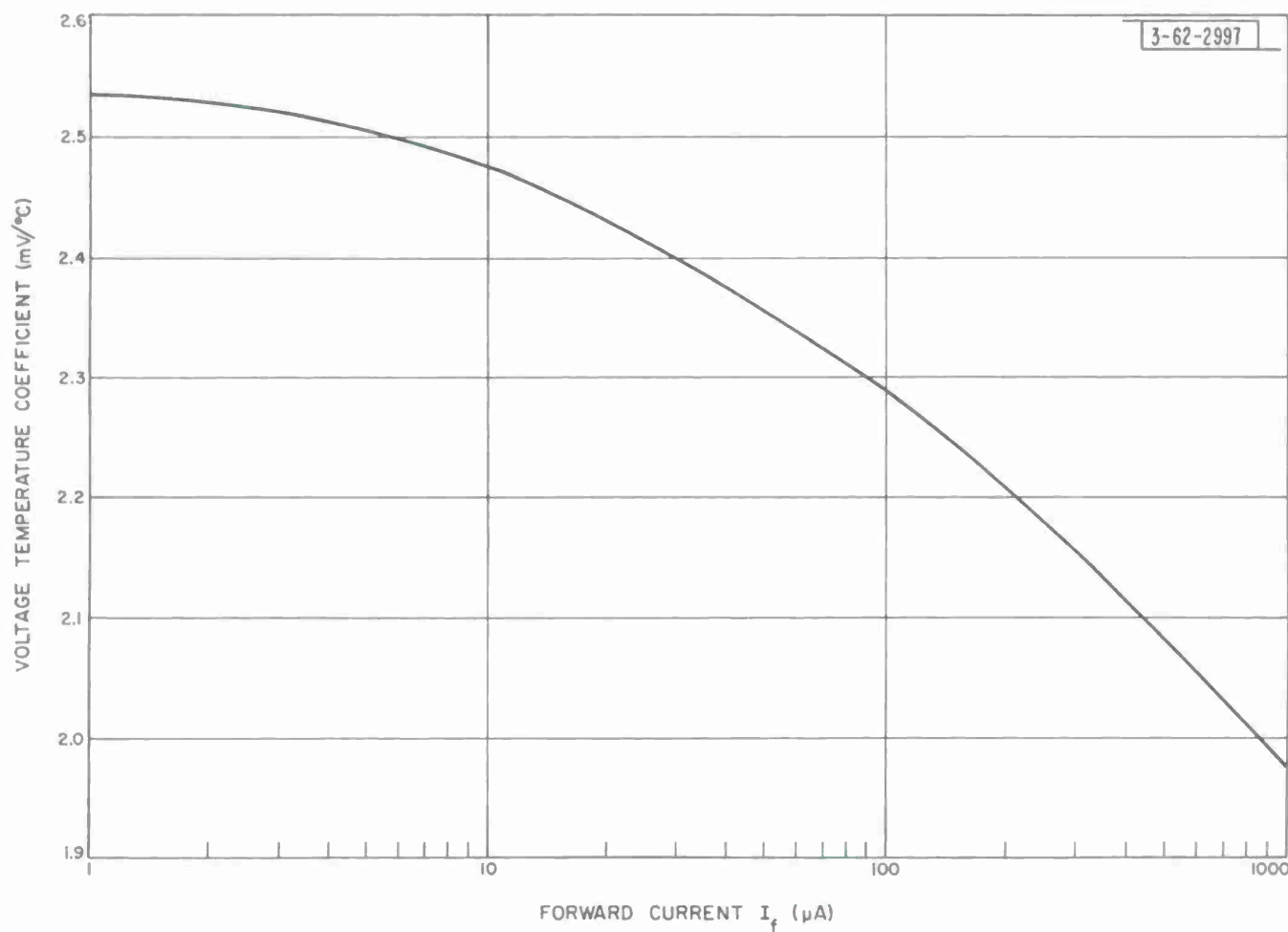


Fig. 15. Voltage temperature coefficient vs. forward current for an SG-22 diode. Note the increase in TC with low currents. This fact permits the diode to be used for a compensating circuit as explained in the Text, IV E.

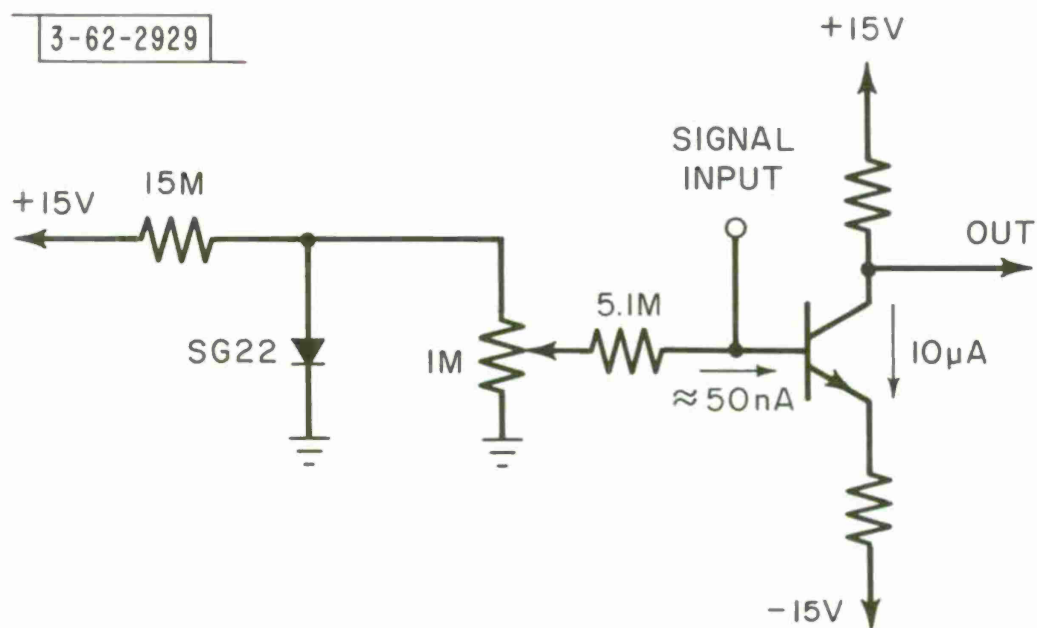


Fig. 16. Diode compensation circuit

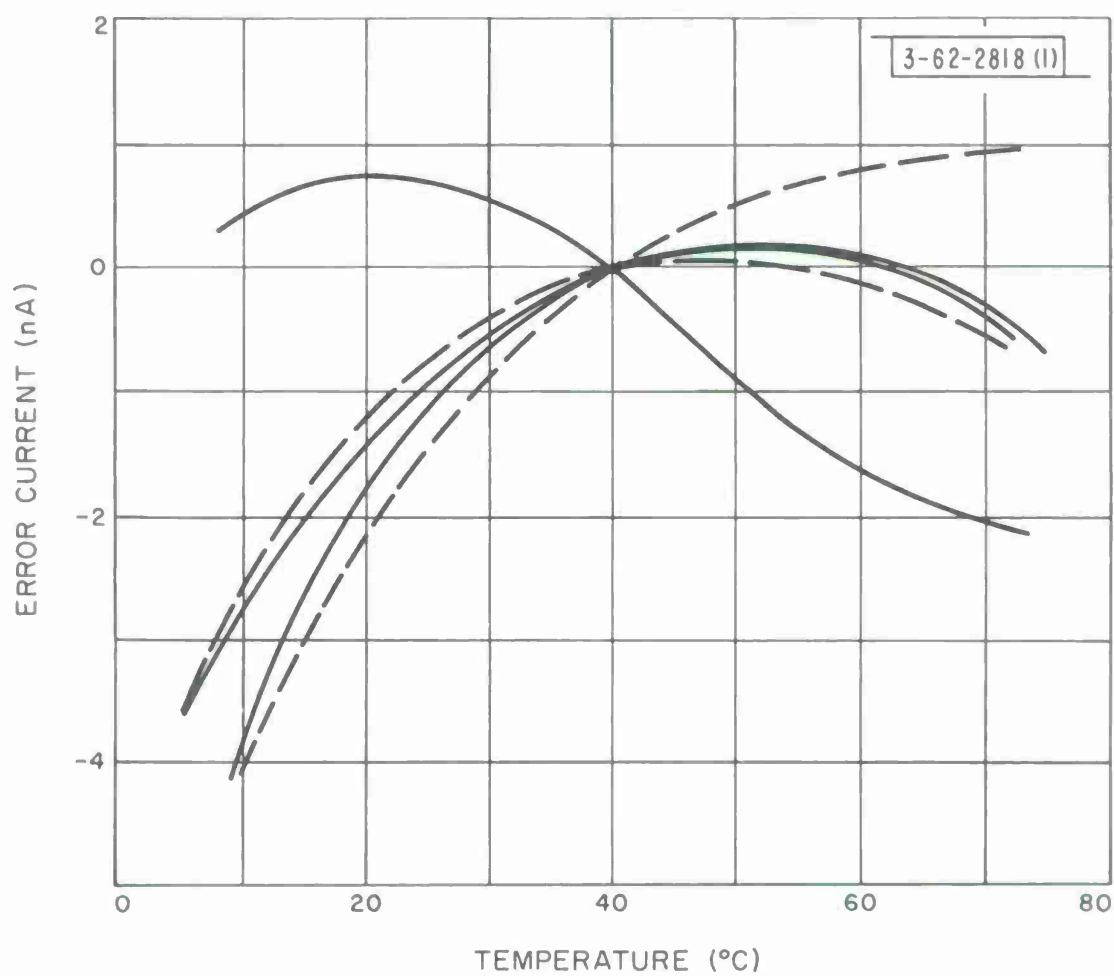


Fig. 17. Error current for diode compensation. The results are shown for five different transistors, all adjusted for zero error (or input) current at 40°C.

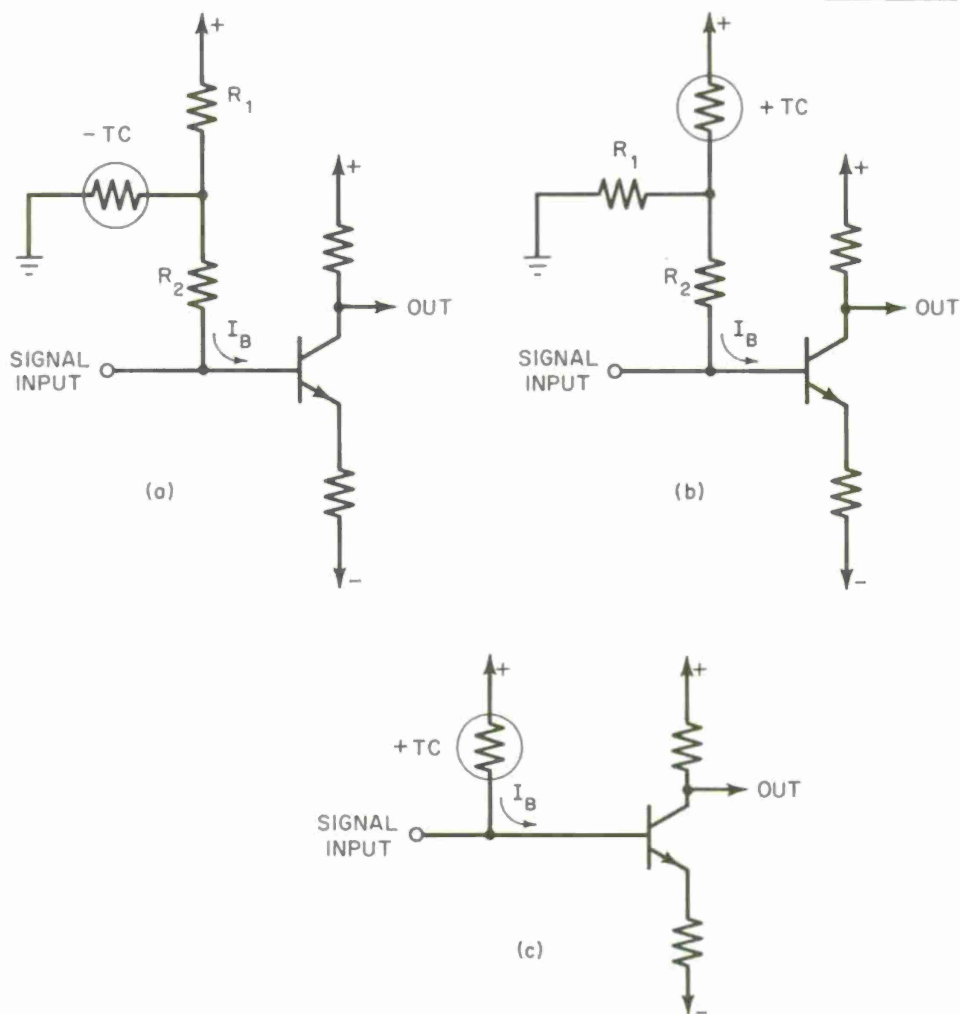


Fig. 18. Compensation circuits using temperature sensitive resistors. Both negative and positive TC elements are shown.

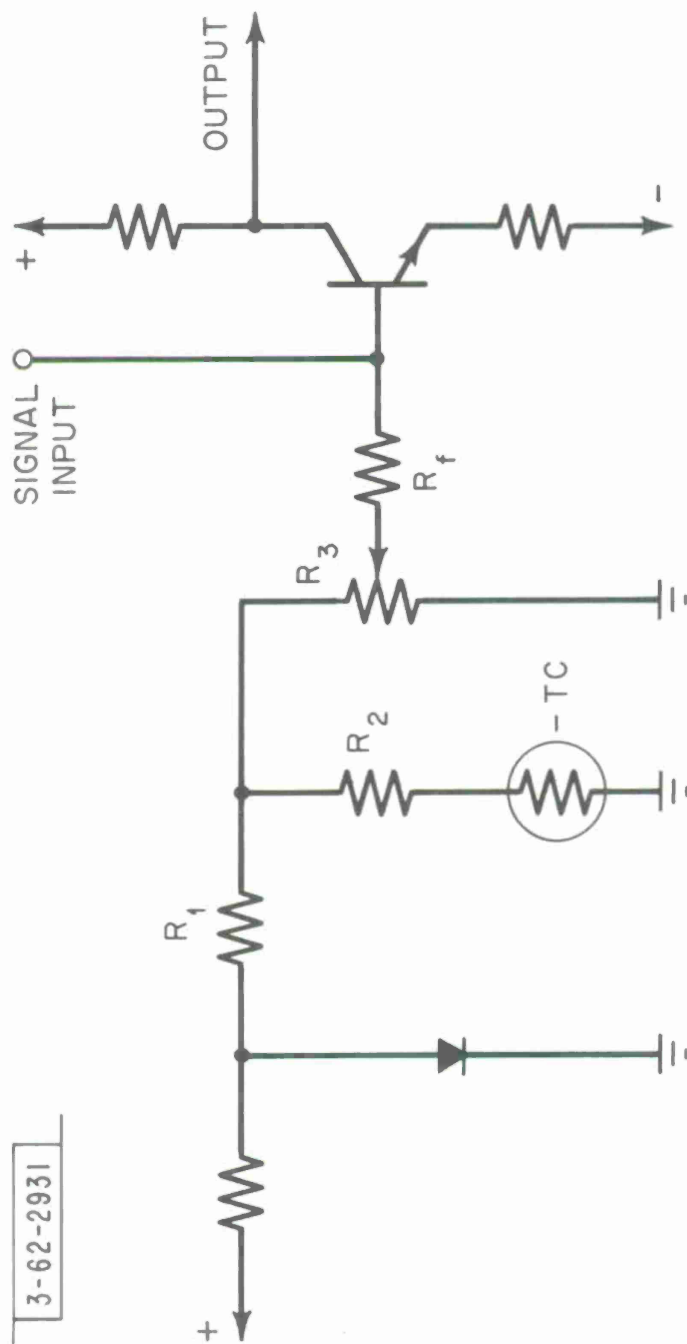


Fig. 19. Resistor - thermistor compensation circuit

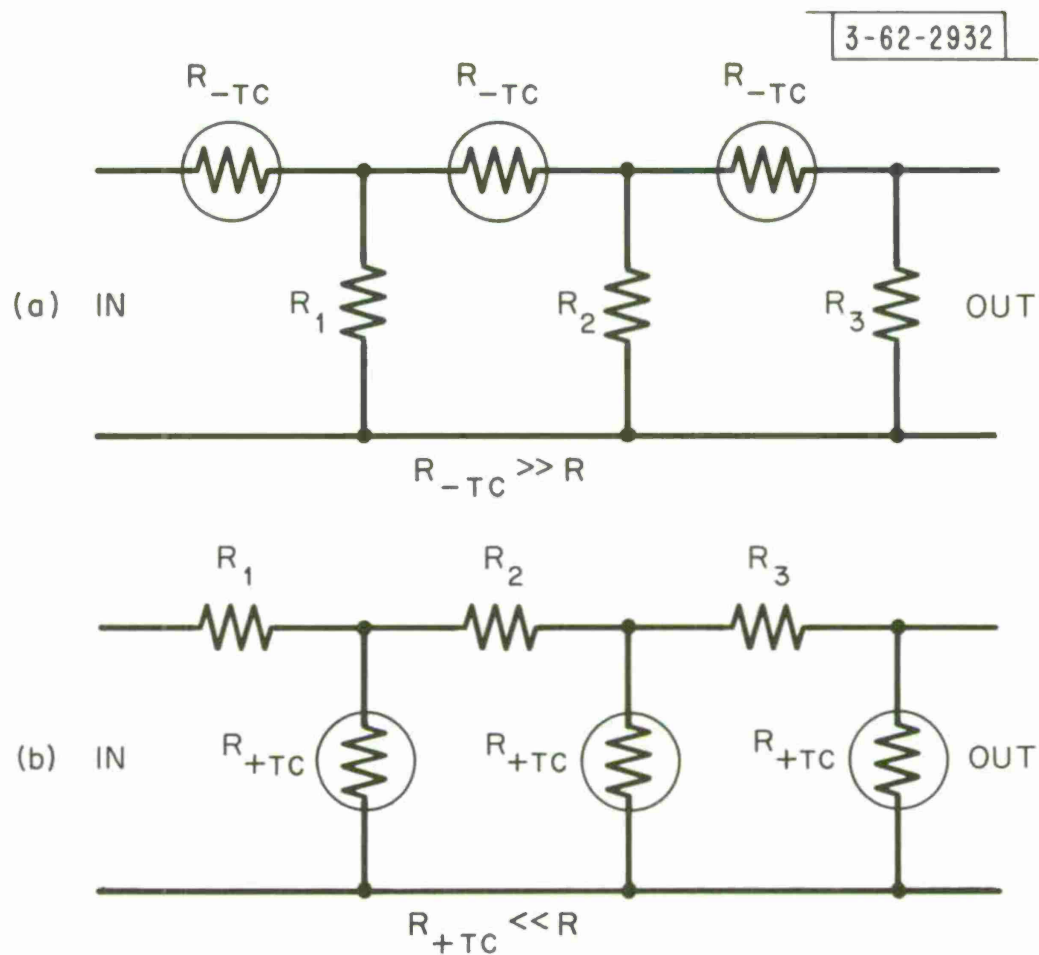


Fig. 20. Cascade of temperature sensitive resistors which can be used to increase the effective temperature coefficient. The values of R_1 , R_2 and R_3 must be suitably chosen so as to provide isolation between the TC elements. The number of stages will determine the increase in TC which can be obtained.

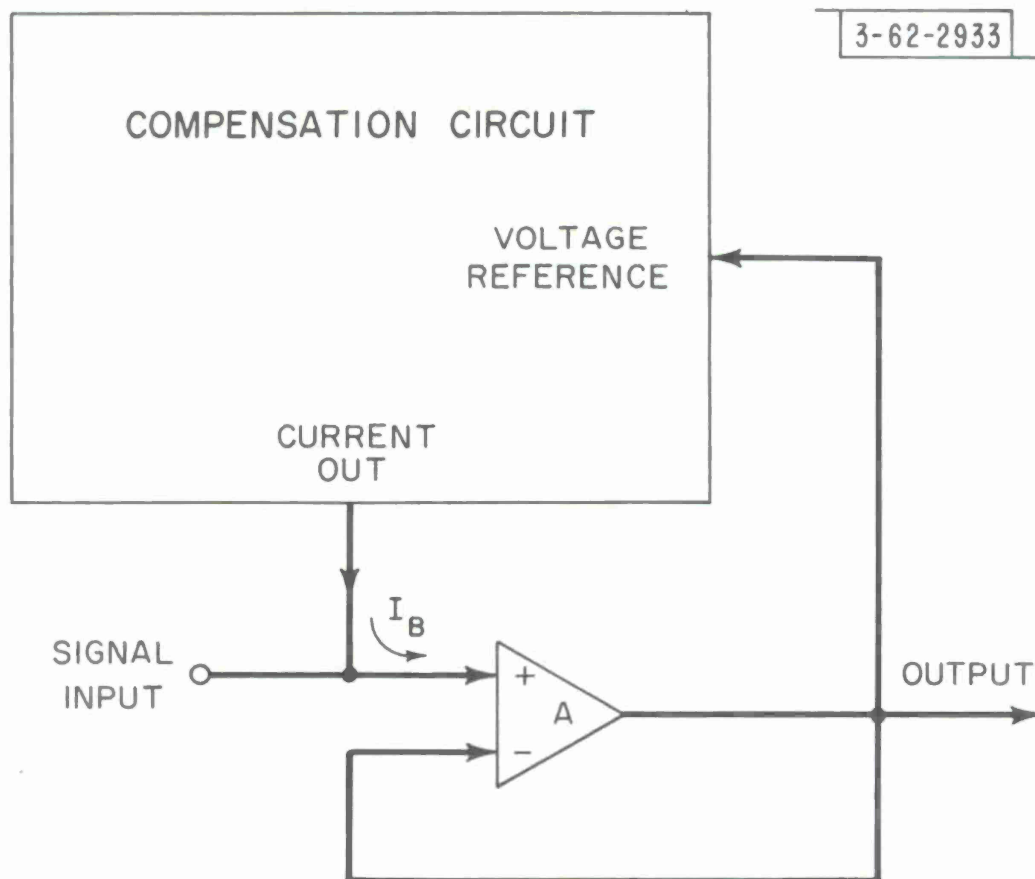


Fig. 21. Compensation circuit used with a voltage follower connected amplifier. For this application the input (and hence the output) terminal of the amplifier follows the signal. It is therefore necessary to reference the compensation to this signal at the output.

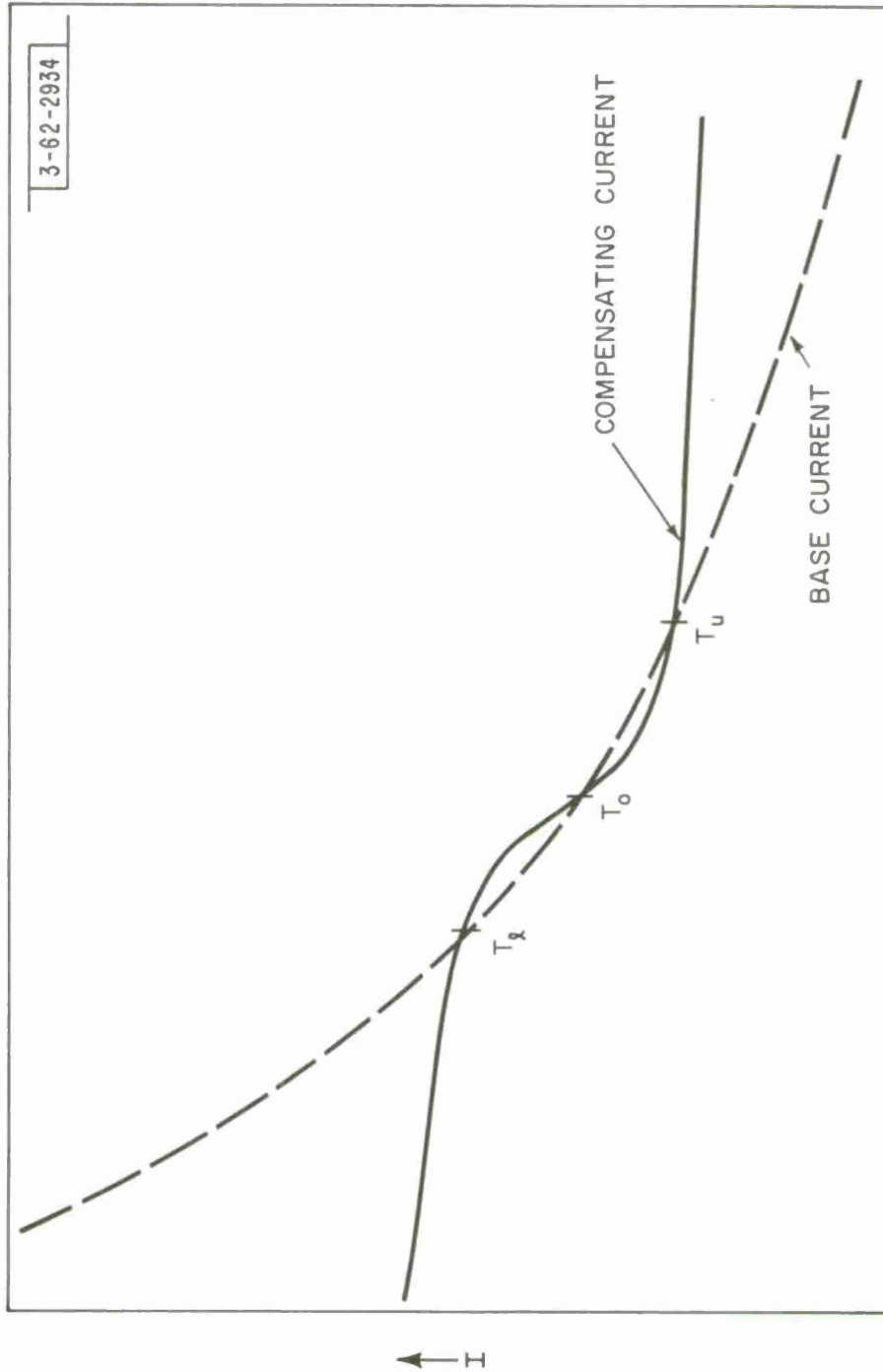


Fig. 22. Comparison of the input base current and the current developed by the compensating circuit (idealized). The "S" curve about the temperature points is typical of this kind of circuit.

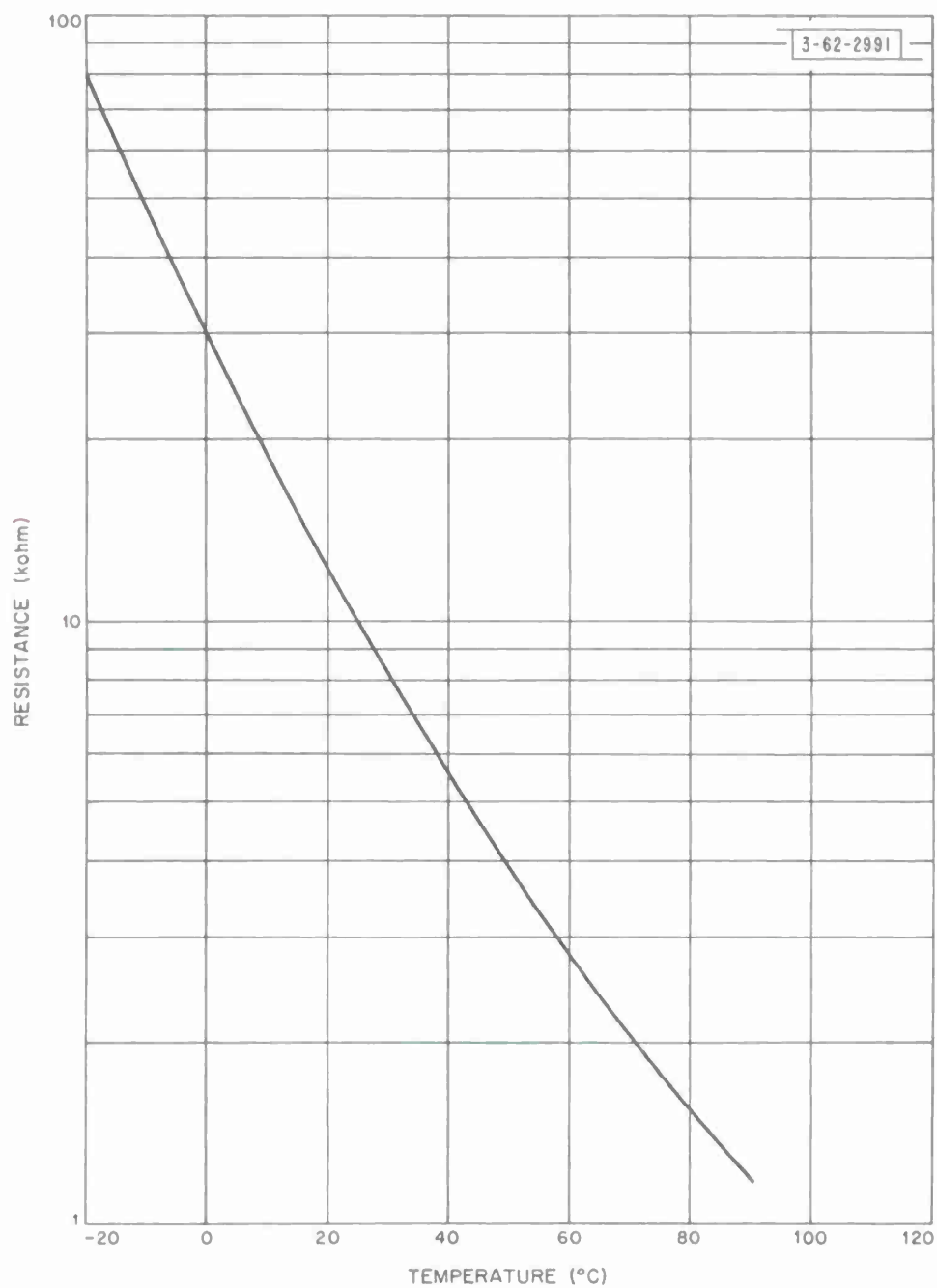


Fig. 23. Typical resistance vs. temperature curve for a $10\text{K}\Omega$ (at 25°C) thermistor. The constants of this thermistor are $\beta = 3495^\circ\text{K}$ and $\alpha = -3.97\%/^\circ\text{C}$ (at 25°C). See Text, V B.

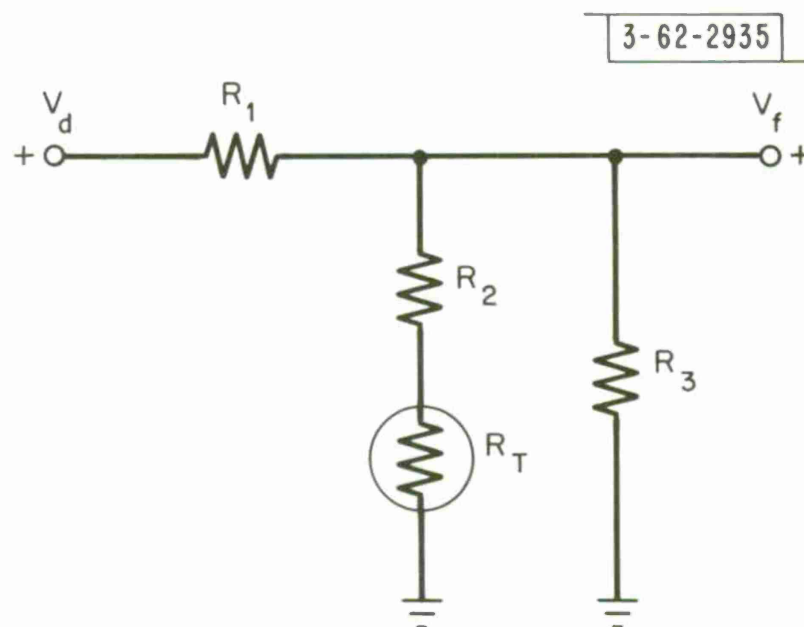


Fig. 24. Analytical model for the resistor-thermistor compensation circuit.

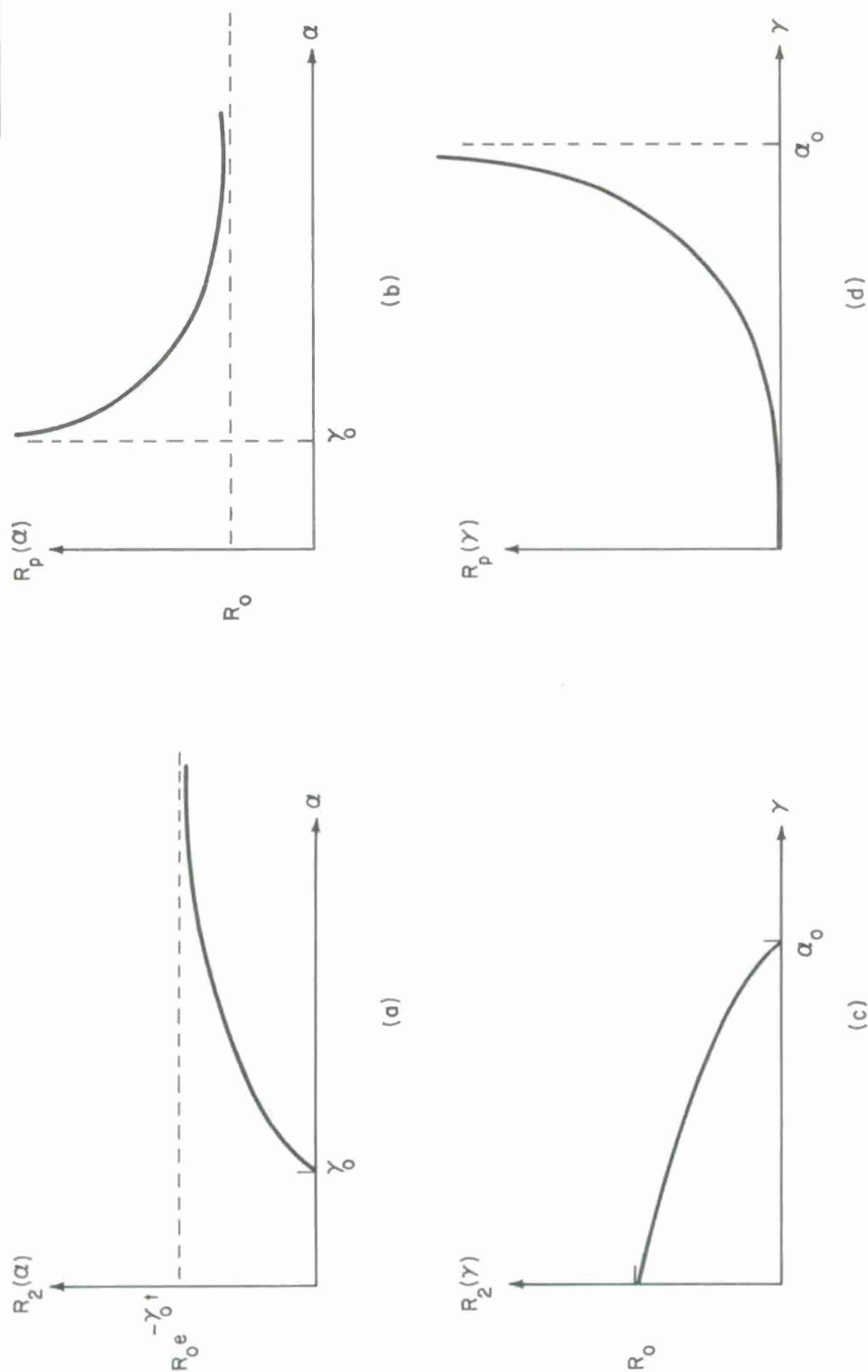


Fig. 25. R_2 and R_p versus α and γ (resistor-thermistor model)

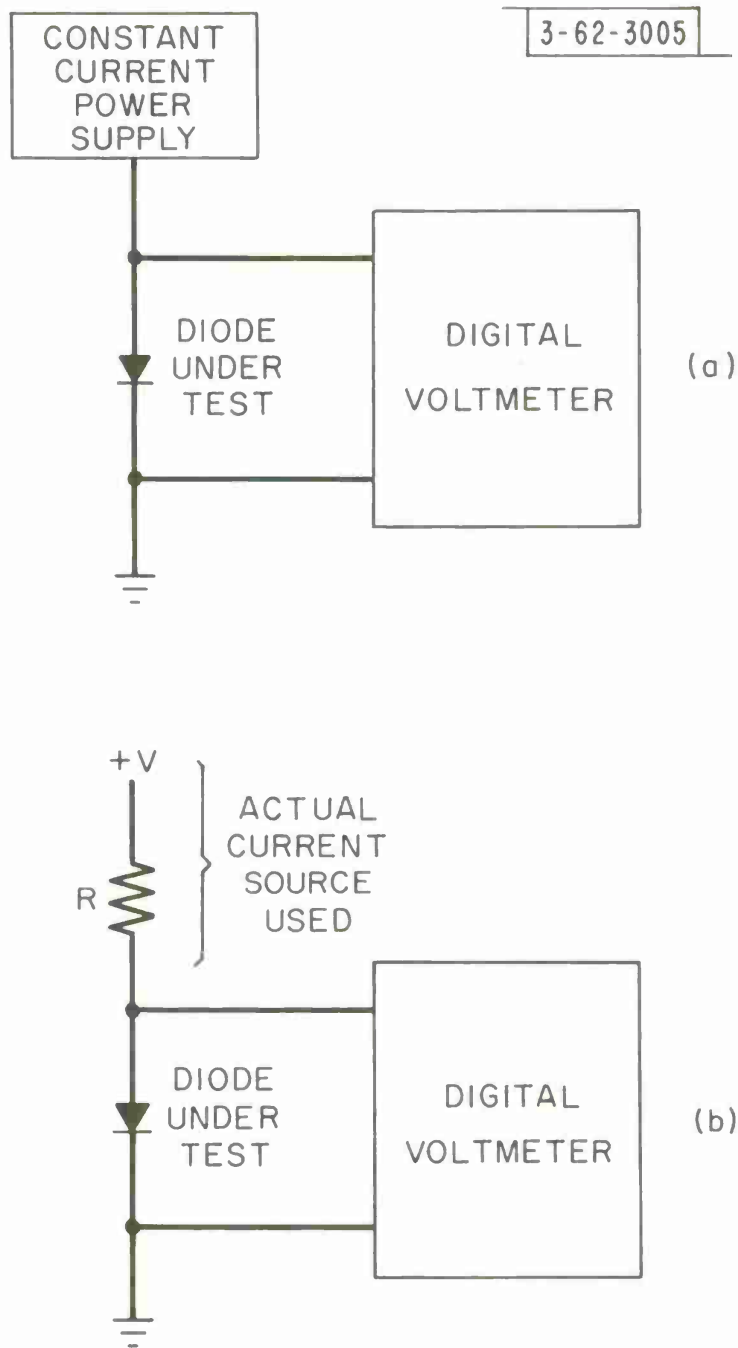


Fig. 26. Diode voltage measurement

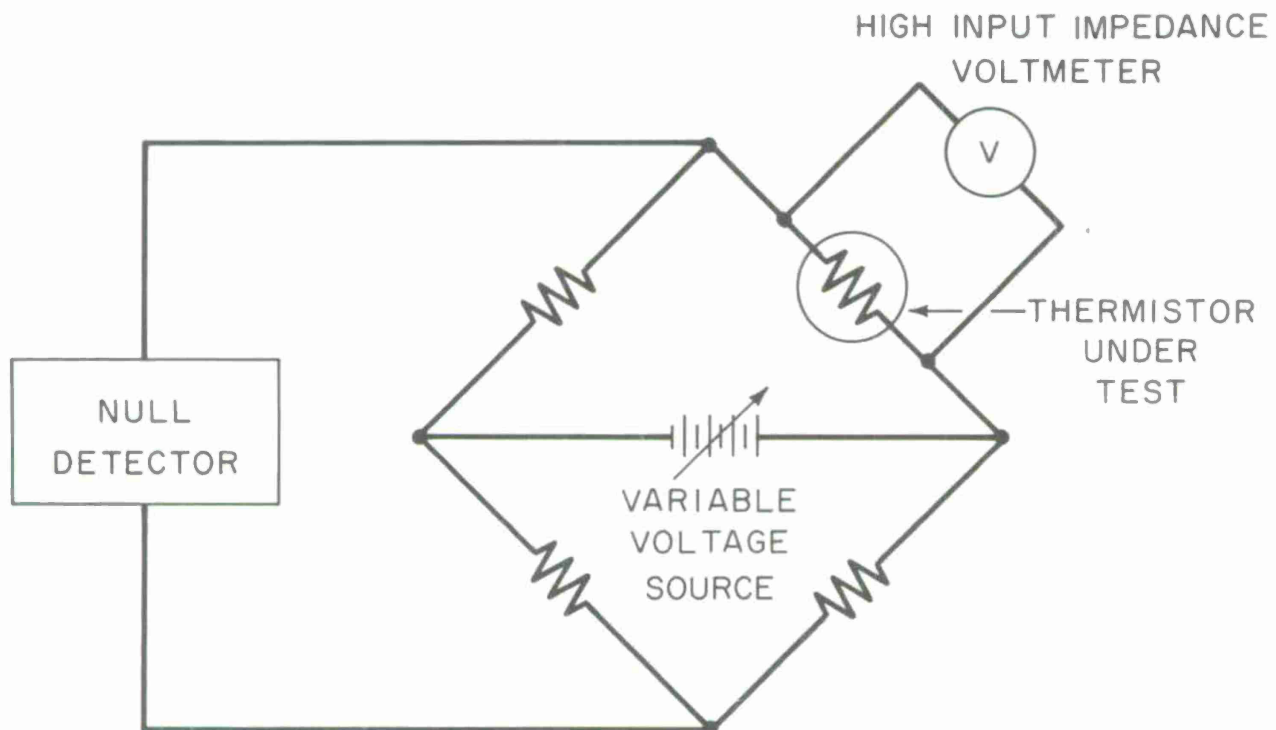


Fig. 27. Thermistor resistance measurement. The high input impedance differential voltmeter permits a measurement of the voltage across the thermistor and hence the power dissipated in the thermistor. The value of this power determines the rise in thermistor temperature due to heating as explained in the Text, IV-H-1 and VII-A-2.

3-62-2993

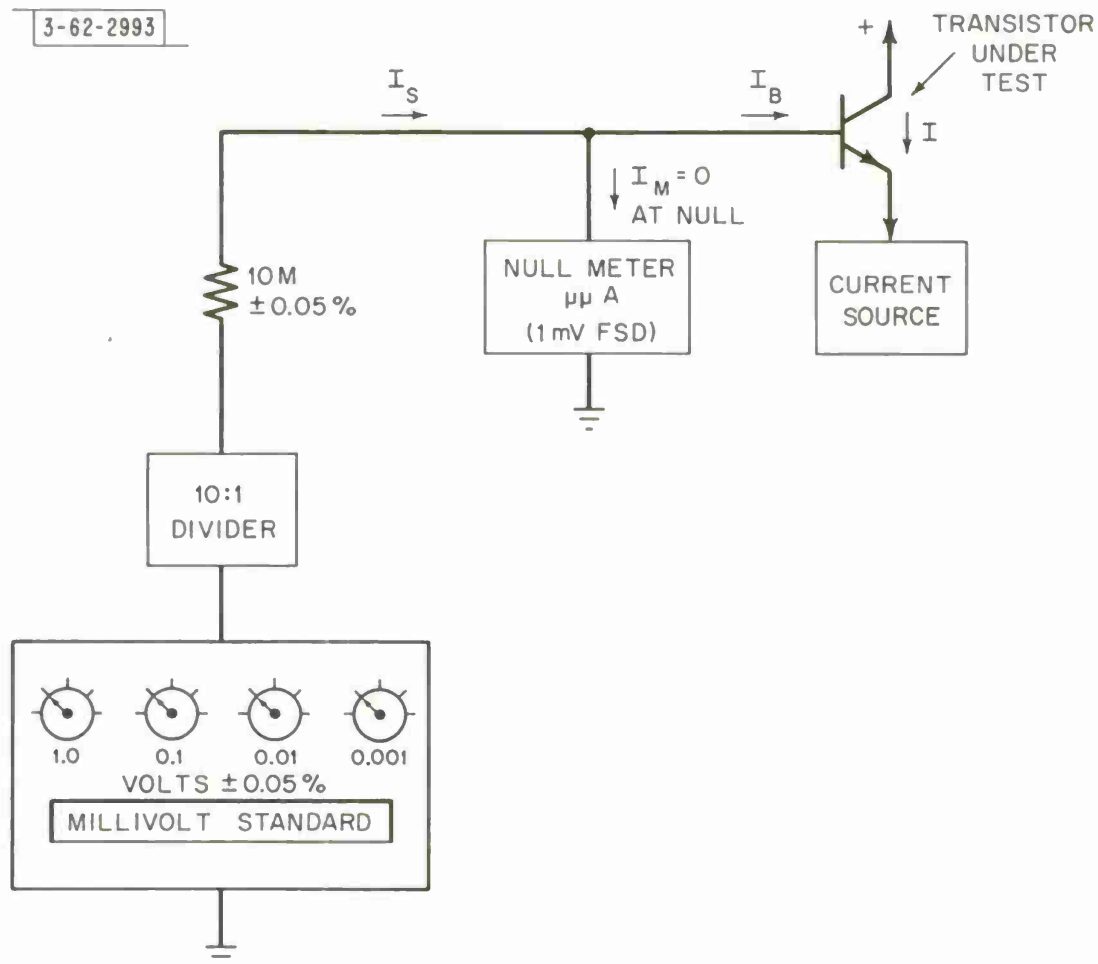


Fig. 28. Transistor base current measurement using the null technique to obtain high accuracy.

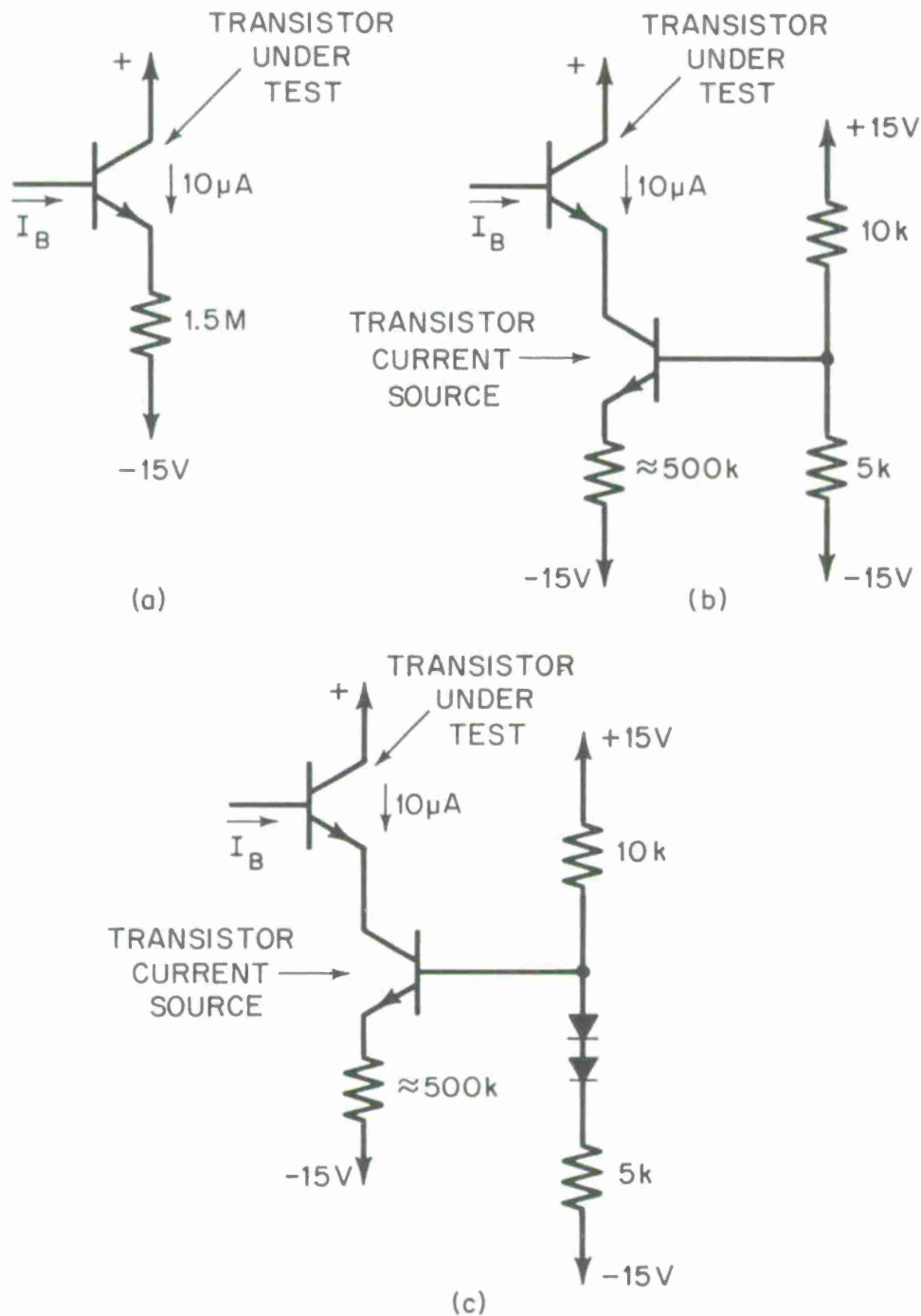
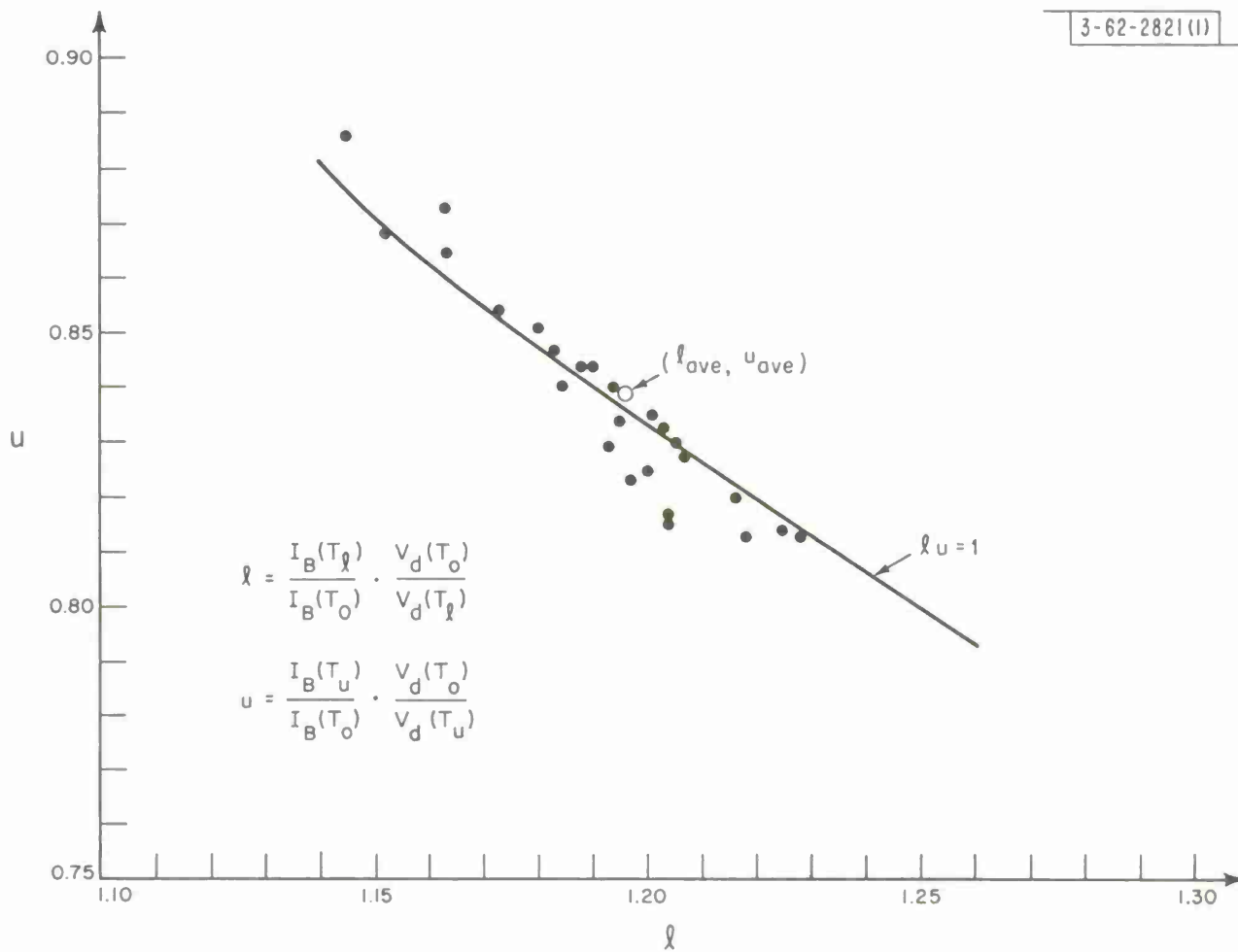


Fig. 29. Emitter current sources for the input stage. The arrangement in (c) provides temperature compensation for the V_{BE} voltage of the current source transistor, thus stabilizing the total emitter current.

Fig. 30. Scatter plot of l and u values.

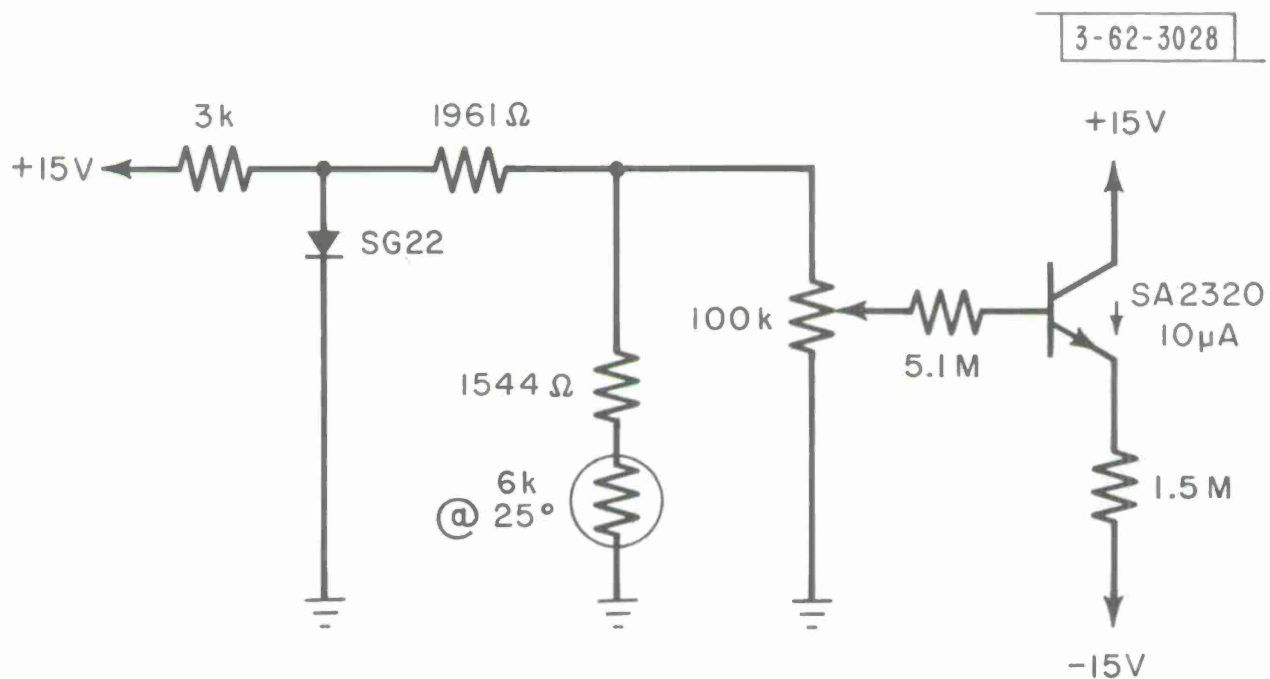


Fig. 31. Individual-Symmetrical compensation circuit. The temperature crossover points for this circuit are 20 - 40 - 60°C.

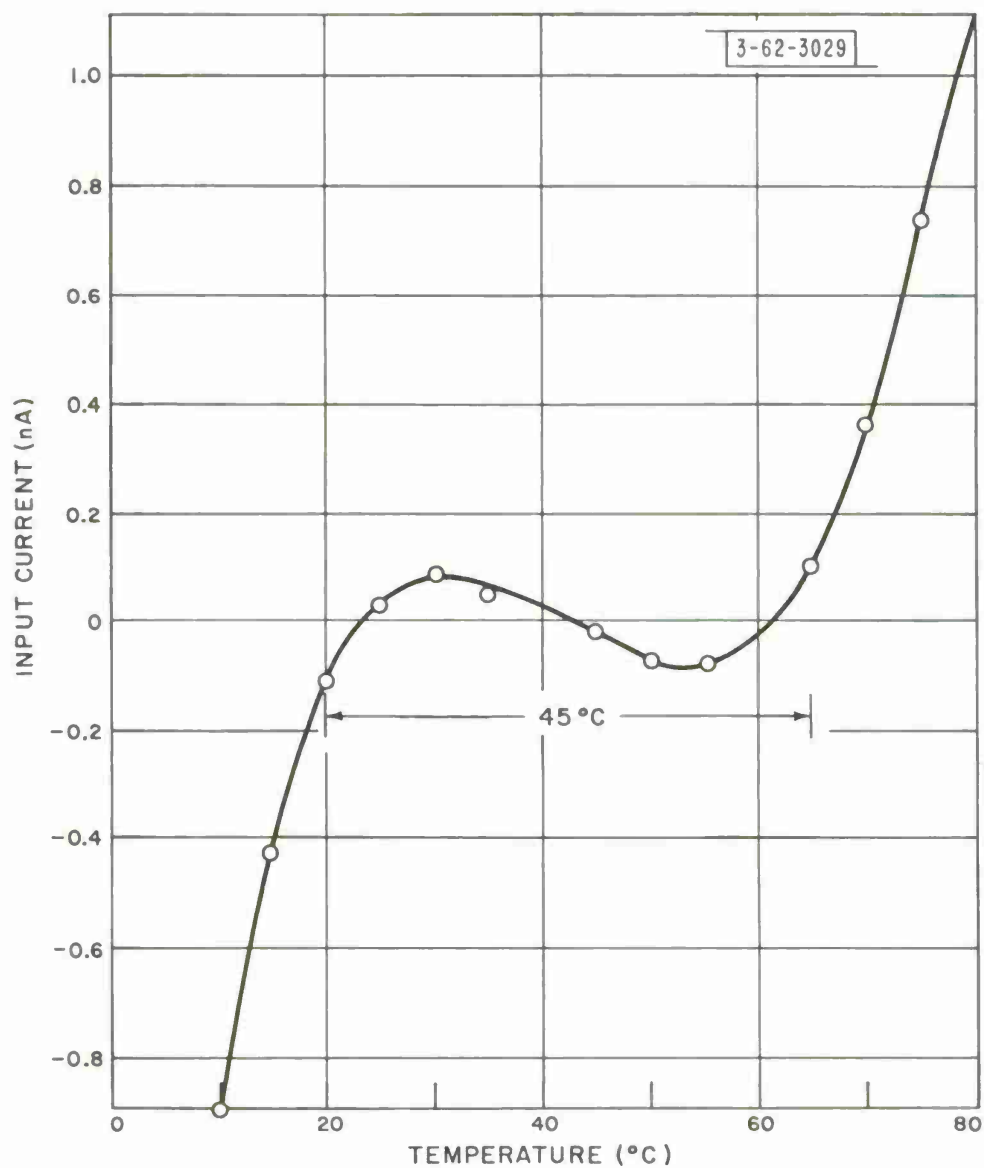


Fig. 32. Resultant input "error" current for the Individual-Symmetrical compensation circuit shown in Fig. 31.

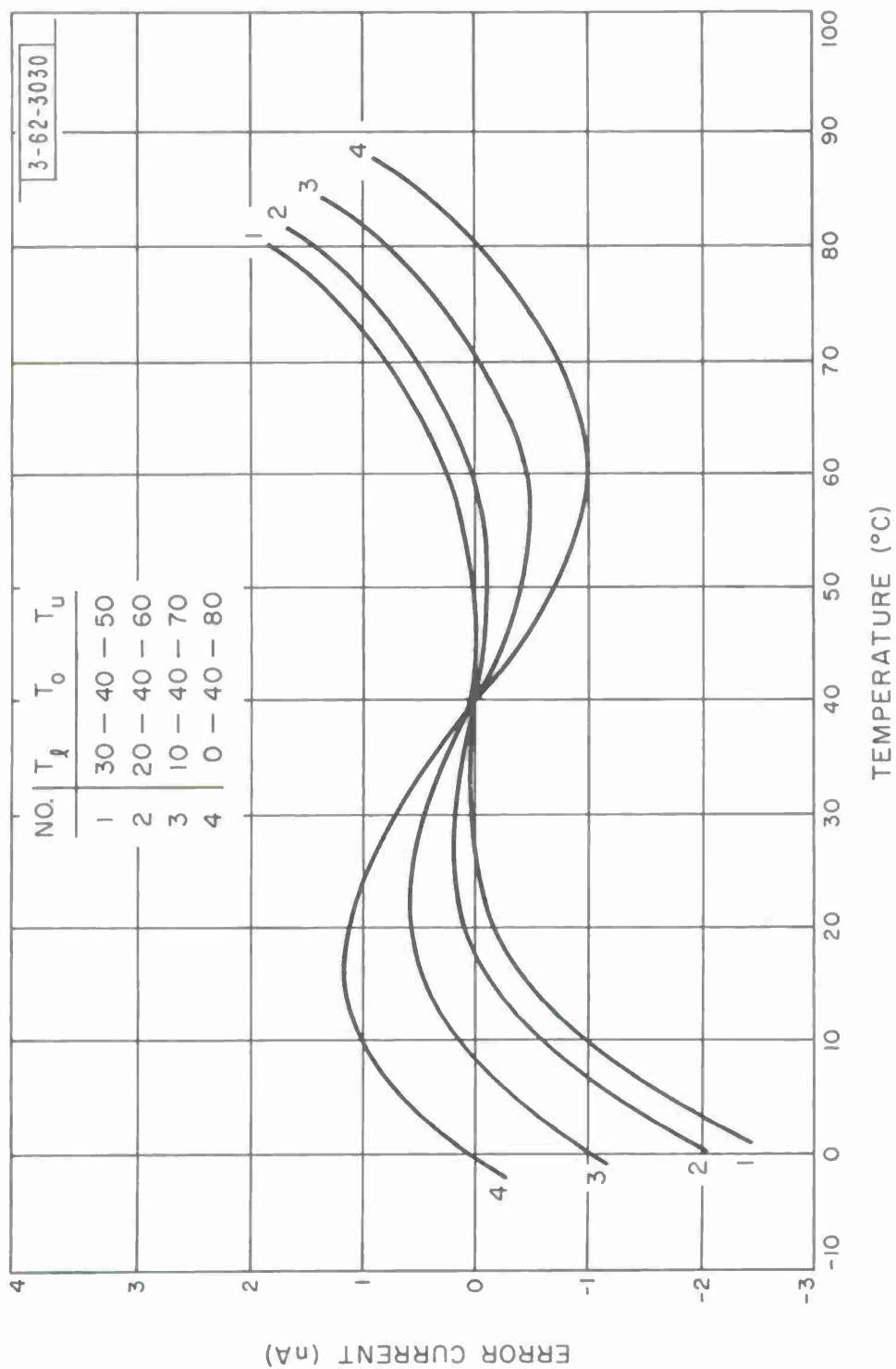


Fig. 33. Input current for Individual-Symmetrical compensation with four different temperature spans.

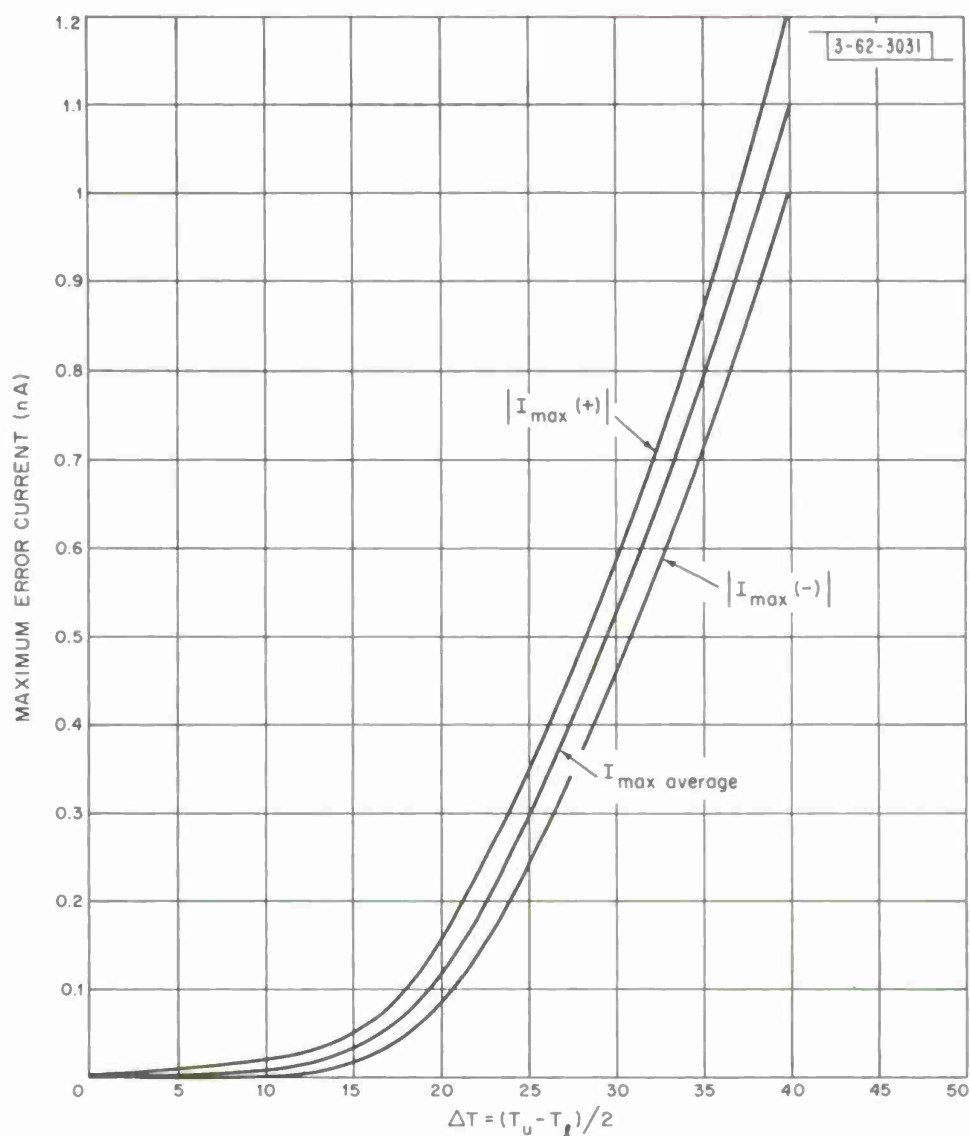


Fig. 34. Variation of the average absolute value of maximum input current vs. temperature span. This curve approximately follows the empirically derived relation $I_{\max \text{ ave}} = \frac{1}{40} (\Delta T)^{2.9}$ pA. On a point to point basis, $I_{\max \text{ ave}} \propto (\Delta T)^3$ approximately.

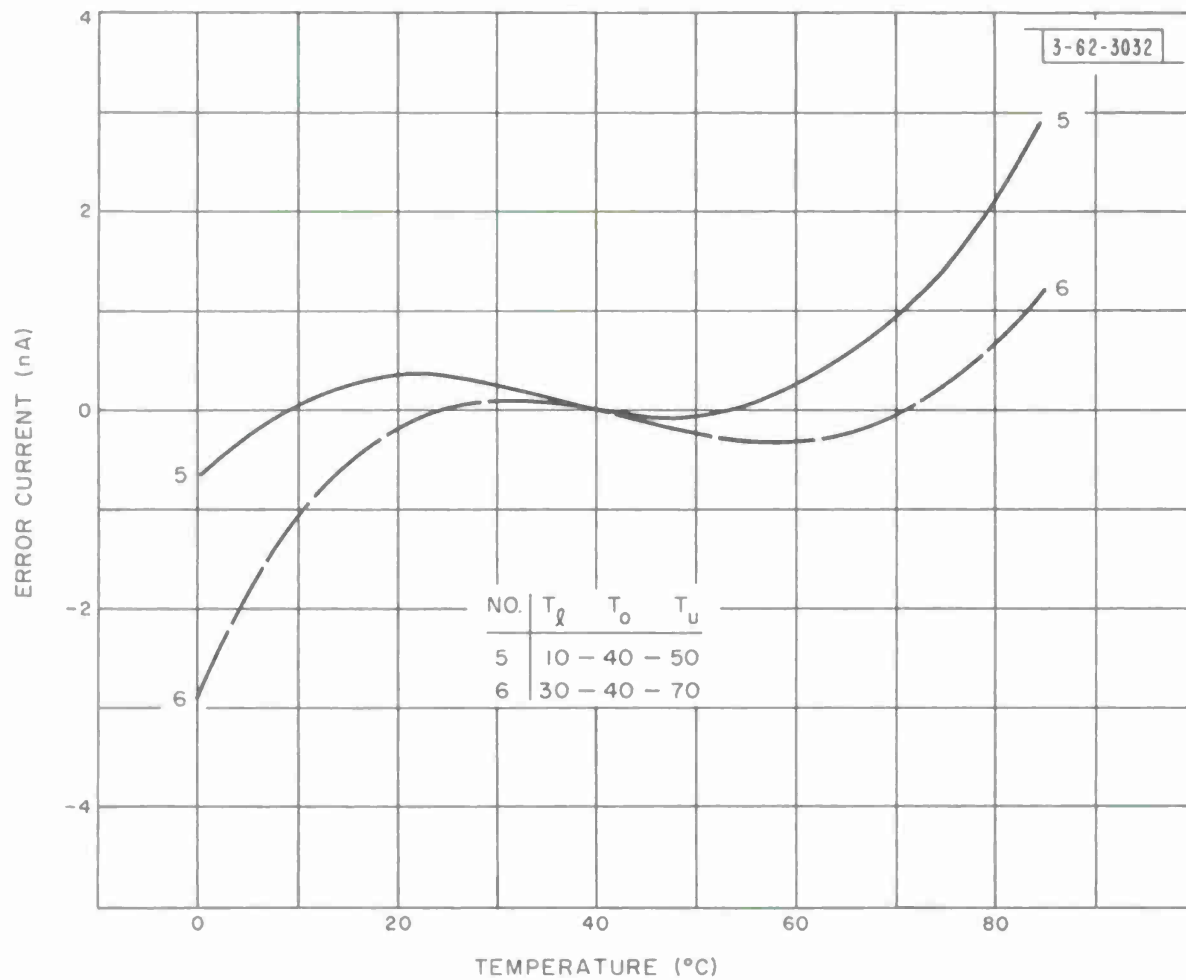


Fig. 35. Input current for Individual-Asymmetrical compensation.

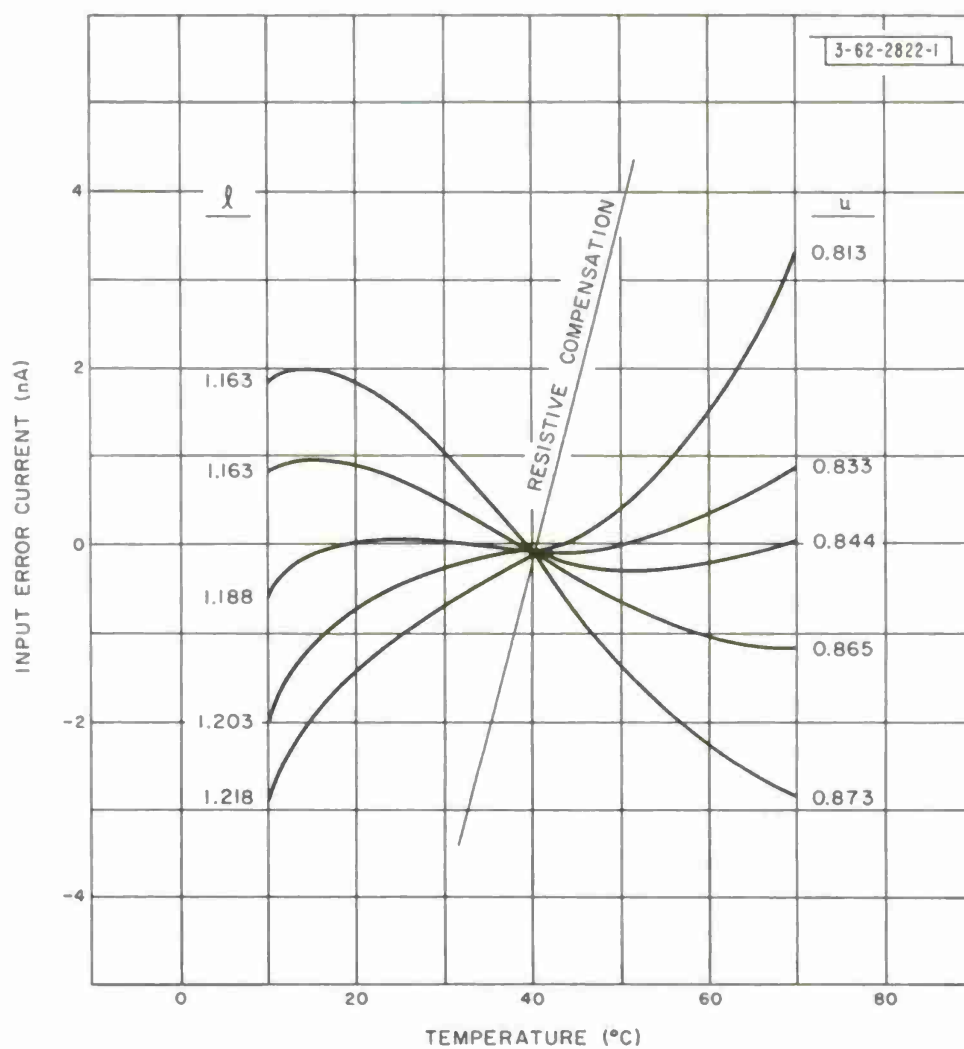


Fig. 36. Input current for Average-Symmetrical compensation curves for 4 different transistors are shown to indicate the range of possible variations.

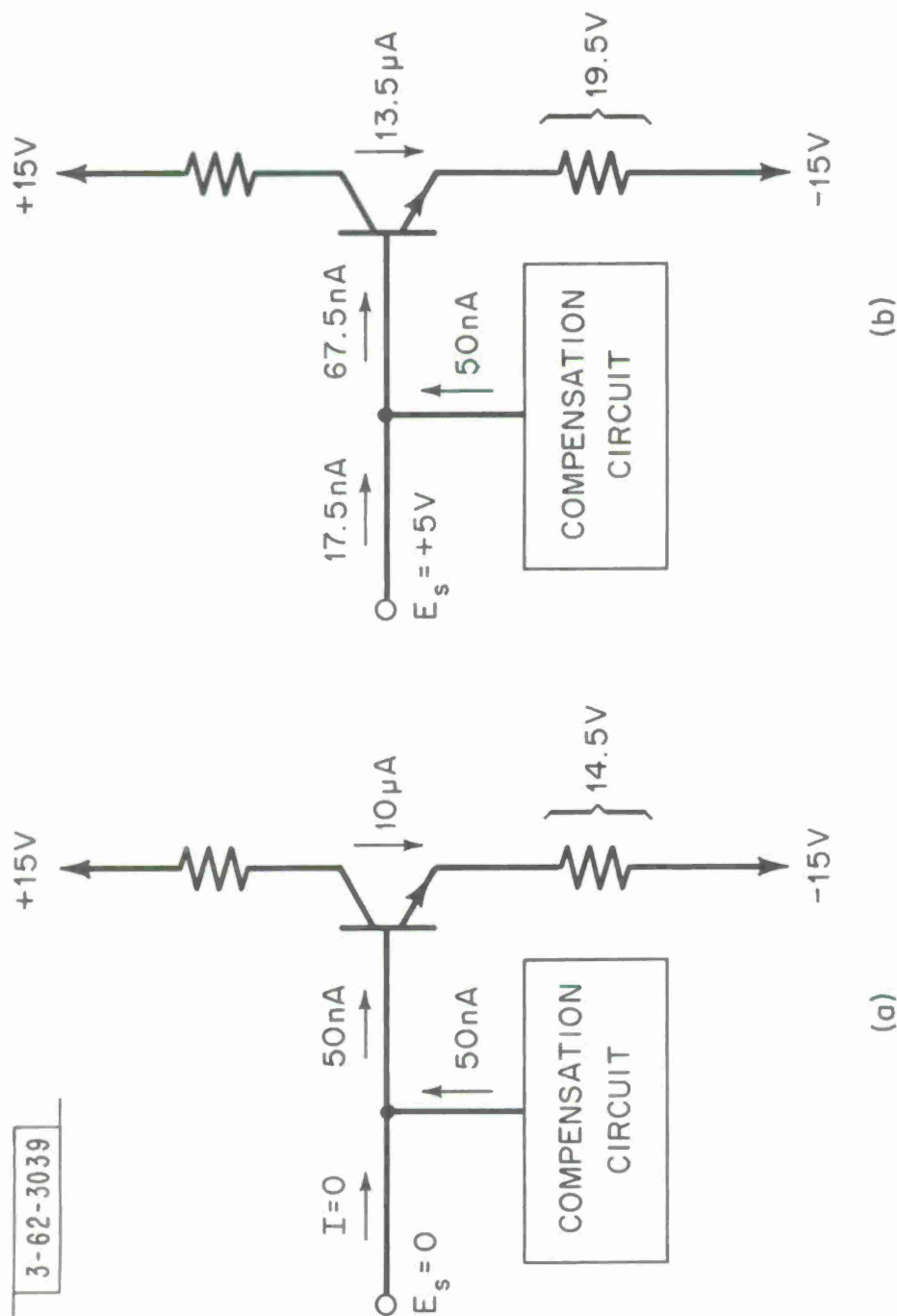


Fig. 37 (a) Resistive Emitter Current Source for voltage follower application.

(b) The same circuit showing how an input signal alters the total emitter current and hence the "error" current at the input.

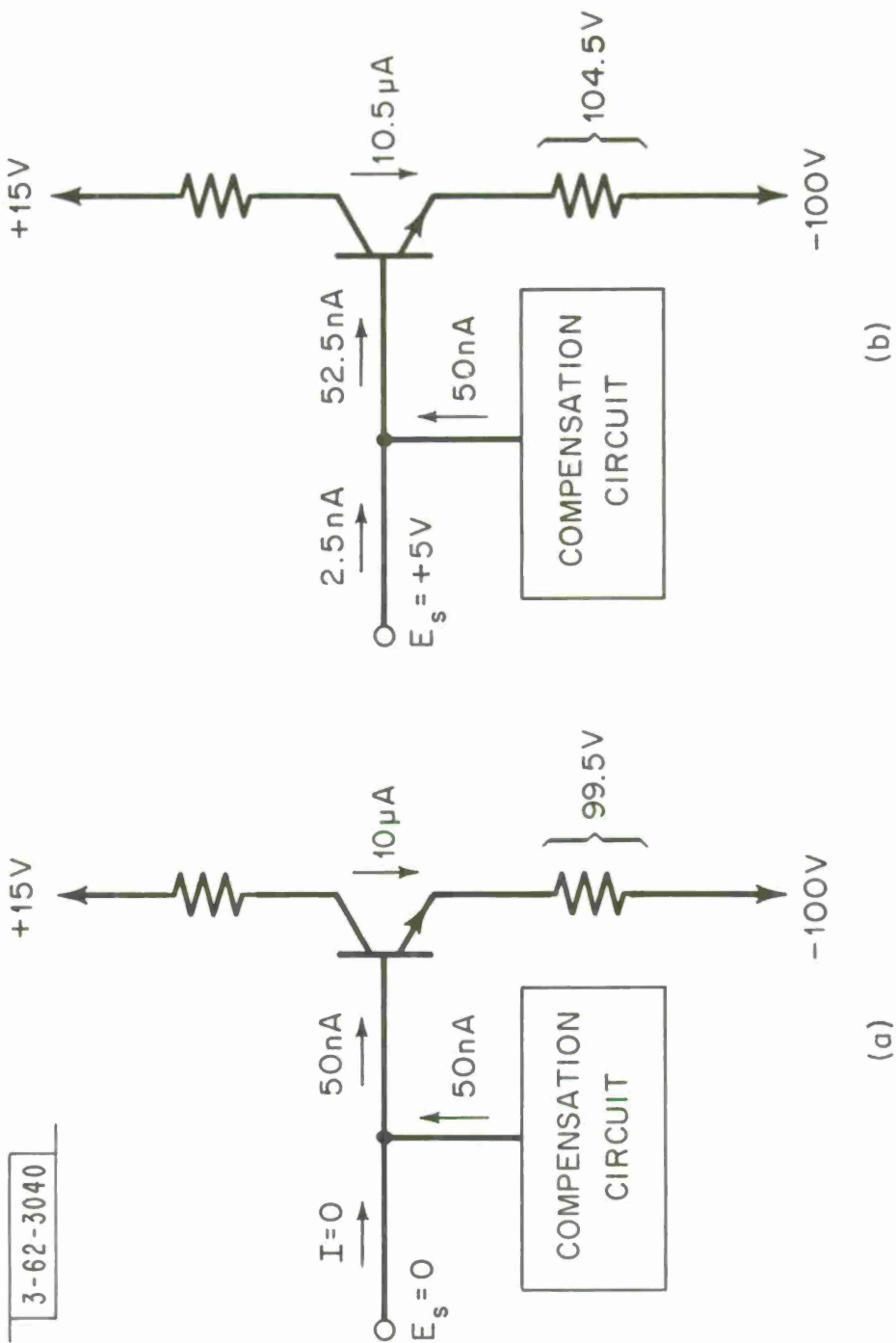


Fig. 38. Improved Resistive Emitter Current Source. Note that with the larger source voltage, the error current is substantially less than that shown in Fig. 37.

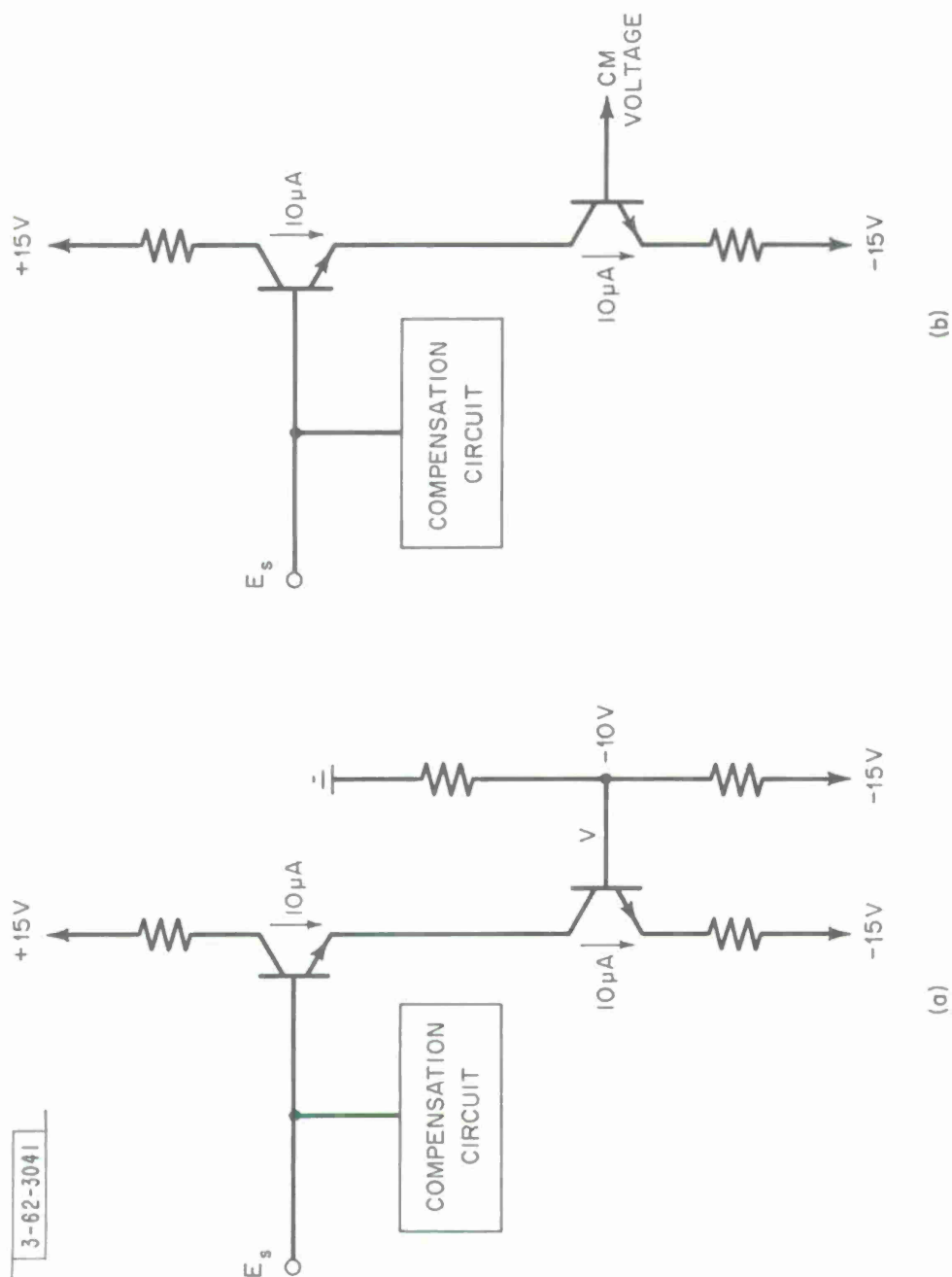


Fig. 39. Active Emitter Current Source which can give the same results as in Fig. 38, but with a lower voltage supply.

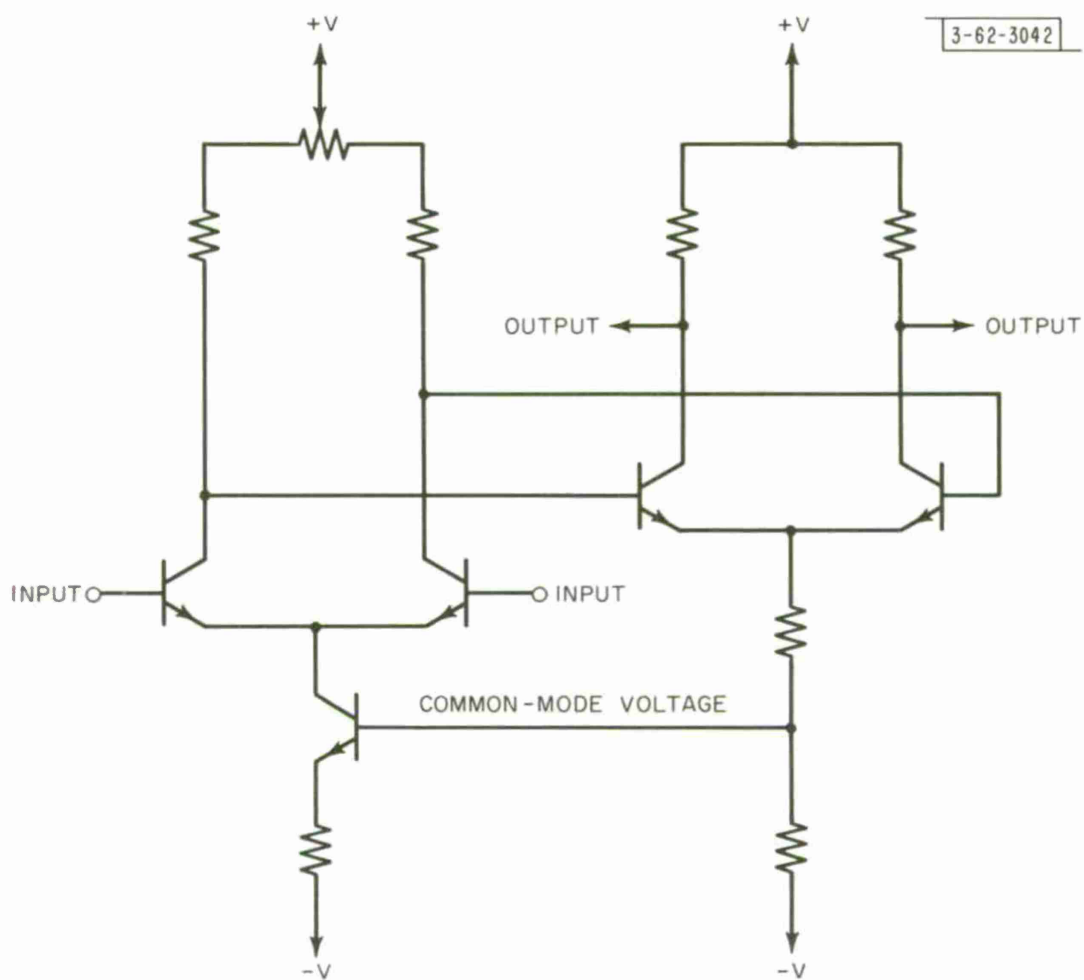


Fig. 40. Common-mode feedback Active Emitter Current Source. This circuit can give an order of magnitude improvement over the circuit in 39. With this technique, the variation of input current with signal level is virtually eliminated.

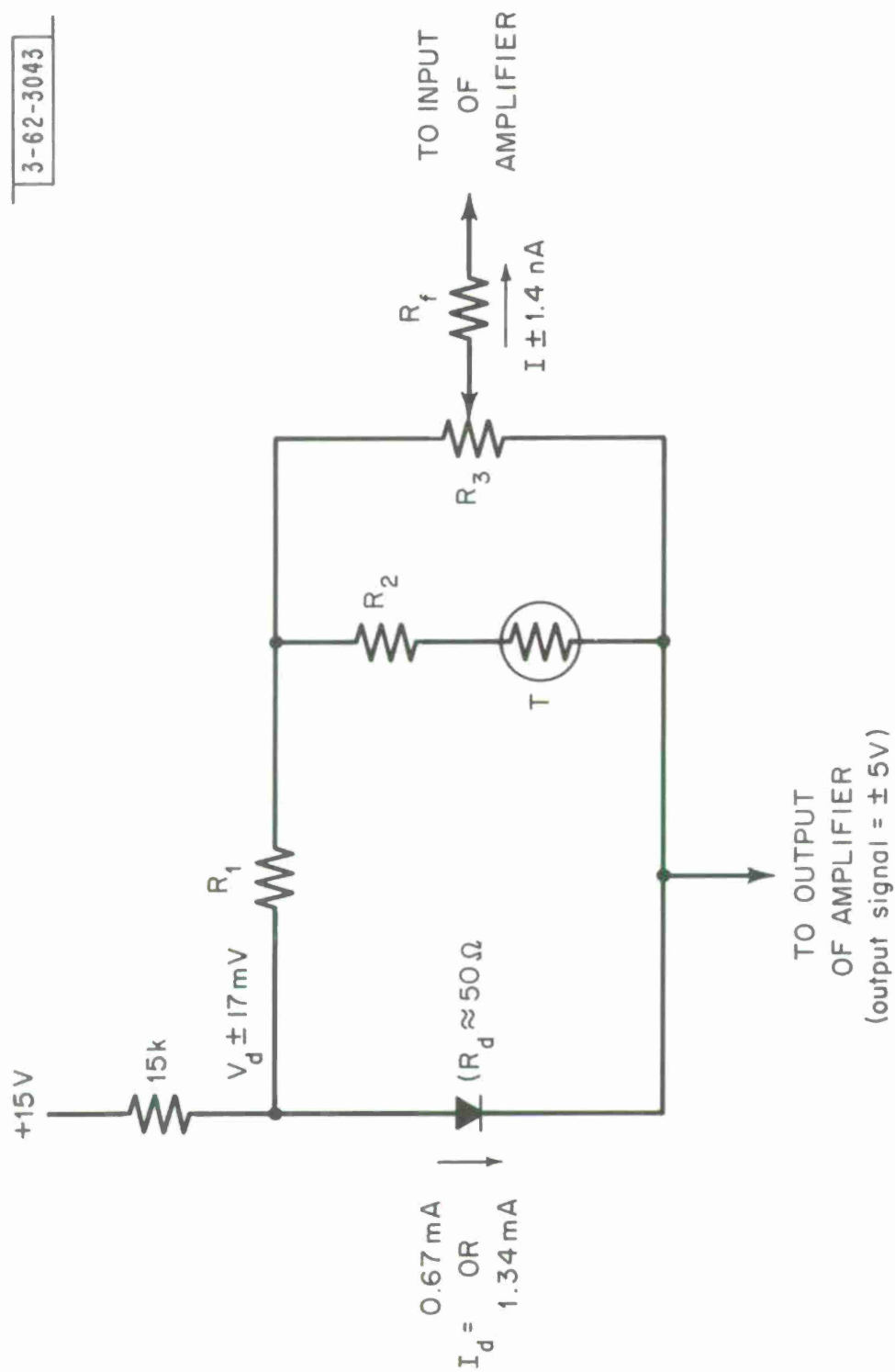


Fig. 41. Effect of input signal on the diode current in the compensation circuit. This current variation results in a variation in the driving voltage for the compensation network and hence an input error current.

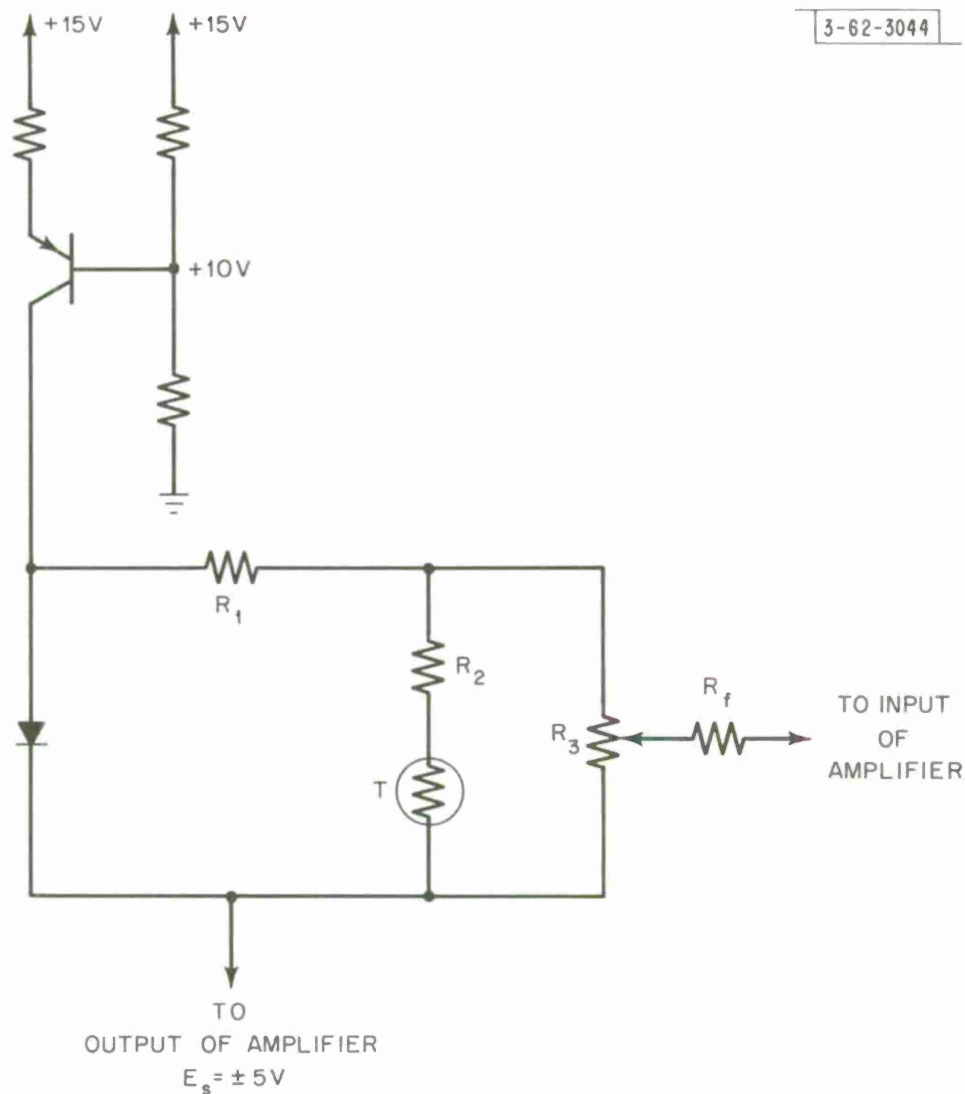


Fig. 42. Active Current Source for the diode in the compensation circuit. This technique reduces the error current to a negligible amount.

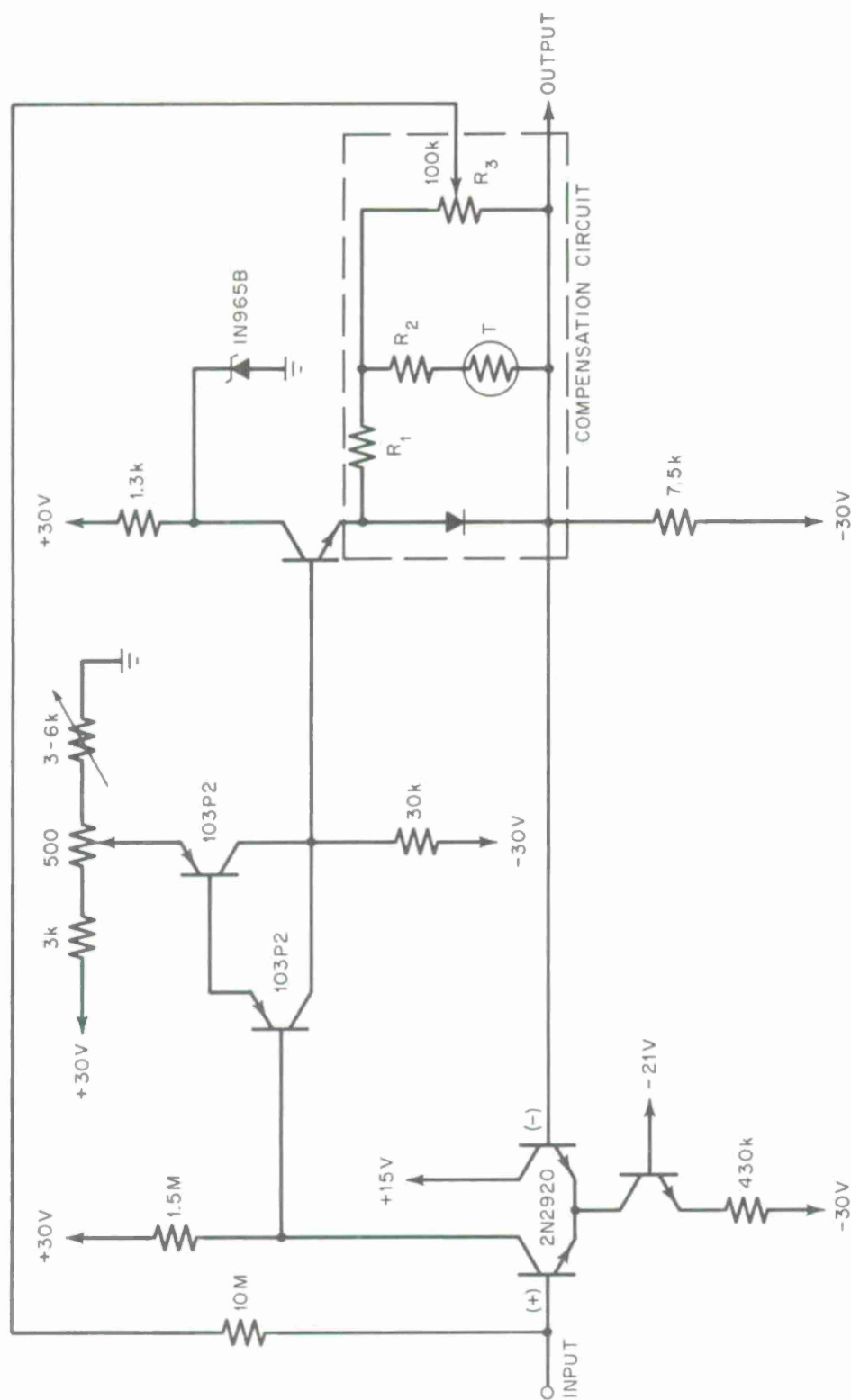
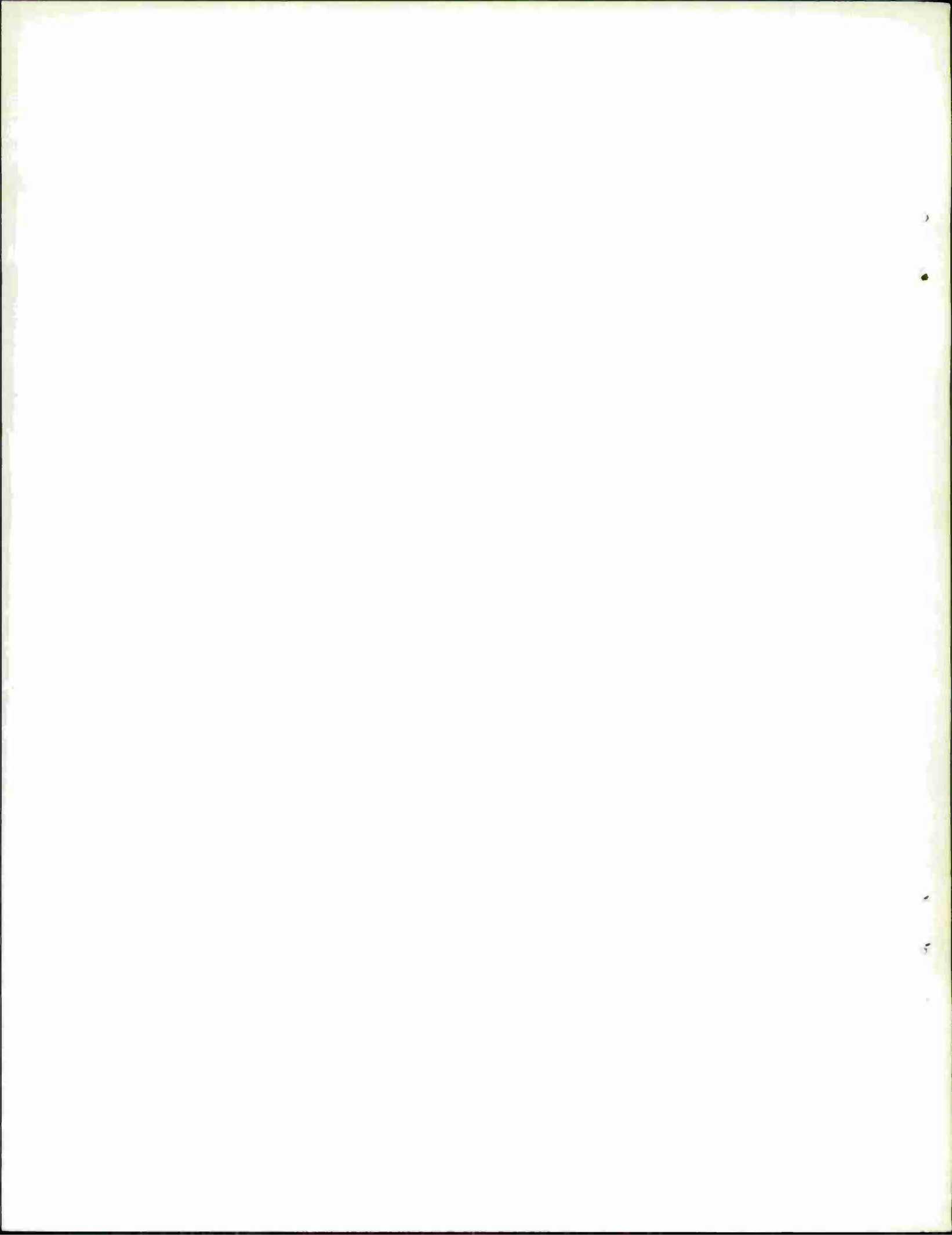


Fig. 43. An alternative compensation circuit for voltage follower application. There is no particular advantage to this circuit it is shown merely as a different approach to the problem.



DISTRIBUTION LIST

Director's Office

W. B. Davenport

AFL

N. Levine

Division 2

F. C. Frick

Group 21

P. J. Harris
R. M. Horowitz
E. J. Peters

Group 23

D. J. Eckl
K. H. Konkle

Division 3

E. F. Lyon

Group 31

J. S. Arthur
G. M. Hyde

Group 41

J. J. G. McCue

Group 42

G. R. McCully

Division 6

G. P. Dinneen
S. Gould
W. E. Morrow

Group 62

E. J. Aho
J. H. Atchison
R. L. Bernier
J. W. Craig
N. L. Daggett
A. F. Dockrey
J. J. Drobot
P. R. Drouilhet
P. R. Gendron
T. E. Gunnison
L. F. Hallowell
J. N. Harris (6)
D. A. Hunt
B. H. Hutchinson
D. Karp
I. L. Lebow
A. H. Levasseur
R. V. Locke
R. W. MacKnight
P. G. McHugh
N. J. Morrisson
B. E. Nichols
A. W. Olson
A. C. Parker
F. G. Popp
C. M. Rader
C. A. Reveal
P. Rosen
S. B. Russell
R. J. Saliga
T. Sarantos
J. F. Siemasko
R. Teoste
J. Tierney
S. R. Tringale
R. V. Wood
R. E. Zemba
Group 62 Files (10)

Group 63

R. S. Berg
B. Howland
R. M. Lerner
W. F. McBride
R. E. McMahon
W. G. Schmidt

Group 64

P. L. Fleck
P. E. Green
C. A. Wagner

Richard S. Orr (6)
Sanders Associates, Inc.
New Crosby Road
Bedford, Massachusetts

Kenneth Perry
Geodyne Corporation
151 Bear Hill Road
Waltham, Massachusetts

MIT, Cambridge

Professor Richard B. Adler
D. S. Arnstein
R. H. Baker
Professor Paul E. Gray
Professor Irwin Jacobs
Dr. Jerome Y. Lettvin
Professor Robert P. Rafuse
Professor Campbell L. Searle
Professor Richard D. Thronton
Professor John M. Wozencraft

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)

Lincoln Labs.,
Lexington, Massachusetts

2a. REPORT SECURITY CLASSIFICATION

2b. GROUP Unclassified

n/a

3. REPORT TITLE

Input Current Compensation for Transistor Operational Amplifiers

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Group Report

5. AUTHOR(S) (Last name, first name, initial)

Harris, J.N.
Orr, R.S.

6. REPORT DATE

Oct 64

7a. TOTAL NO. OF PAGES

128

7b. NO. OF REFS

0

8a. CONTRACT OR GRANT NO.

b. AF19(628)500

9a. ORIGINATOR'S REPORT NUMBER(S)

GR-1964-31

9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

ESD-TDR-64-568

10. AVAILABILITY/LIMITATION NOTICES

Qualified Requesters May Obtain from DDC.
Aval from OTS.

11. SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY

ESD, L.G. Hanscom Field, Bedford, Mass.

13. ABSTRACT

The input current of transistor operational amplifiers limits their application for some uses. Several techniques are described which result in a substantial reduction of this input current. The resulting input current can range from 20% of the original current over a wide temperature span. The percentage reduction depends on the degree of complexity and precision of the compensating circuit used. One type of compensation uses a thermistor-resistor circuit. This technique is developed in detail both analytically and experimentally, and various examples are given. For the case of a transistor having an input current of 50 nA, it is possible to design circuits to reduce this value to as little as 0.5 nA over a 50°C temperature span.

14.

KEY WORDS

Amplifiers
Transistors
Direct Coupling
Stabilization
Input Current
Temperature
Design

LINK A

LINK B

LINK C

ROLE

WT

ROLE

WT

ROLE

WT

INSTRUCTIONS

1. ORIGINATING ACTIVITY: Enter the name and address of the contractor, subcontractor, grantee, Department of Defense activity or other organization (*corporate author*) issuing the report.

2a. REPORT SECURITY CLASSIFICATION: Enter the overall security classification of the report. Indicate whether "Restricted Data" is included. Marking is to be in accordance with appropriate security regulations.

2b. GROUP: Automatic downgrading is specified in DoD Directive 5200.10 and Armed Forces Industrial Manual. Enter the group number. Also, when applicable, show that optional markings have been used for Group 3 and Group 4 as authorized.

3. REPORT TITLE: Enter the complete report title in all capital letters. Titles in all cases should be unclassified. If a meaningful title cannot be selected without classification, show title classification in all capitals in parenthesis immediately following the title.

4. DESCRIPTIVE NOTES: If appropriate, enter the type of report, e.g., interim, progress, summary, annual, or final. Give the inclusive dates when a specific reporting period is covered.

5. AUTHOR(S): Enter the name(s) of author(s) as shown on or in the report. Enter last name, first name, middle initial. If military, show rank and branch of service. The name of the principal author is an absolute minimum requirement.

6. REPORT DATE: Enter the date of the report as day, month, year; or month, year. If more than one date appears on the report, use date of publication.

7a. TOTAL NUMBER OF PAGES: The total page count should follow normal pagination procedures, i.e., enter the number of pages containing information.

7b. NUMBER OF REFERENCES: Enter the total number of references cited in the report.

8a. CONTRACT OR GRANT NUMBER: If appropriate, enter the applicable number of the contract or grant under which the report was written.

8b, 8c, & 8d. PROJECT NUMBER: Enter the appropriate military department identification, such as project number, subproject number, system numbers, task number, etc.

9a. ORIGINATOR'S REPORT NUMBER(S): Enter the official report number by which the document will be identified and controlled by the originating activity. This number must be unique to this report.

9b. OTHER REPORT NUMBER(S): If the report has been assigned any other report numbers (*either by the originator or by the sponsor*), also enter this number(s).

10. AVAILABILITY/LIMITATION NOTICES: Enter any limitations on further dissemination of the report, other than those

imposed by security classification, using standard statements such as:

- (1) "Qualified requesters may obtain copies of this report from DDC."
- (2) "Foreign announcement and dissemination of this report by DDC is not authorized."
- (3) "U. S. Government agencies may obtain copies of this report directly from DDC. Other qualified DDC users shall request through _____."
- (4) "U. S. military agencies may obtain copies of this report directly from DDC. Other qualified users shall request through _____."
- (5) "All distribution of this report is controlled. Qualified DDC users shall request through _____."

If the report has been furnished to the Office of Technical Services, Department of Commerce, for sale to the public, indicate this fact and enter the price, if known.

11. SUPPLEMENTARY NOTES: Use for additional explanatory notes.

12. SPONSORING MILITARY ACTIVITY: Enter the name of the departmental project office or laboratory sponsoring (*paying for*) the research and development. Include address.

13. ABSTRACT: Enter an abstract giving a brief and factual summary of the document indicative of the report, even though it may also appear elsewhere in the body of the technical report. If additional space is required, a continuation sheet shall be attached.

It is highly desirable that the abstract of classified reports be unclassified. Each paragraph of the abstract shall end with an indication of the military security classification of the information in the paragraph, represented as (TS), (S), (C), or (U).

There is no limitation on the length of the abstract. However, the suggested length is from 150 to 225 words.

14. KEY WORDS: Key words are technically meaningful terms or short phrases that characterize a report and may be used as index entries for cataloging the report. Key words must be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location, may be used as key words but will be followed by an indication of technical context. The assignment of links, rules, and weights is optional.

Printed by
United States Air Force
L. G. Hanscom Field
Bedford, Massachusetts