TR-1271

CIRCUIT REALIZATION OF A SQUARE ROOT SUM OF SQUARES COMPUTER

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25 January 1965

U.S. ARMY MATERIEL COMMAND

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ABSTRACT

An electronic system has been developed to compute the square root of the sum of the squares for three input variables. The basic technique is to use a conventional triaxial accelerometer and to process the three input signals, giving as an output one waveform. This report covers specifically the design and evaluation of circuitry that (1) accepts input signals from the accelerometers during impact, and (2) computes an instantaneous magnitude of the acceleration-time curve continuously.

The circuitry has been determined operable over a dynamic range of 4 mv to 4 v, with a frequency response of 4 to over 4000 cps. A computational accuracy of within 5 percent has also been proved between 50 mv and 4 v; an accuracy to within 10 percent has been proved from 4 to 50 mv.

1. INTRODUCTION

A program was initiated[1] during June 1963 to investigate various techniques for realizing an omnidirectional accelerometer, and to determine the one most applicable for a NASA (Langley) experiment to characterize surface characteristics of remote, atmosphereless places such as the earth's moon.

When this program began, no effective technique had been developed to orient a unidirectional conventional accelerometer in a vacuum, nor had there been an omnidirectional responding accelerometer developed. Thus, several electronic and mechanical approaches were investigated, based on the accelerometer being required to:

(a) Display a single output voltage-time waveform to describe the impact;

(b) Operate at 20 v at low current—about 10 ma, from 40 to 40,000 g between approximately 4 and 4000 cps; and

(c) Fit into a ball 3 in. in diameter and include about 5 cu in. of telemetry, batteries, and antenna.

This report describes the electronic approach considered adequate for the application. The basic technique here is to use a conventional triaxial accelerometer and to process the three input signals, giving as an output one waveform.

$$\text{Output} = K\sqrt{X^2+Y^2+Z^2}$$

[1] Authorized by Defense Purchase Request L-31,945.

Subsequent reports will be issued describing the mechanical approaches considered applicable.

2. DESIGN CONSIDERATIONS

The basic problem in designing the computer was to find a computation technique that would be usable over the three-decade range of 40 to 40,000 g. Once squared, the variables would have a dynamic range of 10^6. No conventional squaring circuits were found capable of operating over this range. The technique presented here is based on several methods investigated, approximating the root sum and employing passive systems (ref 1,2). The basic computation is accomplished by a passive resistor matrix capable of computing

$$A = K\sqrt{X^2+Y^2}$$

A is then scaled to A/K and then combined with Z, so that the output is

$$B = K\sqrt{Z^2+A^2/K^2}$$

$$B = K\sqrt{X^2+Y^2+Z^2}$$

Briefly, the computer is a linear piecewise network capable of performing the computation. Some discussion of this technique is included in section 4.3. References 1 and 2 present a more detailed description of this circuit.

Voltages of 4 mv to 4 v have to be processed by the circuits because of the large dynamic range of the accelerometer. The passive resistor computer has two circuit requirements which, together with the 4-mv to 4-v signal strength, poses a formidable electronic problem. First, the resistor computer requires positive inputs. Since each axis of the triaxial accelerometer is a simple uniaxial accelerometer capable of both positive and negative pulses—depending upon the direction of impact—the outputs of each accelerometer have to be rectified. This means rectification of signals from 4 mv to 4 v.

The second problem results because the resistor computer puts out three signals at three different points, the highest voltage being the correct answer. A circuit was therefore required to select the highest output from three inputs. Since millivolt and volt signals had to be processed, no diodes could be used because of their high offset voltages.

3. GENERAL DESCRIPTION OF SYSTEM DESIGN

The primary purpose of the electronic circuitry is to compute the magnitude of the shock experienced by the triaxial accelerometer during impact. Thus, it is required to compute

$$K \sqrt{X^2+Y^2+Z^2}$$

where X, Y, and Z are the three orthogonal outputs of the triaxial accelerometer.

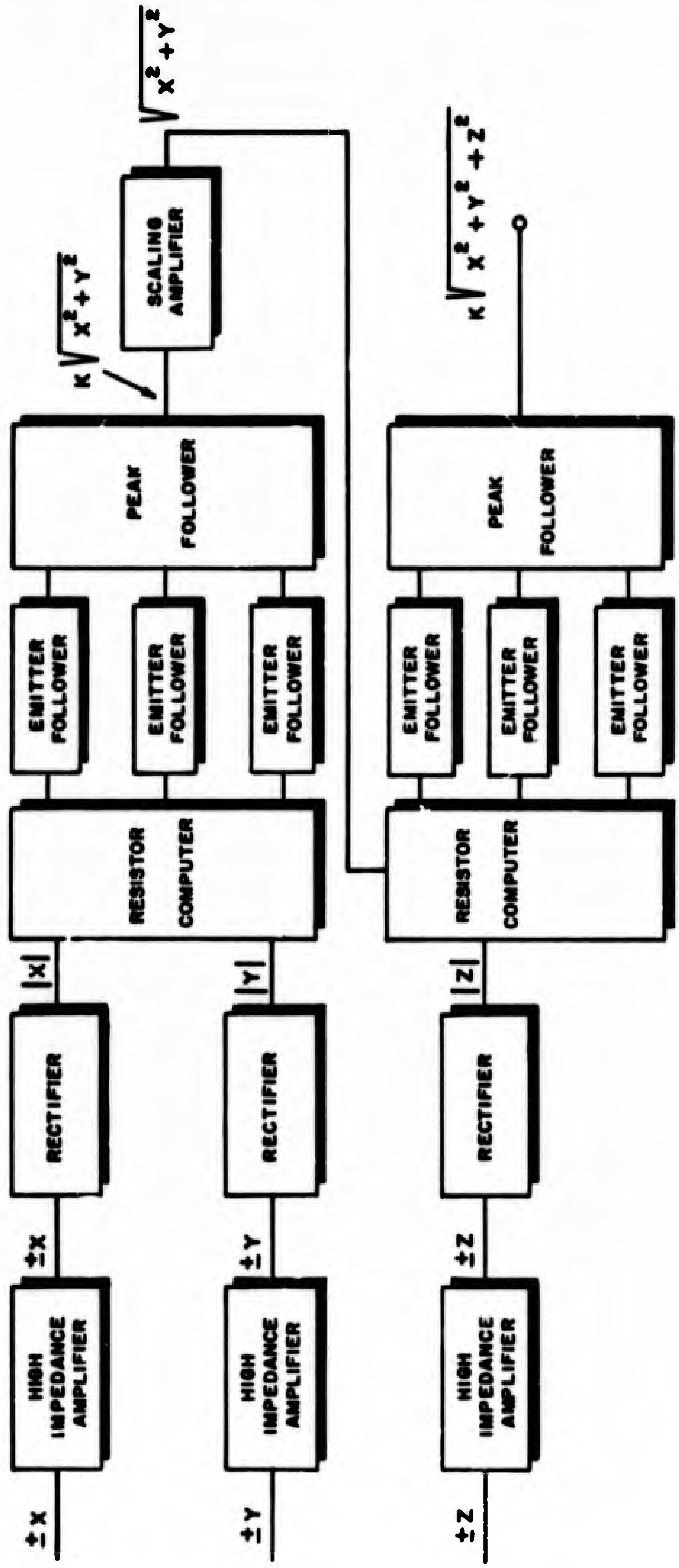
An SRSS (square root of the sum of the squares) circuit was found in the literature (ref 1). The circuit, consisting only of resistors, will be hereinafter referred to as the resistor computer. No power supply is required for the resistor computer; it functions as a voltage divider network and, as a result, minimum power is dissipated.

The computer requires that both input signals be of the same polarity. Thus, additional circuitry is required between the outputs of the triaxial accelerometer and the resistor computer to insure that the computer receives only signals of the same polarity. Since each output of the accelerometer may be either positive or negative—depending upon the impact direction—the intermediate circuitry has the function of a rectifier. The output from the rectifier is a positive signal with the same amplitude and pulse shape as the original output signal of the accelerometer.

The rectifier circuit was designed to function over the dynamic range of 1000, 4 mv to 4 v. Within this range, the rectifier accepts the signal (positive or negative) from a low-output impedance source and provides the resistor computer with the absolute value of the input signature of the three accelerometers.

The accelerometer, whose output is a function of the shock experienced, is a charge generator and requires a matching input impedance in the order of hundreds of megohms. With a high-matching input impedance required for the accelerometer and a low-source impedance required for the rectifier, a high-impedance amplifier with unity gain is used to match the accelerometer output to the rectifier input. This amplifier is biased so that either a positive or negative output from the accelerometer is reproduced. The amplifier output is then fed into the rectifier.

Figure 1 shows block and schematic diagrams of the circuitry required to follow the largest of the three positive output voltages given by the resistor computer. Since the largest voltage represents the correct answer, the three-input peak follower was designed to follow this output. The emitter followers shown between the computer and peak follower are for impedance matching. Most of the circuitry is required to process the input signals into information that the resistor computer can use. The system is therefore designed around the resistor computer.


±X
HIGH IMPEDANCE AMPLIFIER
±X
RECTIFIER
|X|
±Y
HIGH IMPEDANCE AMPLIFIER
±Y
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±Z
HIGH IMPEDANCE AMPLIFIER
±Z
RECTIFIER
|Z|
RESISTOR COMPUTER
EMITTER FOLLOWER
EMITTER FOLLOWER
EMITTER FOLLOWER
PEAK FOLLOWER
$K\sqrt{X^2+Y^2}$
SCALING AMPLIFIER
$\sqrt{X^2+Y^2}$
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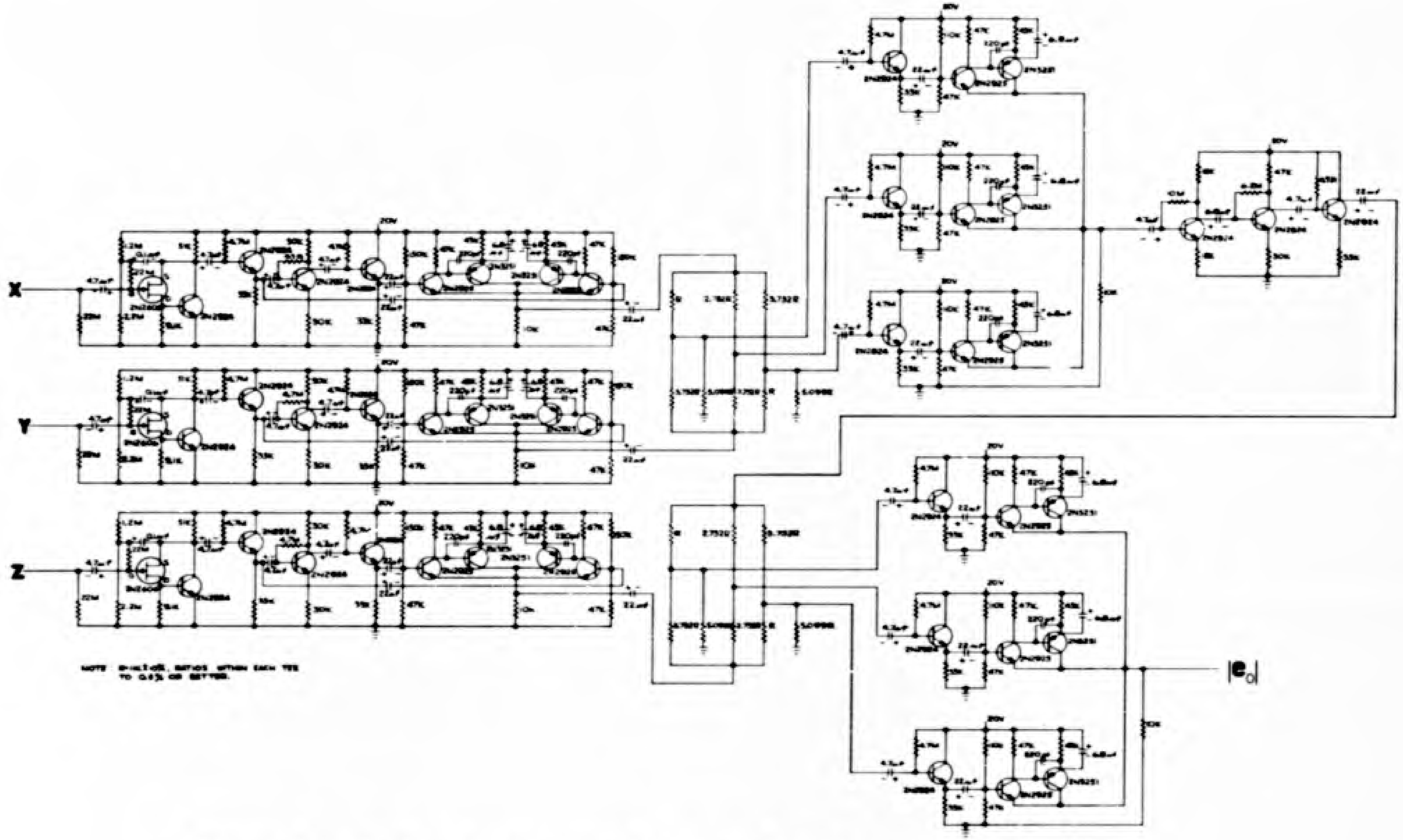


Figure 1. Block and schematic diagrams of SRSS computer system.

The X and Y channels (fig. 1) are fed into one resistor computer from which $K\sqrt{X^2+Y^2}$ is given as an output. This output is then scaled to its proper value and fed with the Z channel into the second resistor computer, which gives the final output of $K\sqrt{X^2+Y^2+Z^2}$.

For the complete system, the voltage and current requirements are 20 v and 9.6 ma respectively. Listed below are the components and individual circuits required for the complete system.

No. circuits per system	Individual circuits	Components per circuit		
		Transistors	Resistors	Capacitors
3	High-impedance amplifier	2	6	2
3	Rectifier	7	16	9
2	Resistor computer	-	8	2
6	Emitter follower	1	2	2
2	Peak follower	6	13	6
1	Scaling amplifier	3	8	3
(TOTALS FOR COMPLETE SYSTEM):				
17		48	128	64

4. CIRCUITRY AND DESIGN PROCEDURE

4.1 High-Impedance Amplifier

To realize a high-impedance amplifier capable of providing the best conditions for low-frequency response of the accelerometer, together with a low-output impedance, the following criteria were established for the amplifier:

(1) High input impedance
(2) Low output impedance
(3) Unity gain
(4) Frequency response 4 to 4000 cps
(5) Low quiescent current

Since the low-frequency response is related to the RC time constant of the accelerometer and its matching electronics, the required input impedance of the amplifier is dependent on the type of accelerometer selected. For the prototype model designed, a piezoelectric accelerometer was used with an average sensitivity of

10 mv/g for each axis. A sensitivity of only 0.1 mv/g was required, however. Consequently, it was necessary to decrease the output of the accelerometer by a factor of 100, which was obtained by increasing the shunting capacitance across the accelerometer. The increase in capacitance decreases the required input impedance of the amplifier proportionally to give the same RC time constant at the lowest frequency.

The low-frequency response of the amplifier is a function of the fRC product, where f is the frequency in cycles per second, R is the input impedance of the amplifier in ohms, and C is the total shunting capacitance in farads. Within the frequency domain of 4 to 4000 cps, the amplifier is required to have a response that is constant and independent of frequency changes. The fRC must be 1.0 or greater to attain a constant response.

The calculated impedance for the required 0.1-mv/g sensitivity and 4-cps frequency is 6.14 megohms. Any increase in input impedance above the 6.14 megohms, however, insures an fRC product greater than one and a correspondingly better low-frequency response.

The unity gain, high-input, low-output impedance amplifier monitors the output from one axis of the triaxial accelerometer. It is a follower, in that there is no phase reversal. A schematic diagram of this amplifier is shown in figure 2.

The amplifier is composed of a 2N2606 FET (field-effect transistor) followed by a 2N2924 NPN bipolar transistor. The FET is used because of its high-input impedance characteristics. The NPN bipolar transistor serves as a current amplifier, which supplements the FET by supplying most of the current required for the output to follow the input. The FET could supply the required current without the bipolar transistor. But during the process, the operating point would change, thereby introducing nonlinearity in the output. It is also possible that the gate to source junction could become reverse biased, which would decrease the input impedance.

In selecting the bias point for the FET, it was necessary to provide an equal swing (without clipping) for both negative and positive signals of 4 v. Equal swings were provided in either direction by placing the FET source at the center (10 v) of the supply. The drain current I_d was determined by referring to data sheets showing drain current versus gate-source voltage. For the best operating conditions, the FET drain current must be less than I_{dss}, the drain-source saturation current. A drain current corresponding to the minimum pinch-off voltage (1 v) approximates one-third I_{dss}. As plotted on 2N2606 data sheets, a gate-source voltage of 1 v will pin the drain current at 50 μa, which is well within the limits of I_{dss}. For design purposes, the FET bias point was selected as:

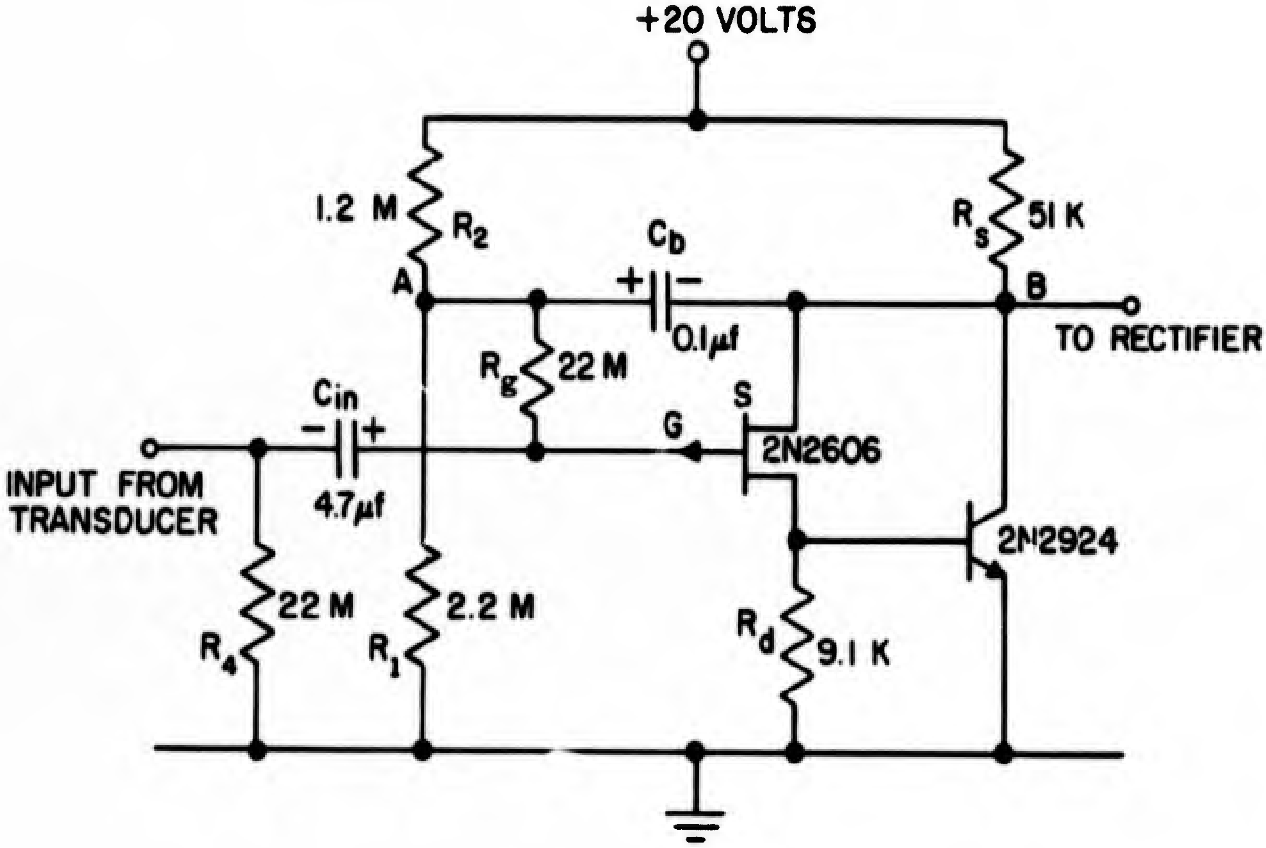


Figure 2. High-impedance amplifier, schematic diagram.

V_s = 10 v

I_d = 50 μa

The following specifications were established for the circuit components:

FET 2N2606: Bias source at center of power supply range

2N2924: Current gain, $\beta > 100$ from I_c, 40 to 225 μa

V_{be} = 0.4 to 0.5 v

Resistors: Tolerance = ±5 percent.

Summarized below are the values of the components used in the high-impedance amplifier (fig. 2). Appendix A describes the procedure followed in determining these values.

R_g = 22 megohms

R_1 and R_2 = 2.2 and 1.3 megohms, respectively; the standard values, 2.2 and 1.2 megohms, are used in the circuit.

R_d = 9 kohms; the nearest standard value, 9.1 kohms, is used in the circuit.

R_s = 50 kohms; the nearest standard value of 51 kohms is used.

R_4 = 22 megohms

4.2 Rectifier

The rectifier in each channel, which insures inputs of the same polarity to the resistor computer(described in sect 3), receives a positive or negative output from the high-impedance amplifier. It then gives the absolute magnitude of the original accelerometer signal within the dynamic range of 1000, 4 mv to 4 v. Following are the specifications established for the rectifier design:

(1) Dynamic range of 1000, 4 mv to 4 v.
(2) Frequency response of 4 to 4000 cps.
(3) Quiescent current not to exceed 1.5 ma.
(4) Low-output impedance.

The rectifier (fig. 3) consists of four stages; the first three stages form a phase splitter. Since either a positive or

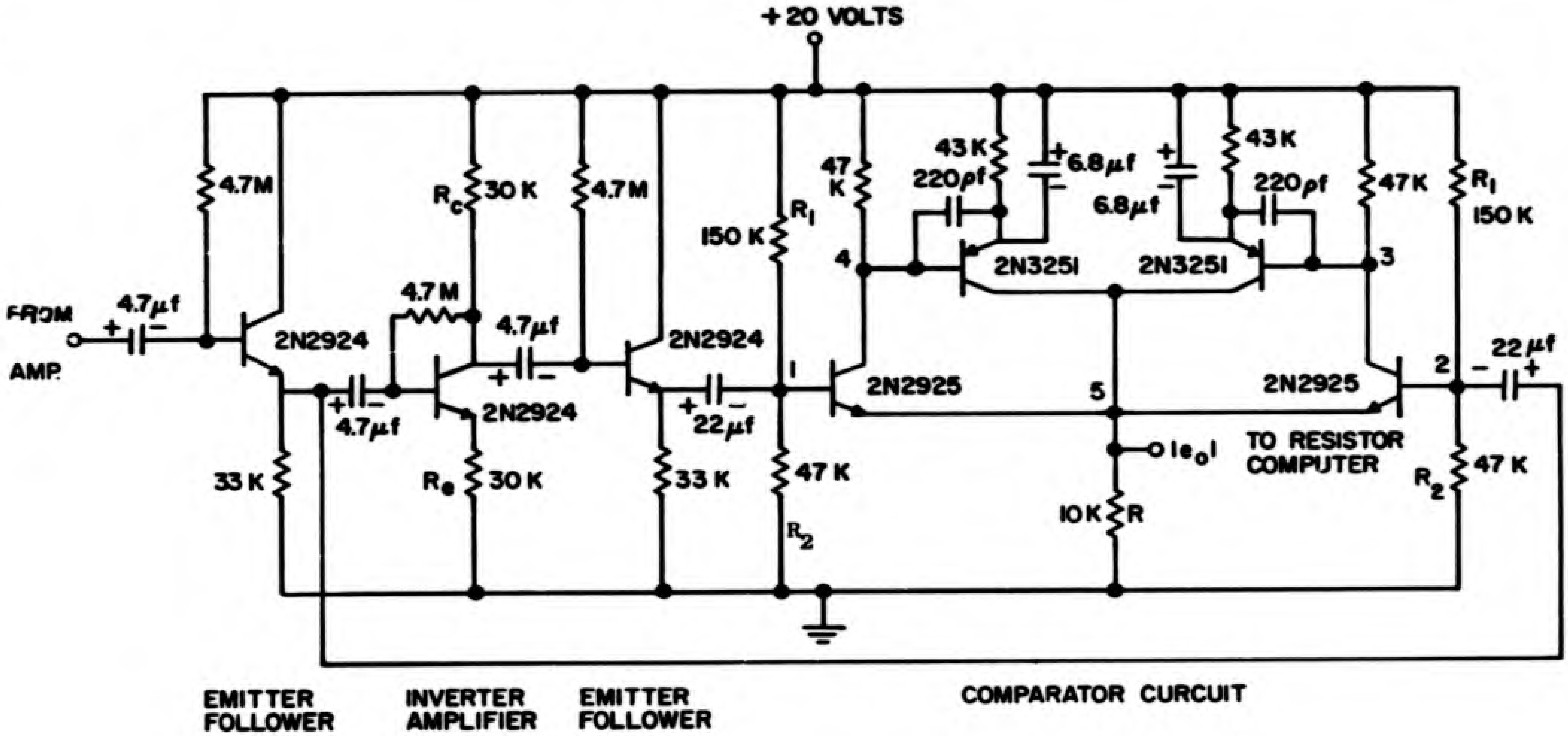


Figure 3. Rectifier, schematic diagram.

negative signal may be received from the high-input, low-output impedance, unity gain amplifier, the phase splitter is required to receive the single-ended input and give two output waveforms—one positive and one negative. It is not known which of these outputs will be positive. A comparator circuit, which represents stage four, compares the two outputs of the phase splitter and follows the more positive of the two signals. The comparator will follow the positive signal, since the phase splitter will always give two equal but opposite outputs to the comparator. The comparator circuit for each channel then gives the absolute magnitude of the accelerometer output, regardless of its original polarity.

4.2.1 Phase Splitter

The phase splitter consists of two emitter followers with an inverter amplifier between them. The first emitter follower (fig. 3) drives the inverter and one side of the comparator circuit. The emitter follower—rather than the high-impedance amplifier—is used as the driver because of its lower output impedance. The circuit for the emitter follower consists of one bipolar 2N2924 and two biasing resistors. The quiescent current requirement is 200 μa. The emitter resistance of 33 kohms was selected to give a high input impedance and to place the emitter at a voltage of approximately 7 v, allowing it to swing in either direction that is necessary to follow a ±4-v signal without going into saturation or cutoff. A 4.7-megohm base resistance was necessary to give the required 200-μa quiescent current. The input impedance of the follower is the parallel combination of R_b and $H_{fe}R_e$, or approximately 2 megohms.

The inverter, driven by the emitter follower, completes the phase splitting process. As a unity gain amplifier, the inverter gives an output of opposite polarity to its input. The component values used in the circuit were chosen as a compromise between input impedance and the collector-emitter voltage of the 2N2924 transistor. For an inverter with a power supply of only 20 v, the collector-emitter voltage is important for ±4-v signals. To avoid driving the transistor into either saturation or cutoff for the ±4-v signal, the collector-emitter voltage must be between 8 and 12 v. A collector-emitter voltage of 10 v will allow a ±5-v swing without reaching saturation or cutoff. The emitter and collector voltages must be at 5 and 15 v, respectively. Before determining the resistances necessary to give these voltages, the quiescent current must be selected. Characteristic curves on the 2N2924 show that for a collector current of 200 μa, a base-emitter voltage of 0.47 v is necessary to keep the bias point in linear operating range of the transistor.

Next, the base-emitter junction of the transistor was biased at 0.47 v to insure a current flow of 200 μa. Since the current gain for the transistor is approximately 100, the base current corresponding to the 200-μa collector current is 2 μa. Therefore with a voltage and current of 9.53 v and 2 μa, the value of the required collector-to-base feedback resistance is 4.76 megohms. The standard value, 4.7 megohms, was used in the circuit, however.

With the base-emitter junction biased to give a 200-μa collector current, the values of both the emitter and collector resistances could be determined. For unity gain, both resistances will be equal, 27.8 kohms. With 27 and 30 kohms being the nearest standard values, the latter value was used because it would increase the input impedance and maintain the collector-emitter voltage within the 8- to 12-v range at 9.2 v. These resistors are matched to better than 1 percent.

Following the inverter, another emitter follower is used for impedance matching; this circuitry is identical with the first emitter follower. The output of this second follower is then fed to the second input of the comparator circuit.

4.2.2 Comparator Circuit

The comparator circuit—last stage of the rectifier—consists of two 2N2925 NPN transistors; each is associated with a common collector or emitter follower configuration. Both transistors have a common emitter resistor. It was originally intended that a configuration like that shown in figure 3 would be used, but without the two inner PNP 2N3251 stages. Without these transistors, the collectors of the 2N2925 transistors would be connected directly to the power supply. Such a configuration would try to follow the more positive of two inputs, but with approximately a 20-percent loss at the 4-mv level.

In the comparator circuit without the two 2N3251 current amplifiers, each 2N2925 transistor was biased to conduct a quiescent collector current of 100 μa. The corresponding base current, which is related to the collector current by the current gain β, is approximately 1 μa. Associated with a particular quiescent base current and base-to-emitter voltage is a characteristic junction impedance, connected in series with the emitter resistor. As the base current is varied, the junction impedance changes—the higher the base current, the lower the junction impedance. In this circuit, the quiescent current level changes, depending upon the input signals. The side receiving less positive signal approaches cutoff and results in decreased collector and base currents. For a base current of less than 1.0 μa, the base-emitter junction impedance increases rapidly, because of the nonlinearity of the change in base current with respect to the change in base-emitter voltage. The side receiving the more positive signal experiences an increase in collector and base currents, and its junction impedance decreases. Without the current amplifiers, the input signal is divided between the junction impedance and the emitter resistor. The output voltage appears across the emitter resistor. With the high junction impedance at the lower input levels, there is a loss of output signal at the lower-input levels. For a 4-mv input, the output was only 3.2 mv.

With the current amplifiers in the comparator to supplement the original 2N2925 transistors, the quiescent current of the 2N2925 remains relatively constant during signal processing. The pulse current is then supplied by the 2N3251, which has a current gain of 100. A 1-μa change in current for the 2N2925 will result in a 100-μa change for the current amplifier. Thus, even with the change in dynamic impedance, sufficient pulse current is supplied to allow the output to follow the input. The base-emitter voltage of the 2N2925 remains constant during the pulse input.

To conserve power, a 100-μa quiescent collector current was chosen for all four transistors. At operating points below 100 μa, the impedance of the base-emitter junction would be too high, resulting in a voltage loss between input and output voltages. It is desired that the voltage at points 1 and 2 be kept close to equal, so that both 2N2925 transistors will conduct about equal quiescent currents. It is also desired that the d-c potential at points 1 and 2 remain constant during inputs. The potential at these points is close to $(R_2B+)/(R_1+R_2)$. However, R_2 has the input impedance of the 2N2925 stages in parallel with it. In stabilizing the voltage at points 1 and 2, it is therefore desired that the input impedance of the 2N2925 stages be high compared with R_2. Also, R_1+R_2 should be high enough so that a minimum of current is required to establish this bias. R_2 should be high so that the input impedance of the stage is high. To satisfy these constraints, the values shown in figure 3 for R_e, R_1, and R_2 were chosen. Point 5 is at 4.0 v.

The collector resistors of the 2N2925 transistors are high enough to bias on the two 2N3251 transistors. The 43-kohm resistors in the emitter of the 2N3251 transistors are to stabilize the d-c operating points. The emitter bypass capacitors are to increase the current gain of the stage. The 220-pf capacitors are used as high-frequency filters.

4.3 Resistor Computer

This section reviews briefly the derivation of the resistor computer technique and its design. Additional details are presented in reference 1, which shows the geometrical-electrical analogy for obtaining the SRSS of two voltages with a piecewise linear network. The magnitude of the resultant vector obtained by the vector sum of two orthogonal inputs is represented by a circle. The circle, in turn, can be approximated by an N-sided polygon.

The family of solutions for the SRSS of two orthogonal inputs lies on a right circular cone having a half-apex angle of 45 deg and its apex at the origin. The cone can be approximated by planes passing through the origin and through the sides of the polygon forming a pyramid (fig. 4). For each value of X and Y, the correct SRSS lies on the surface of the cone, with the approximate value lying on the surface of the pyramid. Each plane is represented by a resistive network of three resistors in a tee shape. A multitude of these networks will therefore represent the pyramid. For each X and Y voltage input to the total resistive network, the network will give out N voltages, each value lying on a plane, where N is the number of planes (and resistive networks). If the inputs to the resistor computer are always positive, only the first quadrant need be considered. Figure 5 shows the total resistive network for three planes per quadrant. In some planes, the center resistor has an infinite resistance. The output is at the center of the tee and, for a given X and Y voltage input, represents the corresponding Z intersect on that plane. Only one output from the network of the tee lies on the surface of the pyramid. As reported in reference 1, the desired value is the highest output of the resistor computer.

Diodes can ordinarily be used to select the highest signal present. Reference 2 has extended this analysis to obtain the SRSS of three inputs directly. A comparison of the results of references 1 and 2 shows that greater accuracy is attained for a given electronic component count by determining the SRSS of two inputs and repeating the process than by a single step where three inputs are processed simultaneously. The results show that the use of three planes to represent the first quadrant for the two-input case introduces a 3.4-percent maximum error. The resistor computer shown in figure 5 is capable of introducing a maximum error of 3.4 percent. The computer design requires that the output impedance of the positive input source be small compared with R, and that the input impedance of the stage following the computer be large compared with R. Since the computer is to function with low-frequency pulses, the input is capacitive coupled. This requires that the input RC time constant be at least 0.1 sec, so that 0.25-sec half sine wave pulses are coupled undistorted. The input impedance of the computer in figure 5 is 1.38 R. To keep the input impedance around 15 kohms, R must be approximately 11 kohms. The measured output impedance of the rectifier used to supply the positive inputs is less than 150 ohms for 4-v pulses and falls to about 20 ohms at 4 mv. The emitter followers that measure the output pulses of the computer have an input impedance of approximately 2 megohms.

The resistor computer (fig. 5) consists of three resistive voltage dividers in which the ratio of the resistances is based on reference 1. The divider on the left produces a signal at the midpoint which equals $f(Y/X)\sqrt{X^2+Y^2}/\sqrt{2}$ for values of Y ranging from zero to 0.57735 X. The resistor 5.099 R serves to adjust the loss incurred by resistor network addition to a value of exactly $2^{-1/2}$. The center divider produces an output equal to $f(Y/X)\sqrt{X^2+Y^2}/\sqrt{2}$ for

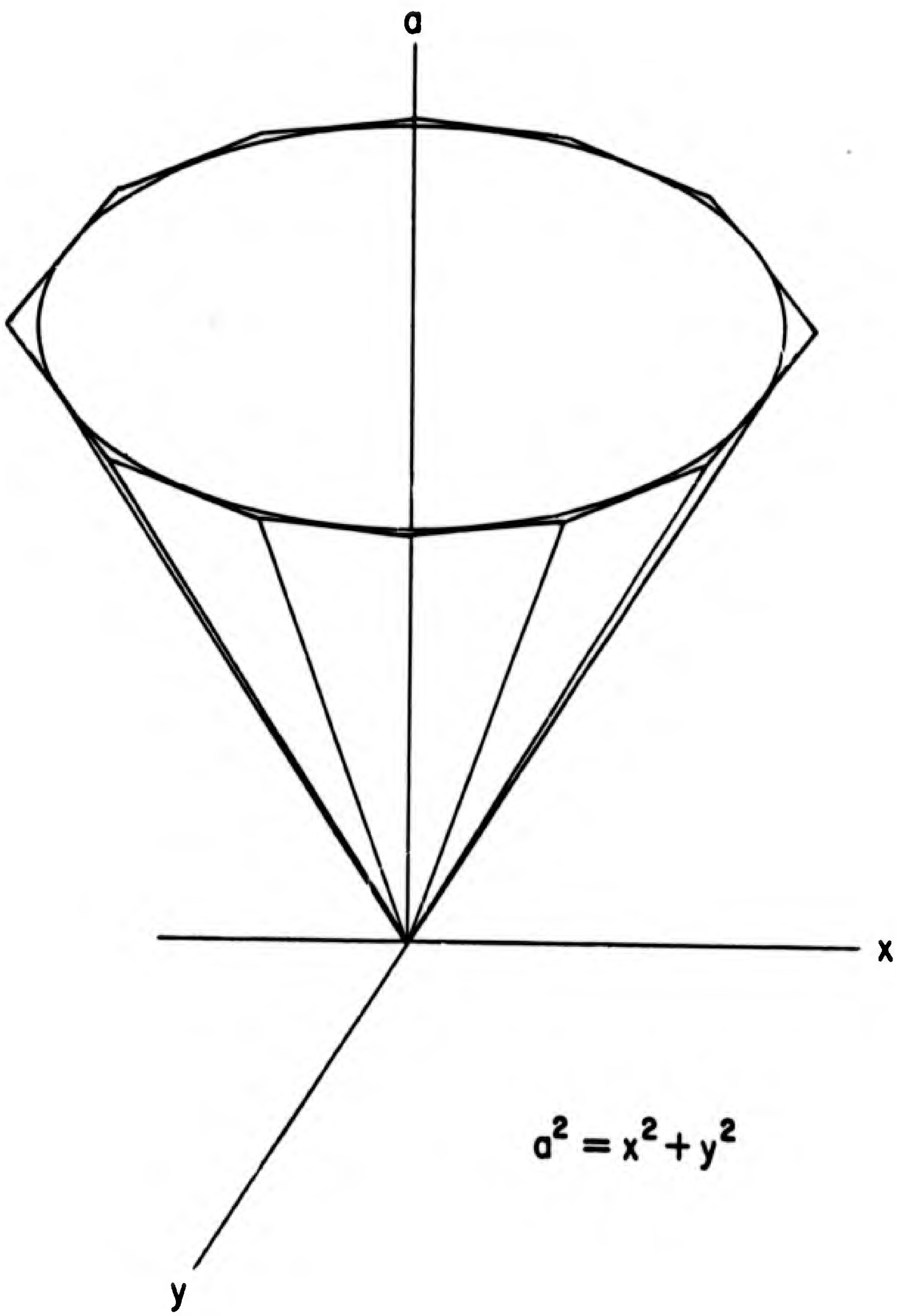
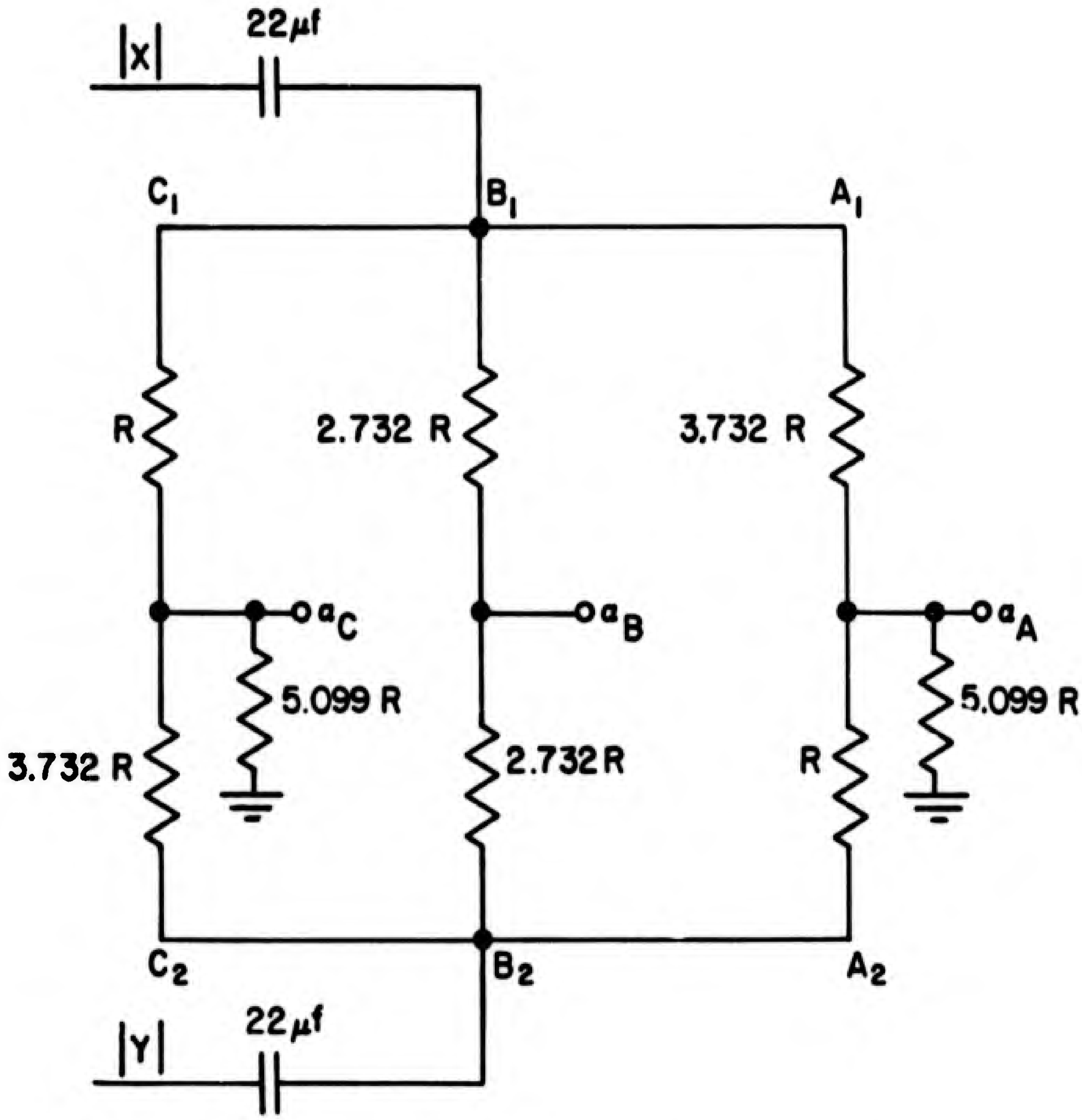


Figure 4. Circumscribed cone.



$$\alpha_A = 1/\sqrt{2}\ (0.9659\ X + 0.2588\ Y)$$
$$\alpha_B = 1/\sqrt{2}\ (0.7071\ X + 0.7071\ Y)$$
$$\alpha_C = 1/\sqrt{2}\ (0.2588\ X + 0.9659\ Y)$$

Figure 5. Resistor computer, schematic diagram.

values of Y ranging between 0.57735 X and 1.7321 X. The loss incurred in this element needs no adjustment since it equals $2^{-1/2}$. The divider on the right produces an output equal to $f(Y/X)\sqrt{X^2/Y^2}/\sqrt{2}$ for values ranging between 1.7321 X and infinite X. In this element, the resistor 5.099 R adjusts the loss to exactly $2^{-1/2}$. The function F(Y/X) represents the accuracy of the approximation, which is 1.00 if Y/X is 0.26795, 1.000, and 3.7321; and the accuracy varies to 0.966 where Y/X is 0.0, 0.57735, 1.7321, and infinity.

Ordinarily, diodes can be used in parallel with the three output points and the monitoring device. In this application, the 4-mv signals would require perfect diodes; therefore, they have been eliminated in favor of the peak follower circuit.

4.4 Emitter Follower

The emitter follower has the characteristics of unity gain and low-output impedance. Impedance matching circuitry was required to match each of the three outputs of the resistor computer with the three inputs of the peak follower. Figure 6 illustrates the circuit, which is identical in design requirements and components with the followers used in the rectifier.

4.5 Peak Follower

The peak follower circuit, shown schematically in figure 7, selects the correct voltage from the three outputs of the resistor computer, the correct output being the largest voltage. The circuit is identical with the comparator circuit, except that another 2N2925 and 2N3251 combination is included to increase the number of inputs to three. The peak follower, therefore, functions the same way as the comparator circuit—selects the most positive input. With the requirement that a quiescient current of 100 μa flow in each transistor, the circuit was biased to a 6-v drop across the 10-kohm emitter resistor. The peak follower circuit has one advantage over the comparator circuit, in that it receives only positive signals. Thus, the transistors receiving the two smaller inputs will experience a decrease in base-emitter voltage, but will not be driven into cutoff as rapidly as transistors receiving negative signals.

4.6 Scaling Amplifier

The scaling amplifier acts as an intermediate stage between the output of the peak follower for channels X and Y and the input of the second resistor computer for channel Z. Since the resistor computer for X and Y channels gives $K\sqrt{X^2+Y^2}$ as an output, the purpose of the scaling amplifier is to amplify $K\sqrt{X^2+Y^2}$ by 1/K to give the correct input for the resistor computer in the Z channel.

The scaling amplifier shown in figure 8 consists of three stages. Stage 1, a unity gain inverter, is needed to maintain the

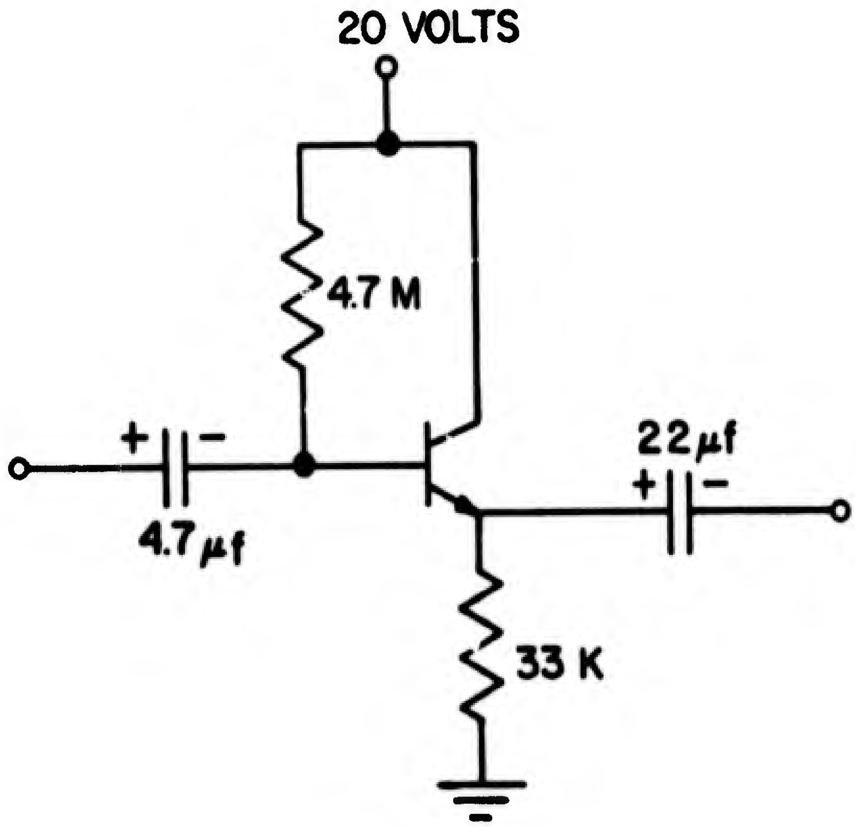


Figure 6. Emitter follower, schematic diagram.

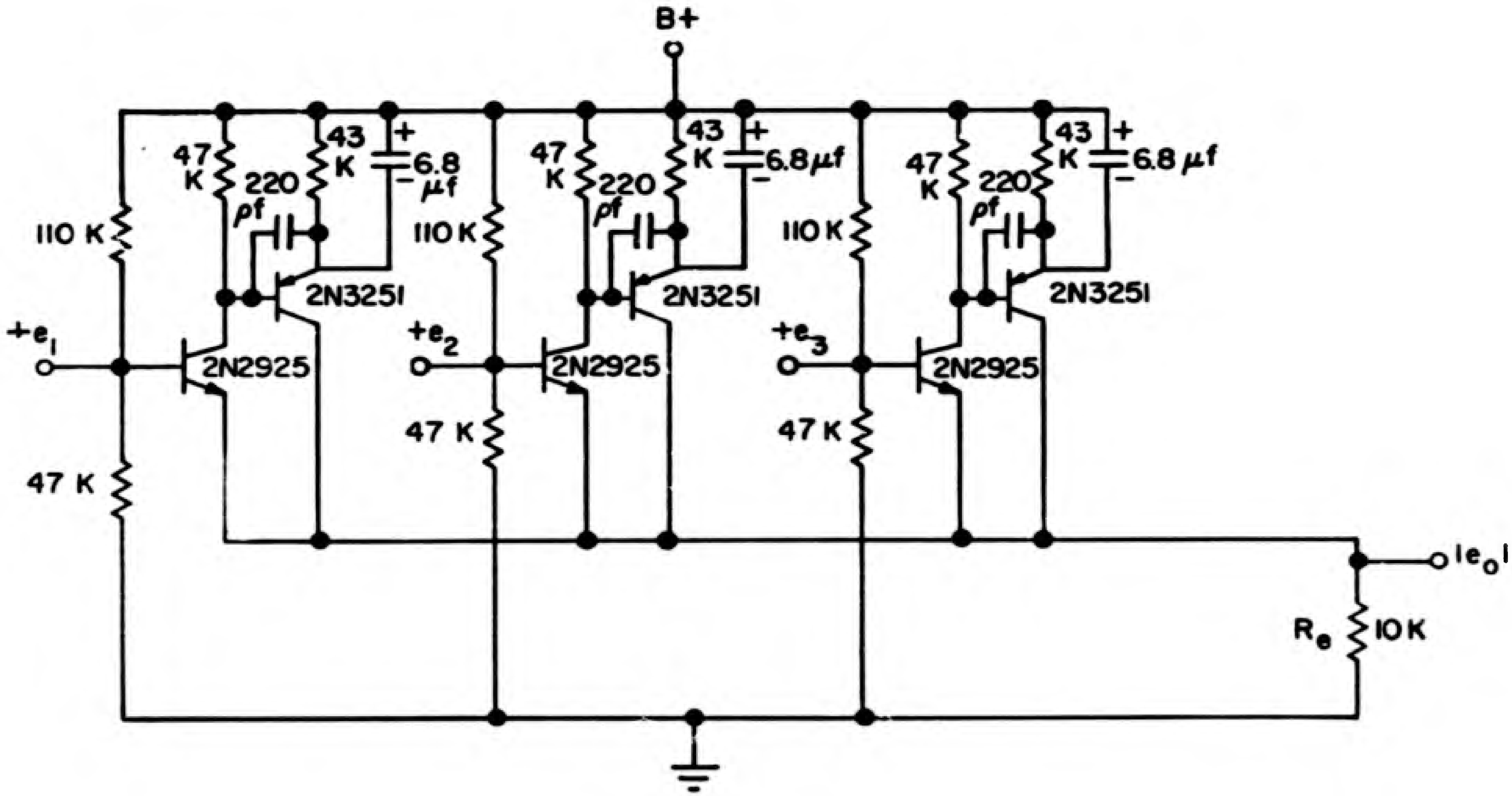


Figure 7. Peak follower, schematic diagram.

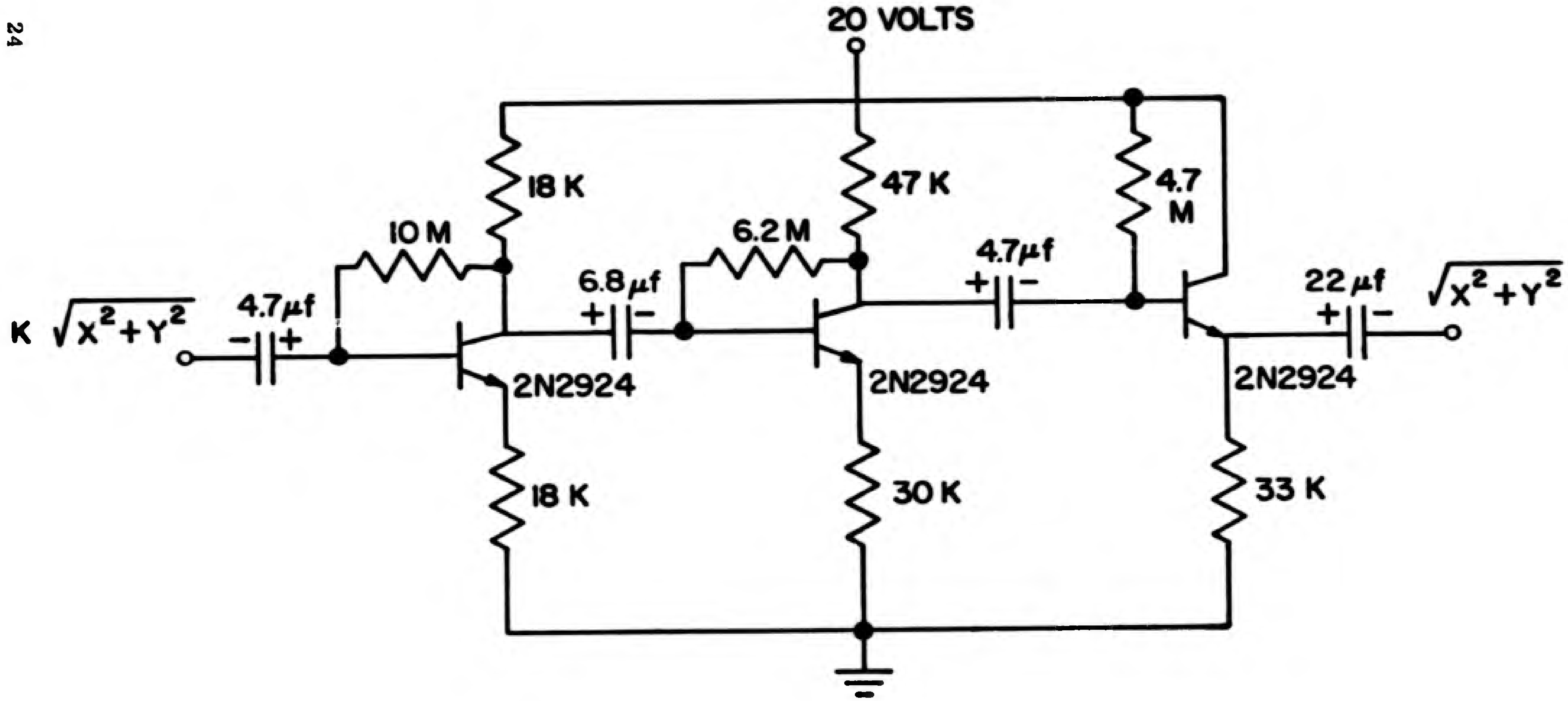


Figure 8. Scaling amplifier, schematic diagram.

correct phase relationship, since stage 2, the amplifier, also gives a phase inversion. The gain of stage 2 is $2^{1/2}$. Stage 3 is an emitter follower that serves as an impedance matching device.

5. EVALUATION OF SYSTEM

Tests were made to determine the computational accuracy and frequency response of the system (table I). Since the resistor computer circuit has an inherent geometrical error that varies from 0 to 3.4 percent with the relative values of the input signals, tests were made at points for minimum and maximum error. For one point of minimum geometrical error, both inputs to each resistor computer are of equal amplitude. For one point of maximum geometric error, one input signal is zero.

To simulate the different conditions, resistive voltage divider networks were designed to give a particular signal level for each channel input. These signal levels were monitored by an oscilloscope unit. Also for each case, one output from the divider network was made equivalent to the calculated SRSS output for the complete system. After establishing the input levels, the oscilloscope was used to measure the voltage difference between the actual output of the system and the simulated SRSS calculated output given by the voltage-divider network.

5.1 Circuit Error

To find the circuit error, it was necessary to test the network under one of the conditions required for minimum geometrical error. This condition requires that the pair of inputs for each resistor computer be equal. Therefore, for an input of E—where E varies from 4 mv to 4 v on the Z channel—the output of the scaling amplifier in the X and Y channels must likewise be equal to E. Thus, if an input of $E/\sqrt{2}$ is used for the X and Y channels, the resistor computer for X and Y gives $\sqrt{(E/\sqrt{2})^2 + (E/\sqrt{2})^2}/\sqrt{2}$, or $E/\sqrt{2}$, which is then amplified by the scaling amplifier to give E.

For the maximum geometrical error, both the Y and Z inputs were made equal to zero. Other test conditions with all three inputs equal to E were used. Such conditions account for a geometrical error between 0 and 3.4 percent. Both negative and positive signals were used to test all stages of the network. The test apparatus used to determine the computational accuracy of the system is block diagrammed in figure 9. The three-input peak follower circuit introduces most of the circuit error for all input values. At the 4-mv input level, the percentage loss in the peak follower is greatest. The remaining circuit error is distributed among the various circuits. It is believed that the circuit error can be reduced by more careful matching of the resistors in the inverter and in the resistor computer. Figure 10 is a graph of the error versus input for the points of maximum and minimum geometric error.

TABLE I. COMPUTATIONAL ACCURACY OF THE SYSTEM

Input	E	A	ΔE_o (mv)	TE_o (percent)
		$A = \frac{\sqrt{X^2+Y^2+Z^2}}{\sqrt{2}}$	$\Delta E_o = (E_o - A)$	$TE_o = \frac{(E_o-A)\ 100}{A}$
$X = \frac{E}{\sqrt{2}}$	4 mv	4 mv	-0.4	-10
	50 mv	50 mv	-1.2	-2.4
$Y = \frac{E}{\sqrt{2}}$	200 mv	200 mv	-2.8	-1.4
	500 mv	500 mv	-8	-1.6
Z=E	1 v	1 v	-12	-1.2
	2 v	2 v	-19	-0.95
	3 v	3 v	-32	-1.07
	4 v	4 v	-64	-1.6
X=E	4 mv	2.83 mv	- 0.3	-10.6
	50 mv	35.4 mv	- 0.8	-2.26
Y=0	200 mv	141.4 mv	- 1	-0.706
	500 mv	354.0 mv	- 8	-2.26
Z=0	1 v	0.707 v	-16	-2.26
	2 v	1.414 v	-36	-2.54
	3 v	2.12 v	-72	-3.4
	4 v	2.83 v	-140	-4.94
X=E	4 mv	6.94 mv	- 0.3	-7.5
	50 mv	86.6 mv	- 1	-2.0
Y=E	500 mv	866.0 mv	-15	-3.0
Z=E	1 v	1.732 v	-28	-2.8
	2 v	3.47 v	-52	-2.6
	4 v	6.94 v	-116	-2.9
X=E	4 mv	6.94 mv	- 0.35	-8.75
	50 mv	86.6 mv	- 2.2	-4.4
Y=E	500 mv	866.0 mv	- 7	-1.4
Z=-E	1 v	1.732 v	-14	-1.4
	2 v	3.47 v	-40	-2.0
	4 v	6.94 v	-104	-2.6

TABLE I. COMPUTATIONAL ACCURACY OF THE SYSTEM (Cont'd)

Input	E	A	ΔE_o (mv)	TE_o (percent)
		$A = \frac{\sqrt{X^2+Y^2+Z^2}}{\sqrt{2}}$	$\Delta E_o = (E_o - A)$	$TE_o = \frac{(E_o - A)\ 100}{A}$
X=E	4 mv	6.94 mv	-0.3	-7.5
	50 mv	86.6 mv	-1.4	-2.8
Y=-E	500 mv	866.0 mv	-7	-1.4
Z=-E	1 v	1.732 v	-15	-1.5
	2 v	3.47 v	-27	-1.35
	4 v	6.94 v	-72	-1.8
X=-E	4 mv	6.94 mv	-0.3	-7.5
	50 mv	86.6 mv	-1	-2.0
Y=-E	500 mv	866.0 mv	-2.2	-0.44
Z=-E	1 v	1.732 v	-2.2	-0.22
	2 v	3.47 v	-3.0	-0.15
	4 v	6.94 v	-4.0	-0.10

A = Calculated SRSS output from measured X,Y, and Z channels.

E_o = Measured voltage output of system.

ΔE_o = Voltage difference between the measured output of the system and the calculated output based upon measured X,Y, and Z inputs.

TE_o = Total percent error for system.

The above data were recorded using an oscilloscope test unit with a maximum sensitivity of 1 mv/cm. At the input level of 4 mv, it was difficult to accurately read a differential voltage of 0.5 mv or less. Therefore, the errors measured at these levels were estimated and estimated on the high side.

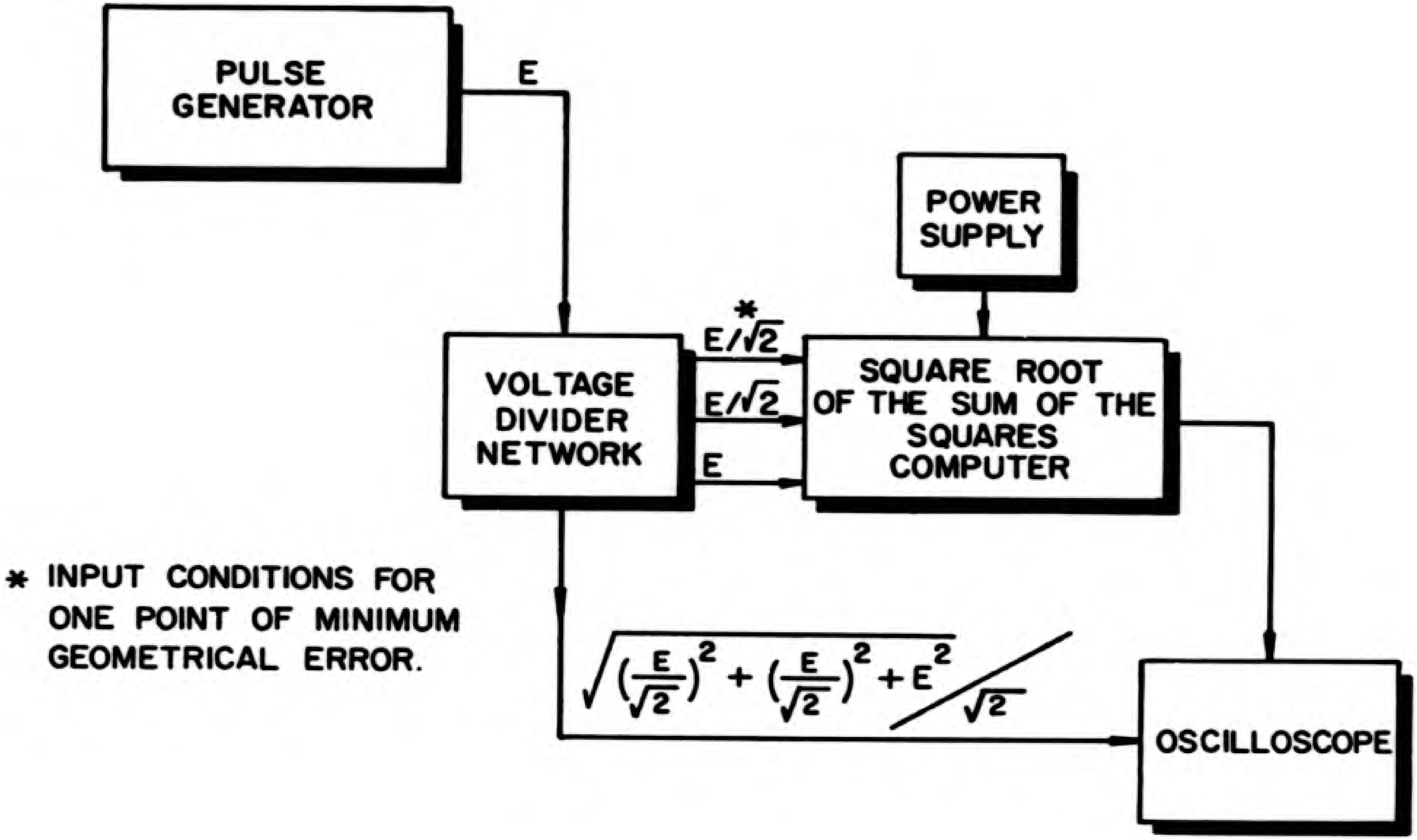


Figure 9. Test apparatus used to determine computational accuracy of system.

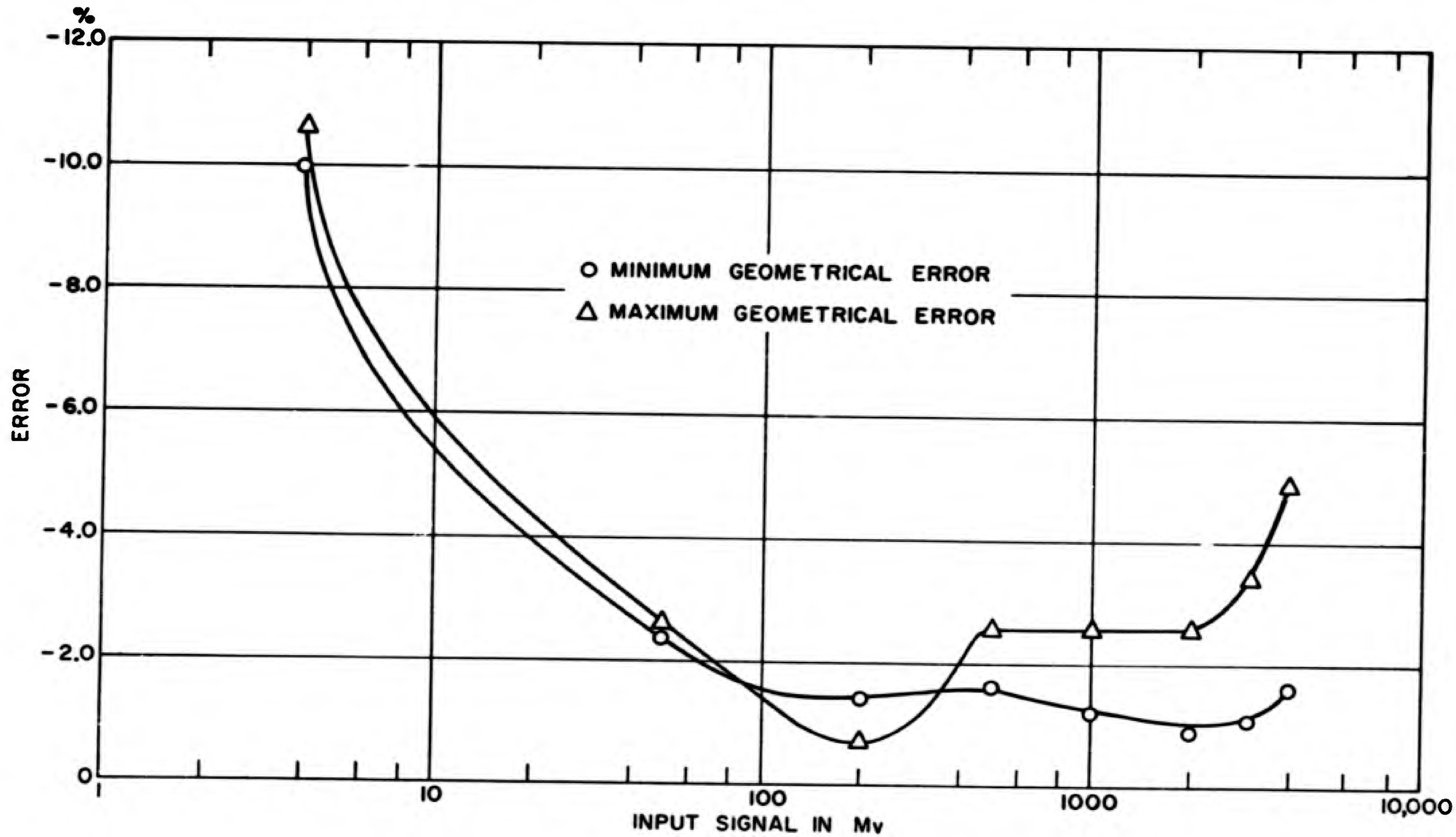


Figure 10. Percentage error versus input signal.

5.2 Frequency Response

Figure 11 illustrates the test apparatus used to determine the frequency response of the system. The simulated input from the divider network was compared with the actual output of the SRSS circuit. Photographs were taken using different coupling capacitances C_c at frequencies between 4 and 4000 cps. To meet the electrical requirements for this frequency response, 4.7- and 6.8-μf coupling capacitors (fig. 3) were used, except that 22-μf capacitors were used to couple the inputs of both the comparator and resistor computer circuits. The curves in figure 12 show that a coupling capacitance of 22 μf was required for the comparator and computer circuits to realize the necessary response.

The data given in table I were obtained by using a 40-μsec rectangular wave pulse at the input signal, whereas a half-sine wave pulse was used for the frequency response data shown in figure 12.

6. SUMMARY

The circuit design described herein has been evaluated and determined feasible for computing the SRSS of three inputs from three orthogonal piezoelectric accelerometers. The system has proved operable from 4 to > 4000 cps, and has an error of less than 5 percent from 50 mv to 4 v and less than 10 percent from 4 to 50 mv.

The circuits will be subjected to shock tests during a subsequent work phase. The components used in the prototype model, however, are considered to be no more sensitive to shock than the batteries and telemetry tube used within the ball.

7. REFERENCES

(1) T. E. Stern and R. M. Lerner, "A Circuit for the Square Root of the Sum of the Squares," Proc IEEE, vol 51, Apr 1963, p. 593.

(2) HDL Report No. TR-1243, "Some Methods of Approximating an Omnidirectional Accelerometer with Multiple Uniaxial Accelerometers," William E. Ryan, 6 May 1964.

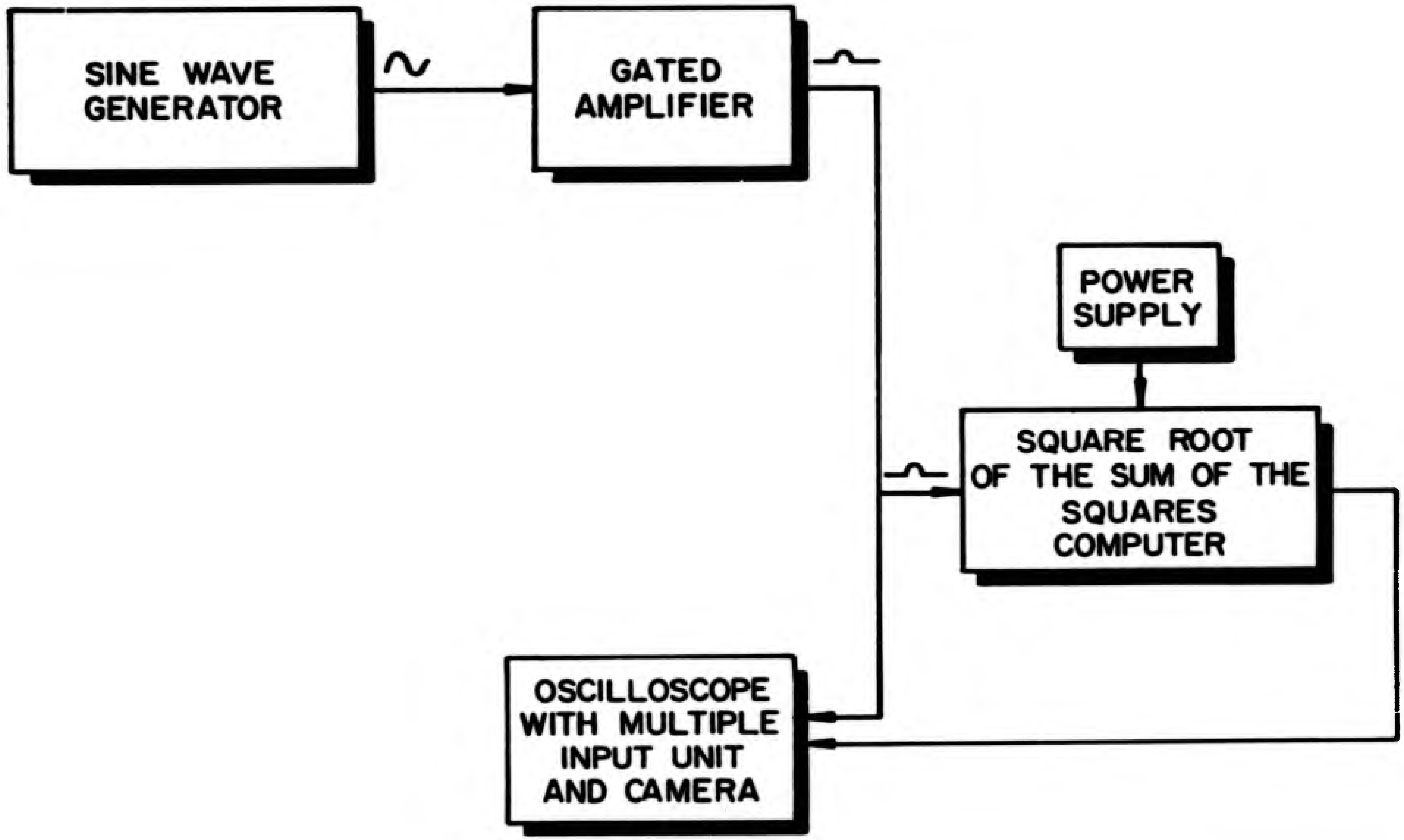


Figure 11. Test apparatus used to determine frequency response of system.

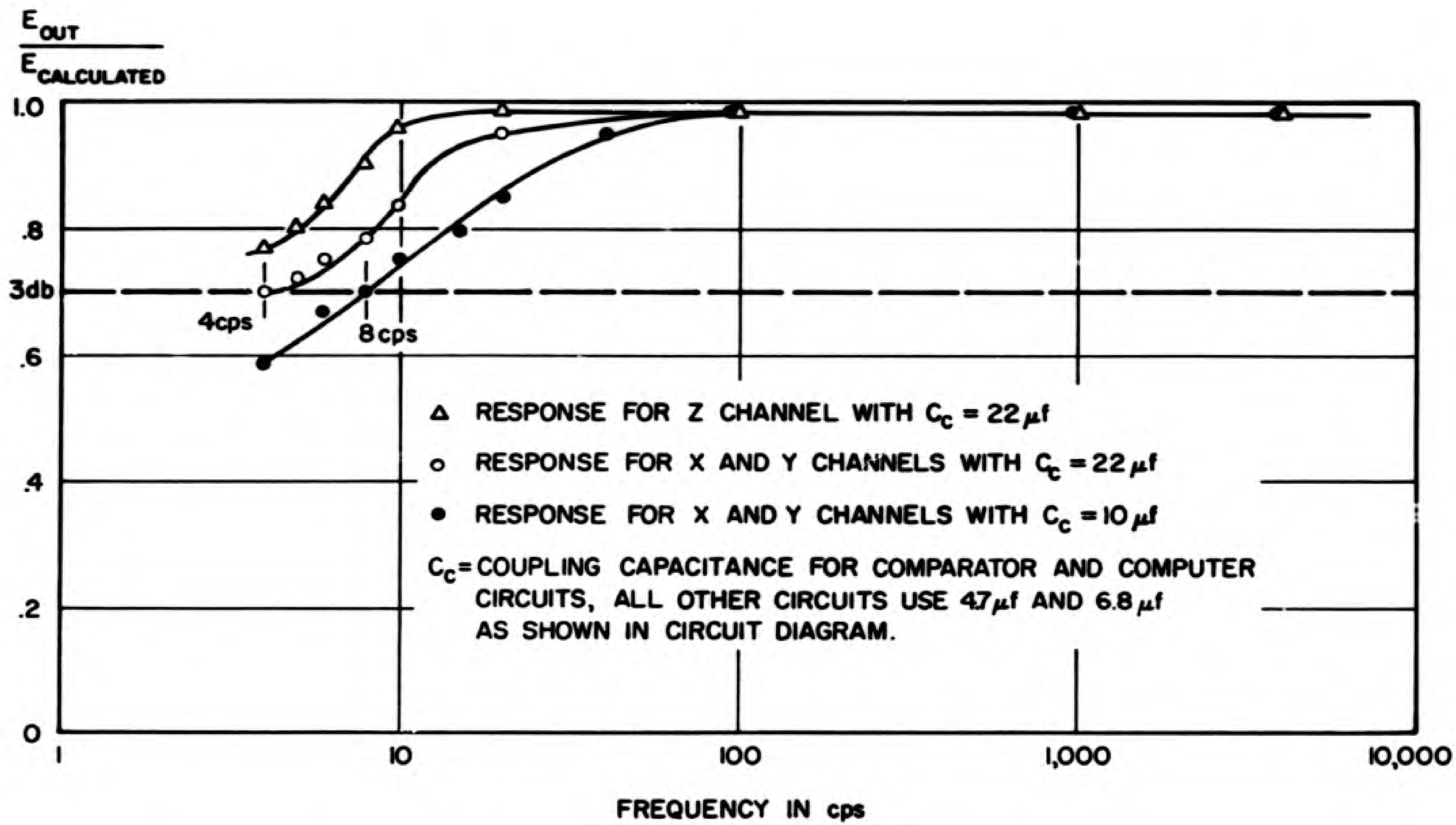


Figure 12. Curves showing frequency response of system.

APPENDIX A.—COMPONENT VALUES ESTABLISHED FOR HIGH-IMPEDANCE AMPLIFIER

Values for the components illustrated in figure A-1 were established by the following procedure.

R_g: At a frequency of 10 kc or higher, the input impedance of the amplifier is equivalent to R_g. At the lower frequencies, the use of capacitor C_b increases the input impedance above the value of R_g. Therefore, to give a minimum input impedance of 22 megohms, R_g was selected at 22 megohms.

With a source voltage of 10 v and a minimum pinch-off voltage of 1 v (as given by the 2N2606 specification sheets), the gate voltage is 11 v. Also given by the specification sheets is a maximum gate saturation current of 65 x 10^{-9} amp. The resulting maximum voltage drop across R_g is 1.43 v. Point A is therefore set at 12.43 v to maintain V_g at 11 v.

R_1 and R_2: A voltage divider network consisting of R_1 and R_2 is used to pinpoint A at 12.43 v. R_1 is selected as 2.2 megohms and R_2 is calculated as 1.3 megohms. The standard values of 1.2 and 2.2 megohms are used in the circuit.

R_d: This resistance controls the biasing of the base-emitter junction of the 2N2924. From the I_c versus V_{be} plot (2N2924 data sheet), V_{be} must be 0.45 v for a collector current of 150 μa. Assuming a base current of 1 μa or less, R_d is

$$R_d = 0.45/I_d = 0.45/50(10^{-6}) = 9 \text{ kohms}.$$

The nearest standard value, 9.1 kohms, was used in the circuit.

R_s: To pinpoint B at the design voltage of 10 v for a known quiescent current, the resistance R_s is used to give the required voltage drop. The total current through R_s is $I_d + I_c$, or 200 μa. Therefore,

$$R_s = 10/200(10^{-6}) = 50 \text{ kohms}.$$

Since 50 kohms is not a standard value, a value of 51 kohms was used.

C_b: Capacitor C_b bootstraps the low side of R_g to the output, thus increasing the input impedance above 22 megohms, which is the case without C_b. 0.1 μF is selected for C_b.

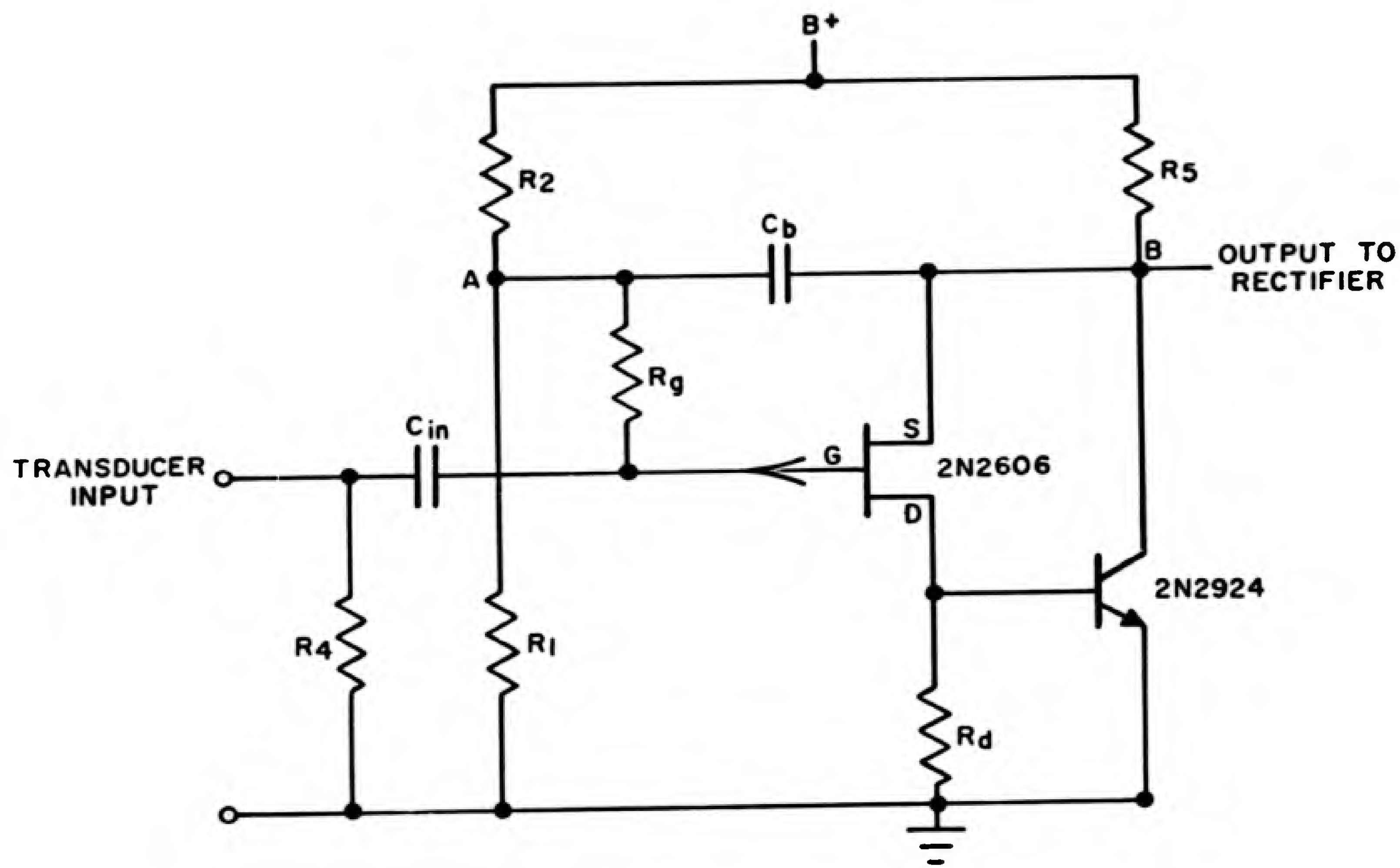


Figure A-1. High-input impedance amplifier.

R_4: The purpose of R_4 is to provide a short equilibrium charge time after power is applied for capacitor C_{in}. A high value of resistance was used to shunt the input of the amplifier. This resistance, R_4, was selected as 22 megohms. In using this criterion for a short equilibrium time, the input impedance was decreased from approximately 150 megohms to the parallel combination of R_4 and the 150 megohms, or 18 megohms. The 18-megohm value, however, still exceeds the 6.14-megohm minimum requirement established for the desired application.

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CIRCUIT REALIZATION OF A SQUARE ROOT SUM OF SQUARES COMPUTER -- I. R. Marcus, J. W. Miller, Jr., A. J. Buschman, Jr.

TR-1271, 25 January 1965, 17 pp text, 13 illus., AMCMS Code 5900.21.23127, HDL Proj 45900, UNCLASSIFIED Report

An electronic system has been developed to compute the square root of the sum of the squares for three input variables. The basic technique is to use a conventional triaxial accelerometer and to process the three input signals, giving as an output one waveform. This report covers specifically the design and evaluation of circuitry that (1) accepts input signals from the accelerometers during impact, and (2) computes an instantaneous magnitude of the acceleration-time curve continuously.
The circuitry has been determined operable over a dynamic range of 4 mv to 4 v, with a frequency response of 4 to over 4000 cps. A computational accuracy of within 5 percent has also been proved between 50 mv and 4 v; an accuracy to within 10 percent has been proved from 4 to 50 mv.

Computer

Square root of the sum of the squares computer

Omnidirectional accelerometer

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