TI Report No.
03-65-35

THIN FILMS FORMED BY ELECTROCHEMICAL REACTIONS

Quarterly Progress Report No. 6

for the Period

1 December 1964 to 28 February 1965

Contract No. DA 36-039 AMC-02324(E)

Prepared for
U.S. Army Electronics Laboratories
Fort Monmouth, New Jersey

By
Coy D. Orr

Texas Instruments Incorporated
P.O. Box 5012
Dallas 22, Texas

ABSTRACT

Reactively sputtered thin films of tantalum oxide deposited onto thermally oxidized silicon offer a very wide range of sheet resistivities. The application of an external d-c bias to the substrate during sputtering alters sheet resistivity with no change in film thickness. Resistors of 237 ohms/sq changed less than 3% after 1000 hours at +125°C and 2.5 watts/sq inch.

Reactively sputtered Ta_2O_5 dielectric films deposited onto aluminum electrodes offer capacitance values from 0.3 to 3.0 pF/mil^2 and d-c breakdown voltages of 60 to 6 volts, respectively. Yields of 64% within ±20% of 0.5 pF/mil^2 and breakdown voltage greater than 18 volts have been demonstrated. Capacitors tested for 1000 hours at +125°C and 60% of destructive breakdown voltage changed less than 2% from initial capacitance.

Coy D. Orr
C.D. Orr
Project Engineer

John D. Brahm
Patent Attorney
Texas Instruments Incorporated

J. A. Cunningham
Section Leader
Semiconductor Network
Technology Group

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF TABLES (Continued)

TRIPS, LECTURES, CONFERENCES

Mr. Coy D. Orr visited the U. S. Army Electronics Laboratories at Fort Monmouth, New Jersey on January 21, 1965.

Mr. I. H. Pratt and Mr. A. J. Raffalovich at Fort Monmouth represented the contract office.

It was decided at the meeting that the work of the eighth quarter will involve applying thin resistive and dielectric films to a silicon substrate that contains diffused active devices.

A demonstration circuit for this purpose is discussed in Section VII of this report.

SECTION I
PURPOSE

The purpose of this investigation is the development of techniques for fabricating thin conductive, resistive and dielectric films, by complete or partial oxidation of a suitable metallic film deposited in predetermined patterns and sequences. The substrate of interest is primarily an oxidized silicon semiconductor slice containing diffused active elements.

SECTION II
OBJECTIVES

The objectives of the contract are:

Compatibility with the present state of diffused planar silicon diode and transistor integrated circuit process technology,
Resistive films of up to 10 megohms per sq inch of substrate,
Dielectric films providing a capacitance of up to 3 microfarads per sq inch of substrate.

These objectives, therefore, take into consideration approaches which improve both the basic film characteristics and the component geometry. The specifics of the contract work statement (Signal Corps Technical Requirement SCL-7577C dated 8 January 1963) include the following film requirements:

RESISTIVE FILM

Resistance up to 10 megohms per sq inch
Tolerance, target ±2%
Temperature coefficient of resistance of ±200 ppm/°C over the range -55°C to +125°C
Power dissipation of 2 watts per sq inch at +125°C
Life test of 1000 hours at +125°C, the resistance shall not change more than 1%.

DIELECTRIC FILM

Capacitance up to 3 microfarads per sq inch

Tolerance (not specified, about ±20% of a desired target value)

Temperature coefficient of capacitance of ±250 ppm/°C over the range -55°C to +125°C

Working voltage is specified as 75% of the anodizing voltage (for investigation of films prepared by other techniques, this suggests a rated working voltage of 15 volts dc at 125°C). The insulation resistance shall exceed 1000 ohmfarads at 15 volts dc at 25°C. The dissipation factor shall be less than 5% at 1 KC at 25°C.

Life test (not specified, initial tests shall be at 15 volts dc at 125°C).

SECTION III
THIN FILM RESISTORS

The process variables for reactive sputtering of Ta_2O_5/Ta resistive films have been further explored, indicating conditions for depositing a wide range of sheet resistivities.

Substrate bias sputtering, sputtered Ta_2O_5 dielectric surface protection, and resistor life-tests were investigated.

A. SUBSTRATE PREPARATION

1. Polishing and Cleaning

Slices of single-crystal "p"-type silicon were mechanically polished and chemically cleaned. The discs were about 1 (one) inch in diameter and 0.010 inch thick.

2. Surface Passivation

A surface passivation of SiO_2 approximately 10,000Å thick was prepared by oxidation of the silicon slices in an open quartz tube furnace at 1200°C in the presence of steam for 100 minutes.

3. Removal of Organic Particles

The oxidized slices are cleaned for about 5 minutes in concentrated H_2SO_4 at 180°C to remove organic particles, then rinsed in flowing hot deionized water.

4. Storage

The oxidized slices were stored in plastic covered dishes until ready for use.

5. Flushing and Drying

Immediately before being placed in the vacuum chamber for film deposition, the oxidized slices were flushed with isopropyl alcohol and dried with a blast of dry air.

B. SUBSTRATE BIAS SPUTTERING

As described in the report for the previous quarter[1], the application of an independent, electronically regulated d-c potential between the substrate holder and the glow-discharge anode very strongly influences the resultant sheet resistivity of reactively sputtered Ta_2O_5/Ta films.

Furthermore, "thicker" films were less sensitive to the effects of this substrate potential.

In a similar manner, the temperature coefficient and elevated temperature drift were altered by the magnitude and polarity of this bias current.

In recent literature, Vratny and Schwart[2] reported that some of the variable properties of tantalum films deposited by glow-discharge sputtering may be due to a fluctuating potential on the substrate. They propose that the use of a negative or positive d-c potential on the substrate holder allows control over the properties of the film because of separation of ion- and electron-bombardment processes on the substrate.

Maissel and Schaible[3] have further reported that if films are sputtered from a tantalum cathode onto a substrate biased negatively relative to the plasma, a curve of film resistivity as a function bias may be obtained. Typical curves reportedly have a minimum resistivity

at about +20 volts and a maximum near -100 volts.

Using the sputtering apparatus of Fig. 1, significant experiments have been completed which support the work of Vratny and Schwartz as well as extend the work by Maissel and Schaible to include sputtering in an oxygen partial pressure.

A series of resistive films of Ta_2O_5/Ta were reactively sputtered with time and substrate potential being the experimental variables.

Sputtering conditions were as follows:

Tantalum cathode, 10 inch^2 disc

Thermally oxidized silicon slices, held by aluminum clips to a 4 inch diameter aluminum holder, electrically isolated from the vacuum system. The spacing between cathode and substrate surface was 2 ± 1/4 inch and the substrate holder was rotated approximately 20 rpm during sputtering.

Sputtering chamber was dynamically flushed with a mixture of approximately 2000 ppm (volume) oxygen in argon, at a total pressure of 5×10^{-2} Torr.

Glow-discharge sputtering current was 5 mA/inch^2 of cathode area at 2.0 Kv dc.

An independent, electronically regulated d-c potential was maintained between the substrate holder and the glow-discharge anode, (base-plate of the system).

The sputtering was performed against a tantalum shutter for 15 minutes (or longer if required to set stable conditions), then against the oxidized silicon substrates for the specified times.

Assembly and testing were as described in Sections III.B.2 and III.B.3 of Report No. 6 of this contract[4].

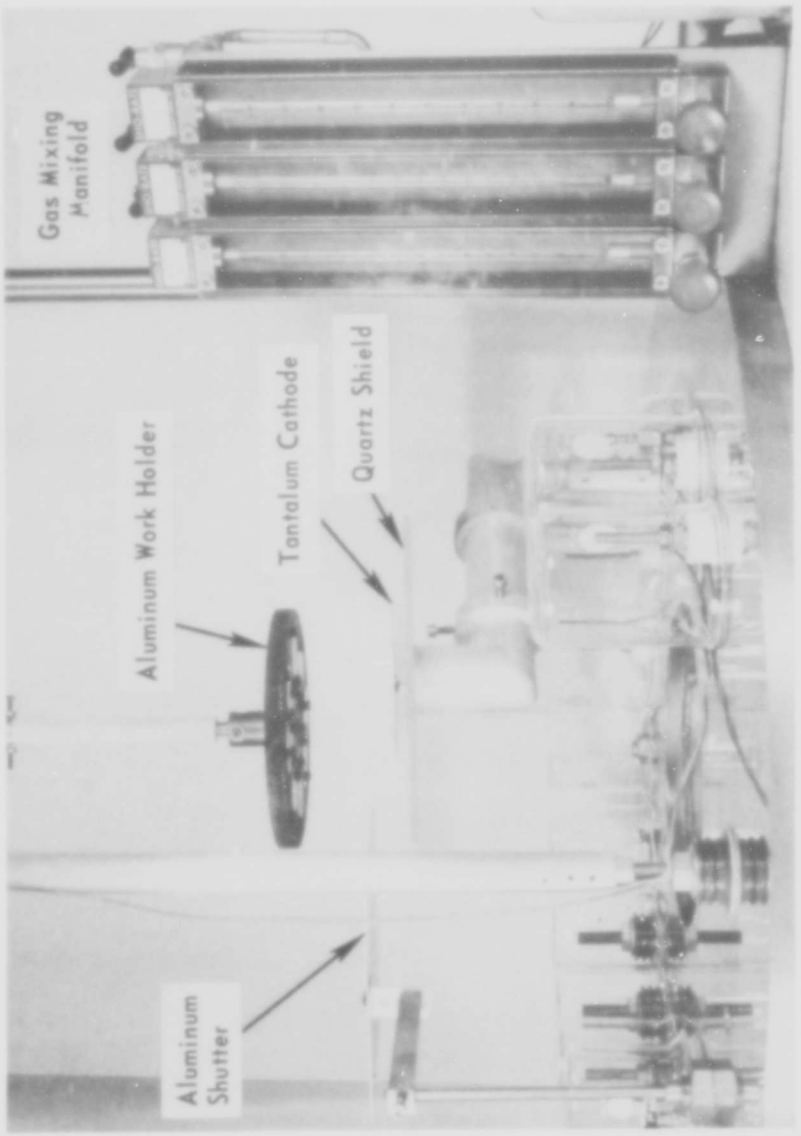


Fig. 1. Apparatus for Reactive Sputtering of Ta_2O_5/Ta Resistive Films

All data presented are the simple average of 10 resistors from each experiment.

As shown in Table 1 and Fig. 2, the initial sheet resistivity of "thin" reactively sputtered Ta_2O_5/Ta films was strongly influenced by the substrate potential.

It should be mentioned that Lot 303 was deposited with the substrate holder electrically connected to the steel base plate of the vacuum system, (that is "shorted" to the anode of the glow-discharge).

For this particular sputtering system (Fig. 1), a substrate potential of about -20 volts dc yielded the widest range of sheet resistivities.

Using a substrate potential of -20 volts dc, reactively sputtered Ta_2O_5/Ta resistive films were deposited onto 5 silicon slices per run for various times, ranging from 10 to 50 minutes.

With the photomask used for earlier experiments[6], about 50 resistors were etched onto each slice.

Figure 3 is a summary of the resistance distribution for 250 resistors from each experiment.

The foregoing data were considered adequate basis for the decision to use -20 volts dc substrate potential for subsequent experiments.

(For example, a sputtering time of 10 minutes could be expected to deposit a film of 950 ohms/square to a tolerance of about ±10%).

Table 1

Effects of Substrate Potential on Sheet Resistivity

Sputtering Time, Minutes	Volts dc Lot No.	Sheet Resistivity, ohms/square -80 301	-20 302	"Shorted" 303	+20 304	+40 305
10		99	-	274	132	178
20		96	834	235	73	154
30		91	187	182	67	137
40		43	178	120	32	-
50		42	154	52	30	-

Thickness measurements[5] of the deposited films indicated that the range of resistivities obtained using substrate bias was due to changes in film composition, not merely due to different film thickness (Table 2).

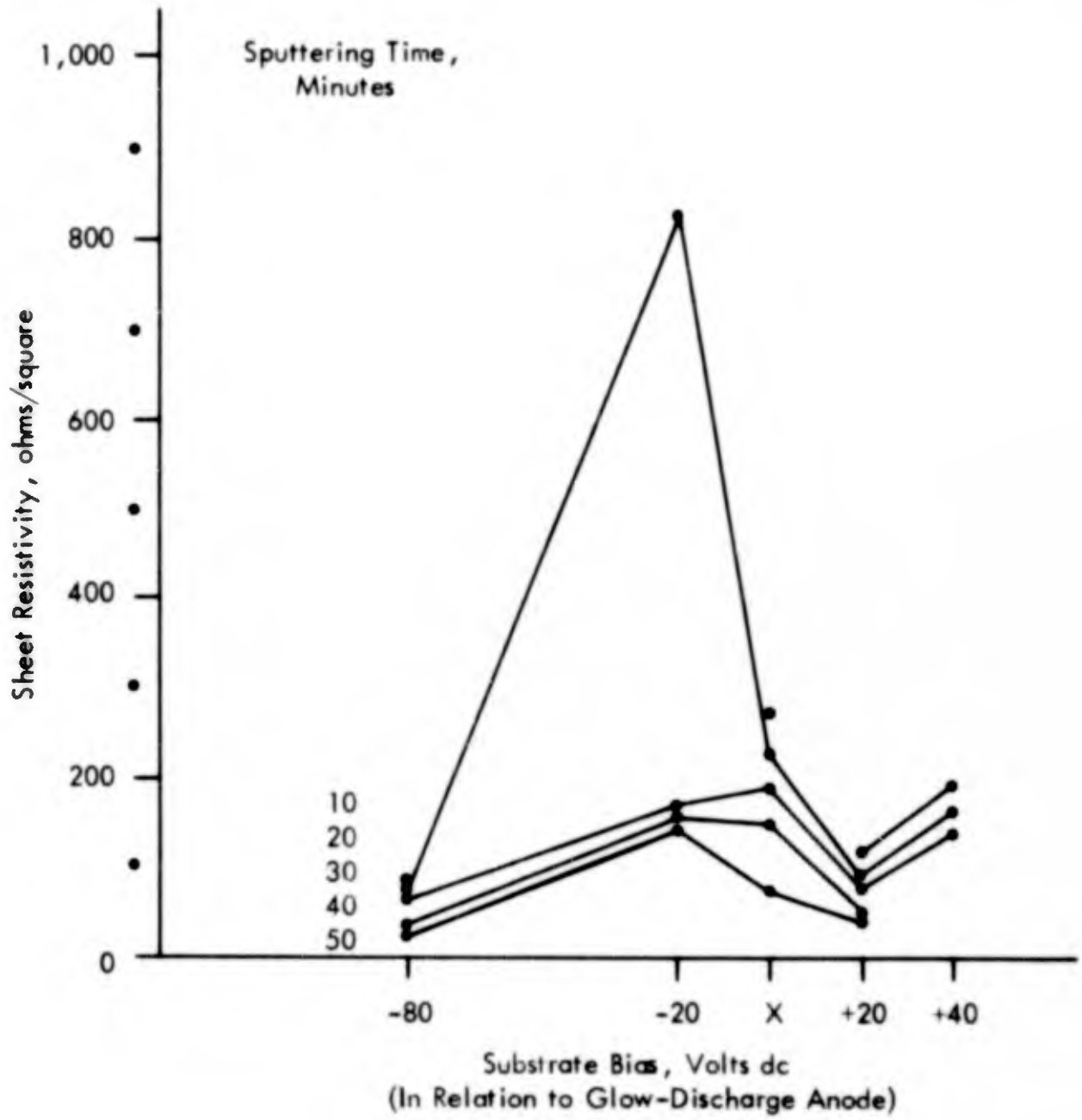


Fig. 2. Sheet Resistivity Altered By Substrate Potential

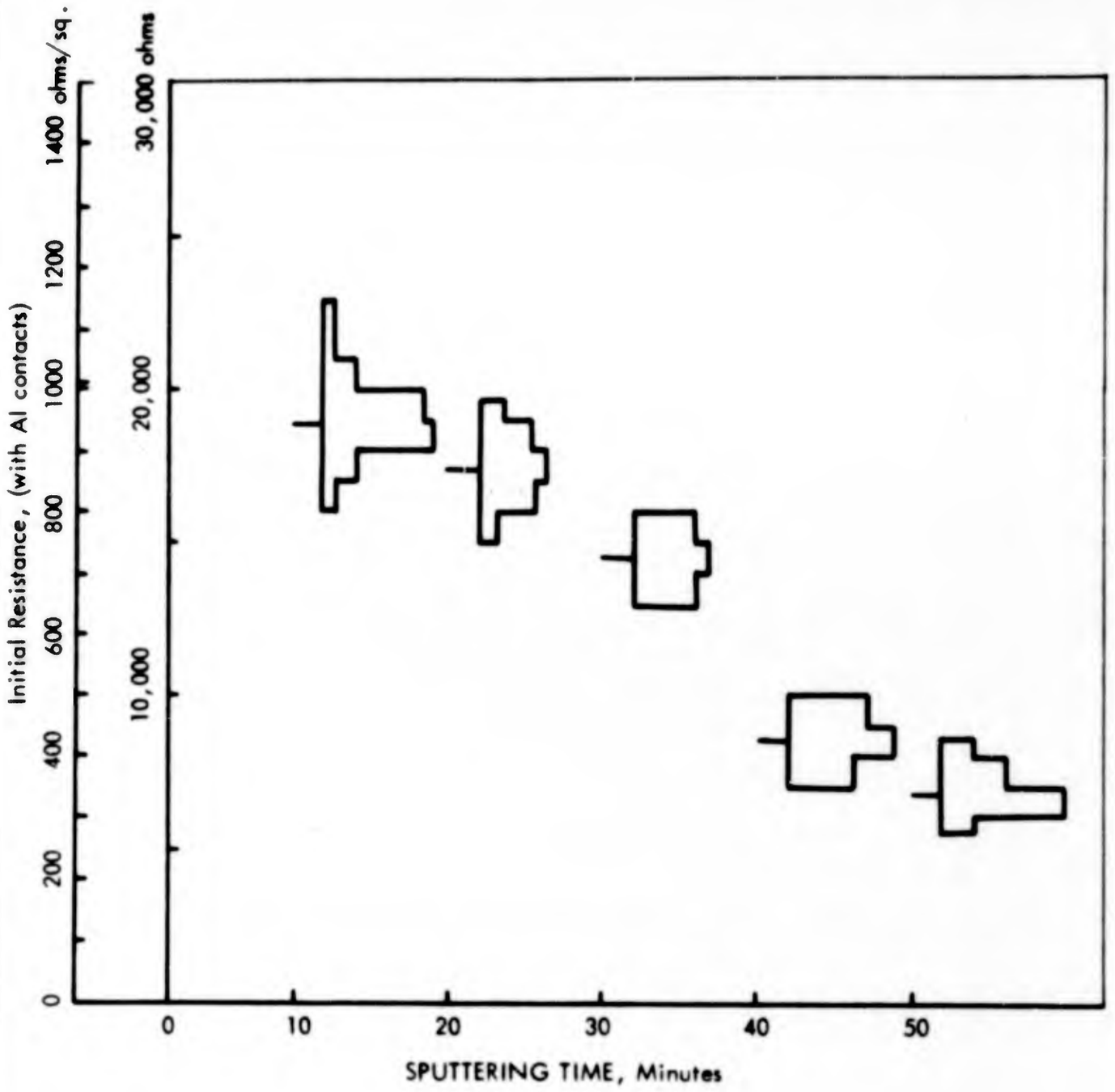
Table 2

Thickness of Resistive Films Deposited at

Various Times with Various Substrate Potentials

Sputtering Time, Minutes	Volts dc Lot No.	Thickness, micro-inches -80 301	-20 302	"Shorted" 303	+20 304	+40 305
10		21	-	22	20	19
20		38	37	41	39	40
30		61	63	61	59	58
40		81	83	87	80	79
50		111	103	107	108	106

The data in Table 2 indicate a deposition rate of about 2 micro-inches per minute.



Reactively Sputtered Ta_2O_5/Ta Films deposited with a substrate potential of -20 volts dc.

Fig. 3. Distribution of 250 Resistors from Each Sputtering Time

C. RESISTORS WITH SPUTTERED Ta_2O_5 SURFACE PROTECTION

Considerable time was spent during this quarter investigating the deposition of reactively sputtered Ta_2O_5 dielectric films onto the surface of reactively sputtered Ta_2O_5/Ta resistive films.

This technology is important for two reasons:

1. The dielectric films might serve as a surface protection for the resistive films.
2. In applying both resistive and dielectric films to form a resistor-capacitor circuit, it might be possible to deposit the resistive film over the entire substrate, etch to define resistors, apply metallic interconnections, deposit dielectric film over the entire substrate, apply metallic capacitor top plates and etch to define the interconnections, thereby utilizing the dielectric film for surface protection.

For most of the work described in this report, simple metal films of evaporated aluminum were used for resistor terminals, capacitor plates and all interconnections.

Reactively sputtered Ta_2O_5/Ta resistive films from 76 to 12,450 ohms per sq were covered with reactively sputtered Ta_2O_5 dielectric films ranging from 0.6 to 2.0 pF/mil^2, and the results are listed in Table 3.

In all data reported here, the mean, minimum and maximum values are presented for 10 samples from each experiment.

The data indicate the changes caused by coating resistive films with reactively sputtered Ta_2O_5 dielectric films. For example, Lot 501-1, 301 ohms/square film was changed about +3% when 2.0 pF/mil^2 dielectric film was sputtered onto it,

$$\frac{3100 - 3008}{3008} \times 100 = +3\%$$

but was changed about +16% when 0.6 pF/mil^2 dielectric was deposited.

This probably is due to the relative thicknesses of the resistive and dielectric films and oxidation of the resistive film during sputtering of dielectric films.

D. RESISTOR LIFE-TESTS

Reactively sputtered Ta_2O_5/Ta resistive films[7] ranging from 37 to 619 ohms/sq were etched to form simple, straight-line resistor patterns of 0.004 inches X 0.040 inches, then evaporated molybdenum-gold contacts were applied. After etching of the molybdenum-gold for contact area definition, the KTFR was removed using a xylol-containing solvent,* and the slices cleaned by a flush in deionized water and a flush in isopropyl alcohol.

The silicon slices were broken into rectangular chips 0.070 inches x 0.200 inches by the use of a diamond scribe and micrometer cross-feed table. Each chip contained one individual resistor element, as discussed above. At least 10 individual chips from each silicon slice were mounted onto TO-5 headers using a thermosetting epoxy resin.† Thermocompression ball bonding of 0.001 inch diameter gold wire to the molybdenum-gold contact tabs was achieved by heating to 300°C for 3 to 15 seconds. This temperature cycle also cured the epoxy resin adequately to provide firm support to the chip.

The resistors were sealed in room atmosphere by welding a nickel can to the TO-5 header.

Table 4 is a summary of the changes caused by the ball bonding operation.

*Resist Strip J-100 from IRC Laboratory, 811 South Sherman, Richardson, Texas 75082
†Bi Pax BP-2108 L/3 available from Tra-Con Inc., 25 Ship Avenue, Medford 55, Mass.

Table 3

Reactively Sputtered Ta_2O_5/Ta Resistive Films Coated with Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Sheet Resistivity Ohms/Square		Initial With Al Contacts	Resistance Values from 10 Samples Each Test, Ohms With Sputtered Ta_2O_5 on Surface Nominal Capacitance pF/mil^2			
				2.0	1.2	0.9	0.6
501-4		L	690	630	750	790	810
	76	M	765	672	817	887	851
		H	830	780	920	1060	890
501-1		L	2850	2950	3375	3225	3275
	301	M	3008	3100	3640	3415	3493
		H	3175	3400	3850	3825	3775
501-3		L	3675	4100	4400	5150	5100
	382	M	3823	4248	4640	5358	5430
		H	4350	4475	5000	5850	6200
501-2		L	96500	146000	149000	132000	91000
	12,450	M	124480	157100	164600	158900	110550
		H	180000	171000	196000	215000	160000

Table 4. Averages of 10 Resistors before and after Bonding

Lot	Resistance, Ohms Initial	After Bonding	% Change
101-5	361	367	+ 1.7%
101-4	536	543	+ 1.3%
101-3	675	689	+ 2.1%
101-2	2342	2367	+ 1.1%
101-1	6127	6189	+ 1.0%

These 10 resistors from each lot were life-tested in the following manner:

1. Measure resistance at +25°C
2. Place in +125 ±10°C over with a d-c voltage across the resistor, dissipating about 2.5 watts per square inch of resistor area.
3. After 250 hours, remove from oven, cool to +25°C, measure resistance.

Table 5 is a summary of this life-test data, the average of 10 resistors.

The resistors were reasonably stable during life test at +125°C, especially in view of the fact that the unprotected surfaces were exposed to can atmosphere.

Table 5. Life-test Data, Reactively Sputtered Ta_2O_5/Ta Resistors

Resistance, Ohms at 25°C, after test at 2.5 watts/in^2 D.C. and +125°C

Lot	Nominal Ohms/Square	Hours on Test 0	250	500	750	1000	Per Cent Change
101-5	37	367	368	369	370	370	+ 0.8%
101-4	54	543	545	545	546	547	+ 0.7%
101-3	69	689	689	691	691	693	+ 0.6%
101-2	237	2367	2368	2370	2371	2374	+ 0.3%
101-1	619	6189	6197	6218	6289	6307	+ 1.9%

SECTION IV
THIN FILM CAPACITORS

Work during this quarter was concerned with demonstration of yields for reactively sputtered Ta_2O_5 capacitors.

A. SUBSTRATE PREPARATION

All capacitor data in this report are results using evaporated aluminum for plates.

The capacitor electrodes were prepared in the following manner:

Thermally oxidized slices of single crystal silicon were cleaned as previously described (hot sulphuric acid, deionized water, isopropyl alcohol), then placed into a vacuum evaporator, evacuated below 5×10^{-5} Torr.

The slices were heated to 300 ±20°C then coated with approximately 20,000 Å of aluminum, evaporated from a tungsten filament.

Photo-resist techniques were used to form rectangular plates 0.035 inches by 0.045 inches.

B. FILM DEPOSITION, ASSEMBLY AND TESTING

1. Reactive Sputtering

The equipment shown in Fig. 4, consisting of a glass bell jar, steel base plate, silicone oil diffusion pump and a mechanical backpump was used. The work holder was a

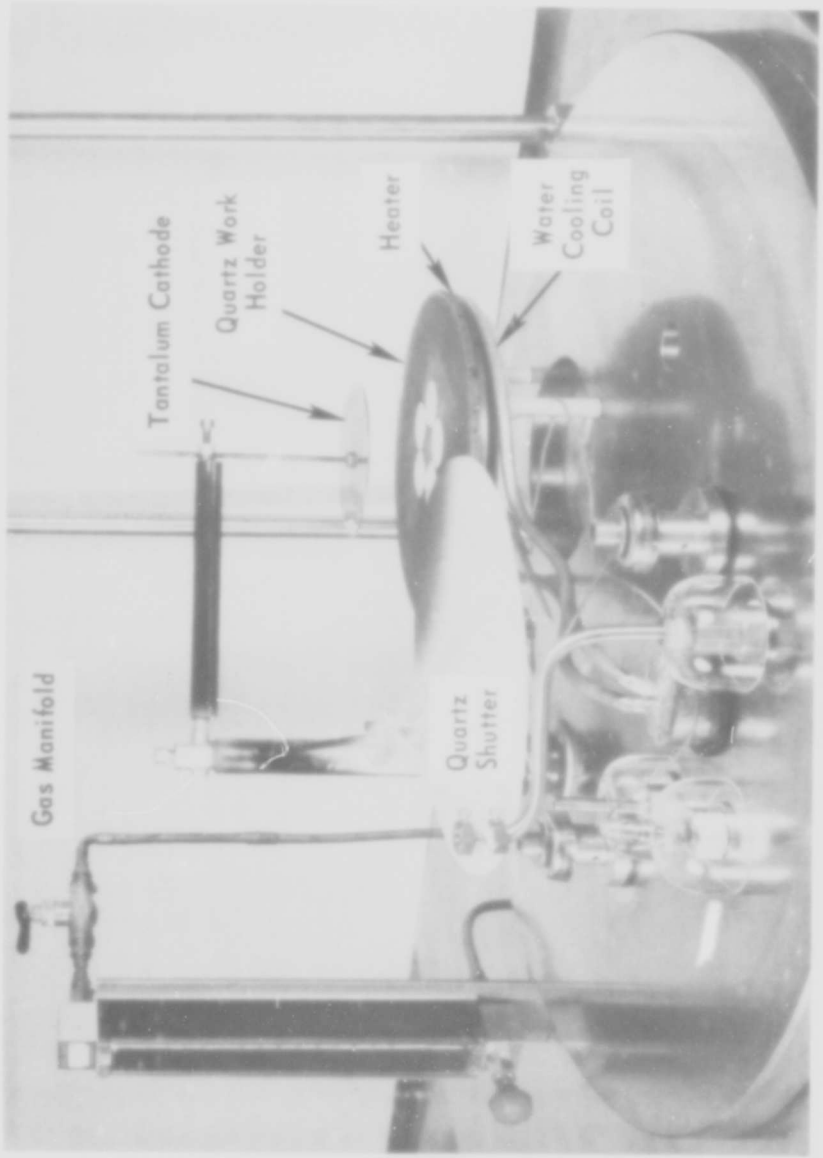


Fig. 4. Apparatus for Reactive Sputtering of Ta_2O_5 Dielectric Films

block of quartz. The steel base plate was connected to the plus terminal of a variable high voltage d-c power su . The cathode was a 3-1/2 inch diameter disc of 99.99+% tantalum. The spacing bet en the cathode and the silicon slices was 1 ± 1/4 inches. The bell jar was evacuated to 5×10^{-5} Torr, flushed with 40% argon-60% oxygen, and then evacuated for 3 cycles. Sputtering was performed at a current density of 0.5 mA per sq inch of tantalum at 1.6 Kv dc against a quartz shutter for 15 minutes before allowing the silicon slices to be exposed.

Pressure was regulated to 5×10^{-2} Torr of 40% argon-60% oxygen by adjustment of a baffle valve between the bell jar and the diffusion pump. After the desired sputtering time, the high vacuum valve was closed, and the reaction chamber filled to atmospheric pressure with 40% argon-60% oxygen.

2. Capacitor Assembly

The top electrodes were prepared by evaporation of aluminum as described and the excess metal removed by the same selective etching techniques.

Using photoresist methods, a small hole was etched through the dielectric film using an etch of 1 volume % HF and 1 volume water, to provide access to the bottom electrode.

After scribing and breaking into individual chips containing one or two capacitors, the chips were mounted on a TO-5 header using a thermosetting epoxy resin,* which is cured during the 5 to 10 seconds at 300°C required to make a ball-bond contact to the electrode tabs.

3. Testing

Capacitance and dissipation factor were measured at 1 Kc using a General Radio 1650-A Impedance Bridge.

* Resist Strip J-100 from IRC Laboratory, 811 South Sherman, Richardson, Texas, 75082

Destructive breakdown voltage was then measured using a Tektronix 575 Transistor Curve Tracer with an internal impedance of one ohm.

C. RANGE OF CAPACITANCE VALUES

On the basis of recent findings,[8] the use of a heated (+125°C) substrates appears to increase capacitor breakdown voltage with little change in capacitance.

Using the equipment shown in Fig. 4, five consecutive lots of capacitors were deposited. Table 6 is a summary of the high, mean and low values for 10 capacitors from each log. Photo-resist problems were encountered with Lot 403. Otherwise, the capacitance reproducibility was good.

D. DEMONSTRATION OF CAPACITOR YIELDS

For several development hybrid/silicon monolithic circuits at Texas Instruments Incorporated, thin film capacitors are being considered.

Reactively sputtered Ta_2O_5 dielectric films of 0.5 pf/mil^2 are of special interest.

Table 7 is an analysis of data from recent efforts to make 0.5 pf/mil^2 capacitors having a breakdown voltage greater than 18 volts dc.

Four consecutive sputtering runs, containing 5 silicon slices each, were performed using the equipment shown in Fig. 4.

Control of sputtering conditions to produce 3.0 pf/mil^2 capacitors is lacking, as indicated by results in Table 8.

As listed in Table 8, control of the average capacitance was poor, ranging from 1.2 pf/mil^2 to 5.9 pf/mil^2. However, the dissipation factor and breakdown voltage

results were encouraging. Specifically, the breakdown voltage was greater than 6 VDC, and dissipation factor was less than 0.050 for all samples tested.

Capacitance changed about +10% during the first 250 hours storage at +125°C, but remained essentially stable between 250 and 500 hours.

E. CAPACITOR LIFE-TESTS

In a prior report[9] of this contract, an arbitrary dc voltage rating of 60% of the average destructive breakdown voltage was found to be possible at +125°C.

Capacitors having 0.035 inch by 0.045 inch evaporated aluminum electrodes were sealed in TO-5 cans in room ambient conditions.

Ten capacitors from each lot were measured at 25°C using the General Radio 1610-A Capacitance Measuring Assembly.

The capacitors were then placed in an oven at 125 ±10°C with a 1000 ohm ±5% resistor in series with each. A steady d-c voltage was applied during life-test.

The capacitors were removed after each 250 hours, allowed to cool over night, then measured at 25°C.

Table 9 is the data from 10 capacitors from each lot.

This arbitrary rating of 60% of breakdown voltage for 125°C operation was proven to be practical, and the capacitance change was found to be less than 2% after 1000 hours.

Table 6. Capacitance Values from 5 Consecutive Lots of Ta_2O_5 Capacitors

Sputtering Time, Minutes		Capacitance, pf, from 10 Samples from 5 Consecutive Lots						pf/Mil^2
		401	402	403	404	405		
30	H	2625	2975	-	2375	3025	2480	1.57
	M	2530	2500	-	2133	2750		
	L	2400	2250	-	1940	2350		
60	H	1570	1710	-	1220	2010	1571	1.00
	M	1560	1650	-	1175	1905		
	L	1550	1610	-	1140	1820		
90	H	1280	1260	1330	-	1310	1209	0.77
	M	1146	1148	1278	-	1265		
	L	1075	1080	1240	-	1220		
120	H	950	1030	-	1050	1130	1010	0.64
	M	949	1024	-	1014	1056		
	L	945	1020	-	960	1000		
150	H	770	-	-	770	770	759	0.48
	M	762	-	-	761	754		
	L	760	-	-	750	730		

Table 7. Yield Distribution of
0.5 pf/mil^2 Capacitors

Lot	Capacitance pf/mil^2	D.f. at 1 Kc	Breakdown Vdc
MP10	0.60	0.001	51
MP11	0.56	0.001	51
MP12	0.62	0.003	35
MP13	0.48	0.001	50
Total 960 Capacitors	0.55	0.002	47

64% yield within ±20% of 0.5 pf/mil^2
and breakdown voltage greater than 18 vdc.

Table 8. Data from 10 Consecutive Lots,
Ta_2O_5 Capacitors of 3 pf/mil^2

		Average of 10 Units				Average of 5 Units, after Storage at +125°C	
						250 Hrs.	500 Hrs.
Lot	Slice	C, pf	pf/mil^2	Df	V_{bd}	C, pf	C, pf
210-	1	4750	3.015	0.013	6	4845	4845
	2	6670	4.235	0.025	6	4650	4630
	3	3245	2.060	0.037	8	3174	3163
	4	4049	2.571	0.030	7	4140	4165
	5	5050	3.206	0.006	9	4840	4835
211-	1	4570	2.901	0.008	8	4530	4575
	2	6124	3.888	0.027	7	5790	5820
	3	4550	2.889	0.009	6	4335	4335
	4	4795	3.044	0.010	8	4491	4525
	5	4380	2.781	0.019	6	4615	4640
212-	1	4040	2.565	0.031	12	4105	4080
	2	4580	2.908	0.030	8	4675	4670
	3	3365	2.137	0.025	9	3515	3480
	4	2428	1.542	0.010	9	2305	2300
	5	5785	3.673	0.014	7	5540	5535
213-	1	3620	2.298	0.028	6	3555	3530
	2	2900	1.841	0.016	11	2920	2885
	3	2112	1.341	0.004	7	2180	2175
	4	4159	2.641	0.033	9	3715	3695
	5	3714	2.358	0.033	10	3530	3485
214-	1	6160	3.911	0.032	11	6070	6085
	2	2755	1.749	0.013	8	2700	2700
	3	5619	2.568	0.012	15	5445	5455
	4	4133	2.624	0.031	12	4215	4205
	5	3065	1.946	0.020	12	3558	3500

Table 8. (Continued)

		Average of 10 Units				Average of 5 Units, after Storage at +125°C	
						250 Hrs.	500 Hrs.
Lot	Slice	C, pf	pf/mil^2	Df	V_{bd}	C, pf	C, pf
215-	1	5385	3.419	0.034	10	5175	5230
	2	5108	3.243	0.017	9	4855	4925
	3	4965	3.152	0.079	7	4665	4685
	4	9420	5.981	0.041	12	5415	5430
	5	6020	3.822	0.046	13	6010	6000
216-	1	4572	2.903	0.030	17	4395	4390
	2	6490	4.121	0.030	7	6065	6040
	3	4414	2.803	0.040	7	3715	3690
	4	5230	3.321	0.020	12	4890	4865
	5	4395	2.790	0.030	13	3865	3815
217-	1	3005	1.908	0.014	12	2865	2855
	2	5180	3.289	0.035	11	4431	4381
	3	3980	2.527	0.026	7	3760	3750
	4	3162	2.008	0.018	9	3410	3365
	5	3023	1.919	0.048	9	3010	3020
218-	1	1908	1.211	0.004	9	2187	2177
	2	2253	1.430	0.011	9	2615	2555
	3	2737	1.738	0.033	11	2675	2620
	4	1915	1.216	0.004	7	3020	3020
	5	2345	1.489	0.020	10	2640	2630
219-	1	2405	1.527	0.006	8	2375	2360
	2	2430	1.543	0.006	9	2525	2525
	3	2430	1.543	0.009	8	2795	2825
	4	4303	2.732	0.037	10	4060	4080
	5	5460	3.467	0.025	7	5865	5920

Table 9. Capacitor Life-test Data

Average from 10 Units					Average Capacitance, pf, 10 Units after +125°C and 60% V_{bd}					
					Hours on Test					
Lot	C, pf	Df	V_{bd}	pf/mil^2	0	250	500	750	1000	Per Cent Change
107-5	1015	0.017	45	0.64	1012	1002	1001	997	996	-1.6%
107-4	1136	0.021	35	0.72	1133	1127	1125	1123	1120	-1.1%
107-3	1569	0.030	30	0.98	1567	1560	1557	1555	1553	-0.9%
107-2	3367	0.036	17	2.13	3360	3347	3345	3343	3340	-0.6%
107-1	4990	0.041	8	3.16	4987	4932	4928	4922	4917	-1.4%

SECTION V
RESISTIVE AND DIELECTRIC FILMS ON THE SAME SUBSTRATE

Most of the prior work under this contract was concerned with exploring the range of values, characteristics, and deposition controls for either resistive or dielectric films.

During this seventh quarter, considerable progress has been achieved in developing methods for the deposition of resistive, dielectric and conductive films onto thermally oxidized silicon to form resistor-capacitor networks. For most of this work, evaporated aluminum was used for the conductive film. For special circuits, subject to elevated temperature cycles, a multilayer metal interconnection scheme might be better than aluminum.

There are three basic sequences for using sputtered resistive films, evaporated metal films and sputtered dielectric films on the same substrate.

A. USE OF A REVERSE METAL MASK

This method is the most complicated, involving many process steps and many photomasks:

1. Evaporate aluminum over entire substrate, use photo-resist techniques for selective metal removal from resistor areas.

2. Reactively sputter Ta_2O_5/Ta resistive film over entire substrate.

3. Dip the substrate into a dilute phosphoric acid or dilute sodium hydroxide etch, which will remove the aluminum and lift off the resistive film from unwanted areas.

4. Evaporate aluminum over entire substrate, followed by photo-resist etching to define resistor contacts, interconnections and lower plates for capacitors.

5. Reactively sputter Ta_2O_5 dielectric films.

6. Evaporate aluminum, followed by photo-resist etching to define upper plates for capacitors.

7. Selective etch through dielectric to provide access to lower plates of capacitor.

Direct photo-resist definition of reactively sputtered Ta_2O_5/Ta resistive films was found to be better than using an evaporated aluminum reverse mask, as the resistance distributions in Table 10 indicate.

B. RESISTIVE FILMS COATED WITH DIELECTRIC FILM

This method requires fewer process steps and provides surface protection for the resistors.

1. Reactively sputter Ta_2O_5/Ta resistive film over entire substrate.

2. Use photo-resist etching to define resistor patterns.

3. Evaporate aluminum, etch to define resistor contacts, interconnections and lower plates for capacitors.

4. Reactively sputter Ta_2O_5 dielectric film over entire substrate.

5. Evaporate aluminum, followed by photo-resist etching to define upper plates of capacitors.

6. Selective etching through dielectric to provide access to lower plates of capacitor.

Results from this method were presented in Table 3 of this report. It should be noted that the resistive films are altered by sputtering of the dielectric layer. For example, Lot 501-1, initially 301 ohms/sq was increased to about 350 ohms/sq when thick Ta_2O_5 dielectric films were deposited to 0.6 pf/mil^2.

No problems have been evident with the capacitors made by this method.

C. DIELECTRIC FILM COVERED WITH RESISTIVE FILM

This method is the least complicated in terms of the number of photomasks required, but requires very careful attention to the photo-resist operations.

1. Evaporate aluminum, etch to define lower plates for capacitors.

2. Reactively sputter Ta_2O_5 dielectric film.

3. Reactively sputter Ta_2O_5/Ta resistive film.

4. Selective etching to define resistor area and capacitor area.

5. Evaporate aluminum, followed by photo-resist etching to define resistor contacts, interconnections and upper plates for capacitors. (Other evaporated metals, such as molybdenum-gold could be used).

At the time of writing this report, only one experiment was completed using this sequence of operations, and the data are in Table 11.

Table 10. Data from Ta_2O_5/Ta Resistors Defined by Photo-resist Etching and by Reverse Metal Masks

Lot (10 Resistors from 1 slice each experiment)		Initial Resistance, Ohms for 4 Mil x 40 Mil Resistors	
		Using KTFR Mask (Remove unwanted Ta_2O_5/Ta with $HF/HNO_3/HA_c/H_2O$)	Aluminum Masks (Remove Al with hot NaOH)
601	L	743	731
	M	754	759
	H	762	782
602	L	1296	1127
	M	1360	1370
	Hi	1372	1410
603	L	5673	5467
	M	5980	6012
	H	6213	6427

Table 11. Data from Dielectric Films Covered with Resistive Films
(10 Units Each Experiment)

Lot		C, pf	Df	V_{bd}
		Capacitors, 1575 mil^2 with Mo-Au Plates		
904	L	700	0.007	47
	M	760	0.009	58
	H	820	0.014	69
		Capacitors, 1575 mil^2 with 160 ohms/square Ta_2O_5/Ta between Dielectric and Mo-Au Plates		
904Z	L	680	0.008	40
	M	745	0.012	53
	H	810	0.016	62
		Resistors, 4 x 40 mils with Mo-Au Contacts R, Ohms		
	L	1620		
	M	1660		
	H	1700		

SECTION VI
CONCLUSIONS — PROJECT TO-DATE

A. RESISTIVE FILMS

Reactively sputtered Ta_2O_5/Ta resistive films deposited onto thermally oxidized silicon offer a very wide range of sheet resistivity values.

Many of the process variables of reactive sputtering have been investigated to determine methods for controlling sheet resistivity.

During this seventh quarter, substrate bias sputtering was found to cause changes in film resistivity for a given film thickness, therefore, implying that the film composition was different under substrate potentials.

Resistor load life tests at +125°C and 2.5 watts per sq inch were completed in which resistance change after 1000 hours was less than 1% for films of 37 to 69 ohms per sq.

Films of 237 ohms per square changed +3% and 619 ohms/per sq films were unstable under these life test conditions.

B. DIELECTRIC FILMS

During the last several months of this contract, significant improvements have been demonstrated for reactively sputtered Ta_2O_5 dielectric films.

The sputtering variables of substrate temperature, cathode current density, gas composition and flow rate have been explored to develop a practical capacitor process.

The yields from consecutive runs for 0.5 pf/mil^2 and 3 pf/mil^2 were encouraging.

For example, in an attempt to make a large quantity of capacitors to a target of 0.5 pf/mil^2, 64% of the capacitors were within ±20% of this capacitance, and had a breakdown voltage greater than 18 volts dc.

Capacitor life tests at +125°C with an arbitrary 60% of the destructive breakdown voltage applied resulted in less than 2% capacitance change after 1000 hours.

C. INTERCONNECTION METALS

Evaporated aluminum films were found to be a suitable metal for resistor contacts, capacitor electrodes and interconnecting leads. However, for use with diffused silicon active devices, a sandwich of a refractory metal and gold would be desirable to provide a gold surface for bonding gold wires.

Processing sequences have been demonstrated for the application of resistive films, dielectric films and aluminum interconnections to form resistor-capacitor networks on silicon oxide.

SECTION VII
PROGRAM FOR EIGHTH QUARTER

Reactively sputtered Ta_2O_5/Ta resistive films of 200 ohms per sq and reactively sputtered Ta_2O_5 dielectric films of 0.35 pF/mil^2 are being designed into a thin-film R-C active filter for use with a diffused silicon 455 KC IF amplifier.

The composite circuit will contain 14 diffused silicon planar transistors, 17 diffused resistors, 5 reactively sputtered Ta_2O_5/Ta resistors, 3 reactively sputtered Ta_2O_5 capacitors, and evaporated metal interconnections.

Figure 5 is the schematic diagram of the amplifier circuit and the thin film R-C filter.

The entire circuit represented by Fig. 5 is being designed to be manufactured using reactively sputtered thin tantalum films deposited onto the oxidized silicon slice containing the diffused amplifier circuit.

Figure 6 is a composite layout of the entire circuit, which will be a silicon chip 0.070 inches by 0.170 inches.

In preparation for the processing of this demonstration circuit, resistive films, dielectric films and evaporated metal interconnections are being investigated using the sequence listed in Section V-B of this report.

The photomasks for the diffused amplifier portion will use existing designs. The only new masks required are for interconnections and for the tantalum R-C filter.

The circuit is of immediate practical use for 455 KC IF stages of superheterodyne AM receivers.

Work on the fabrication of the composite circuit shown in Fig. 6 will begin about May 1, 1965. Functional sample quantities of packaged circuits are expected before the preparation of the final report which is due July 31, 1965.

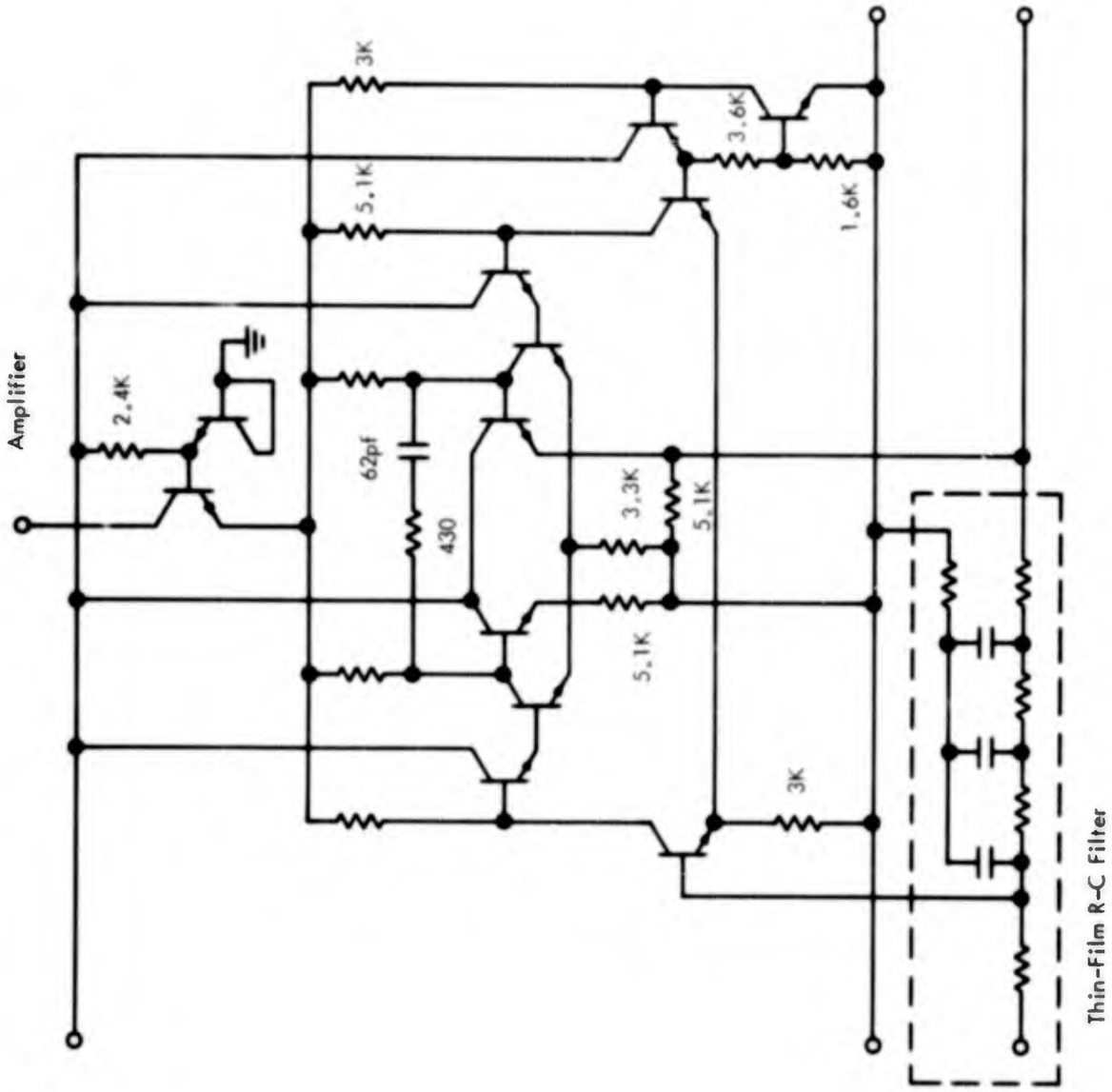
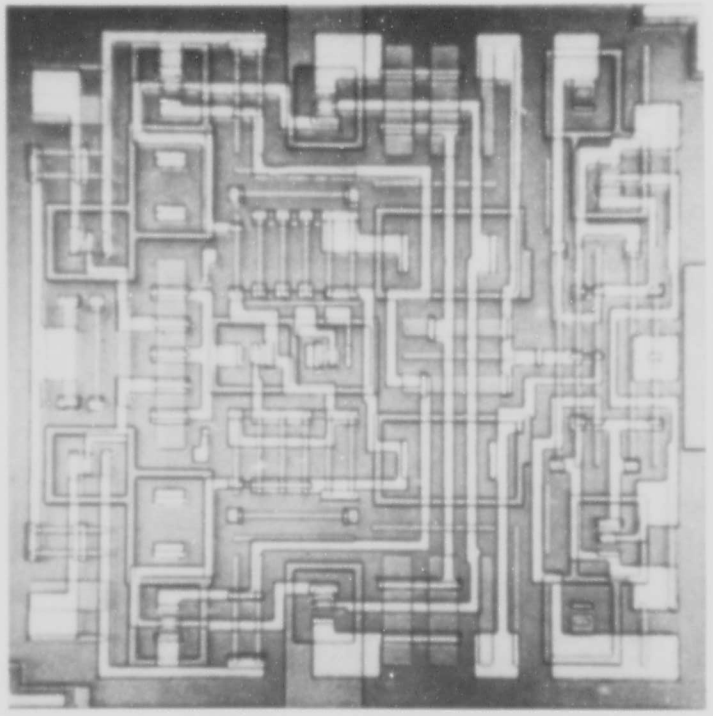


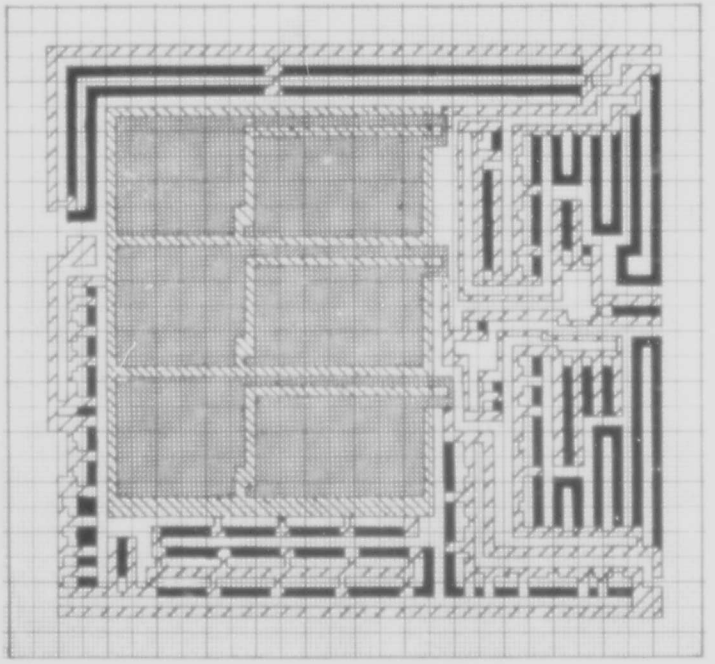
Fig. 5. Schematic Diagram of a Hybrid/Monolithic 455 KC IF Amplifier Circuit

Diffused Silicon Amplifier



Size 0.070" X 0.170"
14 Transistors
17 Diffused Resistors

Reactively Sputtered Tantalum R-C Filter



5 Resistors 200 ohms/square
3 Capacitors 0.35 pF/mil^2

Fig. 6. Composite Layout of a Hybrid/Monolithic 455 KC IF Amplifier

SECTION VIII
PERSONNEL

A. MAN-HOURS

During the period 1 December 1964 through 28 February 1965, the following Texas Instruments employees performed work for this contract:

	Hours
Mr. Coy D. Orr	528.5
Dr. James A Cunningham	*
Dr. Jay W. Lathrop	*

B. BIOGRAPHIES OF TECHNICAL PERSONNEL

ORR, COY D. Project Engineer, Semiconductor Network Technology Group, Semiconductor Research & Development Laboratory

B.A. in Chemistry, Texas Technological College, 1953

Mr. Orr was assigned as Project Engineer of this contract in December 1963. Mr. Orr brings to the project over seven years experience at Texas Instruments in the design, development, and manufacture of tantalum electrolytic capacitors. Mr. Orr has published work on tantalum capacitors in the National Electronics Conference (1958) and on silicon oxide capacitors in the Proceedings of the IEEE (1961).

Member: Electrochemical Society, Institute of Electrical and Electronic Engineers, American Vacuum Society

*Not directly charged to the contract

CUNNINGHAM, JAMES — Section Leader, Fabrication, Thin Films and Packages, Semiconductor Network Technology Group, Semiconductor Research and Development Laboratory

Ph.D., in Inorganic Chemistry, University of Texas, 1961
M.A. in Physics and Chemistry, University of Texas, 1958
B.A. in Chemistry, University of Texas, 1957

Dr. Cunningham joined Texas Instruments in 1961 as Group Leader in the Surface Studies Branch. He is currently assigned to the Semiconductor Research and Development Laboratory, where his work is in integrated circuit fabrication. During the summers of 1956 and 1957, Dr. Cunningham was employed in the Chemistry Laboratory at Convair, Fort Worth. Dr. Cunningham has published in Electrochem. Tech. and J. Electrochem. Soc., and was recipient of "Young Authors Award for 1963," sponsored by the Electrochemical Society for the above paper. He also has several patent applications pending.

Member: Phi Lambda Upsilon, Sigma Xi, Electrochemical Society

LATHROP, J.W. — Manager, Semiconductor Network Technology Group, Semiconductor Research and Development Laboratory

Ph.D. in Physics, Massachusetts Institute of Technology, 1952
M.S. in Physics, Massachusetts Institute of Technology, 1949
B.S. in Physics, Massachusetts Institute of Technology, 1948

A member of the technical staff since 1958, Dr. Lathrop is responsible in the Semiconductor Research and Development Laboratory for the direction of programs concerned with slice processing, assembly techniques, package development, thin film technology and photomask fabrication. Prior to joining the R&D Laboratory, he directed the semiconductor network technology development in the Integrated Circuits Department. Previously, he was a senior engineer in the Device Electronics Branch of the Research and

Engineering Department where he was responsible for the development of photolithographic and oxide masking techniques applied to diffused silicon transistors and for device structure investigation. From 1953 to 1958 Dr. Lathrop was employed by the Diamond Ordnance Fuze Laboratories, Washington, D.C. where he conducted research and development work on semiconductor devices applicable to 2D techniques. He was a member of the five-man team awarded the Department of Army Civilian Meritorious Award in 1959 for the development of integrated circuits. Dr. Lathrop is author of numerous papers and articles for technical publications.

Member: American Physical Society, Sigma Xi, Electrochemical Society

APPENDIX

BIBLIOGRAPHY

1. C.D. Orr, "Thin Films Formed by Electrochemical Reactions," Report No. 6, Contract DA36-039-AMC-02324(E), January 1965, pp. 21-30.

2. F. Vratny, N. Schwartz, "Deposition of Tantalum Films by Substrate-Electrode Bias Sputtering," J. Vac. Science and Tech. Vol. 1, No. 2, pp. 79.

3. L. I. Maissel, P.M. Schaible, "Bias Sputtering," J. Appl. Physics, Vol. 36, No. 1, Jan. 1965, pp. 237-242.

4. Ref. 1, pp. 10-15.

5. N. Schwartz, R. Brown, "A Stylus Method for Evaluating the Thickening of Thin Films and Substrate Surface Roughness," 1961 Trans. American Vacuum Society, Vol. II, pp. 842-846.

6. Ref. 1, pp. 11-12.

7. C.D. Orr, "Thin Films Formed by Electrochemical Reactions," Report No. 5, Contract DA36-039-AMC-02324(E), Sept. 1964, p. 22.

8. Ref. 1, p. 39.

9. R.S. Clark, C.D. Orr, "Thin Films Formed by Electrochemical Reactions," Report No. 4, Contract DA36-039-AMC-02324(E), June 1964, pp. 97-98.